SiGe BASED MULTIPLE-PHASE VCO OPERATING FOR MM-WAVE FREQUENCIES

by

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SUMMARY

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Keywords: Voltage-controlled oscillator (VCO), millimetre-wave (mm-wave), silicon germanium (SiGe), heterojunction bipolar transistor (HBT), Colpitts oscillator, phase noise, impulse sensitivity function, phased arrays, vector sum, hybrid coupler, variable gain amplifier (VGA), Gilbert mixer, integrated circuit (IC)

The ever-increasing demand for higher speed in wireless consumer applications has increased the interest in the unlicensed spectrum of 7 GHz around 60 GHz. The high atmospheric oxygen absorption at 60 GHz and small size of the antennas at this frequency requires the use of integrated phased-array systems to overcome the deficiencies of lossy channels at these frequencies. The phased arrays combine signals from multiple paths to obtain higher receiver sensitivity and directivity. The system thus requires phase-shifted voltage-controlled oscillator (VCO) signals to implement phase shifting in the local-oscillator (LO) path.

In this research, the vector sum method to generate various phases of the signal at 60 GHz was investigated for its suitability in phased-array systems. The main focus was on improving the phase noise performance of the VCO. The VCO was implemented using a fully differential common-collector Colpitts oscillator in the cascode configuration, which

was found to be the VCO configuration with acceptable phase noise performance and stability in the millimetre-wave range.

The research focus was on modelling the phase noise of the VCO, and was performed by identifying the impulse sensitivity function for various noise sources, followed by analysing its effect on the linear time varying (LTV) model of the oscillators. The analysis led to a closed-form expression for the phase noise of the oscillator in terms of process and design parameters. The design was then optimised in terms of identified parameters to attain minimum phase noise. The phase noise expression using LTV theory and SpectreRF simulations reported the same optimum value for the design parameter, of around 0.3 for the capacitor ratio.

The simulation results utilising the vector sum phase shifting method to generate multiple phase oscillator signals suggest its suitability in implementing phased-array systems in the millimetre-wave range. The vector sum was realised by generating quadrature signals from the oscillator using hybrid couplers. Variable gain amplifiers (VGAs) based on Gilbert mixer topology were used to combine the in-phase and quadrature phase signals to generate the phase-shifted oscillator signal. The gains of the VGAs were linearised by using a pre-distortion circuit, which was an inverse `tanh` cell.

A fully differential 60 GHz VCO was fabricated using a SiGe process with a f_T of 200 GHz. The fabricated integrated circuit (IC) measured at the wafer level had a centre frequency of 52.8 GHz and a tuning range of 7 GHz. It demonstrated a phase noise performance of -98.9 dBc/Hz at 1 MHz offset and a power dissipation of 140 mW, thus providing a VCO figure of merit of 172 dBc/Hz. It delivered a differential output power of 8 dBm and the IC occupied an area of 0.54 mm^2, including the bondpads. It was thus concluded that a 10% design margin for the tuning range is required while using SiGe BiCMOS technology.

The simulation results demonstrate that the VCO, along with an active interpolator, provides a range of phase-shifted signals from 0° to 360° in steps of 22.5° for various gain settings of the VGAs. The power dissipation of the active interpolator is around 60 mW and the system could thus be employed in LO path shifting architecture of the phased arrays with increased power consumption.

OPSOMMING

SiGe-GEBASEERDE VEELVULDIGEFASE-VCO WAT FUNKSIONEER VIR MM-GOLFFREKWENSIES

deur

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Sleutelwoorde: Spanningsbeheerde ossillator (VCO), millimetergolf (mm-golf), silikon-germanium (SiGe), heterovoegvlak bipolêre transistor, Colpitts-ossillator, faseruis, impulssensitiwiteitsfunksie, gefaseerde rangskikking, vektorsom, hibried-koppelaars, verstelbare wins versterker (VGA), Gilbert-menger, geïntegreerde stroombaan

Die steeds toenemende vraag na hoër spoed in draadlose verbruikerstoepassings het die belangstelling in die ongelisensieerde 7 GHz spektrum rondom 60 GHz verhoog. Die hoë atmosferiese suurstof absorpsie by 60 GHz en klein dimensies van die antennas by hierdie frekwensie benodig die gebruik van geïntegreerde gefaseerde rangskikkingsisteme om die tekortkomings van verliesige kanale by hierdie frekwensies die hoof te bied. Die gefaseerde rangskikkingsisteme kombineer seine van veelvuldige kanale om beter ontvangersensitiwiteit en -gerigtheid te verkry. Die sisteem vereis dus faseverskuifde spanningsgekontroleerde ossillatorseine om faseverskuiwing in die plaaslike ossillator te implementeer.

In hierdie navorsing is die vektorsommetode geïmplementeer om verskeie fases van die sein by 60 GHz op te wek en te ondersoek, om die geskiktheid daarvan vir gefaseerde rangskikkingsisteme te bepaal. Die hoofklem was op die verbetering van die faseruiswerksverrigting van die spanningsbeheerde ossillator (VCO). Die VCO is geïmplementeer deur gebruik te maak van ’n ten volle differensiële gemene kollektor

Colpitts-ossillator in die kaskodekonfigurasie, wat geblyk het om die VCO-konfigurasie met aanvaarbare faseruiswerkverrigting en stabiliteit in die millimetergolfbereik te wees.

Die fokus van die navorsing was op die modellering van die faseruis van die VCO en dit is uitgevoer deur die impulssensitiwiteitsfunksie van verskeie ruisbronne te identifiseer, waarna die effek daarvan op die liniêre tydwisselende model van die ossillators geanaliseer is. Die ontleding het gelei tot ’n geslotevormuitdrukking vir die faseruis van die ossillator ingevolge proses- en ontwerpsparameters. Die ontwerp is daarna geoptimeer kragtens geïdentifiseerde parameters om die minimum faseruis te behaal. Die faseruisuitdrukking wat liniêre tydwisselingsteorie en SpectreRF simulasies gebruik het, het dieselfde optimumwaarde van ongeveer 0.3 vir die kapasitorverhouding bevestig.

Die simulasieresultate tydens die gebruik van die vektorsomfaseverskuiwingsmetode om veelvuldigefase-ossillatorseine te genereer, dui die geskiktheid daarvan aan vir gebruik in gefaseerde rangskikkingsisteme in die millimetergolfbereik. Die vektorsom is bereik deur die opwekking van kwadratuurseine van die ossillator deur die gebruik van hibried-koppelaars. Verstelbare wins versterkers (VGAs) gebaseer op Gilbert-mengertopologie is gebruik om die infase- en kwadratuurfaseseine te kombineer om die faseverskuifde ossillatorsein op te wek. Die versterking van die VGAs is gelineariseer deur die gebruik van ’n opsetlike vervormingsbaan, naamlik ’n omgekeerde `tanh`-sel.

’n Ten volle gedifferensieerde 60 GHz VCO is vervaardig deur gebruik te maak van ’n SiGe BiCMOS-proses met ’n f_T van 200 GHz. Die geïntegreerde stroombaan wat vervaardig is, gemeet op vlokkie-vlak, het ’n sentrale frekwensie van 52.8 GHz asook ‘n instem-omvang van 7 GHz gehad. Dit het ’n faseruiswerksverrigting van -98.9 dBc/Hz gespesifiseerd by 1 MHz afwyking en kragverbruik van 140 mW gelewer, en dus ’n VCO-gevoeligheidskonstante van 172 dBc/Hz. Dit het ’n differensiële uitsetkrag van 8 dBm gelewer en die geïntegreerde stroombaan het ’n oppervlakte van 0.54 mm^2 op die vlokkie beslaan, insluitende die verbindingstukke. Daar is dus tot die gevolgtrekking gekom dat ’n 10 %-ontwerpstoleransie vir die instemgebied vereis word as SiGe BiCMOS-tegnologie gebruik word.

Die simulasie resultate toon dat die VCO, saam met ’n aktiewe interpoleerder, ’n omvang van faseverskuifde seine van 0° tot 360° lewer in stappe van 22.5° vir verskeie versterkerstellings van die VGAs. Die kragverlies van die aktiewe interpolator is ongeveer

60 mW en die stelsel kan dus met verhoogde drywingsgebruik in die plaaslike ossillator-baanverskuiwingsargitektuur van die gefaseerde rangskikkings aangewend word.

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LIST OF ABBREVIATIONS

ADE	Analog Design Environment
BEOL	Back-end-of-line
BiCMOS	Bipolar and CMOS
BJT	Bipolar junction transistor
CMOS	Complementary metal oxide semiconductor
CBE	Collector-base-emitter
CBEBC	Collector-base-emitter-base-collector
DAC	Digital-to-analogue converter
DC	Direct current
DUT	Device under test
EM	Electromagnetic
FET	Field effect transistor
FOM	Figure of merit
GaAs	Gallium arsenide
GBP	Gain-bandwidth product
GSG	Ground-signal-ground
HBT	Heterojunction bipolar transistor
IC	Integrated circuit
IF	Image frequency
InP	Indium phosphate
I/O	Input / output
ISF	Impulse sensitivity function
LO	Local oscillator
LVS	Layout versus schematic
LTI	Linear time-invariant
LTV	Linear time-varying
MEP	MOSIS educational program
MIM	Metal-insulator-metal
MMIC	Monolithic microwave integrated circuit
MOS	Metal-oxide-semiconductor
MOSIS	MOS implementation service
MPW	Multi-project wafer

NDA	Non-disclosure agreement
NF	Noise figure
PCB	Printed circuit board
PDK	Process design kit
PLL	Phase locked loop
RBW	Resolution bandwidth
RF	Radio frequency
SiGe	Silicon germanium
SPICE	Simulation program with integrated circuit emphasis
VCO	Voltage-controlled oscillator
WPAN	Wireless personal area network

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CHAPTER 1: INTRODUCTION

1.1 BACKGROUND TO THE RESEARCH

The millimetre-wave (mm-wave) band has been attracting world-wide attention because of the high speed data communication that can be achieved with the wide band of unlicensed spectrum available at 60 GHz [**1**]. The IEEE 802.15.3 Task Group 3c (TG3c) has developed a mm-wave based physical layer for the wireless personal area network (WPAN) standard, which operates in the 57-64 GHz unlicensed band and can provide high data rates over 2 Gbps [**2**]. The channel frequencies allocated in the IEEE 802.15.3c standard are 58.32 GHz, 60.48 GHz, 62.64 GHz and 64.8 GHz, which are similar to other standards, such as ECMA, WiGig, WirelessHD etc. The advancement in silicon integrated circuits (ICs) [**3**] [**4**] have also driven the development activity in the mm-wave consumer and commercial market, namely in WPANs at 60 GHz [**5**] [**6**] and also in automotive radars at 24 GHz and 77 GHz [**7**] [**8**] [**9**]. In addition to achieving higher communication speeds and improved radar detection, higher imaging resolution is another applications that is being explored in the mm-wave range [**10**].

The 57-64 GHz band is in the mm-wave portion of the electromagnetic (EM) spectrum, where the wavelength ranges from ten millimetres (30 GHz) to one millimetre (300 GHz). The specific attenuation characteristics of 10 to 15 dB/km due to atmospheric oxygen absorption at 60 GHz makes this band suitable for short-range (<1 km) communications. The high attenuation factor also helps in frequency re-use, as one 60 GHz radio link is attenuated enough not to interfere with another 60 GHz link operating in its geographic vicinity [**1**].

In addition to obtaining high-speed systems, the added advantage of moving to higher frequencies is the reduction in the size of the antennas (λ of about 2.4 mm in silicon dioxide at mm-wave), which can create compact systems. The small size of the antennas necessitates highly directional beams for communication, which could be obtained using

techniques such as phased arrays. This is also suitable as the behaviour at V-band is more line-of-sight and there is less diffraction compared to lower frequencies [**11**].

1.1.1 Phased-array systems

A complete integrated phased-array system consists of several antenna elements arranged in one or two dimensions, with each element having its own signal path. A phased-array receiver and transmitter implementation is shown in Figure 1.1 and Figure 1.2 respectively.

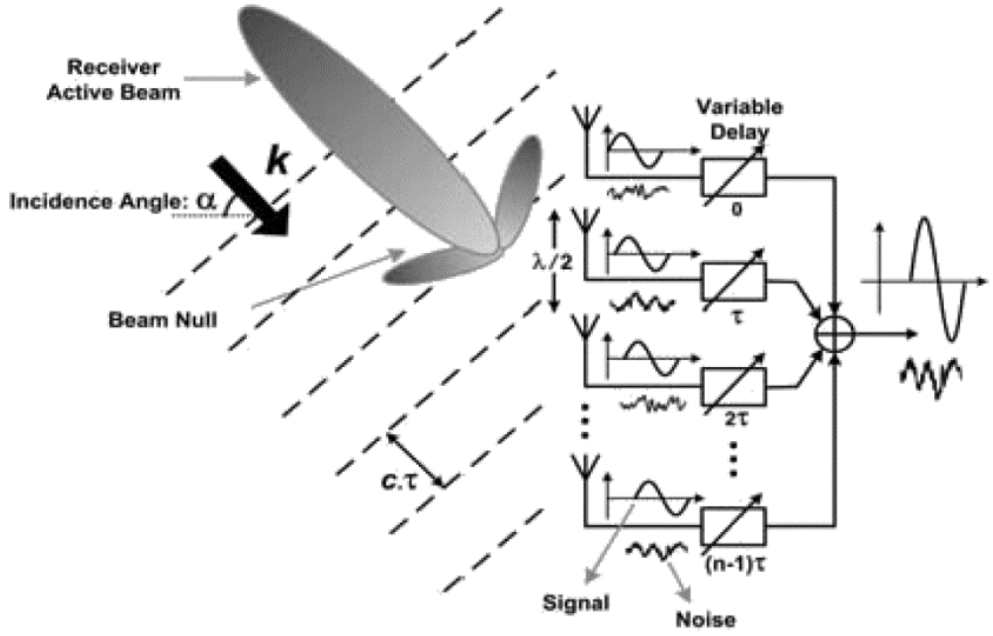

Figure 1.1. Phased-array receiver [11**] (Copyright © [2008] IEICE)**

In a phased-array receiver as in Figure 1.1, the signal reaches each of the spatially separated antennas at different times, depending on the angle of incidence and the spacing between the antennas. The time delay between the signals at different antenna elements are compensated for and the signals are coherently combined by the receiver to enhance the reception from the desired direction [**12**]. This helps in rejecting any interference that does not originate from the direction of the intended signal.

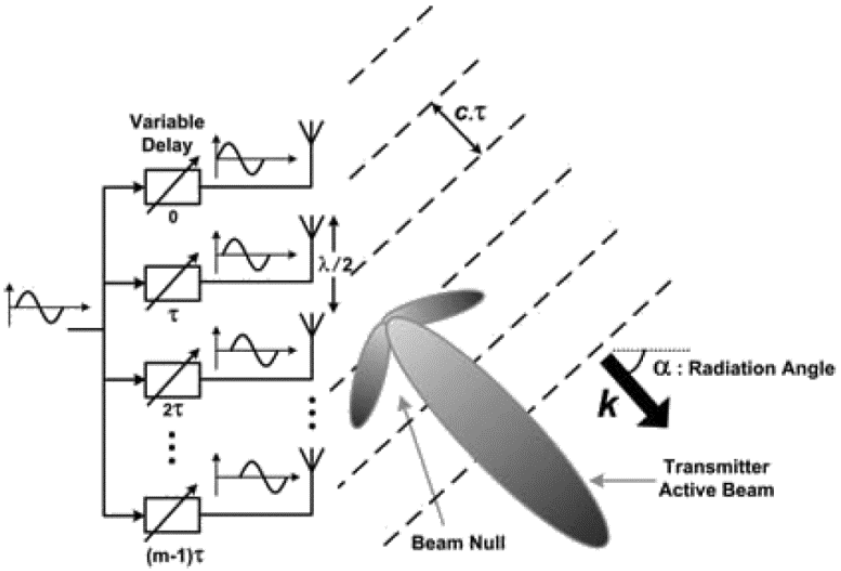

Figure 1.2. Phased-array transmitter [11**] (Copyright © [2008] IEICE)**

In a phased-array transmitter as in Figure 1.2, the signals radiating from each element are delayed such that they add up coherently and thus transmit in the intended direction. In a transmitter with n antenna elements, the total power radiated is n^2 times that of the power radiated by a single antenna element. Thus the power-handling requirement of each of the active devices is also alleviated, while migrating to a newer technology node, which has higher performance but a lower breakdown voltage.

Better sensitivity and improved rejection capability to interference are the main attributes of a phased-array receiver. The directivity of a transceiver also results in improving the frequency reuse ratio, thus increasing the capacity of the network.

In narrow-band systems, the required time delay in the signals at each element of the phased array can be obtained by a phase-shift. A phase shifter with a phase control range of 360° and a phase resolution of 22.5° is the typical requirement for phased-array systems [**13**].

The phase-shift can be applied at radio frequency (RF), baseband/IF or the local oscillator (LO) path. The RF path phase-shifting approach has the lowest power consumption, and

hence is the architecture implemented most often in phased-array implementations [**6**] [**13**]. The advantage of LO path phase-shifting is that the phase-shifter loss does not directly deteriorate the receiver sensitivity [**7**] [**8**]. The various phases required at the antenna elements can be obtained in a centralised or decentralised method. In the centralised approach, all the necessary phases are generated in one place [**7**], while in the decentralised approach, the LO signal is distributed and the remaining phases are generated locally using a phase rotator in each LO path [**8**]. In a centralised LO-path approach, the phase resolution is limited by the number of phases generated by the voltage controlled oscillator (VCO). Also, the phase distribution network becomes quite complex as the number of antenna elements is increased and they tend to perform less efficiently at mm-wave frequencies. Therefore, the decentralised option or *local* LO-path phase-shifting system is preferred in phased-array systems where the phase resolution will depend on the resolution of interpolator weights, employed as part of the phase rotator, and can be generated by using high-resolution digital-to-analogue converters (DACs).

The phase-shifted signals for implementing phased-array transceivers could be achieved using passive architecture such as a reflection-type phase shifter [**14**]. The disadvantage of implementation with passives is the high insertion loss of about 4.2 dB – 7.5 dB at 60 GHz. An active interpolator for the RF-path phase shifting approach at 60 GHz [**15**] is reported to achieve 360° phase variation, -2 dB gain, 12 GHz 3 dB bandwidth and a 16.5 dB noise figure.

1.1.2 Vector-sum phase-shifting method

The vector-sum phase-shifting method could be employed to generate a random phase signal from an in-phase and a quadrature phase signal [**16**] [**17**] [**18**]. As the amplitudes of both signals are varied independently, the resulting phase and amplitude will vary accordingly, as shown in Figure 1.3, and are given by (1.1)

$$V_R = \sqrt{V_I^2 + V_Q^2} \quad ; \quad \varphi = \tan^{-1}\frac{V_Q}{V_I} \tag{1.1}$$

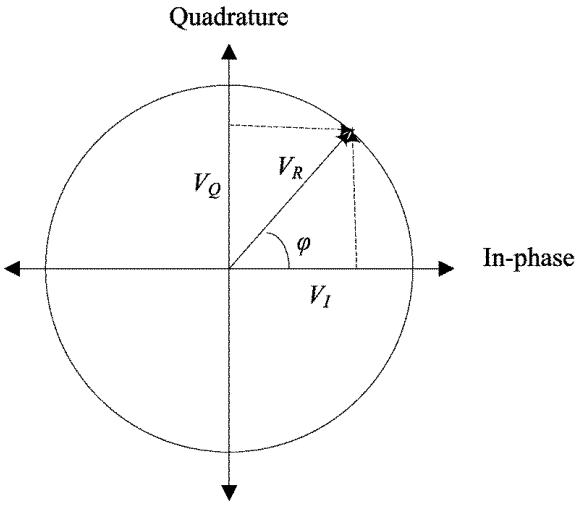

Figure 1.3. Vector sum phase-shifting method

As shown in Figure 1.3, the quadrature-phased signals are combined to obtain the signal whose magnitude and phase depends on the magnitudes of the in-phase and quadrature signals. The LO phase-shifting approach for phased-array systems requires a phase-shifted oscillator signal to be applied to the mixers in each signal path. Such a linearly varying phase signal generator could be conceptualised as an integrated phase-shifted VCO, as shown in Figure 1.4.

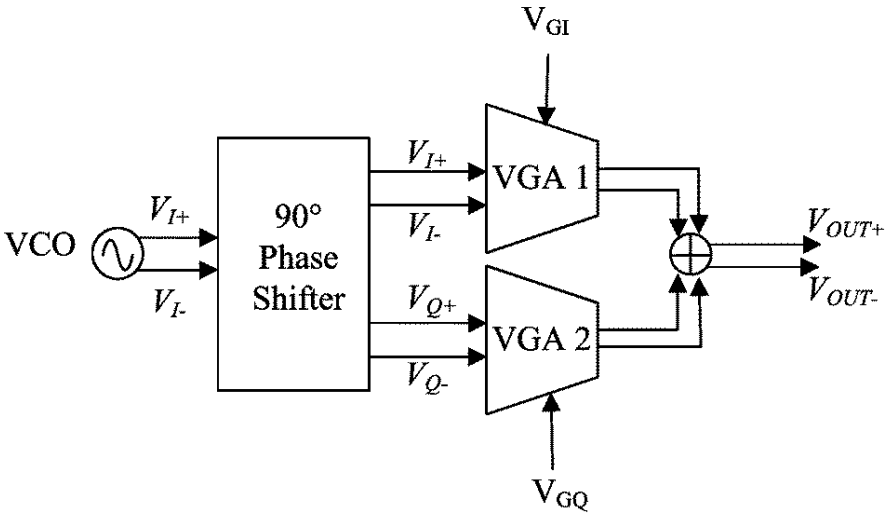

Figure 1.4. Block diagram of the integrated phase-shifted VCO

According to Figure 1.4, the essential components of the integrated phase-shifted VCO are the VCO, the 90° phase shifter to generate V_I, V_Q and variable gain amplifiers (VGAs) whose gain could be controlled by current-steering DACs. In a phased-array system with multiple antenna elements, a single VCO along with buffers and transmission lines in the distribution network could channel the signals to the phase shifter circuits. The phase shifter circuits could then generate the required phase shifts locally by using quadrature generators and VGAs in each signal path of the phased arrays as in a decentralised approach.

1.2 MOTIVATION FOR THE RESEARCH

Traditionally, the III-V compound semiconductors technology, which has a relatively high f_T, high breakdown voltage and lower passive losses, has been used for RF design, but its commercialisation is not viable owing to the associated higher cost. The technology advances have pushed the f_T of silicon germanium (SiGe) and metal-oxide-semiconductor (MOS) transistors to as high as 500 GHz [**19**], thus making high performance systems based on these technologies commercially viable.

The objective of this research was to test the feasibility and accuracy of a SiGe production technology based integrated phase shifted VCO for implementing a phased-array system. The objective was to minimise the rms phase error in the output of the integrated phase-shifted VCO to reduce the jitter in the output transmitter beam of phased arrays [**8**]. In addition, the particular requirement of an oscillator in any communication system (especially for ones with narrow channel spacing) is the low phase noise of the oscillator, as the channel spacing is constrained by the phase noise. Hence this research also targeted the improvement of phase noise performance of VCOs, particularly at 60 GHz, by studying the phenomenon of phase noise generation. It focused on analytically modelling the phase noise to optimise the design performance by identifying the high-impact process or design parameters. This helped in generalising a design procedure for optimum phase noise performance at any mm-wave frequency.

1.3 RESEARCH PROBLEM AND HYPOTHESIS

This research aimed to investigate the performance of an integrated phase shifter system at 60 GHz, which could be used to implement the *local* LO-path phase shifting for phased-array systems. To minimise the rms phase error in the output of an integrated phase-shifted VCO, the focus was placed on improving the performance of the VCO. The following research hypothesis was proposed to improve that aspect of the research problem.

- *If a linear time varying (LTV) model could be used to analyse a mm-wave VCO configuration, then an analytical expression for phase noise in terms of process and design parameters could be derived and optimised to improve the phase noise performance of the VCO.*

In the mm-wave spectrum, phase noise primarily depends on the quality factor of the varactor and hence, instead of researching the improvement of the inductor quality factor at mm-wave frequency, the focus will be on studying the effect of the varactor performance and thus on optimising its value during the design.

To validate the hypothesis, a mm-wave VCO was prototyped using a production-ready IC process, namely the IBM 8HP 130 nm SiGe BiCMOS process with the devices including the passives and the heterojunction bipolar transistors (HBTs) using their process design kits (PDKs).

The performance improvement of the VCO was then quantified by calculating the VCO figure of merit (FOM) [**20**] defined as in (1.2),

$$FOM = -L(f_c, \Delta f) + 10\log\left(\left(\frac{f_c}{\Delta f}\right)^2 \frac{1\,mW}{P_{supply}}\right) \tag{1.2}$$

where $L(f_c, \Delta f)$ is the phase noise at offset Δf in dBc/Hz; P_{supply} is the power consumption in mW; f_c and Δf are the carrier and offset frequency.

Another research problem investigated was the feasibility of implementing an integrated phase shifter using the vector-sum phase-shifting method in the IBM 130 nm process.

1.4 JUSTIFICATION FOR THE RESEARCH

The demands for higher speeds in communication systems and the channel allocation by IEEE 802.15.3c have accelerated the research activity in the mm-wave spectrum, where phased arrays are implemented to achieve the necessary directivity. These phased arrays require LO signals at multiple phases to steer the direction of the beam. These signals could be generated from the VCO using vector interpolation and this would mean that its performance would depend on the performance of the VCO.

In general, a wireless transceiver requiring a VCO to perform RF to baseband conversion needs good phase noise performance for the VCO, as it determines the system sensitivity. To design a VCO with good phase noise performance, it is imperative to model the effects of various noise sources in the circuit on the final phase noise, and thus decide on the design choices. The linear time-varying (LTV) model of oscillator was thus studied and the effect of various noise sources was quantified by using their impulse sensitivity function (ISF). This eventually led to an expression, which was then optimised and thus the design choices were developed. These design choices serve as a reference for any mm-wave VCO design that would require optimum phase noise performance.

The hypothesis was validated by a VCO prototype using the IBM 130 nm SiGe BiCMOS process, which is a production-ready process for mm-wave applications. This would mean that the design could be performed without the need for any time-consuming EM simulations, which is mostly used to design passives for the mm-wave circuit design arena [**21**].

1.5 METHODOLOGY

As a 60 GHz VCO was prototyped to validate the hypothesis, the design methodology consisted of literature study performed on the various mm-wave VCO configurations that have been implemented to date. The most popular VCO configuration was identified as the

differential Colpitts oscillator with a cascode buffer. As proposed, phase noise modelling using the ISF was performed on the LTV model of the oscillator. This would lead to an analytical expression, which would help in optimising the phase noise.

The design choices leading from the above analysis were used in designing a mm-wave VCO. The simulations were performed using the PDK supplied by IBM for the 130nm process. Numerical simulations on the design using SpectreRF also led to the same conclusion as the analytical modelling. Simulations were performed to verify the proposed vector interpolation scheme to generate various phases from the VCO output.

Finally, the layout of the designed 60 GHz VCO was submitted for fabrication in the IBM 8HP 130 nm SiGe BiCMOS process. A PCB was then designed and fabricated to characterise the monolithic microwave integrated circuit (MMIC) on the wafer level. The measurements were then performed using a spectrum analyser, MS2668C, and the VCO characteristics were recorded.

1.6 DELIMITATIONS OF SCOPE AND KEY ASSUMPTIONS

A mm-wave design methodology usually encompasses interconnect modelling, where the ‘electrically long’ interconnects need to be treated as transmission lines rather than shorts. This would mean that after the layout, interconnects have to be characterised in EM simulation software and incorporated back into the schematic design for proper simulation of the circuits. This approach was not followed in the research and this decision is justified, as care was taken during the layout to keep the interconnect length as short as possible.

1.7 CONTRIBUTIONS TO THE FIELD

Phase noise analysis has been performed on a mm-wave VCO configuration, and an analytical expression for phase noise in terms of process and design parameters has been derived. A detailed list of the resulting contributions to the body of knowledge is given here.

- The major contribution of the research has been the modelling of phase noise of a mm-wave VCO configuration, using the ISF of various noise sources on the LTV model of oscillators. This led to an analytical expression for phase noise in terms of process and design parameters for the specific circuit configuration, followed by minimisation of its value by optimisation of these parameters.

- A common collector Colpitts oscillator in the cascode configuration has been analytically modelled for its phase noise performance. The phase noise contributions from the noise sources associated with active devices in the circuit have been quantified using their impulse sensitivity function. The resulting analytical expression for phase noise provides an explanation for the design choices made by the designer.

- The lumped element approach to mm-wave design followed in this work used the PDK provided by the foundry and no EM simulations were performed to characterise the components.

- A mm-wave VCO was fabricated based on the analysis and was measured to demonstrate a phase noise performance of -98.9 dBc/Hz at 1 MHz offset, from a centre frequency of 52.8 GHz. The power consumption of the MMIC was around 140 mW and it occupied an area of 0.64 mm^2, including the bondpads.

Oscillator designs can be widely varied in design criteria and include optimisation in area or any design specification such as phase noise or power consumption, the technology used etc. Generally the parameter FOM given by (1.2), which includes the design specifications such as oscillating frequency, phase noise and power consumption, is reported for benchmarking the design. A summary of the performance of state-of-the-art SiGe VCOs is given in Table 1.1.

Table 1.1. Comparison with state-of-the-art SiGe VCOs in the mm-wave range

References	[**22**]	[**23**]	[**24**]	[**25**]	This work [**26**]
Impact Factor (2011)	3.226	3.226	1.853	3.226	0.618
Cited Half-life (2011)	7.1	7.1	9.0	7.1	5.0
Technology	0.35 µm SiGe HBT	0.18 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.35 µm SiGe HBT	0.13 µm SiGe BiCMOS
Frequency (GHz)	41	52.5	70.5	80	52.8
Freq Tuning Range (%)	26	26.5	5	30	13.5
Phase Noise at 1 MHz	-110	-108	-93	-97	-98.9
Differential Output Power (dBm)	6.5	1.5	0	12	8
Power Consumption (mW)	280	132	73	240	140
Area (mm^2)	0.5 (with pads	0.168	Not Given	Not Given	0.28
FoM (dBc/Hz)	178	181	171	171	172

From Table 1.1, it is evident that the VCO in this work presents an FOM comparable to the state-of-the-art VCOs. [**22**] presents a higher FOM, but is achieved at twice the power dissipation than that of this work. The output power is not taken into account in the presented FOM, and that is the reason for the high FOM of [**23**]; as can be noted, it

provides very low output power. The reason for the low output power is that it is a push-push VCO, in which the second harmonic is combined at the output to provide a higher frequency of oscillation. A push-push topology is advantageous in achieving a wide tuning range and low phase noise with low power consumption, as the tank operates at half the frequency [**27**]. The disadvantage is that the power output at the second harmonic, which is the useful one, is very low.

- The suitability of a vector interpolator in phased-array systems to steer the beam direction was demonstrated through simulations. The interpolator provided VCO signals from 0° to 360° in steps of 22.5° with a total power consumption of about 60 mW. This could be successfully implemented in a *local* LO-path shifting architecture to provide phase-shifted VCO signals to mixers in the signal path of a transceiver.

1.8 PUBLICATIONS DERIVED FROM THE RESEARCH

The following peer-reviewed journal (listed by the Thomson Reuters Web of Knowledge) article has been published:

- D. George and S. Sinha, "Phase noise analysis for a mm-wave VCO configuration", *Microwave and Optical Technology Letters*, vol. 55, no. 2, pp. 290-295, February 2013.

A second article on the research work has been submitted for publication to a journal (also listed by the Thomson Reuters Web of Knowledge):

- D. George and S. Sinha, "Vector-sum method for multiple-phase generation in mm-wave phased array systems using BiCMOS technology", *Analog Integrated Circuits and Signal Processing*.

1.9 OUTLINE OF THE THESIS

Chapter 1 provides the background and context of the research that was undertaken. The research problem and hypothesis are stated. A summary of the research methodology that

was adopted and the contribution of the research to the body of knowledge are discussed, followed by the publication derived from the research.

Chapter 2 provides the details of the literature that was reviewed to validate the proposed research hypothesis. The choice of SiGe technology and the way in which the noise sources in the technology are converted into phase noise in the oscillators are discussed briefly. The VCO implementations in the mm-wave range and current circuit techniques used to improve the phase noise performance have been thoroughly studied.

Chapter 3 describes the research methodology in detail. It provides a study of the process to be used in designing the prototype mm-wave VCO. It also discusses the details of the measurement setup that to be used, so that the layout of the MMIC can be finalised according to any equipment setup requirements.

Chapter 4 discusses the analytical model for phase noise developed in the research. An analytical expression for phase noise was derived for a mm-wave VCO configuration, so that any design optimisation could be performed. The design and process parameters that influence the phase noise performance were identified in this process. This helped in providing a solution to the design choices that are crucial to circuit performance.

Chapter 5 describes the design and simulation of the VCO and the vector interpolator using components available in the IBM 130 nm SiGe BiCMOS process. Numerical simulations have been performed to verify the optimum value of the design parameter capacitors' ratio, *n*, as indicated by the analytical model derived in Chapter 4.

Chapter 6 details the layout of the MMIC, and provides microphotographs of the chip. It also describes the PCB and its components. The measurement setup for characterising the VCO is described and the results are presented. The measurement results are compared with the simulation and reasons for discrepancies are identified.

Chapter 7 provides a critical evaluation of the work, along with suggestions for future work.

Due to a non-disclosure agreement (NDA) between the author and the foundry through the University of Pretoria, certain process parameters have been excluded from this thesis.

1.10 CONCLUSION

This chapter provided background and motivation to the research work. The hypothesis and research questions were developed. A brief research methodology followed in the work and limitations to the research were stated. The contributions from the research were also provided and finally, the outline of the thesis was given.

CHAPTER 2: LITERATURE REVIEW

2.1 INTRODUCTION

This chapter details the literature study performed for the research work. It provides a background study of the SiGe semiconductor technology and the targeted system implementation, which includes the VCO. The study describes how the noise sources in the technology would manifest as phase noise of the oscillator, in turn determining the random phase error in the phase shifter system.

2.2 SIGE TECHNOLOGY FOR MM-WAVE APPLICATIONS

The intrinsic device characteristics are dependent on the constituent material systems and device physics underlying a transistor's operation [**4**]. Table 2.1 shows the properties of several semiconductor materials that determine the preferred constituent material for the deployment of an RF transceiver system.

Table 2.1. Electron properties of several materials [4]

Property	Si	Ge	GaAs	InP	GaN
Bandgap (eV)	1.12	0.66	1.42	1.35	3.26
Lattice constant (Å)	5.431	5.646	5.653	5.869	5.189
Breakdown field ($\times 10^6$ V/cm)	0.3	0.1	0.4	0.5	2
Electron mobility at 300 K (cm^2/Vs)	1450	3900	8500	4600	1000-2000
Saturation velocity ($\times 10^6$ cm/s)	9	-	6	9	25
Thermal conductivity (W/cm-K)	1.3	0.58	0.3	0.68	1.3

In Table 2.1, the semiconductor bandgap and the breakdown field determine the maximum device operating voltage of any device technology. The drift velocity and carrier mobility influence the device speed. The thermal resistance of a semiconductor substrate limits the device's power-handling capability. The lattice constant determines whether high-quality

single-crystal growth of certain materials is possible on a substrate without any introduction of strain layers. It is evident from Table 2.1 that Si has a relatively high thermal conductivity; however, the lack of a semi-insulating substrate and low mobility (resulting in a low drift velocity) stalled the development of low-cost Si-based RF systems. Historically, compound semiconductors such as GaAs, InP, etc have been deployed in RF applications because of their high mobility and the ease of preparation of semi-insulating substrates. The associated high cost has limited their success in commercial applications, and has led to an increased focus on SiGe HBTs.

SiGe HBT is a modification over the standard silicon bipolar junction transistor (BJT), in which the bandgap energy of the base is lowered by introducing Ge atoms to its base. The graded concentration of Ge reaches its maximum in the base-collector junction, as shown in Figure 2.1.

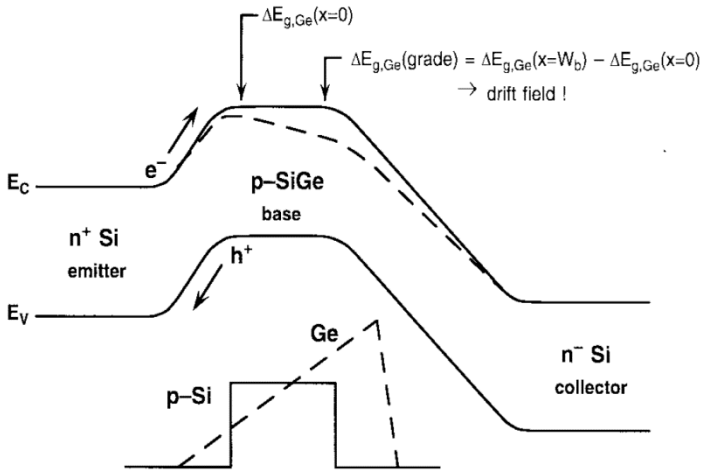

Figure 2.1. The energy bandgap diagram of the Si/SiGe HBT [28**] (© [1998] IEEE)**

The lowered bandgap in the base, as seen from Figure 2.1, improves the emitter injection efficiency γ of the transistor, as the potential barrier for the holes injected back into the emitter is increased. The high emitter injection efficiency enables one to increase the doping concentration in the base and thus to lower the physical base resistance r_B. The graded Ge profile in the base also results in a *drift field*, which accelerates the electrons from the emitter to the collector, thus lowering the base transit time τ_b. Hence, SiGe HBT offers higher performance transistors with high f_T given by (2.1)

$$f_T = \frac{1}{2}\left[\frac{1}{g_m}(C_{eb} + C_{cb}) + \tau_b + \tau_e + \tau_{bc}\right]^{-1} \quad (2.1)$$

where C_{eb} (also known as C_π) is the parasitic emitter-base junction capacitance, C_{cb} (or C_μ) is the parasitic collector-base junction capacitance, g_m is the device transconductance, τ_b is the base transmit time, τ_e is the emitter delay time and τ_{bc} is the base-collector junction depletion layer time.

Another FOM of an active device is the maximum oscillation frequency f_{max} given by (2.2),

$$f_{\max} = \sqrt{\frac{f_T}{8\pi r_b C_{cb}}} \quad (2.2)$$

where r_b is the parasitic base resistance.

Thus SiGe HBT offers bandgap engineering with the cost of fabrication and process reliability similar to that of the Si BJTs. However, SiGe HBT has poorer device ruggedness in wireless applications owing to its relatively low open-base collector-to-emitter breakdown voltage (BV_{CEO}). This is one of the key parameters limiting the power output from oscillators, thus controlling its phase noise [**29**].

It has been reported that bipolar MMIC design is relatively easier and has a better chance of first-pass silicon success than CMOS design. One of the main reasons is that the bipolar model is simpler and models the physical processes in the transistor quite accurately. The layout effects of wiring parasitics, substrate contacts and proximity effects to adjacent devices have much less impact on the device performance in bipolar design than in CMOS. As device parasitics play a major role in the close matching of simulated and measured results, this also influences the choice of one technology over another for efficient circuit implementation. 60 GHz transceiver circuits implemented in SiGe technology have shown good model-to-hardware correlation [**30**]. Also, SiGe VCOs have better phase noise performance and a better tuning range than their MOS counterparts [**31**], but at the expense of higher power consumption.

The low *1/f* noise of SiGe makes it the preferred choice over MOS technology for VCO design. The reason is that *1/f* noise is up-converted and shows up as the phase noise of the

oscillator (see section 2.6). The low-frequency (*1/f* or flicker) noise has a power spectral density inversely proportional to *f* as shown in Figure 2.2.

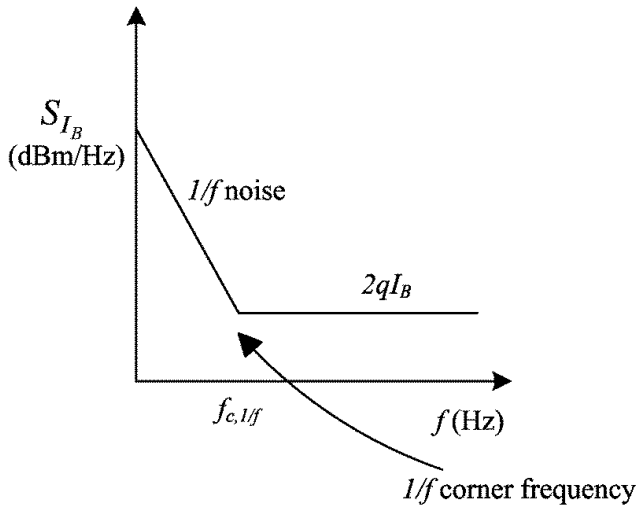

Figure 2.2. A typical low-noise frequency spectrum of SiGe HBTs [20**] (**Reproduced by permission from J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*, Norwood, MA: Artech House, Inc., 2003. © 2003 by Artech House, Inc.)

As shown in Figure 2.2, a typical low-frequency noise spectrum of the base current has an *1/f* component which intercepts the $2qI_B$ shot noise level at the *1/f* corner frequency given by $f_{c,1/f}$. The polysilicon-to-crystal silicon interfacial oxide and the oxide spacers around the emitter perimeter are responsible for *1/f* noise in SiGe HBTs [**32**].

In general, S_{I_B} is related to the DC component of the base current, I_B by

$$S_{I_B} = K_F \frac{I_B^{\alpha}}{f} \tag{2.3}$$

where K_F and α correspond to the flicker noise coefficient (KF) and flicker noise exponent (AF) model parameters in SPICE. The value of α is close to 2 for typical SiGe HBTs.

For a certain value of the collector current, S_{I_B} is lower in SiGe HBTs than in Si BJTs. This is because of the lower base current due to higher β. The *1/f* noise factor K_F is

inversely proportional to the emitter area A_E and thus substituting for the base current in (2.3) gives (2.4)

$$S_{I_B} = \frac{K}{A_E}\frac{I_B^2}{f} = \frac{K}{\beta^2}\frac{1}{A_E}\frac{I_C^2}{f} \tag{2.4}$$

Hence, a higher β and a larger device reduce S_{I_B}, but this reduces the f_T of the device owing to lower collector current density J_C. The *1/f* corner frequency is obtained by equating the two noise spectral densities as shown

$$\frac{K}{A_E}\frac{I_B^2}{f_{c,1/f}} = 2qI_B \tag{2.5}$$

$$f_{c,1/f} = \frac{KI_B}{2qA_E} = \frac{KJ_C}{2q\beta} \tag{2.6}$$

The *1/f* noise factor *K* is seen to increase with technology scaling, but this is usually offset by the increase in β due to scaling. However, the phase noise corner frequency in an oscillator is seen to be much lower than the *1/f* noise corner frequency given by $f_{c,1/f}$ (see section 2.6.2)

The added advantage of integrating SiGe and CMOS technology into BiCMOS processes is that it helps in the development of system-on-chip mm-wave systems where analogue, RF and digital circuitry can reside on a single chip. In the IBM 8HP process, SiGe HBTs with f_T = 200 GHz have been integrated into a 130 nm BiCMOS technology while fully retaining the field effect transistor (FET) device and interconnect properties of IBM's standard 130 nm CMOS technology.

The quality of the passive devices is also important in high-frequency designs. Though the III-V materials have low-loss dielectric properties, the RF-enhanced processes offer Si passives whose *Q*-factor is approaching that of III-Vs [**3**]. The *Q* of the inductors in the mm-wave range is much higher compared to the varactors [**31**], and this holds true for the IBM 8HP process as well.

2.3 INTEGRATED PHASED-ARRAY IMPLEMENTATIONS

Phased-array implementations have been demonstrated in SiGe [**5**] [**6**] [**7**] [**8**] [**9**] [**17**] and CMOS [**33**] [**34**]. A phased-array receiver with an LO-path-based approach is implemented in [**9**] and [**33**], while the phased-array transmitter implementation in Q-band [**17**] has the phase shift implemented in the RF path. Reported simulations in [**17**] show that an on-chip phased array with 0-360º phase shifters can drive 4 × 4 elements with virtually no penalty for a system with up to 10% bandwidth.

The integral module in any phased-array implementation is the phase shifter circuitry, which is incorporated in the RF path for an RF-based approach, or after the VCO in the LO path-based approach.

2.4 PHASE SHIFTERS

The phase shifters could be implemented using passive elements, as by using a quadrature coupler with a C-L-C load as in a reflection-type phase shifter [**14**] or by using vector-interpolation scheme. As discussed earlier, the disadvantage with the passive phase shifters is the high insertion loss. The phase shifters for the LO path shifting architecture in [**8**] have been implemented using phase rotators, where a $\lambda/4$ t-line has been used to generate a quadrature LO signal which is then provided to an analog phase rotator. The quadrature signal for vector-interpolation could also be obtained using a quadrature all-pass filter, and an I/Q phase error of less than 5º is reported at 30-46.5 GHz band [**17**].

2.5 MULTIPLE-PHASE VCO

The LO-path phase-shifting architecture for phased arrays requires multiple phases of the LO signal. This can be obtained by using a VCO and a phase shifter circuitry to implement the vector-sum method [**8**].

The resolution of an LO path-based phase shifting transmitter system depends on the resolution of the interpolator weights generated by the DACs and the phase-noise of the LO signal, which translates to jitter in the beam direction [**8**]. As the output is obtained by

interpolating the in-phase and quadrature-phase (delayed version) signals, the rms jitter in the phase setting is given in radians by (2.7)

$$\left\langle \theta^2(t) \right\rangle = 2 \int_{f_{\min}}^{\infty} 10^{L(f)/10} df \tag{2.7}$$

where *L(f)* is the phase noise of the oscillator in dBc/Hz.

It was noted that the resolution of the phase-shift is not the same as that of the DAC weights. There would be an error in some phase settings if a phase shift from 0º to 360º is generated with a step size of $360^\circ / 2^{n+1}$ using a *n*-bit DAC.

2.6 PHASE NOISE IN OSCILLATORS

Phase noise in oscillators is given by (2.8),

$$L_{total}\{\Delta\omega\} = 10.\log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1\,\text{Hz})}{P_{carrier}}\right] \tag{2.8}$$

where $P_{sideband}(\omega_0 + \Delta\omega, 1\,\text{Hz})$ represents the single sideband power at a frequency offset $\Delta\omega$ from the carrier in a measurement bandwidth of 1 Hz and $P_{carrier}$ is the total power under the spectrum in Figure 2.3.

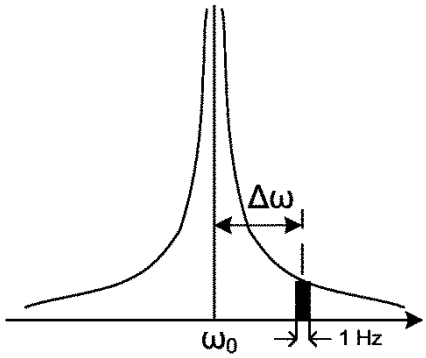

Figure 2.3. The phase noise per unit bandwidth at offset Δω

The phase noise is an undesirable feature in any communication system, as it leads to "reciprocal mixing" and thus a significant degradation of the wanted signal [**35**]. This also affects the channel spacing, especially in narrow band systems.

The increasing demand for bandwidth thus places a stringent requirement on the phase noise of the oscillators, and low phase noise oscillators have become a requirement for attaining good communication system characteristics. Also, the phase noise of the LO signal is a critical performance measure of the VCO in an LO-path phase-shifting transmitter architecture, as it translates to jitter of the beam [**8**]. These requirements emphasise the need to model phase noise accurately.

The noise in the circuit undergoes various frequency translations before ultimately contributing to the phase noise. These translations, caused by non-linearities in the oscillator, should be properly modelled to optimise the circuit performance. The pioneering work on modelling the phase noise was done by Leeson in 1966 and was based on a linear time-invariant (LTI) approach [**36**]. Though the LTI approach was successful in providing qualitative design insights, it failed to predict the phase noise quantitatively. In 1998, Hajmiri and Lee described oscillators as an LTV system, which could be characterised by an ISF [**37**]. The two approaches to phase noise modelling are discussed in the following subsections.

2.6.1 Leeson's LTI approach

Leeson's model was the first one to provide an approximation for the phase noise of an oscillator. In an ideal oscillator the only noise source is the loss of the tank *G*, as shown in Figure 2.4.

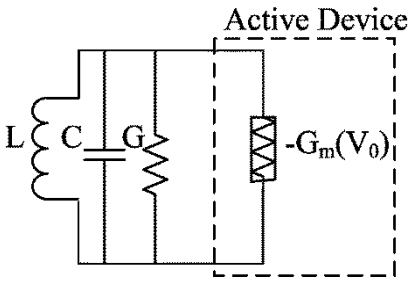

Figure 2.4. The one-port model of an LC oscillator

The average thermal current noise spectral density of a resistor with conductance G is given by (2.9),

$$\frac{\overline{i_n^2}}{\Delta f} = 4kTG \tag{2.9}$$

where k is the Boltzmann's constant (8.617×10^{-5} eV/K) and T is the absolute temperature in K.

The spectral density of the mean-square voltage is obtained by multiplying the current noise spectral density by the square of impedance of the tank.

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \bullet |Z|^2 \tag{2.10}$$

For a relatively small offset frequency ($\Delta\omega$) from the centre frequency ω_0, the impedance of the tank Z can be approximated by (2.11).

$$Z(\omega_0 + \Delta\omega) \approx \frac{j.\omega_0 L}{2\frac{\Delta\omega}{\omega_0}} \tag{2.11}$$

Substituting for L from the expression of loaded quality tank factor Q in the equation for Z, as in (2.12)

$$Q = \frac{R}{\omega_0 L} = \frac{1}{\omega_0 GL} \tag{2.12}$$

$$Z(\omega_0 + \Delta\omega) \approx \frac{1}{G} \bullet \frac{\omega_0}{2Q\Delta\omega} \tag{2.13}$$

Thus the mean-square noise voltage spectral density is given by (2.14):

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \bullet |Z|^2 = 4kTR\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{2.14}$$

Thus the power spectral density of the output noise varies as $1/f^2$ at an offset frequency Δf from the centre frequency and contains the combined effect of both amplitude and phase variations. The equipartition theorem of thermodynamics states that, in equilibrium, the amplitude and phase-noise power are equal. The inherent amplitude-limiting mechanism present in an oscillator limits the amplitude noise and hence the phase noise will be half of that given in (2.14)

Phase-noise, defined as the ratio of noise spectral density to the carrier power P_{sig}, will thus be given by (2.15):

$$L\{\Delta\omega\} = 10 \bullet \log\left[\frac{2kT}{P_{sig}} \bullet \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{2.15}$$

It is evident from the equation that increasing the signal power and Q of the tank improves the phase noise of the system. It also seems logical, as increasing the signal power improves the ratio as thermal noise is fixed and increasing Q improves the ratio quadratically as tank impedance falls off as $1/Q\Delta\omega$. However, in a practical oscillator there are additional noise sources to be accounted for, namely the noise sources from the active devices that form the energy-restorer element [**38**]. The modified model known as the Leeson-Cutler phase noise model includes the noise from the active devices as well and is given by (2.16).

$$L(\Delta\omega) = 10 \bullet \log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \bullet \left[1+\frac{\Delta\omega\ {}^{1}\!/_{f^3}}{\Delta\omega}\right]\right\} \tag{2.16}$$

The features of (2.16) are that it has an additive factor F, which is an empirical fitting parameter to account for the increased noise in the ${}^{1}\!/_{(\Delta\omega)^2}$ region, an additive factor of unity with the term $\left(\frac{\omega_0}{2Q\Delta Q}\right)^2$, to account for the noise floor, and a multiplicative factor (the term in the second set of brackets) to provide ${}^{1}\!/_{(\Delta\omega)^3}$ behaviour at sufficiently small offset frequencies. The phase noise could be plotted as in Figure 2.5.

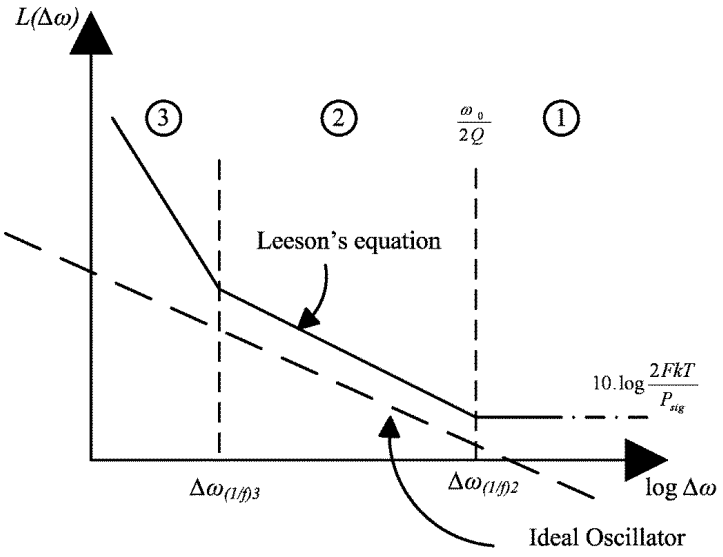

Figure 2.5. Oscillator phase noise spectrum [29**](© [2000] IEEE)**

In Figure 2.5, region 1 is the thermal noise floor that arises because of both active devices as well as the resistive loss of the RLC tank and is given by (2.17).

$$L(\Delta\omega) = 10.\log\frac{2FkT}{P_{sig}} \tag{2.17}$$

Region 2 has the -20 dB/decade slope described by the original Leeson's equation for an ideal oscillator; however, the value is shifted up because of the factor *F*. This then flattens off into Region 1 around the resonator 3 dB bandwidth given by $^{\omega_0}/_{2Q}$. Region 3 begins at a corner frequency $\Delta\omega_{(^1/_f)^3}$ and is dependent on the $^1/_f$ noise corner of the device.

The inadequacy of Leeson's model was that though it was successful in predicting the dependence of the tank *Q* and signal power on phase noise performance, there was no indication of the factors on which *F* was dependent. Thus good oscillator designs could not be developed, as designers could not control the factor *F*. The inability to predict the phase noise quantitatively has necessitated revision of the assumptions made in the derivation.

2.6.2 Hajmiri and Lee's LTV approach

The concept of linearity and the time-invariance of oscillators in Leeson's model were re-examined by Hajmiri and Lee [**39**]. They demonstrated that oscillators are time-varying systems [**29**], though linearity appeared to be a reasonable assumption as far as the noise-to-phase transfer function is concerned.

To prove that oscillators are fundamentally time-varying systems, they considered an impulse at the input of a lossless LC tank oscillating with constant amplitude until the instance of the impulse, as in Figure 2.6 .

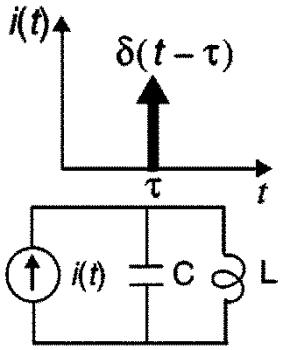

Figure 2.6. LC oscillator excited by current pulse [29**](© [2000] IEEE)**

They analysed the system's response to an impulse occurring at two different time instances. Each noise source may cause both amplitude and phase variations as in Figure 2.7.

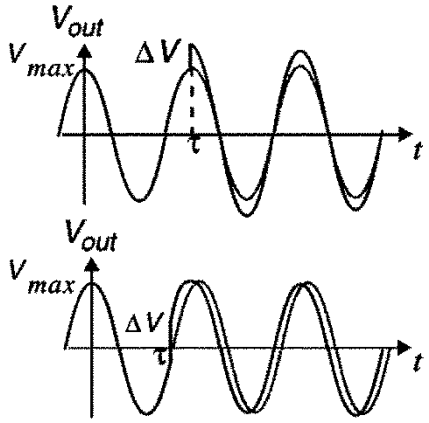

Figure 2.7. Impulse response of LC tank [29](© [2000] IEEE)

According to Figure 2.7, it was observed that if the impulse coincides with the maximum of the voltage, the amplitude increases abruptly, but the phase superimposes with the pre-existing oscillation and thus the timing of the zero crossings does not change. An impulse occurring at any other instance is seen to cause a change in both amplitude and zero crossings in the oscillations. Therefore, an oscillator is basically an LTV system with periodicity.

The impulse response for the phase is a function of two arguments, the observation time *t* and the excitation time *τ*, and can be written as in (2.18):

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0 \tau)}{q_{\max}} u(t-\tau) \tag{2.18}$$

Γ(x) is called the ISF and is a dimensionless, frequency-and amplitude-independent function periodic in *2π* that describes the amount of phase shift from applying a unit impulse at any point in time. The shape of the ISF depends on the oscillator waveform. Once the ISF of an oscillator has been determined through simulation or analytical methods, the excess phase may be determined using the superposition integral (2.19):

$$\phi(t) = \int_{-\infty}^{+\infty} h_{\phi}(t,\tau) i(\tau) d\tau = \frac{1}{q_{\max}} \int_{-\infty}^{t} \Gamma(\omega_0 \tau) i(\tau) d\tau \tag{2.19}$$

ISF is a periodic function with a period related to the oscillator frequency and hence can be expressed as a Fourier series (2.20),

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \bullet \cos(n\omega_0\tau + \phi_n) \tag{2.20}$$

where coefficient c_n is real and ϕ_n is the n^{th} harmonic phase. ϕ_n could be ignored if the noise sources are uncorrelated, hence their relative phase is insignificant.

Substituting the Fourier expansion into the integral (2.19), the excess phase is given by (2.21) and shown graphically in Figure 2.8.

$$\phi(t) = \frac{1}{q_{\max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau)d\tau\right] \tag{2.21}$$

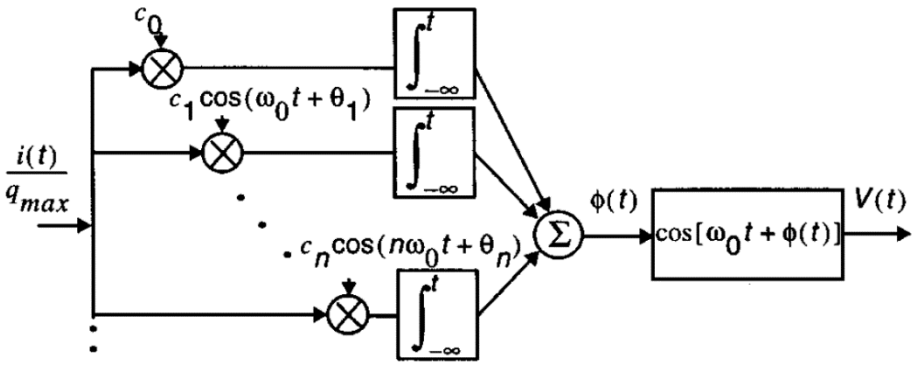

Figure 2.8. Equivalent system for ISF decomposition [29**](© [2000] IEEE)**

This system in Figure 2.8 is analogous to a superheterodyne receiver, where the normalised noise current, which can be considered as a "broadband RF signal", is undergoing down-conversions by "local-oscillator signals" at all harmonics of the oscillating frequency.

If a sinusoidal current *i(t)* as in (2.22), whose frequency is near an integer multiple *m* of the oscillation frequency, is injected into the system,

$$i(t) = I_m \cos\left[(m\omega_0 + \Delta\omega)t\right] \tag{2.22}$$

where $\Delta\omega << \omega_0$.

Substituting in (2.21) and noting that there is a negligible component from the terms other than $n=m$, one obtains the following approximation (2.23):

$$\phi(t) \approx \frac{I_m c_m \sin(\Delta\omega t)}{2q_{\max}\Delta\omega} \tag{2.23}$$

Therefore, the spectrum of $\phi(t)$ contains two sidebands at $\pm\Delta\omega$, even though the injection occurs near some integer multiple of ω_0, as seen in Figure 2.9.

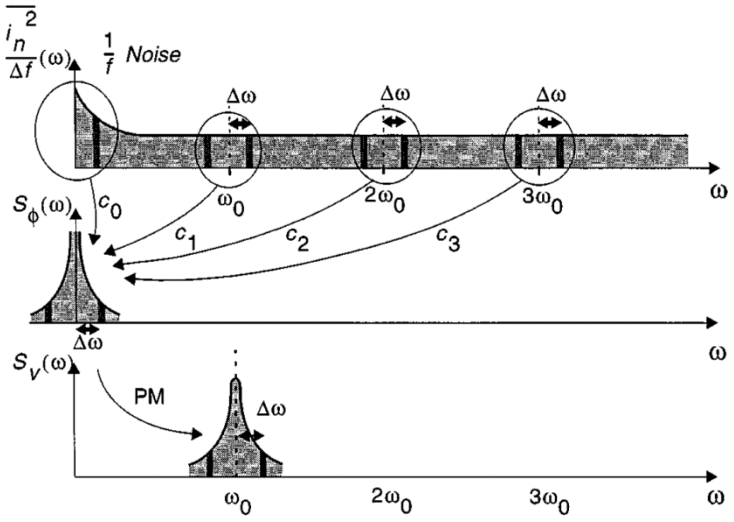

Figure 2.9. Evolution of circuit noise into phase noise [29](© [2000] IEEE)

As seen in Figure 2.9, the spectrum of the output voltage of the oscillator could be evaluated from the phase spectrum by considering the output sinusoid, given by (2.24),

$$v_{out}(t) = \cos\left[\omega_0 t + \phi(t)\right] \approx \cos(\omega_0 t) - \phi(t)\sin(\omega_0 t) \tag{2.24}$$

where it is assumed that $\cos(\phi(t)) \approx 1$ and $\sin(\phi(t)) \approx \phi(t)$ for small values of $\phi(t)$. Using this narrowband tone modulation approximation, an injected current at $m\omega_0+\Delta\omega$ is seen to result in a pair of equal sidebands at $\omega_0+\Delta\omega$, with single sideband carrier power given by (2.25):

$$P_{SBC}(\Delta\omega) \approx 10 \bullet \log\left(\frac{I_m c_m}{4q_{\max}\Delta\omega}\right)^2 \tag{2.25}$$

It may be extended to the general case of a white noise source:

$$P_{SBC}(\Delta\omega) \approx 10 \bullet \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\sum_{m=0}^{\infty} c_m^2}{4q^2\Delta\omega^2}\right) \tag{2.26}$$

From (2.26), it is implied that noise components near the integer multiple of ω_0 fold into noise near the carrier itself, as shown in Figure 2.9; thus $1/f$ noise of the device becomes $1/f^3$ noise near ω_0 and white noise near the higher integer multiple of ω_0 undergoes down-conversion into the noise in the $1/f^2$ region. It can be understood from the expressions that minimising the various coefficients of ISF (c_m) will minimise the phase noise of the system.

Using Parseval's theorem (2.27),

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\Pi}\int_0^{2\Pi} |\Gamma(x)|^2 \, dx = 2\Gamma_{rms}^2 \tag{2.27}$$

the spectrum in the $1/f^2$ region can be expressed as in (2.28),

$$L(\Delta\omega) = 10 \bullet \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{\max}^2 \Delta\omega^2}\right) \tag{2.28}$$

where Γ_{rms} is the rms value of the ISF.

The spectrum in the $1/f^3$ region can be evaluated by assuming that the current noise behaves as in (2.29) in the $1/f$ region.

$$\overline{i_{n,1/f}^2} = \overline{i_n^2} \bullet \frac{\omega_{1/f}}{\Delta\omega} \tag{2.29}$$

where $\omega_{1/f}$ is the corner frequency.

Using (2.28), the spectrum in the $1/f^3$ region can be written as in (2.30):

$$L(\Delta\omega) = 10 \bullet \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}c_0^2}{8q_{\max}^2 \Delta\omega^2} \bullet \frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2.30}$$

The $^{1}/_{f^3}$ corner frequency is then given by (2.31)

$$\Delta\omega_{1/f^3} = \omega_{1/f} \bullet \left(\frac{\Gamma_{dc}}{\Gamma_{rms}}\right)^2 \tag{2.31}$$

Thus the phase noise theory explains why the $^{1}/_{f^3}$ noise corner frequency is lower than the $^{1}/_{f}$ noise corner frequency and also demonstrates that it could be controlled by Γ_{dc} and Γ_{rms} of the ISF. The ISF is determined by the oscillator waveform's shape whose rise-time and fall-time symmetry can be controlled by the designer.

In addition to the phase noise improvement techniques derived from the LTI model, namely improving the tank *Q* and signal power, the LTV model suggests that the phase noise contribution from active devices, which act as the energy-restorer, should be minimised. From the ISF theory, it is quite obvious that there are sensitive and in-sensitive instances in an oscillation cycle. Hence the transistor (active element) should deliver the energy *all at once* to the LC tank, i.e. the transistor would remain off almost all the time and wake up periodically to deliver the current impulse at the signal's peak in each cycle. The oscillators should also be designed to possess symmetry properties (rise-time and fall-time) so as to reduce Γ_{dc} for minimum up-conversion of $^{1}/_{f}$ noise.

2.7 DESIGN OF VCO CORE

In the mm-wave range, LC oscillators are preferred to ring oscillators because of better phase-noise performance [**39**]. The most popular VCO topology in the mm-wave region is the differential Colpitts oscillator [**25**] [**40**], as shown in Figure 2.10. A differential configuration is preferred, especially at high frequencies, to minimise the generation and coupling of high-frequency signals. It also has the advantage of less criticality to on- and off-chip decoupling of supply and bias voltages due to the virtual ground node [**41**]. The differential architecture also minimises the substrate noise and power supply variation effects by rejecting common mode noise. The physical design process is also made simpler because of the virtual grounds in differential circuits.

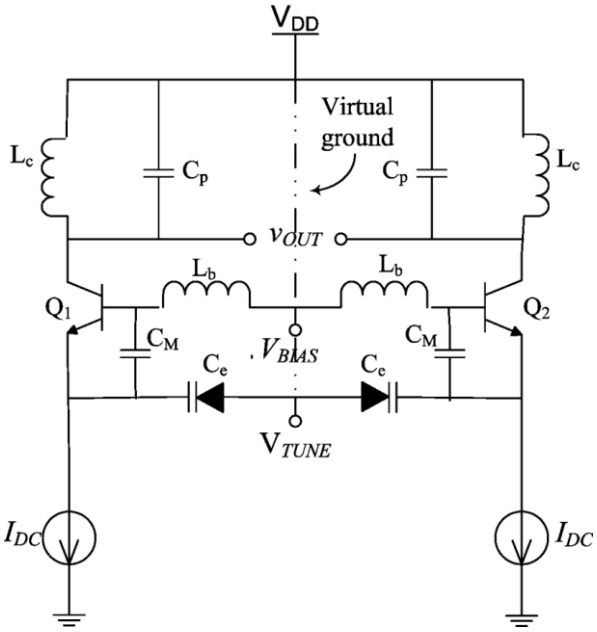

Figure 2.10. Differential Colpitts oscillator topology [20] (Reproduced by permission from J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*, Norwood, MA: Artech House, Inc., 2003. © 2003 by Artech House, Inc.)

The impedance between the base of transistor Q_1 in Figure 2.10 and the virtual ground shows a capacitive reactance, which resonates when an inductor (L_b) is connected across it. This could be seen from the analysis of the basic Colpitts oscillator core, as in Figure 2.11.

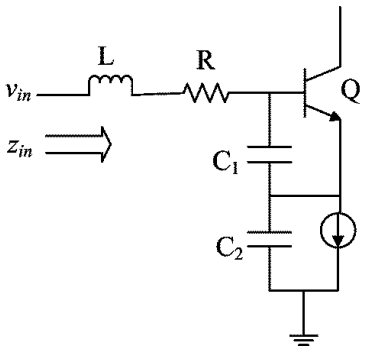

Figure 2.11. Oscillator core analysis

$$z_{in} = j\omega L + R + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2} \tag{2.32}$$

Therefore, the condition for oscillations is given by

$$\frac{g_m}{\omega^2 C_1 C_2} > R_B \tag{2.33}$$

The varactor (C_e) in Figure 2.10, which forms C_2 in Figure 2.11, helps in tuning the VCO, using the bias voltage V_{TUNE}. The B-E capacitance of the transistor usually forms C_1 and an additional capacitance in parallel could be placed if required by the design. The VCO core should be followed by a buffer for decoupling the load from the core [**42**], and a cascode buffer would be advantageous in terms of lower power consumption.

2.7.1 Design considerations

In this section, the design considerations identified in the literature study undertaken for a high-performance VCO are discussed.

As phase noise decreases with the quality factor, a high Q LC tank is the primary requirement for a low-noise design. In the mm-wave frequency range, the Q of the tank is limited by the varactor Q, unlike in the case of low-frequency designs where the tank Q is dominated by the inductor Q [**43**]. This is because high quality inductors with superior isolation could be realised using transmission lines in the mm-wave range. This was true for the IBM 130 nm process, where high Q inductors were realised using microstrip lines but varactor Q was just around 6 (see Chapter 5).

Varactors available in the process need to be carefully studied to know their suitability for the design. It has been demonstrated that minimum gate width (to reduce gate resistance) and minimum gate length (to reduce channel resistance) for MOS varactors and minimum anode size for junction varactors are required to attain a high Q. It has also been observed that increasing the varactor size tends to increase the total Q of the tank, though not that of the varactor Q [**40**].

The VCO core consists of the LC tank and a negative resistance applied as feedback to compensate for the losses in the LC tank. A tapped capacitor and an amplifier form the feedback in a Colpitts oscillator. A summary of the design methodology followed in VCO design in the literature is given on the next page.

i. The voltage swing across the tank is set to the maximum allowed for the safe operation area of the transistor and the smallest inductor size is chosen for the tank (for low phase noise)

ii. The transistors are biased at optimum noise current density [**44**]. (In the W-band, optimum noise current density is seen to shift towards the peak f_T current density because of the correlation between base and collector noise currents [**40**])

iii. The transistor and the varactor size, and the capacitance ratio C_1:C_2, should be scaled for minimum phase noise.

The normal VCO topology has low phase noise performance and a narrow tuning range due to parasitics interfering with the core. The high-frequency noise generated by the current source adds to the noise of the VCO core. The tuning range is also reduced, because of the parasitic capacitance C_{par} of the output current source, which shunts the varactor capacitance, as shown in Figure 2.12(a).

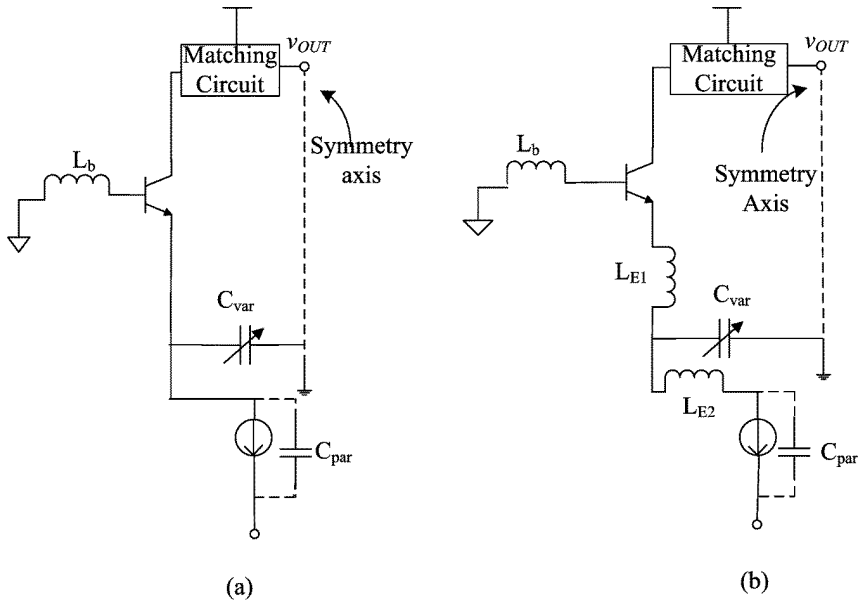

Figure 2.12. (a) Normal VCO topology showing the current source parasitic and (b) LC filtering technique to improve phase noise and tuning range [22**] (© [2003] IEEE)**

To improve the phase noise performance of the VCO, an LC filtering technique [**22**] could be used. The LC filtering technique using inductors at the emitter, as shown in Figure 2.12(a), can improve the phase noise performance and tuning range of the VCO. L_{E2} forms

a low-pass LC filter and thus helps in decoupling the high-frequency noise generated by the current source from the core of the oscillator. It also prevents C_{par} from shunting the varactor capacitance. L_{E1} is said to increase the loaded quality factor of the tank and thus improves the phase noise. A VCO with the LC filtering technique is seen to demonstrate a relatively high FOM [**22**]. An output buffer added to decouple the oscillator core from the external load is also reported to demonstrate better phase noise performance [**45**]. It also helps in obtaining large output power. HBT cascode, common source amplifier and MOS-HBT cascade are the possible options for the implementation of a buffer [**40**].

2.8 IMPLEMENTATION OF VECTOR-SUM INTERPOLATOR

The vector-sum interpolator requires I and Q signals to be interpolated to generate the necessary phase shift. The quadrature generation could be performed using passive devices to reduce power consumption and the interpolation could be performed with active devices.

The quadrature signal for the vector sum phase-shifting method could be generated from the VCO output. The I/Q phase accuracy of the generated quadrature phase signal is important, though the amplitude variations could be adjusted with the gain of the VGAs following the phase shifters.

2.8.1 Lange couplers

Lange couplers as shown in Figure 2.13 are passive devices that could be used for quadrature signal generation [**46**]. They are popular in the mm-wave region because of their low insertion loss. A D-band Lange coupler in a 0.13 µm SiGe BiCMOS technology is reported to have an insertion loss of 0.7 dB at the centre frequency of 140 GHz [**47**]. A Lange coupler implemented in the IBM 0.13 µm SiGe process using the top thick AM layer has a 42 Ω characteristic impedance and an insertion loss of 1.8 dB [**14**] .

The design parameters of a Lange coupler, are the voltage coupling coefficient (c) and the even and odd mode characteristic impedances ($Z_{o,even}$ and $Z_{o,odd}$).

$$Z_{0,even} = Z_0\sqrt{\frac{(1+c)}{(1-c)}} \tag{2.34}$$

$$Z_{0,odd} = Z_0\sqrt{\frac{(1-c)}{(1+c)}} \tag{2.35}$$

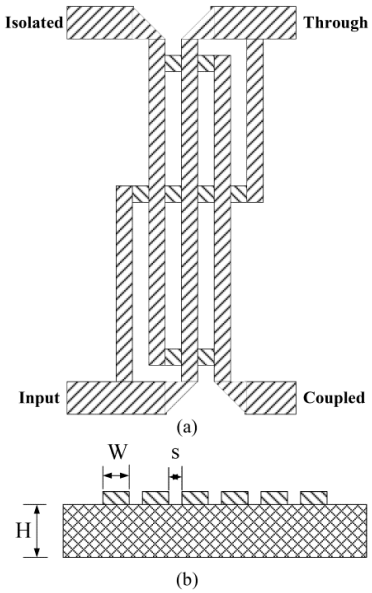

Figure 2.13. (a) Lange coupler (b) Cross-section of Lange coupler [48] (© [2009] IEEE)

As observed in Figure 2.13, the Lange coupler consists of four interconnected metal lines. There is a 90° phase difference between the through and coupled ports, and hence it is a quadrature hybrid [**46**].

2.8.2 Design of VGA

The vector interpolation requires a VGA to interpolate the I and Q signals. A VGA could be implemented using a Gilbert mixer topology as in Figure 2.14 [**20**]. The gain control voltage is applied to transistors $Q_{3\text{-}6}$ to steer the currents in the branches, which are then passed through the loads to provide an output voltage.

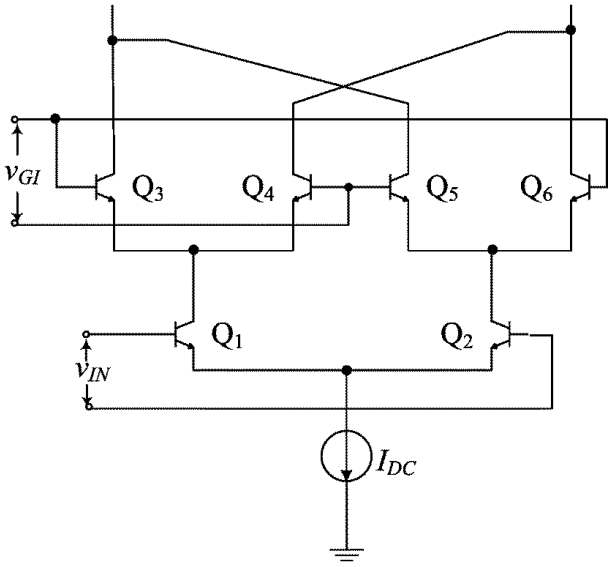

Figure 2.14. Variable gain amplifier [20**]** (Reproduced by permission from J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*, Norwood, MA: Artech House, Inc., 2003. © 2003 by Artech House, Inc.)

The currents i_3 , i_4, i_5, i_6 in transistors Q_3, Q_4, Q_5, Q_6 respectively in Figure 2.14 are given by (2.36)

$$\begin{aligned} i_3 &= \frac{i_1}{1+e^{-v_{GI}/v_T}} \\ i_4 &= \frac{i_1}{1+e^{v_{GI}/v_T}} \\ i_5 &= \frac{i_2}{1+e^{v_{GI}/v_T}} \\ i_6 &= \frac{i_2}{1+e^{-v_{GI}/v_T}} \end{aligned} \tag{2.36}$$

Assuming symmetrical collector resistors R_C, the output voltage is given by (2.37)

$$v_o = (i_1 - i_2)R_C = ((i_3 + i_4) - (i_5 + i_6))R_C = -2R_C I_{DC} \tanh\left(\frac{V_{GI}}{2v_T}\right)\tanh\left(\frac{v_{IN}}{2v_T}\right) \tag{2.37}$$

2.9 MILLIMETRE-WAVE DESIGN CHALLENGES

In the mm-wave range, the chip dimensions are in the order of the wavelength, hence MMIC designers need to account for distributed effects in the interconnects. The approach has been that the individual blocks, such as amplifiers, mixers, oscillators etc, are designed as lumped circuits and are interconnected to one other using transmission lines, which have a distributed nature. This traditional approach is said to give way to a new class of holistic circuit design technique combining device physics, circuits, and electromagnetics [**11**]. However, The author of this thesis feels that the modular approach helps to analyse and efficiently design the individual circuit blocks that can be employed in a wide range of applications. Hence, the traditional approach will be followed in this thesis, thus optimising the VCO design and its associated phase shifter circuitry, which could be incorporated as a module in phased-array systems.

The challenges faced in such a modular design approach are discussed in the following subsections.

2.9.1 Substrate effects

The finite conductivity of Si substrate causes energy loss due to magnetically induced eddy currents. Additional losses are caused due to the coupling of energy back into the substrate by the transmitting antennas. The passive devices also cause energy loss due to the small skin depth at mm-wave frequencies (at 60 GHz, Cu has a skin depth of 300 nm). The high dielectric constant of the Si substrate ($\varepsilon_r = 11.7$) can cause the rectangular Si substrate to act as a dielectric waveguide sustaining undesirable propagation modes in the mm-wave range. This may cause energy leakage into the substrate modes and cause parasitic coupling between different on-chip components. The substrate effects are pronounced in the mm-wave range and have significant effects on the design performance. Therefore, techniques to shield these effects or to model them accurately should be implemented to obtain the desired performance. One such technique would be the lower grounding metal in the microstrip line, which helps shield the substrate loss very effectively.

2.9.2 Packages and module design

The various packaging solutions possible for the 60 GHz chipsets are multi-layer low temperature co-fired ceramic technology and standard RF solutions such as ball grid array surface mount packages, direct-chip attachment to FR4 PCB laminates and liquid crystal polymer substrates with superior 60 GHz properties.

The high-frequency interface to the outside world also causes matching problems. The two most common techniques to attach the die to the package are using bond wires or flip-chip technology [**49**]. If the chip is to be connected to a perfectly matched transmission line on a printed circuit board using a wirebond, it would present an impedance of 12 Ω + *j*360 Ω at 60 GHz (modelling a 1 mm long wirebond as a 1 nH inductor with a *Q* of 30 [**11**]). This impedance match would be very difficult to attain using the conventional approach. At mm-wave frequencies, it can behave as an unintended radiative element, thus causing problems at the system level. In a flipchip technology, the series inductance is about an order of magnitude lower than the bondwire and is attractive for applications above 10 GHz and provides excellent performance up to 100 GHz [**50**]. In order to achieve low reflections at the interconnect, a smaller transition area should be considered to attain a higher operating frequency. The first-order parameters in the mm-wave frequency range are the bump diameter and the bump-pad area. If wirebond is used, the structure should be made be made to emulate a transmission line [**7**]. These constraints would make the measurement of the chip's performance difficult, as the interconnect characteristics influence the final measurements. Hence the MMIC in this work was measured at the wafer level.

2.10 CONCLUSION

A literature survey on mm-wave oscillators has been performed and the most popular configuration, optimal in terms of performance parameters such as phase noise, area etc, was identified as the cascode configuration of the Colpitts oscillator. The modelling of phase noise in oscillators was studied to understand how the flicker noise in the transistors is converted to the phase noise of the oscillators. The LTV model developed by Hajimiri and Lee (Section 2.6.2) was found to be accurate in predicting the phase noise in terms of

the ISF of the noise sources at the tank. It was found that modelling using the ISF would lead to an analytical expression for phase noise in terms of design and process parameters. This would help in enhancing the design performance, by optimising the identified parameters that affect the phase noise. Some of the design techniques that were implemented in the earlier works, such as inductor filtering, will be used in the current research to optimise the phase noise performance. The study also included identifying circuit techniques to realise vector-sum interpolation to obtain multiple-phase VCO signals that could be fed to the mixers in the signal path of the phased-array architecture. The topology will be simulated to quantify its performance and thus determine its suitability in phased-array implementations.

CHAPTER 3: RESEARCH METHODOLOGY

3.1 INTRODUCTION

Chapter 2 provided a review of the literature on mm-wave VCOs, and also identified the most popular VCO topology. The major criterion for topology selection was the phase noise performance. It was noted that the quality factor of the passives in the tank plays a major role in determining the phase noise. This has necessitated analysis of the performance of the passives in the process, which was the first step undertaken in the research. To save design cycle time, only the standard components available in the process were used for the design. Part of the research methodology was to identify the methods to analyse the phase noise performance, in particular to use the LTV model to optimise the parameters to improve the design. The last section of the chapter involved a study of the measurement setup, so that the final chip layout could be performed to adhere to any specific setup requirements of the measuring equipment.

3.2 INTEGRATED CIRCUIT PROCESS

The process selected for the design and fabrication is the IBM 8HP 0.13 µm SiGe BiCMOS process available through MOS implementation systems (MOSIS). The chip was to form part of a multi-project wafer (MPW) run offered by MOSIS educational programme (MEP) for the process. The 0.13 µm process has HBTs with f_T of 200 GHz and it also offers varactors and transmission lines necessary for VCO implementation [**51**] [**52**]. It has five metal layers, which could be used to interconnect; the bottom three metal layers, M1, M2 and MQ, are made of copper and the top two, LY and AM, are aluminium layers.

3.2.1 SiGe HBT characteristics

The IBM 8HP process has *npn* models that support only single stripe emitter geometry and has a c-b-e-b-c layout for the high f_T device. The single stripe emitter has a fixed width of 0.12 µm and emitter length could be varied from 0.52 µm to 18 µm. The transistors have polysilicon emitters with a non-self-aligned extrinsic base. It was noted earlier that the

transistors should be biased at the optimal noise current density to improve the phase noise performance. Another important electrical parameter of importance is the open base C-E breakdown voltage of the transistor (BV_{CEO}). It restricts the maximum possible swing across the transistors, which in turn determines the phase noise performance. The design has restricted the voltage swing to below the nominal BV_{CEO} of 1.7 V for guaranteed safe operation. The range of values of the device characteristics of HBTs for increasing emitter length dimensions from 0.52 to 12 µm are given in Table 3.1, the exact values are not disclosed due to NDA.

Table 3.1. NPN device characteristics of IBM 8HP process

Device Parameter	**Drawn Emitter Dimensions (µm) (W = 0.12)**
	L = 0.52 - 12
Extrinsic R_e (Ω)	38 - 1.5
Extrinsic R_b (Ω)	236 - 13
Intrinsic R_b (Ω)	125 - 5
Extrinsic R_c (Ω)	51 - 4
Intrinsic R_c (Ω)	198 - 6
BE Intrinsic cap (fF)	0.6 - 18
BE Oxide cap (fF)	0.8 - 18
BC Extrinsic cap (fF)	0.1 - 1.4
BC Intrinsic cap (fF)	0.5 - 9
BC Oxide cap (fF)	1 - 9
CS Intrinsic cap (fF)	0.075 - 0.6
Peak f_T I_C (mA)	0.75 - 17

It can be observed from Table 3.1 that the extrinsic resistances decrease with size, while the capacitances increase with the size of the transistors. This is expected, as resistance varies inversely with the cross-section area, whereas capacitance is proportional to the area of cross-section.

3.2.2 Inductors

Spiral inductors in the process are available only in the range 0.15 – 35 nH. Millimetre-wave designs usually require very low inductance values in the range of pHs. Inductors with a very low inductance value could be implemented using *rfline* or shorted microstrip lines.

The *rfline* device provides a transmission line structure with an accurate high-frequency model. It is typically used as an inductive element for applications requiring very low inductance with a relatively high quality factor. It has AM over a DT lattice and the available size range from 100 µm $\leq L \leq$ 1500 µm and 4 µm $\leq W \leq$ 25 µm. The 8HP process also offers microstrip transmission lines, namely *singlewire* and *coupledwires*, which incorporate one or two wires, a metal ground plane and optional side shields. These could be shorted at the end or connected in the circuit as a virtual short to present a low inductance, as the design demands. The line and the ground plane levels could be chosen by the designer.

3.2.3 Capacitors

The IBM 8HP technology provides variable capacitance (*ncap*, *dgncap*, *havar*) and fixed capacitance (*mim).*

The nMOS varactors, which are thin (*ncap*) or thick oxide (*dgncap*) NFET-in-Nwell MOS capacitors operate between depletion (gate negative) and accumulation (gate positive). The hyper-abrupt varactor (*havar)* is a p^+/n junction created from the p^+ S/D implant and it operates in the reverse-bias mode. An additional *n*-type implant below the junction creates a more linear varactor with a large tuning range.

The fixed capacitance is a single nitride metal-insulator-metal (*mim*). It uses an optional mask QY, which is the top aluminum metal capacitor plate and is separated from the aluminum metal level bottom plate LY by a thin nitride dielectric layer.

The MOS varactors have the highest area capacitance among all the four, with the *ncap* topping the list due to the thin oxide layer.

The *ncap* and *dgncap* p-cells generate an array of wired varactor gates, consisting of diffusion islands that are constituted by the *nrep* parameter and also the number of gates constituted by the *nf* parameter. The wiring parasitic resistance and capacitance corresponding to the array layout are included in the model. The aspect ratio of *mim* capacitors should not be larger than 3:1 to assure accurate modelling, and the quality factor of *mim* decreases with the aspect ratio.

All the varactors have a parasitic junction between the *n*-type region and the substrate. This is the subcollector/substrate junction for the *havar* and *n*-well/substrate junction for the nMOS varactors. Hence, the varactors in the circuit should be operated in such a way that the *n*-type region is ac grounded. Otherwise, the parasitic junction will be excited in parallel with the varactor junction, thus deteriorating the tuning properties and *Q*. Thus, for the *havar*, anode excitation is preferred and for the nMOS varactors, gate excitation is preferred.

3.2.4 Resistors

The IBM 8HP process provides four types of resistors and they are ranked according to the value of their sheet resistances in the increasing order in Table 3.2.

Table 3.2. 8HP resistors

Specification	***NS* diffusion**	**P^+ poly**	***RR* poly**	***KQ BEOL***
R_S [Ω/sq] (0 V, 25° C)	I	III	IV	II

According to Table 3.2, the diffusion resistor has the lowest sheet resistance, while the polysilicon one has the highest, with the high-resistance polysilicon (RR poly) one topping the list. The KQ resistor is made of a KQ metal layer, which is above the MQ layer, with end contacts using VY vias connecting to the LY layer. The design values of the resistances and their current handling capability form the basis of the selection criteria for the resistors.

3.3 PHASE NOISE MODELLING IN THE $1/f^2$ REGION USING THE ISF THEORY

The process of up-conversion from device flicker noise to the phase noise near the oscillating frequency could be explained using the LTV model for the oscillators (Section 2.6.2). The effect of various noise sources on the output was evaluated, using their ISF. The approach could be used in deriving the phase noise expression for a circuit configuration, to analyse how the device noises in the circuit could be up-converted. This would help in optimising the circuit performance by optimising any process and design parameters that would influence the phase noise performance. An analysis of the common collector Colpitts configuration and the contribution of the active device noise sources, such as base resistance thermal noise and collector current shot noise, could be deduced using the ISF approach. This will be detailed in Chapter 4 of this thesis.

3.4 OSCILLATOR SIMULATIONS IN CADENCE (PSS, PNOISE)

The complex process of conversion from component noise to phase noise could be evaluated with the help of advanced circuit simulators. SpectreRF from Cadence design systems is a SPICE based circuit simulator that can compute steady-state solutions and also perform simulation on circuits that translate frequency, which are common in RF circuit design. The features that are useful in oscillator simulation include the periodic steady state (PSS) and PNoise capability of the simulator [**53**].

PSS analysis is an extensive signal analysis that can compute the steady-state response of the circuit, which will later be used in performing periodic small signal analyses. It can handle both autonomous (non-driven) and non-autonomous (driven) circuits. Oscillators

fall into the category of autonomous circuits, which are time-invariant circuits that have time-varying responses. An estimate of the oscillation period is specified by the user and PSS analysis computes the precise period. PSS can also be used to compute the periodic solution waveforms. PSS analysis for oscillators (autonomous circuits) requires a pair of nodes to be specified; the potential difference between the two is monitored and used in the transient phase of the PSS, which is the first phase of the PSS analysis.

PSS analysis has two phases – (a) an initial transient phase, and (b) a shooting phase.

The initial transient phase initialises the circuit and has three intervals. The first interval starts at *tstart* (which is normally zero) and continues through the onset of periodicity of the independent sources, *tonset* (this is also zero in the case of oscillator analysis). The second is the *tstab*, the optional stabilisation interval. The final phase exclusive to the autonomous PSS analysis, monitors the waveforms in the circuit for a length of four times the specified estimate of the oscillation period, and thus a final estimate of the oscillation period is derived.

The shooting phase, which computes the periodic steady-state solution using the shooting method, starts after the initial transient phase has been completed. In this phase, multiple simulations of the circuit are performed over a period. An estimate of the initial condition is generated for a transient analysis with an interval *period*, such that the final state matches the initial state. A transient analysis is performed and the mismatch is calculated. If it does not meet the convergence criterion, another estimate has to be generated, and it repeats the process until convergence is achieved. In general, the process will need about three to five iterations to obtain a steady state solution. Typically, PSS can simulate the nonlinear circuit behaviour within the shooting interval, and this is the strength of the shooting method over other steady-state methods such as harmonic balance [**53**].

SpectreRF thus computes the periodic steady state of the oscillator using PSS analysis. It then linearises the system around this trajectory, to obtain a time-varying linear system to proceed with the calculation of noise power density.

Virtuoso Schematic Editor and Virtuoso Layout Editor from Cadence were used respectively for the schematic and layout design entries. The DRC/LVS tool used was Assura, which is also integrated into the Cadence Virtuoso software suite.

3.5 MEASUREMENT SETUP AND EQUIPMENT

As discussed in chapter 2, on-wafer measurements were performed to characterise the MMIC device under test (DUT). The measurements were performed with the help of a probe station; hence the pad's layout and its pitch should adhere to the specifications of the probe used. Figure 3.1 shows a block diagram of the entire measurement setup.

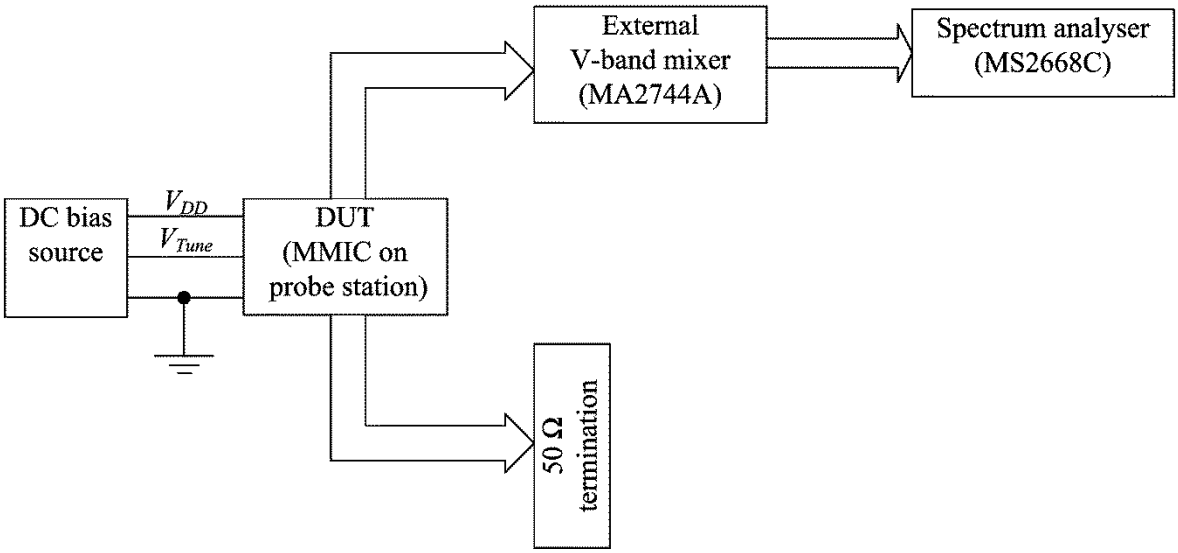

Figure 3.1. Block diagram of the measurement setup

As seen in Figure 3.1, the PCB was placed on the wafer probing station, and is thus the DUT for measurement purposes. The ground-signal-ground (GSG) pads on either side of the MMIC were contacted with GSG probes attached to a PM5/Suss MicroTec probe station. One side of the probe was terminated with a 50 Ω termination and the other was connected to the spectrum analyser channel for measurements. The PM5/Suss MicroTek is shown in Figure 3.2. It allows wafer or substrate measurements of up to 6 inches.

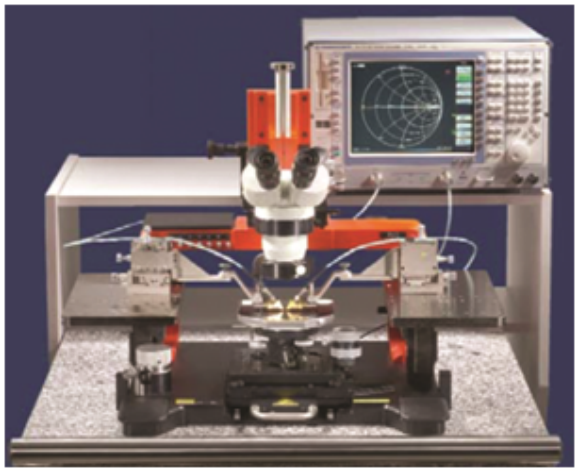

Figure 3.2. PM5/Suss MicroTec Probe Station

The Picoprobe model shown in Figure 3.3, which is a 67A DP-type mounting style, was used for the measurements. The probe has a frequency range from DC to 67 GHz and the pitch is 150 µm.

Figure 3.3. Picoprobe model 67A DP-style

The spectrum analyser used was the Anritsu MS2668C (9 kHz – 40 GHz), shown in Figure 3.4. It was extended to operate for 50-75 GHz by connecting an external V-band mixer (MA2744A).

Figure 3.4. Anritsu MS2668C

3.6 CONCLUSION

This chapter discussed the methodology followed in the research. It outlined the PDK, the simulation software and finally, the measurement setup and equipment that was used to characterise the MMIC to validate the hypothesis.

CHAPTER 4: ANALYTICAL MODELLING

4.1 INTRODUCTION

This chapter deals with the mathematical analysis of the common collector Colpitts oscillators, in order to analyse the effects of design and process parameters on the oscillator performance [**54**]. To aid the design process, an attempt has been made to study the contribution of major phase noise sources in an oscillator analytically. In this work, the approach followed was to identify the dominant noise sources in the circuit and to obtain closed-form expressions for its contribution to phase noise by evaluating their ISF. A basic core of the differential common collector Colpitts oscillator is shown in Figure 4.1.

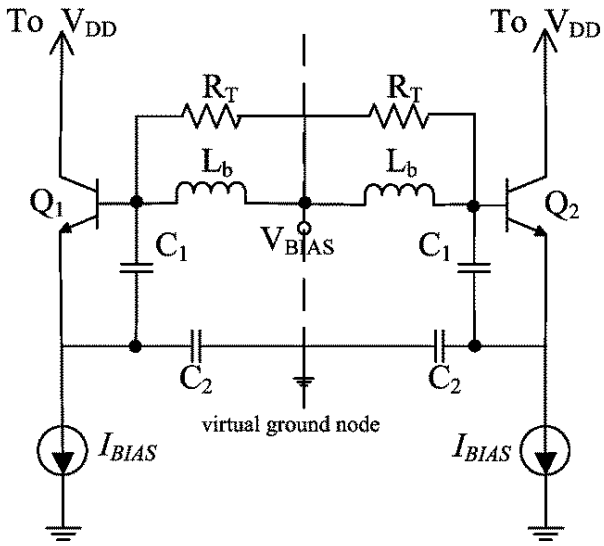

Figure 4.1. Differential common collector Colpitts oscillator

As seen in Figure 4.1, it comprises two half-circuits consisting of Q_1, L_b, C_1 and C_2. R_T models the total tank resistance, mainly contributed by the passives in the tank and I_{BIAS} is the bias current for a half circuit.

4.2 OSCILLATION AMPLITUDE

The oscillator will be driven by a large sinusoidal signal at the base, provided the tank has a reasonable Q, as shown in Figure 4.2.

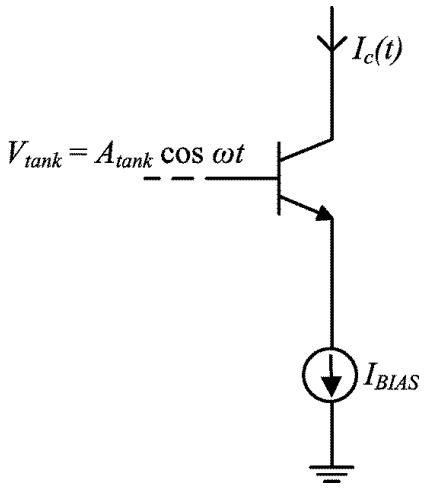

Figure 4.2. Transistor driven by the sinusoidal tank voltage

In Figure 4.2, the transistor is ON only for a part of an oscillation cycle, during which it delivers a large pulse of current $I_c(t)$ with a fundamental component I_1 in the tank. The large signal transconductance G_m of the transistor is given by (4.1), where V_1 is the B-E voltage of the transistor.

$$G_m = \frac{I_1}{V_1} \tag{4.1}$$

Thus the equivalent circuit of the oscillator could be modelled with the transistor T-model, as shown in Figure 4.3, which has a current generator of I_1 and a large signal B-E resistance $r_e = 1/G_m$

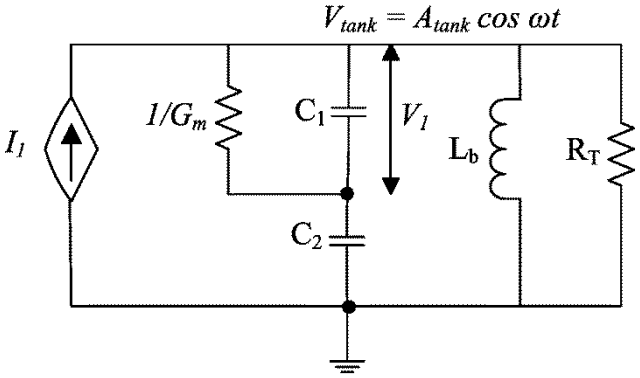

Figure 4.3. Equivalent T-model of the common collector Colpitts oscillator with large signal G_m

As noted from Figure 4.3, the resonator voltage will be the fundamental current times the total equivalent resistance seen across the tank,

$$A_{tank} = I_1 R_{total} \tag{4.2}$$

The total resistance seen across the tank comprises the resonator losses and the loading of the transconductor on the resonator. The transconductor presents the impedance as in (4.3)

$$\frac{1}{G_m}\left(\frac{C_1+C_2}{C_2}\right)^2 = \frac{1}{G_m n^2} \tag{4.3}$$

where design parameter n is the ratio of the capacitors or the equivalent impedance transformation ratio given by (4.4)

$$n = \frac{C_2}{C_1+C_2} \tag{4.4}$$

Thus the total resistance is given by (4.5)

$$R_{total} = R_T \,//\, \frac{1}{G_m n^2} = \frac{R_T}{1+G_m n^2 R_T} \tag{4.5}$$

Thus A_{tank} will be given by (4.6)

$$A_{tank} = I_1 \frac{R_T}{1+G_m n^2 R_T} \tag{4.6}$$

Substituting (4.1) and (4.7) in (4.6) would give the expression for A_{tank} as in (4.8)

$$V_1 \approx n A_{tank} \tag{4.7}$$

$$A_{tank} \approx 2 I_1 R_T (1-n) \approx I_1 R_T (1-n) \tag{4.8}$$

The preliminary investigation shows that the amplitude is controlled by the design parameter, capacitive divider ratio n.

4.2.1 Analytical expression for fundamental current i_{fund}

In this subsection, an expression for the fundamental current I_1 is derived to investigate the effect of the design parameter further. Defining A_e as the base-emitter junction signal voltage and V_{BE} as the bias voltage across the junction, the collector current could be written as in

$$A_e = n A_{tank} \tag{4.9}$$

$$I_c(\phi) = I_s e^{\frac{V_{BE}+A_e\cos\phi}{V_T}} \tag{4.10}$$

where I_s is the BJT saturation current and

$$V_T = \frac{k_B T}{q} \tag{4.11}$$

The average value of the transistor current should be equal to the bias current I_{BIAS}.

$$I_{BIAS} = \frac{1}{2\pi}\int_{-\pi}^{+\pi} I_c(\phi)d\phi = \frac{1}{2\pi}\int_{-\pi}^{+\pi} I_s e^{\frac{V_{BE}+A_e\cos\phi}{V_T}} d\phi \tag{4.12}$$

The modified Bessel function of the first kind is given by (4.13)

$$B_m(x) = \frac{1}{\pi}\int_0^{\pi} e^{x\cos t}\cos(mt)dt \tag{4.13}$$

where m is the order of the $B_m(x)$. Equation (4.12) could be re-written in terms of the modified Bessel function of the first kind of order zero, $B_0(A_e/V_T)$,

$$I_{BIAS} = I_s e^{\frac{V_{BE}}{V_T}} B_0\left(\frac{A_e}{V_T}\right) = I_s e^{\frac{V_{BE}}{V_T}} B_0(a_e) \tag{4.14}$$

where

$$a_e = \frac{A_e}{V_T} \tag{4.15}$$

Thus V_{BE} is derived as

$$V_{BE} = V_T \ln\left(\frac{I_{BIAS}}{I_s . B_0(a_e)}\right) \tag{4.16}$$

The first harmonic I_1 of the transistor current is given by Fourier's theory as

$$I_1 = \frac{1}{\pi}\int_{-\pi}^{+\pi} I_c(\phi)\cos(\phi)d\phi = \frac{1}{\pi}\int_{-\pi}^{+\pi} I_s e^{\frac{V_{BE}+A_e\cos\phi}{V_T}}\cos(\phi)d\phi \tag{4.17}$$

This could be written in terms of the modified Bessel function of the first order $m = 1$

$$I_1 = 2I_s e^{V_{BE}/V_T} . B_1(a_e) = 2I_{BIAS}\frac{B_1(a_e)}{B_0(a_e)} \tag{4.18}$$

4.3 PHASE NOISE CONTRIBUTION FROM ACTIVE DEVICE NOISE SOURCES

In this work, the phase noise contribution of active device noise sources, such as the collector current shot noise, base current shot noise and base resistance thermal noise, as shown in Figure 4.4, is analysed for a common collector configuration. The symbolic ISF expression of the noise source of LC-tank (2.28) is used for predicting the ISFs associated

with the transistor noise sources. The ISF of an individual noise source is calculated by injecting current impulse in parallel to the noise source and its effect on the tank capacitance is evaluated by using small-signal model circuit analysis. Finally, a closed-form expression for the *1/f*^{2} phase noise in LC-oscillators is obtained so that the researcher could obtain insight into the variation of the phase noise in relation to circuit design parameters and process parameters.

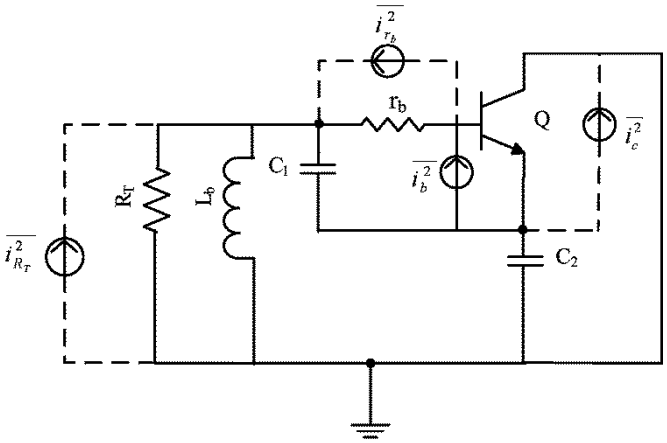

Figure 4.4. Active device noise sources

From Figure 4.4, the base current shot noise contribution is neglected, as it is very small [**55**]. The tank resistance R_T causes a phase noise at offset frequency $\Delta\omega$ given by (2.28), which could be re-written in terms of tank voltage A_{tank} and tank capacitance C as in (4.19)

$$L(\Delta\omega) = 10\log\left(\frac{\Gamma_{R_T,rms}^2}{q_{\max}^2} \bullet \frac{\overline{i_{R_T}^2}/\Delta f}{2\Delta\omega^2}\right) = 10\log\left(\frac{\Gamma_{R_T,rms}^2}{A_{tank}^2 C^2} \bullet \frac{\overline{i_{R_T}^2}/\Delta f}{2\Delta\omega^2}\right) \tag{4.19}$$

where $\overline{i_{R_T}^2}/\Delta f$ is the power spectral density of white noise generated by the tank resistance R_T given by (4.20) and Γ_{R_T} is the ISF of the noise source due to tank resistance R_T.

$$\frac{\overline{i_{R_T}^2}}{\Delta f} = \frac{4k_B T}{R_T} \tag{4.20}$$

The Γ_{R_T} for an LC tank differential oscillator [**55**] is given by (4.21),

$$\Gamma_{R_T}(\phi) = \frac{\sin(\phi)}{N} \tag{4.21}$$

where $N = 1$ for a single-ended oscillator and $N = 2$ for a differential oscillator.

The contribution of the collector current shot noise and base resistance thermal noise is evaluated by using their ISF. The approach followed to find the ISF of any noise source is to relate it to the ISF of the tank resistance, by evaluating the voltage change at the tank capacitance caused by the respective current impulses, as shown in the subsections below.

4.3.1 Phase noise contribution of collector current shot noise

When the collector current shot noise shown in Figure 4.5(a) is considered, (4.19) has to be modified to include the cyclo-stationary behaviour by using the effective ISF $\Gamma_{i_c,eff}$ given by

$$\Gamma_{i_c,eff}(\phi) = \Gamma_{i_c}(\phi).\alpha_{i_c}(\phi) \tag{4.22}$$

where the dependence of noise power on ϕ is taken into account by $\alpha_{i_c}(\phi)$.

$\Gamma_{i_c}(\phi)$ is found by injecting a current impulse of area ΔQ into the same oscillator node where the noise current flows, as in Figure 4.5(b).

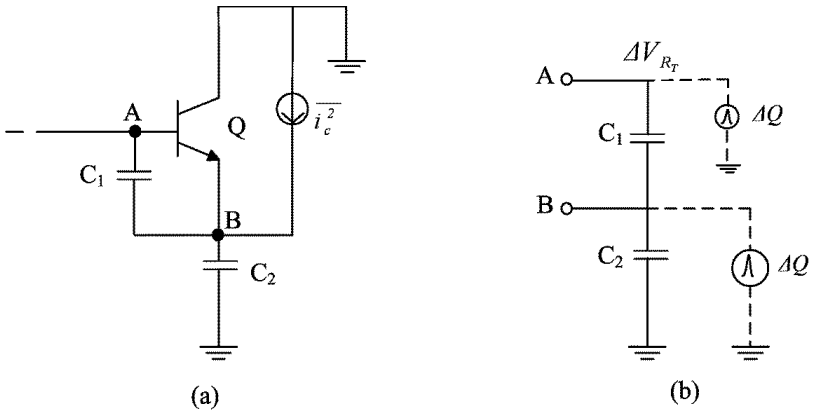

Figure 4.5. (a) Collector current shot noise in an oscillator (b) Circuit to calculate the ISF of collector current shot noise

In Figure 4.5(b), the voltage change ΔV_{R_T} across the tank capacitor caused by a current impulse of area ΔQ injected in parallel to the tank resistance at node A is given by

$$\Delta V_{R_T} = \frac{\Delta Q}{C} \tag{4.23}$$

where

$$C = \frac{C_1 C_2}{C_1 + C_2} \tag{4.24}$$

The voltage $\Delta V_{A,B}$ measured at node A, generated by a current impulse flowing into node B, is given by

$$\Delta V_{A,B} = \frac{\Delta Q}{C_2} = \frac{\Delta V_{R_T} C}{C_2} = \Delta V_{R_T} \frac{C_1}{C_1 + C_2} = (1-n)\Delta V_{R_T} \tag{4.25}$$

Hence the ISF of the collector current shot noise Γ_{i_c} is related to the ISF of the tank resistance, Γ_{R_T} according to (4.25) and substituting (4.21) would give the following:

$$\Gamma_{i_c} = (1-n)\Gamma_{R_T} = (1-n)\frac{\sin(\phi)}{N} \tag{4.26}$$

The periodicity information $\alpha_{i_c}(\phi)$ for calculating the effective ISF in (4.22) is obtained from the expression of collector current shot noise

$$\frac{\overline{i_c^2}}{\Delta f} = 2qI_c(\phi) \tag{4.27}$$

Substituting (4.10) in (4.27)

$$\frac{\overline{i_c^2}}{\Delta f} = 2qI_s e^{\frac{V_{BE} + A_e \cos\phi}{V_T}} = \frac{\overline{i'^2_c}}{\Delta f}\alpha_{i_c}^2(\phi) \tag{4.28}$$

where (4.11), (4.15) and (4.16) were used to define

$$\frac{\overline{i'^2_c}}{\Delta f} = 2qI_s e^{\frac{V_{BE}}{V_T}} = 2q\frac{I_{BIAS}}{B_0(a_e)} = \frac{2k_B T}{V_T}\frac{I_B}{B_0(a_e)} \tag{4.29}$$

and

$$\alpha_{i_c}(\phi) \equiv \sqrt{e^{a_2\cos(\phi)}} \tag{4.30}$$

Thus $\Gamma_{i_c,eff}(\phi)$ is defined as

$$\Gamma_{i_c,eff}(\phi) = \Gamma_{i_c}(\phi).\alpha_{i_c}(\phi) = (1-n)\frac{\sin(\phi)}{N}\sqrt{e^{a_e\cos(\phi)}} \tag{4.31}$$

The expression for $\Gamma_{i_c,eff}(\phi)$ is the same as that for a common base configuration [**55**], thus the expression for $L_{i_c}(\Delta\omega)$, the phase noise contribution of the collector current shot noise, is given by

$$L_{i_c}(\Delta\omega) = 10\log\left(\frac{k_B T(1-n)}{2NR_T nC^2 A_{tank}^2 \Delta\omega^2}\right) \tag{4.32}$$

4.3.2 Phase noise contribution of base resistance thermal noise

The noise contribution by the base resistance thermal noise in Figure 4.6 is calculated by relating the ISF of the noise source $\Gamma_{r_b}(\phi)$ to the ISF of the tank resistance $\Gamma_{R_T}(\phi)$

$$\Gamma_{r_b}(\phi) = \frac{\Delta V_{r_b}(\phi)}{\Delta V_{R_T}(\phi)} \Gamma_{R_T}(\phi) \tag{4.33}$$

where $\Delta V_{r_b}(\phi)$ is the voltage change across the tank capacitor caused by injecting a current impulse ΔQ parallel to r_b and as defined earlier, $\Delta V_{R_T}(\phi)$ is the voltage change across the capacitor caused by injecting a current impulse parallel to R_T and given by

$$\Delta V_{R_T} = \frac{\Delta Q}{C} \tag{4.34}$$

As $\Delta V_{r_b}(\phi)$ and $\Delta V_{R_T}(\phi)$ are both evaluated across the same tank capacitance, the ISF could be re-written as

$$\Gamma_{r_b}(\phi) = \frac{\Delta Q_{r_b}(\phi)}{\Delta Q(\phi)} \Gamma_{R_T}(\phi) \tag{4.35}$$

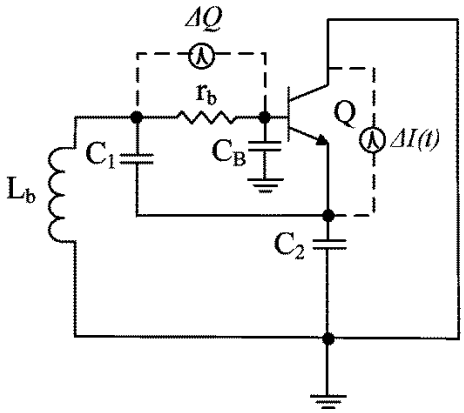

Figure 4.6. Circuit to calculate the ISF of base resistance thermal noise

The analysis is done by assuming a negligible parasitic capacitance at the base, C_B to the ground, as shown in Figure 4.6, and injecting a charge impulse in parallel to r_b at time t_0. C_B is in series with a relatively large tank capacitance C; hence the charge in the current impulse is collected by C_B and is discharged through the network C_B-r_b-C with a time constant $\tau = r_b C_B$ as $C_B << C$. The voltage at the base of the transistor is given by

$$V_{C_B}(t) = \frac{\Delta Q}{C_B} e^{-\frac{(t-t_0)}{\tau}} \tag{4.36}$$

This leads to an impulsive current given by the transistor transconductance and the base voltage according to

$$\Delta I(t) = g_m(\omega_0 t) V_{C_B}(t) = g_m(\omega_0 t) \frac{\Delta Q}{C_B} e^{-\frac{(t-t_0)}{\tau}} \tag{4.37}$$

It could be noted from Figure 4.6 that the ISF of the impulsive current $\Delta I(t)$ will be similar to that of the collector current shot noise $\Gamma_{i_c}(\phi)$ in Figure 4.5(a). The charge in the impulsive current $\Delta I(t)$ could be found as follows:

$$\Delta Q'_{r_b}(\phi) = \int_{t_0}^{\infty} \Delta I(t) dt = g_m(\phi) r_b \Delta Q(\phi) \tag{4.38}$$

The ISF associated with the base resistance thermal noise $\Gamma_{r_b}(\phi)$ is given by

$$\Gamma_{r_b}(\phi) = \frac{\Delta Q_{r_b}(\phi)}{\Delta Q(\phi)} \Gamma_{R_T}(\phi) = \left[\frac{\Delta Q_{r_b}(\phi)}{\Delta Q'_{r_b}(\phi)} \Gamma_{R_T}(\phi) \right] \frac{\Delta Q'_{r_b}(\phi)}{\Delta Q(\phi)} \tag{4.39}$$

$$\Gamma_{r_b}(\phi) = \Gamma_{i_c}(\phi) \frac{\Delta Q'_{r_b}(\phi)}{\Delta Q(\phi)} = \Gamma_{i_c}(\phi) g_m(\phi) r_b \tag{4.40}$$

Substituting (4.26) for $\Gamma_{i_c}(\phi)$ would give the following expression for $\Gamma_{r_b}(\phi)$:

$$\Gamma_{r_b}(\phi) = (1-n) \frac{\sin(\phi)}{N} g_m(\phi) r_b \tag{4.41}$$

This expression for $\Gamma_{r_b}(\phi)$ is the same as that for a common base configuration [**55**], hence the phase noise due to the base resistance thermal noise is given by

$$L_{r_b}(\Delta\omega) = 10 \log \left(\frac{k_B T I_{BIAS} r_b (1-n)}{2 N V_T R_T n C^2 A_{tank}^2 \Delta\omega^2} \cdot \frac{B_1(2a_e)}{B_0(a_e) B_1(a_e)} \right) \tag{4.42}$$

Thus the total phase noise for the common collector configuration is obtained by adding the individual contribution and is given by

$$L_{tot}(\Delta\omega) = 10 \log \left\{ \frac{k_B T (1+n)}{2 N R_T n C^2 A_{tank}^2 \Delta\omega^2} \cdot \left[1 + \left(\frac{I_{BIAS} r_b (1-n)}{V_T (1+n)} \cdot \frac{B_1(2a_e)}{B_0(a_e) B_1(a_e)} \right) \right] \right\} \tag{4.43}$$

The optimum value of the design parameter n for a mm-wave oscillator could be determined by plotting the phase noise for different values of n after substituting the following typical values from Table 4.1 in (4.43).

Table 4.1. Typical value of the design parameters at mm-wave

Design Parameter	Value
Temperature (T)	310 K
Oscillating frequency (f_{osc})	60 GHz
Bias current (I_{BIAS})	18 mA
Tank capacitance (C)	142 fF
Tank resistance (R_T)	100 Ω
Tank quality factor (Q)	6
Base resistance (r_b)	12 Ω

In Table 4.1, the tank Q is given by the Q of the varactor. The value of tank resistance R_T is obtained from tank capacitance and tank Q. The typical values when substituted in (4.43) give the phase noise for different values of n as in Figure 4.7.

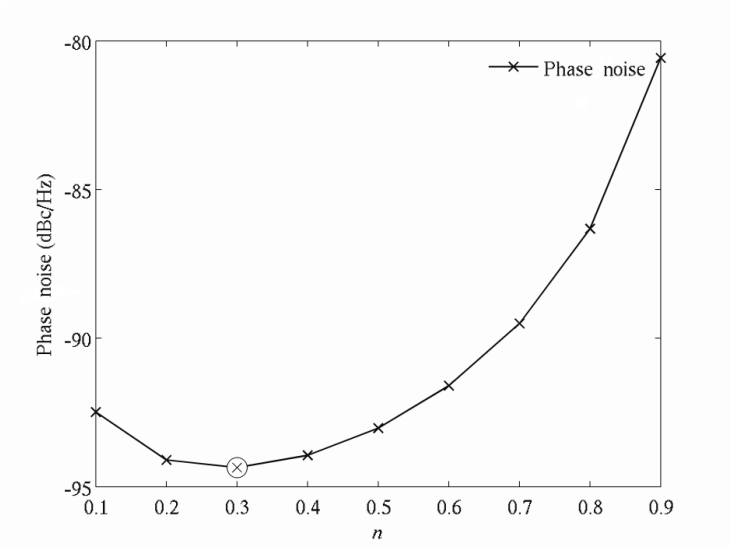

Figure 4.7. Phase noise for different values of n [26] (Publication resulting from this research work)

From Figure 4.7, the lowest value of phase noise is reported for a capacitors ratio of *n* around 0.3.

4.4 CONCLUSION

This chapter provided the LTV analysis of a differential common collector Colpitts oscillator. The ISF of individual noise sources were analytically derived and used to obtain an analytical expression for phase noise. The optimum value of the design parameter was then obtained by substituting the typical values of other parameters in the phase noise expression.

CHAPTER 5: CIRCUIT DESIGN AND SIMULATION

5.1 INTRODUCTION

This chapter details the design of the circuitry and discusses the circuit simulation results. The design is performed with IBM 8HP SiGe BiCMOS with the PDK. The optimum value of the design and process parameters obtained using the mathematical analysis in Chapter 4 has been taken into account. The simulations of the designed circuit were performed using SpectreRF from Cadence Virtuoso Suite with the PDKs from IBM, which provide the parameterised device models (p-cells) to aid the circuit designer.

5.2 DIFFERENTIAL COLPITTS OSCILLATOR

A cascode topology with a basic common collector oscillator core extended with a cascode buffer, as shown in Figure 5.1, was chosen for better isolation and stability.

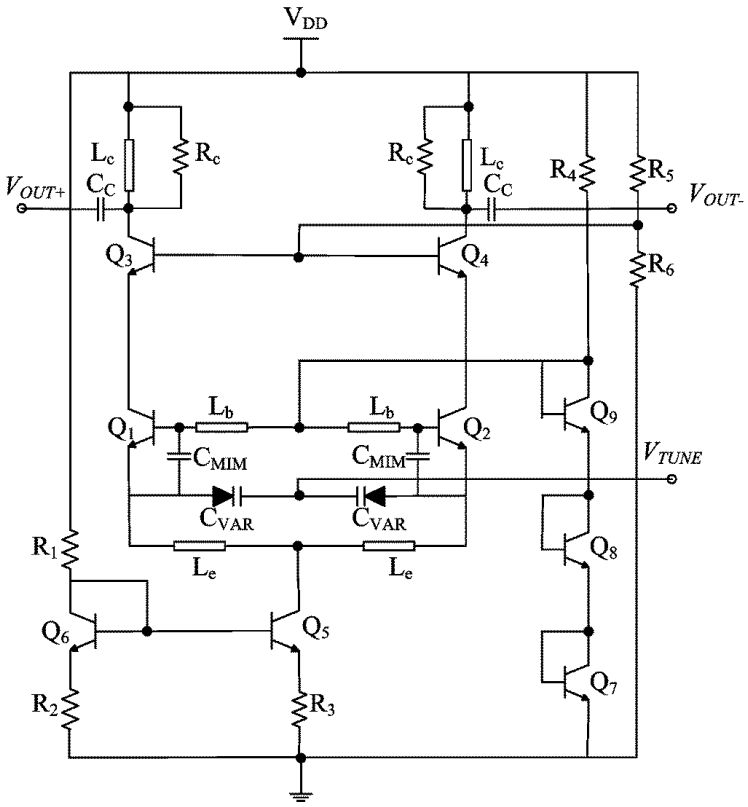

Figure 5.1. Circuit schematic of the 60 GHz VCO [26**]**

In Figure 5.1, the tank inductors L_b at the base of the transistors Q_1 (or Q_2) are presented with a negative real part and a capacitive reactance. This reactance is influenced by the varactor, $C_{VAR,}$ and helps in tuning the oscillation frequency. Q_3 and Q_4 form the cascode transistors to buffer the tank from the load. As Q_3 (or Q_4), is separated from the tank by Q_1 (or Q_2), its impact on phase noise is minimal. This is because noise sources of Q_3 (or Q_4) do not affect the voltage across the tank capacitance, formed by C_{MIM} and C_{VAR}. The inductors L_c at the collector of Q_3 and Q_4 form the output network designed to resonate at 60 GHz. Inductors L_e are placed in the emitter branch of the circuit to implement the LC filtering technique to reduce the phase noise contribution of the current source [**56**]. It also enables the use of a single current source instead of two. $Q_{5\text{-}9}$ and $R_{1\text{-}6}$ constitute the bias network of the circuit, which supplies the oscillator current and also provides appropriate bias voltages at the required nodes. The actual output network, which includes, R_c, L_c and also C_c, C_{pad} (not shown in the figure) should be designed to present a 50 Ω impedance to the measurement setup. This would require additional inductors at the output side to cancel out the bondpad parasitic (C_{pad}), which was not taken into consideration to simplify the design. As on-wafer measurements will be performed, the die would not be packaged and hence bondwire inductances were not taken into consideration during the design.

The design required setting up the maximum allowable voltage swing to be the nominal BV_{CEO} across the transistors for safe operation (1.7 $V_{p\text{-}p}$). Simulations were performed to decide on transistor size, as it is required to bias the transistors at optimum current density. The current in the circuit was determined based on the amount of negative resistance required to compensate for the losses in the tank and also maximise the output power that can be obtained in the transistor safe operating area. Transistors were sized to operate at optimum current density, the transistor size was W = 0.12 µm and L = 18 µm (the width was fixed for the process and the length was the largest available in the process). In addition, the larger sized transistors have lower extrinsic and intrinsic resistances, which reduce the thermal noise contribution to phase noise, even though the influence on the tuning range by the device parasitic capacitance is higher.

The circuit operates with a V_{DD} of 4 V and the current source supplies about 35 mA.

5.3 DESIGN OF THE PASSIVE COMPONENTS

As the quality factor of the passives in the tank play a major role in determining the phase noise, care should be taken to employ good quality passives in the tank for the realisation of the VCO.

5.3.1 Inductors in the circuit

The circuit has three inductors in each of the half circuit: the tank inductance L_b, the inductors in the output network L_c and the inductors L_e, used for phase noise minimisation. The smallest realisable inductance in the process was chosen for the tank to maximise the varactor capacitance, which in turn maximises the varactor Q, and thus the tank Q. The inductors in the collector, L_c, are designed for maximum output power. The emitter inductors, L_e, form a low pass filter, which filters out the current source noise.

L_c and L_e are realised using *rfline* components available in the process. L_b is realised using microstrip lines available in the process. The microstrip lines are connected such that a virtual short is achieved at their ends. This would provide the tank inductance, as transmission lines ($l \leq \lambda/4$) with a real or virtual short at their ends have inductive characteristics [**22**] given by (5.44)

$$L_{eff} = \frac{Z_0}{2\pi f} \tan\left(2\pi \frac{l}{\lambda}\right) \tag{5.44}$$

5.3.2 Design of capacitors

After choosing the minimum realisable inductance value, the value of the required tank capacitance is determined by the desired oscillating frequency. Apart from the passives in the tank, transistor parasitics also influence the oscillating frequency. This requires fine tuning the capacitances C_1 and C_2 for a specific oscillating frequency; say 60 GHz. The values of phase noise are simulated for a set of capacitance values using SpectreRF and are given in Figure 5.2.

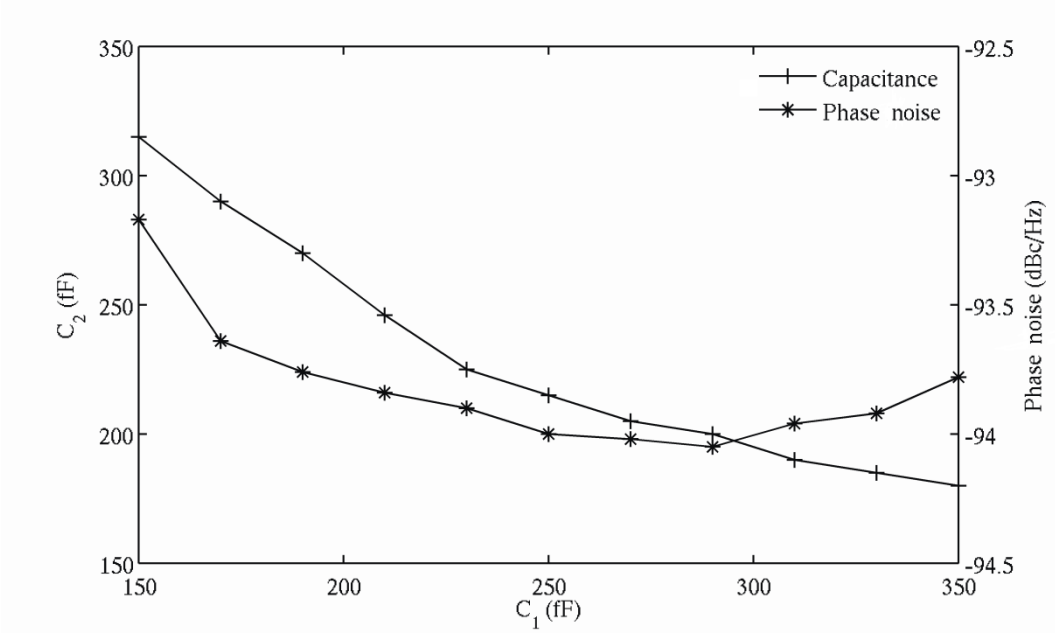

Figure 5.2. Capacitances for an oscillating frequency of 60 GHz and their simulated phase noise [26**]**

From Figure 5.2, it can be seen that the phase noise is at a minimum for a certain value of the capacitance. Substituting these values along with transistors' intrinsic capacitances provides the optimum capacitor design ratio, *n*, which was found to be around 0.3. This matches with the observation derived from analytical modelling in Chapter 4. Thus the analytical modelling using the LTV theory provides a physical insight for this observation, and does not rely only on simulation results based on numerical methods.

5.3.3 *Q* and C-V characteristics of the varactors

The nMOS (*ncap*, *dgncap*) and *havar* varactors with capacitance value around 200 fF in the process have been simulated to compare the performances and to observe whether they cover the desired tuning range. The capacitance and the quality factor in Figure 5.3, are obtained from the *S*-parameter plots according to the following equations

$$C_{in} = \left(\frac{imag(Y_{11})}{\omega} \right) \tag{5.45}$$

$$Q = \left(\frac{imag(Y_{11})}{real(Y_{11})} \right). \tag{5.46}$$

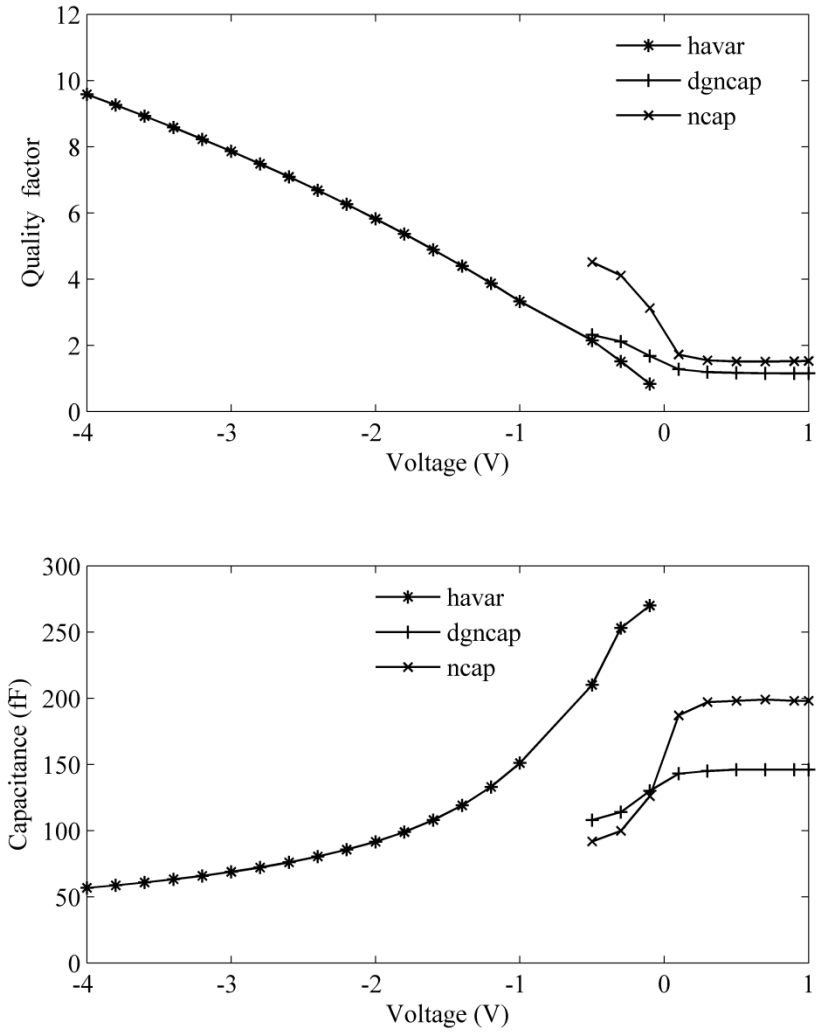

Figure 5.3. *Q* and C-V characteristics of the varactors

The *havar* device has higher *Q*, and MOS varactors have higher voltage-tuning sensitivity, as observed in Figure 5.3. HBT varactors were used in the implementation of the VCO, as they havea better quality factor and tuning range than MOS varactors in the mm-wave range. Varactor *Q* also improves with reduced width and an increased number of base stripes because of a reduction in the base resistance.

The simulated VCO in this work had a tuning range of 57 - 64 GHz and a differential output power of 8 dBm at the fundamental, as shown in Figure 5.4.

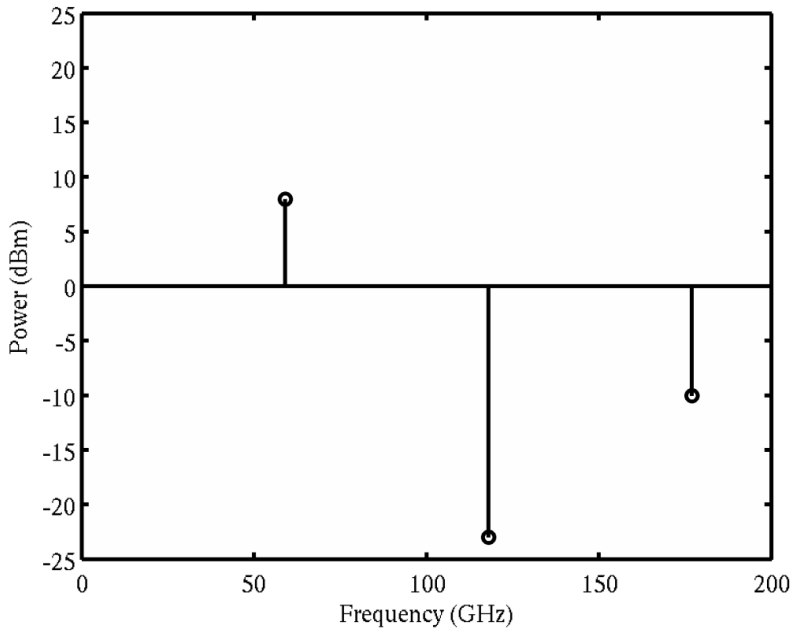

Figure 5.4. The VCO output power at the fundamental, second and third harmonics

From Figure 5.4, it can be observed that there is also power at the harmonics of the desired signal.

5.4 QUADRATURE SIGNAL GENERATION

The vector interpolator requires quadrature signals to be generated from the VCO output. This could be obtained using passives such as the Lange coupler, as discussed in Chapter 2.

5.4.1 Lange coupler

The PDK for the 8HP process provides the behaviour-based model for the *Lange coupler* that accounts for the losses, coupling and Si-substrate effects. The *Lange coupler* in the PDK has a characteristic impedance of 50 Ω and consists of a 1.52 µm wide LY layer finger, which is spaced at 1.52 µm from the adjacent finger. The LY layer, which is 1.25 µm thick, carries the signal and a 0.29 µm thick M1 layer serves as the bottom ground shield. The characteristics of the *Lange coupler* in the 0.13 µm process are shown in Figure 5.5 and Figure 5.6

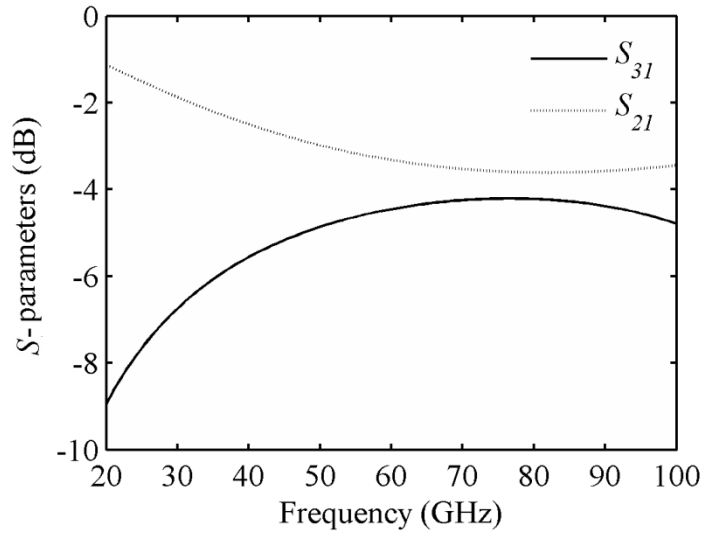

Figure 5.5. *S*-parameters of the *Lange coupler* in the IBM 8HP process

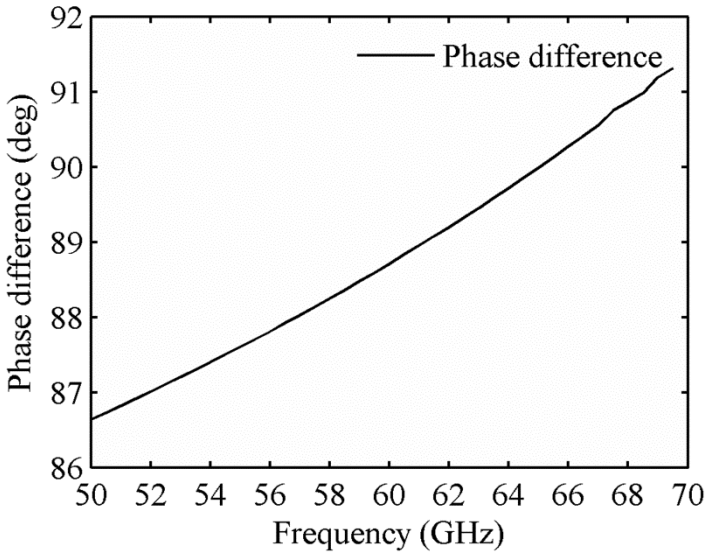

Figure 5.6. Phase difference between the through and coupled ports of the *Lange coupler*

Figure 5.5 shows the S_{21} (coupling) and S_{31} (through) magnitude in dB. At 60 GHz, S_{21} is about -3.3 dB and S_{31} is -4.4 dB, thus the coupler insertion loss is about 1.6 dB. Figure 5.6 shows the phase difference between the signals from the through and coupled ports; it is observed that it varies linearly in the bandwidth of interest from 57 to 64 GHz. The linear

variation is because the coupler is designed to be of length $\lambda/4$ at the centre frequency of 60 GHz.

5.5 VGA

The VGA for the vector interpolator is implemented using a Gilbert mixer topology, with resistors R_1 to R_4 included to increase the linearity of the amplifiers. The gain control voltages are generated using a pre-distortion circuit, which is an inverse-`tanh` cell, so as to improve the linearity further. The VGA, along with the pre-distortion circuit, is shown in Figure 5.7.

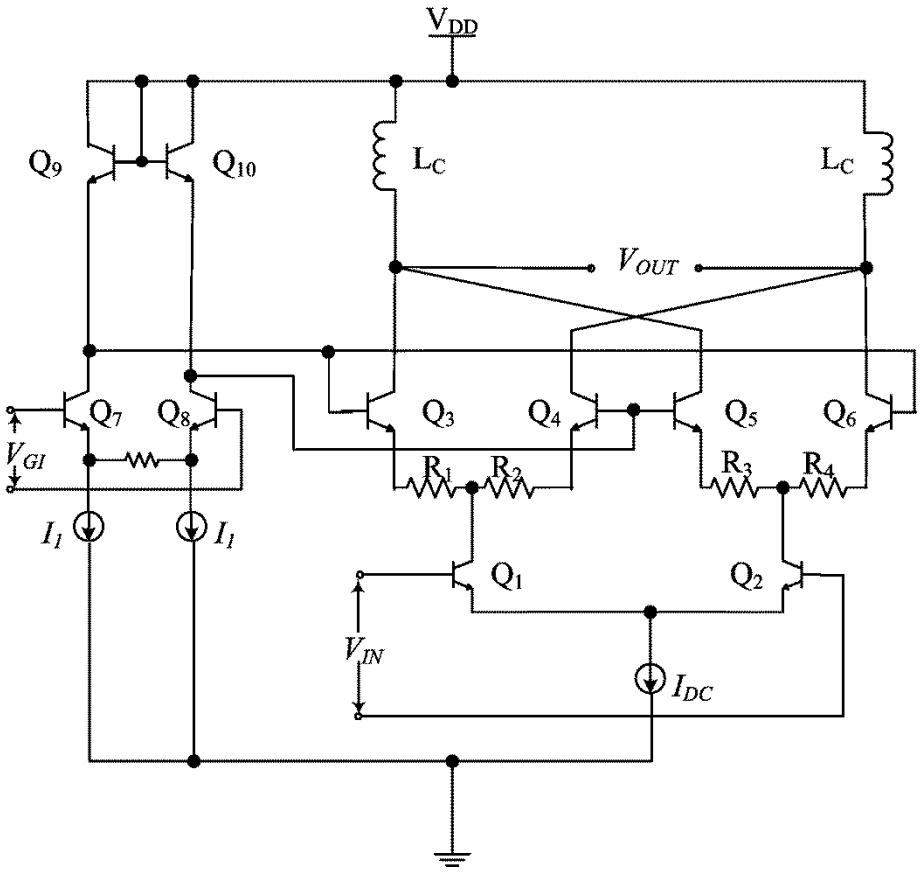

Figure 5.7. Variable gain amplifier

In Figure 5.7, the in-phase/quadrature phase VCO signals are applied at the base of transistors $Q_{1\text{-}2}$. The bias current is steered through these transistors using the gain control voltage applied to $Q_{3\text{-}6}$, via a pre-distortion circuit ($Q_{7\text{-}10}$). The gain versus control voltage characteristics of the VGA are shown in Figure 5.8.

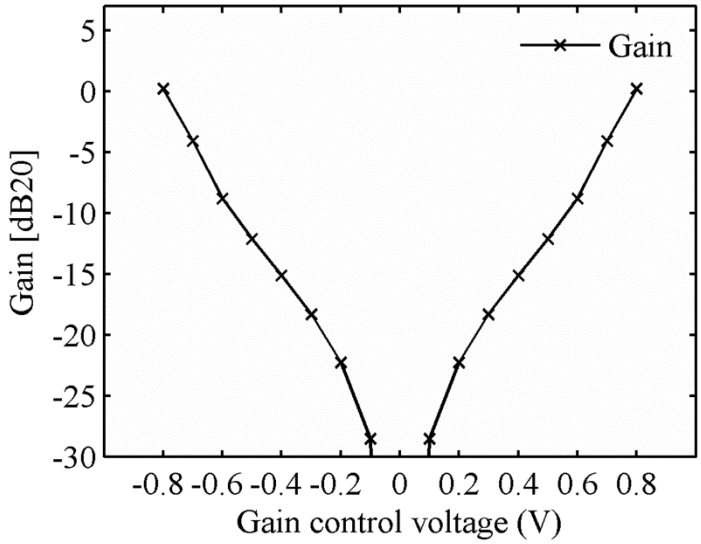

Figure 5.8. Gain characteristics of the VGA

In Figure 5.8, the gain varies almost linearly with the control voltages applied to the pre-distortion circuit; a variation from 0 dB to -30 dB was achieved with a gain control voltage variation from -0.8 V to 0 V. This linear variation is useful in generating multiple phases, using the vector interpolation scheme. The signals in the I/Q paths were individually adjusted for any amplitude differences. The simulation results of the entire vector interpolator system are shown in Figure 5.9.

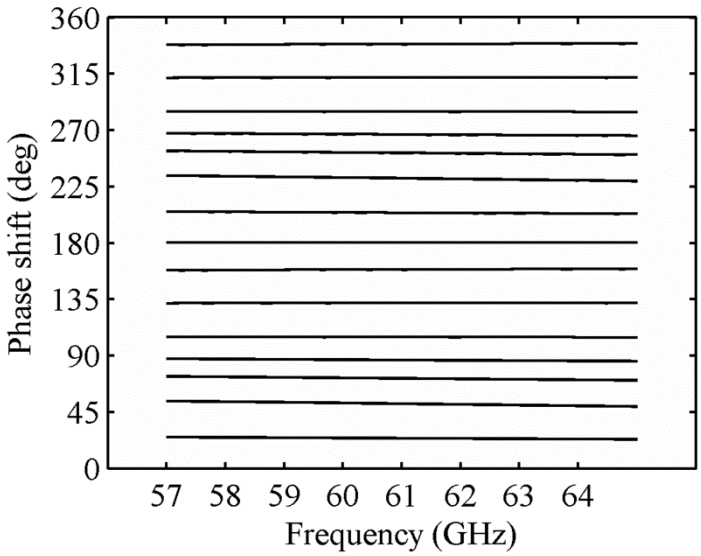

Figure 5.9. Vector interpolator phase shift for different gain settings

From Figure 5.9, it is observed that vector interpolation provides LO signals with phases ranging from 0° to 360° in steps of 22.5° and could be used for steering the beam in a phased array. It has to be noted that incorporating a vector interpolator for *local* LO-path phase-shifting in phased arrays would require buffers in the path to provide VCO signals to the input of the interpolator. As discussed earlier, the noise figure of this system does not affect the receiver sensitivity, as this is placed in the LO-path.

A VCO with differential output signals feeding the vector interpolator system, would avoid the need for any baluns at 60 GHz, to split the signals to feed the I and Q paths. It should be noted that the same vector interpolator could be used in an RF-path shifting architecture if the baluns could be incorporated after the hybrid couplers and before feeding to the mixers. In such a case, the performance of the phase shifter, including its gain, noise figure and linearity, would affect the system's performance, as these would then have to be placed in the signal path.

5.6 CONCLUSION

This chapter discussed the circuit design and simulation of the VCO and the integrated phase shifter. The VCO provided a tuning range to cover the entire band of unlicensed spectrum (57-64 GHz) and numerical simulations were also performed to obtain the optimum value of the capacitor's ratio *n*. This validated the hypothesis that LTV analysis could be used to optimise the design and process parameters, to obtain good phase noise performance.

The simulation results of the integrated phase shifter provide LO signals with phases ranging from 0° to 360° in steps of 22.5°. This demonstrates the suitability of the vector-sum method in providing adequate phases of LO signal for phased array operation, as was stated in the research question.

CHAPTER 6: LAYOUT, FABRICATION AND MEASUREMENT

6.1 INTRODUCTION

The first section of this chapter details the layout and fabrication of the mm-wave VCO IC and also the final PCB. The second section discusses the measurement setup to characterise the MMIC, followed by a discussion of the results.

6.2 IC LAYOUT AND FABRICATION

The layout as shown in Figure 6.1, occupied an area of 800 µm × 675 µm including the bondpads, and it measured 650 µm × 450 µm without the bondpads.

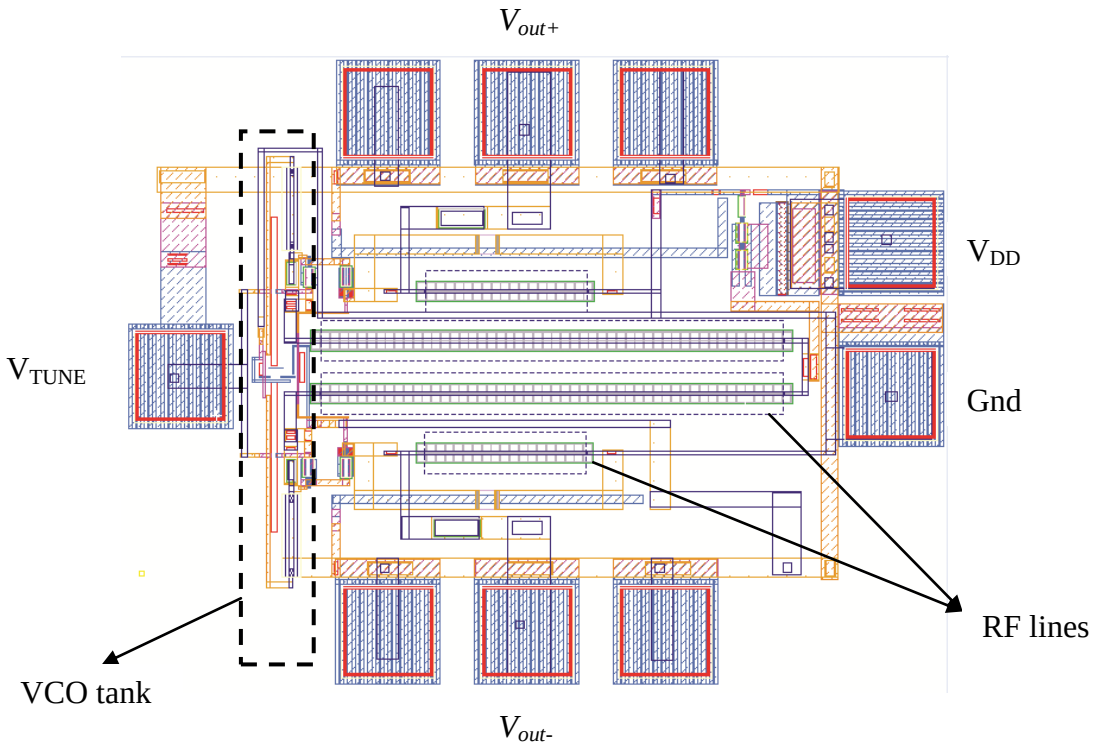

Figure 6.1. Layout of the mm-wave VCO

From Figure 6.1, it can be seen that the VCO was laid out symmetrically. The differential outputs connected to GSG pads, were spaced 50 µm apart. The VCO tank, as highlighted

in Figure 6.1, consists of the transistors providing negative resistance and the tank inductors, along with the MIM and the varactors. The IBM 130 nm SiGe BiCMOS 8HP process used for the current design is a 5LM technology, which implies it has five levels of metal layers (M1, M2, MQ, LY, AM) for design implementation. The interconnect lines using metal layers and the inter-level connections to lines including vias and contacts were designed to adhere to the standard electromigration rules that set a maximum I_{DC} and also local-heating enhanced electromigration that sets a maximum I_{rms}.

A photograph of the entire chip using a scanning electron microscope (SEM), Vega II LMU from TESCAN is shown in Figure 6.2.

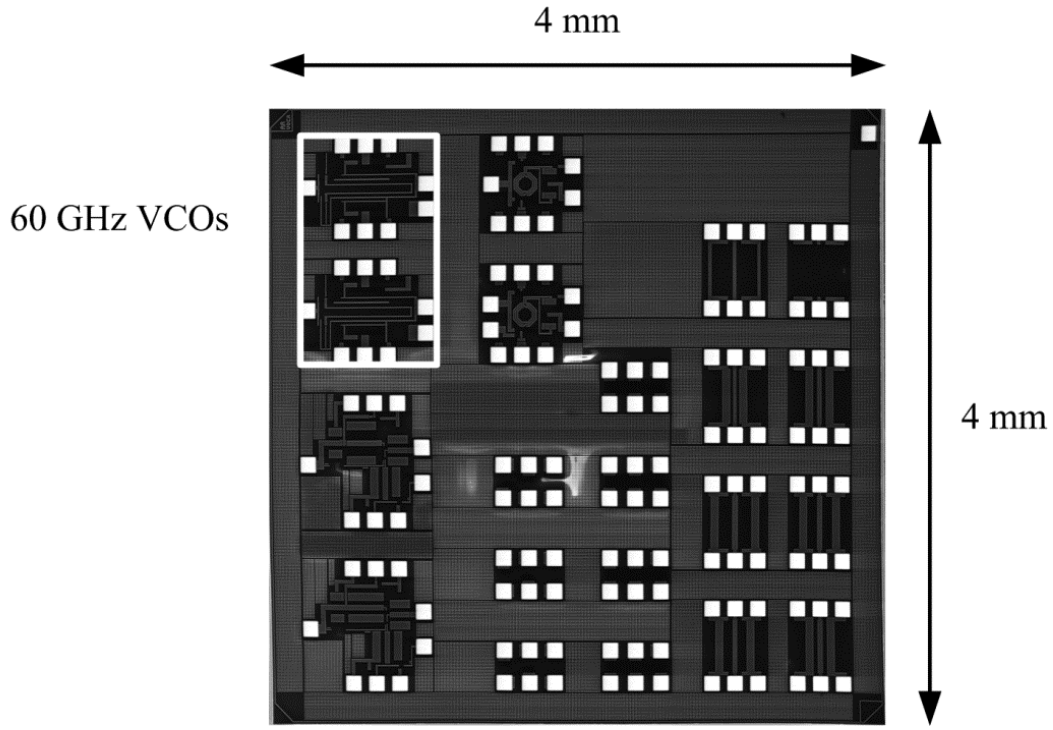

Figure 6.2. Microphotograph of the entire chip including the mm-wave VCO

The entire chip was 4 mm × 4 mm in size, and in Figure 6.2, the 60 GHz VCO implementations are highlighted, as two other projects were also part of the MPW run. The SEM photograph of the VCO as such is shown in Figure 6.3.

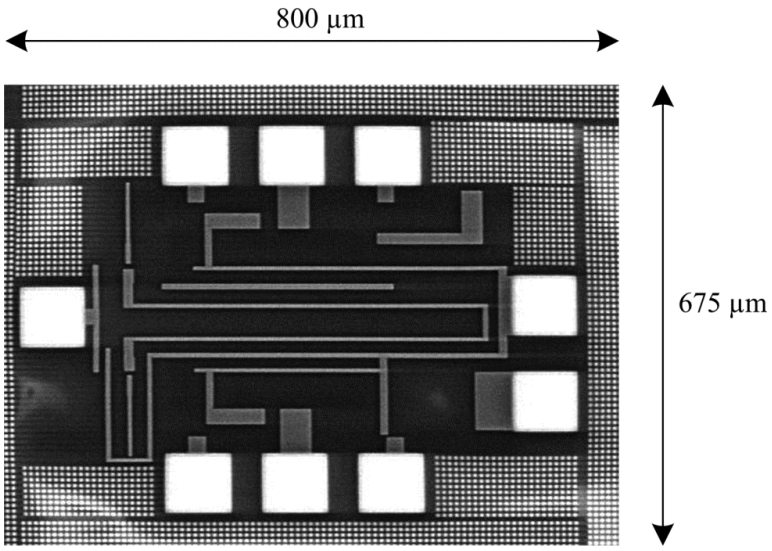

Figure 6.3. Microphotograph of the 60 GHz VCO MMIC [26]

In Figure 6.3, the differential GSG outputs at the top and bottom, and the bias pads on either side can be seen.

6.3 PCB LAYOUT AND FABRICATION

The PCB was 12 cm × 12 cm × 4 cm in dimension, and the layout is shown in Figure 6.4.

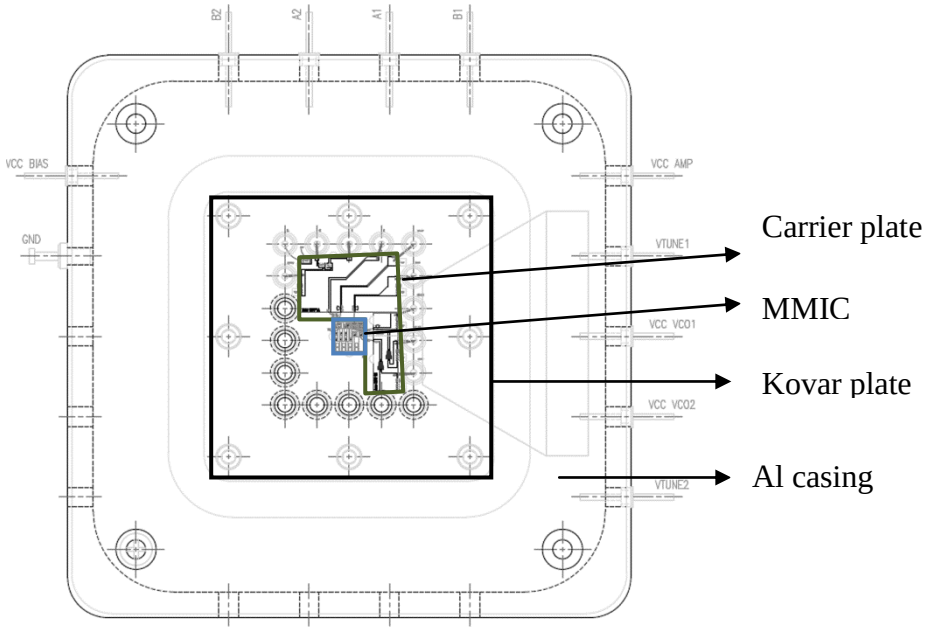

Figure 6.4. PCB Layout

The 4 mm × 4 mm MMIC is epoxied onto a gold-plated Kovar carrier plate using conductive epoxy, as shown in Figure 6.4. The surrounding bias circuitry on an Alumina substrate was soldered onto the carrier plate and connections were made to the chip using bondwires of size 0.7 mil (18 µm) in diameter. The Kovar carrier plate was bolted down onto a larger aluminium housing, which was nickel-plated and feedthroughs were inserted to provide connections to the external world.

6.4 MEASUREMENT RESULTS

Figure 6.5 shows the MMIC on the probe station with the ground-signal-ground (GSG) probes placed on the pads for measurement.

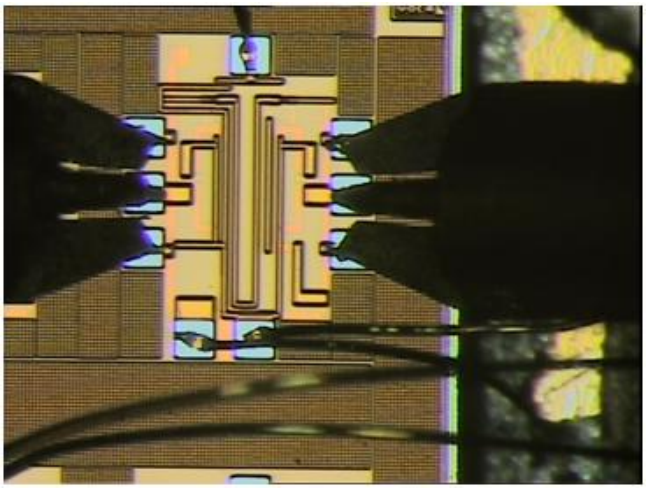

Figure 6.5. A photograph of the MMIC with the GSG probes placed on the pads

In Figure 6.5, the bondwires attached to the DC bias pads are also evident. The pitch of the output pads corresponded to that of the GSG probes.

The VCO operated with a V_{DD} of 4 V and drew a supply current of about 35 mA. The spectrum analyser output is shown in Figure 6.6. To compare the phase noise performance of the mm-wave VCO with other published VCOs, the filter bandwidths in the spectrum analyser have been set to resolution bandwidth (RBW) of 100 kHz and video bandwidth of 10 kHz as in [**22**] [**25**].

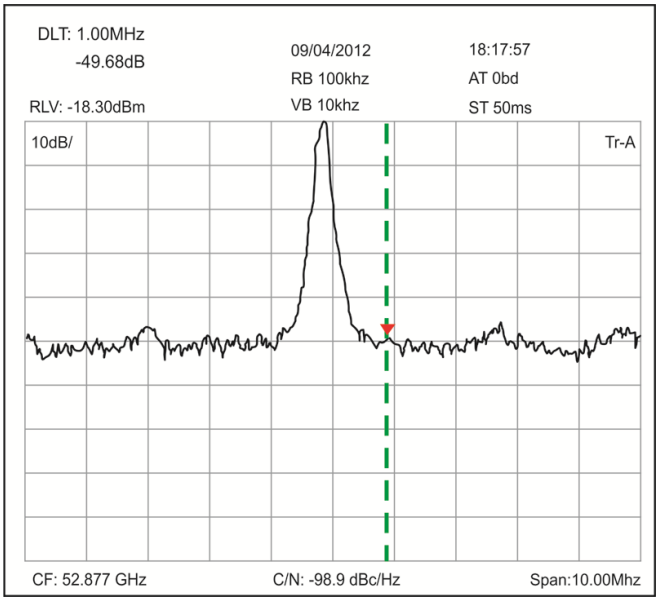

Figure 6.6. Spectrum analyser output at a centre frequency of 52.8 GHz [26**]**

In Figure 6.6, the centre frequency of 52.8 GHz and the corresponding phase noise value at 1 MHz offset of -98.9 dBc/Hz could be seen from the bottom panel.

The tuning voltage was varied from 2.5 V to 6.5 V and a tuning range of 50 GHz – 57 GHz was obtained. The simulated and measured tuning ranges are displayed in Figure 6.7.

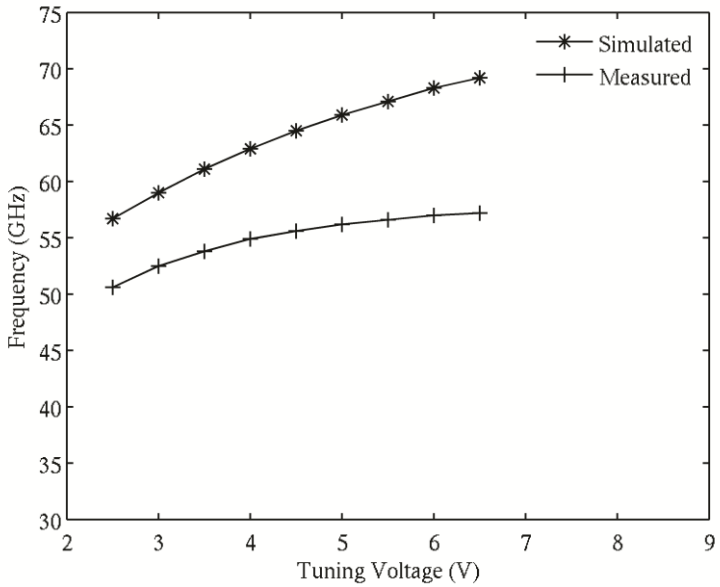

Figure 6.7. Measured and simulated tuning characteristics of the mm-wave VCO [26**]**

The difference in tuning characteristics in Figure 6.7 is due to interconnect parasitics and process variations, which brought about the 10% reduction in the tuning range available from the tank. This verifies what has been stated in [**23**], that when SiGe BiCMOS technology is used for fabricating an LC-VCO, the capacitance variations lead to a 10.1% variation in the frequency range. Thus a margin of 10% should be taken into account while designing the VCO.

Initially, the supply for the VCO was provided using the Semiconductor Characterization System (DC) with wafer probing station - 4200-SCS/C/Keithley Easyprobe EP6/Suss MicroTec. The spectrum of the signal thus obtained was distorted and phase noise measurements could not be performed. When the DC supply was provided with batteries, a clean spectrum at the output was obtained. It was also observed that the microscope attached to the probe station was causing a distortion at the output and hence had to be turned off to get a clean spectrum before making the phase noise measurements.

6.5 CONCLUSION

This chapter detailed the layout and fabrication of the MMIC and the final PCB. The measurement results of the VCO were presented, which validated the hypothesis that analytical modelling of phase noise could lead to optimisation of design parameters for better phase noise performance. The tuning range of the fabricated VCO was also compared with the simulation results provided by the simulator.

CHAPTER 7: CONCLUSION

7.1 INTRODUCTION

Chapter 1 dealt with the background and streamlining of the research problem, along with its relevance in the present technological space. Chapter 2 discussed the study of the current literature, which also formed the foundation of the proposed solution. The accuracy of the LTV model in predicting the phase noise of oscillators suggested an approach to modelling the phase noise in a mm-wave circuit configuration. Chapter 3 focused on the methodology, which included studying the IBM 8HP process and also the measurement setup details required to finalise the layout of the MMIC for measurements. Chapter 4 discussed the analytical modelling of the phase noise, using the impulse sensitivity function of the individual contributing noise sources. Chapter 5 detailed the simulation results of the schematic design entry obtained using the Cadence suite. Chapter 6 discussed the final layout that was prototyped, followed by the details of the PCB with the MMIC used for measurements. It also discussed the measurement setup in detail and the final results, which were then compared with state-of-the-art VCO designs to date.

This chapter provides a critical evaluation of the work, and summarises the deductions from the research. It also makes some suggestions for future work.

7.2 CRITICAL EVALUATION OF THE WORK

In Section 1.3 it was hypothesised that the LTV model could be used in predicting the phase noise variation w.r.t design parameter n and process parameter r_b in a mm-wave VCO configuration, and also that a possible solution for optimising the design could be suggested from such an approach.

This hypothesis was validated and an analytical expression for phase noise in a mm-wave VCO configuration was derived. The analytical expression was then optimised with respect to process and design parameters to improve phase noise performance. The optimum value of the design parameter, namely the capacitors ratio n in a Colpitts oscillator, was found to

be around 0.3 using the model. It was also verified by numerical simulations performed on the design, using SpectreRF.

The conclusions derived using the model were used in designing and fabricating a 60 GHz VCO using the IBM 8HP 0.13 µm SiGe BiCMOS process. The fabricated VCO was measured to demonstrate a centre frequency of 52.8 GHz, and a phase noise performance of -98.9 dBc/Hz at 1 MHz offset. The VCO has a FOM of 172 dBc/Hz, which was found to be in the range of values presented by other mm-wave VCOs. The research yielded understanding and thus a structured approach to the design choices in VCO design, especially the passive components used in the VCO tank. The comparison of the simulated and measured characteristics show that a 10% design margin from the simulation results has to be allowed for the tuning range of the VCO while using a SiGe BiCMOS technology. Another conclusion that could be drawn is about the limits of the technology, namely the effect of process parameters on the design performance. The analytical expression has projected the direct effect that transistors' base resistance has on phase noise. It was also observed that the C-E breakdown voltage of the technology limits the maximum obtainable swing from the design, thus affecting phase noise performance. The design could have yielded better phase noise performance if it had been left to operate with V_{CE} above the BV_{CEO}.

Another research problem investigated was whether the vector interpolation scheme could be used to provide multiple phases of the LO signals to steer the beam in a mm-wave phased-array system. The simulations of the proposed system show that phases ranging from 0° to 360° in steps of 22.5° could be obtained using the vector interpolator. Thus the vector interpolator could be used in the *local* LO-path shifting scheme for phased arrays, with the added complexity of including a buffered binary tree distribution network following the VCO to provide the oscillator signals to the input of the vector interpolator.

7.3 SUGGESTIONS FOR FUTURE WORK

Some suggestions for future work in the research area are provided below.

It was mentioned that the research was focused on using components available in the IBM 130 nm process and the simulations used the foundry provided p-cells for the design. As there are five metal layers available in the process, inductor design using EM simulation software could have been performed to provide a wider design space and it might have improved the quality factor of the tank; which would have helped in enhancing the VCO performance.

In Figure 6.6, the noise marker for measurement is seen to be embedded in the noise floor of the spectrum analyser, thus the reported measurement can be denoted as "worst case." For future, it is recommended that the RBW of the analyser should be reduced to improve the analyser noise floor and consequently correct the measurement or accuracy thereof. Separately, a dedicated phase noise test set could be setup for measuring the phase noise and in this way overcoming the limitation of comparable phase noise performance of the spectrum analyser LO.

The vector interpolator system would have been fully characterised if it had also been fabricated in the IBM 8HP process, as the correctness of any IC design has to be verified by its measurement results. This would have helped in assessing its performance and viability for future use in phased-array systems.

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