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PHASE NOISE REDUCTION OF A 0.35 µm BiCMOS SiGe 5 GHz VOLTAGE CONTROLLED OSCILLATOR

by

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SUMMARY

PHASE NOISE REDUCTION OF A 0.35 µm BiCMOS SiGe 5 GHz VOLTAGE CONTROLLED OSCILLATOR **BY** JOHANNES WYNAND LAMBRECHTS

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The research conducted in this dissertation studies the issues regarding the improvement of phase noise performance in a BiCMOS Silicon Germanium (SiGe) cross-coupled differential-pair voltage controlled oscillator (VCO) in a narrowband application as a result of a tail-current shaping technique. With this technique, low-frequency noise components are reduced by increasing the signal amplitude without consuming additional power, and its effect on overall phase noise performance is evaluated. The research investigates effects of the tail-current as a main contributor to phase noise, and also other effects that may influence the phase noise performance like inductor geometry and placement, transistor sizing, and the gain of the oscillator.

The hypothesis is verified through design in a standard 0.35 µm BiCMOS process supplied by Austriamicrosystems (AMS). Several VCOs are fabricated on-chip to serve for a comparison and verify that the employment of tail-current shaping does improve phase noise performance. The results are then compared with mathematical models and simulated results, to confirm the hypothesis.

Simulation results provided a 3.3 dBc/Hz improvement from -105.3 dBc/Hz to -108.6 dBc/Hz at a 1 MHz offset frequency from the 5 GHz carrier when employing tail-current shaping. The relatively small increase in VCO phase noise performance translates in higher modulation accuracy when used in a transceiver, therefore this increase can be regarded as significant. Parametric analysis provided an additional 1.8 dBc/Hz performance enhancement in phase noise that can be investigated in future works. The power consumption of the simulated VCO is around 6 mW and 4.1 mW for the measured prototype. The circuitry occupies 2.1 mm^2 of die area.

Keywords:

Active circuit, analogue integrated circuit (IC), bipolar CMOS (BiCMOS), heterojunction bipolar transistor (HBT), LC oscillator, narrowband, performance trade-offs, single sideband (SSB) phase noise, Silicon Germanium (SiGe), tail-current suppression, voltage controlled oscillator (VCO).

SAMEVATTING

FASE GERAAS VERMINDERING VAN 'N 0.35 µm BiCMOS SiGe 5 GHz SPANNINGS BEHEERDE OSSILATOR **DEUR** JOHANNES WYNAND LAMBRECHTS

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In die navorsing wat hierdie verhandeling beskryf is die effek van faseruis in 'n BiCMOS Silikon Germanium (SiGe) verskil-versterkte spanning beheerde ossilator (SBO) in 'n noueband toepassing as gevolg van 'n put-stroom verbeterings tegniek bestudeer. Deur gebruik te maak van hierdie tegniek word lae frekwensie ruis komponente verminder deur die totale sein se amplitude te verhoog sonder om meer krag toe te voer. Die effek hiervan op totale faseruis word dan geëvalueer. Die navorsing bestudeer die effek van put-stroom verbetering as hoof bydraer, maar ook ander aspekte wat die ruissyfer kan beïnvloed soos induktor grootte en plasing, transistor grootte, en die wins van die kringbaan.

Die hipotese is geverifieer deur die ontwerp van die kringbaan in 'n standaard 0.35 µm proses wat deur Austriamicrosystems (AMS) verskaf word. 'n Aantal SBOs is op 'n mikroskyfie geïmplementeer en dien as maatstawwe om die effek van die verbeterings-tegniek op faseruis te bepaal. Die resultate word daarna met wiskundige modelle vergelyk asook met simulasie resultate om die hipotese te bewys.

Simulasie resultate het 'n 3.3 dBc/Hz verbetering vanaf -105.3 dBc/Hz tot -108.6 dBc/Hz teen 'n 1 MHz afwyking van die 5 GHz draer frekwensie bewys as gevolg van put-stroom verbetering. Die relatiewe lae verbetering in faseruis dui op 'n hoër modulasie-akkuraatheid wanneer dit in 'n kommunikasie stelsel gebruik word, dus kan hierdie verbetering as beduidend beskou word. Parametriese analise het 'n addisionele 1.8 dBc/Hz verbetering getoon, wat in toekomstige werke bestudeer kan word. Die drywingsverbruik van die ossilator is naastenby 6 mW, en 4.1 mW vir die prototipe. Die totale stroombaan beslaan 'n area van 2.1 mm^2 op die mikroskyfie.

Sleutelwoorde:

Aktiewe stroombaan, analoog integreerde stroombaan, bipolêre CMOS (BiCMOS), enkelsyband (SSB) faseruis, hetero-aansluiting bipolêre transistor (HBT), LC ossilator, noueband, Silikon-Germanium (SiGe), put-stroom suppressie, spannings beheerde ossilator (SBO), verrigtings-kompromieë.

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LIST OF ABBREVIATIONS

AC	Alternating current
ADE	Analog design environment
AMS	Austriamicrosystems
AMS	Analogue- and mixed-signal
APS	Accelerated parallel simulator
ASIC	Application specific integrated circuit
BJT	Bipolar junction transistor
CAD	Computer aided design
CMIM	Metal-metal capacitor
CMOS	Complementary metal oxide semiconductor
DC	Direct current
DIP	Dual in-line package
DRC	Design rule check
DUT	Device under test
FFT	Fast fourier transform
FOM	Figure of merit
GHz	Gigahertz
HBT	Heterojunction bipolar transistor
HS	High speed
HV	High voltage
IBM	International Business Machines
IC	Integrated circuit
LVS	Layout versus schematic
MEMS	Microelectromechanical system
MIM	Metal-insulator-metal
MMIC	Monolithic microwave integrated circuit
MOS	Metal oxide semiconductor
MPW	Multi-project wafer
NF	Noise figure
PCB	Printed circuit board
PSD	Power spectral density
PSRR	Power supply rejection ratio
PSU	Power supply unit
QFN	Quad flat no leads
QVCO	Quadrature VCO
RF	Radio frequency
SiGe	Silicon Germanium
SNR	Signal-to-noise ratio
SOI	Silicon-on-insulator
SOIC	Small-outline integrated circuit
SPICE	Simulation program with integrated circuit emphasis
TOI	Third order intercept
VBIC	Vertical bipolar inter-company
VCO	Voltage controlled oscillator
VLSI	Very large scale integration

CHAPTER 1: INTRODUCTION

1.1 MOTIVATION

Voltage controlled oscillators (VCOs) are essential components in radio frequency (RF) systems and are used in narrow band receivers for communication (clock generation and data recovery), tracking, and radar applications. VCOs are positive feedback amplifiers that have a tuned resonator in the feedback loop [1] and a VCO can be viewed as an energy conversion engine (from direct current to alternating current) [2]. The resonant frequency of a VCO is controlled (tuned) by applying a direct current (DC) voltage at the input.

Noise in these oscillators limits the channel capacity of communication systems, degrades the resolution of radar, and restricts the resolution of spectrum analyzers. The term phase noise is widely used for describing short term random frequency fluctuations of a signal, whereas frequency stability is a measure of the degree to which an oscillator maintains the same value of frequency over time [3]. Phase noise performance in RF communication applications has become more stringent as the noise in the sidebands at high frequencies result in spurious responses of the receiver to nearby interfering channels. This contributes to the degradation of the modulation accuracy of the transmitter [4].

Focus on the research issues of a low phase noise VCO for use in RF narrow band receivers, using Silicon Germanium (SiGe) BiCMOS[1] technology is proposed in this dissertation. Modern communication's increasing bandwidth requirements as a result of low-temperature growth of Silicon epitaxy has rekindled research in the BiCMOS field [5]. Combining bipolar with complementary metal-oxide semiconductor (CMOS) transistors enhance system performance when operating in the GHz range (especially from 5 GHz), as heterojunction bipolar transistors (HBTs) with SiGe doped bases can easily have switching delays of less than 10 ps [6].

[1] BiCMOS is the integration of bipolar junction transistors and complementary metal-oxide semiconductors into a single device.

1.2 FOCUS OF RESEARCH

Several techniques exist to improve phase noise performance in VCOs. These techniques range from VCO topology considerations, inductor dimensioning and placement for improved quality factor (*Q*-factor), semiconductor process parameter considerations, and reducing low-frequency tail-current noise sources. The latter option is employed in this dissertation to study the overall effect on VCO phase noise performance, as it has been recognized that the tail transistor may have a large impact on the generation of phase noise, often being the largest contributor [7].

Tail-current noise suppression in RF BiCMOS VCOs prevents the low-frequency tail-current noise from being converted into phase noise during normal operation of the oscillator [7]. The tail current is made large when the oscillator output voltage reaches its maximum or minimum value and when the sensitivity of the output phase to injected noise is the smallest [8]. The tail current is made small during the zero crossings of the output voltage when the noise sensitivity is large. No additional power is added to the system, ensuring low power operation at low noise levels. Tail-current shaping techniques reduce phase noise with three separate, but simultaneous mechanisms [9]. The increased oscillation amplitude, narrower drain current pulses, and finally the shunt capacitor that acts as a noise filter for the tail current, all contribute to lowering the phase noise.

A challenge that arises when designing an oscillator for low phase noise, is maintaining a reasonable tuning range to allow operation in the frequency bands adjacent to the centre frequency. A large tuning range and a low available control voltage (limited by the supply voltage and device breakdown voltage) results in a large oscillator gain, which increases both intrinsic device noise and coupled spurious tones up-conversion around the centre frequency [10]. Another concern is limiting the power dissipation of the oscillator, without compromising the output voltage amplitude, as a too low output signal might be overshadowed by noise.

1.3 SYSTEM MODEL

Figure 1 depicts the placement of a VCO in a communication system. The VCO is the primary tuning mechanism in any communication system, responsible for selecting the channel on which communication can commence, by generating an output signal from a synthesizer.

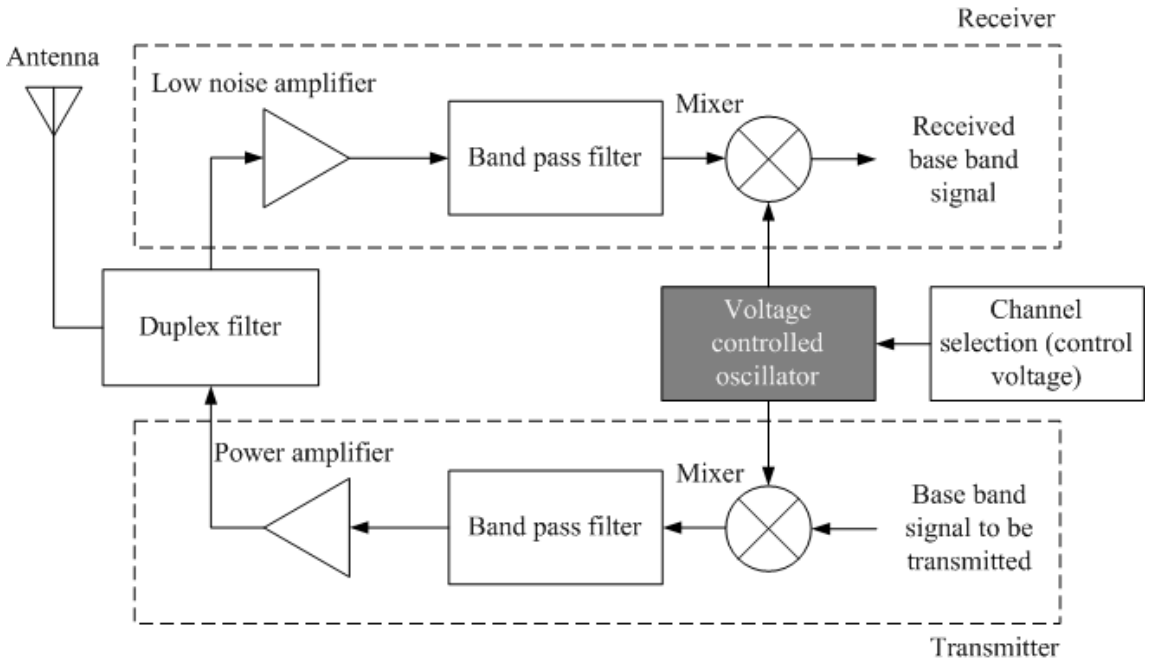

Figure 1. System model illustrating the placement of the VCO.

Figure 1 illustrates how a signal passes through a communication system where a VCO is used. The signal is received by the antenna and passed through a duplex filter to distinguish between the input and output signal. If an input signal is received, it passes through a band pass filter to remove signal components outside the frequency band of interest. This signal is mixed with the signal generated by the VCO and the base band signal is extracted (down-converted). If a signal is to be transmitted, the base band signal is up-converted in the mixer when modulated with the VCO signal. The signal passes through a narrow band-pass filter, is then amplified before transmission, distinguished as an output signal according to its frequency characteristics and transmitted by the antenna. The importance of the VCO in any transceiver system is evident, and low-noise operation enhances modulation accuracy.

1.4 RESEARCH HYPOTHESIS

The hypothesis considered for this dissertation is whether it was possible to improve the phase noise ratings for a BiCMOS SiGe VCO operating at 5 GHz, using the 0.35 µm process supplied by Austriamicrosystems (AMS), using a tail-current shaping technique that does not require any alterations to standard process procedures?. Phase noise performance of about -110 dBc/Hz at an offset of 1 MHz (see Section 2.4 for a detailed analysis on phase noise) from the centre frequency was expected, where an improvement using standard components only of at least 3 – 8 dBc / Hz would prove significant.

In order to prove this hypothesis, the proposed VCO was first simulated using software able to create the proposed system on schematic level. Simulated results were used to confirm that the hypothesis was in fact feasible. For this dissertation, to strengthen the hypothesis, an integrated circuit (IC)-level design is prototyped based on the schematic design. The prototype was measured, and these results were used to confirm the real-world operation of the proposed system and hypothesis.

1.5 RESEARCH METHODOLOGY

Figure 2 depicts the flow diagram of the research methodology that was followed to research and prototype a VCO operating with very low phase noise.

Primarily, all specifications need to be identified and proven feasible. High frequency, BiCMOS-based VCOs are prone to tradeoffs between various core specifications. Therefore it is of utmost importance to know which specifications are less stringent, allowing the core specification (phase noise performance) to be enhanced.

Next, the different techniques available to improve phase noise performance should be identified and studied. Each technique allows for a certain degree of improvement, again weighing the effects in terms of the tradeoffs are considered vital. The top of Figure 2 shows five circles, each displaying a technique to improve phase noise performance. Each technique is carefully researched, ensuring each contributes to overall system performance.

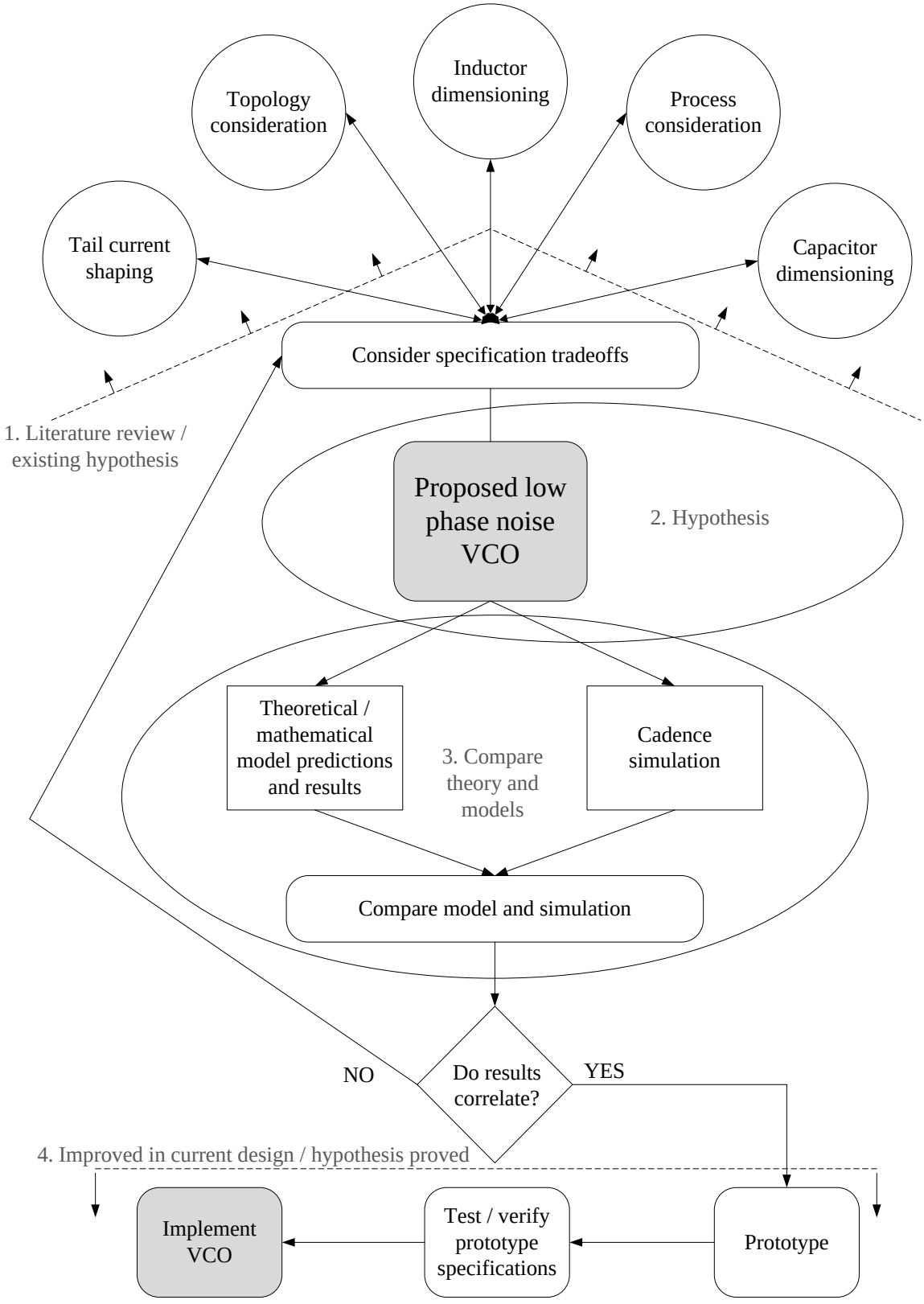

Figure 2. Flow diagram of research methodology.

All of the abovementioned steps lead toward the statement of the research hypothesis. The hypothesis is given in Section 1.4 and can only be proven as a feasible hypothesis once all techniques and tradeoffs have been considered.

Theoretical and mathematical models [11] are constructed to accurately predict the phase noise of the VCO. These ratings can then be compared to simulated results. If the simulation results coincide with the theoretical model, and are within bounds of the core specification, the design can be prototyped. Rigorous testing on the final prototype ensured that implementation was successful and the hypothesis has been confirmed. If the results do not coincide with the specifications, consideration of the performance improvement techniques should be re-evaluated in future works.

Following a strict research methodology [13] will improve chances for successful operation of the proposed system, eliminating the feared stage of receiving a finished prototype that does not operate desirably. A brief overview in point-form of this procedure is outlined below.

1. Literature review / existing hypothesis – this step identifies the possible techniques to improve phase noise performance, and gives the researcher a general outline of viable specifications.
2. Hypothesis – the core specifications are set to which the designer must strive to.
3. Comparing theory and model – mathematical models and simulated designs are compared, to ensure that no errors were made in creating these models.
4. Improved on current design / hypothesis proved – if all assumptions and calculations were correct, the manufactured prototype should operate within bounds of the design specifications.

The following two sections describe the context and contribution of this dissertation by comparing it to other works that have been completed in the same field of research.

1.6 CONTEXT OF RESEARCH

Monolithic ICs reduce production cost since it allows for mass volume production. These high volume markets are governed by attributes like price, packaging, performance, and power dissipation. RF components operating in the GHz range has become essential in modern day

technology and is the driving force behind the explosion in wireless RF communication. VCOs are excellent examples of circuits inherent to tradeoffs in terms of price versus performance. This dissertation focuses on reducing the phase noise of an integrated VCO whilst maintaining respectable ratings for the physical size by careful consideration of component choices, low power consumption, high tuning range, and high frequency operation. Similar literatures have been completed and Table 1 lists these literatures, including this dissertation, to illustrate the context of this research.

Table 1. Summary of previous literature phase noise ratings.

Source	Operating frequency / supply	Process technology	Topology	Noise reduction technique	Phase noise @ offset
[14]	5.8 GHz 2.5 V	0.13 µm CMOS (foundry not specified)	Cross-coupled negative transconductance	Accumulation mode MOS varactors	-115 dBc/Hz @ 1 MHz
[15]	5.2 GHz 1.5 V	STMicroelectronics 0.25 µm SiGe BiCMOS	Quadrature cross-coupled (QVCO)	Single MOS and bipolar stack	-93 dBc/Hz @ 1 MHz
[16]	5 GHz 1.4 V	STMicroelectronics 0.13 µm CMOS	Cross-coupled negative transconductance	Low resistivity SOI substrate Q-enhancements	-116 dBc/Hz @ 1 MHz
[17]	5 GHz 3.3 V	IBM 0.35 µm SiGe BiCMOS	Cross-coupled negative transconductance	High quality factor MIMs for feedback	-109.8 dBc/Hz @ 1 MHz
[18]	5-6 GHz 2.5 V	Motorola 0.4 µm CDR SiGe BiCMOS	Cross-coupled negative transconductance	I/Q phase imbalance compensation	-114.6 dBc/Hz @ 1 MHz
[19]	5 GHz 2.5 V	1P5M 0.25 µm CMOS	Cross-coupled negative transconductance	Symmetry adjustment voltage	-119 dBc/Hz @ 1 MHz
[20]	5 GHz 2.5 V	LSI Corporation 0.25 µm CMOS	Cross-coupled negative transconductance	Bias current flicker noise up-conversion	-117 dBc/Hz @ 1 MHz
[This dissertation]	5 GHz 3.3 V	AMS 0.35 µm SiGe BiCMOS	Cross-coupled negative transconductance	Tail-current noise suppression	-110 dBc/Hz @ 1 MHz or better

Comparing all of the obtained results given in Table 1, it is evident that it is in fact possible for SiGe BiCMOS to present phase noise ratings near the -110 dBc/Hz at 1 MHz offset frequency level. The smaller, CMOS processes do present lower phase noise levels and could be realized. The proposed VCO will be implemented using the 0.35 µm BiCMOS (with HBTs) technology from AMS.

1.7 CONTRIBUTION OF WORK

The contribution of the proposed VCO is evident when reviewing previously researched, low phase noise VCOs. These designs give a clear indication of the specifications that have been achieved and the viability of the current specifications. Current GaAs InGaP devices used in similar RF applications (see Table 2) could eventually be replaced with SiGe HBT technology which theoretically exhibits superior noise figures and higher electron mobility. Note that this device (Hittite) is designed for a wide band of operation (4 – 8 GHz), but this research focused on narrowband application to concentrate on phase noise performance, as a wide tuning range is considered a trade-off (see Section 3.2.6 and 4.1.1) to phase noise performance. Designing a VCO with phase noise performance better than -110 dBc/Hz at an offset of 1 MHz from the centre frequency by combining MOSFET and HBT technology which has not been reported in many works to date, will greatly benefit RF spectrum surveillance and signal analysis, as the noise in the sidebands result in spurious responses of the receiver to nearby interfering channels and they also contribute to the degradation of the modulation accuracy of the transmitter [9]. As mentioned in Section 1.4, a cost-effective way of reducing phase noise in oscillators by shaping of the tail-current is proven feasible in this dissertation. This method can be combined with other existing methods that have process enhancement characteristics to further improve phase noise performance.

Table 2. Performance parameters of off-the-shelf GaAs InGaP VCO used for similar applications as presented in this dissertation.

Parameter	Value
Device name	Hittite HMC586LC4B
Device type	Wideband MMIC VCO with buffer
Operation frequency	4 – 8 GHz
Output power	5 dBm
Single sideband phase noise @ 100 kHz offset	-100 dBc/Hz
Single sideband phase noise @ 1 MHz offset	~ -120 dBc/Hz
Tuning voltage	0 – 18 V_{DC}
Maximum supply current	75 mA
Supply voltage (Single supply)	+ 5 V_{DC}

Simulated phase noise improvements of 3.3 dBc/Hz at a 1 MHz offset from a 5 GHz carrier has been achieved using this technique, implemented with the AMS S35D4M5 SiGe BiCMOS process. This dissertation provides mathematical models relating to circuit parameters providing insight towards SiGe based oscillator performance in terms of phase noise.

The major research challenge is to ensure that the hypothesis can be proven feasible not only through mathematical analysis and simulated results, but also through prototyping and physical measurement of an IC. This involves the procedure of converting a schematic layout of the circuit, to a physical layout. In RF systems, many inherent tradeoffs exist due to intrinsic parameters obtained during normal operation. These parameters should be taken into account when designing on IC-level, as even the IC packaging can contribute as unwanted parasitics.

1.8 ORGANIZATION OF DISSERTATION

A brief discussion on the layout and organization of this dissertation is given here.

Chapter 1 (*Introduction*) motivates the research topic for this dissertation by highlighting the demands for low phase noise VCO circuits and places this research in context of previously completed works. A brief background of the research leads to a research problem definition and hypothesis, also justifying the proposed topic. Research methodology is also briefly presented to outline the procedure for formulating the logic order steps to implement the proposed system.

Chapter 2 (*Literature review*) is a thorough literature review of the origin of phase noise in integrated VCOs. The chapter also explains the contribution to phase noise of different components in VCO circuits. Comparisons and considerations for high frequency VCOs are discussed together with techniques available to reduce phase noise in these circuits. The mathematical and graphical interpretation of phase noise is given in this chapter, and mathematical results to quantize phase noise in oscillator circuits are given at the end of the chapter.

Chapter 3 (*Methodology*) researches models and process parameters that will aid in proving the hypothesis based on measured results of a prototype circuit of the proposed VCO. This involves the careful consideration of all of the process models and parameters that influence noise performance, especially at RF frequencies, provides a methodology outline to summarize the steps towards the final prototype, and gives a brief overview of the software used to construct the schematic and layout of the final circuit. Prototyping options are briefly discussed, and packaging is also considered as final steps towards the completion of the prototype, ensuring its readiness when measured results are required (Chapter 5).

Chapter 4 (*Circuit design*) outlines the proposed schematic and layout of the low phase noise VCO. This chapter is separated into two sections. The first section discusses all of the mathematical calculations that were done to do a schematic design of the proposed circuit, operating at the desired frequency, and employing the tail-current shaping circuitry to reduce phase noise. The second section, briefly discusses the decisions made during the layout of the physical circuit which is to be prototyped, and how to create the individual components while bearing in mind its RF operation, and lowest possible noise performance on a physical and practical basis.

Chapter 5 (*Results*) is dedicated to the simulation results of the proposed design in simulation software. These qualitative results are used for comparison and to finally establish whether the hypothesis presented in this dissertation holds true. As the proposed circuit was also prototyped, some measurement results are also given in this chapter, and these results are expected to coincide closely with the simulated results.

Chapter 6 (*Conclusion*) summarizes the theories and hypothesis presented in this dissertation and provides an opinion regarding these based on the results obtained during mathematical, simulated, and measured results. In this chapter, comments are also made on future works that can be completed related to this study, which could further improve phase noise performance and also on how to improve the measured results obtained in this dissertation.

CHAPTER 2: LITERATURE REVIEW

2 SOURCES OF NOISE IN SEMICONDUCTOR DEVICES

A discussion on the noise sources present in semiconductors and the techniques available to reduce phase noise is presented in this section. The discussions in this section are not process specific, and are only generalized theories and representations. Detailed and process-specific parameters are presented in Chapter 3.

2.1 NOISE MODELS OF IC COMPONENTS

A general noise model for bipolar junction transistors (BJT), HBT, MOS transistors, capacitors, and inductors is provided in this section.

2.1.1 BIPOLAR JUNCTION TRANSISTORS

For a BJT operating in the forward-active region, minority carriers diffuse and drift across the base region to be collected at the collector-base junction. Minority carriers entering the collector-base depletion region are accelerated by the field existing there and swept across this region to the collector. The time of arrival at the collector-base junction of the diffusing carriers can be modelled as a random process, and thus the transistor current consists of a series of random current pulses. Consequently, collector current I_C shows full shot noise, and this is represented by a noise current generator i_c^2 from collector to emitter as shown in Figure 3 [21]. *Figure 3 is adapted from [21].*

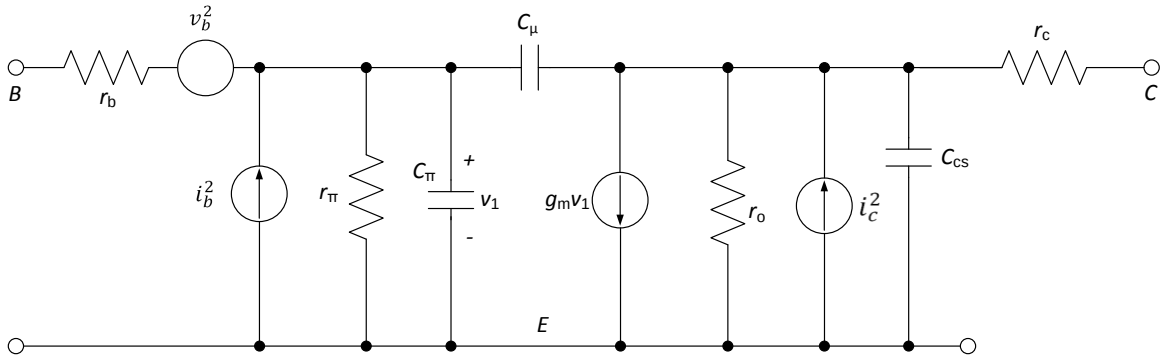

Figure 3. Small-signal representation of a bipolar transistor with noise sources included.

2.1.2 HBT TRANSISTORS

The principle difference between the HBT and the BJT is the use of differing semiconductor materials for the emitter and base regions (for instance SiGe), creating a heterojunction. HBTs are an improvement on BJTs and present very low noise figures in the wireless frequency (GHz) range (see Section 2.4). With increasing frequency, two main effects become important to consider. Firstly, the distributed nature of the base affects the small-signal equivalent circuit. This means that the base-collector intrinsic feedback capacitance (C_μ in Figure 3) has to be accounted for. Secondly, the emitter-collector current is a shot noise source in both space charge regions, at the emitter-base junction and at the base-collector junction. A detailed analysis on the correlation between these noise sources is presented in [11].

2.1.3 MOS TRANSISTORS

For MOS transistors, the resistive channel under the gate is modulated by the gate-source voltage so that the drain current is controlled by the gate-source voltage. Since the channel material is resistive, it exhibits thermal noise, which is a major source of noise in MOS transistors. The noise source can be represented by a noise-current generator i_d^2 from drain to source in the small-signal equivalent circuit, depicted in Figure 4 [21]. *Figure 4 is adapted from [21]*.

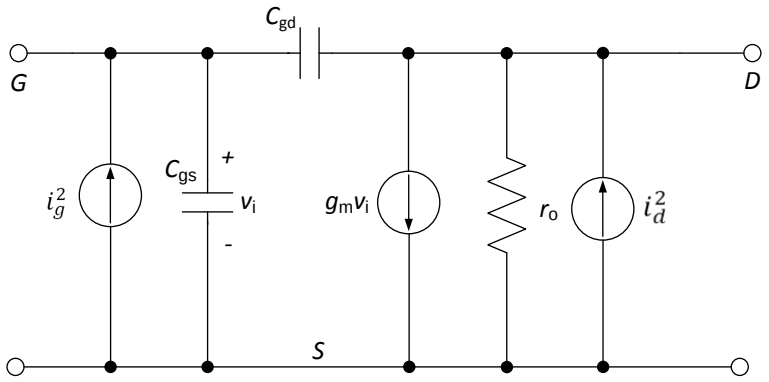

Figure 4. Small-signal representation of a MOS transistor with noise sources included.

2.1.4 CAPACITORS AND INDUCTORS

Capacitors are common elements in integrated circuits, either as unwanted parasitic or as elements introduced for a specific purpose. Inductors can be realized on the silicon die in integrated high-frequency communication circuits. There are no sources of noise in ideal capacitors or inductors and they present an infinite *Q*-factor [22]. In practice, real components

have parasitic resistance that does display noise as given by the thermal noise equations in Section 2.2.2. In the case of integrated circuit capacitors, the parasitic resistance usually consists of a small value in series with the capacitor. Parasitic resistance in inductors can be modelled by either series or shunt elements [23]. Specific process parameters and models are discussed in Section 3.2.3.

This section only described the noise performance of individual transistors. In [21], a detailed discussion on noise performance on different transistor configurations is presented. The section aids in determining the noise model for the proposed LC VCO, but is not presented here and only referenced briefly.

2.2 TYPES OF NOISE PRESENT IN SEMICONDUCTOR DEVICES

Since any oscillator is a periodically time-varying system [3] [10], its time-varying nature must be taken into account to permit accurate modelling of phase noise. Noise sources can be divided into two groups, namely, device noise and interference [10]. Shot noise, thermal noise, and flicker noise ($1/f$) are examples of device noise, while substrate and supply noise are interference. Shot, thermal, and flicker noise contribute to phase noise in high-frequency systems. These noise sources can however be minimized to improve phase noise performance, and these techniques are discussed in this section. It should be stressed that the theories and representations in this section are not process specific, and are generalized to aid in providing insight to noise models in general. The effects of these models on phase noise are presented in Section 2.4.

2.2.1 SHOT NOISE

Shot noise is associated with a DC flow [11] and is present in diodes, MOS transistors, and bipolar transistors. The origin of shot noise can be seen by considering the diode in Figure 5 and the carrier concentrations in the device in the forward-bias region also shown in Figure 5 [21]. *Figure 5 is adapted from [21].*

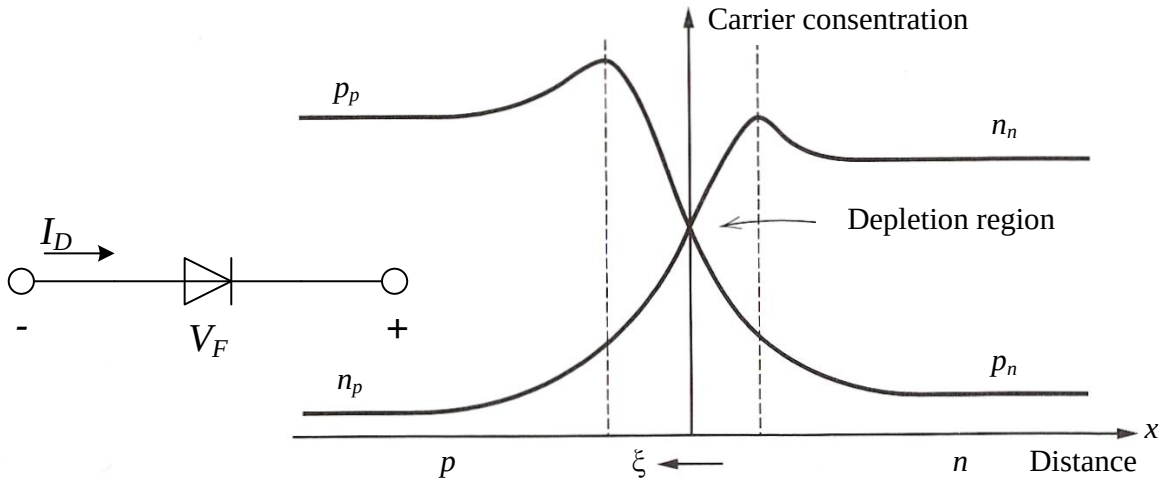

Figure 5. Forward biased *pn* junction diode (left) and its carrier concentrations (right).

An electric field ξ exists in the depletion region and a voltage $(\varphi_0 - V_F)$ exists between the *p*-type and the *n*-type regions, where φ_0 is the built-in potential and V_F is the forward bias of the diode. The forward current (I_D) of the diode is composed of holes from the *p* region and electrons from the *n* region, which have sufficient energy to overcome the potential barrier at the junction. Once the carriers have crossed the junction, they diffuse away as minority carriers. The passage of each carrier across the junction, which can be modelled as a random event, is dependent on the carrier having sufficient energy and a velocity directed toward the junction. Thus external current I_D, which appears to be a steady current, is in fact composed of a large number of random independent current pulses. If the current is examined on a sensitive oscilloscope, the trace appears as in (1), where I_D is the average current. The fluctuation I is termed shot noise and is generally specified in terms of its mean-square variation about the average value. This is written as i^2, where

$$i^2 = \lim_{T\to\infty} \frac{1}{T} \int_0^T (I - I_D)^2 \, dt. \tag{1}$$

It can be shown that if a current I is composed of a series of random independent pulses with average value I_D, the resulting noise current has mean-square value of

$$i^2 = 2qI_D\Delta f \tag{2}$$

where q is the electronic charge (1.6×10^{-19} C) and Δf is the bandwidth in Hertz. This equation (2) shows that the noise current has a mean-square value that is directly proportional to the bandwidth Δf of the measurement. Thus a noise-current spectral density $i^2/\Delta f$ can be defined to be constant as a function of frequency. Noise with such a spectrum is often called white or Gaussian noise. Since noise is a purely random signal, the instantaneous value of the waveform cannot be predicted at any time. The only information available for use in circuit calculations concerns the mean-square value of the signal. The bandwidth is determined by the circuit in which the noise is acting [21].

2.2.2 THERMAL NOISE

Thermal noise is generated by a completely different mechanism from shot noise. In conventional resistors it is due to the random thermal motion of the electrons and is unaffected by the presence or absence of DC [11], since typical electron drift velocities in a conductor are much less than electron thermal velocities. Since this source of noise is due to the thermal motion of electrons, it is related to absolute temperature *T*. In fact, thermal noise is directly proportional to *T* (unlike shot noise, which is independent of *T*) and, as *T* approaches zero, thermal noise approaches zero. In a resistor *R*, thermal noise can be represented by a series voltage generator v^2 and a shunt current generator i^2 as shown in Figure 6. *Figure 6 is adapted from [21]*.

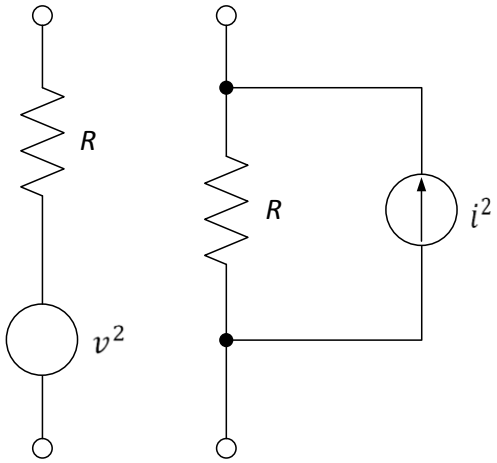

Figure 6. Series voltage (left) and shunt current (right) representation of noise sources.

These representations are equivalent and given in (3) and (4) as

$$v^2 = 4kTR\Delta f \tag{3}$$

$$i^2 = 4kT\frac{1}{R}\Delta f \tag{4}$$

where k is Boltzmann's constant, and R represents the physical resistance. At room temperature, $4kT$ = 1.66 × 10^{-20} V-C. These equations show that the noise spectral density is again independent of frequency and, for thermal noise, this is true up to 10^{13} Hz. Thus thermal noise is another source of Gaussian noise. At room temperature (300 K), the thermal noise spectral density in a 1 kΩ resistor is $v^2/\Delta f \approx 16 \times 10^{-18}$ V^2/Hz. This can be written in the rms form as $v \approx 4$ nV/$\sqrt{Hz}$ where the form nV/$\sqrt{Hz}$ is used to emphasize that the rms noise voltage varies with the square root of the bandwidth. The thermal noise-current generator of a 1 kΩ resistor at room temperature is the same as that of 50 µA of DC exhibiting shot noise [21].

2.2.3 *FLICKER NOISE*

This is a type of noise found in all active devices, as well as in some discrete passive elements such as carbon resistors [11]. The origins of flicker noise are varied, but it is caused mainly by traps associated with contamination and crystal defects. These trapping centres capture and release carriers within the inversion layer in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies, inducing fluctuations in the DC path of the circuit. Mobility modulation induces flicker noise when scattering of these trapped charges occur. Flicker noise is also associated with a flow of DC, and displays a spectral density of the form

$$i^2 = K_1\frac{I^a}{f^b}\Delta f \tag{5}$$

where K_1 is the flicker noise coefficient, a is a constant in the range 0.5 to 2, and b is constant in the range of unity [21]. If b = 1, the noise spectral density has a $1/f$ frequency dependence. It is apparent from (5) that flicker noise is most significant at low frequencies, although in devices exhibiting high flicker noise levels; therefore devices with a higher K_1 which is dependent on device-scaling of MOS and HBT technology, this noise source may dominate the device noise at frequencies well into the MHz (and even GHz) range. Device noise

undergoes multiple frequency translations during circuit operation to become oscillator phase noise and $1/f$ noise tends to be up-converted to produce a $1/\Delta f^3$ noise spectrum [12]. As most oscillators make use of a negative resistance circuit, implemented using non-linear components, these non-linear components add rich harmonic content to the output waveform. Up-conversion of the low-frequency (and DC) waveform changes the slope of the phase noise from -20 to -30 dB/decade, resulting in a corner frequency closer to the carrier.

This concludes the general background of noise models and types of noise present in different transistor technologies. An important consideration now is the effect of these models and types with regard to the topic discussed for this dissertation, which is phase noise performance of SiGe HBT transistors. The ability to relate the abovementioned theories to the process specific transistor models used in the design of the low phase noise VCO contributes to providing insight on how to reduce phase noise through careful consideration of all of the theoretical models presented thus far.

The first step in achieving this is to have a closer look at the general phase noise properties of SiGe HBTs, and the noise models used to represent it. Section 2.3 discusses the noise sources present in SiGe HBTs.

2.3 PHASE NOISE PROPERTIES OF SiGe HBTS

This section will attempt to provide more insight into the noise sources present in SiGe HBTs on a general level. The goal is to ultimately narrow down all the factors responsible for phase noise, and provide a detailed and process specific model for phase noise in a differential VCO as proposed in this dissertation. Once this is achieved, it should be possible to decrease the phase noise in the system by evaluating the theoretical approaches presented in this section.

The primary RF noise sources in a SiGe HBT are the noises associated with the DC base and collector currents and the thermal noise of the base resistance [25].

2.3.1 BASE AND COLLECTOR CURRENT NOISE

Based on macroscopic views, the power spectral density (PSD) of the terminal resistance voltage noise is $4kTR$ and the PSD of the base and collector current noises are $2qI_{DC}$ or "shot" like, with I_{DC} being the DC base or collector current. The derivation of $2qI_{DC}$ shot noise

assumes a Poisson stream of an elementary charge q [25]. These charges need to overcome a potential barrier, and thus flow in a completely uncorrelated manner. In a bipolar transistor, the base current shot noise $2qI_B$ results from the flow of base majority holes across the emitter-base junction potential barrier. The reason that I_B appears in the base shot noise is because the amount of hole current overcoming the emitter-base junction barrier is determined by the minority hole current in the emitter. Similarly, the collector current shot noise results from the flow of emitter majority electrons over the emitter-base junction potential barrier, and has a spectral density of $2qI_C$.

2.3.2 TRANSPORT NOISE MODEL (UNIFIED MODEL)

The emitter current noise has two parts, one due to electron injection into the base, and the other due to hole current injection into the emitter. The PSD of the two parts are "shot" like, and given in (6) and (7).

$$S_{i_{ne}} = \frac{\langle i_{ne}^2 \rangle}{\Delta f} = 2qI_C \tag{6}$$

$$S_{i_{pe}} = \frac{\langle i_{pe}^2 \rangle}{\Delta f} = 2qI_B. \tag{7}$$

Further, because electron and hole injections are independent, $\langle i_{ne} i_{pe}^* \rangle = 0$. The collector current shot noise is a delayed version of the emitter electron injection induced shot noise, $i_c = i_{nc} = i_{ne} e^{-j\omega \tau_n}$, where τ_n is the transit time associated with the transport of emitter injected electron shot noise current and can be extracted from measured noise data or noise simulation [15]. Using the above results, the following are obtained.

$$\langle i_c^2 \rangle = \langle i_{nc} i_{nc}^* \rangle = 2qI_C \Delta f \tag{8}$$

$$\langle i_e^2 \rangle = \langle i_{ne}^2 \rangle + \langle i_{pe}^2 \rangle = 2qI_E \Delta f \tag{9}$$

$$\langle i_e i_c^* \rangle = 2qI_C e^{-j\omega \tau_n} \Delta f. \tag{10}$$

This transport shot noise model is also referred to as the unified model, in part because it can be reduced to the conventional Simulation Program with Integrated Circuit Emphasis (SPICE) noise model by setting τ_n equal to zero (or when $\omega \ll 1/\tau_n$). Several investigations have shown that this model enables accurate modelling of both experimental (macroscopic) and

microscopic noise simulation data in SiGe HBTs [25].

2.3.3 AVALANCHE NOISE

So far, it was assumed that collector current equals the electron current entering the collector-base depletion layer. At high collector-base voltages, however, electrons can gain enough energy to create electron-hole pairs via impact ionization and cause avalanche multiplication of carriers. The collector current can be considerably higher than the electron current transported from the emitter. The electron current shot noise transported from the emitter-base junction will experience the same collector-base electric field and hence be amplified through avalanche multiplication. In addition, the impact ionization process itself has noise. The net result is a significant increase of transistor terminal current noise at high collector-base voltages. In a typical SiGe technology, the highest f_T device has the lowest breakdown voltage and can suffer from avalanche noise at high collector-base voltage [25].

Transistor noise models, types of noise present in semiconductor devices, and more specifically, noise sources in SiGe HBTs have now been discussed and should have provided the reader with valuable insight into noise generation in semiconductors. As mentioned in Chapter 1, this dissertation focuses on phase noise in oscillators, specifically in SiGe BiCMOS 0.35 µm process technology. The following section (Section 2.4) is dedicated to provide insight on phase noise in oscillators, to aid in determining the final model or equation for the phase noise generated in the proposed design. A background to phase noise with reference to Leeson's model is presented together with additional terms to evaluate phase noise performance in oscillators.

2.4 PHASE NOISE IN OSCILLATORS

Before presenting the model for phase noise in the form of Leeson's model, it is important to first point out on a graphical representation what exactly phase noise means from a practical point of view. Once this has been done, Leeson's model is presented providing more mathematical insight into phase noise.

2.4.1 INTERPRETING PHASE NOISE (GRAPHICAL APPROACH)

The unit for phase noise is dBc/Hz at a specified offset. For instance, -150 dBc/Hz means that for 1 Hz bandwidth, at a specified offset frequency from the carrier (centre) frequency, the

single sideband noise power is 10^{-15} of the total signal power [1]. The offset from the carrier frequency where the phase noise is measured is depicted in Figure 7.

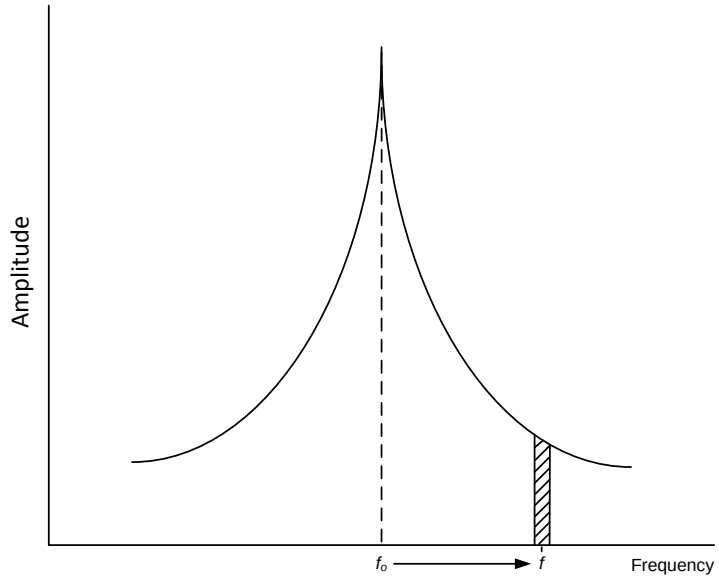

Figure 7. Single sideband phase noise to carrier power ratio.

This offset (f) is usually rated at 10 kHz, 100 kHz, or 1 MHz from the carrier (f_0), depending on the actual size (frequency) of the carrier signal and the application. For circuits operating in the GHz range, the phase noise is often measured at 1 MHz offset from the carrier [14], [15], [16], [17], and [18]. For this dissertation, the operating frequency is 5 GHz and the offset frequency specification is 1 MHz. As phase noise is the ratio of power in the carrier compared to the power present at the specified offset, it is evident that this ratio will increase as the offset frequency decreases [3]. This relationship is depicted in Figure 8. *Figure 8 is adapted from [3]*.

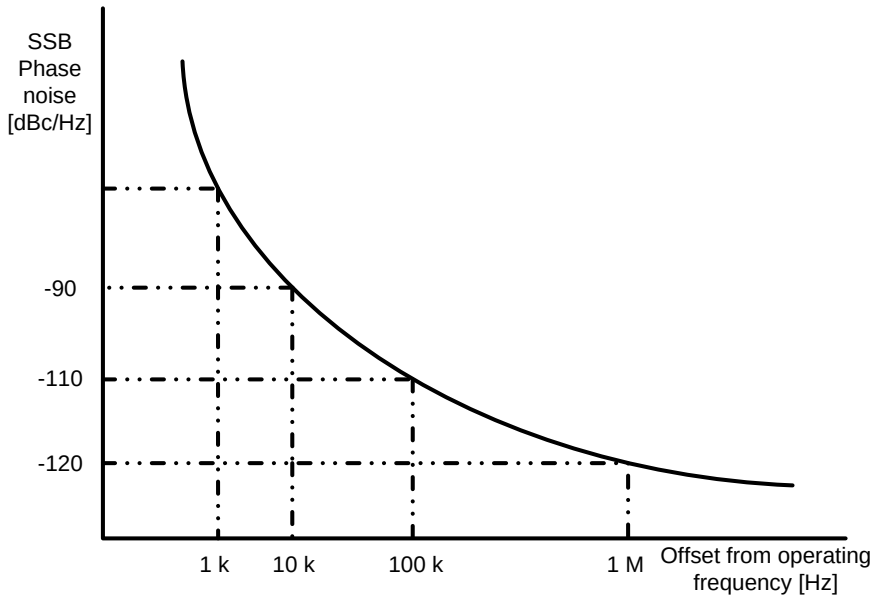

Figure 8. Single sideband offset relations.

Figure 8 is a spectral density plot of the phase modulation sidebands in the frequency domain and is expressed in dB relative to the carrier per Hz bandwidth.

2.4.2 INTERPRETING PHASE NOISE (MATHEMATICAL APPROACH)

One of the most well-known models for predicting phase noise in feedback oscillators is Leeson's model [27]. This model is depicted in Figure 9. *Figure 9 is adapted from [26]*.

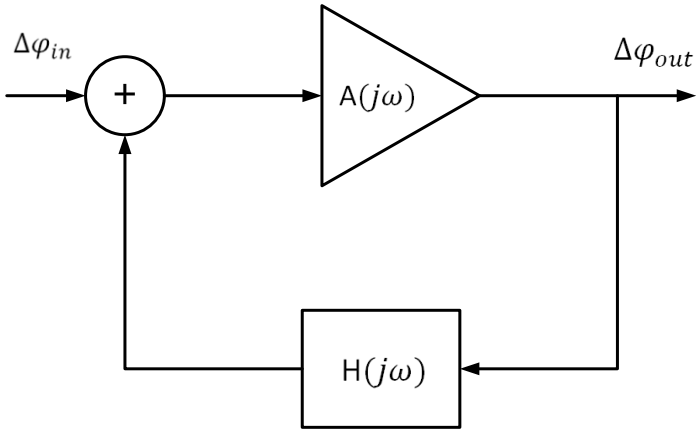

Figure 9. Representation of feedback oscillator using Leeson's model.

Leeson [27] has derived the following expression by using a single resonator feedback network. This expression [26] is called the *Leeson* formula (11) and is given on the following page,

$$\mathcal{L}\{2\pi f_m\} = 10\log\left[\left[\left(\frac{f_0}{2Q_L f_m}\right)^2 + 1\right] \times \frac{FkT}{P} \times \left(\frac{f_c}{f_m} + 1\right)\right] \quad (11)$$

where f_m is the offset frequency (measured at 1 MHz) from the 5 GHz carrier (f_0), $L\{2\pi f_m\}$ is the noise level at f_m in dBc/Hz, Q_L is the loaded Q (refer to Section 2.5.2) of the tank circuit, k is Boltzmann's constant (1.38 x 10^{-23} J/K), F is the noise factor, T is the operating temperature (300 K), P is the carrier power in mW, and f_c is the corner frequency for flicker noise.

To get a better understanding of this equation, a derivation is given below.

An oscillator is in actual fact an amplifier with positive feedback, as can be seen it Figure 9. The noise figure (F) of this amplifier is given by [28]

$$F = \frac{SNR_{in}}{SNR_{out}} \quad (12)$$

where SNR_{in} is the signal-to-noise ratio at the amplifier input, and SNR_{out} is the signal-to-noise ratio at the output of the amplifier. This can be related to the total noise power. By taking into account that the input noise power (N_{in}) is always taken as the noise in the source resistance which is a constant, and equal to $N_{in} = kT_0B$ = -174 dBm at room temperature (with a 1 Hz specified bandwidth), and the output noise power (N_{out}) is the total output noise including the circuit contribution and noise transmitted (with gain added) from the source resistance [28]. From (12), the noise figure can be rewritten as

$$F = \frac{S_{in}}{N_{in}}\frac{N_{out}}{S_{out}} \quad (13)$$

where S_{in} and S_{out} are the input and output signals respectively. For an ideal noiseless amplifier, all output noise comes from the source resistance at the input, and thus if the circuit gain is *G*, the output signal and the output noise is given by

$$S_{out} = GS_{in} \tag{14}$$

$$N_{out} = GN_{in} \tag{15}$$

however, substituting these two equations into (13), the noise figure is found to always be 0 dB. An alternative definition for the noise figure can be derived from (13) as follows.

$$F = \frac{S_{in}}{N_{in}} \frac{N_{out}}{S_{out}} = \frac{N_{out}}{GN_{in}} \tag{16}$$

This equation can be rewritten as

$$F = \frac{total\ \ output\ \ noise}{part\ \ of\ \ output\ \ noise\ \ due\ \ to\ \ source\ \ resistance} \tag{17}$$

which is given as a power ratio, and the value is given dB. The noise power at the input of the amplifier can be rewritten as GkT_0B, leading to the following equation:

$$F = \frac{N_{out}}{GkT_0B} \tag{18}$$

where T_0 is the absolute temperature of operation (usually 300 K) and B is the bandwidth for which the noise is measured. According to [28], the input phase noise in a 1 Hz bandwidth at any offset frequency $f_0 + f_m$ from the carrier frequency, produces a phase deviation of

$$\Delta\theta_{peak} = \frac{V_{nRMS\ 1}}{V_{sRMS}} \tag{19}$$

$$= \sqrt{\frac{FkT_0}{P_{ave}}} \tag{20}$$

where $V_{nRMS\,1}$ represents the phase noise at the offset frequency $f_0 + f_m$ and V_{sRMS} represents the phase noise at the carrier frequency (f_0) and P_{ave} is the average power of the oscillator circuit. This equation (20) can be expressed in RMS terms as

$$\Delta\theta_{1RMS} = \frac{1}{\sqrt{2}} \sqrt{\frac{FkT_0}{P_{ave}}}. \tag{21}$$

A correlated random phase relation exists at the opposite side of the carrier frequency $(f_0 - f_m)$ therefore the total RMS phase deviation can be written as

$$\Delta\theta_{totalRMS}\,(f_m) = \sqrt{\frac{FkT_0}{P_{ave}}}\,. \tag{22}$$

From (22), the one-sided spectral density (distribution) of the oscillator can be equated by taking the square of the RMS phase deviation at an offset f_m divided by the bandwidth [29], thus giving

$$S_\theta(f_m) = \frac{\Delta\theta^2_{totalRMS}\,(f_m)}{B} = \frac{FkT_0}{P_{ave}}\,. \tag{23}$$

This noise is therefore defined as a constant, and is dependent on the average power dissipation in the oscillator, and the constant term kT_0B = -174 dBm (in a specified 1 Hz bandwidth) as well as the oscillator noise figure. This noise is active from the frequency

$$f_1 = \frac{f_0}{2Q_L} \tag{24}$$

where Q_L is the loaded *Q*-factor of the oscillator tank circuit.

The active devices in the oscillator degrade the spectral purity of the signal as flicker noise in these devices is generated close to the carrier signal. This frequency has a $1/f$ characteristic, with a specified corner frequency f_c. The spectral density can thus be characterized, including the effect of flicker noise and the corner frequency, by adding a term to (23) as given below, and by multiplying the bandwidth into the term,

$$S_{\theta in}(f_m) = \Delta\theta^2_{totalRMS}\,(f_m) = \frac{FkT_0B}{P_{ave}}\left(1 + \frac{f_c}{f_m}\right)\,. \tag{25}$$

Thus the noise spectral density now has a certain gradient, compared to the constant value obtained in (23). This will become apparent when the phase noise plot is given in Figure 10.

For an amplifier with positive feedback, the phase noise at the input of the amplifier is affected by the bandwidth of the resonator circuit. The amplitude response should give a clear representation of this bandwidth. The transfer function of a band-pass circuit (as is the case of any resonator), can be characterized by an equal low-pass transfer characteristic [29], given below.

$$L(2\pi f_m) = \frac{1}{1+j\left(2Q_L\frac{f_m}{f_0}\right)} \tag{26}$$

where the term $f_0/2Q_L$ is equal to half the bandwidth of the low-pass transfer function of the oscillator. The phase noise of the oscillator is transmitted non-attenuated through the oscillator up to half the bandwidth. The closed loop response of the phase feedback, can therefore be determined from (26), and is given by

$$\Delta\theta(f_m) = \left(1 + \frac{f_0}{j(2Q_L f_m)}\right)\Delta 2\pi f_{in}(f_m) \tag{27}$$

and similarly to (23),the spectral density can be found by taking the square of the phase, as

$$S_{\theta out}(f_m) = \Delta\theta^2(f_m) = \left[1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right] S_{\theta in}(f_m) \tag{28}$$

where $S_{\theta in}(f_m)$ is the input spectral phase noise, defined by (25).
The single sideband phase noise at the output of the amplifier can thus be expressed by (29).

$$\begin{aligned}\mathcal{L}(f_m) &= \frac{1}{2}\left[1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right] S_{\theta in}(f_m) \\ &= \frac{1}{2}\left[1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right]\frac{FkT_0B}{P_{ave}}\left(1 + \frac{f_c}{f_m}\right)\end{aligned} \tag{29}$$

and if this equation is rearranged, it can be shown to resemble Leeson's equation given in (11), and the final phase noise equation is given on the following page. Therefore,

$$\mathcal{L}\{f_m\} = 10\log\left[\left[\left(\frac{f_0}{2Q_L f_m}\right)^2 + 1\right] \times \frac{FkT_0}{P} \times \left(\frac{f_c}{f_m} + 1\right)\right] \quad (30)$$

represents single sideband phase noise of an oscillator in dBc/Hz. This equation can be represented in graphical form to give an indication of the influence each term has on the overall phase noise. A representation is given in Figure 10.

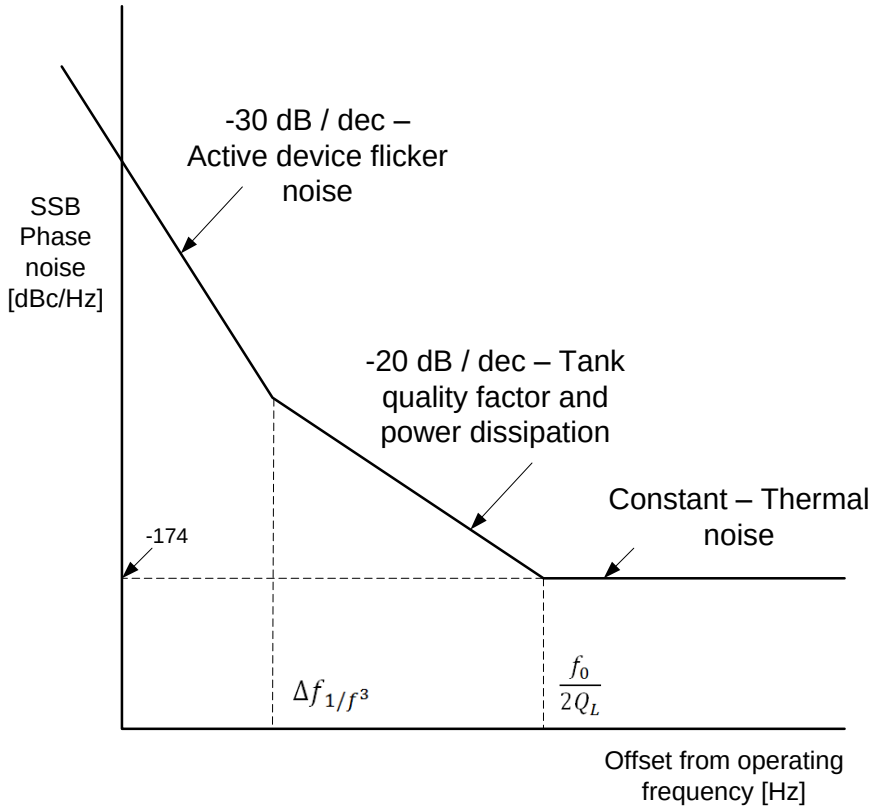

Figure 10. Phase noise graphical representation of Leeson's equation.

From (30) [26], it is evident [11] that phase noise (at a given offset frequency) improves with increasing carrier power (which is considered a trade-off in a low power design strategy as followed in this dissertation) as the ratio to the fixed thermal noise is increased, and increasing Q_L, the tank's loaded quality factor. At large frequency separations, the flat noise floor in dBc/Hz simply becomes the difference between the power delivered into the amplifier and the noise floor of the amplifier in dBm/Hz. Also, at frequencies close to the carrier frequency, the bandwidth of the filter causes the noise that is produced at the amplifier output to be amplified with a positive feedback that depends on the frequency separation. Finally, it can be noted that at some frequency separation, flicker noise will cause phase modulation. The flicker noise slopes at 10 dB/decade and changes the slope of the amplifier phase shift from

20 dB/decade to 30 dB/decade. In [26] it is shown that by directly applying Leeson's formula, a maximum (flattened) noise floor of -174 dBc/Hz can be achieved at 100 kHz from the offset frequency.

2.4.3 EVALUATING OSCILLATOR PERFORMANCE (FIGURE OF MERIT)

To evaluate the overall performance of a VCO, the figure of merit (FOM) can be determined in terms of the phase noise presented in Section 2.4.2 by [3]

$$FOM = 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log L\{\Delta f\} - 10\log P_{DC} \tag{31}$$

where $L\{\Delta f\}$ is the single sideband phase noise measured at a frequency Δf from the carrier, and P_{DC} is the DC power consumption in milliwatt (mW). From [8], (31) can be rewritten as

$$FOM = 10\log\left(\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P_{DC}}\right). \tag{32}$$

where the inverse proportionality between the FOM and the power in the carrier is evident.

2.5 TECHNIQUES OF REDUCING PHASE NOISE

Now that the theory behind the phase noise phenomenon has been discussed, an approach to reducing phase noise in oscillators should be followed to move closer to determining a well-defined phase noise model for the proposed VCO with phase noise reduction included. This will, as mentioned, contribute significantly to current works in giving a good mathematical model for determining phase noise. This section describes the available techniques that can be employed to reduce the phase noise of a VCO operating in the GHz frequency range, taking into consideration topology enhancements as well as factors that affect component noise. Firstly, some considerations in terms of the specific topology used for the oscillator are researched to determine which topology should present the best phase noise performance considering the processes available (i.e. cost effectiveness also considered).

2.5.1 VCO TOPOLOGY CONSIDERATIONS

The topologies considered are crystal, ring and LC oscillators. Each topology is discussed briefly and the advantages and disadvantages of each are highlighted.

Crystal oscillators

A quartz crystal oscillator is a thin slice of quartz crystal with conducting electrodes on opposing sides. Applying a voltage across the crystal displaces the surfaces, and vice versa. The quartz is stiff, and the crystal has a natural mechanical resonant frequency, depending on the orientation of the slice in relation to the crystal lattice (cut) [30]. Optimum oscillation frequencies for crystal oscillators are usually in the MHz range [32], with quality factors even exceeding 50000 in some cases [33]. For GHz crystal oscillators, expensive crystals eliminate the ability to manufacture cost-effective integrated oscillator systems.

Ring oscillators

A ring oscillator consists of a loop of a string of N identical stages. A single stage consists of an inverter together with a transmission line that connects subsequent stages to one another. In addition, there is a feedback connection between the first and last stage of the ring oscillator [34] and [35]. A ring oscillator can easily be designed using standard cell components. The transmission lines are used as delay lines and with the help of the resulting respective delay times, which influence the oscillation periods of the ring oscillators, one is able to calculate the transmission line parameters. The transmission lines must therefore dominate the behaviour of the ring oscillators.

Ring oscillators are a promising option due to their ease of implementation and wide frequency tuning range. They are compatible with digital CMOS technologies and occupy small chip area. Ring oscillators generally have inferior phase noise performance compared to LC oscillators due to the fact that a ring oscillator stores a certain amount of energy in the capacitors during every cycle and then dissipates all the stored energy during the same cycle, while an LC resonator dissipates only $2\pi/Q$ of the total energy stored during one cycle. Thus, for a given power dissipation in steady state, a ring oscillator suffers from a smaller maximum charge swing q_{max} [36]. Even though ring oscillators acquire small die area, it cannot meet the superior phase noise specification of LC oscillators. In order to achieve phase noise comparable with that of the LC oscillators, fast transitions are needed. Devices have to operate in a hard switching mode and be switched on and off completely, decreasing phase noise performance. The influence of parasitic elements is dominant at GHz operating frequencies, and circuit complexity must be low. Every additional device will add device and

interconnect parasitic elements that reduce the oscillation frequency and the carrier level. Although ring oscillators have not found many applications in RF systems until recently, they can be used for some low-tier RF systems [35]. Phase noise ratings of -98.5 dBc/Hz at 1 MHz offset from the carrier (operating at 5.43 GHz) have been reported for ring oscillators in [35].

LC tank oscillators

A general LC VCO consists of an inductor (L) and a capacitor (C) building a parallel resonance tank. It has an active element ($-R$), compensating the resistive losses of the inductor and the capacitor in the tank circuit [26] [16]. Both these components consist of internal, parasitic resistances that need to be countered in order to maintain oscillation. These circuits have a general resonant centre frequency, f_0, of

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{33}$$

The varactor capacitance is proportional to the tuning voltage V_{TUNE}, and f_0 is also dependant on V_{TUNE}, hence the term *voltage controlled* oscillator. Figure 11 represents the basic configuration of a LC VCO.

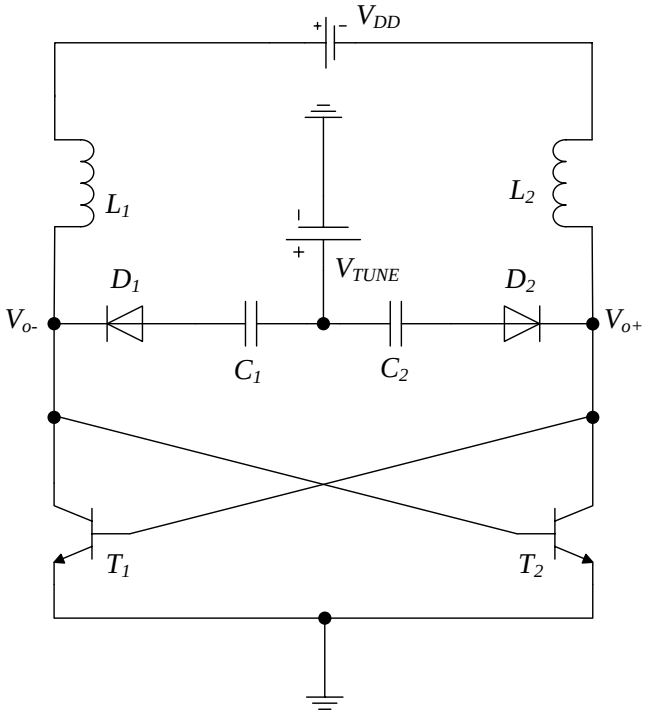

Figure 11. Basic representation of a LC oscillator circuit.

In comparison to ring oscillators, LC oscillators have a rather limited tuning range, but feature better phase noise performance and lower power consumption. For this dissertation, phase noise is the main design concern and therefore a topology that exhibits the lowest phase noise will be considered. The tradeoffs concerning this design choice will be closely studied and analyzed. The area of an LC oscillator with an integrated coil (inductor) is much bigger than the area of a ring oscillator. For RF applications operating at very high frequencies, inductor area does not have as large effect, as the inductor size decreases with higher frequencies.

Considering the background information of phase noise and oscillator topologies, it is now possible to discuss some methods of increasing oscillator performance, especially phase noise, by applying techniques of component placement and sizing, and topology enhancements. These methods will be applied to the LC oscillator topology as this topology presents the lowest phase noise available at high frequencies. Phase noise ratings between -110 dBc/Hz to -130 dBc/Hz at 1 MHz offset from the carrier, where the carrier frequency operates above the 5 GHz range is readily obtainable using this topology [9], [14], [16], [17], [18], [19], [20], and [26].

2.5.2 INDUCTOR AND CAPACITOR DIMENSIONING

BASIC INDUCTOR THEORY

An inductor (coil) generally consists of many windings of small diameter wire. A larger diameter would cut down the ohmic resistance, but might make the coil too large to use. Ideal inductors have no loss of power when current flows through the inductor. Practical inductors do in fact exhibit power losses due to several factors. These factors are due to

1. the skin effect which causes the coil wire resistance to increase at high frequencies [38],
2. eddy currents and hysteresis effects in the core that cause power loss that is dependent on both frequency and the core material [38],
3. the coil wire having finite resistance [41], and
4. radiation of power to the surroundings that takes place [38].

The losses in an inductor due to its finite resistance can be modelled as shown in Figure 12.

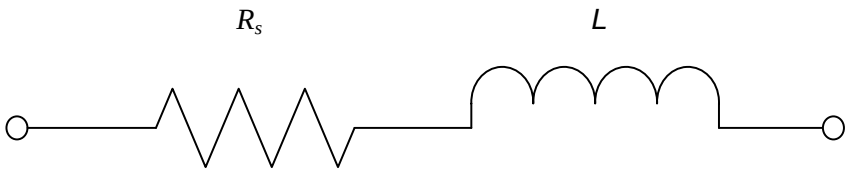

Figure 12. Inductor model with series resistance representing the losses in the inductor.

In Figure 12, L represents the inductance of the inductor and R_S represents the losses in the coil at the operating frequency [23]. The Q-factor of the inductor can thus be determined by

$$Q = \frac{2\pi f L}{R_S} \tag{34}$$

where f is the operating frequency. By adding a lossless capacitor in parallel with the inductor and resistor (as shown in Figure 13), a resonant circuit is created.

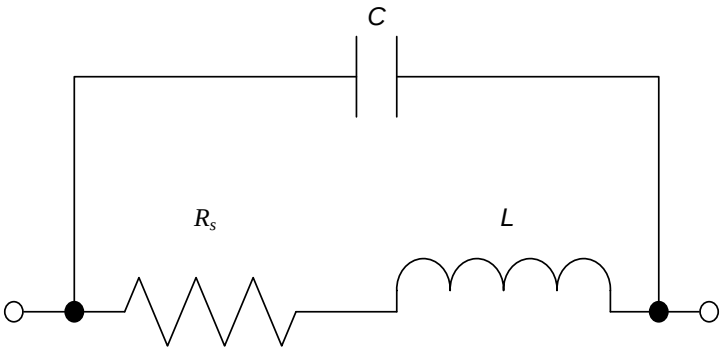

Figure 13. Parallel resonant circuit with addition of capacitor.

The Q-factor of this circuit still remains the same as in (34), as the capacitor is assumed to be lossless. The resonant frequency of the circuit in Figure 13 can be calculated by the following equation, which resembles (33) closely,

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{35}$$

where C is the capacitance of the capacitor. The impedance of this 'tank' circuit can be calculated by

$$Z = \frac{R_S + j2\pi fL}{-(2\pi f)^2 CL + j2\pi f R_S C + 1}. \quad (36)$$

Figure 14 depicts this magnitude as a function of frequency [23]. From Figure 14, it is evident that the parallel resonant circuit displays very large impedance at the resonant frequency. This characteristic can be used even in amplifier circuits when the load is to be tuned to a certain frequency, filtering out all frequencies adjacent to the centre frequency, depending on the bandwidth. *Figure 14 is adapted from [23]*.

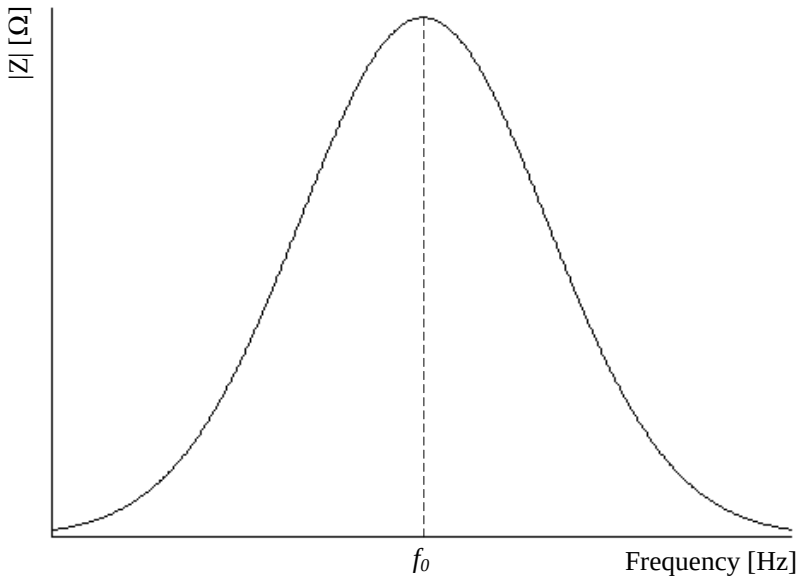

Figure 14. Magnitude of Z as a function of frequency.

The loaded Q of a resonator circuit describes the passband characteristics of the circuit under loaded or operating conditions. The loaded Q is expressed in terms of its parallel (shunt) resistor R_P where losses occur during operation. The effective, or loaded Q, due to resistive losses is given by [23]

$$Q_L = \frac{R_P}{2\pi f_0 L} \quad (37)$$

where f_0 is the operating frequency or the circuit in which the inductor is acting and $2\pi f_0 L$ is the reactance (X_p) of the inductor at resonance. Since the effective Q of the circuit is lowered by this resistor, the bandwidth of the circuit increases to

$$BW = \Delta f = \frac{f_0}{Q_L}. \quad (38)$$

One method that is readily used is the dimensioning and placement of the inductor and varactor in the LC tank. The optimization of the tank quality factor automatically leads to a different design, as when separate inductor and capacitor quality factors are minimized [42]. The total tank inductance equals the inductance of the inductor. The total capacitance, in contrast, is the sum of the parasitic inductor capacitances (winding to substrate and winding to winding), the varactor capacitance, the unavoidable capacitances of the active elements compensating the losses in the tank, and the VCO loads (prescaler, mixer, inter-stage buffers, or output buffers). Many techniques exist for implementing inductors on CMOS integrated circuits, as the *Q*-factor of commercially available silicon processes are typically low with values ranging from less than 12 in the 1 – 5 GHz frequency range [43].

The tank design goals are to maximize the ratio of inductance to capacitance and the ratio of inductance to parasitic resistance [42]. For highest tank inductance to capacitance ratio, a MOS varactor with a high ratio of maximum capacitance over minimum capacitance (C_{max}/C_{min}) is preferred, as it enables the use of higher inductance values. For the maximum varactor quality factor, a minimum gate length is preferred, but the length should also be chosen higher to increase C_{max}/C_{min}. The detailed study of MOS varactor design will not be covered in this dissertation. The first goal is limited by the systematic tuning range specified for a given application, which has to be increased to meet the frequency specifications over component tolerances, and the specified temperature range. The second goal is fundamentally limited by the given technology back-end (number and type of metals, thickness and conductivity), although much can be obtained from an optimized inductor layout.

In inductor design, high quality factors are necessary as it affects the performance of RF subsystems [44]. Higher quality factors are achieved when inductor losses are minimized. Losses associated with inductors in CMOS are generally classified into two categories: metal losses and substrate losses [44]. Metal losses limit the realizable quality factor of inductors at lower frequencies, while substrate losses limit the quality factor at higher frequencies. Quality factor enhancement techniques are used to improve inductor *Q* by minimizing inductor losses. Several enhancement techniques that are considered in [44] are patterned ground shields, halo

substrate contacts and shunted metal layers. These structures are ideal for standard CMOS processes due to its ease of implementation and do not add to the cost of manufacturing the IC.

INDUCTOR IMPLEMENTATION TYPES

Numerous inductor implementations exist when designing and implementing circuits on IC level, although each option has its advantages and disadvantages. Some of the available options are external inductors, microelectromechanical system (MEMS) inductors, spiral inductors, bond wires, and micro-strip [40] style inductors. These inductors can present unloaded *Q*-factors of greater than 500 at 9.6 GHz [41], but they are used more for the higher RF frequency spectrum (from 10 GHz and up) and are therefore not discussed here. For the purpose of designing a low phase noise VCO operating at very high frequencies; it is of importance to choose an inductor that exhibits a good quality factor with minimum additive noise to the circuit, and keeping power dissipation to a minimum. Although standard spiral inductors supplied by AMS were used in the proposed design, the following discussion serves as a good background when designing inductors, whereas [41] provides detailed information on inductor design.

External inductors

External inductors, as the name suggests, are not implemented on the IC and are connected to the circuitry externally via the IC pins. At high operating frequencies, this can be very detrimental to overall system performance due to parasitic effects having a large effect on the inductance and the *Q* of the inductor. Figure 15 is a representation of an external (off-chip) toroid inductor.

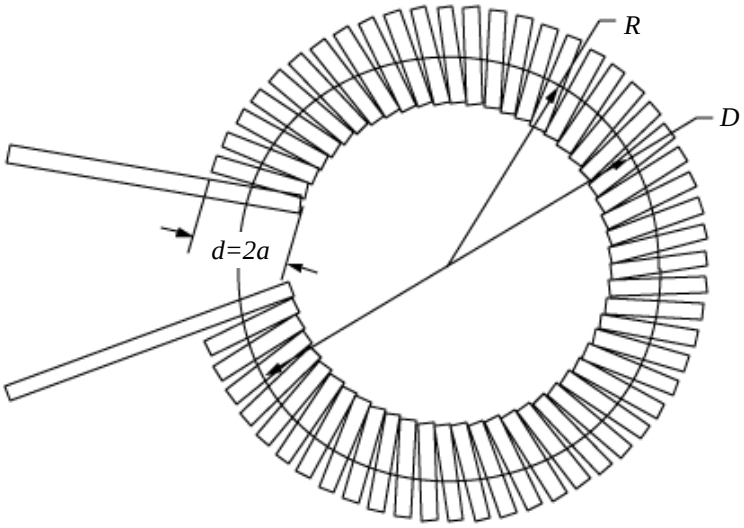

Figure 15. External inductor (toroid).

The toroid inductor shown in Figure 15 is commonly used as an external inductor due to its small physical size relative to solenoid inductors. The inductance of the toroid can be calculated by [46],

$$L \cong 0.01257N^2\left(R - \sqrt{R - a^2}\right) \tag{39}$$

where L is the inductance (in μH), R is the mean diameter of the windings to the core, N is the number of turns (windings), and a is the radius of the windings as can be seen from Figure 15.

MEMS inductors

In order to implement high Q inductors on a silicon substrate, two major loss mechanisms that limit the Q-factor on standard silicon processes have to be minimized. These losses are ohmic and the other is substrate induced losses. These factors can be minimized using MEMS inductors in CMOS implementations. Resistive losses arise from high resistivity materials used in etching processes, and the thickness of the metal layers that should ideally be much larger than skin depth. Substrate induced losses are due to electromagnetic coupling to the conductive substrate, where energy is coupled and dissipated through the lossy substrate, effectively lowering the Q of the inductor. With MEMS technology, the inductor is suspended by approximately 40 – 50 μm [47] from the top most layer of the substrate, and significantly reduces substrate coupling and resistive losses. Figure 16 represents an example of a suspended spiral inductor. Note the 40 μm air gap from the substrate. *Figure 16 is*

adapted from [47].

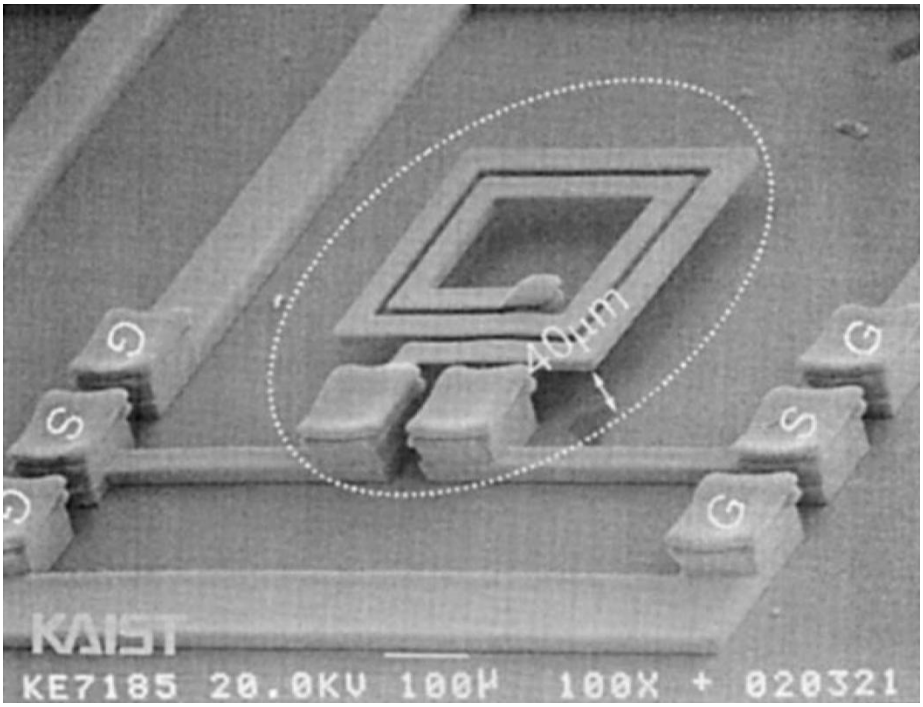

Figure 16. Suspended spiral inductor implemented using MEMS technology.

Techniques like suspended spiral MEMS inductors using surface micromachining technology can achieve *Q*-factors of over 25 in the 1 – 4 GHz frequency range [43]. Performance improvements of up to 7 dB have been reported in [43] at various offset frequencies by using MEMS inductors in VCOs. Implementing inductors using this method requires modifications to standard fabrication processes, making these designs less cost-effective, and alternative, less expensive methods are researched.

Multi-layer spiral inductors

Multi-layer spiral inductors (for instance helical inductors) are widely known and have been used extensively in CMOS chip designs [28]. The windings are stacked on top of each other in a multi-layer structure. The bottom layer winding acts as a shield for all the upper layers, resulting in significant reduction in substrate and fringe capacitance. A drawback is higher series resistance and lower quality factor [28]. Multi-layer inductors are also more expensive and difficult to fabricate [49]. For a 0.18 μm CMOS technology with a 2 μm thick top metal layer, a *Q* of 18 at a 4 GHz carrier has been reported in [50].

Bond wires

A physical representation showing the dimensions and placement of a bond wire [51] is depicted in Figure 17. *Figure 17 is adapted from [51]*.

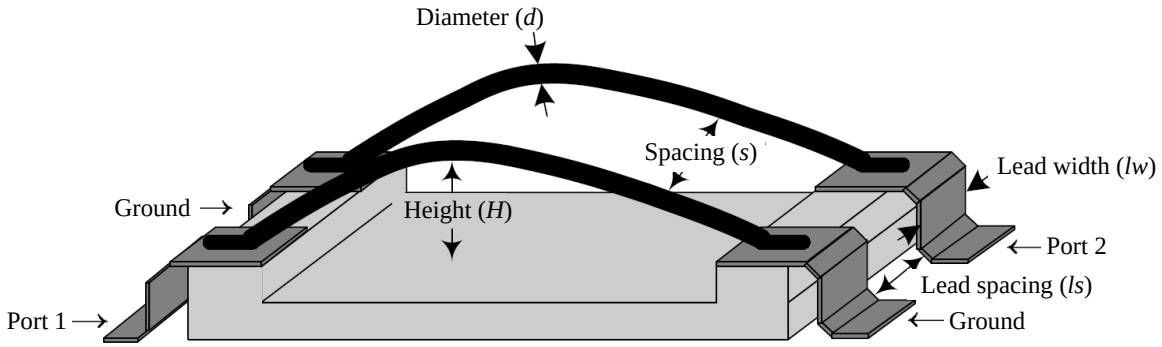

Figure 17. Bond wire representation.

A bond wire's characteristics (inductance and quality factor) are determined by the diameter (d) of the bond wire, the height (H) above the ground plane and the spacing between adjacent bond wires (s). By changing these dimensions, it is possible to control the inductance and Q-factor of the bond wires for use in integrated circuits [51]. From [52], due to bond wire characteristics, a Q value of 25 at 1 GHz can be achieved, exhibiting VCO phase noise ratings of -137 dBc/Hz at 1 MHz offset from the centre frequency [52], however; limitations to the actual inductance values (usually larger than 1 nH) make bond wires a less attractive option at frequencies of 5 GHz and beyond where inductance values below this value are needed.

Spiral (on-chip) inductors

Spiral inductors (see Figure 18) are commonly used in CMOS and BiCMOS processes because these inductors present a comparable quality factor to helical and micro-strip style inductors [48], but have an advantage of occupying less space compared to micro-strip style inductors, decreasing the required total die size. Spiral inductors can be constructed in a number of configurations (square, hexagonal, octagonal, and circular), but due to its ease of implementation, square spiral inductors are most commonly used [41]. Spiral inductors present a lower Q-factor compared to bond wires (see Figure 17); its inductance value is well defined over a broader range of process variations [41], whereas the software presented in [41] can be used in the design of the on-chip spiral inductor. Relevant geometrical parameters of spiral inductors are the number of turns (n), the conductor width (w), the spacing between the

conductors (s), and the inner and outer diameter of the spiral (d_{in} and d_{out}).

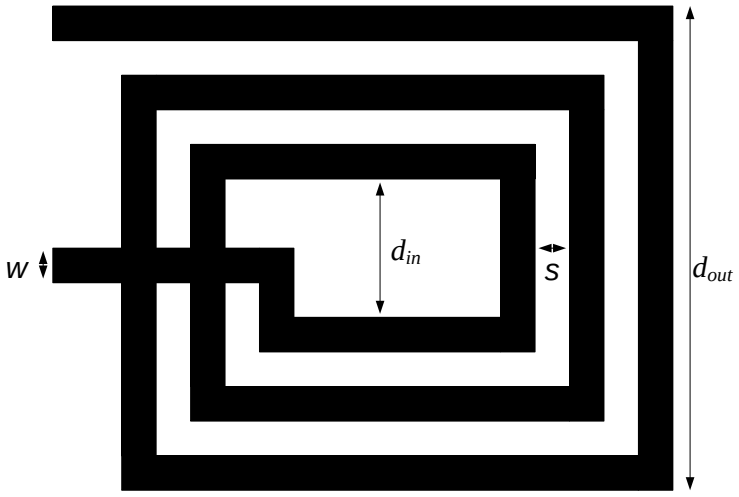

Figure 18. Integrated spiral inductor dimensions.

In order to determine the highest possible inductor quality factor for a given inductance value, in a given frequency range, it is of importance to be able to calculate the behaviour for any possible geometrical combination, and also taking into account the process parameters. Integrated on-chip metal inductors formed on conventional CMOS or BiCMOS processes suffer from performance limitations relating to issues like substrate injection through the oxide, substrate coupling by ohmic and displacement current, lateral currents to nearby substrate taps, and the skin effect. These effects limit the maximum inductor quality factor to quite low values (Q < 10) on typical low-resistivity substrates. Spiral inductors suffer from two fundamental problems. Firstly, the magnetic fields from the inductors project straight into the substrate where they induce *eddy* currents that cause resistive losses. Secondly, skin and proximity effects push the inductor current to the outer winding edge, reducing the effective winding cross-section, in effect lowering the total inductance. The inductance can be determined by the Wheeler equation [53], namely

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1+K_2 \rho} \tag{40}$$

where n is the number of turns, K_1 and K_2 are process parameters(for a square spiral inductor, K_1 is equal to 2.34 and K_2 is 2.75), d_{avg} is the average diameter of the inductor ($\frac{d_{out}+d_{in}}{2}$), and

ρ is the fill ratio ($\frac{d_{out}-d_{in}}{d_{out}+d_{in}}$). For the purpose of enhancing the *Q*-factor of the silicon integrated spiral inductor, the patterned-ground shield inductor has been presented by [54], showing 30 % improvement in its *Q*-factor, and another 33 % improvement in [55].

For the proposed design, spiral inductors as supplied by the foundry were used to minimize complexity and cost of the circuit. The inductor model used is presented in Section 3.2.3.

2.5.3 DESIGN PROCESS

Some comparable oscillator specifications have been achieved to date using CMOS, BiCMOS, and InGaAs/GaAs technologies. It is therefore important to weigh performance versus cost-effectiveness and ease of implementation as trade-offs when choosing the process technology.

A 5 GHz VCO designed in a 0.13 µm partially depleted silicon-on-insulator (SOI) CMOS has achieved a phase noise of -116 dBc/Hz at an offset of 1 MHz from the carrier. This design is however expensive due to the high resistivity SOI substrate and needs additional digital circuitry for the tuning varactors [16].

In [56], GaAs metamorphic high electron mobility transistor (mHEMT) based VCOs have achieved phase noise ratings of -120 dBc/Hz at 1 MHz offset (with a 7 GHz carrier), proving this technology to be more than sufficient. GaAs transistors exhibit extremely low noise figures and high f_{max}, but have low breakdown and operating voltages. Positive and negative voltage supplies are also needed and foundries are only now commercializing their mHEMT processes, making it expensive.

A 1.8 – 6 GHz multi-band (achieved using switched resonators) SiGe BiCMOS based VCO has been presented in [57]. This design operates at a supply voltage as low as 0.29 V due to the low knee-voltage provided by the technology, and consumes 580 µW of power. The design exhibits low power operation, good phase noise performance (-112.2 dBc/Hz at 1 MHz offset from a 5.8 GHz carrier) and a wide tuning range. To achieve the high tuning range, switched resonators are used that consist of MOS transistors, which are lossy and degrade the resonator *Q*.

From the above examples, it is evident that all these technologies, combined with some enhancement technique, display very good phase noise performance. Considering cost-effectiveness versus performance and ease of implementation, SiGe BiCMOS was chosen. An advantage of this process (without SOI) compared to GaAs, is its compatibility with silicon VLSI processes and scalability to higher current densities. This technology will be implemented using 0.35 µm SiGe BiCMOS process.

Relating noise figure (see Section 2.4.2) to SiGe HBTs presents the following. The ability to simultaneously achieve high cutoff frequency (f_T), low base resistance (r_b), and high current gain (β) using Si processing underlies the low levels of flicker noise, RF noise, and phase noise of SiGe HBTs. The minimum noise figure for a SiGe HBT with $g_m r_b \gg 0.5$ [16] is

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2} \tag{41}$$

This equation suggests that NF_{min} decreases (improves) with increasing β (160 for AMS S35D4M5 process) and f_T (60 GHz for AMS S35D4M5 process), and decreasing r_b. From [17], SiGe HBT excels in all three of these aspects, rendering the technology a very good competitor for low noise RF circuits.

2.5.4 TAIL-CURRENT SHAPING

Tail-current noise suppression in RF BiCMOS VCOs prevents the low-frequency tail-current noise from being converted into phase noise during normal operation of the oscillator [7]. The tail current is made large when the oscillator output voltage reaches its maximum or minimum value and when the sensitivity of the output phase to injected noise is the smallest [8]. The tail current is made small during the zero crossings of the output voltage when the noise sensitivity is large. No additional power is added to the system, ensuring low power operation at low noise levels. Tail-current shaping techniques reduce phase noise with three separate, but simultaneous mechanisms [9]. The increased oscillation amplitude, narrower drain current pulses, and finally the shunt capacitor that acts as a noise filter for the tail current, all contribute to lowering the phase noise. Figure 19 is a representation of the tail-current shaping technique.

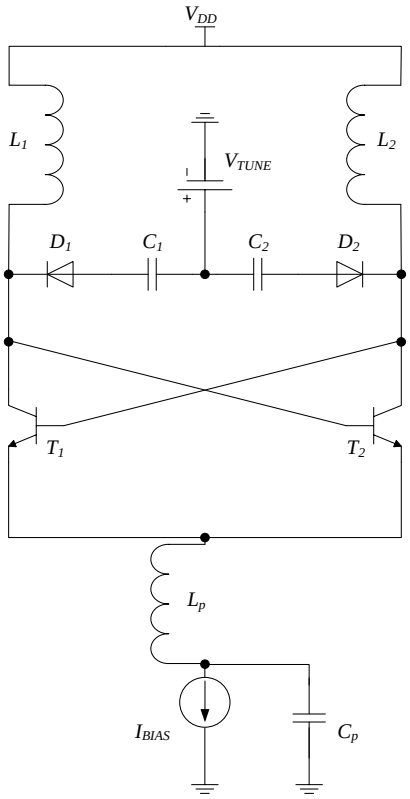

Figure 19. LC-based VCO with tail-current shaping circuit included.

This technique entails the use of an additional inductor (L_p) in series between the switching transistors and the MOS current source I_{BIAS}, to increase the impedance path between these sections at the oscillation frequency. It should be noted that MOS transistors are used in the tail-current source as its low frequency white noise which is up-converted to phase noise [58] can be reduced by reducing its transconductance / gain (g_m) through sizing of its aspect ratio (*W/L*). The power of the MOS transistor in the current source is reduced by the factor $\left|1 + j g_m \omega L_p\right|$ [7] where f_0 is the operating frequency. Capacitor C_p creates a small reactance path at the second harmonic, effectively shorting the noise effects at $2f_0$ towards ground.

Very few documented results were found using tail-current shaping through inductor and capacitor filtering for BiCMOS VCOs operating in the 5 GHz frequency range and using a BiCMOS technology. In [54] inductive filtering was used and a phase noise figure of -115 dBc/Hz at a 1 MHz offset from a 4.52 GHz centre frequency using TSMC 0.18 µm technology was presented. In [59] a phase noise of -90 dBc/Hz was achieved but at an offset frequency specified at 100 kHz (1 MHz offset performance not specified in [59]) from the 5.5 GHz carrier, using 0.18 µm CMOS technology.

The tail-current shaping technique is employed in the proposed design to reduce phase noise in the oscillator. By taking into account all of the theoretical derivations and mathematical models obtained up to this point, it is now possible to finally derive a mathematical model for the specific VCO implemented in the 0.35 µm BiCMOS process technology and using tail-current shaping to improve phase noise performance. The following section details the analysis.

2.6 SHAPING TECHNIQUE INFLUENCE ON PHASE NOISE

To reduce the phase noise with a filter added at the tail current-source, the following discussion is presented. The bias current is proportional to the output voltage, often referred to as the "current-limited" regime [8]. The high impedance path circulates odd harmonics in a differential path, while even harmonics flow in a common-mode path, through the switching transistors towards ground, and need to be bypassed by creating a temporary low impedance path. This entails the employment of a filtering technique to suppress low noise modulation of the dominant even (second) harmonic. Subsequent harmonics are assumed very small and negligible. The transistors in the differential pair then inject the tail current into the tank at the instants where the output phase of the VCO is less sensitive to injected noise currents. Additionally, at the zero crossings of the VCO output, where the phase sensitivity of the VCO to noise is at its maximum, the tail current becomes zero and the differential pair transistors do not carry any current, hence not generating any noise [8].

The first step is to add a capacitor across the MOS transistor in the current source. This capacitor (C_p) in parallel with the current source, is seen in Figure 20.

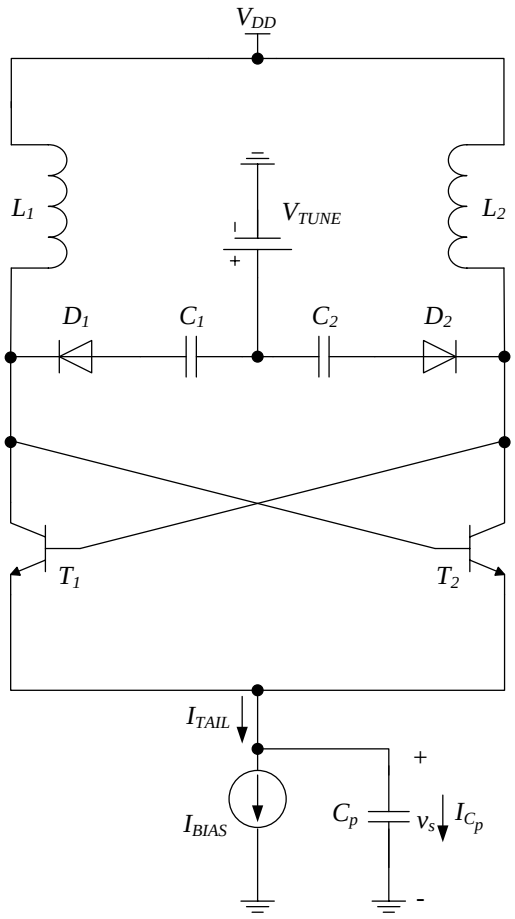

Figure 20. Differential, tail-biased VCO with bypass capacitor.

The capacitor adds a path that the current may follow during operation, as shown in (42).

$$I_{TAIL} = I_{BIAS} - I_{C_p} \tag{42}$$

It should be possible to limit the amount of current that passes through this newly added path by sizing of the capacitor. If it can be sized so that most of the current generated at $2f_0$, which is responsible for most of the noise up-conversion (see Section 2.5.4), it would mean that the noise performance should be improved. From [8] it can be shown that the voltage across the capacitor (v_s), is given by

$$v_s = A_s \cos(2\omega_0 t - \theta) \tag{43}$$

where A_s is the voltage amplitude at this point, and θ is the phase delay between the output

signal and the signal measured at the common emitters of the switching transistors. The current through the capacitor can therefore be equated by taking the differential,

$$i_c = C_p \frac{dv_s}{dt} = -2A_s\omega_0 C_p \sin(2\omega_0 t - \theta) \tag{44}$$

where v_s is given by (43). Therefore, the maximum current through the capacitor is $-2A_s\omega_0 C_p$. Referring back to (42), if this maximum current is set to I_{BIAS}, a minimum current I_{TAIL} is achieved at $2\omega_0$. Thus, if

$$C_p = \frac{2I_{BIAS}}{2A_s\omega_0} \tag{45}$$

where the $2I_{BIAS}$ current reflects the peak-to-peak value, the dominant part of the current at the distorted second harmonic will flow through the capacitor, towards ground during $2\omega_0$.

To ensure that the current at the fundamental frequency component, where most of the power lies, does not pass through the capacitor freely, an inductor (L_p) is placed between the current source and the differential pair, as depicted in Figure 21.

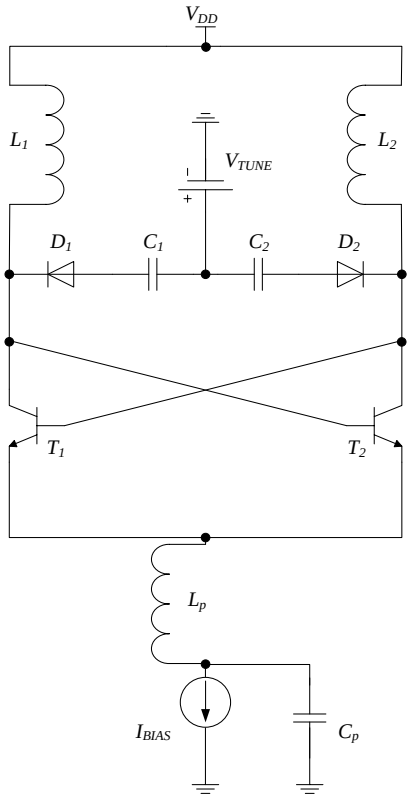

Figure 21. Differential, tail-biased VCO with bypass capacitor and inductor.

The inductor essentially creates a band-pass LC filter configuration together with the capacitor. If the ratio between the inductor and capacitor is chosen correctly, this should induce a filter with centre frequency $2f_0$. The inductor also increases the impedance path between the switching transistors and current source to avoid noise from the low frequency currents to be up-converted to phase noise in the oscillator. The inductor should therefore be sized according to the value of the capacitor at

$$L_p = \frac{1}{C_p(4\pi f_0)^2} \tag{46}$$

where the impedance is given by

$$Z_{L_p} = 4\pi f_0 L_p. \tag{47}$$

From (47) it is evident that the impedance of an inductor is dependent on the frequency of operation and the inductance of the inductor. Choosing a higher inductance would therefore

results in a higher impedance at a specific operation frequency.

2.7 CONCLUSION

This concludes the literature review of this dissertation. Chapter 3 discusses the methodology followed to implement the VCO. Further theoretical analysis will also become evident in the results section, where physical results will be compared to theory.

From [7], [8], and [22] an expected phase noise improvement of between 3 and 8 dB could be expected when implementing tail-current filtering. Designing the VCO using the differential LC topology, should provide a phase noise rating of between -100 and -110 dBc/Hz at 1 MHz offset when compared to current works (Table 1). Therefore, by combining the proposed topology and filtering technique, a minimum estimated phase noise of -110 to -115 dBc/Hz at 1 MHz offset from the centre frequency can be expected for the final implemented VCO. Further improvements can also be expected as proper inductor placement, as well as careful transistor sizing and placement will also be considered in the layout phase.

CHAPTER 3: METHODOLOGY

3 THEORY OF SCIENCE RESEARCH METHODOLOGY

This chapter describes the research methodology followed with reference to the methods introduced by [13].

3.1 RESEARCH METHODOLOGY OUTLINE

The following methodology was followed in order to undertake thorough research (and additionally the design) of the proposed topic of a low phase noise VCO. For a chronological summary of the steps taken for this dissertation, refer to Section 1.5 of this document. Section 1.5 also provides a flowchart of the research methodology followed to implement a low phase noise VCO operating in the GHz range.

This dissertation comprises of two main steps. Firstly, a literature study on some possible methods to reduce the phase noise of an integrated VCO. These techniques are discussed in Chapter 2. Each technique has its advantages and disadvantages, which are closely studied in order to find a suitable compromise in terms of design specifications, where phase noise performance was considered the core specification. The contribution of each technique towards lowering phase noise was therefore of utmost importance. The literature study (the hypothesis) was concluded by deciding on which technique to implement, and knowing the effect it would have on system performance. Simulations were created to prove the hypothesis, and these results are given in Chapter 5.

Secondly, (after choosing the appropriate phase noise reduction technique), the design was prototyped to further verify the hypothesis. Considering the theory of reducing phase noise by suppressing tail-current noise; also required were the consideration of all other aspects that might add to the noise introduced to the system. These include floor planning of the sub-systems on the IC (especially inductors which can mutually interfere), transistor sizing for optimum noise performance while considering power dissipation, operating speed of the VCO at 5 GHz, and effective packaging of the prototype to ensure that unaccounted, external, parasitic effects do not jeopardize system performance. A flow diagram of this process is provided in Figure 22.

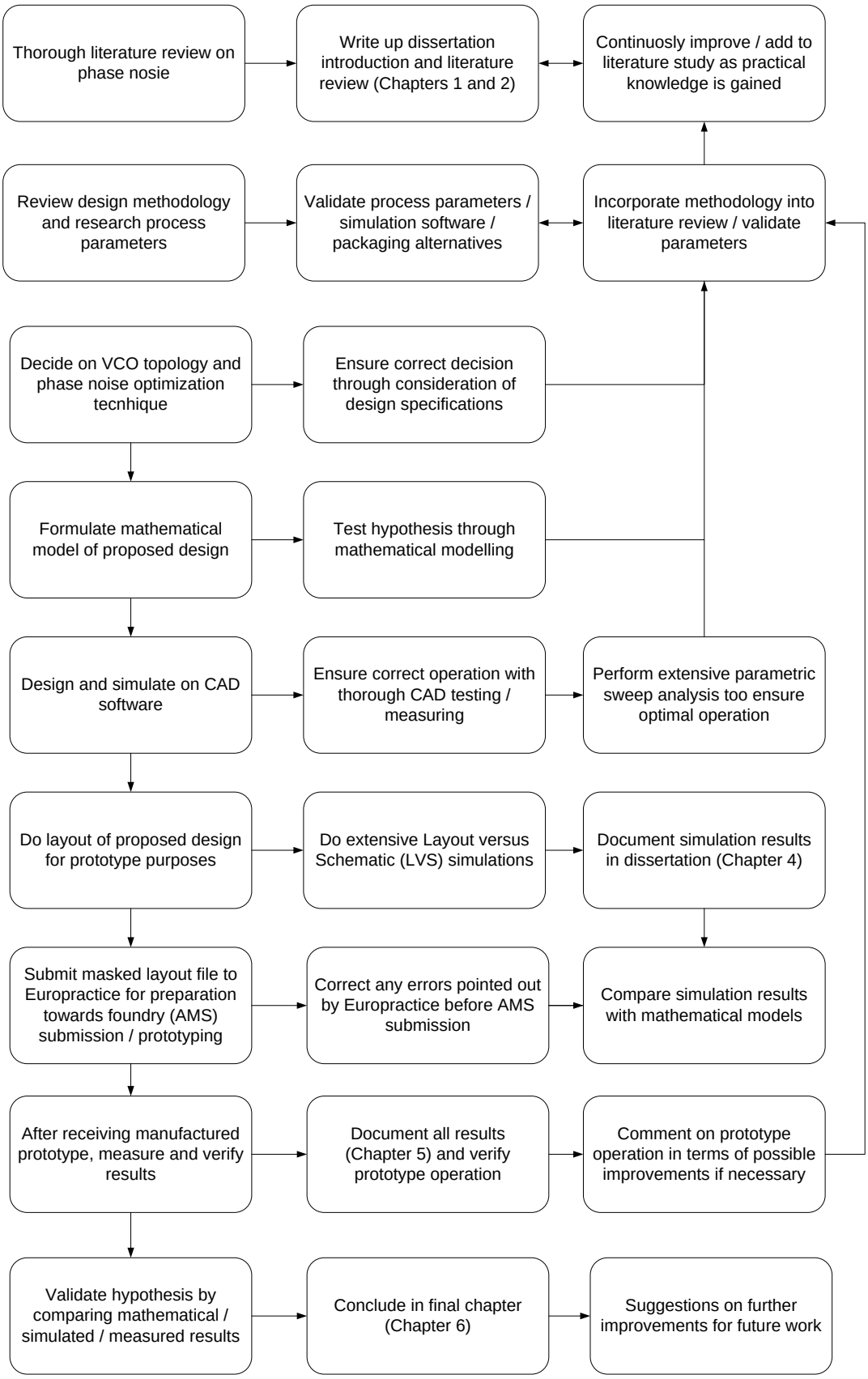

Figure 22. Flow diagram of overall research methodology followed in this dissertation.

Important factors to be considered are the technology used, process parameters, and component sub-circuit parasitic models. These models assist to understand the parasitic effects present at high operation frequencies by being able to physically model the component, and designing a circuit to counteract these effects. Thus, the first part of this chapter is dedicated to discussing the components that are implemented in the proposed VCO design. Specific values and physical dimensions of individual components are not discussed in this chapter (given in Chapter 4), as a general discussion of these components is given in this chapter.

The section following the discussion of component parameters looks at the software packages used to simulate (and prototype) the designs. The software discussed are Cadence® Virtuoso® [61] and Tanner Tools® [62], as both packages were used for the proposed design. Cadence® was used for the schematic design as phase noise can be simulated in this software, whereas Tanner Tools® was used to do the circuit layout. The reason for this choice is the fact that early layout simulations were done in Tanner Tools®, and license constraints delayed the switch to Cadence® Virtuoso® in turn limiting the amount of time available to port all designs to Cadence®. The decision was made to keep layout simulations in Tanner® Tools®. A limitation induced by this decision, is that the built-in "*layout versus schematic*" (LVS) of neither software packages could be utilized due to netlist incompatibilities between the software and manual hand-analysis LVS was done. Due to the relatively small size of the circuit, this did not present a big drawback. Library files containing the process parameters of the components for both packages were available and used. These files include all parameters present in each component supported by AMS, and are therefore of utmost importance to attain from the foundry before beginning the simulations (applicable for schematic and layout simulations).

A brief reference to how the IC is prototyped is then mentioned. Some aspects that need to be considered in terms of packaging of the prototype are discussed.

Finally (just before the conclusion), the measurement equipment used to practically determine the operation accuracy of the prototype compared to simulation results is discussed.

3.2 MANUFACTURING PROCESS

This section discusses the manufacturing process parameters and simulation software used to validate the hypothesis of the proposed phase noise reduction technique of the VCO. In this

section the AMS S35D4M5 components used in the proposed design are discussed in terms of general information, layout structure, sub-circuit model, main parameters, and some informative parameters considered during schematic design. Firstly however, a brief discussion of some of the general parameters is provided before considering each component individually.

3.2.1 *AMS 0.35 µm GENERAL PROCESS PARAMETERS*

The process chosen for manufacturing of the prototype was the S35D4M5 (thick metal) BiCMOS process, provided by AMS [63]. This section will point out some of the important parameters that were considered when designing the proposed circuit [64]. The author and the University of Pretoria are bounded by a non-disclosure agreement (NDA) with AMS, therefore complete details with regards to the process are not provided in this dissertation. Parametric models of components are included in this section which aid the designer in understanding the parametric parameters of each component, where it is situated and how to compensate for it. *It is important to note that the chosen component values are not discussed here, and are given in Chapter 4. Table 3 is adapted from [64].* The process parameters in Table 3 refers to typical mean, short-channel MOSFET devices, and typical mean, VBIC HBT models, as these models were used in this dissertation to simulate typical behaviour of the VCO. Future work could include adapting these simulations for worst-case models.

Table 3. 0.35 µm BiCMOS process parameters.

Parameter	S35D4M5
Drawn MOS channel length	0.35 µm
Drawn MOS emitter length	0.40 µm
Operating voltage CMOS	2.5 – 3.6 V
Gain (β)	160
Early voltage	100 V
Collector-emitter breakdown voltage (VBIC)	2.7 V
Cutoff frequency, f_T (VBIC)	60 GHz

Section 3.2.2 discusses the process parameters for the HBT transistor model used [65] with reference to Table 3.

3.2.2 *NPN TRANSISTOR MODEL*

The vertical bipolar transistor uses the buried layer as the collector, the SiGe base layer and the poly emitter. Two modules are available: high speed (*HS*) and high voltage (*HV*). A set of

model parameters for the Vertical Bipolar Inter-Company (VBIC) are supplied in this section. The RF SPICE model is valid for the following range.

Table 4. Validity of vertical HBT model.

Parameter	Maximum range
Frequency range	Few kHz – 20 GHz
Emitter width	0.40 µm
Individual emitter length	0.8 – 24 µm

Layout structure

Figure 23 depicts the cross section of a vertical bipolar transistor. The exact model shown is the NPN121 transistor, which means the transistor is a multiple base contact, single collector contact transistor. (NPN*xyz* refers to a NPN transistor with *x* amount of collector contacts, *y* base-, and *z* emitter-contacts).

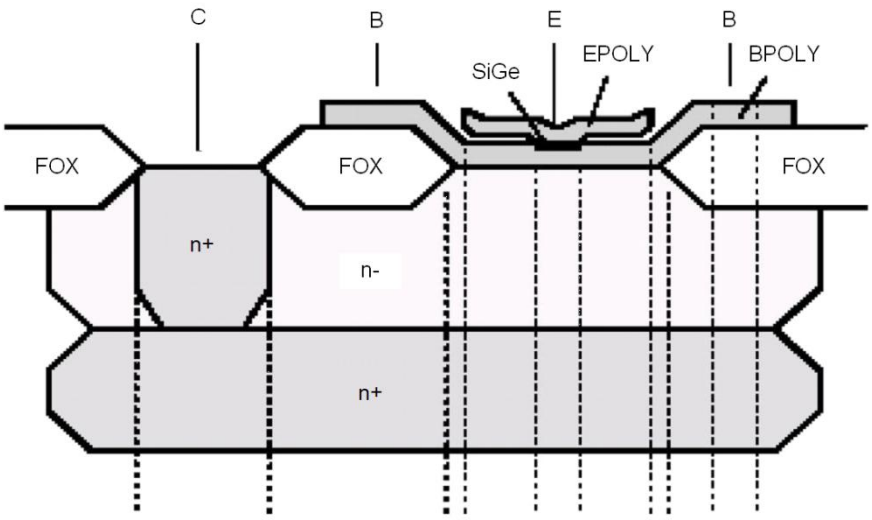

Figure 23. Vertical HBT layout structure.

Note from Figure 23 the insertion of SiGe on the base between the base and emitter region. Also important to note is that the circuit simulation parameters of the NPN bipolar transistors are referred to as an emitter length of L_0 = 1 µm. Thus, the actual emitter length (in µm) of the device L must be specified as the device area ($AREA = L / L_0$).

Main parameters

The f_T and f_{max} specifications for some of the transistor models are given in Table 5. The values for *HS* and *HV* transistors are given, with a V_{CE} of 2 V for *HS*, and V_{CE} of 3 V for the *HV* HBT transistors.

Table 5. HBT transistor measured parameters.

	f_T [GHz]		f_{max} [GHZ]	
	HS	*HV*	*HS*	*HV*
NPN111_12	< 60	≈ 40	< 50	< 50
NPN121_12	< 60	≈ 40	< 65	< 65

For the proposed design (see Section 4.1), the NPN111_12 *HS* transistor is chosen, and from Table 5 is it evident that the transistor can operate well above the 5 GHz range where the design is specified.

Information parameters

Some important parameters that are used in the schematic design of the proposed oscillator for the vertical NPN *HS* transistor model are given in Table 6. The table is valid for a constant emitter width.

Table 6. Vertical HBT information parameters.

Parameter	Typical	Unit
50 % gain collector current	< 2	mA/µm
Early voltage	> 100	V
Emitter resistance	< 30	Ω.µm
DC base resistance	< 600	Ω.µm
Collector-emitter breakdown voltage (open base)	≈ 2.5	V

Section 3.2.3 describes the parameters and models used to implement the inductors in the schematic and layout of the proposed VCO [65].

3.2.3 INDUCTOR MODEL

For effective operation in the 5 GHz range, thick metal inductors are used and not 3-metal inductors which are only rated at 2.4 GHz. The 3-metal library consists of 23 square inductors with values ranging from 1.3 nH up to 20 nH and 6 square symmetric inductors with values ranging from 1.4 nH up to 2.8 nH. The thick metal library consists of 14 square inductors ranging from 1.1 nH to 13.3 nH, with quality factors described later in this section. As

discussed in Section 2.5.2, the fixed square layout for inductors is used in the design, to minimize the complexity and cost of the IC.

Layout structure

The layout structure is not given here, as the standard layout is used without any alterations possible to the design. Only different inductors are chosen to alter the inductance and *Q*-factor, without adjusting its physical properties. Refer to [53] for more information.

Sub-circuit model

To account for the parasitic effects present at high frequency operation, a sub-circuit model is constructed for the inductor. Models are optimized for single ended operation, and P_1 always denotes the terminal with the higher quality factor. Figure 24 depicts the sub-circuit model for the inductor (3-metal and thick metal modules).

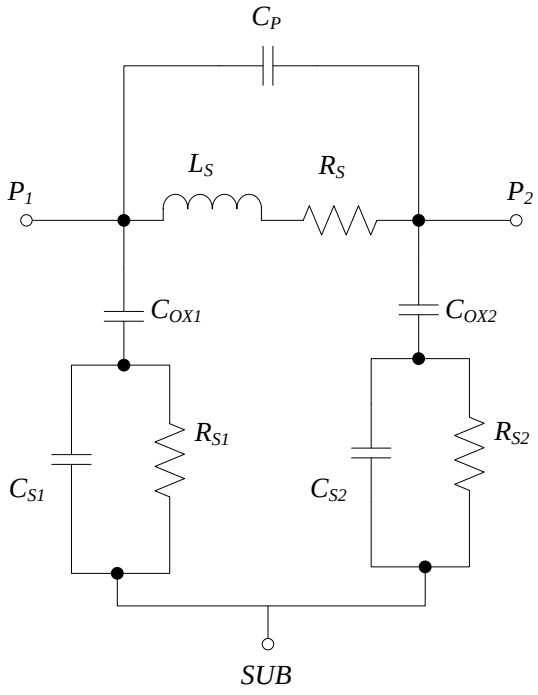

Figure 24. Inductor sub-circuit SPICE model.

Table 7 describes the parameters of the sub-circuit model shown in Figure 24. P_1 and P_2 are the contact areas of the inductor.

Table 7. Inductor model parameters with reference to Figure 24.

Parameter	Parameter description
L_S	Series inductance
R_S	Series resistance
C_P	Parallel capacitance
$C_{OX1/2}$	Oxide capacitances
$C_{S1/2}$	Substrate capacitances
$R_{S1/2}$	Substrate resistances

The following paragraph stipulates some of the main parameters that need to be taken into account when designing with the inductors, and gives some measured values of these parameters under certain operating conditions.

Main parameters

Important electrical parameters are summarized for P_1 drive operation calculated from the impedance ($Z = 1/y_{11}$).

- Effective Series Inductance: $L = \frac{Im(Z)}{\omega}$
- Effective Series Resistance: $R = R_e(Z)$
- Quality Factor: $Q = \left|\frac{Im(Z)}{Re(Z)}\right|$

where $\omega = 2\pi f$ and f is the frequency of operation (5 GHz), *Re(Z)* and *Im(Z)* are the real and imaginary part of the impedance. The main parameters are given in Table 8 below.

Table 8. Thick metal inductor measured parameters.

Inductor	Inductance [nH]			Q_{max}	Q		f_{res} [GHz]
	L_s	@ 2.4 GHz	@ 5.0 GHz		@ 2.4 GHz	@ 5.0 GHz	
Inductor A	≈ 1.5	≈ 1.5	≈ 1.5	≈ 11	≈ 10	≈ 10	> 6
Inductor B	≈ 2.5	≈ 2.5	≈ 2.7	≈ 10	≈ 9	≈ 6	> 6

As the *Q*-factor of the inductor plays the largest role in determining the *Q*-factor of the tank circuit (see Section 4.1.1), it is important to use an inductor with the maximum attainable quality factor while enabling the circuit to oscillate at 5 GHz through the design equations for the operating frequency, where the capacitance of the tank also has an effect on the parameter,

but with smaller effects on quality factor depreciation. The specific inductor that is chosen for the proposed design, and the reasoning thereof, will become apparent in Section 4.1.1.

Information parameters

No further electrical or informational parameters are available. Refer to Chapter 5 for simulation results. Section 3.2.4 describes the capacitor models (CMIM) that are used to construct the schematic and layout structures of capacitors in the circuit design [65].

3.2.4 METAL-METAL CAPACITOR (CMIM) MODEL

These capacitors were used to create the tank circuit for the oscillator, and therefore determine the oscillating frequency of the circuit. Capacitors ranging from 0.1 pF to 1 pF and different *W/L* ratios were measured to create the model described below. Based on theoretical calculations the series resistance lies within the order of 0.1 Ω resulting in *Q*-factors exceeding 100. The exact values of capacitances used to design for an operating frequency of 5 GHz are given and explained in Section 4.1.1 and 4.1.3. The model used in this section is valid in the following range, as given in Table 9.

Table 9. Validity of CMIM model.

Parameter	Maximum range
Frequency range	Few kHz – 6 GHz
Capacitance range	0.1 pF – 1 pF

The top plate contacts are placed over the whole area of the capacitor, and in the case of the bottom plate contacts, at least the opposite (longer) sides are contacted. The *WELL* (*n*-well) terminal is connected to the substrate or AC ground (e.g. V_{CC}).

Sub-circuit model

The sub-circuit model of the CMIM capacitor used in this design is given in Figure 25.

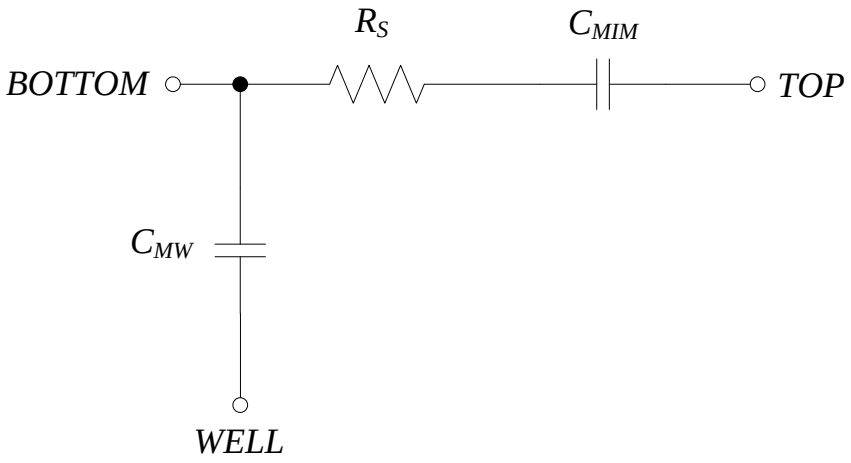

Figure 25. CMIM sub-circuit SPICE model.

Table 10 lists and explains the parameters present in Figure 25. *BOTTOM* and *TOP* refers to the bottom and top plate contacts, respectively. *WELL* is connected to the AC ground. Note that the major *Q*-factor limiting feature is the TOP plate contact resistance.

Table 10. CMIM model parameters with reference to Figure 25.

Parameter	Parameter description
C_{MIM}	Series capacitance
R_S	Series resistance
C_{MW}	METAL2-well capacitance

Information parameters

Important informative parameters are given in this section. These parameters allow for an oscillating frequency of 5 GHz, by altering the area (or effectively the *W/L* ratio) of the top and bottom plate of the capacitor.

Table 11. CMIM information parameters.

Parameter	Typical	Unit
CMIM area capacitance	1-2	fF/μm^2
CMIM perimeter capacitance	≈ 0.1	fF/μm
CMIM temperature coefficient	< 40	ppm/K

The *CMIM area capacitance* parameter is used to determine the precise capacitance of the implemented capacitor. Section 3.2.5 describes the important parameters and parasitic model of the MOS transistor, used in the proposed design to construct a current source for the VCO [65].

3.2.5 MOS MODEL

This section describes the structures used to create MOS transistors in the proposed circuit. MOS transistors are used in the current source of the VCO and the aspect ratio (*W/L*) is used to determine the amount of current supplied by the source. An active resistor, i.e. a MOS transistor with its gate connected to its drain is used instead of a resistor (see Section 3.2.7) to minimize thermal noise. This is only done in later simulations, as the results section in Chapter 5 will specify. The impedance of the active resistor is adjusted by altering the aspect ratio. Minimum length MOS transistors have been characterized at RF, with multi-finger transistors modelled as single transistors. Characterizing this model is described in this section. The model is valid for the following range, as given in Table 12.

Table 12. Validity of MOS model.

Parameter	Maximum range
Frequency range	Few kHz – 6 GHz
Maximum width	NMOS: 200 µm
Width of a single finger	5 or 10 µm

There are no PMOS implementations in the circuit design, therefore the width restriction of a PMOS can be ignored from this point forward. The frequency range of the transistor is within bounds, as this circuit will operate at 5 GHz, which is 1 GHz lower than its limitation as given in Table 12. The following paragraph describes the physical layout structure of the NMOS transistor (again the PMOS have been omitted).

Layout structure

Figure 26 depicts the physical layout structure of the NMOS transistor. This cross-section points out the fact that the n^+-contacts are situated in the p-well, with an underlying p-substrate. The source and drain of the transistor are connected to the n^+-contacts, and the bulk is connected to the p-substrate.

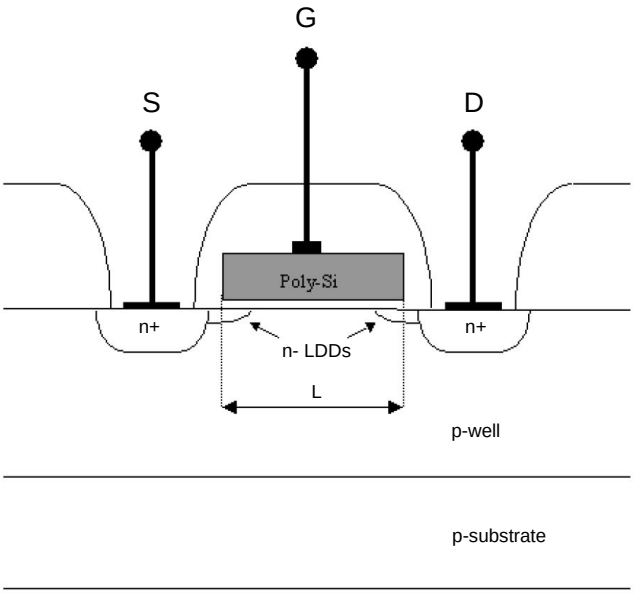

Figure 26. NMOS layout structure.

The poly-silicon gate of the transistor is altered in terms of its aspect ratio to manually control the amount of current flowing through the transistor. Through simulation and mathematical analysis it can be determined how much current should pass through the transistor in order to minimize the amount of noise generated. This is however discussed in 4.1.2. In order to take into account parasitic effects present in these transistors, thus not assuming an ideal structure, the sub-circuit model can be constructed to represent the non-ideal NMOS transistor practically implemented. This is discussed in the following paragraph.

Sub-circuit model

Figure 27 represents the sub-circuit model for the NMOS transistor.

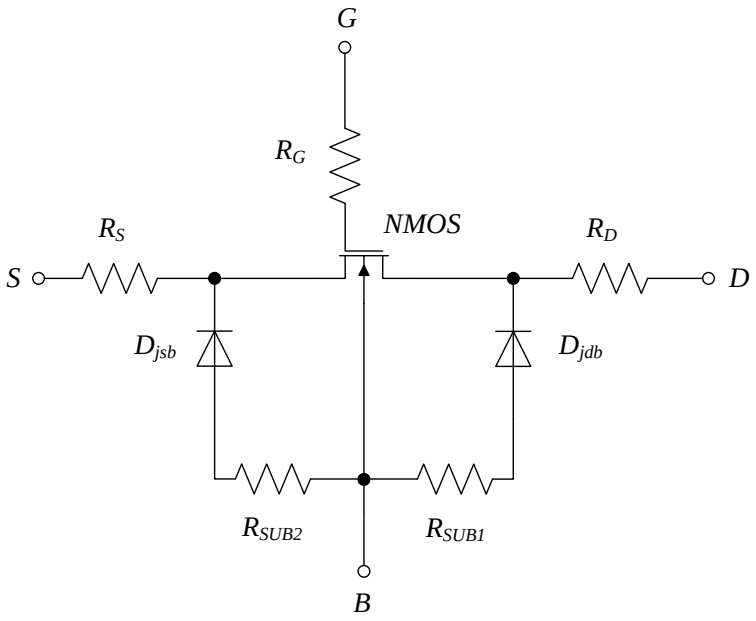

Figure 27. NMOS sub-circuit SPICE model.

From Figure 27, *G* refers to the gate contact, *S* to the source, *D* to the drain, and *B* to the bulk contact (for an NMOS, the bulk is always connected to ground, and for a PMOS, it is connected to V_{CC}) of the transistor. Table 13 describes the parameters of the NMOS sub-circuit model as shown in Figure 27.

Table 13. NMOS model parameters with reference to Figure 27.

Parameter	Parameter description
R_G	Gate resistance
R_D	Drain resistance
R_S	Source resistance
NMOS	Intrinsic NMOS transistor
$R_{SUB1/2}$	Model the substrate resistance
$D_{jdb/jsb}$	External diodes are used to model depletion capacitance of the D/B and S/B junction

Main parameters

For the NMOS transistor, Table 14 stipulates the f_T and f_{max} values compared to the width of a single finger. The finger-width used for the proposed design is given in Section 4.1.

Table 14. NMOS measured parameters.

W of finger [µm]	f_T [GHz]	f_{max} [GHz]
5	< 30	< 50
10	< 30	< 40

Information parameters

For this design, a 3.3 V power supply is used. Therefore, the electrical parameters of the NMOS operating under a 3.3 V (not the 5 V high-voltage parameters) supply is specified in Table 15. Short and long channel parameters are given, and Section 4.1 will specify clearly which type is used in the design of the current source.

Table 15. NMOS information parameters (3.3 V).

Parameter	Typical	Unit
Threshold voltage (long channel 10 x 10 µm)	≈ 0.50	V
Threshold voltage (short channel 10 x 0.35 µm)	≈ 0.50	V
Gain factor	< 200	$\mu A/V^2$
Effective mobility	< 400	cm^2/Vs

Table 15 specifies the typical values obtainable for each parameter.

Section 3.2.6 describes the varactor (CVAR) models that are used to construct the schematic and layout structures for variable capacitors in the tank circuit design [65].

3.2.6 VARACTOR (CVAR) MODEL

A varactor is achieved through an accumulation-mode MOS capacitor, implemented as a three terminal device. The model is valid in the following range, as stipulated in Table 16.

Table 16. Validity of CVAR model.

Parameter	Maximum range
Frequency range	Few kHz – 6 GHz
Total width	100 – 1000 µm

The frequency range for the varactor model presents no problems as the proposed circuit will operate at 5 GHz, there giving the device an overhead of 1 GHz to its maximum operating frequency. The design will however take into account the preferred column / row ratio, as this ratio affects the C_{max}/C_{min} ratio, which in turn affects the allowable tuning range of the device, as well as phase noise performance. For a detailed description of the ratios chosen for the design, refer to Section 4.1.1. The following paragraph describes the layout structure of the device.

Layout structure

The layout structure is important when considering the design of the device layout after the schematic design has proven good results for phase noise and tuning range. Depending on the ratios chosen, as mentioned in the previous paragraph, the following methodology is followed in constructing the physical layout of the device. Figure 28 depicts this layout structure.

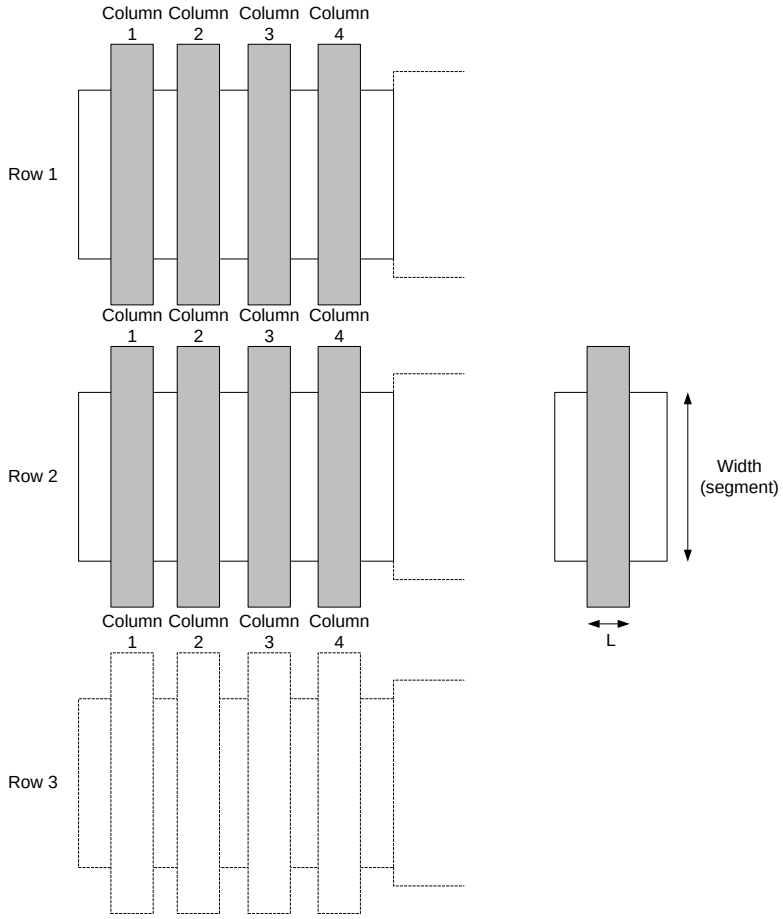

Figure 28. CVAR layout structure.

From Figure 28, it is evident where the width and length of the varactor is situated in terms of its geometry. This is used to determine the ratios needed for sufficient operation. For a detailed description on the specific width and length used in the circuit design, refer to Section 4.1.1. Table 17 gives the C_{max} and C_{min} values for the different available layout topologies in terms of the amount of rows and columns chosen.

Table 17. CVAR geometric dimensions.

W [µm]	Row	Col	L [µm]	C_{min} [pF]	C_{max} [pF]
950.4	9	16	0.65	< 1	< 3
158.4	3	8	0.65	< 0.2	< 0.5

The ratio of C_{max}/C_{min} is used to determine the tuning range of the device, and its phase noise performance. The sub-circuit model of the varactor depicts the parasitic components of the device for accurate mathematical modelling. Without this model, it would be assumed that the device is in fact ideal, which is however not the case in any practical implementation, especially in RF circuits, as parasitic effect often have a very large influence on circuit operation. This model is depicted in Figure 29.

Sub-circuit model

In Figure 29, it is important to note that *G* is the gate terminal of the device, *B* is the bulk (n-well) and *SUB* is the p-substrate, which in this design is always grounded.

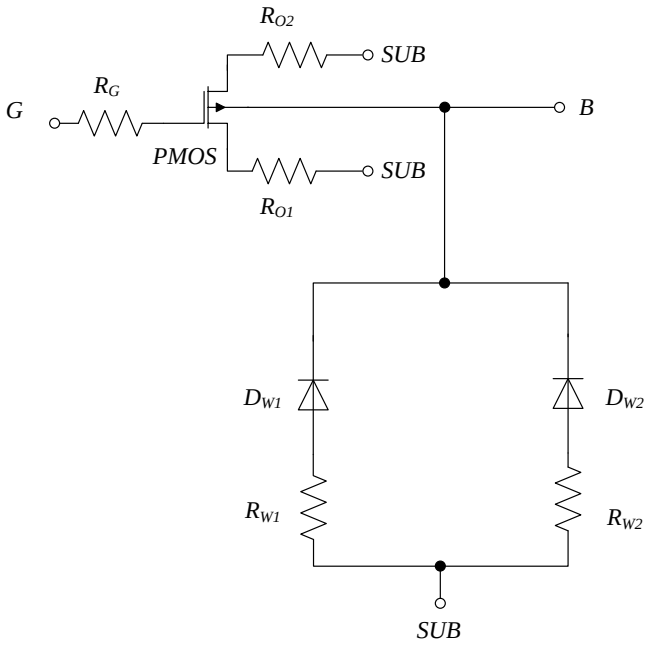

Figure 29. CVAR sub-circuit SPICE model.

Table 18 describes the parameters of the accumulation mode MOS varactor sub-circuit model as shown in Figure 29.

Table 18. CVAR model parameters with reference to Figure 29.

Parameter	Parameter description
R_G	Series resistance of the MOS capacitor
PMOS	Gate-bulk capacitance of a PMOS transistor
$R_{o1/2}$	Prevents the gate-bulk capacitance from rising to C_{max} in inversion
$R_{w1/2}$	Series resistance of the well
$D_{w1/2}$	Diodes used to model the depletion capacitance of the well

Main parameters

Important electrical parameters are calculated using the impedance between the gate and the bulk of the device ($Z = 1/y_{11}$).

- MOS Capacitance: $C = \frac{1}{-\omega Im\,(Z)}$
- Series Resistance: $R = R_e(Z) = R_G$
- Capacitance Tuning Range: $\gamma = \pm\frac{C_{max} - C_{min}}{C_{max} + C_{min}}$
- Quality Factor: $Q = \left|\frac{Im\,(Z)}{Re\,(Z)}\right| = \left|-\frac{1}{\omega RC}\right|$

where $\omega = 2\pi f$ and f is the frequency of operation (5 GHz), *Re(Z)* and *Im(Z)* are the real and imaginary part of the impedance, respectively. The real characteristics of *C* and *R* are independent of frequency, whereas *Q* depends heavily on the frequency of operation. The strong deviation in the *Q*-*V* characteristics is due to the approximation of the nonlinear series resistance with a constant resistance. A few of the measured parameters for the different layout structures are given in Table 19. Γ represents the tuning range of the device (which can be noted are very similar for all structures). The minimum *Q*-factor for each structure is also given, although this is at 2.4 GHz only, the 5 GHz value can be extrapolated from the information given in [65]. Note that the *Q*-factors are high compared to the inductor's quality (Section 3.2.3), and as mentioned in Section 2.5.4, do not play a large role in determining the overall quality factor of the tank circuit.

Table 19. CVAR measured parameters.

W [µm]	C_{max}/C_{min}	Γ [%]	Q_{min} (at 2.4 GHz)
950.4	< 4	< 60	< 80
158.4	< 4	< 60	< 45

The C_{max}/C_{min} ratios also appear to be very similar, almost appearing as a constant, limiting the amount of control on tuning range. This is not a problem, as the tuning range (although being somewhat compromised due to this reason) is not specified for the application of the proposed VCO which is intended for narrowband applications. Some general information parameters are given in the following paragraph.

Information parameters

The parameters given below are important to consider during the schematic design on the proposed circuit. Biasing the varactor at any of the voltages mentioned in Table 20 will help in giving a clear indication of the capacitive value added to the tank circuit of the VCO. As mentioned in the previous paragraph, the tuning range for this structure is almost constant.

Table 20. CVAR information parameters.

Parameter	Typical	Unit
Capacitance at -1.0 V	< 1.5	fF/µm^2
Capacitance at 0.0 V	< 3.0	fF/µm^2
Capacitance at +1.0 V	< 5	fF/µm^2

The table specifies the typical values obtainable for each parameter.

Section 3.2.7 describes the sheet resistance models that are used to construct the schematic and layout structures for resistors in the circuit design [65].

3.2.7 SHEET RESISTANCE MODEL

Rpoly2, *Rpolyh*, which is a high resistive poly, and *Rpolyb* resistors having a width of 1, 2, and 3 µm and different ratios of *W/L* is measured in straight line, meander type and segmented type of structures in order to extract a model as described in this section. The extracted model is valid in the following range, as given in Table 21.

Table 21. Validity of RPOLY models.

Parameter	Maximum range
Frequency range	Few kHz – 6 GHz
Width (drawn)	1 – 3 µm
Maximum length of *Rpoly2*	90 µm
Maximum length of *Rpolyh*	30 µm
Maximum length of *Rpolyb*	60 µm

Note that parameters of all three resistors are given in this table, and the chosen resistor for the proposed circuit in given in Section 4.1.4.

Layout structure

The layout structure is not defined here. The layout structure for the resistor used in this design is given in detail in Section 4.2.6. The exact value of resistance and amount of space available on the die determines the structure of the resistor.

Sub-circuit model

The sub-circuit model is given in Figure 30. From the model it should be noted that the *WELL* (n-well) terminal is connected to the substrate or to AC ground (e.g. V_{cc}). P_1 and P_2 are the two contact terminals of the resistor.

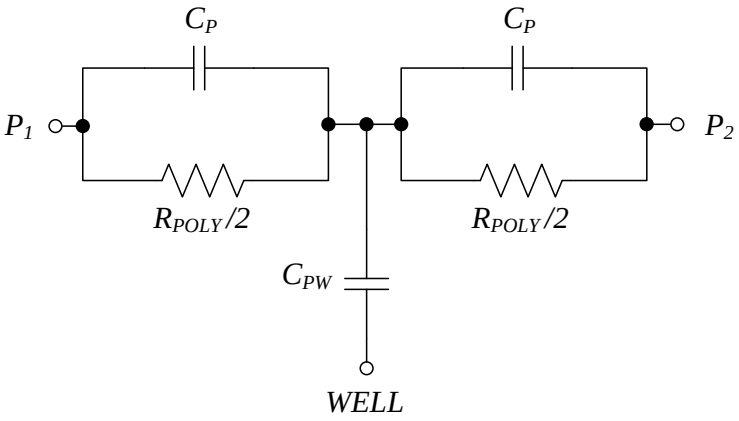

Figure 30. RPOLY sub-circuit SPICE model.

Table 22 describes the parameters of the RPOLY sub-circuit model as shown in Figure 30. These parameters are used to determine the parasitic effects due to high-frequency operation.

Table 22. RPOLY model parameters with reference to Figure 30.

Parameter	Parameter description
R_{POLY}	Poly resistance of resistor
C_P	Stray capacitance
C_{PW}	Poly-well capacitance

Information parameters

Important parameters of the RPOLY are given in this section. These parameters represent the actual resistances that can be achieved per square. For the proposed design, *Rpoly2* was used due to the resistance required in the circuit, as specified in Section 4.2.6, therefore the parameters of *Rpoly2* only are given in Table 23.

Table 23. RPOLY (*Rpoly2*) information parameters.

Parameter (RPOLY)	Typical	Unit
Sheet resistance	≈ 50	Ω/□
Effective width (0.65 µm)	< 0.50	µm
Sheet resistance temperature coefficient	< 0.6	10^{-3}/K

The table specifies typical values obtainable for each parameter.

The ability to implement the parameters given in Section 3.2 using computer aided design (CAD) software is an important aspect. The software forms an intricate role in the design, and needs to be able to use all parasitic modelling accurately in order to ensure good simulation results, which correspond well to measured results of the prototype. The software used for the proposed VCO is described in Section 3.3.

3.3 SIMULATION (CAD) SOFTWARE

The ultimate soundness and validity of the proposed hypothesis will be based on an intuitive approach. The simulation software aids in finding the perfect balance of operating frequency versus phase noise, taking into account other aspects like tuning range and parasitic interference. The simulation software therefore acts as a first source for determining if the design conforms to specifications. Prototyping of the VCO on-chip will evaluate the soundness and accuracy of the simulations, leading to the truthfulness of the hypothesis. A convincing (and finally cogent) prototype will depend on the integrity of these characteristics.

Sections 3.3.1 and 3.3.2 provide an overview of the software used for the schematic and layout simulations of the proposed VCO. Cadence® Virtuoso® (used as a schematic editor), and Tanner Tools® L-Edit® (used as a layout editor) are briefly discussed below.

3.3.1 SIMULATION SOFTWARE – CADENCE® VIRTUOSO®

Cadence® enables global electronic design innovation and plays an essential role in the creation of integrated circuits and electronics. Cadence® software and hardware, methodologies, and services are used to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. Cadence® reported 2008 revenues of approximately $1.039 billion (R7.8 billion), and has approximately 4,900 employees. The company is headquartered in San Jose, California, with sales offices, design centers, and research facilities around the world to serve the global

electronics industry. More information about the company, its products, and services is available at [61].

The Cadence® Virtuoso® Spectre® SPICE engine was used for the schematic design of the VCO. Cadence® Virtuoso® Spectre® Circuit Simulator provides fast, accurate SPICE-level simulation for RF and mixed-signal circuits. Reasons for using Cadence® as a schematic editor includes,

- the high-performance, high-capacity SPICE-level analogue and RF simulation with precision tuning for accuracy and convergence,
- enabling of accurate and efficient post-layout simulation with RLCK parasitics, S-Parameter models (n-port), and lossy coupled transmission lines (mtline),
- fast interactive simulation set-up, cross-probing, visualization, and post-processing of simulation results through tight integration with Virtuoso® Analogue Design Environment (ADE).

Figure 31 [61] summarizes the abilities of the Virtuoso® simulation engine. For the proposed design, RF implementation using the Spectre® engine is implemented. Spectre®, UltraSim®, and the Accelerated Parallel Simulator (APS) all have analogue- and mixed-signal (AMS) capabilities. *Figure 31 is adapted from [61]*.

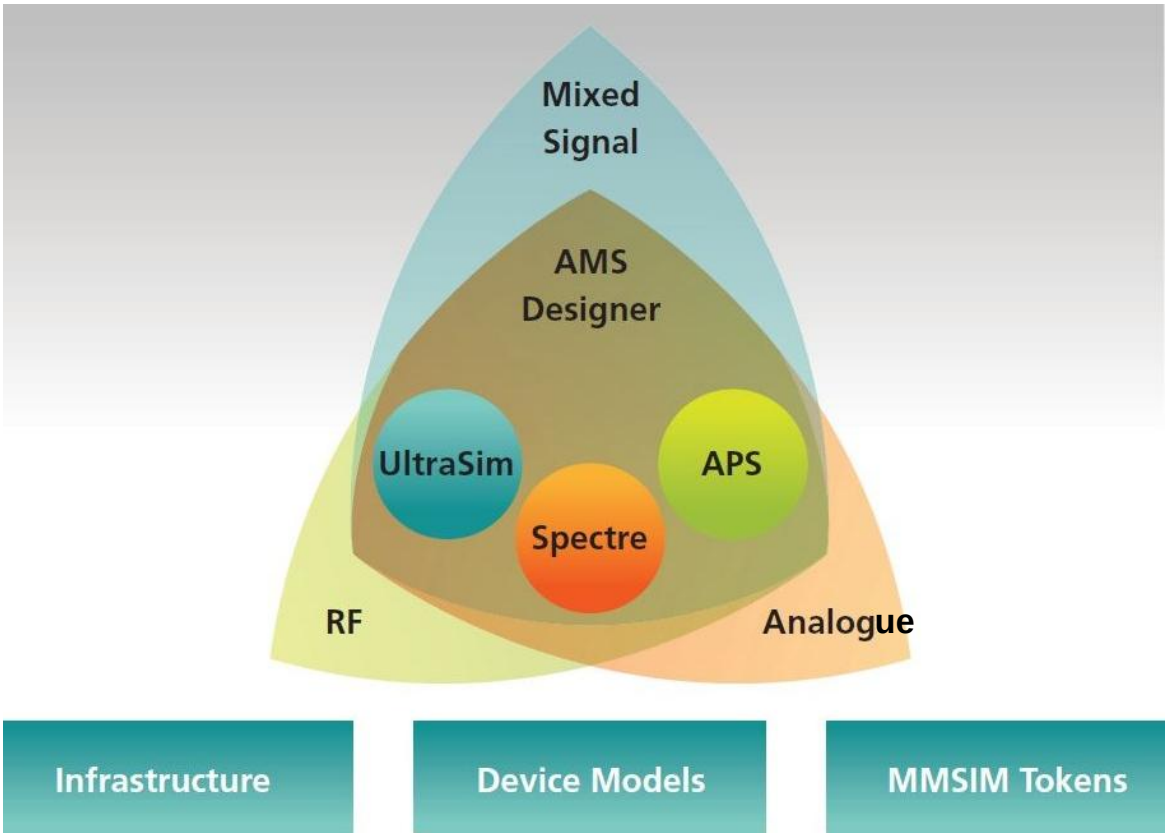

Figure 31. Cadence® Virtuoso® summary of simulator abilities.

From Figure 31 it can clearly be seen where the schematic simulations of the RF VCO can be carried out using the Cadence® Virtuoso® Spectre® schematic editor engine.

The layout editor (Tanner Tools® L-Edit®) is briefly discussed in the following section.

3.3.2 SIMULATION SOFTWARE – TANNER TOOLS® L-EDIT®

Tanner Tools® is supplied by IC design tools specialist, Tanner EDA®. "Tanner EDA® provides electronic design automation software used by companies in a wide variety of industries. Its solutions enable designers to move rapidly from concept to silicon by enabling the design, layout, and verification of analogue / mixed-signal ICs, ASICs, and MEMS" [62].

Tanner EDA® solutions include tools for:

- Schematic Capture: S-Edit
- Simulation: T-Spice, W-Edit
- *Physical Layout: L-Edit*
- Verification: HiPer Verify, *L-Edit Standard DRC*, L-Edit LVS
- Parasitic Layout Extraction: HiPer PX, 2D and 3D parasitic layout extraction

The L-Edit® *Layout Editor* used in this design gives designers complete control over all their layout operations. An easy-to-use, intuitive interface lets users begin designing immediately, without a steep learning curve or extended setup. With L-Edit®, it is possible to increase the drawing speed by using its powerful editing tools such as object snapping, one-click horizontal or vertical alignment, and base point. Performing complex Boolean and derived layer operations with arbitrary polygonal curves and shapes are made easy and the use of external GDSII cell libraries ensures a smooth design flow. The L-Edit® Interactive design rule check (DRC) makes corrections as errors occur, displays DRC violations in real-time and lets the designer fix the errors while editing the layout [62].

3.4 IC PROTOTYPING

The IC was prototyped by AMS, using their S35D4M5 SiGe BiCMOS Process Technology as specified in [63]. The design was first sent to Europractice ASIC Prototyping (MPW runs). After all DRC errors picked up on the design (described in Appendix B) were corrected, the design could be submitted for prototyping by AMS. AMS provides application notes at [63] for the S35D4M5 SiGe BiCMOS Process Technology where some important characteristics are specified below:

- Transceivers for: 868 MHz, 915 MHz, 2.4 GHz, 5.6 GHz
- Clock recovery circuits up to 10 GHz
- S35D4M2 4P/4M SiGe BiCMOS mixed-signal, RF, PIP+MIM, thick metal
- Feature Sizes: 0.35 µm gates / 0.40 µm emitters
- Supply Voltage: CMOS 3.3 V
- f_T > 60 GHz, f_{max} > 70 GHz
- BV_{CEo} > 2 V

AMS SiGe BiCMOS process is based on the proven 0.35 µm mixed-signal CMOS process and includes an additional high performance analogue oriented SiGe HBT transistor module. This advanced RF process offers high-speed HBTs with excellent analogue performance such as high f_{max} and low noise as well as CMOS transistors with the option of 5V I/O CMOS transistors. Accurately modelled high linear precision capacitors are available as *Poly1* / *Poly2* or *Metal2* / *Metal3* versions. The modular integration of linear resistors, high quality varactors and thick *Metal4* spiral inductors makes this process ideally suitable for a wide range of high performance RF applications up to 20 Gb/s [63].

3.5 PROTOTYPE ENCAPSULATION

Several options exist for encapsulating microelectronic ICs to use it on hole-mounted printed circuit boards (PCBs). From older technologies like the dual in-line package (DIP) which is sometimes referred to as a DIL package, to its successor, the small-outline integrated circuit (SOIC), which is a surface-mounted integrated circuit occupying about 30 – 50 % less area than its DIP predecessor. Although DIPs are still used today regardless of being succeeded by SOIC, it is generally used for lower speed circuits (up to about 20 MHz) and not for high-speed RF circuitry. SOIC packages present better frequency characteristics than DIPs, but are still not ideal for RF operation. Another option to be considered is quad flat no leads (QFN) packages. QFN packages are also surface mount technology, similar to quad flat packages, but the leads do not extend from the sides of the package. QFN packages come in two types; air-cavity QFN and plastic-moulded QFN. However, the plastic-moulded QFN is only rated to about 3 GHz, whereas air-cavity QFN is rated up to 25 GHz. A big advantage to QFN packages (the main advantage taken into consideration when deciding to choose this package as the package for the 5 GHz VCO) is the fact that due to the ground leads of the package not extending out the sides of the package and rather extend only to the bottom of the package, lead inductance is significantly reduced. The bottom of the entire package is considered as its ground, and thermal conductivity is also improved with this method. Figure 32 shows a picture of a QFN-56 package, where the ground plane can be seen on the picture to the right. The ground leads of the designed IC are lead to this plane, shortening overall lead length and decreasing lead inductance.

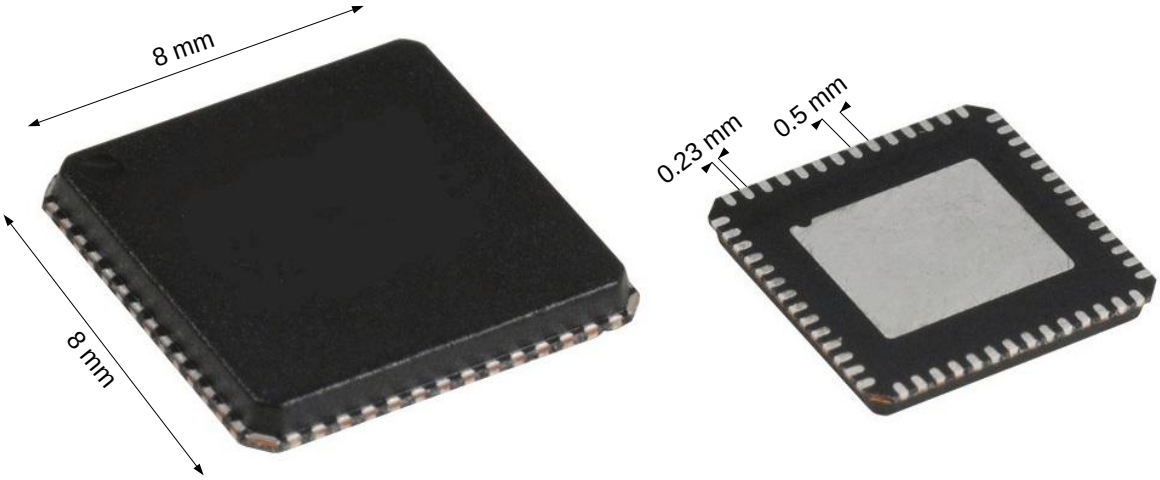

Figure 32. Photo of QFN-56 package showing bottom grounded plane.

When packaging is complete, the IC can be mounted on a PCB for easier access to inputs and outputs. The design of the PCB is another step toward finalizing and measuring the VCO without adding noise. The design procedures are discussed in Section 3.6.

3.6 PCB TEST CIRCUIT

The design of the PCB test circuit was done by a third party. Input was given to the party to ensure that the design of the PCB, which aided in measuring the results of the IC and compare these results to the theoretical (and simulated) hypothesis, was done to specifications important to the researcher.

Two software packages were used. OrCAD® Capture® [66] was used to design the schematic representation (Figure 48) of the test PCB, where the IC was manually created, or drawn, and inserted in the schematic. Only the basic layout of the IC was drawn, with no interconnections between pins, thus no simulated results were obtained from this schematic.

For the layout of the PCB, Mentor® PADS® [67] was used. This software allows the designer to physically do the layout of all the tracks and connections required in the final circuit. The layout was done by comparing each track with the schematic design, and ensuring all components are connected in the correct way. Refer to Appendix A for silkscreen layout, soldermask layout, and drill drawing of the test circuit.

Finally, all components were soldered on the PCB (including the IC), and the measurements could be done. Test points were added throughout the circuit to aid the testing procedure, and determine important currents flowing in the circuit. The schematic and layout designs are given in Section 4.3.

3.7 MEASURING EQUIPMENT

The Rohde and Schwarz® [70] range of spectrum analyzers present good dynamic range, phase noise, level accuracy, and resolution bandwidth. The Rohde and Schwarz® FSU8® 8 GHz spectrum analyzer was used to perform various measurements on the IC prototype of the integrated VCO created to prove the hypothesis of tail-current shaping on phase noise performance on a more practical level compared to simulation results only (see Chapter 5). These measurements were carefully obtained and accuracy of the measurements was of utmost importance to avoid. The FSU8® spectrum analyzer provides this level of performance, and some of the main characteristics are given below.

- Frequency range from as low as 20 Hz up to 8 GHz
- Displayed average noise level of -158 dBm in a 1 Hz bandwidth
- Typical SSB phase noise of -123 dBc at a 10 kHz offset in a 1 Hz bandwidth
- Typical third order intercept (TOI) of +25 dBm
- Resolution bandwidth of 1 Hz up to 50 MHz
- 2.5 ms sweep time in the frequency domain; 1 µs in the time domain

Phase noise and output power measurements were taken on this spectrum analyzer and these results are displayed in Chapter 5.

3.8 MEASUREMENT SETUP

To ensure accuracy of measured results, the measurement setup was important. This setup aims to improve the integrity of the results. The device under test (DUT) (see Figure 70 for a photograph) was connected to the spectrum analyzer as shown in Figure 33.

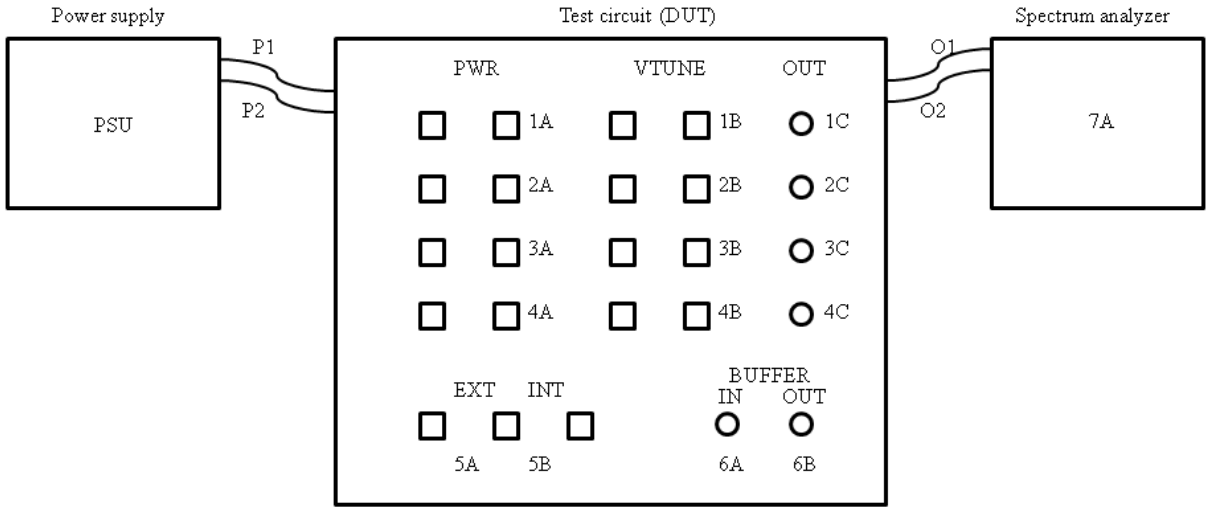

Figure 33. Presentation of measurement setup.

The procedure for taking measurements of the IC on the test circuit is outlined here. The power supply unit (PSU) is connected to the test circuit's main power connectors, P1 and P2. For each VCO (of the four that could be measured and compared – see Section 5.3 for a breakdown of each VCO configuration), a separate power source was supplied, which was redirected from the main source. Each of these sources could be activated by using jumpers 1A – 4A. In conjunction with the source jumpers, each VCO also had a separate voltage tuning ability. The selected VCO also needed to be tuned by its specific tuning source, and is selected with jumpers 1B – 4B. The decision whether internal (via variable resistor) or external (via external power supply) tuning were to be done, could be made at any time through jumpers 5A and 5B. The outputs of the VCOs (1C – 4C) could either be directly connected to the spectrum analyzer (7A – see Section 3.7) using O1 and O2, or the outputs could be passed through a buffer circuit by first connecting the VCO output to 6A, and then connecting the buffer output (6B) to the spectrum analyzer (7A).

3.9 CONCLUSION

Chapter 3 includes the methodology for completion of this dissertation. The methods for designing, simulating, and prototyping the proposed circuit was discussed. These methods aim to prove and justify the theoretical hypothesis, with reference to the different software packages used during each of these stages. Chapter 4 is dedicated to the schematic and layout design of the proposed VCO.

CHAPTER 4: CIRCUIT DESIGN

4 INTRODUCTION

Chapter 4 is dedicated to a discussion of how the full VCO circuit schematic, layout, and PCB design was approached. The chapter deals with the design choices made in terms of which components was used for each section of the full circuit, with motivations why these components were chosen, referring back to Chapter 3 which gives all of the available choices for the components and their respective characteristics. Choosing the correct component to minimize phase noise is important in this design, and therefore some trade-offs had to be made; for instance tuning range is limited (see choice of varactor). The chapter is divided into two sections. The first section describes the schematic design, with accompanied equations, whereas the second part describes the layout design of the circuit. Importantly, there are no simulation results in this chapter, as the results are only given in Chapter 5, accompanied by measured results for comparison purposes. Therefore the values obtained in this chapter are acquired mathematically, and fine adjustments to these values are only made once simulations were run in Cadence® Virtuoso®. The adjustments are purely based on a performance review of the simulation results when differing component values and / or dimensions, to find better overall phase noise performance.

4.1 CIRCUIT DESIGN (SCHEMATIC)

The first criterion to be met is the design of the oscillating frequency (5 GHz) by choosing values for the inductor and capacitors in the LC tank circuit. By choosing these values, and keeping in mind how these choices influence noise performances, the tank circuit can be designed to operate at the correct frequency, whilst maintaining good noise performance, fair tuning range, and low power consumption. Section 4.1.1 describes the process of designing the LC tank.

4.1.1 LC TANK DESIGN

The design of the LC tank is one of the most important design aspects of the entire circuit. The tank contributes largely to the total amount of phase noise introduced into the circuit, mainly due to the limiting *Q*-factor of the inductor in the tank circuit. The tank circuit is also

responsible for the frequency at which the circuit oscillates, through the following equation [23] (repeated (33) from Section 2.5.1).

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{48}$$

where f_0 = 5 GHz. The inductor that was chosen stems from the fact that this inductor has a slightly larger inductance than that of the model just before it, which is the first model supplied, but has a good *Q*-factor compared to the models that follow this inductor (refer to Table 8 for a list of available inductors). The inductor has a *Q*-factor of around 11 with an inductance of around 1.5 nH at 5 GHz, presenting a suitable balance between inductance and quality. The choice of the inductor is thus purely based on its *Q*-factor, with some consideration for its inductance to control the size of the capacitance needed, and the capacitance is then manipulated to achieve the oscillation frequency. Therefore, the capacitance is calculated to be (together with the inductor to achieve 5 GHz oscillation)

$$\begin{aligned} C &= \frac{1}{(2\pi f_0)^2 L} \\ &= 641.273 \text{ fF}. \end{aligned} \tag{49}$$

Thus, a capacitance of 641.273 fF is needed to achieve an operating frequency of 5 GHz. The metal-metal (CMIM, see Section 3.2.4) capacitor provided is a good choice due to its almost constant capacitance through the frequency spectrum [65] (see Figure 34 on the following page).

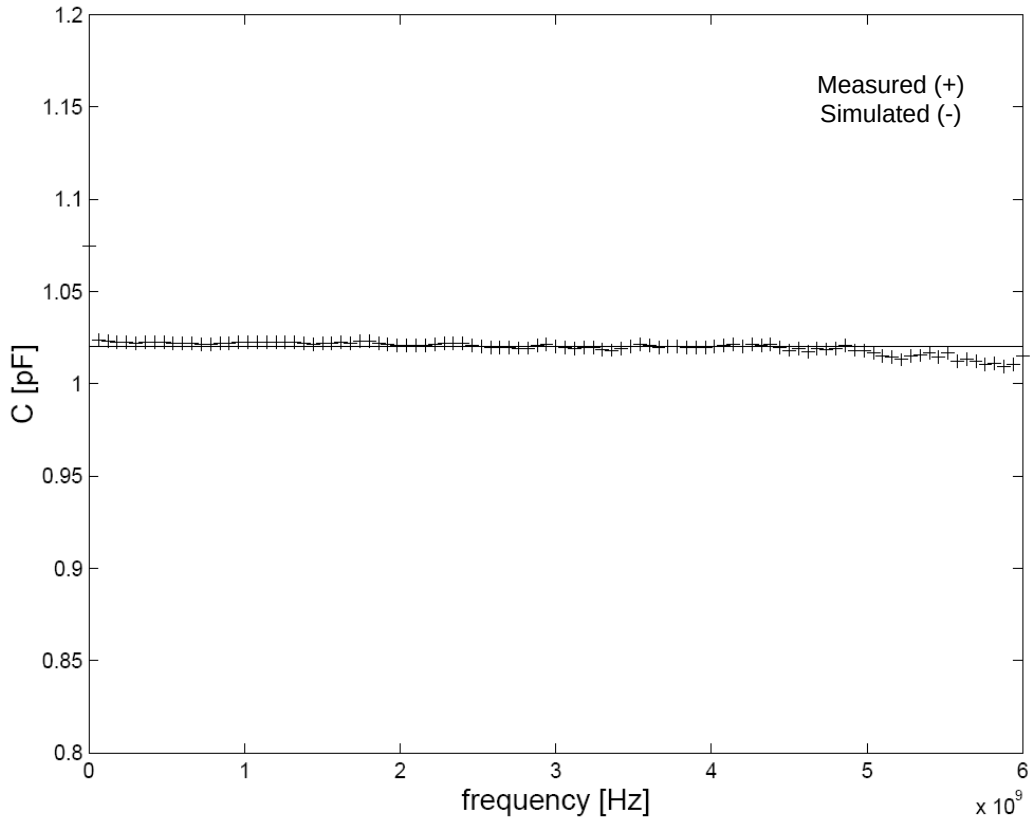

Figure 34. Measured and simulated capacitance versus frequency for CMIM.

However, the main consideration that makes this capacitor a good choice (compared to the *poly1-poly2* (CPOLY) capacitor) is the fact that the CMIM capacitor has no parasitic resistance between its bottom plate and its well (see Section 3.2.4). As a result of this, the CMIM capacitor presents better quality factors than its CPOLY counterpart due to less resistive losses internally. Although its range is limited compared to CPOLY (0.1 pF – 1 pF compared to CPOLY having a range of 0.1 pF – 5 pF), the size of this capacitor needed to achieve the oscillating frequency falls well within this range and is therefore not a concern. After several mathematical iterations, it was decided to make use of CMIM capacitors with an area of 10 x 10 μm^2 (width and length), resulting in an overall area of 100 μm^2. In order to achieve a total capacitance of 641.273 fF, a total amount of

$$= 641.273 \times 10^{-15} / 129.56 \times 10^{-15}$$
$$= 4.949 \approx 5$$

capacitors were needed (in parallel combination). Thus the tank circuit, in summary, consists of 5 CMIM capacitors of area 100 μm^2 each, in parallel, together with an inductor to achieve the oscillating frequency of 5 GHz with highest possible overall *Q*-factor.

The amplitude of the output voltage (and hence the gain of the oscillator) is an important characteristic to design for when designing a low phase noise oscillator. The oscillator is seen as a basic amplifier, with positive feedback. The gain of this amplifier should not be high as to increase (amplify) intrinsic device noise in the active devices (see Section 1.2). A decision to design the amplifier with lowest possible gain was therefore made to complement this theory and achieve low noise. The gain of the amplifier circuit was arbitrarily chosen to be 1 (or 0 dB). The gain (G) of the oscillator, which is in essence a common emitter amplifier, can be proven to be [21]

$$G = -g_m Z_{eq} \tag{50}$$

where g_m is the transconductance of the transistor, and Z_{eq} is the equivalent impedance as seen from the collector of the transistor. From first principles, the equivalent impedance at the collector can be written as

$$Z_{eq} = Z_C \parallel Z_L \parallel r_o \tag{51}$$

where Z_C represents the real impedance presented by the capacitor in the tank circuit, Z_L represents the real impedance of the inductor, and r_o is the output impedance of the transistor as seen from the collector. For now, the impedance r_o will be assumed much larger than the factors Z_C and Z_L, and can therefore be omitted from this equation. This assumption will be verified later. Thus, (51) can be rewritten as

$$\begin{aligned} Z_{eq} &= Z_C \parallel Z_L \\ &= \frac{1}{2\pi f_0 C} \parallel 2\pi f_0 L \end{aligned} \tag{52}$$

where C and L represent the capacitance and inductance values of the tank circuit respectively. It is now possible to compute the transconductance, and hence the collector current of the circuit, by following the next couple of steps.

$$\begin{aligned} G &= -g_m Z_{eq} \\ &= -g_m \frac{1}{2\pi f_0 C} \parallel 2\pi f_0 L \\ &= -g_m \frac{1}{2\pi \times 5 \times 10^9 \times 641.273 \times 10^{-15}} \parallel 2\pi \times 5 \times 10^9 \times 1.58 \times 10^{-9} \\ \therefore 1 &= -g_m \times 24.82 \\ \therefore |-g_m| &= \frac{1}{24.82} \\ g_m &= 40.29 \text{ mS}. \end{aligned}$$

Thus, the transconductance is equal to 40.29 mS. From this, the collector current can be equated. The equation used to achieve this is (where V_T is the thermal voltage of 26 mV)

$$\begin{aligned} I_{BIAS} &= g_m \times V_T \\ &= 40.29 \times 10^{-3} \times 26 \times 10^{-3} \\ &= 1.047 \text{ mA}. \end{aligned} \tag{53}$$

Thus, a steady DC bias current of around 1 mA is needed to achieve the gain specification. To prove the assumption for the transistor output impedance was correct, (54) is presented [21].

$$r_o = \frac{V_A}{I_{BIAS}} \tag{54}$$

where V_A is the transistor Early voltage (see Section 3.2.1). This equation results in a impedance of 95.51 kΩ, which is in fact much larger than Z_C (around 50 Ω) and Z_L (also around 50 Ω).

It is now also possible to compute the output voltage of the oscillator under normal operating conditions. To do this, the following equation is presented for the peak output voltage (A) of a LC configured differential oscillator [23]

$$A = \frac{2}{\pi} I_{BIAS} R_p \tag{55}$$

where R_p is the parallel resistance of the inductor, and I_{BIAS} is the total current supplied by the current source. From [23], in order to compute R_p, (56) is adapted from (37):

$$R_p = 2\pi f_0 L Q_0 \tag{56}$$

where Q_0 is the unloaded Q-factor of the inductor, L is the inductance of the inductor, and f_0 is the frequency of operation (5 GHz). Thus

$$R_p = 506.299\ \Omega$$

Rewriting (55), and having equated the parameter R_p, the voltage amplitude can be found by

$$\begin{aligned} A &= \frac{2}{\pi} I_{BIAS} R_p \\ &= 337.47\ \text{mV} \end{aligned}$$

The expected output voltage has a peak-to-peak value of 337.47 mV if the oscillator amplifier gain is limited to 0 dB.

And the bandwidth of the circuit (38) can be calculated (which will be simulated and measured and the results confirmed in Chapter 5) and is given by [23]

$$\begin{aligned} BW = \Delta f &= \frac{f_0}{Q_0} \\ &= 490.2\ \text{MHz}. \end{aligned} \tag{57}$$

Note that this equation assumes that the loaded Q and unloaded Q are the same, which will in fact not be the case. However, the loaded Q is expected to be relatively close to the unloaded Q, therefore this should give a good first estimate of the overall bandwidth.

The tuning range of the circuit is determined by the C_{max}/C_{min} ratio of the varactor in the tank circuit. A high ratio means that it is possible to use a higher inductance value, but with a

lower *Q*-factor, hence decreasing the overall phase noise performance, but enhancing the tuning range. For low phase noise operation however, a lower ratio is needed. The varactor models provided by AMS have almost constant C_{max}/C_{min} ratios, therefore the smallest model was chosen to reduce total size on chip. Again, two choices of varactors exist from AMS, the junction varactor model (JVAR), and the MOS varactor model (CVAR). The final choice stems from the fact that the MOS varactor can achieve its maximum *Q*-factor at a biased voltage of around 1 V, whereas the junction varactor reaches its maximum *Q*-factor at a bias voltage of larger than 3 V. Thus voltage correlates to the tuning voltage supplied to the circuit, and a lower tuning voltage will offer lower power consumption whilst maintaining maximum quality factor (added to the *Q*-factor of the overall tank circuit). The characteristic *Q*-factor curves are presented in Figure 35 below [65].

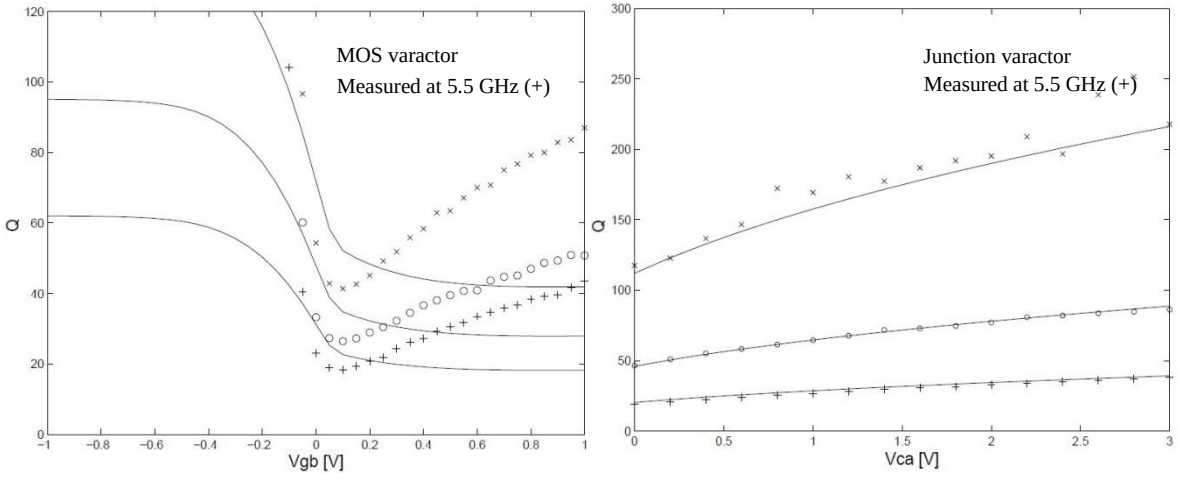

Figure 35. *Q*-factor characteristics for MOS varactor and junction varactor.

It can be seen from Figure 35 that the MOS varactor achieves its maximum *Q*-factor of about 41 at about 1 V applied to its gate-bulk contact, whereas the junction varactor achieves its maximum of about 40 as well at about 3 V applied to its anode and cathode. From Section 3.2.6, CVAR with a width of 158.4 µm and a length of 0.65 µm (fixed) is chosen. The resulting in a C_{max}/C_{min} ratio of about 4 and a capacitance tuning range of around 60 %. The tuning range of the circuit is given through the simulation results in Chapter 5. A current source able to supply a bias current of 1.047 mA is designed and described in Section 4.1.2.

4.1.2 CURRENT SOURCE DESIGN

For the current source, a simple current mirror is employed to minimize the amount of components used that generate noise. The circuit diagram of the current mirror is given

below. Note that the reference current (I_{REF}) is replaced by a single resistor responsible for supplying the current to the mirror circuit. The value of this resistor is also calculated in this section.

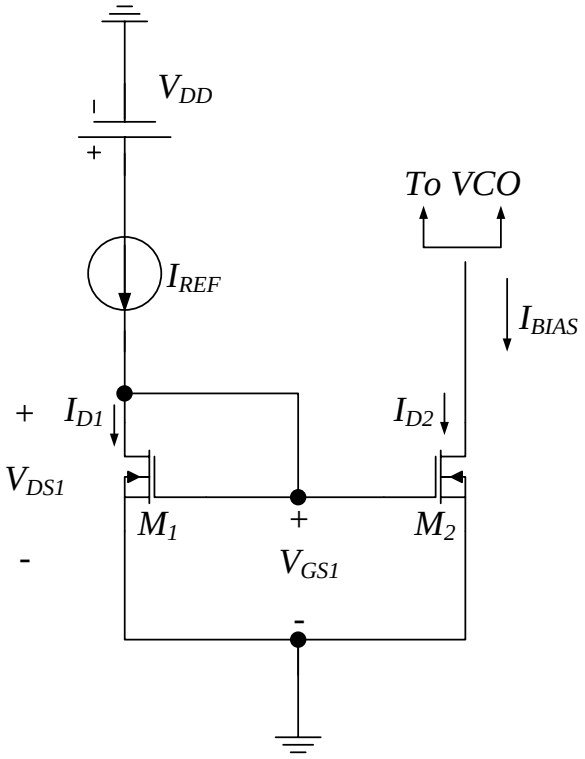

Figure 36. Circuit diagram of current source used in VCO design.

From this figure, I_{OUT} = 1.047 mA. This current passes through the drain of M_2 and is given by (58) [21],

$$I_{D2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH})^2(1 + \gamma V_{DS2}) \tag{58}$$

where μ_n is the effective mobility of the NMOS transistor, C_{ox} is the gate-oxide capacitance of the transistor, $\left(\frac{W}{L}\right)$ is the aspect ratio of the transistor (arbitrarily chosen as 40, with L = 0.5 µm and W = 20 µm), V_{GS} is the gate-source voltage of the transistor, V_{TH} is the threshold voltage, γ is the channel-length modulation parameter (assumed to be 0), and V_{DS2} is the drain-source voltage of the transistor. Thus, from (58), when assuming the channel-length modulation parameter to be zero for long channel analysis [21],

$$V_{GS2} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} + V_{TH} \tag{59}$$
$$= 1.018 \text{ V}.$$

But, from Figure 36, $V_{GS2} = V_{GS1} = V_{DS1}$. Thus R is determined by

$$R = \frac{V_{DD} - V_{DS1}}{I_{REF}} \tag{60}$$
$$= 2.179 \text{ k}\Omega.$$

Thus, as a first iteration, and without bearing in mind the phase noise operation of the current source and without the use of tail-current suppression, these values were used to create a current source (with current mirror) able to supply the 1.047 mA current needed. These values are however altered later on, to achieve the same current but while manipulating the dimensions of the MOS transistor, and noting its effects on noise performance, to achieve the best possible phase noise performance even before the tail-current shaping circuitry. The tail-current shaping circuit design is discussed in Section 4.1.3.

4.1.3 TAIL-CURRENT SUPPRESSION CIRCUIT DESIGN

Section 2.6 describes the tail-current shaping technique with a theoretical approach. From this discussion, it is evident that the tail-current adds large noise components especially at odd harmonics, with the second harmonic having the largest effect. Therefore, it was decided to design the tail-current shaping circuit, as a filter tuned to the second harmonic of the circuit (twice the oscillating frequency). The circuit entails the addition of a capacitor and an inductor at the current source, connected as shown in Figure 37.

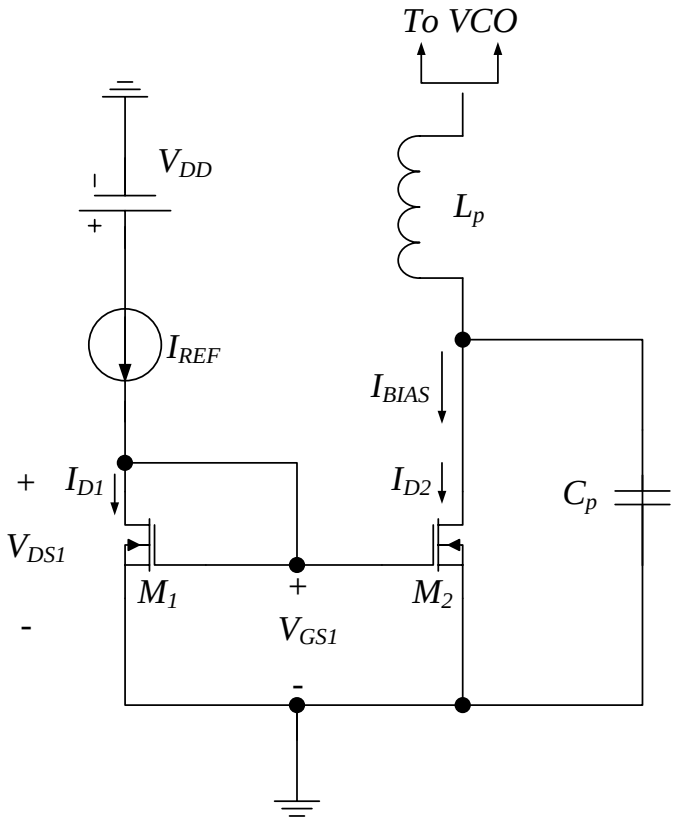

Figure 37. Current source with tail-current shaping circuit connected.

The capacitor C_p creates a small reactance path at the second harmonic, effectively shorting the noise effects at $2f_0$ to ground. The placement of L_p between the current source and the differential pair of the VCO increases the impedance path from the switching transistors towards the current source at the centre frequency. Thus, choosing an inductor with a large inductance, and hence a large impedance will benefit this operation.

From (45), the capacitor (C_p) can be equated as

$$C_p = \frac{2I_{BIAS}}{2A_s\omega_0}$$
$$= 12.818 \text{ fF}$$

Note that the value for A_s is assumed to be 2.6 V which is the assumed transistor base-emitter voltage (0.7 V) subtracted from the supply voltage (3.3 V). Thus a value of about 13 fF is needed to short current signals at $2f_0$ to ground. The same capacitor dimension that was used

to design the tank circuit is used in this section. Therefore, connecting seven capacitors in series achieves a total capacitance of about 18.508 fF.

This value of 18.508 fF is assumed to be close enough to the specified value, as there was seen in simulation results that a tolerance in this value does not have large effects on the overall performance.

Now in order to filter the components falling outside of the frequency band of interest, the inductor (L_p) should be chosen. Regarding (C_p), and (46), the value is found to be

$$\begin{aligned} L_p &= \frac{1}{C_p(4\pi f_0)^2} \\ &= \frac{1}{12.818\times10^{-15}(4\pi\times5\times10^9)^2} \\ &= 19.761 \text{ nH} \end{aligned}$$

Thus, and inductor of around 20 nH is needed. The chosen inductor has a large inductance of 19.23 nH with a quality factor of below 1.5 at 5 GHz. Simulation results confirmed that the *Q*-factor of this inductor does not have a negative effect on the *Q*-factor of the tank or overall circuit. Following (47),

$$Z_{L_p} = 2\pi f_0 L_p$$

the impedance for the low-frequency noise created by the inductor is 604.13 Ω.
The simulation results in Chapter 5 confirm that this filter circuit does in fact have considerable effect on the overall phase noise of the circuit.

4.1.4 OUTPUT BUFFER DESIGN

An output buffer is connected to the VCO to minimize the effect of external voltages and parasitic effects when physically measuring the output of the VCO. The output buffer should ideally add no noise components to the overall circuit performance. The design of the output buffer is rather simple (again to limit the amount of components used that generate noise in the overall circuit). The buffer can be either connected to the output of the VCO, or if the noise performance without the buffer is to be measured, it can also be disconnected from the circuit.

The buffer circuit consists of SiGe HBTs (instead of MOS transistors which suffer from slower switching time, and could affect the circuits noise performance) connected as shown in Figure 38. The figure on the left in Figure 38 is the proposed design for the output buffer. It is a simple Class-E amplifier, with tuned circuit (to 5 GHz) on the collector of transistor T_1. This allows only signals in the 5 GHz range to be amplified to the final output of the circuit. However; two problems occurred when designing a Class-E output stage for the VCO. The first problem is a general layout problem, and the fact that an extra inductor is used, which uses up a large amount of space on the die, presented a problem as the total area on the chip had already been used up to this point. Another problem is the fact that the tuned circuit is tuned to a specific frequency (5 GHz). The VCO does in fact have a tuning range, thus the output of the VCO is not always exactly 5 GHz, depending on the value of the tuning voltage. Therefore whenever the VCO is set to a frequency different from 5 GHz, the output might be attenuated severely, and this would not be ideal. Also, the added components (especially the inductor) might degrade phase noise performance by adding noise components to the output. The output buffer was therefore reduced to the figure on the right in Figure 38. Although the chosen topology for the output buffer exhibits low levels of distortion to the output signal, which is important as this can add to the phase noise of the device, the buffer has a very low efficiency. This trade-off leads to higher power consumption when the buffer is connected, and future works could investigate better performing output buffers. The bias current circuitry to supply I_{BIAS}, is the same current source used as the main current source of the VCO (see Section 4.1.2), with the same dimensions for the transistors, supplying a current of 1.047 mA.

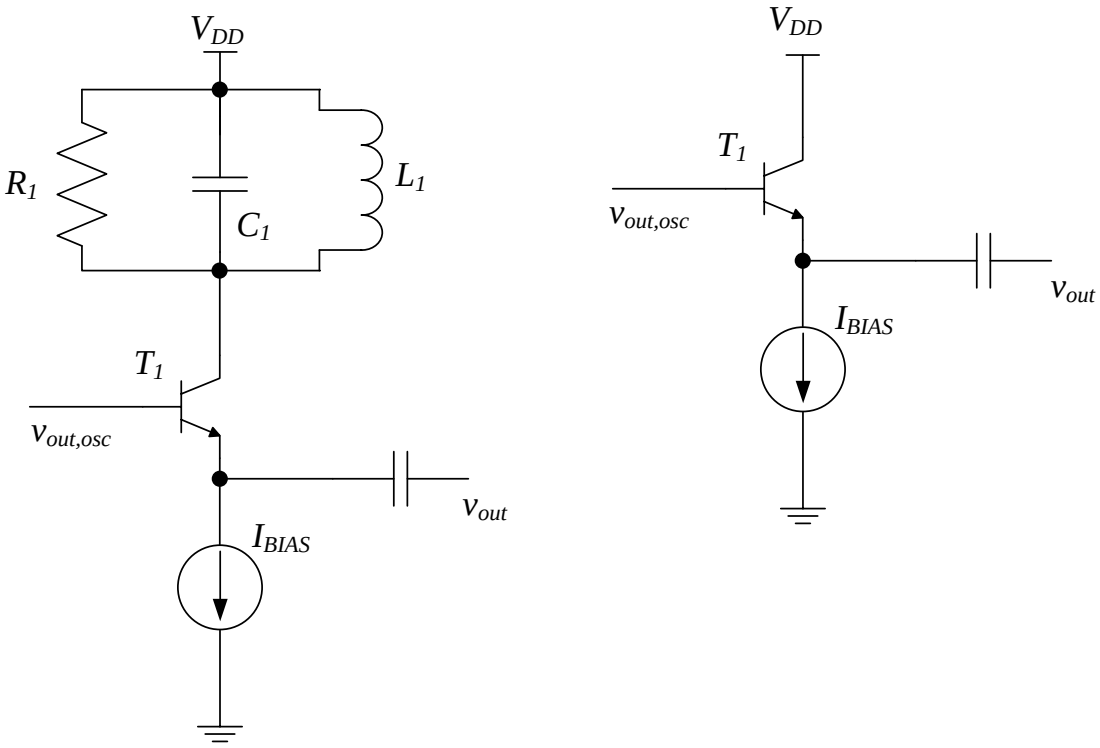

Figure 38. Proposed output buffer circuitry (left) and implemented circuit (right).

The design of the tuning circuit on the left of Figure 38 commenced in the same way as the oscillating frequency for the VCO was designed earlier. The same inductor together with a 641.273 fF CMIM capacitor was used to achieve the tuning frequency of 5 GHz. A 1 kΩ resistor is connected in parallel. The magnitude of the output voltage can be changed (increased) by increasing the size (area) of the emitter of the transistor. The default area (1 μm^2) was used for this design, as the output was still measured to be around 300 mV.

Chapter 5 shows some simulation results for the VCO output when the buffer circuit is connected (together with results if it is not connected) to show the overall effect of the circuit on the output.

The next step was to physically design the layout of the circuit. A discussion follows in Section 4.2.

4.2 CIRCUIT DESIGN (LAYOUT)

This section describes the design choices made during the layout of the VCO. These layouts are designed using the values obtained in Section 4.1. The final layout, thus the dimensions of

the components, might differ due to subtle changes made to some components during simulation runs, but the overall layout and structure of the circuit remains the same. Refer to Appendix B for the final layout of the VCO. Figure 39 represents the physical placement and hierarchical design for all materials used in the AMS BiCMOS S35D4M5 design process [64].

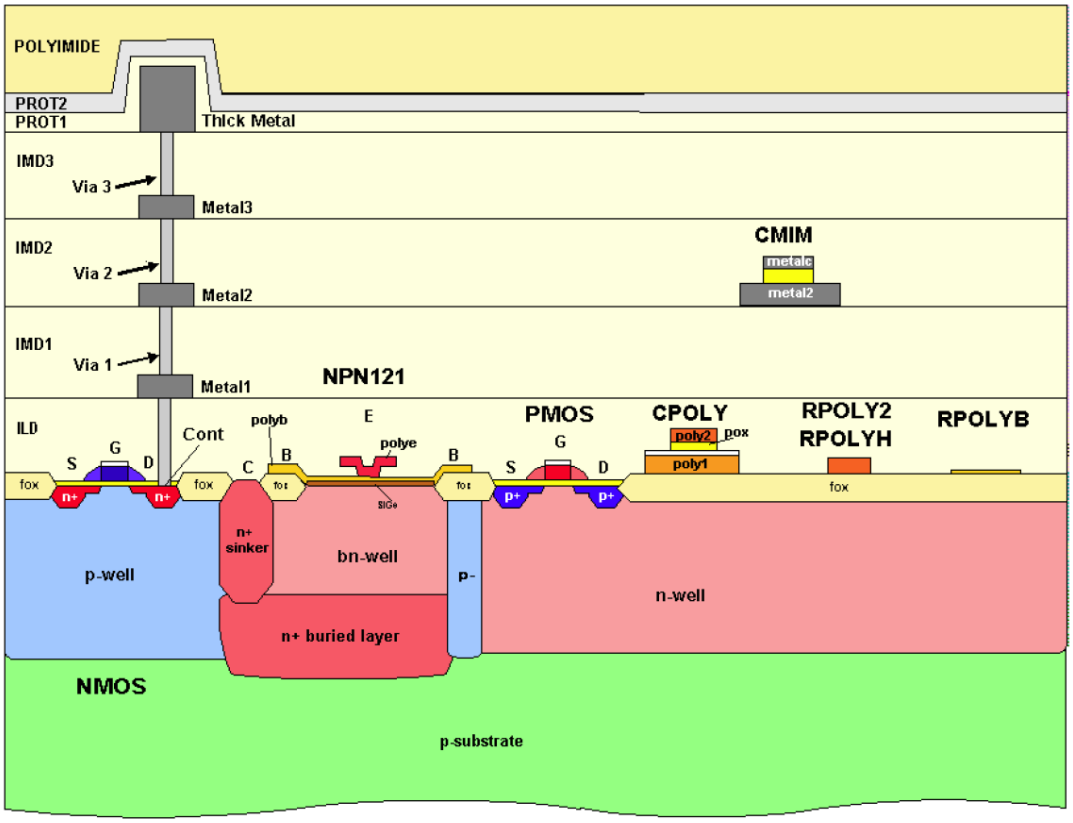

Figure 39. AMS 0.35 µm S35D4M5 wafer cross-section.

The wafer cross-section depicted in Figure 39 describes the process thickness parameters for the AMS process used. Note the height of the metal contacts, and how they are connected to each other using vias. This procedure is described later on in this section. Note that careful consideration for the process design rules [46] are implemented, as these rules define the minimum distances between adjacent materials in the layout design.

4.2.1 INDUCTOR LAYOUT

The layout of the thick metal inductors used (SP015S250T and SP100S250T), is supplied by AMS and cannot be altered. The characteristics and parasitic models are defined for the models provided by AMS, and as mentioned in Chapter 3, the standard inductor models are used in this design. These are spiral inductors, and for further information regarding the physical layout of a spiral inductor, refer to Section 2.5.2. The measured *Q*-factor and

inductance values of the two inductors used (in the tank circuit, and tail-current shaping filter) are given here for convenience.

Table 24. Thick metal inductor measured parameters used in design.

Inductor	Inductance [nH]			Q_{max}	Q		f_{res} [GHz]
	L_s	@ 2.4 GHz	@ 5.0 GHz		@ 2.4 GHz	@ 5.0 GHz	
SP015S250T Used in tank	≈ 1.5	≈ 1.5	≈ 1.5	≈ 11	≈ 10	≈ 10	> 6
SP100S250T Used in filter	≈ 10	≈ 12	≈ 19	≈ 7	≈ 7	≈ 1	> 6

Figure 40 depicts the layout used in Tanner® Tools L-Edit® for the inductors. Note that the inductor on the left has a much larger inductance and therefore has two more spiral turns in the physical layout. The losses induced in these extra turns account for the reduced Q-factor.

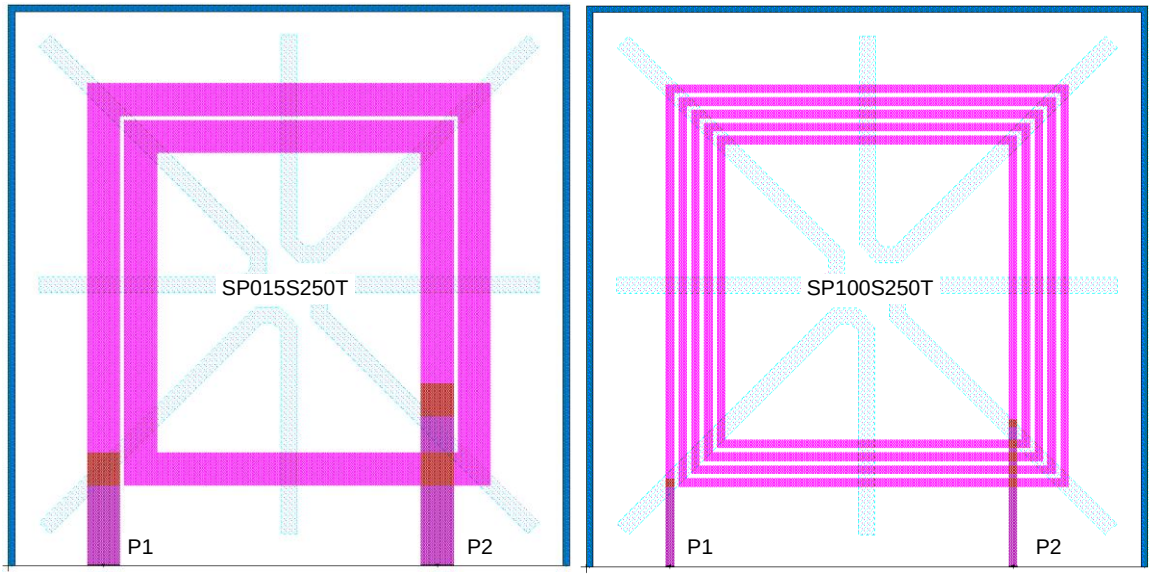

Figure 40. Inductor layout.

Also note the placement of the NTUB material (light blue 45^o angled materials in Figure 40) are included by AMS as default to reduce losses induced by the inductor due to *eddy* currents. The pink material is *metal4*. The layout of the capacitor (CMIM) is given in Section 4.2.2. A netlist of this component is not given in Appendix B, as Tanner® Tools® L-Edit® could not recognize this component as an inductor (this is an extraction limitation of L-Edit®), and the component was assumed correct as supplied (part of the design library) by AMS.

4.2.2 CAPACITOR (CMIM) LAYOUT

The metal-metal capacitor (CMIM) consists of two metal plates placed on top of each other with an insulator in between. Before attempting to explain the layout of the component, a figure of the device together with its cross-section obtained in L-Edit® is given in Figure 41.

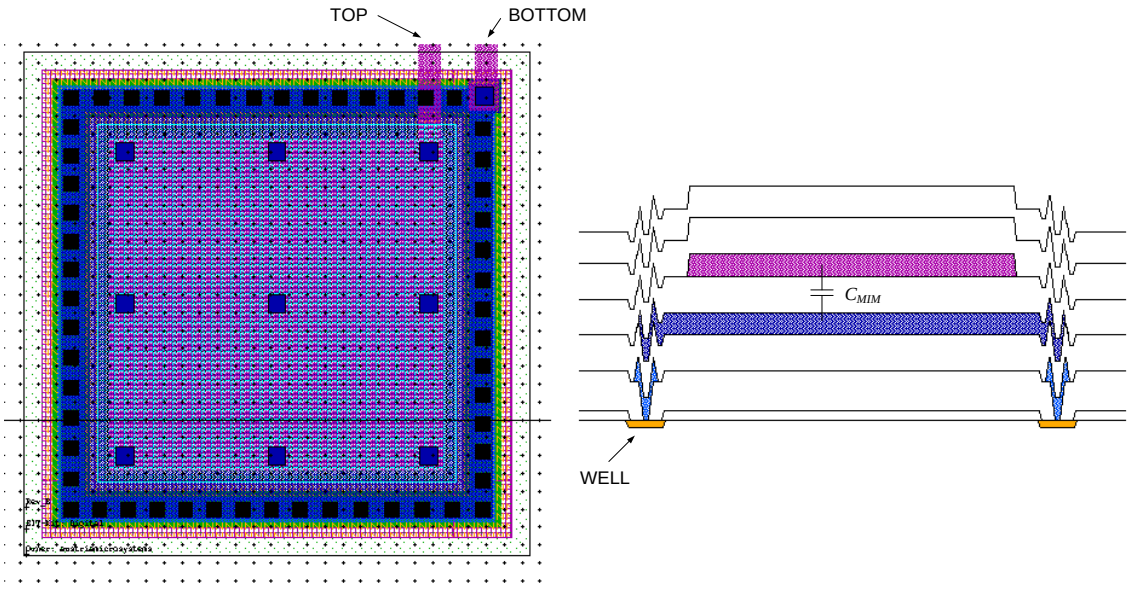

Figure 41. AMS 0.35 µm CMIM (left) and cross-section view (right).

For convenience, the cross-section view is placed on the right of the component and not below as done by L-Edit®. From the cross-section view in Figure 41, it is evident that there are two materials placed on top of each other (dark blue and purple materials). These materials represent the metals (dark blue is *metal2* and purple being *metal3*), which make up the two conducting plates of a capacitor. A third material, called METCAP, is placed between the two metals. The contact metal path surrounding the component is 2 µm wide to preserve the high quality of the device. Refer to Appendix B for a netlist of this capacitor used for hand-analysis LVS.

4.2.3 VARACTOR (CVAR) LAYOUT

The varactor used in this design is described in Section 3.2.6. For convenience, an entry from Table 17 is repeated below.

Table 25. CVAR used in design.

W [µm]	Row	Col	L [µm]	C_{min} [pF]	C_{max} [pF]
158.4	3	8	0.65	< 0.2	< 0.5

From this entry, it can be noted that the CVAR used in this design should consist of 3 rows and 8 columns, having a total width of 158.4 µm, and standard length of 0.65 µm. The maximum and minimum capacitance values are also given in this entry. To design the layout, Figure 42 depicts the CVAR model and its cross-section.

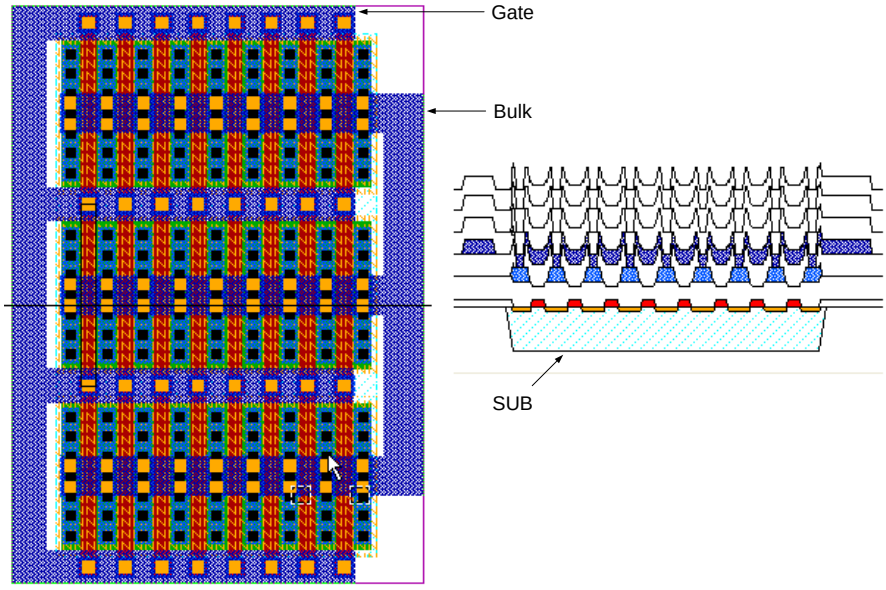

Figure 42. AMS 0.35 µm CVAR (left) and cross-section view (right).

As the name suggests (MOS varactor), the device looks almost like a type of MOS device (see Section 4.2.5). From the cross-section view in Figure 42, it can be noted that *metal1* (light blue) and *metal2* (dark blue) are used to connect the different sections of the device. The *poly1* (red) material acts as the conducting material, and defines the number of columns of the device. Therefore, from the left side of Figure 42, it is evident that there are 8 columns (red material) in 3 rows (MOS configurations from top to bottom), and therefore the design coincides with a 3 x 8 CVAR device, as defined in Section 3.2.6. A netlist of this component is not given in Appendix B, as Tanner® Tools® L-Edit® could not recognize this component as a MOS varactor, and the component was assumed correct as supplied (part of the design library) by AMS.

4.2.4 VERTICAL NPN LAYOUT

The vertical NPN transistor is another component (same as inductor models) that was not modified for this design, but rather the AMS supplied default design model was used. In order to create a transistor with a larger area (as described in Section 4.1.4), transistors were connected in parallel. This has the same effect of increasing the transistor area as it would

have been in changing the physical emitter length of the device. Thus, the default area is 1.2 µm^2, and to achieve an area of for instance 4.8 µm^2, four transistors are connected in parallel. Figure 43 depicts this operation.

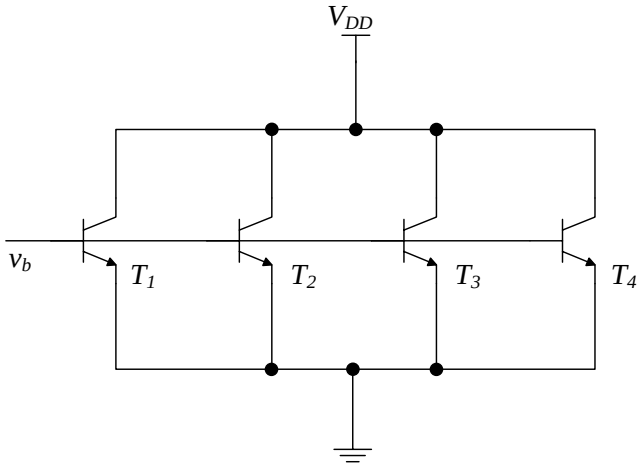

Figure 43. Four NPN transistors connected in parallel to increase overall area.

The cross-section and device definition can be found in [65], is not presented here, as this device can get complicated to understand and is beyond the scope of this dissertation. The L-Edit® component used is given in Figure 44.

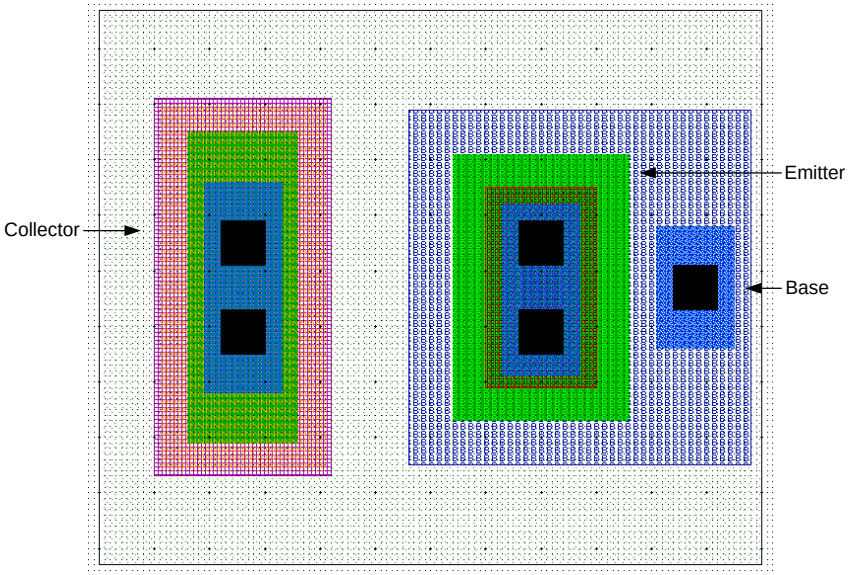

Figure 44. Four vertical NPN transistor used in L-Edit®.

From Figure 44, the collector of the transistor is defined by the node to the left of the figure, consisting of COLL (collector) material, placed on top of DIFF (diffusion) and NPLUS material. The centre node is the emitter, where the EMITT material defines the length (area)

of the transistor. This material is also used in conjunction with DIFF and EPOLY. The base node (on the right side) is just a contact placed on the BPOLY material surrounding the base and emitter. Section 4.2.5 describes the layout design procedure for the MOS transistors used in the design. A netlist of this transistor is not given in Appendix B, as Tanner® Tools® L-Edit® could not recognize this component as an HBT, and the component was assumed correct as supplied (part of the design library) by AMS.

4.2.5 MOS TRANSISTOR LAYOUT

The layout for the MOS (NMOS) transistor was modified to be used in the current source, to supply the correct amount of current (1.047 mA) and to limit the amount of noise generated by these transistors. The physical dimensions for the transistors are given in Section 4.1.2, and for descriptive purposes, only the 20 x 0.5 µm^2 transistor layout is discussed in this section. The principle for designing the different transistors remains the same, with only the dimensions changing. Figure 45 shows where the dimensions of the transistor are implemented when designing the component using a layout editor, such as L-Edit®. This shows the width and length of the transistor, in the case of the transistor described in this section, these parameters are 20 µm (*W*) and 0.5 µm (*L*). In this figure, *d*, *g*, and *s* represents the drain, gate, and source of the transistor respectively.

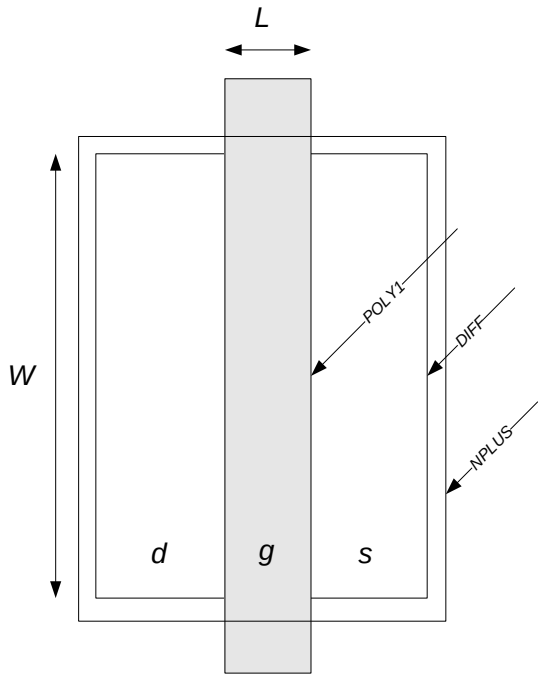

Figure 45. MOS transistor showing dimensions in layout design procedure.

Figure 46 depicts the NMOS transistor as designed in L-Edit® accompanied by its cross-section view on the right. Note, that to achieve the desired dimensions, a multi-fingered transistor was designed instead of a single, long transistor. Thus, from Figure 46, it can be seen that the transistor consists of two (red *poly1* material) transistor gates connected together, and the drains and sources are also connected, effectively creating two transistors of dimensions 10 x 0.5 µm^2 in parallel, to add up to a total of 20 x 0.5 µm^2.

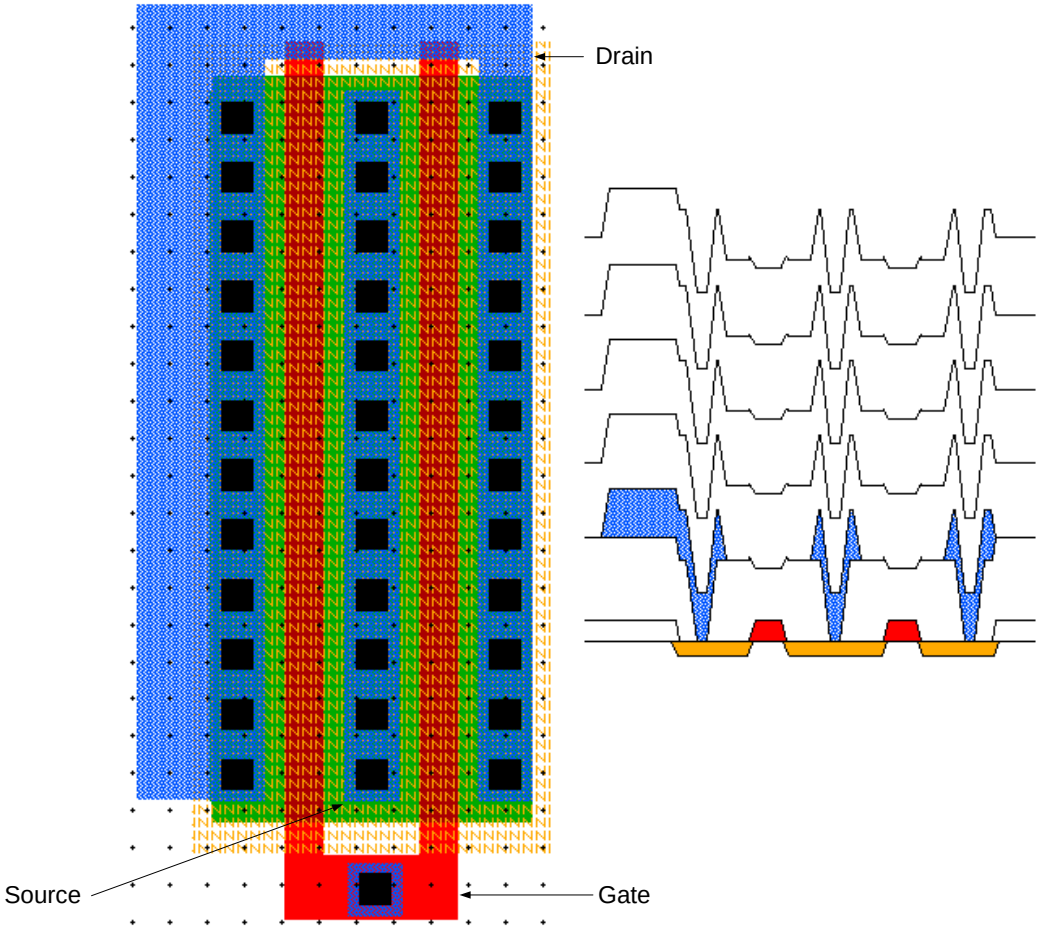

Figure 46. NMOS (left) and cross-section view (right).

The cross-section view shows that *metal1* (light blue material) is used to connect the terminals to each other. The transistor lies in NPLUS material (whereas a PMOS would lie in PPLUS) and several contacts are put on the drain and source terminal for maximum conduction and to reduce substrate losses due to bad contacts. The same procedure is followed to design transistors with different dimensions, and is not shown in this section. The following section (Section 4.2.7) describes how the entire circuit layout is designed to accommodate all of the abovementioned components. Refer to Appendix B for a netlist of this transistor used for hand-analysis LVS.

4.2.6 RPOLY SHEET RESISTANCE LAYOUT

A 2.179 kΩ sheet resistance was created using the RPOLY sheet resistor. The total resistance can therefore be achieved by adding a number of squares of RPOLY material, to effectively create a resistance of 2.179 kΩ. The total amount of squares needed, regardless of the layout of the resistor, would amount to 43.58 squares.

The L-Edit® layout and cross-section view of this resistor is given in Figure 47.

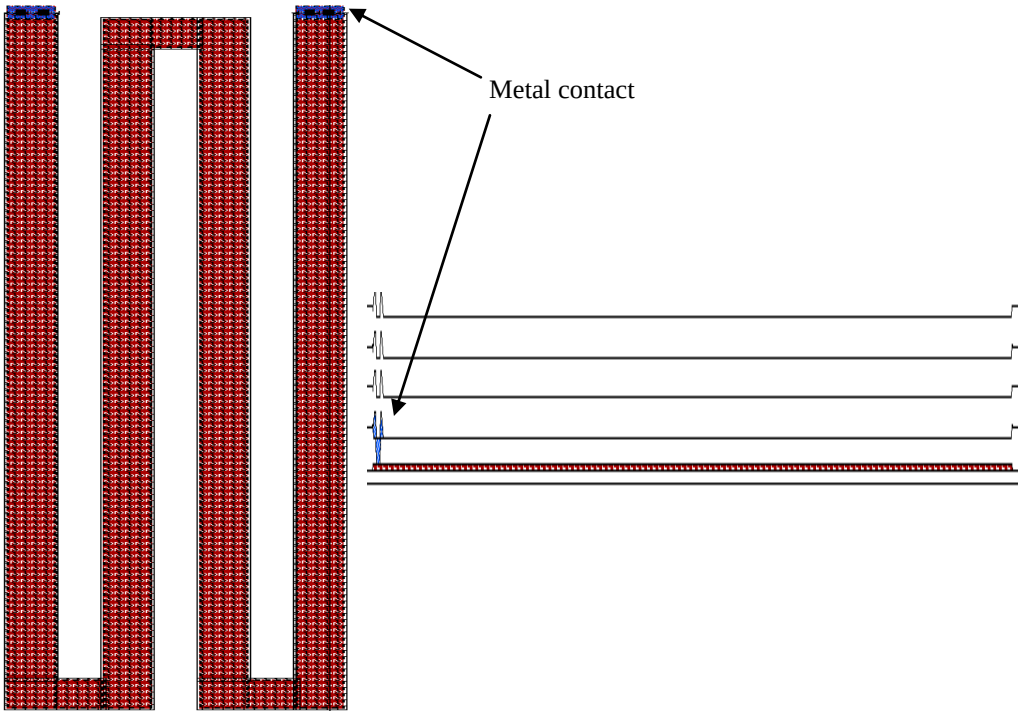

Figure 47. AMS 0.35 µm RPOLY sheet resistor (left) and cross-section view (right).

From the cross-section view, it can be seen that the blue (*metal1*) is used to connect RPOLY to the contact terminals. Note that the cross-section is taken from the vertical perspective of the resistor for easier display.

4.2.7 OVERALL CIRCUIT LAYOUT

Please refer to Appendix B for a figure on the floor plan of the proposed VCO.

4.3 PCB CIRCUIT DESIGN

Some design decisions are outlined in this section. As mentioned in Section 3.6, the PCB was designed by a third party who considered input parameters supplied by the researcher.

For the schematic design of the PCB, this section describes the outline of this procedure. Close comparison with the layout of the IC (as described in Section 4.2) are done, to ensure that the correct part of each subsystem of the test PCB is connected to the correct pins of the IC. The discussion below only considers one VCO (as multiple VCOs were manufactured on the IC for comparison purposes), as the design procedure are the same for all VCOs. Figure 48 depicts the schematic layout of the PCB design and a discussion regarding this layout is given below.

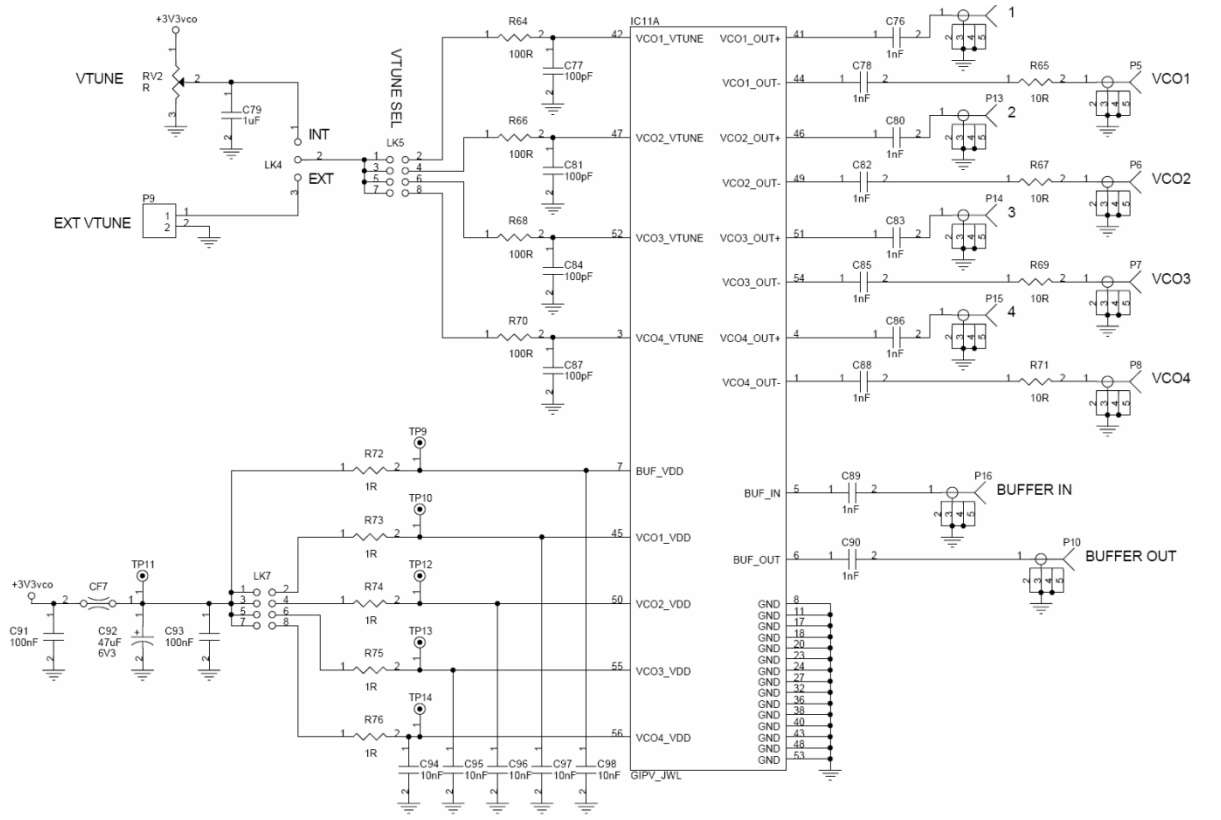

Figure 48. Schematic layout of PCB design.

The supply voltage pin of the VCO (PIN 45) receives a regulated 3.3 V supply voltage. This regulated voltage is provided by using the Texas Instruments® TPS78633DCQ voltage regulator. This regulator has a maximum current of 1.5 A and a high power supply rejection ratio (PSRR) of 49 dB at 10 kHz. It exhibits low noise characteristics of 48 μV_{RMS} and a fast start-up time of only 50 µs. A high-power (1 W), 1 Ω resistor is connected to the regulator input, in series, to absorb any high current that might flow due to a short circuit, protecting the IC from these currents. Capacitors towards ground filter out any noise presented to the circuit at his point. A green LED indicating that the system is ON is connected to the 3.3 V supply (with a 330 Ω current limiting resistor, R78, in series). Another capacitor (CF7) is placed in

series with the regulator, also to remove any high-frequency noise added to the system. A switch (LK7) is used to provide power to any of the VCOs (one at a time). Two test points are also placed on this line (TP11 and TP10) with a 1 Ω resistor (R73) in series between them. Measuring the voltage between these two test points, allows the user to actually determine the current flowing into the supply of the VCO by dividing the measured voltage by 1.

The tuning pin of the VCO (PIN 42) is used to manually adjust the frequency of operation. The regulated 3.3 V supply voltage is connected to a variable resistor (RV2), where the voltage across the resistor is fed to the pin of the IC (through a 100 Ω resistor, R64, which limits the current flowing to the IC and reduces the voltage with a factor) and used to adjust the operation frequency around 5 GHz. A switch (LK5) determines which VCO is currently connected to the tuning voltage. A 100 pF capacitor (C77) is connected at pin towards ground, to filter out high-frequency noise components.

The output pins of the VCO (PIN 41 and 44) are used to measure the output signal. The positive output signal is connected directly to the output connector (P12). It does however pass through a 1 nF capacitor (C76) to remove an added DC voltage. The negative output signal passes through an additional 10 Ω resistor.

The output signals can also be fed through the buffer circuitry designed in Section 4.1.4. The buffer receives the same supply voltage as the VCO (3.3 V regulated supply). The input to the buffer is connected to PIN5 of the IC, through a 1 nF capacitor (again removing any DC components) at P16. The output of the buffer can be measured at PIN 6 of the IC, using the connector P10.

All ground connections are grouped and grounded.

CHAPTER 5: RESULTS

5 INTRODUCTION

Chapter 5 discusses the results obtained for the proposed VCO circuit during simulation in Cadence® Virtuoso® [61]. The schematic circuit designed in Chapter 4 was constructed in the schematic editor and simulations were completed to ensure that the circuit operated correctly. Phase noise performance was measured in Cadence® Virtuoso® for two separate circuits. The first circuit was a standard design for a VCO operating at 5 GHz. This measurement was then compared to a second circuit. The second circuit was in essence similar to the first, only with the addition of a tail-current noise suppression circuit between the tail-current source and the emitters of the differentially connected HBT switching transistors in the VCO. Successful implementation could then be assumed if the phase noise rating of the second circuit outperformed the first by a noticeable margin. This chapter details some simulation results obtained, including but not limited to the phase noise. Current and voltage measurements at crucial nodes in the circuit were also measured and compared.

As mentioned, a physical IC was also created using the AMS S35D4M5 BiCMOS process to serve as further comparison of the hypothesis on a practical perspective. The IC was created purely based on the schematic design, so practical results should coincide with simulated results. These measurements were also taken and are outlined in this chapter for comparison purposes.

5.1 CIRCUIT EXCLUDING TAIL-CURRENT SHAPING

The first set of simulation results are obtained from the circuit with which tail-current shaping is *not* employed. This is the standard design for a differential VCO using HBT transistors and a NMOS-based tail-current source. The discussion of this circuit is given in Sections 4.1.1 and 4.1.2. The full circuit layout is given in Figure 49.

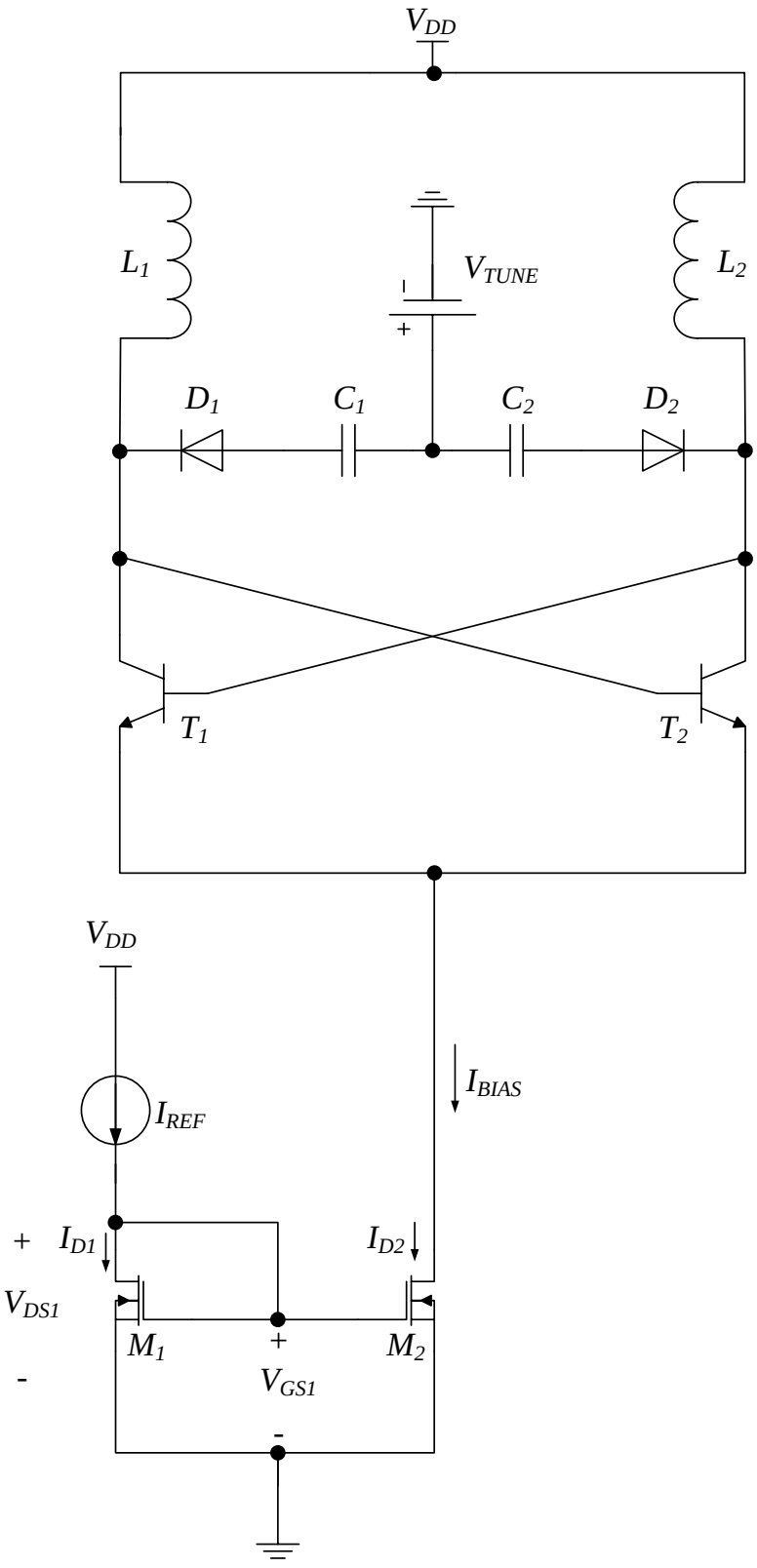

Figure 49. Full circuit layout of VCO without tail-current shaping.

5.1.1 OPERATING FREQUENCY RESULTS

The first and most important result that should be confirmed is the operating frequency of the circuit. The operating frequency was designed at 5 GHz, so a fast fourier transform (FFT) of the circuit operation should point this out. A time domain measurement was also taken. Figure 50 depicts the FFT obtained in Cadence® Virtuoso®. This figure does not have any markers in order to aid the reader to see exactly where the frequency components are situated as the markers tend to obstruct these components.

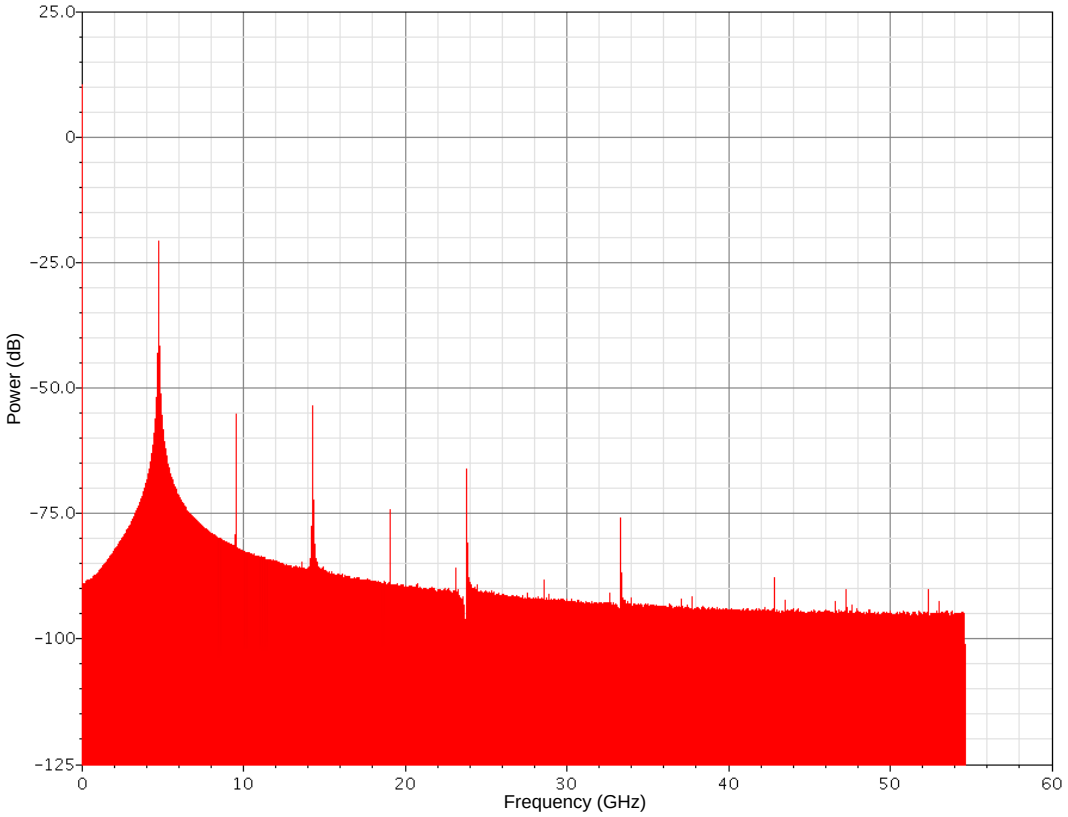

Figure 50. FFT of VCO without tail-current shaping (no markers).

The following figure, Figure 51, displays the exact same information, except that the markers are now included to give a clear indication of the values of the frequency components.

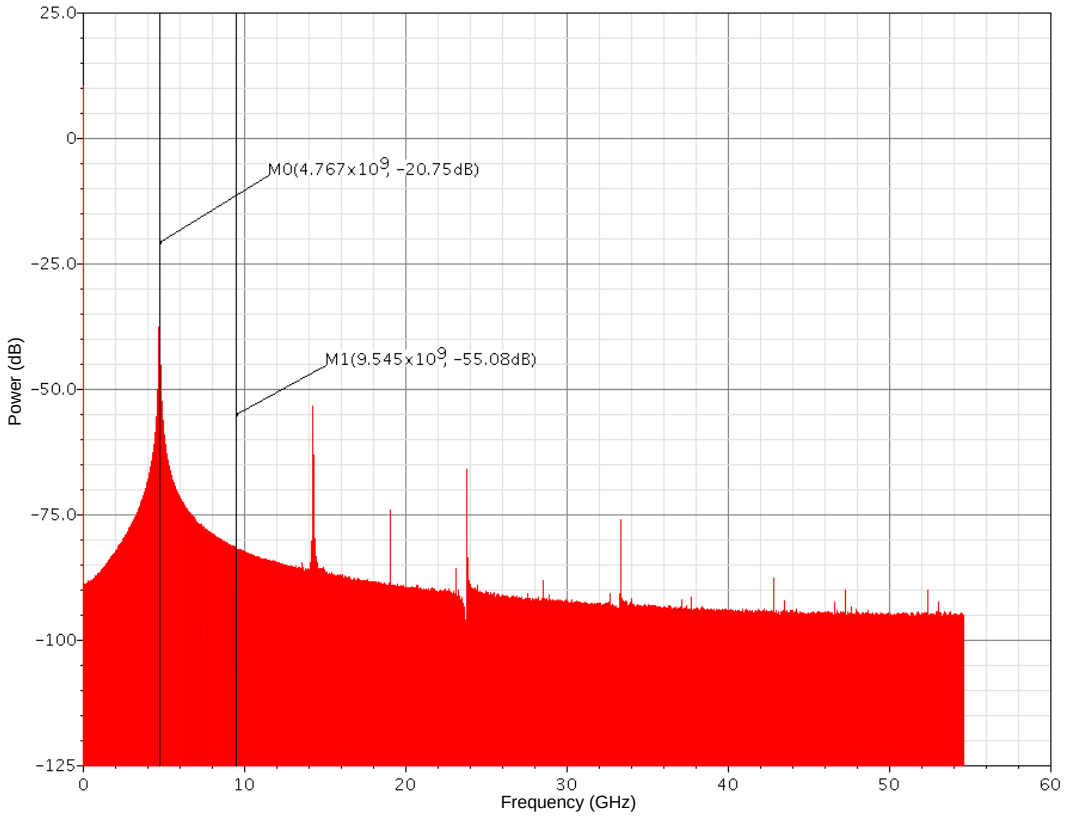

Figure 51. FFT of VCO without tail-current shaping (including markers).

From Figure 51 it is evident that the prominent frequency component is situated near, but not exactly at the 5 GHz region[2] (4.767 GHz with -20.75 dB power output at the fundamental frequency). The power at the fundamental frequency component, in mW, can therefore be determined by the following equation.

$$20\log P(mW) = P(dB) \tag{61}$$

$$20\log P(mW) = -20.75$$

$$\therefore P(mW) = 10^{-20.75/20}$$

$$= 91.73 \text{ mW}$$

[2] The reason that this component is not exactly at 5 GHz is not due to a design error though. In Cadence® Virtuoso®, in order to get a VCO to start oscillating, a separate source supplying a large voltage component needed to be included in the circuit to act as a disturbance in the circuit. This source however cannot be removed from the circuit once the oscillation started. The problem with this is that the source is not an ideal component and adds parasitic components to the node where it is connected and therefore changes the oscillation frequency somewhat. For most of the simulation results however, this source could be removed and the output netlist was used to verify the oscillation frequency. A short extract from this netlist is provided on the following page to prove that the oscillation frequency, with the additional voltage supply, is much closer to the 5 GHz range.

The amount of power present at the first harmonic is also of importance, as this can be used to determine the amount of distortion present in the circuit. From Figure 51, the power in the first harmonic is -55.08 dB (34.33 dB lower than the fundamental frequency), which can be equated by using (61) to be 1.76 mW.

```
Fundamental frequency is 4.96823 GHz.
pss: The steady-state solution was achieved in 7 iterations.
Number of accepted pss steps = 608.
Total time required for pss analysis `pss' was 1.77 s.

*******************************************************************************
Periodic Noise Analysis `pnoise': freq = 4.96823 GHz + (1 kHz -> 10 MHz)
```

From the above extract it can be noted that the oscillation frequency without the additional source is 4.96823 GHz, which is sufficiently close to 5 GHz. A FFT representation to highlight the output power of the fundamental frequency in dBm is given in Figure 52.

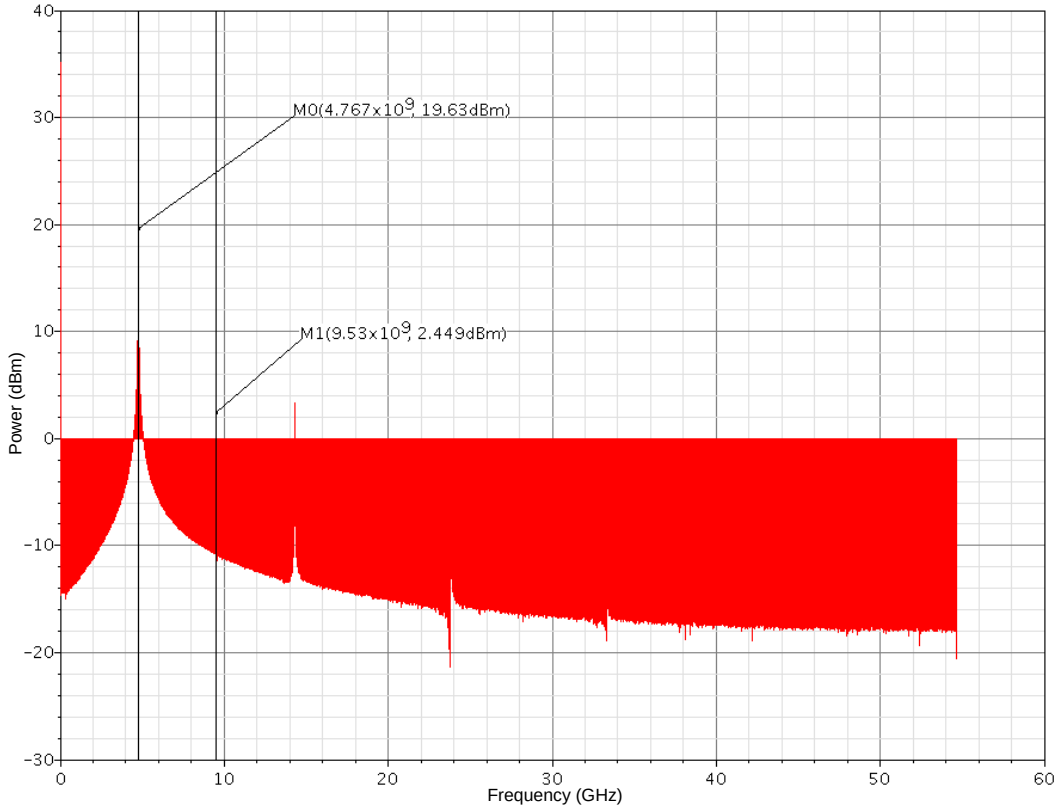

Figure 52. FFT (dBm) of VCO without tail-current shaping.

From Figure 52, the power in mW can again be calculated for the fundamental frequency, given as 19.63 dBm at 4.767 GHz. The result is expected to be the same as the above

calculation from the dB power, and the following expression is used to confirm this relationship.

$$P(mW) = 10^{\left(\frac{P(dBm)}{10}\right)}/1000 \quad (62)$$
$$= 10^{19.63/10}/1000$$
$$= 91.83 \text{ mW}$$

which, compared to 91.73 mW, is within bounds to be assumed equal. The power of the first harmonic (2.449 dBm at 9.53 GHz) can be equated as 1.76 mW.

A time-domain representation of the output voltage is given in Figure 53.

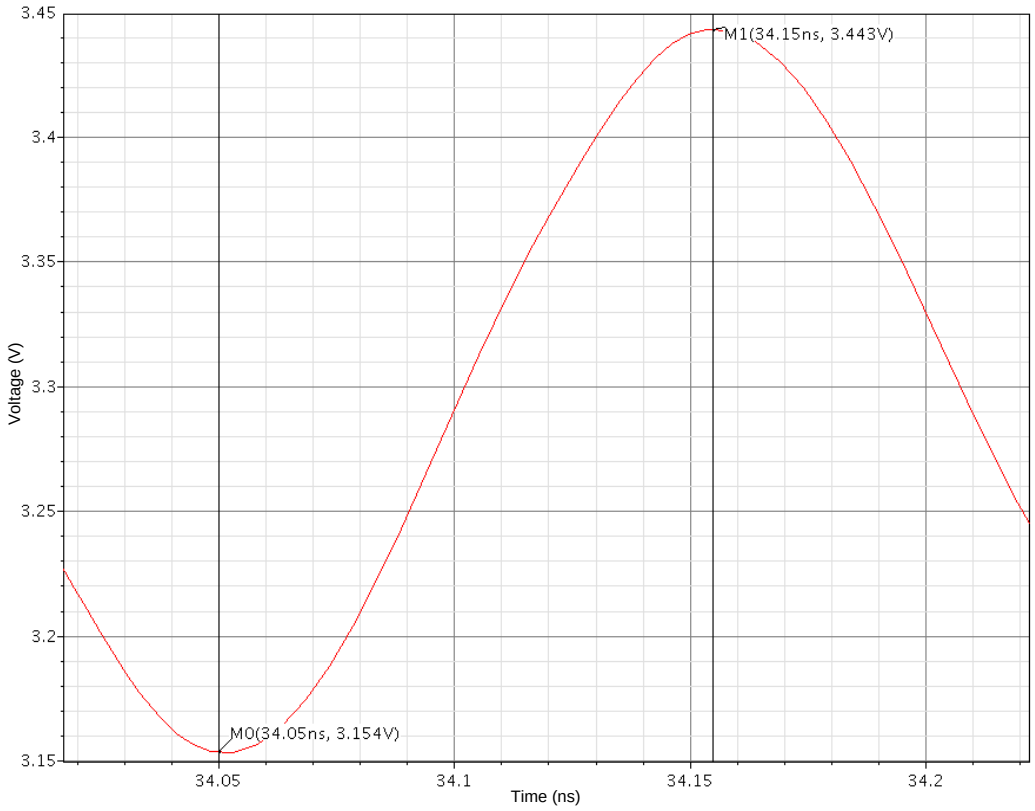

Figure 53. Time domain output of VCO without tail-current shaping.

From Figure 53 the operating frequency can be determined by taking the time between the two peaks and applying (63).

$$f_0 = \frac{1}{2\Delta T} \tag{63}$$
$$= \frac{1}{2(34.15\ ns - 34.05\ ns)}$$
$$= 5\ \text{GHz}$$

where the multiplication by two is due to the fact that only half a period of the output signal is used. The reason that this equation results at exactly 5 GHz is due to the lower accuracy provided as the time values are only rounded to two decimal digits.

This output voltage is not yet passed through an output buffer or capacitive component to remove the added DC component of 3.3 V (supply voltage). Thus the output voltage amplitude can be determined by subtracting the high and low peak voltages (3.443 V – 3.154 V) which results in an output voltage swing of 289 mV. This value can be compared the designed value of 337.47 mV in Section 4.1.1.

5.1.2 DC RESULTS

From Section 4.1.2, the current source was designed to provide a steady DC current to the VCO of 1.047 mA. A measurement was taken of the current flowing through the drain of transistor M_2 (see I_{D2} - Figure 49) and this is plotted in Figure 54.

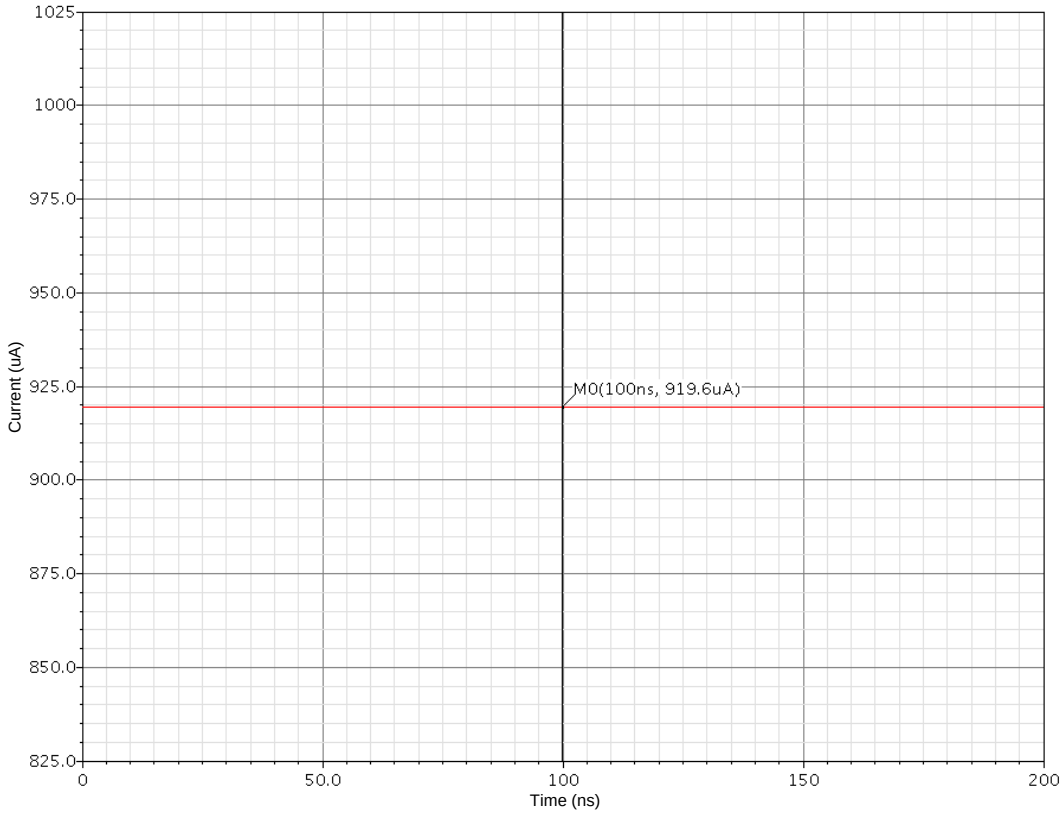

Figure 54. DC current through transistor M_2.

From Figure 54, a marker was placed at the 100 ns operating time of the circuit (the straight line DC enabled that the marker could be placed anywhere). The value obtained at the 100 ns point, and therefore during the entire operation of the circuit, was 919.6 µA. This value is within 88 % of the designed value and was considered sufficient.

The DC voltage drop across the gate-source terminal of transistor M_2 (see Section 4.1.2) is given in Figure 54.

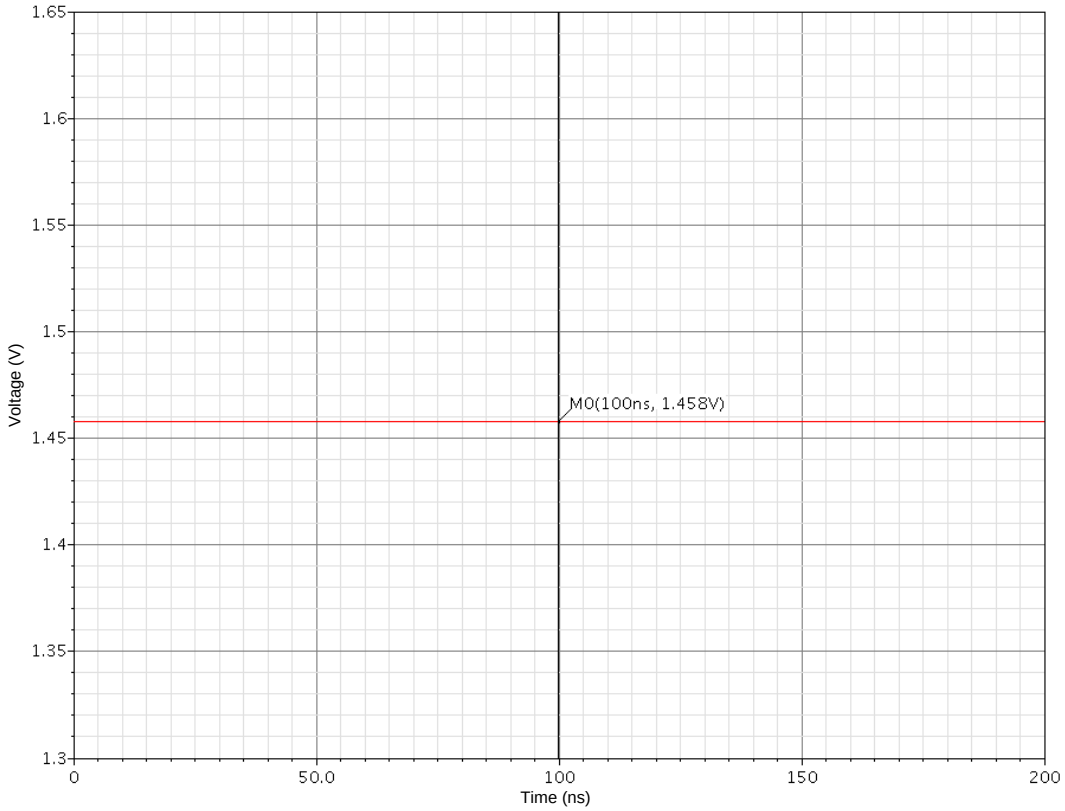

Figure 55. DC voltage across gate-source terminal of transistor M_2.

From Figure 55, where the marker is again placed arbitrarily as the 100 ns point, the voltage across the gate-source terminal of transistor M_2 (and therefore the voltage V_{GS1} in Figure 49) is 1.458 V. Due to an apparent mismatch between the output impedance of the switching HBTs and the output impedance of the NMOS used in the current source, this value of V_{GS1} differs slightly from the value obtained in Section 4.1.2. This mismatch in output impedances forces a higher value of V_{GS1} and can also be attributed to the higher than anticipated power consumption in the circuit (see next paragraph).

The average DC output power of the circuit measured at the output and given in mW is depicted in Figure 56.

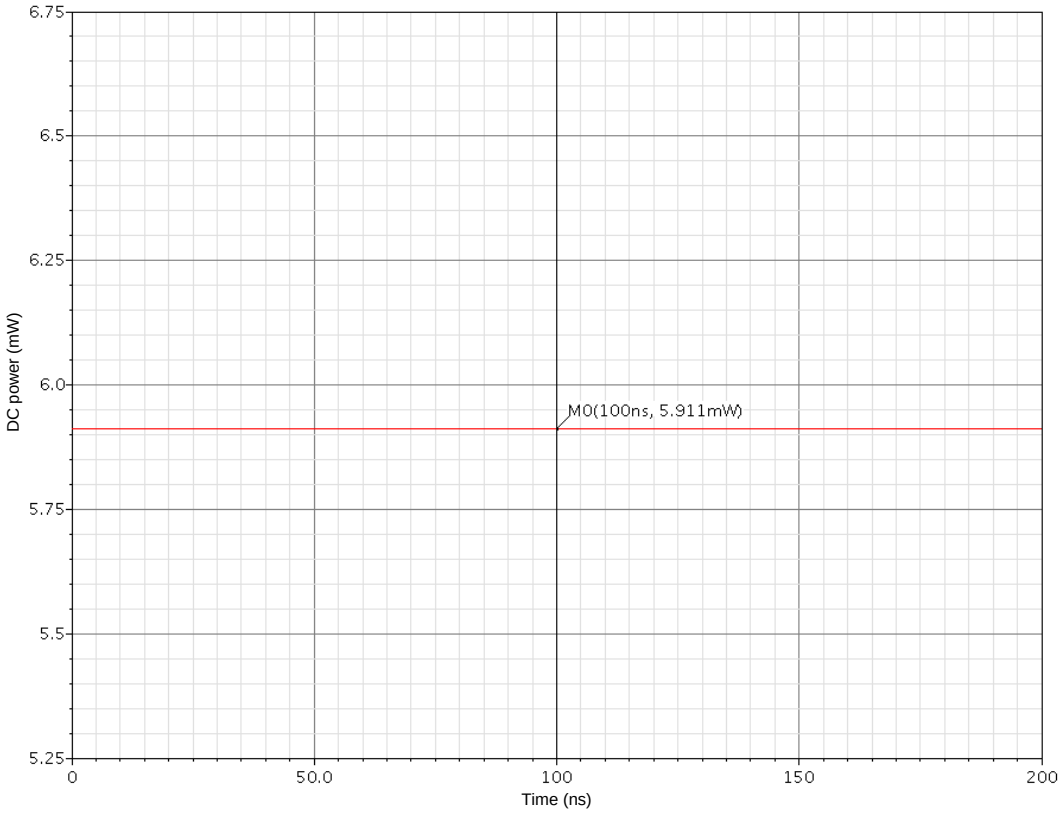

Figure 56. DC output power at output in mW.

From Figure 56, the average DC output power of the VCO circuit is 5.911 mW.

5.1.3 PHASE NOISE PERFORMANCE RESULTS

The most important parameter to be inspected when obtaining the simulated results is the phase noise performance of the VCO circuit. The hypothesis for this dissertation, as a reminder, is that the phase noise performance can be improved by applying a tail-current shaping circuit across the driver transistor of the MOS current source to eliminate low frequency noise in this transistor to be up-converted by the oscillating circuit to add as phase noise at the output.

The phase noise rating at different offset frequencies was taken (10 kHz, 100 kHz and 1 MHz) and the results are plotted in Figure 57.

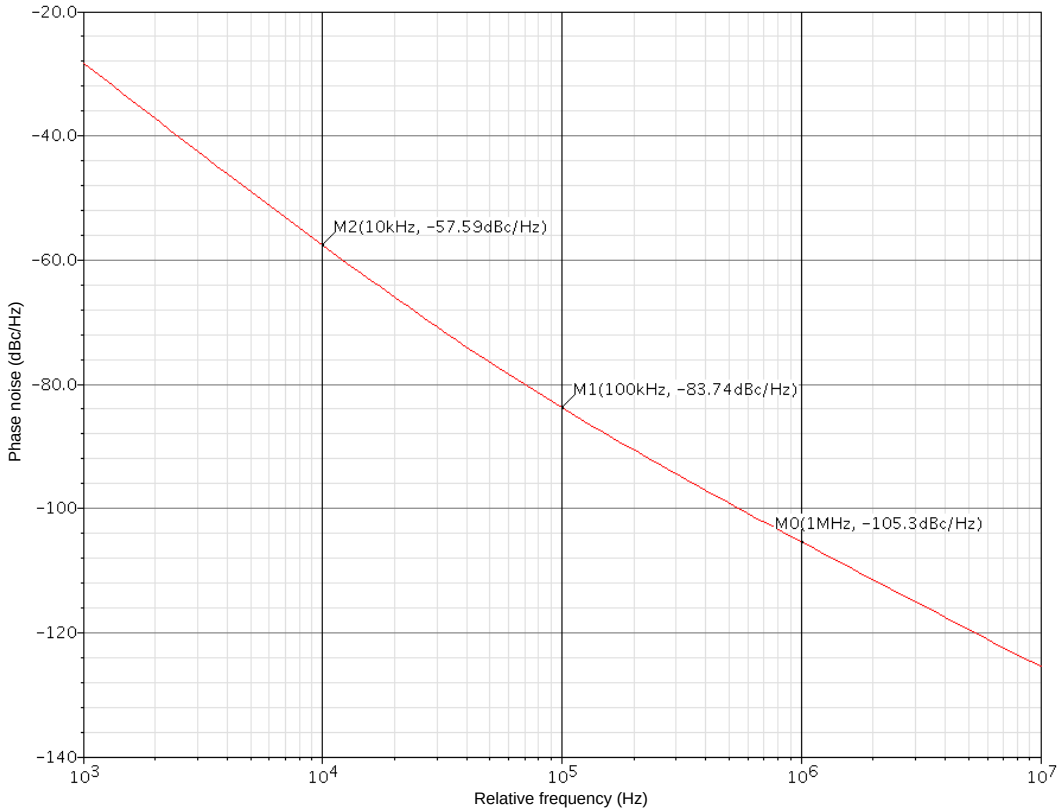

Figure 57. Phase noise ratings of VCO without tail-current shaping.

These results are at this moment only relative, as they will be compared to the phase noise performance of the same circuit but with tail-current shaping employed in Section 5.2. The overall performance of this circuit, with phase noise of -105.3 dBc/Hz at a 1 MHz offset from the 5 GHz carrier is not much better than current VCOs published as from Table 1. There were numerous additional simulations performed (see Section 5.4) to try and improve the phase noise performance of the specific circuit, but the results were not significant enough. The reason for the relatively poor phase noise performance (even with tail-current shaping employed) was written off as lacklustre or average performance of the AMS S35D4M5 process, and its accompanying models (with the main focus being a low inductor *Q*-factor). Better results should be able to be achieved when using a newer (and hence a smaller) process.

Table 26 summarizes the results of the phase noise performance of the VCO when tail-current shaping is not employed.

Table 26. Phase noise performance of VCO without tail-current shaping.

Offset frequency	Phase noise [dBc/Hz]
10 kHz	-57.59
100 kHz	-83.74
1 MHz	-105.3

These results will later be used as comparison for phase noise performance improvement.

Referring back to (31) in Section 2.4.3, the figure of merit for the oscillator operating without tail-current shaping can be equated to serve as a performance evaluation. From the equation the FOM is found to be -147.093 dBc/Hz.

Section 5.1.4 compares the results obtained in simulation, with results that are obtained using the mathematical model for phase noise, and simulating this model using Matlab®[2].

5.1.4 PHASE NOISE MATHEMATICAL COMPARISON

Taking into consideration the results obtained in simulations, it is possible to determine phase noise by combining these results with the ones obtained in Section 2.4.2. This can prove that the mathematical interpretation of phase noise is correct. Recall Leeson's formula for phase noise in an oscillator. This equation (30) is repeated below.

$$\mathcal{L}\{f_m\} = 10\log\left[\left[\left(\frac{f_0}{2Q_L f_m}\right)^2 + 1\right] \times \frac{FkT_0}{P} \times \left(\frac{f_c}{f_m} + 1\right)\right]$$

If all of the variables in this equation are known, it would be possible to predict the phase noise of the oscillator without tail-current shaping by simulating the equation for different offset frequencies using Matlab®[3]. This section will do just that, by determining the variables by designing the schematic of the circuit in Cadence® Virtuoso® and extracting the unknown parameters from the simulation results in order to predict phase noise performance.

Starting off with the known parameters, the following summary can be compiled.

[3] Matlab®, developed by Mathworks®, is a high-level language and interactive environment that is able to perform computationally intensive tasks on computer systems.

f_0 which represents the oscillation frequency, is well known as the tank circuit values are designed to achieve this. The operating frequency is 5 GHz (5 x 10^9 Hz), and is a constant in this equation. f_m is the offset frequency from the carrier where the phase noise is measured, and this value will be iterated to draw a graph connecting the phase noise at each offset. Values that will be used as f_m are for example 1 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz up to about 10 GHz, and the results are plotted logarithmically. k is Boltzmann's constant and has a constant value of 1.38 x 10^{-23} J/K and the temperature T_0 is 300 K during normal operation.

To determine the loaded quality factor (Q_L) of the tank circuit, the bandwidth of the circuit should be simulated as Figure 14 suggests. This is done by simulating the differential oscillator as a single common emitter amplifier, with the same tank and current source characteristics. Thus, from Figure 58 the bandwidth can be determined. This is done below.

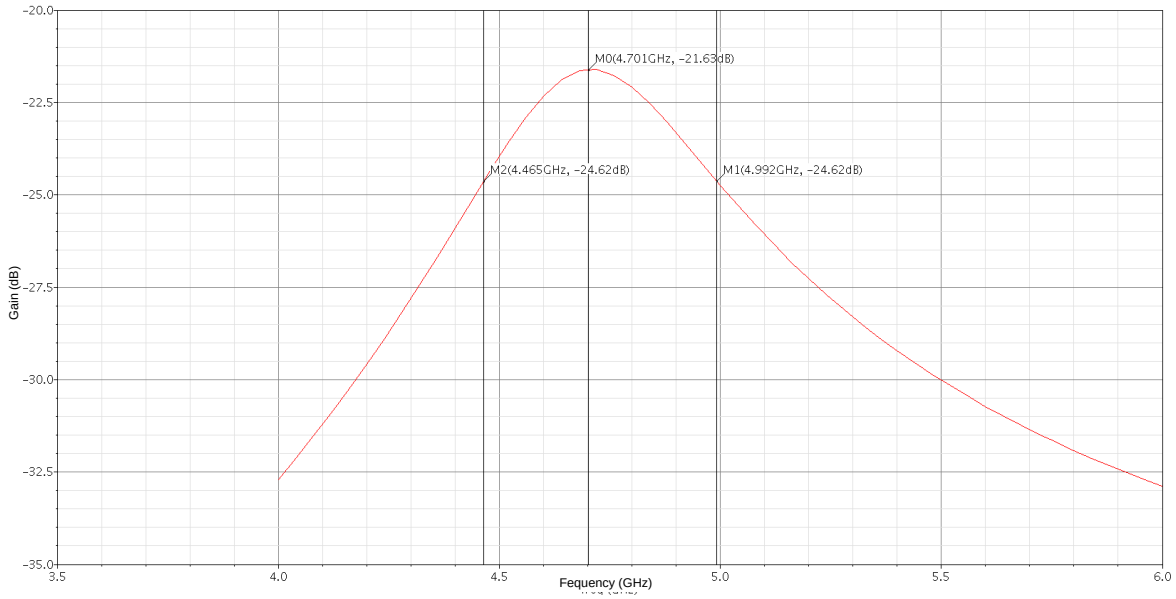

Figure 58. Representation of oscillator bandwidth due to tank quality factor.

From Figure 58, the gain drops 3 dB from its maximum value of -21.63 dB at the two frequencies of 4.465 GHz and 4.994 GHz respectively (in a band-pass configuration), giving a total loaded bandwidth of 529 MHz. Thus the loaded Q can be determined as (4.701 GHz / (4.994 GHz – 4.465 GHz) = 8.886).

The average power dissipation in the circuit (in mW) is also simulated, and this results in power dissipation (P) of 5.911 mW (see Figure 56). For the phase noise equation, average power dissipation must be specified in mW, therefore there is no conversion to dB or dBm.

The corner frequency (f_c) and noise factor (F) can be determined through simulation of the noise performance of the oscillator. From Section 2.4.2, theory implies that the corner frequency (where the thermal noise and the flicker noise graphs intersect), assuming that the circuit has a reasonable loaded Q-factor, appears at exactly half the circuit bandwidth. Following this assumption, the corner frequency is determined to be in the region of about (529 MHz / 2 = 264 MHz).

Finally, the noise factor or noise figure of the circuit should be determined to accurately simulate the phase noise based on the mathematical model supplied by Leeson. Again, by referring back to Section 2.4.2, the equation for the noise figure (13) can be rewritten in the following format [28].

$$N_{out}\,(dBm) = F + kTB(dBm) + 10logB \tag{64}$$

where $N_{out}\,(dBm)$ is the output noise of the oscillator measured in dBm (including the gain of the positive feedback amplifier, which in this case is 0 dB), F is the noise figure (also in dBm, which can later be converted to a ratio), $kTB(dBm)$ is the thermal noise floor of any circuit, for which the value is -174 dBm for a 1 Hz bandwidth at 300 K, and B is the bandwidth at which the noise is measured. Since phase noise is measured in dBc/Hz, the bandwidth here would be 1 Hz. Rewriting (64) and making noise figure the subject, the following equation,

$$F = N_{out}\,(dBm) - kTB(dBm) - 10logB \tag{65}$$

is used to finally determine the noise figure. From (65) it is evident that only the noise amplitude at the output is unknown ($N_{out}\,(dBm)$). This can easily be simulated using Cadence® Virtuoso®, and the result is given in Figure 59.

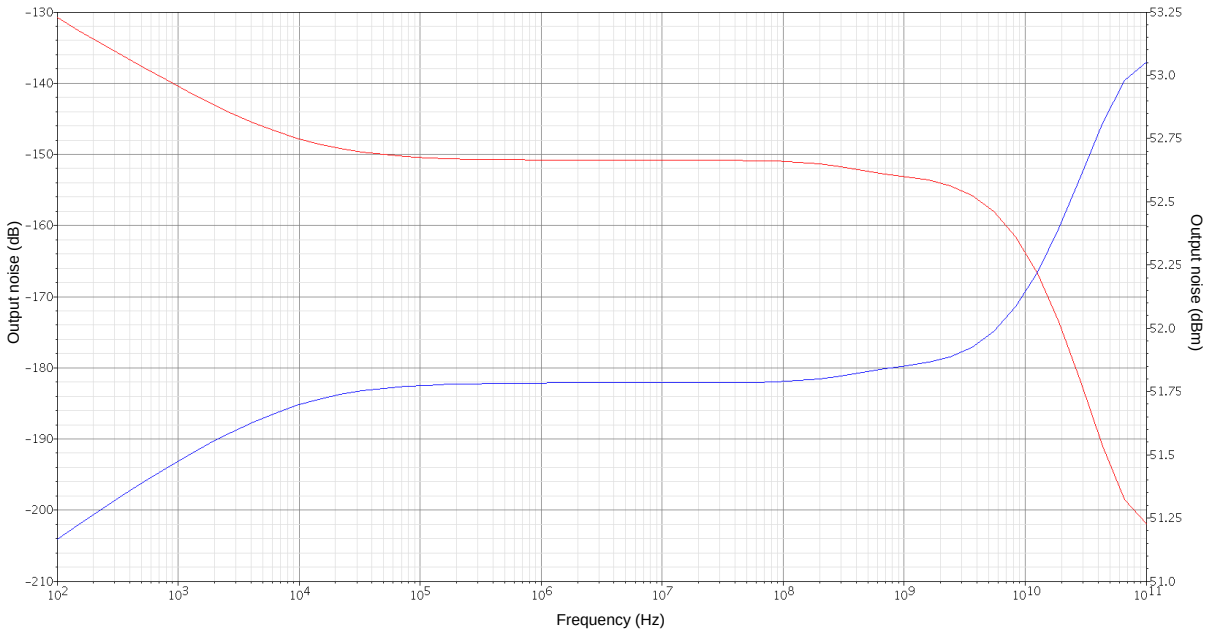

Figure 59. Noise at oscillator output simulated in Cadence® Virtuoso®.

From Figure 59, the output noise (in dBm) at the 5 GHz operating point is read from the figure and determined to be around -170 dB. This correlates to a value of 10^{-17}, which can then be converted to dBm using (62).

$$N_{out}\,(dBm) = 10\log\frac{10^{-17}}{1mW} \tag{66}$$

which equals -140 dBm. Therefore, returning to (65), the noise figure is equated as

$$F = -140\ dBm + 174\ dBm - 10log1$$
$$= +34\ dBm$$

This value in dBm can now be converted back using the same method as in (62) but working backwards, to a value in dB (2.51 dB) or a unit-less value of 4, which represents the noise factor as used in Leeson's equation.

Now that all of the variables in Leeson's equation are known, it is possible to simulate the phase noise in Matlab®.

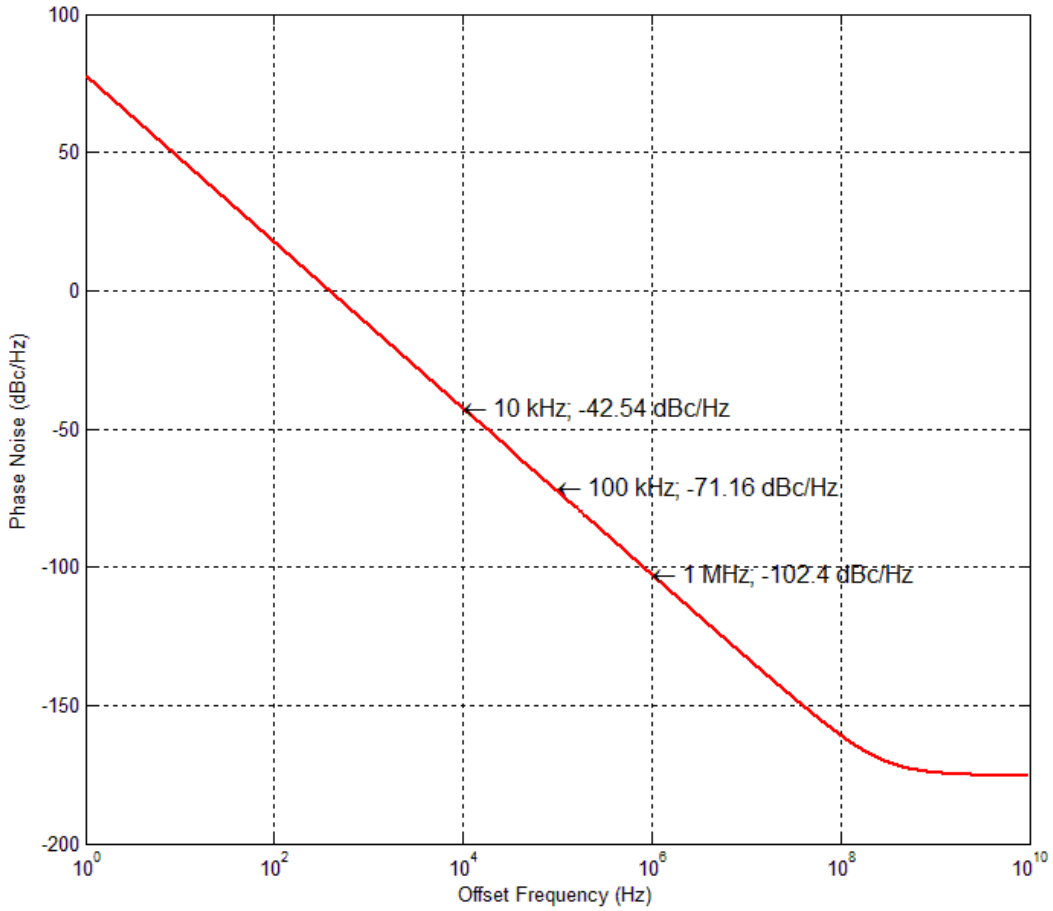

Figure 60. Leeson's equation for phase noise simulated in Matlab®.

Comparing Figure 60 with the simulation results in Figure 57, it is evident that the results correlate quite well near the 1 MHz offset frequency. The phase noise ratings nearer to the operating frequency has somewhat of a discrepancy as the schematic simulator struggles to accurately simulate the $1/f^2$ noise due to the low *Q*-factor presented by the inductor. As can also be seen from Figure 57, the phase noise never reaches a definite transition from $1/f^2$ to $1/f$ noise, due to the low *Q*-factor. Further comments on the shortcomings of (11) as a predictive phase noise model is discussed in Appendix A.

Section 5.2 discusses the simulated results obtained when using the same circuit as in Section 5.1 but with the addition of a tail-current shaping technique at the current source.

5.2 CIRCUIT INCLUDING TAIL-CURRENT SHAPING

The circuit used in this section is the same as the circuit discussed in Section 5.1 but with the addition of a tail-current shaping circuit. The discussion of this particular circuit is given in Section 4.1.3, and a schematic representation is given in Figure 61.

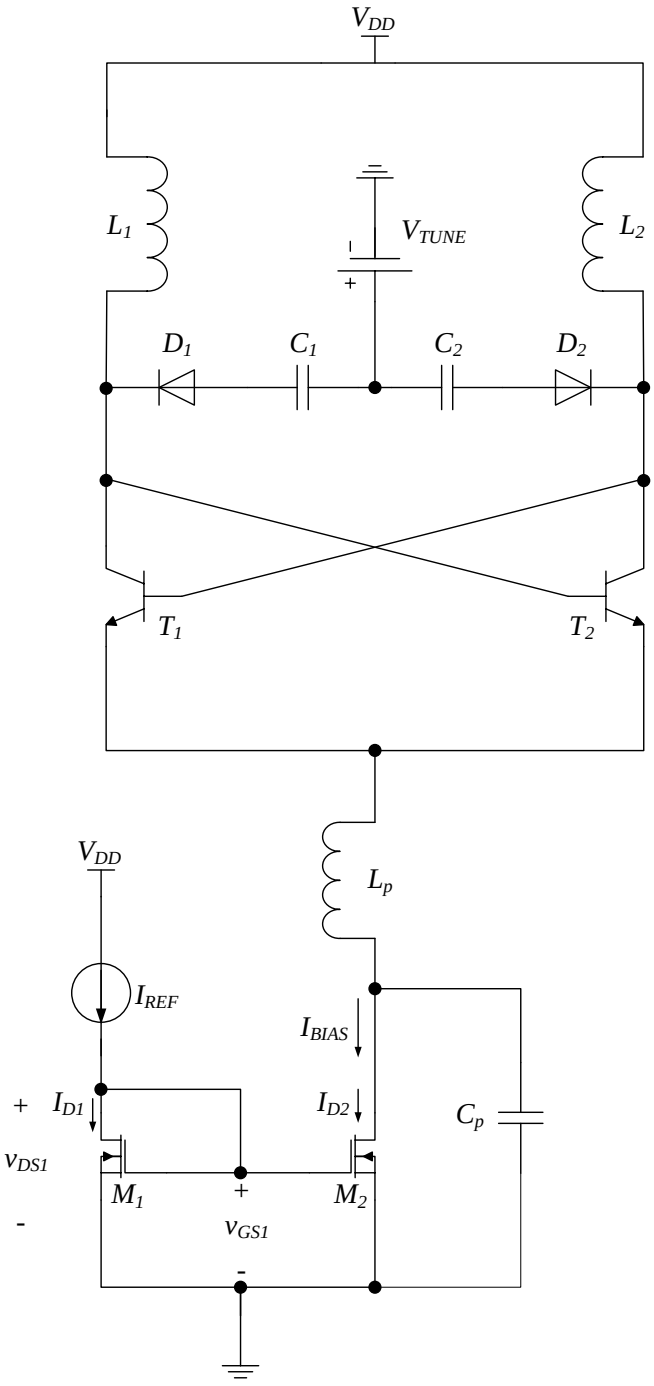

Figure 61. Full circuit layout of VCO with tail-current shaping.

Note from Figure 61 the addition of the inductor (L_p) and capacitor (C_p) which are inserted between the driver transistor M_2 and the emitters of the HBT transistors (T_1 and T_2) in the VCO circuit. These components prevent the up-conversion of the low-frequency noise to phase noise and the component values were designed and are given in Section 4.1.3.

5.2.1 OPERATING FREQUENCY RESULTS

The operating frequency of this circuit should ideally also be centered at 5 GHz as no changes to the LC tank section were made and the addition of the capacitor and inductor components should not influence the overall inductance and capacitance values of the tank circuit. To prove this hypothesis, a FFT at the output node of the circuit was obtained and is given in Figure 62. Again, as in Section 5.1.1, two FFTs are given, with and without markers.

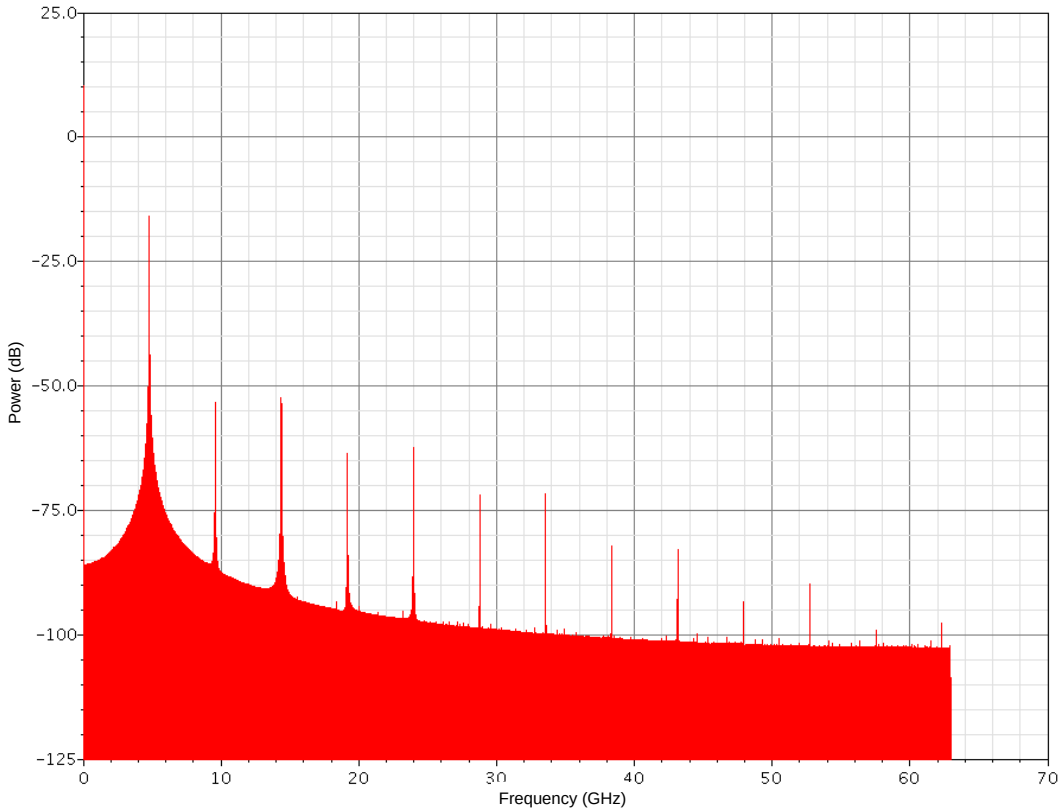

Figure 62. FFT of VCO with tail-current shaping (no markers).

The most prominent frequency components can be seen in Figure 62, and the values of these components can be seen in Figure 63.

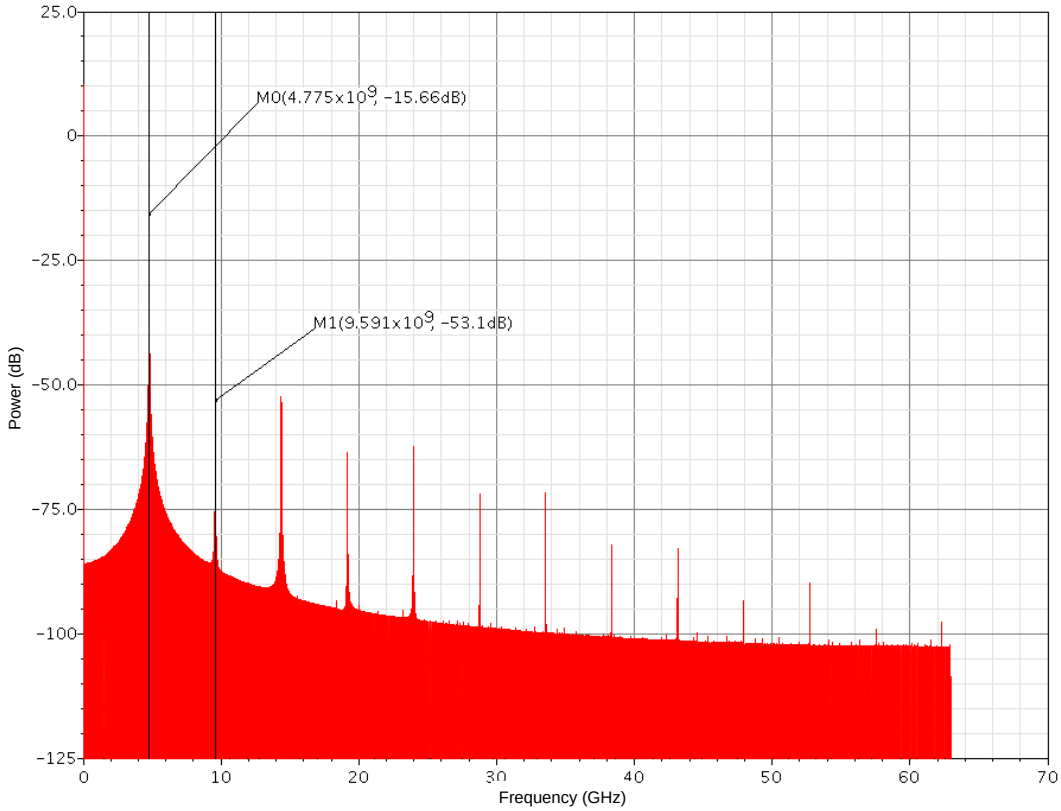

Figure 63. FFT of VCO with tail-current shaping (including markers).

The first maker (M0) is placed at the fundamental component of the frequency spectrum. The value at this marker is 4.775 GHz, and the slight disposition from a 5 GHz component is again not due to design inaccuracies but due to the addition of a voltage source to supply the circuit with the necessary disturbance before oscillation can commence. The power output at the fundamental frequency is -15.66 dB, compared to -53.1 dB for the first harmonic at 9.59 GHz (twice the fundamental frequency). This shows a 37.44 dB difference from the fundamental frequency compared to the 34.33 dB difference when the tail-current filter was not employed. By using (61), the power in the fundamental frequency component can be calculated (-15.66 dB) to be 164.8 mW. The power in this component is therefore (164.8 mW – 91.73 mW) 73.07 mW larger than the power of the fundamental frequency component of the circuit where tail-current shaping is not employed, increasing noise performance due to larger oscillation amplitudes (power). The power in the first harmonic (-53.1 dB) is around 2.2 mW, which is 0.44 mW larger than the circuit without tail-current shaping.

The following paragraph is again an extract from the output netlist, where the additional supply is removed, to prove the oscillation frequency is close to 5 GHz.

```
Fundamental frequency is 4.99785 GHz.
pss: The steady-state solution was achieved in 3 iterations.
Number of accepted pss steps = 601.
Total time required for pss analysis `pss' was 1.41 s.

*******************************************************************************
Periodic Noise Analysis `pnoise': freq = 4.99785 GHz + (1 kHz -> 10 MHz)
```

From this extract it can be noted that the actual operating frequency with the voltage source removed is in fact very close to 5 GHz, with an exact value of 4.99785 GHz. This value differs slightly from the value obtained in Section 5.1.1 (4.96823 GHz) due to the apparent addition of capacitance in series with the intrinsic base-emitter capacitance (C_{je}) of the HBT transistors T_1 and T_2, adding to the intrinsic characteristics of these components and therefore changing the operating frequency somewhat. The effect is however negligible.

The output power, specified in dBm with a marker added to the fundamental frequency component and the first harmonic is given in Figure 64.

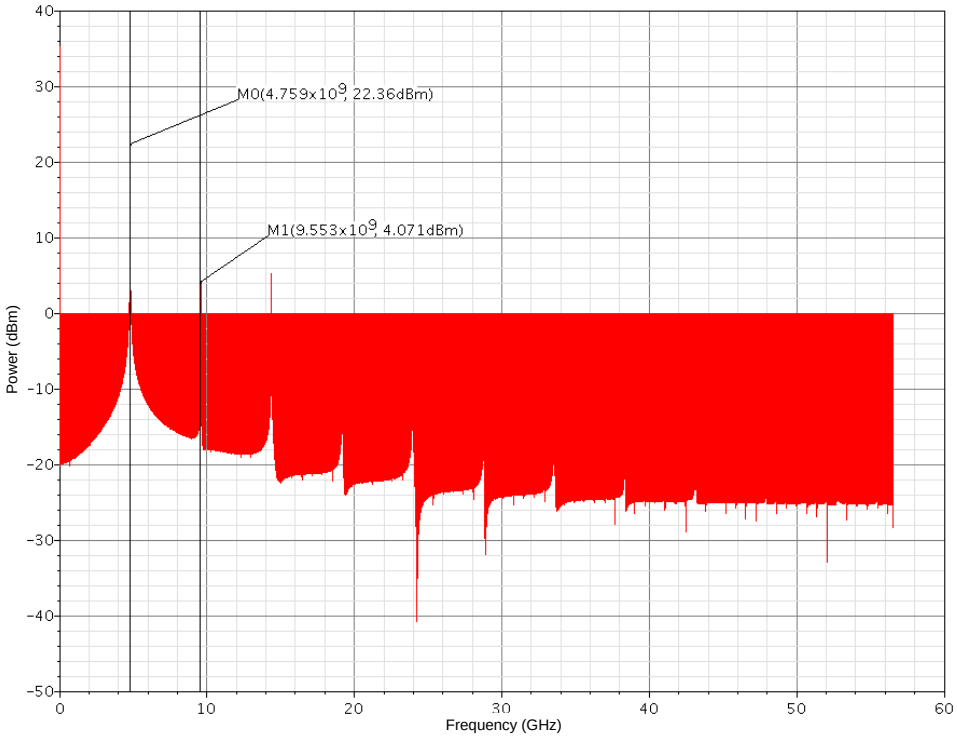

Figure 64. FFT (dBm) of VCO with tail-current shaping.

On a dBm scale, the power in the fundamental frequency component and the first harmonic can be determined by using (62). From (62), the power in the fundamental component (22.36 dBm) is around 172.2 mW (compared to the 164.8 mW from the dB scale) which is again an improvement from the 91.83 mW from the circuit without tail-current shaping. The power in the first harmonic (4.071 dBm) is 2.55 mW (2.2 mW from the dB scale). Note the significant drop in power between the fundamental frequency component at 4.759 GHz (22.36 dBm) and the first harmonic at 9.553 GHz (4.071 dBm) due to the addition of the inductive and capacitive filtering technique at the current source.

The time domain representation at the output of the circuit is given in Figure 65.

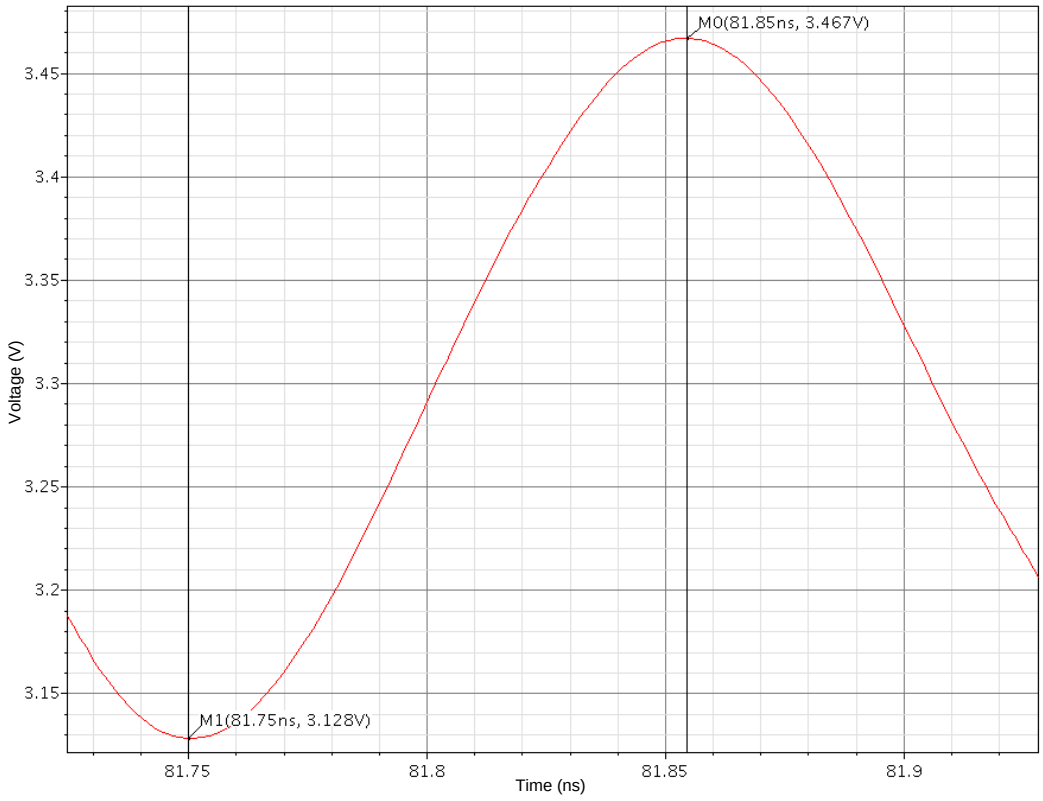

Figure 65. Time domain output of VCO with tail-current shaping.

By using (63) where ΔT (81.85 ns – 81.75 ns) is equated to be 100 ps, the frequency obtained is again 5 GHz. This value is again to be expected as the addition of the tail-current shaping circuitry should not influence the operating frequency of the VCO substantially.

The amplitude of the output voltage can again be determined (around the 3.3 V DC offset) to be (3.467 V – 3.128 V) in the region of 340 mV. The amplitude of the output oscillation voltage has thus increased by 17.5 % from its nominal 289 mV due to the improved DC-to-RF conversion (see Section 2.5.4 and [21]), which is expected to improve the phase noise performance.

5.2.2 DC RESULTS

As given in Section 5.1.2, the DC current of the circuit operating under normal conditions is given in this section. The results are expected no to differ substantially from that of Section 5.1.2 as the addition of the tail-current shaping circuit should not affect biased DC currents. The results are given in Figure 66 where reference to Figure 49 should be noted.

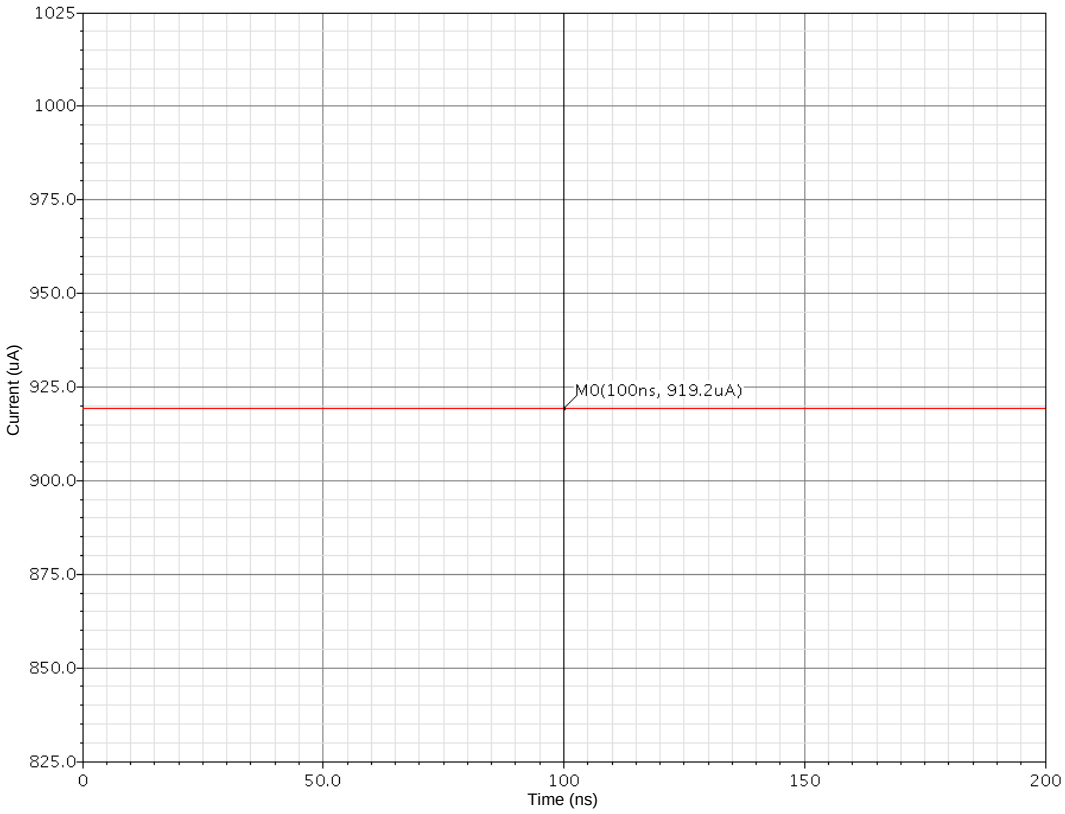

Figure 66. DC current through transistor M_2.

The DC current flowing in this circuit, according Figure 66, is 919.2 µA. This value can be compared to the value obtained in Section 5.1.2, which was 919.6 µA. Therefore a slight change of only 0.04 % in the DC current was noted, and regarded as negligible, as expected.

The DC voltage drop across the gate-source terminal of transistor M_2 (see Figure 61) is given in Figure 67.

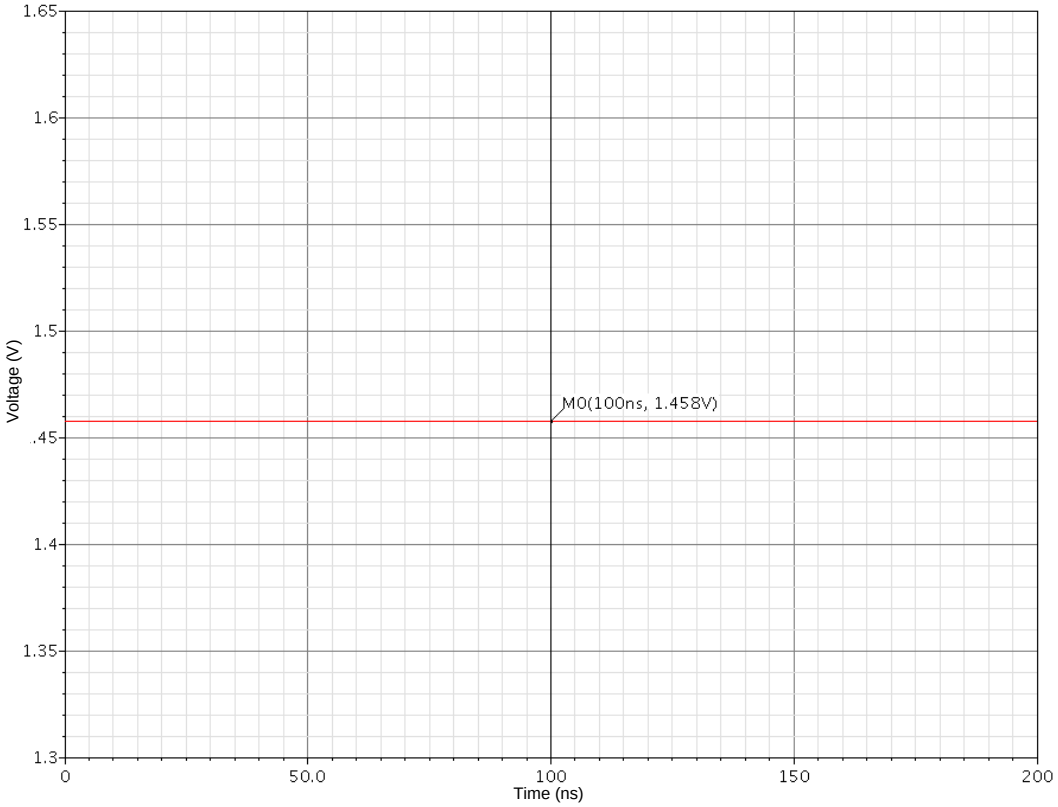

Figure 67. DC voltage across gate-source terminal of transistor M_2.

The result is also unchanged from that of Section 5.1.2 due to the fact that the DC current, which according to Section 4.1.2 determines this value of V_{GS1} (which is the same as the gate-source voltage of M_2) has not changed.

The output power of the circuit, given as a DC constant in mW, is provided in Figure 68.

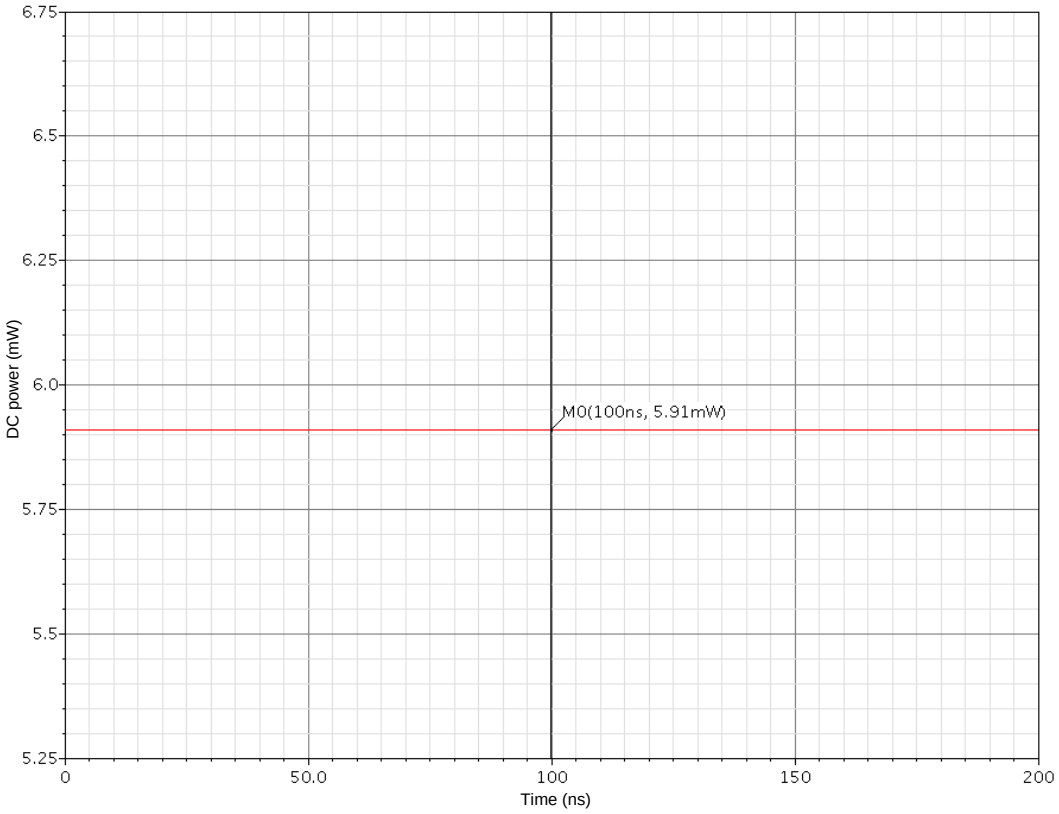

Figure 68. DC output power at output in mW.

Compared to the value of 5.911 mW obtained in Section 5.1.2, this value of the power dissipated in the circuit (5.91 mW) is exactly the same as expected, proving the hypothesis (Section 1.2) that no additional power is added to the circuit when applying tail-current shaping, and only the increased oscillation amplitude together with the narrower drain current pulses add to improve phase noise performance (see Section 2.5.4 and [21]).

5.2.3 PHASE NOISE PERFORMANCE RESULTS

Finally, and most importantly, the phase noise performance of the two circuits can now be compared to validate the hypothesis: "will tail-current shaping have a significant effect on phase noise performance in a RF VCO?".

The phase noise measurements of this circuit was also measured at three offset frequencies, namely 10 kHz, 100 kHz and 1 MHz, to clearly indicate the overall improvement in phase noise, and the linearity of this improvement. Figure 69 depicts these simulation results.

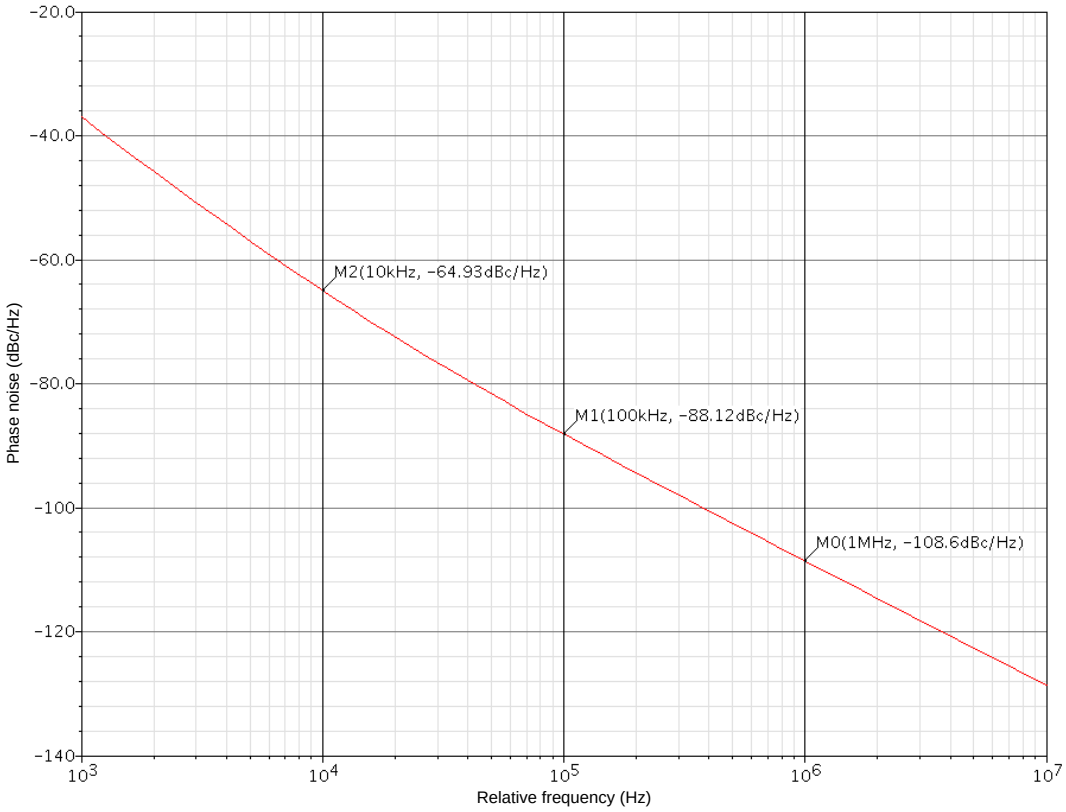

Figure 69. Phase noise ratings of VCO with tail-current shaping.

At first glance of Figure 69, and concentrating on the phase noise of the 5 GHz carrier frequency at a 1 MHz offset, an improvement can definitely be noted. The phase noise given in Section 5.1.3 of -105.3 dBc/Hz at a 1 MHz offset from the carrier frequency, has now been improved to -108.6 dBc/Hz. To summarize these results, Table 27 is constructed.

Table 27. Phase noise performance of VCO with tail-current shaping.

Offset frequency	Phase noise [dBc/Hz]
10 kHz	-64.93
100 kHz	-88.12
1 MHz	-108.6

Referring back to (31) in Section 2.4.3, the figure of merit for the oscillator operating without tail-current shaping can be equated to serve as a performance evaluation. From the equation the FOM is found to be -150.393 dBc/Hz.

Now, combining Table 26 and Table 27, Table 28 serves as a full summary of the two circuits, in terms of phase noise performance.

Table 28. Phase noise performance comparison.

Offset frequency [MHz]	Phase noise without tail-current shaping [dBc/Hz]	Phase noise with tail current shaping [dBc/Hz]	Improvement [%]
0.01	-57.59	-64.93	12.7
0.1	-83.74	-88.12	5.23
1	-105.3	-108.6	3.13

From Table 28 it is evident that an improvement in overall phase noise performance exists over the entire frequency spectrum, in a non-linear fashion. The improvement of the phase noise (in %) decreases as the offset frequency from the carrier increases, as the offset approached the actual noise floor of the circuit at infinite offset (usually reached above a 100 MHz offset from the carrier).

5.3 MEASURED RESULTS

Before continuing to the measured results, it is important to take note that the measured results are somewhat inconclusive. Although measured results were obtained on an operational IC, due to time and money constraints, the results are not clear indications of the proven hypothesis. The reader is advised to focus on the simulated results to conclude the hypothesis, as the measured results are more for completeness, and future works (see Section 6.3) should improve these results for a more concise comparison. Figure 70 is a photo taken of the test circuit on which the measurements were done.

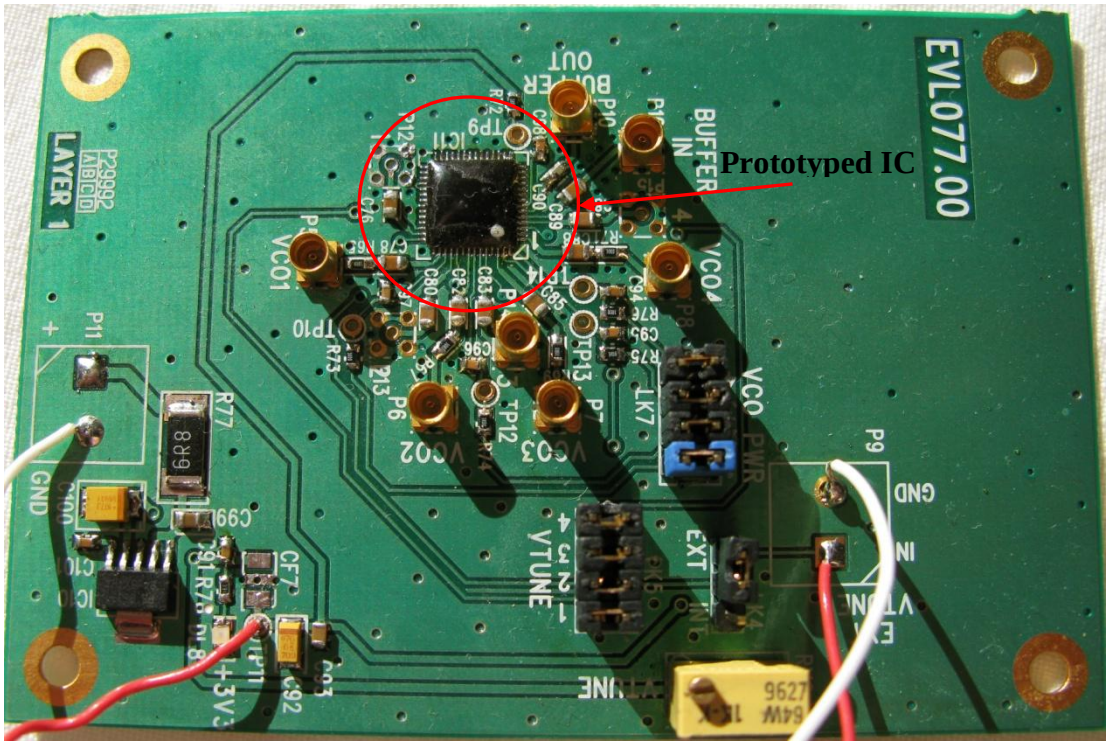

Figure 70. Photo of test circuit with prototyped IC encircled.

For a schematic view of this test circuit, refer to Figure 48. Note that the prototyped IC is encircled in red. The VCO outputs are also visible in Figure 70, where each output is marked VCOX, where 'X' refers to a number between 1 and 4.

This section documents some of the measured results obtained from the prototyped IC. Three separate VCOs were measured on chip. The ideal is to design two VCOs, which are in essence the same, but the only difference being the addition of the tail-current shaping circuit. The VCO that was designed in this way however did not work accurately as designed, as a flaw (see Figure 71) during the design process hindered this operation. The second (improved) VCO therefore is, in its basic design, a little different from the first, as the current source is designed with HBTs instead of NMOS transistors. Simulations however did show that the phase noise of these two VCOs, in their basic configuration (without tail-current shaping) is very similar in fact, so it seems fair to compare these two VCOs. Emphasis should just be concentrated on the fact that these measured results are only relative, and do not replace the cogent results obtained through simulation. IC design (if there were no cost-related limitations) is an iterative process, and future designs would prove more usable as all the errors can be corrected. Important still is to document the measured results, and this is

done in this section. Figure 71 represents the MOS transistor designed in L-Edit® which contained the error that caused the IC not to operate correctly.

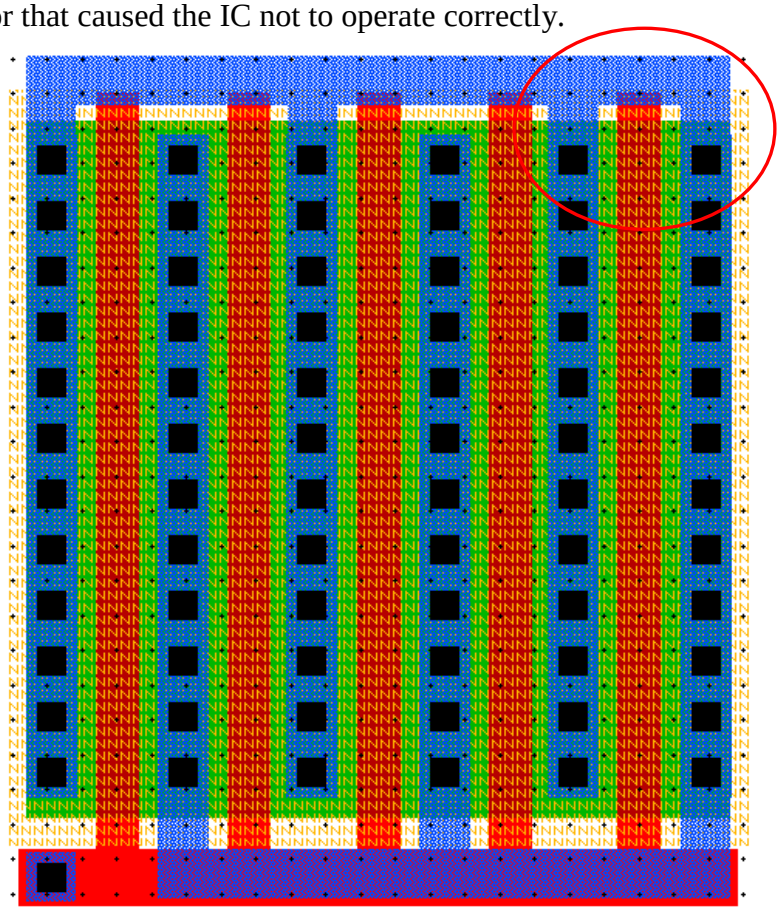

Figure 71. L-Edit® MOS transistor with error in design.

From Figure 71, the red circle shows where the error in the layout occurred. The blue metal material in this figure connects the drain and source of the transistor directly, hence forming a short-circuit that caused incorrect operation. This blue metal contact should only have been connected to the drains of the transistor. If this would be done, the IC would operate correctly, however, a further iteration of the current design would be needed to correct this. Due to this error, the voltage supply had to be reduced from the designed 3.3 V to ≈ 1.1 V (see Table 29) to enable oscillation. Using a 3.3 V supply during measurements resulted in a too large current flowing in the circuit, and the switching transistors could not operate correctly due to saturation.

A summary, the three measured VCOs can be categorized by:

- VCO 1 – this VCO is based on the LC tank design and it does have a tail-current shaping circuit at the current source. The current source is designed using NMOS transistors.
- VCO 2 – is in essence the same as VCO 1, but the configuration of the varactors differs to investigate the effect on phase noise with a higher capacitance on the switching transistor's collector.
- VCO 3 – is similar to VCO 1, but the tail-current source is designed using HBTs.
- VCO 4 is the basic configuration of the LC VCO without tail-current shaping. This VCO would ideally be compared to VCO 1, but did not operate correctly, therefore only relative comparisons could be made.

Figure 72 represents the floor plan of the four VCOs designed in L-Edit®.

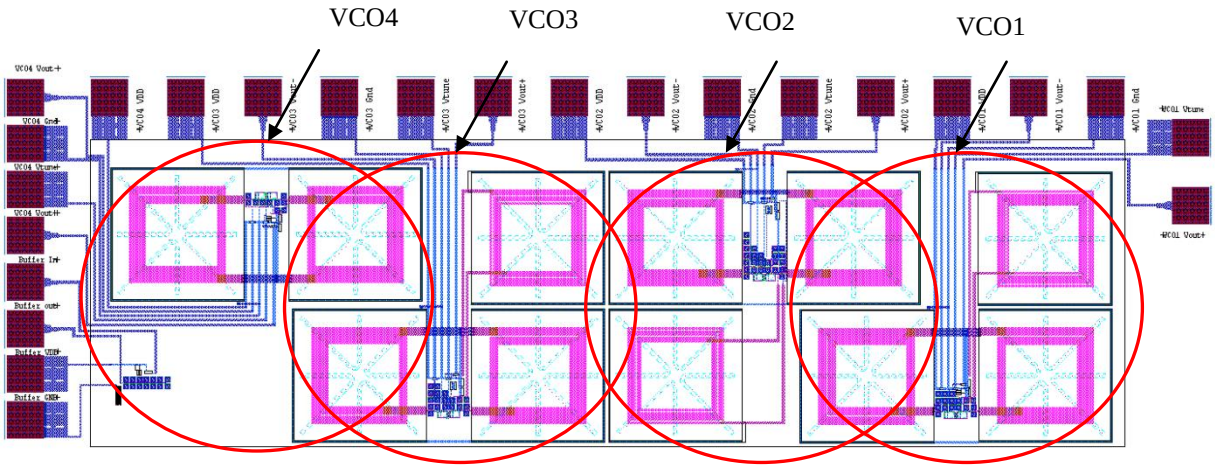

Figure 72. L-Edit® layout of four VCOs designed and simulated.

From Figure 72, the four VCOs can be seen as they are laid out in the final floor plan of the IC. Note that VCO 4 did not operate correctly, and therefore is not included in the measured results section below. Refer to Figure 75 for a photo of this layout.

The measured phase noise results for VCO 1, VCO 2, and VCO 3 are plotted for completeness, and the results for VCO 3 shows that the inclusion of tail-current shaping to the basic LC topology, has the best phase noise results (regardless of the configuration of the components in the circuit). Also note that the operating frequencies for all VCOs are not at 5 GHz. This is also a result from an error in the layout design, and the supply voltage had to be dropped significantly (see Table 29) which resulted in this lower operating frequencies. In

relative terms however, the measurements can be interpreted. Table 29 documents all of the measured results of the first VCO.

Table 29. Documented measured results of three measured VCOs.

Offset frequency f_m	Phase noise [dBc/Hz]		
	VCO 1	**VCO 2**	**VCO 3**
	f_0 = 3.77 GHz	f_0 = 3.77 GHz	f_0 = 4.12 GHz
	V_{cc} = 1.14 V	V_{cc} = 1.14 V	V_{cc} = 1.14 V
	I_{BIAS} = 3.6 mA	I_{BIAS} = 3.6 mA	I_{BIAS} = 3.6 mA
	DC power = 4.1 mW	DC power = 4.1 mW	DC power = 4.1 mW
1.5 kHz	-	-43.36	-43.04
2.5 kHz	-	-	-
5 kHz	-	-	-
10 kHz	-41.29	-45.55	-45.37
25 kHz	-43.03	-50.81	-53.21
50 kHz	-55.48	-60.08	-65.74
100 kHz	-65.06	-71.31	-83.6
250 kHz	-81.02	-92.5	-90.43
500 kHz	-88.97	-96.75	-99.33
1 MHz	-95.70	-102.36	-108.48
2.5 MHz	-109.27	-109.7	-113.29
5 MHz	-115.85	-114.63	-118.68

To see the overall effects clearly, Figure 73 is presented.

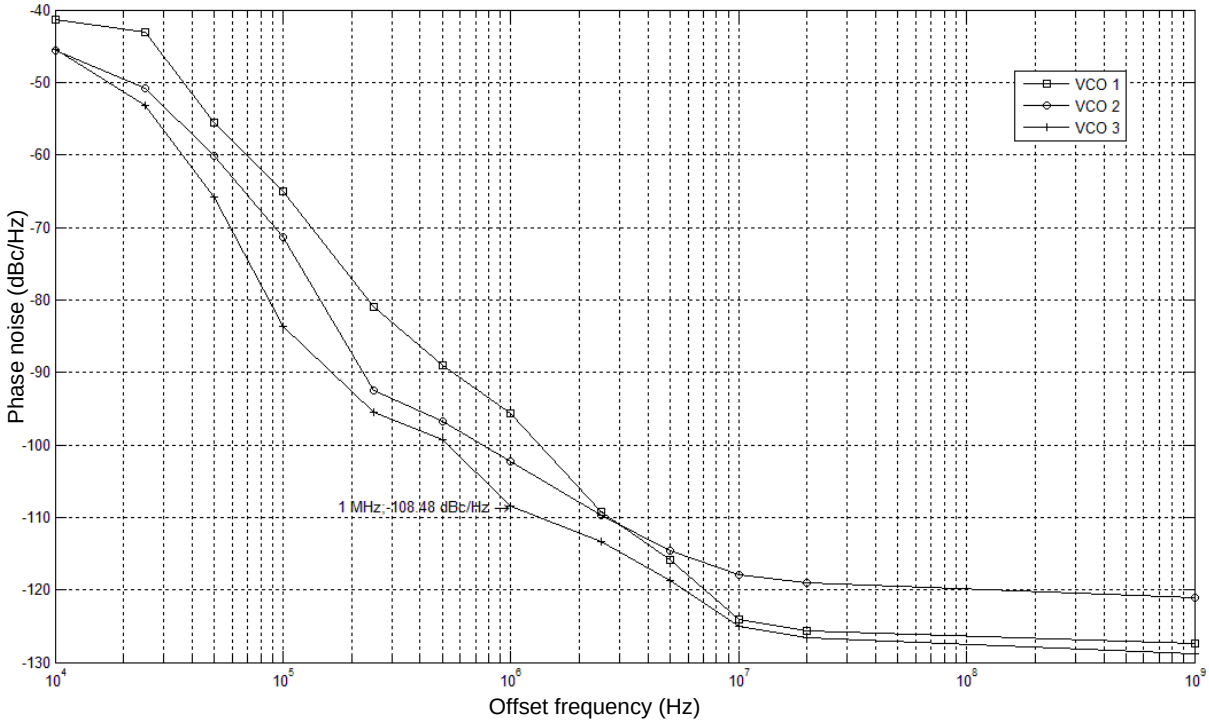

Figure 73. Measured results for all VCOs in prototyped IC.

The measured results obtained for VCO 1, VCO 2, and VCO 3 in Table 29 are presented in Figure 73. Although it is not fair to directly compare all of the results, it should be noted that the phase noise performance of VCO 3 (+) exceeds that of all the other VCOs. The results also correlate well to the simulation results in Section 5.2.3. To improve measured results, the prototyping of the IC should go through a further iterative process, but initial results do prove that the tail-current shaping does increase phase noise performance, and that the simulation results and the measured results correlate, meaning that a successful implementation of research into a practical, measureable component was achieved. When comparing the measured results with Figure 69, it seems that $1/f^3$ noise dominates a larger part of the spectrum during measurements compared to simulation. Simulation algorithms are very complex mathematical derivations. Even with good convergence and high accuracy, statistical fluctuations and simplified component (SPICE) models can lead to inaccurate phase noise predictions especially closer to the carrier frequency where modelling device non-linearities can become extremely involved.

Figure 74 is a photo of the IC that was prototyped for measurement purposes.

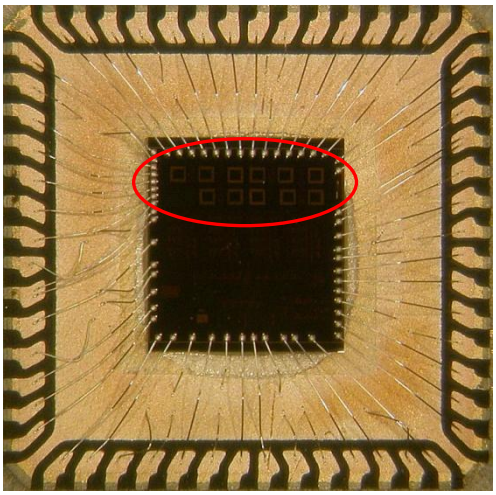

Figure 74. Photo of measured IC prototype.

The red circle in Figure 74 shows where the 4 VCOs (see beginning of this section) are situated. A zoomed in version of this photo is given in Figure 75.

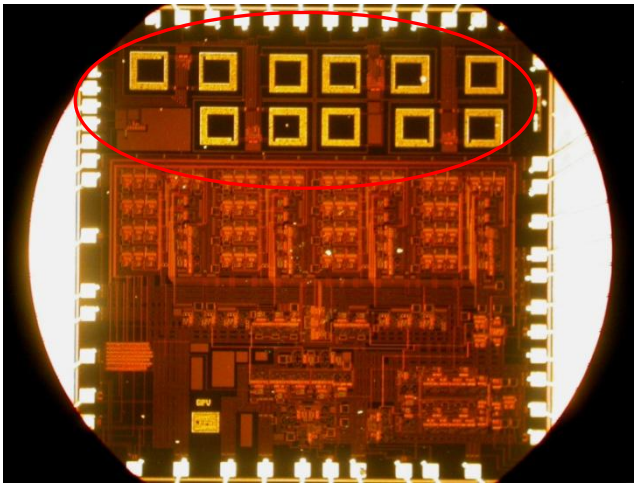

Figure 75. Zoomed in photo of measured IC prototype.

From Section 3.5, it was decided to use the QFN-56 package to encapsulate the IC, and the advantages of this package are also discussed in Section 3.5. A photograph of the final prototype, as enclosed in the QFN-56 package, is given in Figure 76.

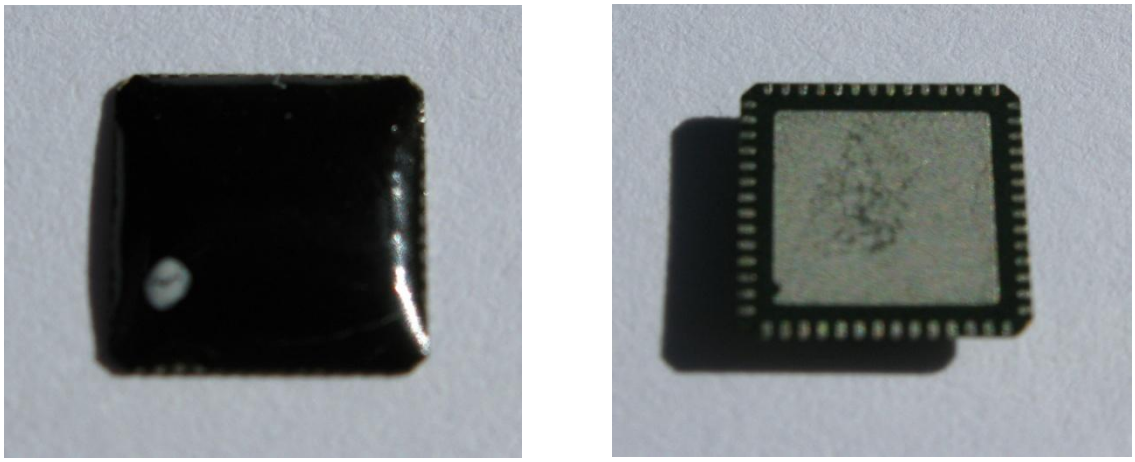

Figure 76. Photograph of QFN-56 package.

More photos of the prototyped IC are provided in Appendix B.

5.4 PARAMETRIC ANALYSIS

After the simulation and prototype results were completed and the hypothesis that phase noise can be improved by introducing tail-current shaping into the circuit was proven feasible, it was decided to find a combination of parameter values for the components in the full VCO circuit (see Figure 61), to further improve the phase noise. The original phase noise rating for the VCO circuit of -108.6 dBc/Hz at a 1 MHz offset frequency from the carrier felt a bit low and it was embarked on to improve this figure. Although this does not change anything regarding

the original hypothesis, this result can be used in a different process (not the AMS S35D4M5 process) where expected phase noise ratings are better (especially in smaller technologies).

Parametric analysis was conducted to find the optimum dimensions or values for the components used in the circuit. Parametric analysis implies setting up the software to change certain parameters in specified intervals, and the CAD software then generated results based on each analysis. The amount of steps or intervals used in each analysis was carefully planned, as the total amount of intervals can easily become extremely large and time consuming. This is the main reason why all of the parameters in the circuit could not be changed in one, large, parametric sweep, as the amount of computing could result in days of simulating, and the computer resources would require the use of computing clusters. This can be investigated in future works.

Table 30 summarizes the component parameters that were changed during each of the parametric analysis simulations done. This table specifies the default values of the components. The default values are actually obtained from earlier mathematical results (see Chapter 4), which was used to create the main simulation profile (and eventually the prototype IC) used to prove the hypothesis. These values were then altered in ten different parametric analysis simulations, to find a better combination of component dimensions for improved phase noise performance, not necessarily mathematically justified (in this dissertation).

Table 30. Parametric analysis default (starting point) values.

Component	Parameter	Value
NMOS (active) M_3	Width	50 µm
	Length	0.6 µm
NMOS (left) M_1	Width	20 µm
	Length	0.5 µm
NMOS (right) M_2	Width	20 µm
	Length	0.5 µm
BJT (left) T_1	Area	4.8 μm^2
BJT (right) T_2	Area	4.8 μm^2
V_{TUNE}	Voltage	1 V

From Table 30, the components that were altered are the dimensions (width and length) of the three CMOS transistors used in the design of the tail-current source (see Section 4.1.2), the areas of the emitters of the two bipolar switching transistors used in the VCO, and the tuning

voltage connected at the LC tank circuit varactors, to find the optimum point for the tuning voltage where phase noise performance is at its best. Default values for each parameter is given in this table, and these serve as starting or reference point for all parametric analysis simulations. As a reminder, the phase noise performance of the VCO circuit using these default values, in simulation, was -108.6 dBc/Hz at a 1 MHz offset from the 5 GHz carrier.

The first set of alterations to the default parameters, are the width dimensions of the two mirrored CMOS transistors in the current source. These transistors have the same dimensions (width and length) to ensure the current (and hence the gate-source voltage) through each transistor is the same. A parametric analysis of six steps, with the width ranging between the values of 5 µm and 50 µm were done. The width of these transistors can also play a large role in the noise performance of the circuit. Not only does the increase in transistor width reduce the equivalent noise charge ratio in the transistor by increasing the input capacitance, it also reduces the transistor thermal noise due to increased transconductance and power consumption in the transistor [60]. From [60] the optimal width of the transistor can be found with (67)

$$Q(W) = ENC(W)P(W) \tag{67}$$

where *Q(W)* is the transistor width, *ENC(W)* is a geometric sum of the transistor flicker noise and the transistor channel noise contribution, and *P(W)* is the power consumption versus the input transistor channel. Further studies can be done on this phenomenon, but for this dissertation, mathematical analysis of this was excluded, and the parametric analysis serves only as a guideline for the optimum transistor width.

Table 31. Parametric analysis 1 – variable current source NMOS width.

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width	50 µm			
	Length	0.6 µm			
NMOS (left) M_1	Width		5 – 50 µm	6	20 µm
	Length	0.5 µm			
NMOS (right) M_2	Width		5 – 50 µm	6	20 µm
	Length	0.5 µm			
BJT (left) T_1	Area	4.8 µm^2			
BJT (right) T_2	Area	4.8 µm^2			
V_{TUNE}	Voltage	1 V			
Best obtainable phase noise			- 108.5 dBc/Hz		

The optimum phase noise obtained in this analysis was slightly lower (only 0.1 dBc/Hz at the 1 MHz offset) and the width dimensions of 20 µm were highlighted as the optimum values.

At this optimum width of these two transistors, the next parametric analysis was done on the lengths of these transistors. In seven intervals, the lengths of both transistors were changed from minimum length (0.35 µm) to 1 µm.

Table 32. Parametric analysis 2 – variable current source NMOS length.

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width	50 µm			
	Length	0.6 µm			
NMOS (left) M_1	Width	20 µm			
	Length		0.35 – 1 µm	7	1 µm
NMOS (right) M_2	Width	20 µm			
	Length		0.35 – 1 µm	7	0.5667 µm
BJT (left) T_1	Area	4.8 μm^2			
BJT (right) T_2	Area	4.8 μm^2			
V_{TUNE}	Voltage	1 V			
Best obtainable phase noise			- 107.2 dBc/Hz		

From these results, no conclusive theories could be formed as to what the size of the transistor lengths should be, as the decreased phase noise performance (-107.2 dBc/Hz at 1 MHz) with different length values (1 µm and 0.566 µm) proved inconclusive.

To expand on the first set of parametric results (Table 31), the width of the 2 CMOS transistors (from which an optimum of 20 µm) was established, were now again under scrutiny. The goal was now to find the exact value (close to, or exactly 20 µm) for which phase noise performance could be improved on. Therefore, a new analysis, in six equal steps or intervals between 18 µm and 22 µm were conducted. For this analysis though, a third parameter were change in accordance with the first two (previous results, not documented here, allowed that this parameter could be added). The CMOS transistor used in the current mirror, which was connected as an active resistor, was also changed. The length of this transistor was kept constant, and the width was changed in six steps between 30 and 70 µm. This would effectively entail that the current in the circuit would change slightly, but careful monitoring was still done to ensure that the current does not fluctuate to a large extend (the length of the transistor could be changed to compensate for the fluctuations in current). The values that were changed are summarized in Table 33.

Table 33. Parametric analysis 3 – variable current source / active NMOS width.

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width		30 – 70 µm	6	54 µm
	Length	0.6 µm			
NMOS (left) M_1	Width		18 – 22 µm	6	18.8 µm
	Length	0.5 µm			
NMOS (right) M_2	Width		18 – 22 µm	6	19.6 µm
	Length	0.5 µm			
BJT (left) T_1	Area	4.8 µm^2			
BJT (right) T_2	Area	4.8 µm^2			
V_{TUNE}	Voltage	1 V			
Best obtainable phase noise			- 108.7 dBc/Hz		

From Table 33, a slight improvement of 0.1 dBc/Hz at 1 MHz offset with optimum values of transistor width can be noted. Again, no real gain on phase noise performance was achieved yet, so further analysis was conducted.

In the following analysis given in Table 34, the optimum CMOS transistor widths of the two mirrored transistors (18.8 µm and 19.6 µm) were used, and the optimum combination of the transistor connected as an active resistor was determined. Again, the influence on the current supplied to the circuit was monitored, but the overall effect on phase noise was measured, as the difference in current does effectively change the design, but was ignored for this simulation.

Table 34. Parametric analysis 4 – variable active NMOS width / length.

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width		30 – 70 µm	10	60 µm
	Length		0.35 – 1 µm	10	0.639 µm
NMOS (left) M_1	Width	18.8 µm			
	Length	0.5 µm			
NMOS (right) M_2	Width	19.6 µm			
	Length	0.5 µm			
BJT (left) T_1	Area	4.8 µm^2			
BJT (right) T_2	Area	4.8 µm^2			
V_{TUNE}	Voltage	1 V			
Best obtainable phase noise			- 108.6 dBc/Hz		

At an optimum channel width of 60 µm and length of 0.639 µm, the phase noise stayed constant at the starting value of -108.6 dBc/Hz at a 1 MHz offset. These values are close to the default values, and the current in the source did not change significantly, so these values were used from this point forward, although no real gain in phase noise were yet achieved.

The next components were looked at were the HBTs present in the VCO. The area of the emitters of the transistors could also play a role in the phase noise performance of the complete circuit, as the fluctuations in the number of carriers due to varying emitter lengths differ and hence the noise present in these devices. An important aspect to remember is that the area of the transistor is related to the length of the emitter ($AREA = L / L_0$) as given in Section 3.2.2. The area (or length) of the transistors were changed in tandem, in ten equal steps between 0.2 μm^2 and 14 μm^2 from the default of 4.8 μm^2.

Table 35. Parametric analysis 5 – variable switching transistor area.

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width	60 µm			
	Length	0.63µm			
NMOS (left) M_1	Width	18.8 µm			
	Length	0.5 µm			
NMOS (right) M_2	Width	19.6 µm			
	Length	0.5 µm			
BJT (left) T_1	Area		0.2 – 14 μm^2	10	4.8 μm^2
BJT (right) T_2	Area		0.2 – 14 μm^2	10	4.8 μm^2
V_{TUNE}	Voltage	1 V			
Best obtainable phase noise			- 108.6 dBc/Hz		

No real advantage was gained from this analysis, and the phase noise was still pinned down at -108.6 dBc/HZ at a 1 MHz offset. However, by fiddling around a bit more, it was noted that an improvement in phase noise performance could actually be achieved by altering the HBT emitter lengths, in conjunction with the width of the active resistor. Table 36 summarizes the change made in the next analysis, where the emitter lengths were varied equally in ten steps between 2.4 and 9.6, and the width of the active resistor was changed also in ten steps between 50 µm and 65 µm, where the change in current was minimal.

Table 36. Parametric analysis 6 – variable switching transistor area.

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width		50 – 65 µm	10	65 µm
	Length	0.6 µm			
NMOS (left) M_1	Width	18.8 µm			
	Length	0.5 µm			
NMOS (right) M_2	Width	19.6 µm			
	Length	0.5 µm			
BJT (left) T_1	Area		2.4 – 9.6 μm^2	10	5.6 μm^2
BJT (right) T_2	Area		2.4 – 9.6 μm^2	10	5.6 μm^2
V_{TUNE}	Voltage	1 V			
Best obtainable phase noise			- 109.3 dBc/Hz		

The results showed a relatively large increase in phase noise performance of the circuit. A total value of -109.3 dBc/Hz at a 1 MHz offset was obtained, which was the best results thus far. The optimum emitter areas were recorded at 5.6 μm^2, where the slight increase in the width of the active resistor to 65 µm also contributed to this figure.

With the areas set, the width of the active resistor was now fine tune, in 15 steps within the range of 60 µm to 75 µm.

Table 37. Parametric analysis 7 – variable active NMOS width.

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width		60 – 75 µm	15	66.43 µm
	Length	0.6 µm			
NMOS (left) M_1	Width	18.8 µm			
	Length	0.5 µm			
NMOS (right) M_2	Width	19.6 µm			
	Length	0.5 µm			
BJT (left) T_1	Area	5.6 μm^2			
BJT (right) T_2	Area	5.6 μm^2			
V_{TUNE}	Voltage	1 V			
Best obtainable phase noise			- 109.4 dBc/Hz		

The result (with a 0.1 dBc/Hz increase in phase noise at 1 MHz), was that a rather constant transistor width of around 66 µm would be kept.

Further analysis (not documented here) proved that a tuning voltage of 1.162 V would result in an optimum phase noise figure. Now, with the dimensions of the active resistor pinned, as well as the areas of the HBTs, the two CMOS mirrored transistors were again changed to find the optimum value based on the new values of the other components. The widths and lengths of these components were fine tuned around the previously obtained optimum values. The widths range between 18 µm and 22 µm, and the lengths between 0.35 µm and 1 µm.

Table 38. Parametric analysis 8 – variable current source NMOS width / length.

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width	66 µm			
	Length	0.6 µm			
NMOS (left) M_1	Width		18 – 22 µm	10	19.33 µm
	Length		0.35 – 1 µm	10	0.5 µm
NMOS (right) M_2	Width		18 – 22 µm	10	19.33 µm
	Length		0.35 – 1 µm	10	0.5 µm
BJT (left) T_1	Area	5.6 μm^2			
BJT (right) T_2	Area	5.6 μm^2			
V_{TUNE}	Voltage	1.162 V			
Best obtainable phase noise			- 109.4 dBc/Hz		

At a constant phase noise of -109.4 dBc/Hz at a 1 MHz offset, the optimum values of these 2 transistors were found at about 19.33 µm for the widths, and 0.5 µm for the lengths.

Finally, a parametric analysis on most of the parameters were done, with some educated guesses as to what parameters have the largest effect, and between what ranges these parameters should be changed. Table 39 summarizes this process, and within these ranges, the phase noise performance could actually be improved from the previous record of -109.4 dBc/Hz at a 1 MHz offset.

Table 39. Parametric analysis 9 – variable (multiple parameters).

Component	Parameter	Value	Range	# of steps	Optimum
NMOS (active) M_3	Width		58 – 68 µm	10	68 µm
	Length	0.6 µm			
NMOS (left) M_1	Width		18 – 22 µm	10	22 µm
	Length	0.5 µm			
NMOS (right) M_2	Width		18 – 22 µm	10	22 µm
	Length	0.5 µm			
BJT (left) T_1	Area		2.4 – 9.6 μm^2	10	7.2 μm^2
BJT (right) T_2	Area		2.4 – 9.6 μm^2	10	7.2 μm^2
V_{TUNE}	Voltage	1.162 V			
Best obtainable phase noise			- 110.2 dBc/Hz		

The nominal values of all component parameters to obtain a final phase noise rating for the VCO of -110.2 dBc/Hz at a 1 MHz is given in Table 40. Note that the oscillation frequency of the VCO with these parameters used was at 4.9066 GHz, which is still relatively close to the desired 5 GHz goal. It must however be stressed that the changes that occurred in current ratings, power and voltage outputs, and gate-source voltages were disregarded, with the sole purpose of this exercise to improve the phase noise performance, while maintaining the

operating frequency within the 5 GHz range. Thus the values of the components in the LC tank circuit were not changed, as these components influence the operating frequency, and the inductor for example could not be changed as the standard inductor with the highest *Q*-factor provided by AMS was already chosen.

Table 40. Parametric analysis – best obtainable phase noise component values.

Component	Parameter	Value
NMOS (active) M_3	Width	68 µm
	Length	0.6 µm
NMOS (left) M_1	Width	22 µm
	Length	0.5 µm
NMOS (right) M_2	Width	22 µm
	Length	0.5 µm
BJT (left) T_1	Area	7.2 μm^2
JT (right) T_2	Area	7.2 μm^2
V_{TUNE}	Voltage	1.162 V

This concludes the additional section on parametric analysis to improve phase noise performance by component scaling in the current source and VCO circuit. The results proved that the phase noise can still be increased from -108.6 dBc/Hz at 1 MHz offset to -110.4 dBc/Hz at a 1 MHz offset, while still maintaining circuit parameters to prove the hypothesis.

CHAPTER 6: CONCLUSION

6 CONCLUDING THE HYPOTHESIS

The goal of this chapter is to make a final conclusion of all the research and data gathered in this dissertation, and summarize this in a final, concluding section that emphasizes the theories and hypothesis.

6.1 INTRODUCTION

Chapters 1 and 2 were dedicated to a thorough literature review on the initial hypothesis. The hypothesis was that it was in fact possible to increase phase noise performance of an integrated VCO, without the need to change process characteristics, and by adding a filter component to the tail current source. Chapter 3 focused on the methodology of the research procedure and specified essential characteristics regarding the process that was used. Chapter 4 highlighted circuit designs that lead to Chapter 5, which documented the results to support the hypothesis.

6.2 TECHNICAL SUMMARY / CONTRIBUTION

As a result of the research conducted in this dissertation, the following lists some of the main aspects throughout the process that adhered to the steps for completing a well documented and well researched topic.

- Literature study / research on many aspects that pertain to electronic circuit and component design. Factors influencing noise performance of electronic circuits were considered. By combining the theoretical research with practical implementation practices, a prototype could be created and measured.
- VCO topologies were carefully studied and a more in depth knowledge of a VCO as a positive feedback amplifier was obtained.
- Simulation profiles were created not only on an ideal case basis, but non-ideal, intrinsic factors were also taken into account during this process. The ability to simulate a circuit, based on any theory, is a crucial part of any research project, as the ability to quantitatively prove the mathematical computations gives the researcher confidence in their theories.

- Actual IC implementation / prototyping enable a researcher an even larger advantage when it comes to circuit design. On a practical level, having the ability to prototype a design forces the researcher to double and triple check any design. Any flaw in the initial design, or even any assumption, needs to be argued before commencing with a physical design aimed for eventual mass production or commercialization, as time and money are crucial factors in this stage.
- The ability to use theoretical / simulated / measured results and use all of these to test the actual soundness and validity of the initial hypothesis is an art on its own. When these three crucial factors intersect, all possible factors that might lead to a discrepancy between values / results must be considered, and the researcher must know exactly where to look and finally find these differences, and accurately explain the reasoning if the need arises.
- The opportunity to report on research activities and present this paper [71] at a peer-reviewed conference, allows for further exposure in the research field and the opportunity to engage with fellow-researchers on their topics and fields of interest.

The contribution of this dissertation can be summarized in the fact that a LC VCO was designed in a technology that not only contains MOSFET transistors, but which is combined with the speed and low noise of HBTs. Few documented works exist that employ this technique in a SiGe BiCMOS configuration, and most of the works only employ the technique when MOSFET technology alone is used. The combination of these two types of transistors can lead to very exciting, low noise circuits, and should be actively researched. By using this technology (BiCMOS), and combining the idea of different technologies on the same die, with the fact that inexpensive, easy to implement components can be added to the circuit to improve phase noise performance, the contribution of this dissertation becomes apparent. Table 41 summarizes the technical specifications of the designed VCO.

Table 41. Technical specifications of designed VCO.

Parameter	Maximum range
Technology (process) used	AMS 0.35 µm thick metal BiCMOS
Supply voltage	3.3 V
Topology	LC Tank
Carrier frequency	5 GHz (simulated)
Improvement technique	Tail-current shaping filter
Phase noise (no improvement technique)	-105.3 dBc/Hz (simulated)
Phase noise (with improvement technique)	-108.6 dBc/Hz (simulated)
FOM (with improvement technique)	-150.393 dBc/Hz
Bandwidth	~ 500 MHz
DC power consumption	~ 6 mW
Chip dimensions	~ 2.693 mm x 0.79 mm

From Table 41 the improvement in phase noise performance can clearly be seen, when the tail-current shaping technique is employed to the default LC oscillator. The figure of merit can also be used as a comparative parameter to other works, as this parameter includes power consumption in the overall unit. For detailed information on all of the results, and how these results were obtained, refer to Chapter 5.

6.3 RECOMMENDATIONS FOR FUTURE WORK

The technique presented in this dissertation to reduce phase noise can be applied to many different technologies, topologies, and in different configurations. The overall phase noise performance of the simulated and designed VCO does not compare well to some of the high-end results that have been obtained in literature. Although some of these methods include expensive process-changing characteristics (techniques of circuit layout not supplied as a standard by the process manufacturer), the benefit of the good phase noise might overcome that.

Future studies to improve the phase noise of the basic LC configuration (of -105.3 dBc/Hz at a 1 MHz offset frequency) can be recommended. The main factor that is responsible for the poor phase noise performance is the quality factor presented by the inductor in the tank circuit. This quality factor should be improved to enable this specific VCO to operate with better performance by applying the techniques presented in [41]. Easy and inexpensive techniques to increase the quality factor is therefore still a field that require some attention, as a quality factor of around only 10, is detrimental to the circuit. At higher frequencies (10 GHz and up),

the inductors can be replaced by transmission lines, but at the lower RF tier (5 GHz), this is not yet feasible as the size (in nH) of the inductors would still be low.

Further research on the effect of the sizing of the MOS transistors in the current source on phase noise is also a very interesting subject that was touched on in this dissertation. The transistors in the current source also have a big effect on the overall phase noise performance (as is proven with this dissertation), but the sizing of these transistors are yet to be researched more thoroughly.

More extensive parametric analyses on different transistor models, for instance worst-case models, and different geometries can also be investigated in future works. These parametric analyses can be realized by using computer clusters to reduce the time that such detailed simulations may require. Valuable information regarding phase noise performance can be gained from this and improvements can be further investigated and researched, and applied to existing research.

Improvement of the output buffer circuit and impedance matching techniques is also recommended for future research. A separate study on the effect of the output buffer and matching would add significantly to the quality of measured results, as frequency drift can be reduced without jeopardizing phase noise performance.

The phase noise reduction technique proposed in this dissertation can also be expanded and applied to quadraphase and octaphase oscillators. Coupling of identical oscillators to achieve for instance quadrature signals can operate from common current sources. The current through the coupling capacitor is analyzed, where equivalent currents for each oscillator are expressed. Following similar phase analysis for each oscillator will then result in a tail-current shaping technique that incorporates each oscillator switching waveform and phase difference.

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APPENDIX A

MATLAB® CODE AND TEST CIRCUIT

Appendix A includes Matlab® code that was used to simulate phase noise and information pertaining to the test circuit used to perform measurements using the prototyped IC.

The Matlab® code that was used to simulate the mathematical model for phase noise is presented in Figure A.1. The code for the simulated phase noise was not adopted from any previous works and was created based on (11) provided in Section 2.4.2 using Matlab®. The results are plotted by varying the offset frequency (Foffset) and drawing the corresponding phase noise in dBc/Hz on a logarithmic scale.

```
grid off;                          %Switch off grid before running
Fop = 5e9;                         %Set operating frequency to 5 GHz
Foffset = 1:10e3:10e9;             %Vary the offset frequency from 1 Hz to 10 GHz in 10 kHz steps
Fcor = 260e6;                      %Set corner frequency to 260 MHz
NF = 4;                            %Set noise figure to 4
P = 5.911e-3;                      %Power consumption of 5.911 mW
k = 1.38e-23;                      %Boltzmann's constant
T = 290;                           %Operating temperature of 290 K
Ql = 8.886;                        %Loaded Q of inductor

TERM1 = ((Fop./(2.*Ql.*Foffset)).^2 + 1);        %First term of phase noise equation
TERM2 = NF*k*T/P;                                %Second term of phase noise equation
TERM3 = ((Fcor./Foffset) + 1);                   %Third term of phase noise equation
PN = 10.*log10(TERM1.*TERM2.*TERM3);             %Multiplication of all terms, answer in dB

semilogx(Foffset,PN,'Color','red', 'LineWidth',2);      %Plot phase noise in logarithmic scale

xlabel('Offset Frequency (Hz)');
ylabel('Phase Noise (dBc/Hz)');

text(1e6, PN(1 , 100),['\leftarrow 1 MHz; ',num2str(PN(100),4) ' dBc/Hz'],'FontSize',12, 'HorizontalAlignment','left')
text(100e3, PN(1 , 10),['\leftarrow 100 kHz; ',num2str(PN(10),4) ' dBc/Hz'],'FontSize',12, 'HorizontalAlignment','left')
text(10e3, PN(1 , 2),['\leftarrow 10 kHz; ',num2str(PN(2),4) ' dBc/Hz'],'FontSize',12, 'HorizontalAlignment','left')

grid on;
```

Figure A.1. Matlab® code used to simulate phase noise equation.

The results of this mathematical simulation are given in Section 5.1.4. From Figure 60, it can be noted that the results do not correspond exactly to the results obtained in schematic simulation (Section 5.1.3). This can be justified by the fact that (11) does not directly take into account the equivalent noise resistance of the tuning diode (varactor) which is also up-converted to phase noise at higher frequencies. Another limitation is that the loaded *Q*-factor of the inductor had to be estimated, and this also applies to the noise figure of the circuit. Future work on calculating the loaded *Q* and noise figure based on the noise modulation theory could be applied to this work.

The schematic layout of the test circuit is given in Figure A.2. For a detailed discussion on this design, refer to Section 4.3. The schematic design was done using Orcad® Capture®.

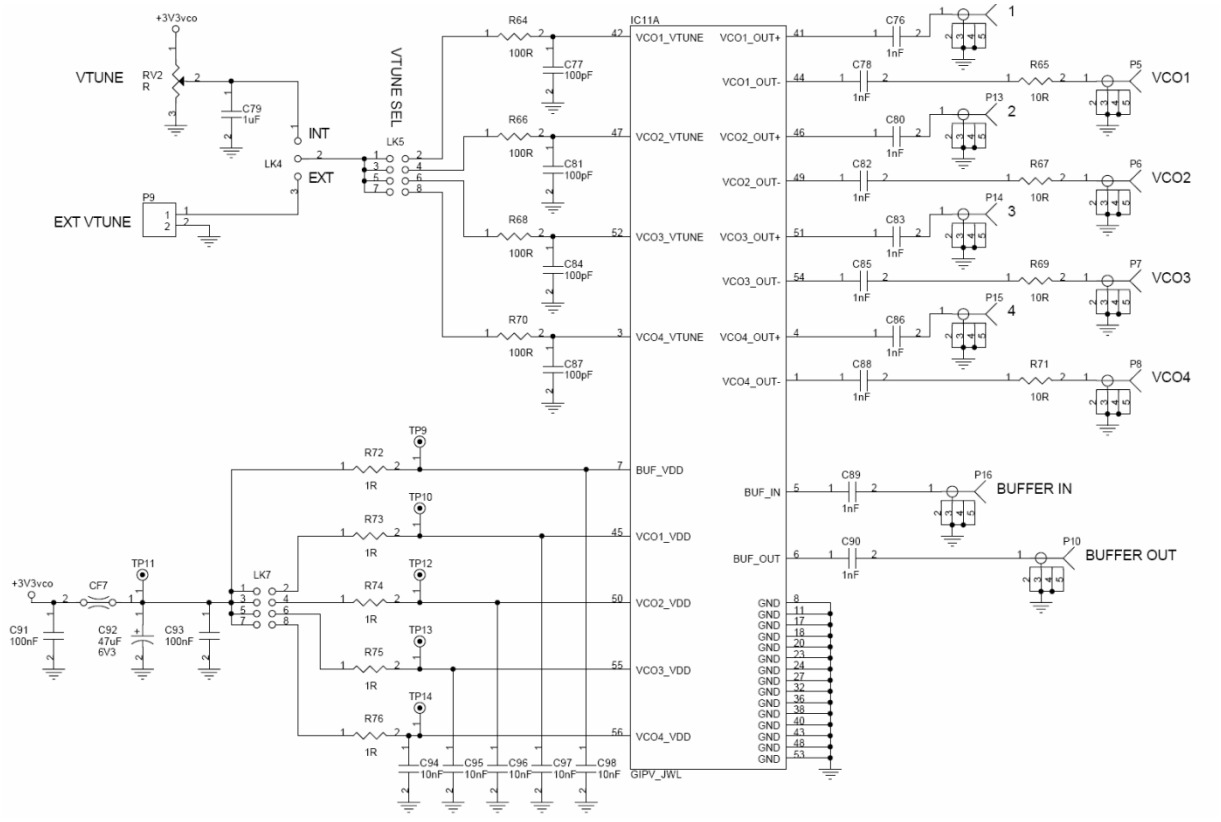


Figure A.2. Test circuit schematic layout.

A description of the test circuit schematic layout is given on the next page. This description is adopted from the description in Section 4.3 for convenience, and highlights some of the more important aspects. For a full description, refer to Section 4.3. The design of the PCB was done by a third party, therefore the placement of decoupling capacitors and protection circuitry was not simulated for performance, and assumed to have a positive influence.

The supply voltage pin of the VCO (PIN 45) receives a regulated 3.3 V supply voltage. This regulated voltage is provided by using the Texas Instruments® TPS78633DCQ voltage regulator. A high-power (1 W), 1 Ω resistor is connected to the regulator input, in series, to absorb any high current that might flow due to a short circuit, protecting the IC from these currents. Decoupling capacitors connected towards ground filter out any noise presented to the circuit at his point. CF7 is placed in series with the regulator, also to remove any high-frequency noise added to the system. Two test points are also placed on this line (TP11 and TP10) with a 1 Ω resistor (R73) in series separating them. Measuring the voltage between these two test points, allows the user to actually determine the current flowing into the supply voltage of the VCO by dividing the measured voltage by 1 Ω.

The tuning pin of the VCO (PIN 42) is used to manually adjust the frequency of operation. The regulated 3.3 V supply voltage is connected to a variable resistor (RV2), where the voltage across the resistor is fed to the pin of the IC (through a 100 Ω resistor, R64, which limits the current flowing to the IC and reduces the voltage with a factor) and used to adjust the operation frequency around 5 GHz. A 100 pF capacitor (C77) is connected at pin towards ground, to filter out high-frequency noise components.

The output pins of the VCO (PIN 41 and 44) are used to measure the output signal. The positive output signal is connected directly to the output connector (P12). It does however pass through a 1 nF capacitor (C76) to remove an added DC voltage. The negative output signal passes through an additional 10 Ω resistor.

The output signals can also be fed through the buffer circuitry designed in Section 4.1.4. The buffer receives the same supply voltage as the VCO (3.3 V regulated supply). The input to the buffer is connected to PIN5 of the IC, through a 1 nF capacitor (again removing any DC components) at P16. The output of the buffer can be measured at PIN 6 of the IC, using the connector P10.

The test circuit silkscreen layer from Mentor® PADS® is given in Figure A.3.

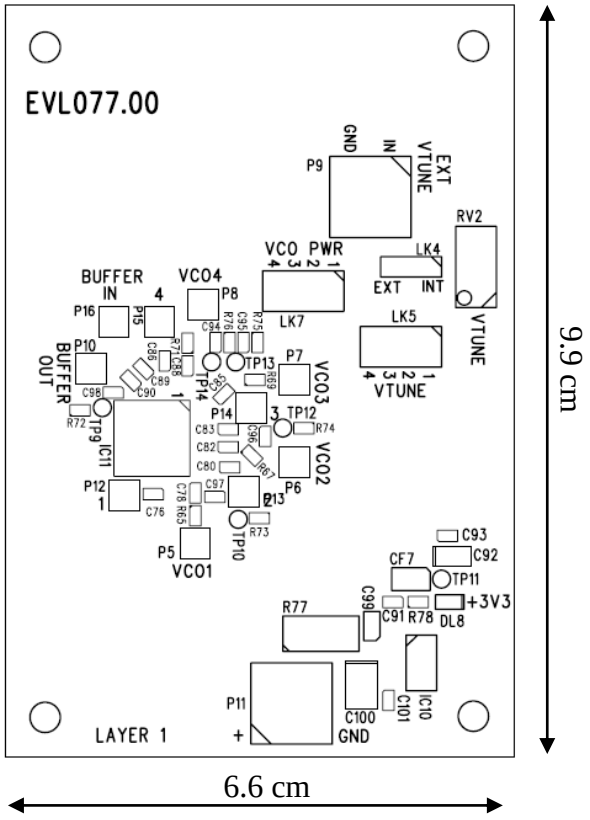


Figure A.3. Test circuit silkscreen layer.

Note that the inscription on the top left corner of Figure A.3 labelled "EVL077.00" is automatically generated as a reference or evaluation number for the blank PCB used internally by Mentor® PADS® during its construction. This number can be specified by the user, but a default code-generator creates this randomly if no input is specified. The labelling for each component was specified to simplify the soldering of the components on the PCB. The placement of the output ports were designed specifically to be as close to the IC as possible. This reduces the effect of noise appearing on the tracks of the PCB which can be converted to phase noise and have a detrimental effect on the noise performance of the IC, with the trade-off being clutter on the PCB near the IC. The DC voltage regulator was placed as far from the IC as possible, to ensure that no high currents / voltages are converted to unwanted noise in the high-frequency outputs. The placement of the tuning circuitry and potentiometers were done more arbitrarily, but some priority was given to placing these components far from the IC also to reduce noise conversion. The test circuit bill of materials is given in Figure A.4 which summarizes all of the components used in the test circuit

Item	Quantity	Reference	Part	
1	1	EVL077.00	Blank board	
2	1	CF7	NFE31PT222Z1E9L	CF1206
3	10	C76,C78,C80,C82,C83,C85, C86,C88,C89,C90	1nF	C0603
4	4	C77,C81,C84,C87	100pF	C0603
5	1	C79	1uF	C0603
6	2	C91,C93	100nF	C0603
7	1	C92	47uF 6V3	ETC-A
8	6	C94,C95,C96,C97,C98,C101	10nF	C0603
9	1	C99	1uF	C0805
10	1	C100	100uF 6V3	ETC-B
11	1	DL8	Green	LED\0805
12	1	IC10	TPS78633DCQ 3V3	SOT223-5
13	1	IC11	GIPV_JWL	QFN56
14	1	LK4	LINK-3	LINK-3
15	2	LK5,LK7	LINK-2X4A	LINK-2X4
16	10	P5,P6,P7,P8,P10,P12,P13, P14,P15,P16	MMCX	CON\MMCX\V
17	2	P11,P9	2way Term Block	TB\2P
18	1	RV2	R 3296W	VRES\A\T
19	4	R64,R66,R68,R70	100R	R0603
20	4	R65,R67,R69,R71	10R	R0603
21	5	R72,R73,R74,R75,R76	1R	R0603
22	1	R77	1R 1W	R2512
23	1	R78	330R	R0603
24	6	TP9,TP10,TP11,TP12,TP13,	Test Point	TP\1MM

Figure A.4. Test circuit Bill of Materials.

The solder-mask for the test circuit is given in Figure A.5 and the drill-drawing and accompanying legend is provided in Figure A.6. The solder-mask is related to the silkscreen layer given in Figure A.3, but shows only the markers on the PCB where the actual components were soldered, thus giving an indication of the number of pins of each component.

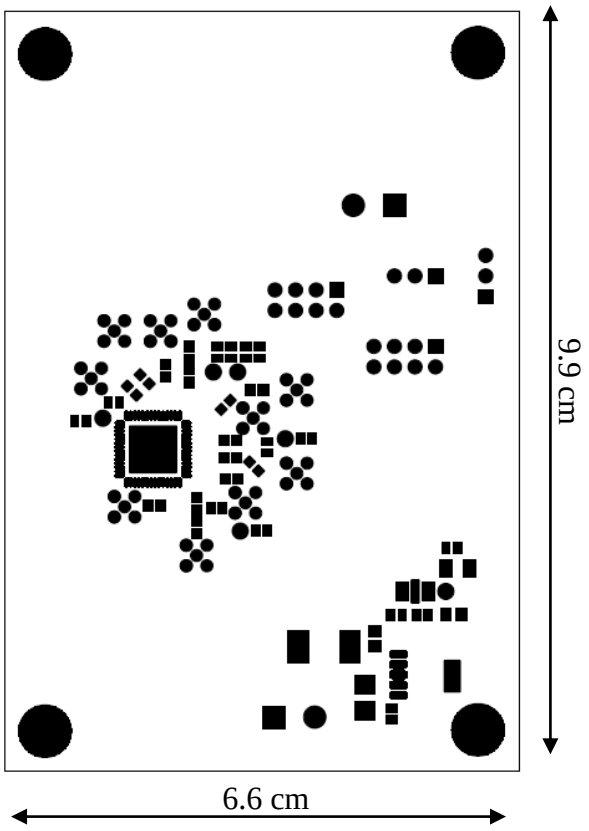
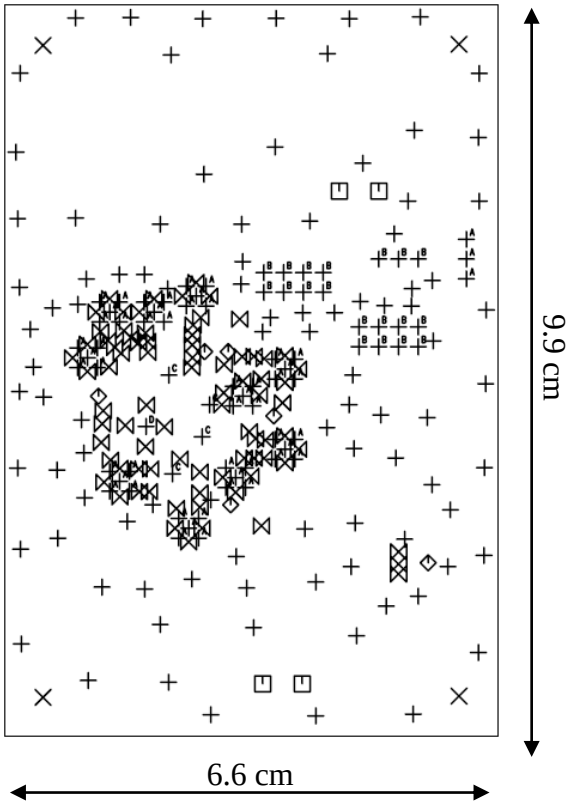


Figure A.5. Test circuit solder-mask.



SIZE	QTY	SYM	PLATED	TOL
28	94	+	YES	+/-0.0
138	4	X	YES	+/-0.0
63	4	⊡	YES	+/-0.0
39	6	◇	YES	+/-0.0
24	81	⋈	YES	+/-0.0
31	53	+A	YES	+/-0.0
35	19	+B	YES	+/-0.0
20	4	+C	YES	+/-0.0
71	1	+D	YES	+/-0.0

Figure A.6. Test circuit drill-drawing and legend.

APPENDIX B

DETAILED CIRCUIT LAYOUTS AND NETLISTS / DRC

Appendix B provides detailed circuit layouts of the prototyped IC, a bonding diagram of the QFN-56 package, and photos of the entire circuit.

A legend of the circuit layout designed in Tanner® Tools® L-Edit® is given in Figure B.1.

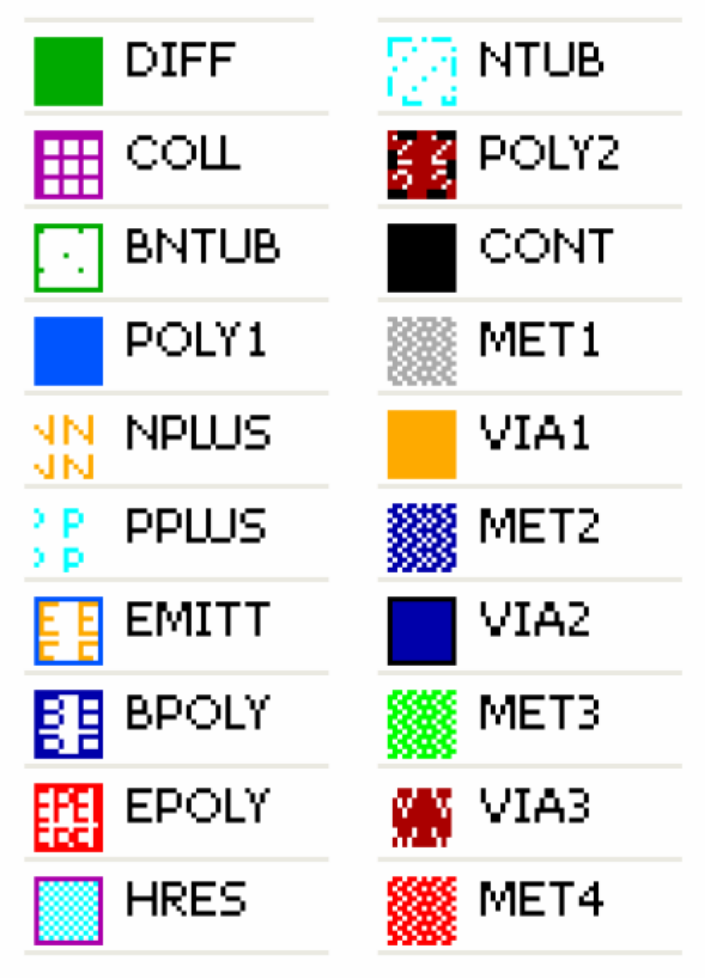


Figure B.1. Tanner® Tools® L-Edit® legend for circuit layout.

The complete circuit layout in Tanner® Tools® L-Edit® is given in Figure B.2. Note that the layout is rotated 90^{o} for a larger display. The bonding pads are also visible from Figure B.2, and this type of bonding pad is provided by [61] to reduce external noise from the IC pins.

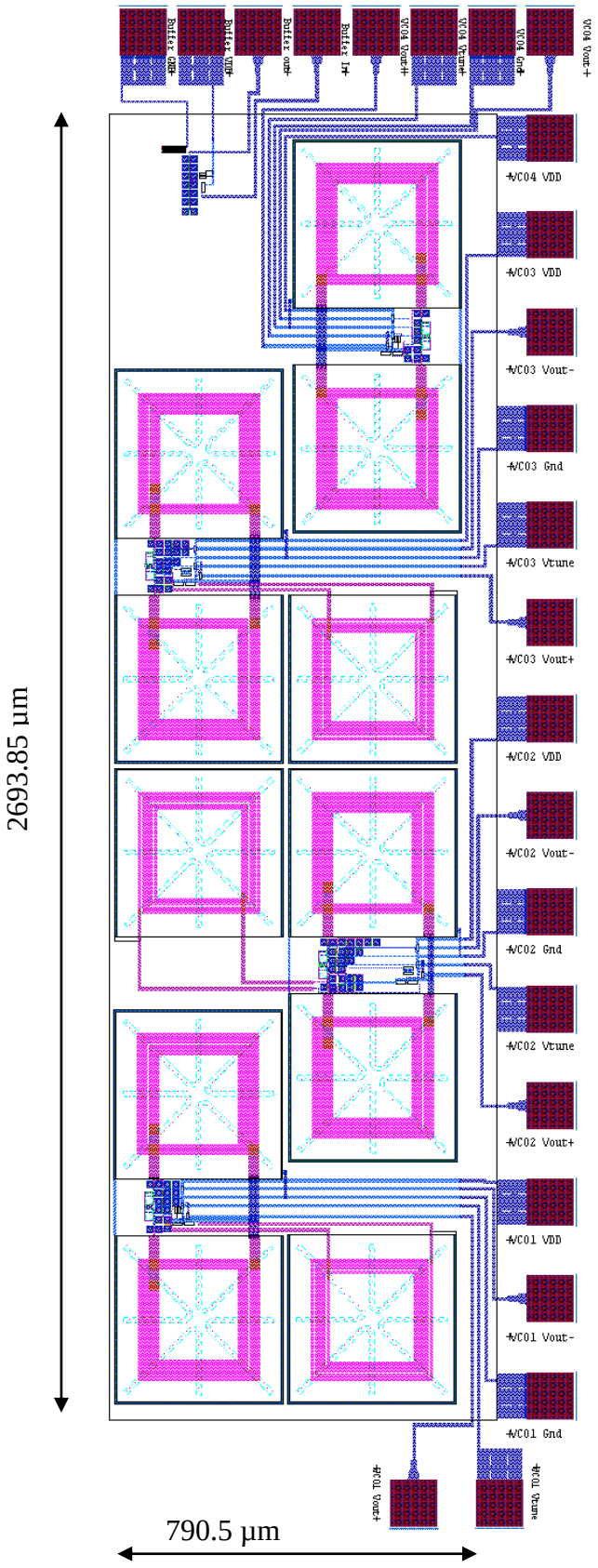


Figure B.2. Tanner® Tools® L-Edit® complete circuit layout.

The layout of each VCO is given in the figures below. VCO 1 is displayed in Figure B.3.

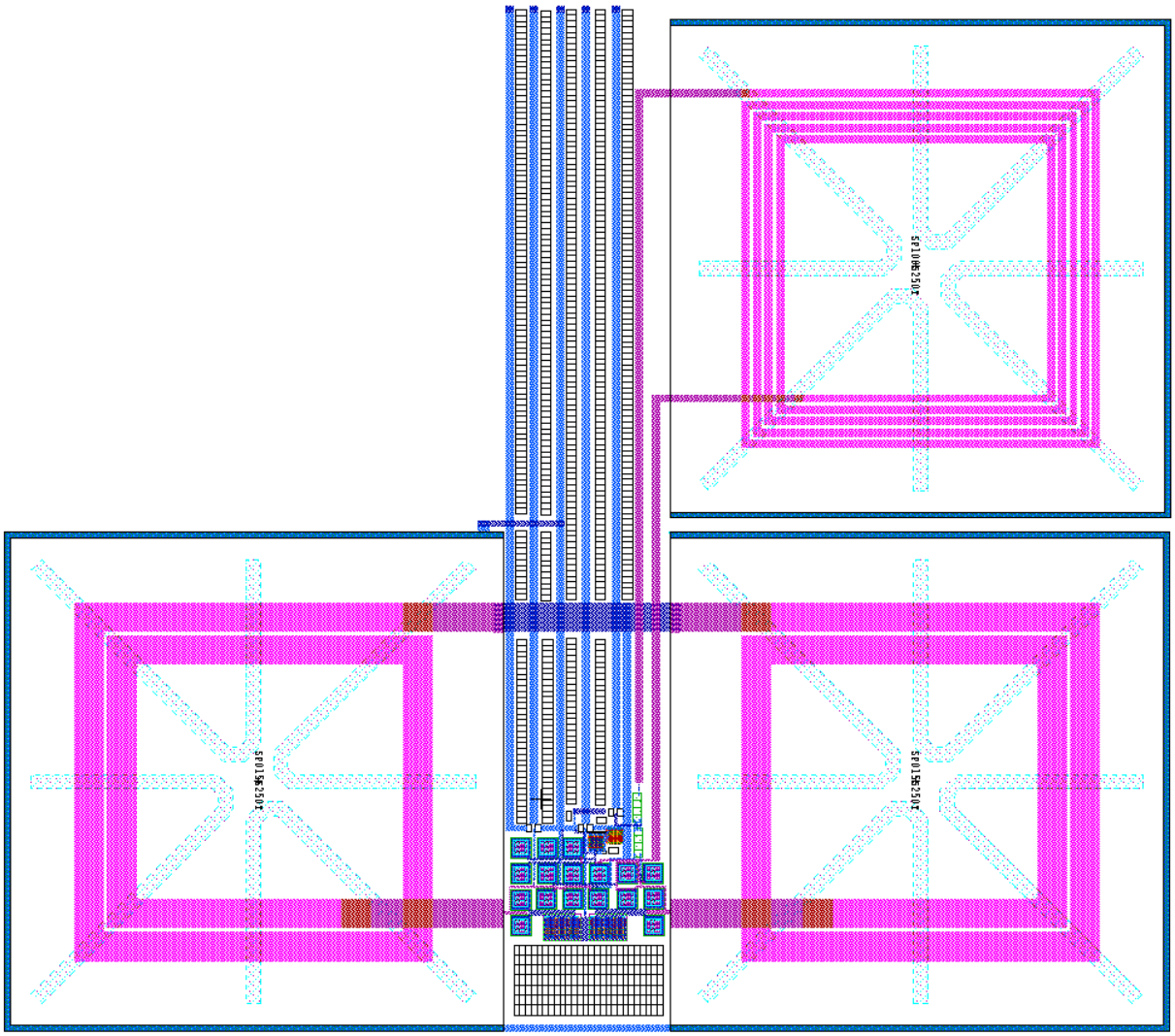


Figure B.3. Tanner® Tools® L-Edit® circuit layout of VCO 1.

Figure B.4 displays the layout of VCO 1 with the inductors removed from the frame to increase the size of the actual circuit.

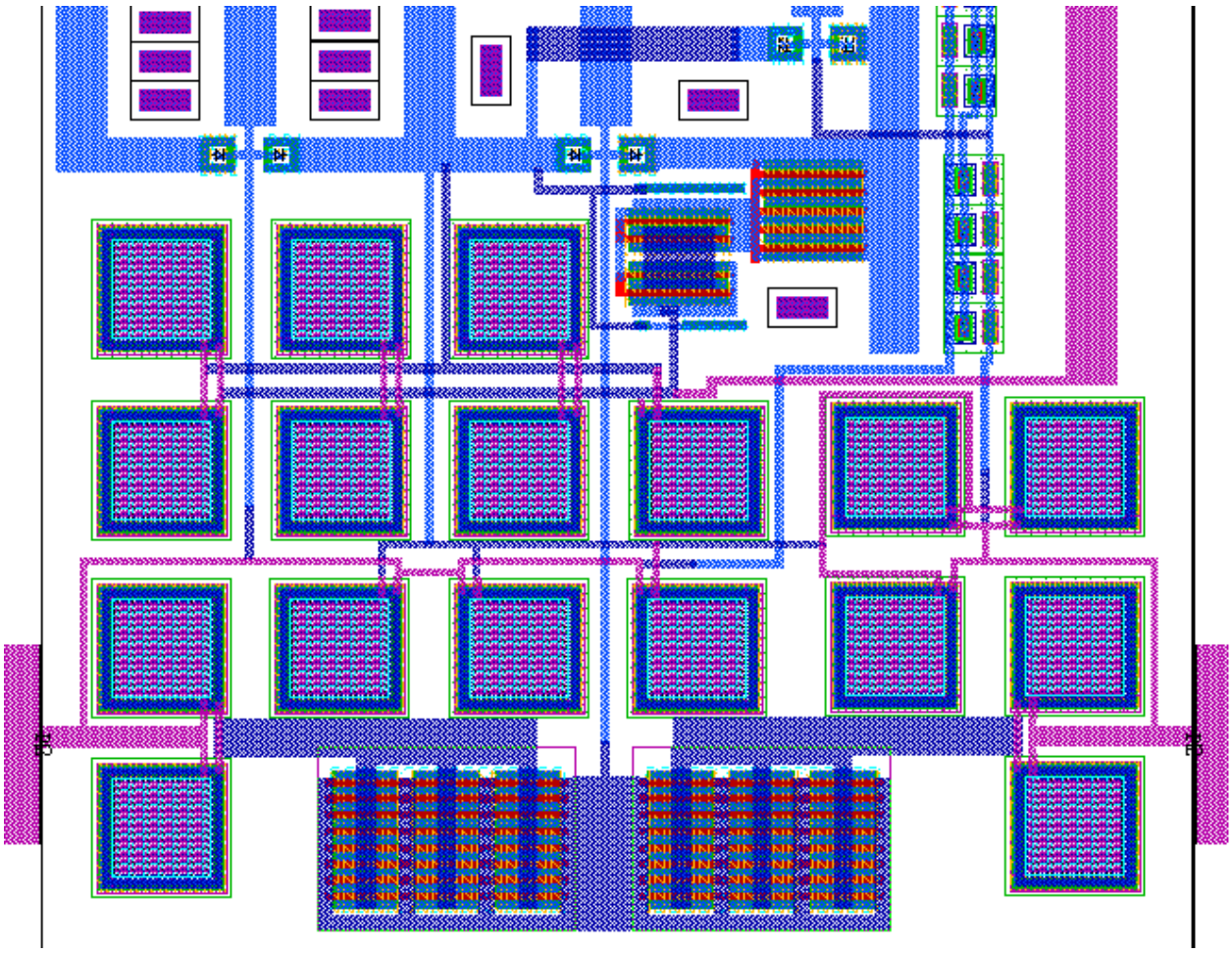


Figure B.4. Tanner® Tools® L-Edit® circuit layout of VCO 1 (inductors removed).

The Tanner® Tools® circuit layout for VCO 2 is given in Figure B.5.

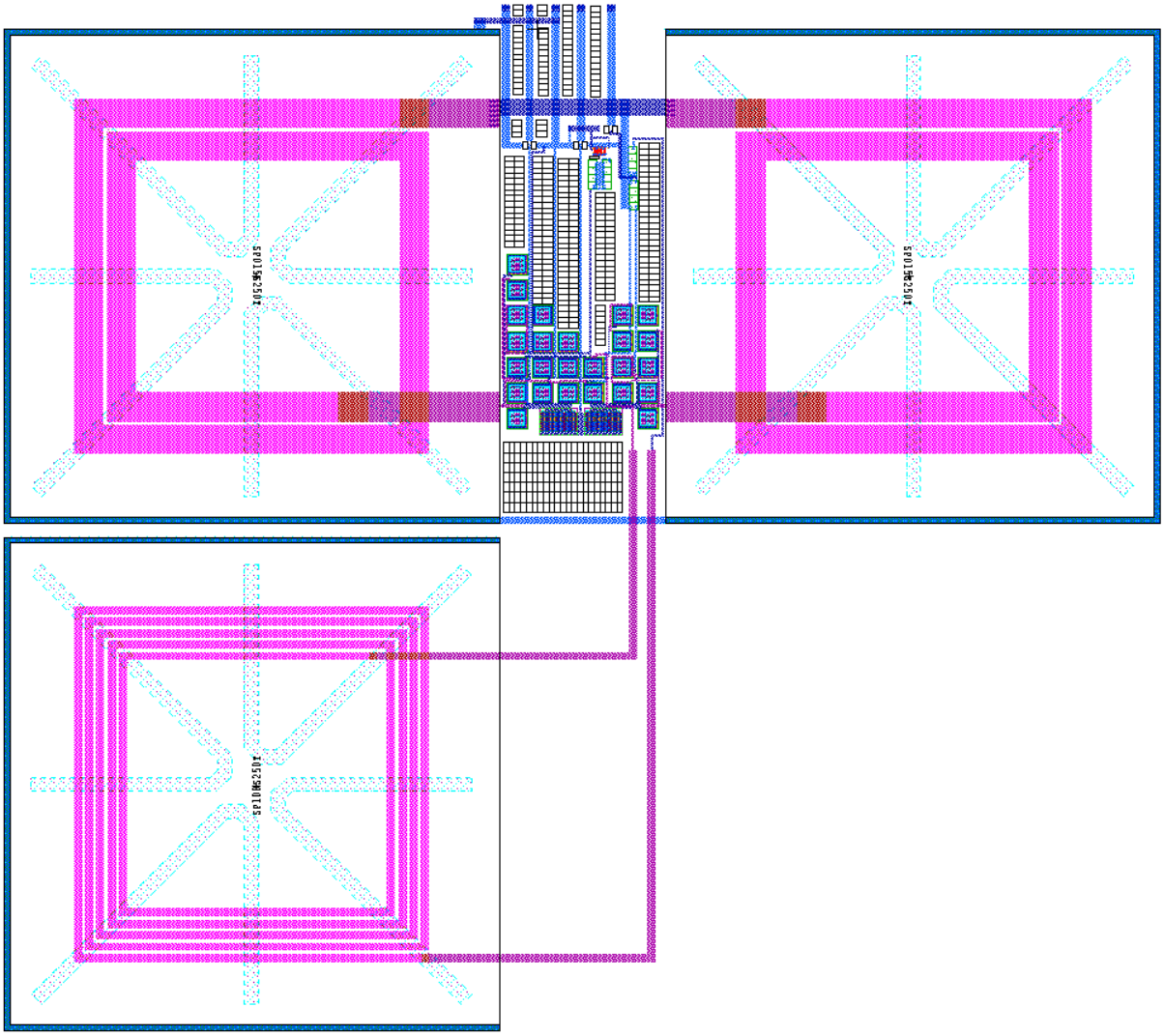


Figure B.5. Tanner® Tools® L-Edit® circuit layout of VCO 2.

Figure B.6 displays the layout of VCO 2 with the inductors removed from the frame to increase the size of the actual circuit.

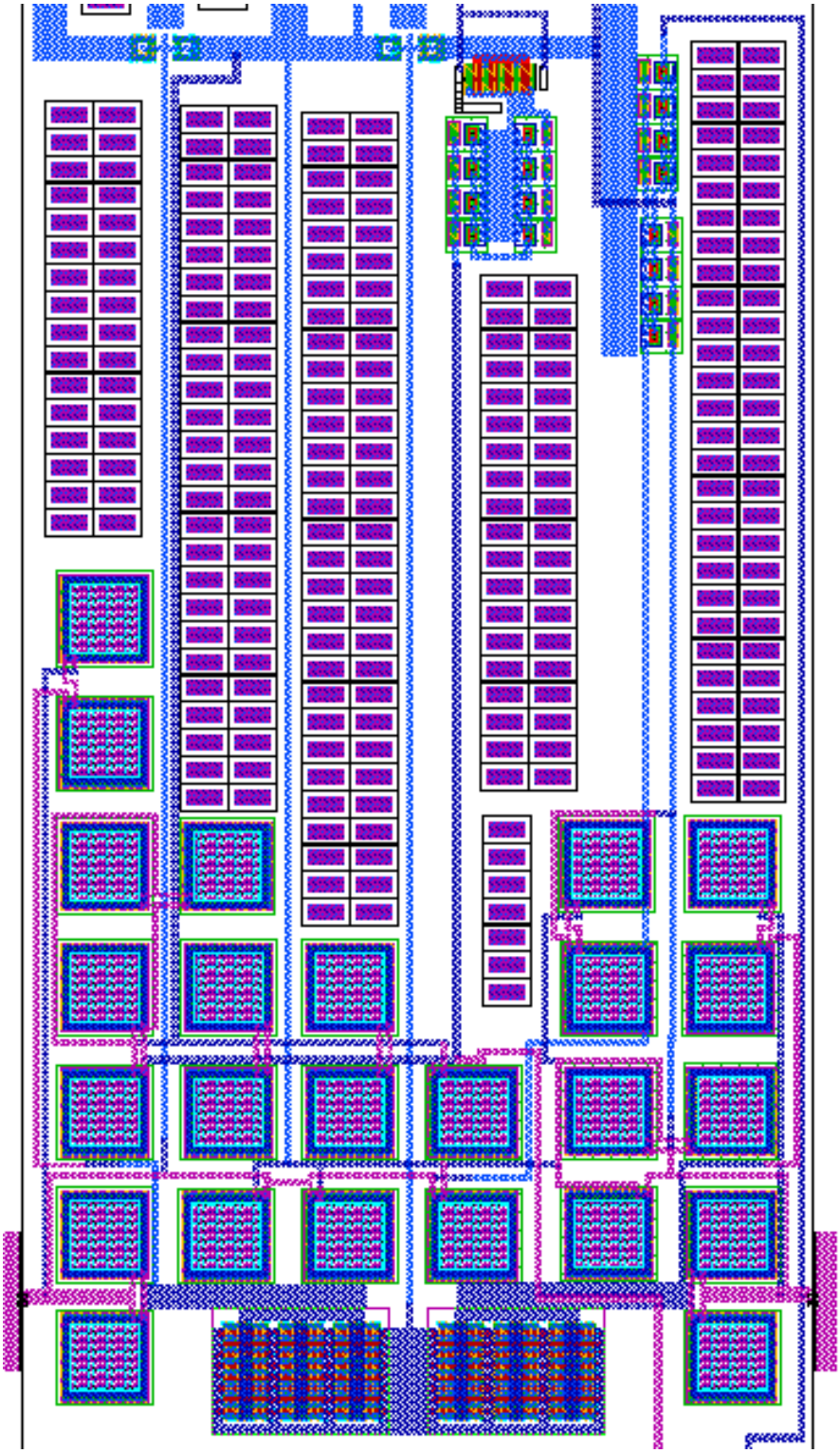


Figure B.6. Tanner® Tools® L-Edit® circuit layout of VCO 2 (inductors removed).

The Tanner® Tools® circuit layout for VCO 3 is given in Figure B.7.

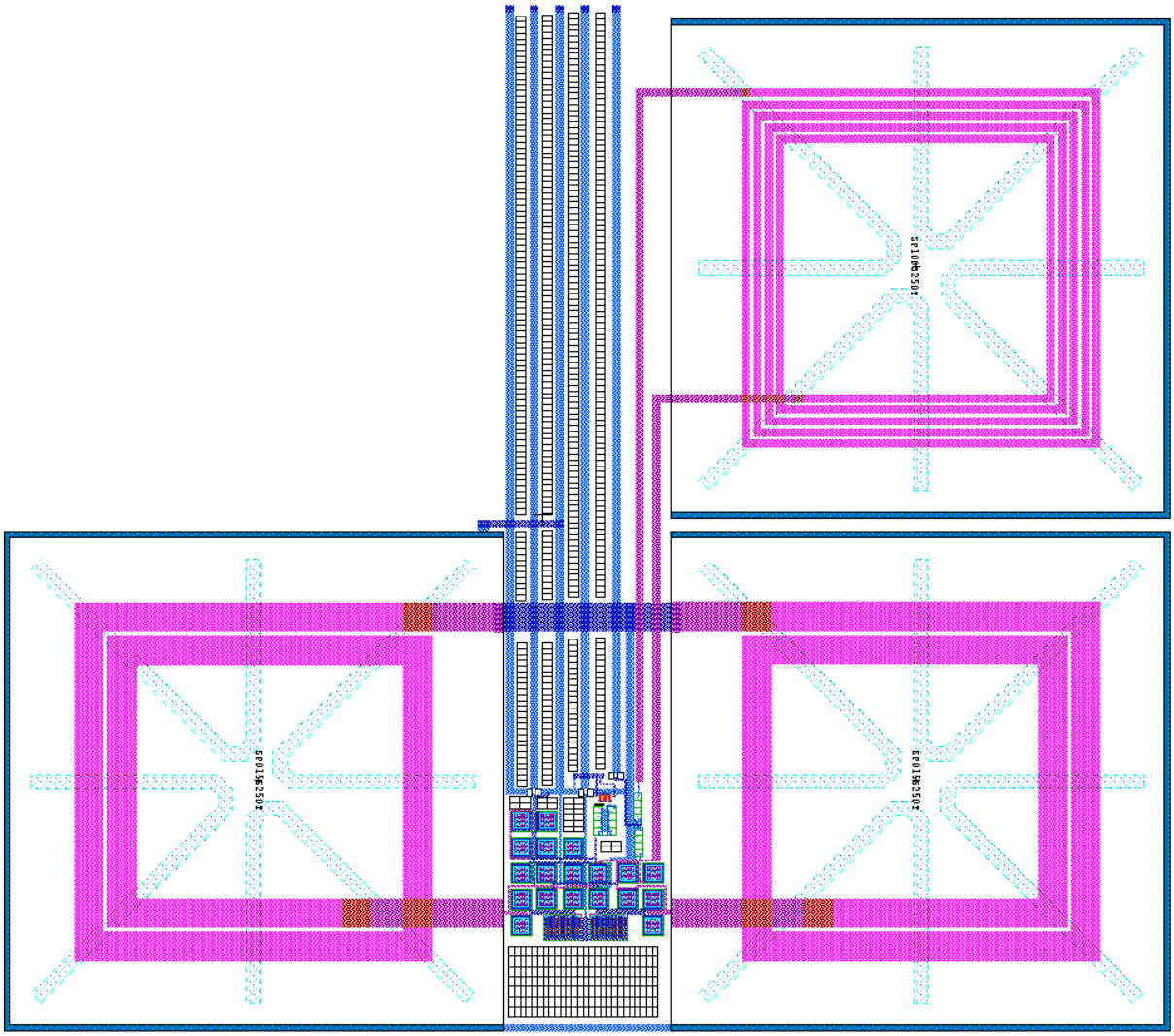


Figure B.7. Tanner® Tools® L-Edit® circuit layout of VCO 3.

Figure B.8 displays the layout of VCO 3 with the inductors removed from the frame to increase the size of the actual circuit.

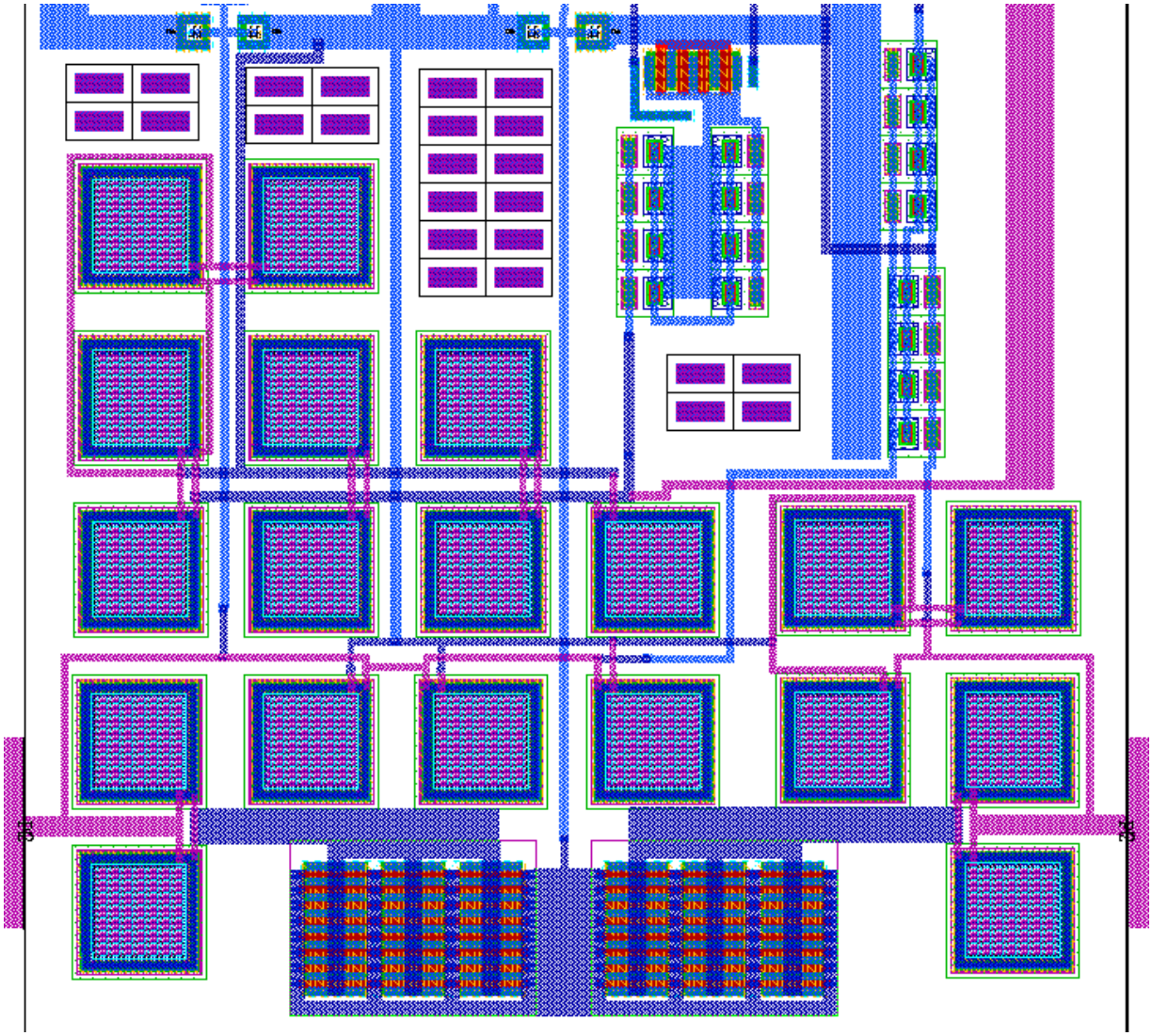


Figure B.8. Tanner® Tools® L-Edit® circuit layout of VCO 3 (inductors removed).

The Tanner® Tools® circuit layout for VCO 4 is given in Figure B.9.

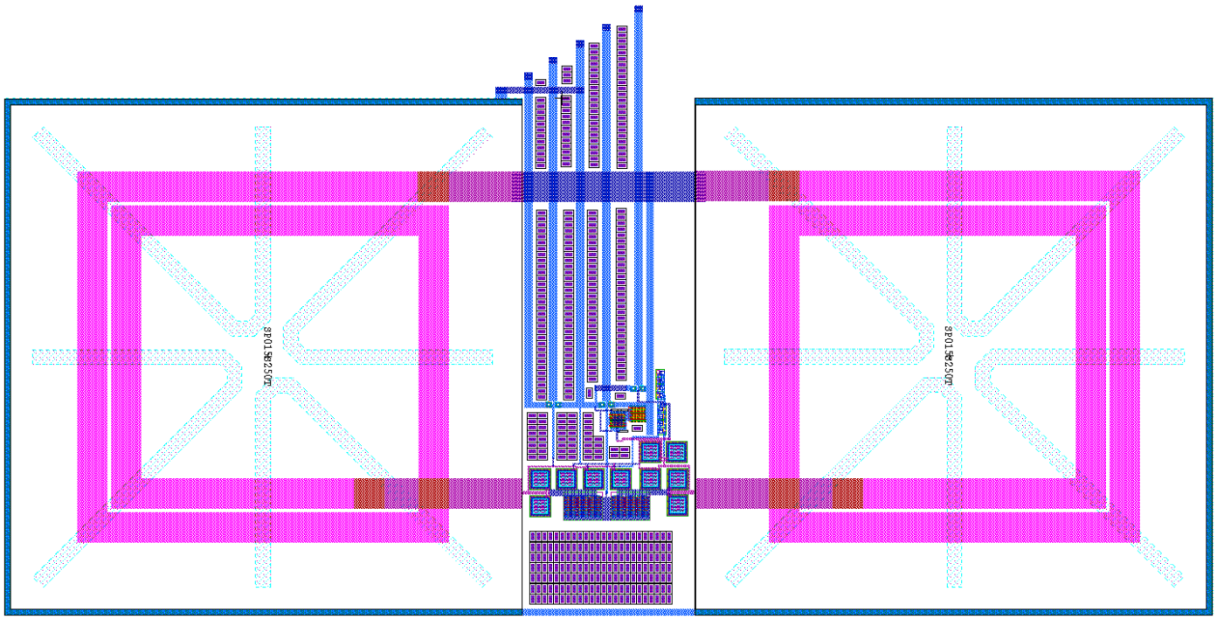


Figure B.9. Tanner® Tools® L-Edit® circuit layout of VCO 4.

Figure B.10 displays the layout of VCO 4 with the inductors removed from the frame to increase the size of the actual circuit.

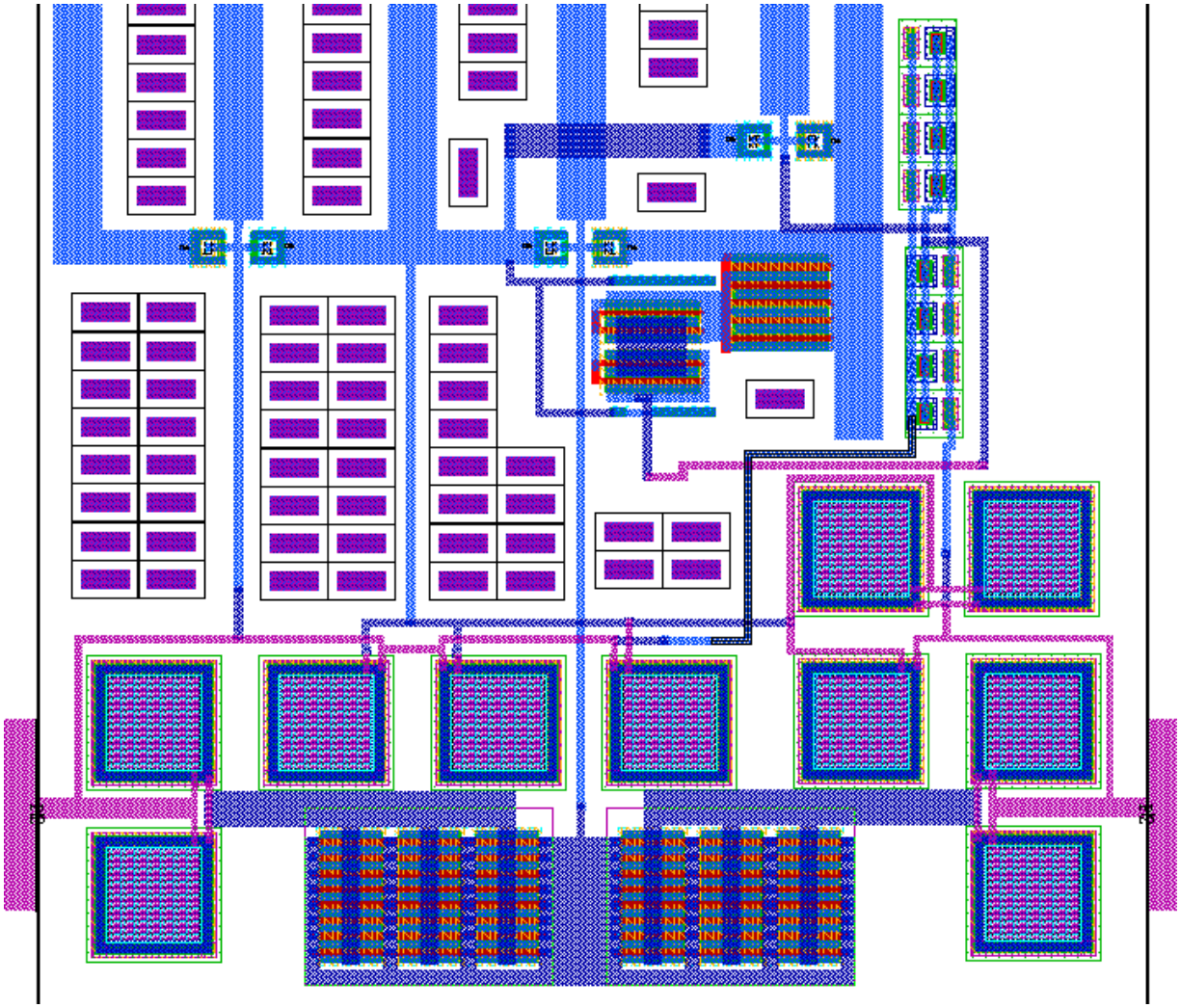


Figure B.10. Tanner® Tools® L-Edit® circuit layout of VCO 4 (inductors removed).

The Tanner® Tools® circuit layout for the MOS current source is given in Figure B.11.

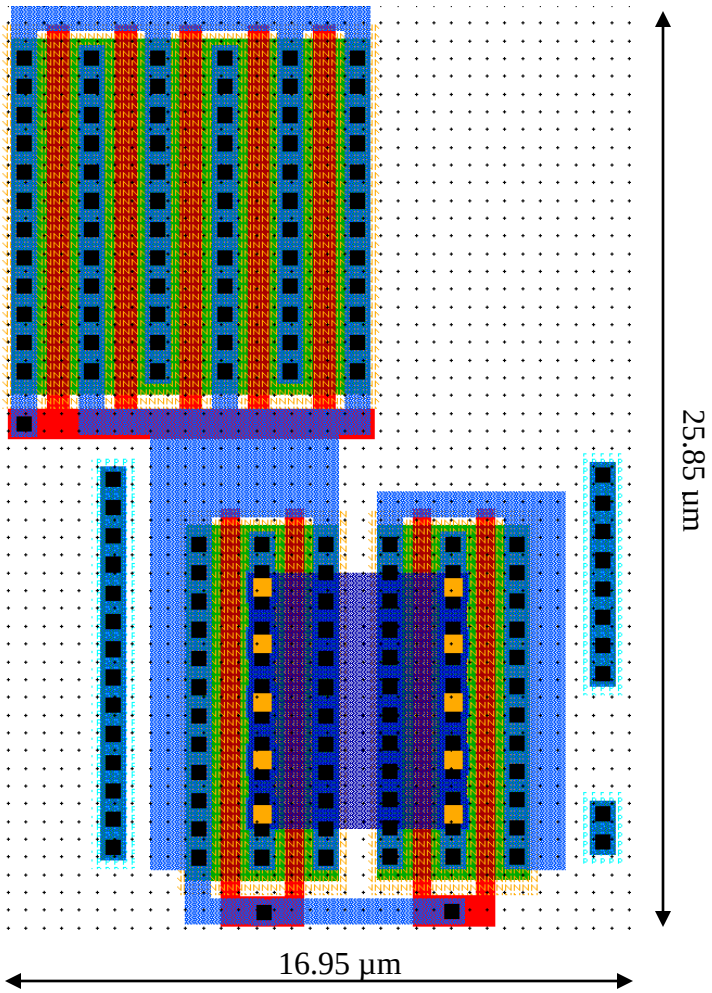


Figure B.11. Tanner® Tools® L-Edit® circuit layout of MOS current source.

For hand-analysis LVS, the netlists of some of the components in the final layout is provided here. These netlists were used to ensure that the components created in Tanner® Tools® L-Edit®, coincided with the components added in the schematic design (which is only referenced here). Firstly, the netlist for the two different NMOS transistors used in the current source is provided in Figure B.12 and Figure B.13. The netlist (Figure B.12) is the netlist of the smaller (0.5 x 20 µm) MOS transistor (seen at the bottom of Figure B.11).

```
********************************************************************************
* SPICE netlist generated by HiperVerify's NetList Extractor
*
* L-Edit Version:            L-Edit Win32 13.11.20080904.19:23:30
*
Resources\Work Folder\L-Edit VCO\ams_S35.ext
* Cell Name:                 JWL_NMOS_0_5x20
* Write Flat:                YES
********************************************************************************

.model MODN
M1 1 2 3 4 MODN l=0.5e-006 w=10e-006  $(41.5 22 42 32)
M2 3 2 1 4 MODN l=0.5e-006 w=10e-006  $(43.3 22 43.8 32)
****************************************
```

Figure B.12. Netlist used for hand-analyis LVS of 0.5 x 20 µm NMOS transistor.

From the netlist in Figure B.12, it is apparent that the 0.5 x 20 µm NMOS transistor was constructed using two transistors each with dimensions 0.5 x 10 µm, and the drain and source of each transistor connected. This technique allows for large transistors to be created in more rectangular geometries, avoiding transistors that can become very long. Therefore, it could be confirmed that the transistor designed in Tanner® Tools® L-Edit® could be used as the 0.5 x 20 µm schematic version. Figure B.13 represents the 0.6 x 50 µm transistor, which can be seen in the top section of Figure B.11.

```
********************************************************************************
* SPICE netlist generated by HiperVerify's NetList Extractor
*
* L-Edit Version:            L-Edit Win32 13.11.20080904.19:23:30
*
* TDB File Name:             C:\Documents and Settings\User\Desktop\GIPV_JWL_QFN56.tdb
* Cell Name:                 JWL_NMOS_0_6x50
* Write Flat:                YES
********************************************************************************

.model MODN
M1 1 2 1 3 MODN l=0.3e-006 w=20e-006  $(0.2 44.6 0.8 54.6)
M2 1 2 1 3 MODN l=0.3e-006 w=20e-006  $(2.1 44.6 2.7 54.6)
M3 1 2 1 3 MODN l=0.3e-006 w=20e-006  $(3.95 44.6 4.55 54.6)
M4 1 2 1 3 MODN l=0.3e-006 w=20e-006  $(5.85 44.6 6.45 54.6)
M5 1 2 1 3 MODN l=0.3e-006 w=20e-006  $(7.7 44.6 8.3 54.6)
****************************************
```

Figure B.13. Netlist used for hand-analyis LVS of 0.6 x 50 µm NMOS transistor.

The netlist provided in Figure B.13 provides evidence that this transistor was in fact not created successfully, and is the reason for the incorrect operation of the prototype. From the

netlist, it is evident that the setup created here, resulted in a short-circuit between five transistors of dimensions 0.3 x 20 µm, which can be corrected in future works.

The Tanner® Tools® circuit layout for the HBT current source is given in Figure B.14.

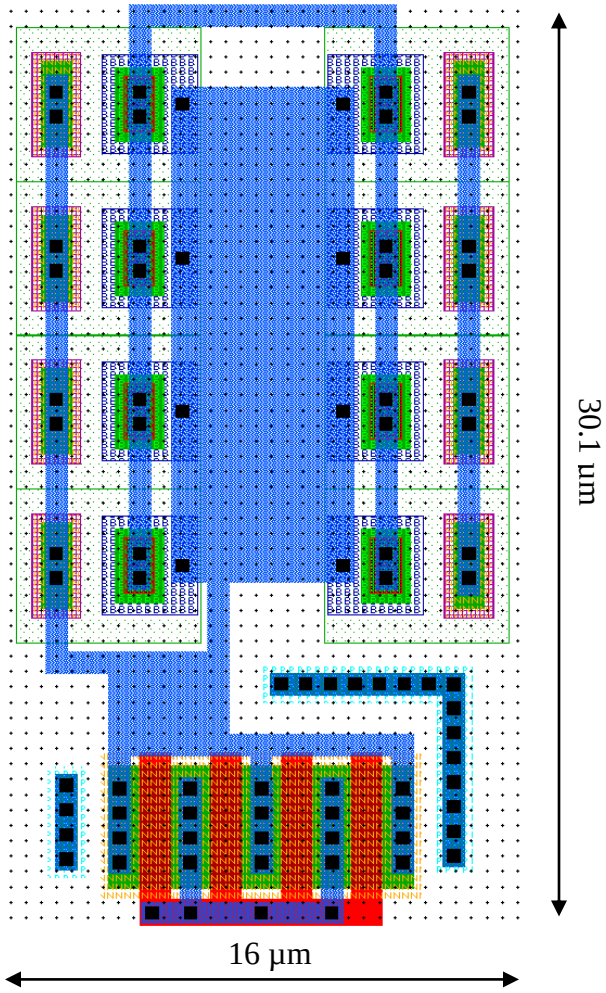


Figure B.14. Tanner® Tools® L-Edit® circuit layout of HBT current source.

The netlist of the HBT current source is not provided here, as Tanner® Tools® L-Edit® could not identify the HBT transistors in the layout. Therefore, the layout was assumed to be correct, as these HBT models were supplied by AMS and considered standard. L-Edit® could also not identify the inductors (considered these components as only a section of metal), or the CVAR component (see Section 4.2.3), therefore the netlists of these components are not provided here. The CMIM (see Section 4.2.2) layout and netlist is provided in Figure B.15 and Figure B.16 respectively, and was used to confirm hand-analysis LVS for this component.

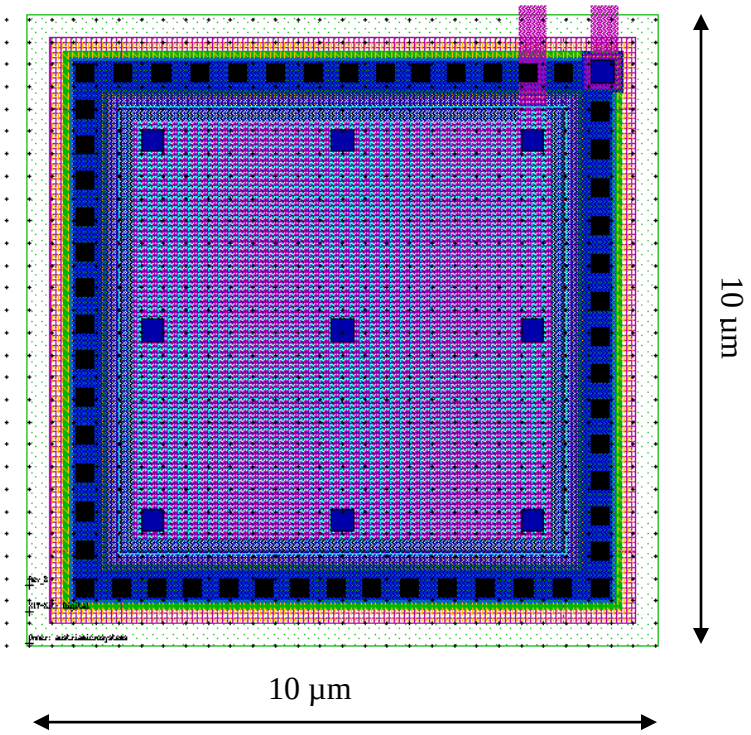


Figure B.15. Tanner® Tools® L-Edit® circuit layout of CMIM capacitor.

The netlist for the CMIM capacitor that was used to compare LVS is given in Figure B.16.

```
********************************************************************************
* SPICE netlist generated by HiperVerify's NetList Extractor
*
* L-Edit Version:            L-Edit Win32 13.11.20080904.19:23:30
*
* Cell Name:                 JWL_CMIM
* Write Flat:                YES
********************************************************************************


.model CMIM
*****************************************
.SUBCKT CMIM Plus Minus
.ENDS

X1 1 2 CMIM area=100e-012 peri=40e-006  $(26.5 19.05 36.5 29.05)
*****************************************
```

Figure B.16. Netlist used for hand-analyis LVS of 0.6 x 50 µm CMIM capacitor.

From Figure B.16, the area of the capacitor is confirmed as 0.1 pm^2 and the perimeter of 40 µm. This is consistent with the dimensions required as given is Section 4.2.2 for hand-analysis LVS.

The only DRC error that was picked up and had to be corrected in this design, is given in Figure B.17. This error pertains to a placement where the METAL 4 was placed at a 45^{o} angle, which is not permitted in this technology node. The error was corrected and the prototype could be manufactured. A figure of the actual error as displayed in Tanner® Tools® l-Edit® is not supplied here, as this error was promptly corrected and the final version of the layout did not contain the error to be illustrated here.

```
================================================================================
Rule No. 94 : MET4 not multiple 45 degrees REC002

Real Error Count : 4; Flat Error Count : 4
================================================================================

--------------------------------------------------------------------------------
Cell Name : GIPV_JWL_TOP layout 66175_I04170_01

              Cell Errors    Real Errors   Cell Placements     Environments
                   4             4              1              1
--------------------------------------------------------------------------------
Env.  Env. Placements          X1          Y1          X2          Y2

 1       1            -771.750    -1235.300    -623.300    -1136.200

Shape             Environments Status & Error Marker

       1         X1         Y1         X2         Y2

  1     X    -771.750  -1163.750  -623.650  -1137.650
  2     X    -771.650  -1235.300  -623.550  -1209.200
  3     X    -771.500  -1162.300  -623.400  -1136.200
  4     X    -771.400  -1233.850  -623.300  -1207.750

================================================================================
Rule No. 96 : INFO: hot nwell

Real Error Count : 92; Flat Error Count : 348
================================================================================
```

Figure B.17. DRC error from AMS, 45 ^{o} placement of METAL4 – corrected.

The bonding diagram of the QFN-56 diagram is given in Figure B.18.

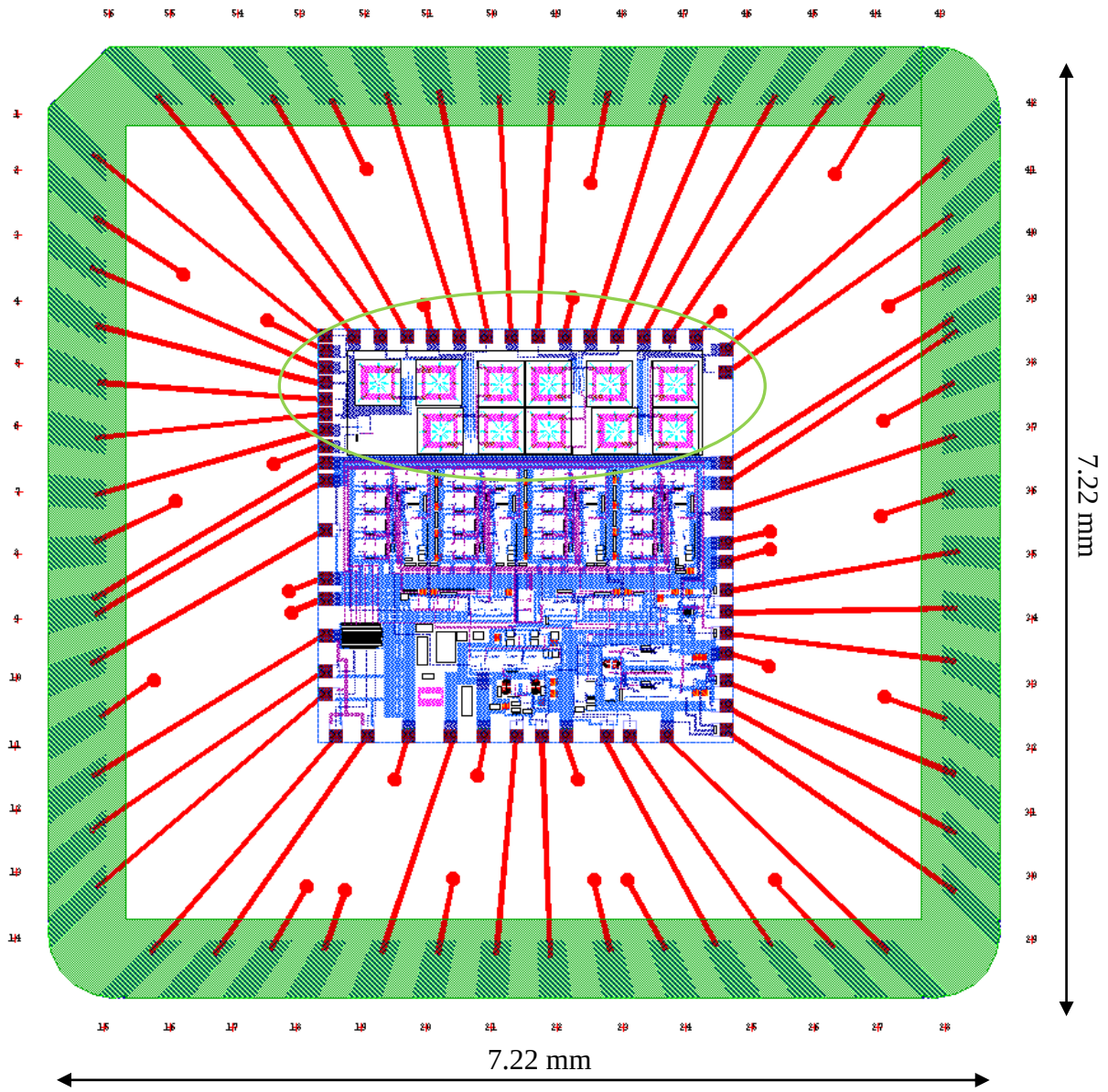


Figure B.18. Tanner® Tools® L-Edit® QFN-56 bonding diagram.

The following figures are photos of the prototyped IC taken using a microscope and a digital camera. These photos can be related to the Tanner® Tools® L-Edit® circuit layouts given in the figures above. Figure B.19 is a photograph of the entire IC. The bonding wires are also visible from this figure. Note that the top third (encircled in green) of the actual IC is where the VCOs for this dissertation are situated. The bottom section of the IC is a separate, non-related design designed by a third party. Prototyping was enabled via a multi-project wafer programme.

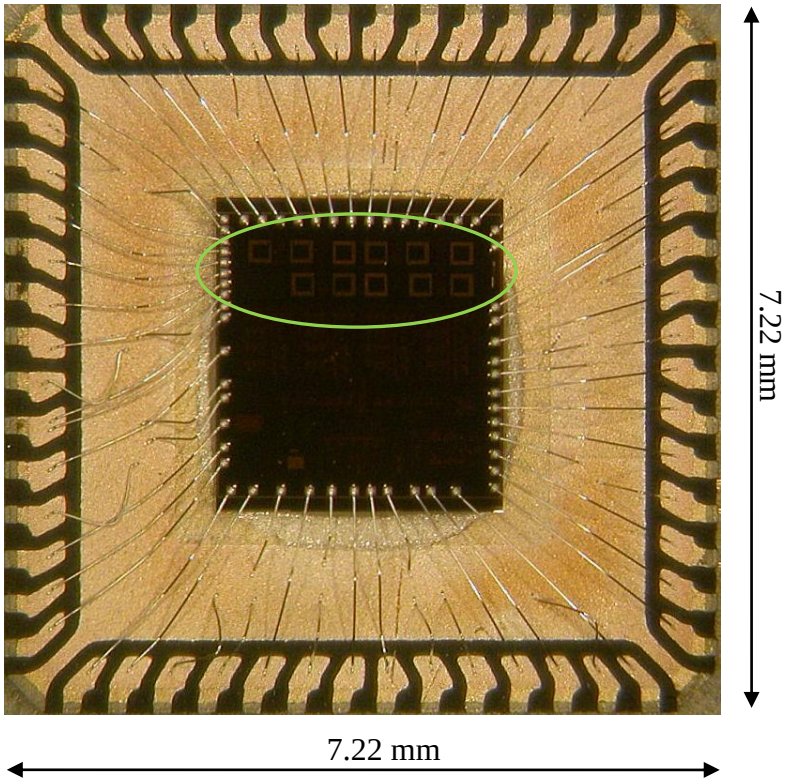


Figure B.19. Photograph of entire IC including bonding wires.

A zoomed-in version of Figure B.19 is given in Figure B.20. Note that the four VCOs are visible on the top of this figure (encircled in green).

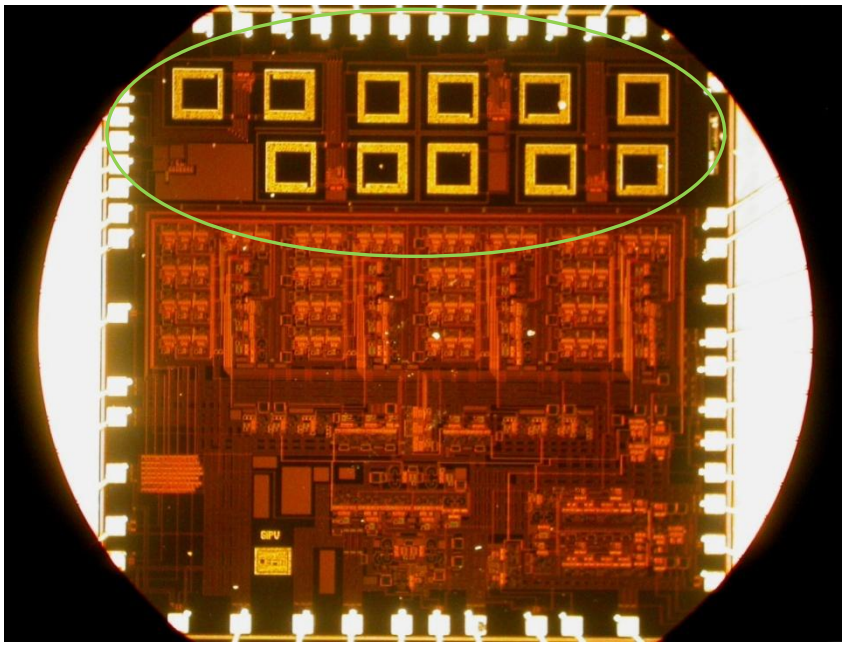


Figure B.20. Photograph of entire IC zoomed-in.

Figure B.21 shows only the first VCO separately. The inductors that are a part of this circuit, are the top right, bottom right, and bottom left inductor in Figure B.21.

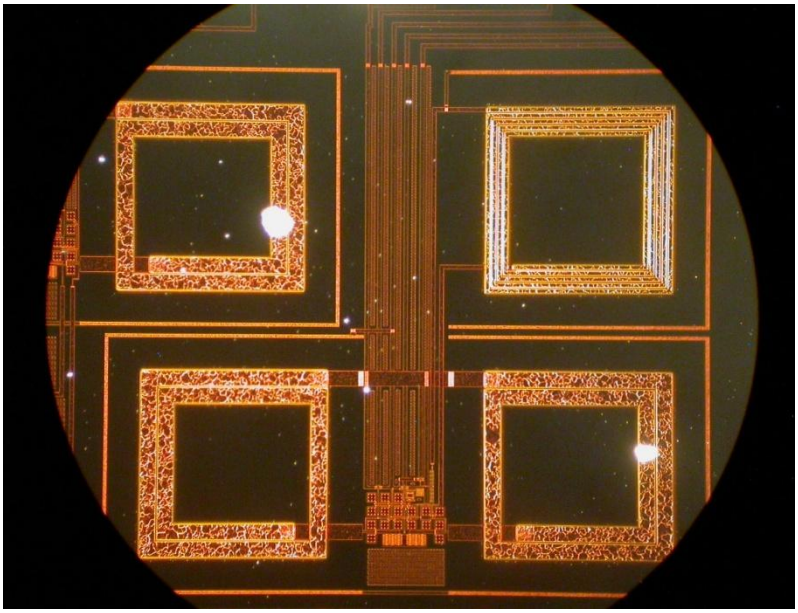


Figure B.21. Photograph of VCO 1.

Figure B.22 shows only the second VCO separately. The inductors that are a part of this circuit are the top right, top left, and bottom left inductor in Figure B.22.

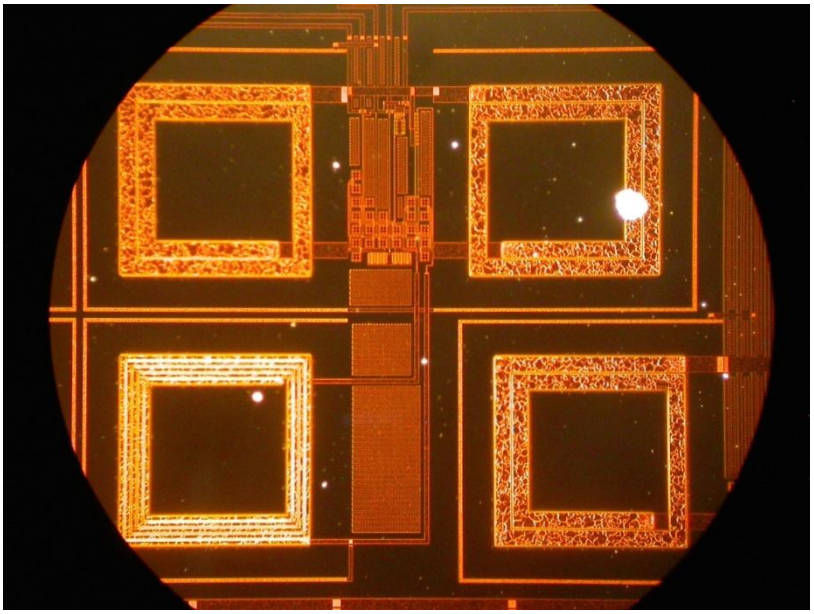


Figure B.22. Photograph of VCO 2.

The third VCO, VCO 3, is represented in Figure B.23. The inductors that are a part of this circuit are the top right, bottom right, and bottom left inductor in Figure B.23.

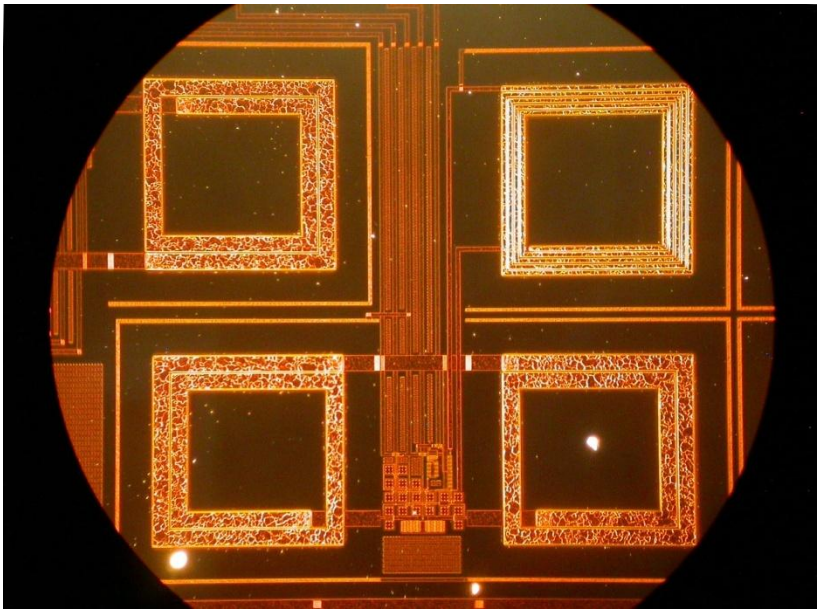


Figure B.23. Photograph of VCO 3.

The following figure, Figure B.24, shows only the fourth VCO separately. The inductors that are a part of this circuit are the top left inductor and the top right inductor which is not clearly visible from Figure B.24, but is visible as the top left inductor in Figure B.23.

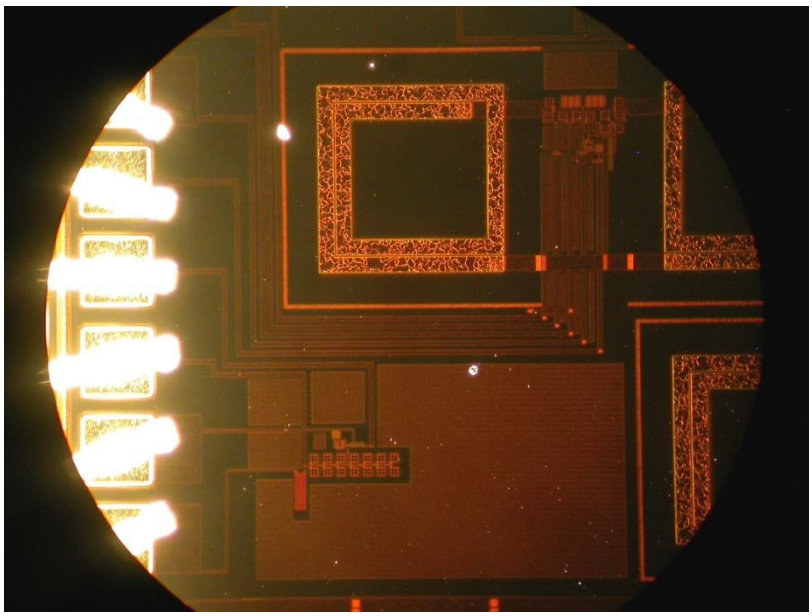


Figure B.24. Photograph of VCO 4.

A photograph of the buffer circuit is given in Figure B.25.

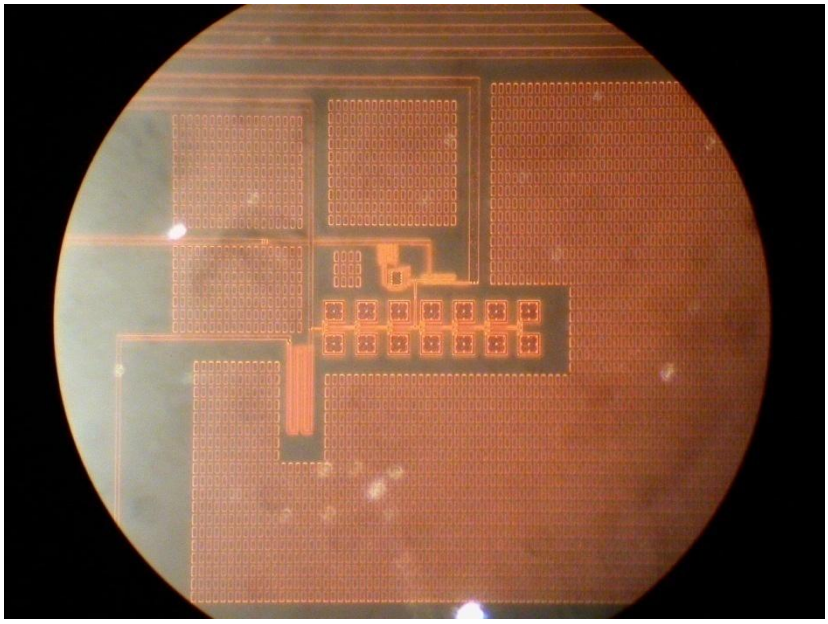


Figure B.25. Photograph of buffer circuit.

To indicate the relative size of the passive inductors compared to the active circuitry, Figure B.26 is presented.

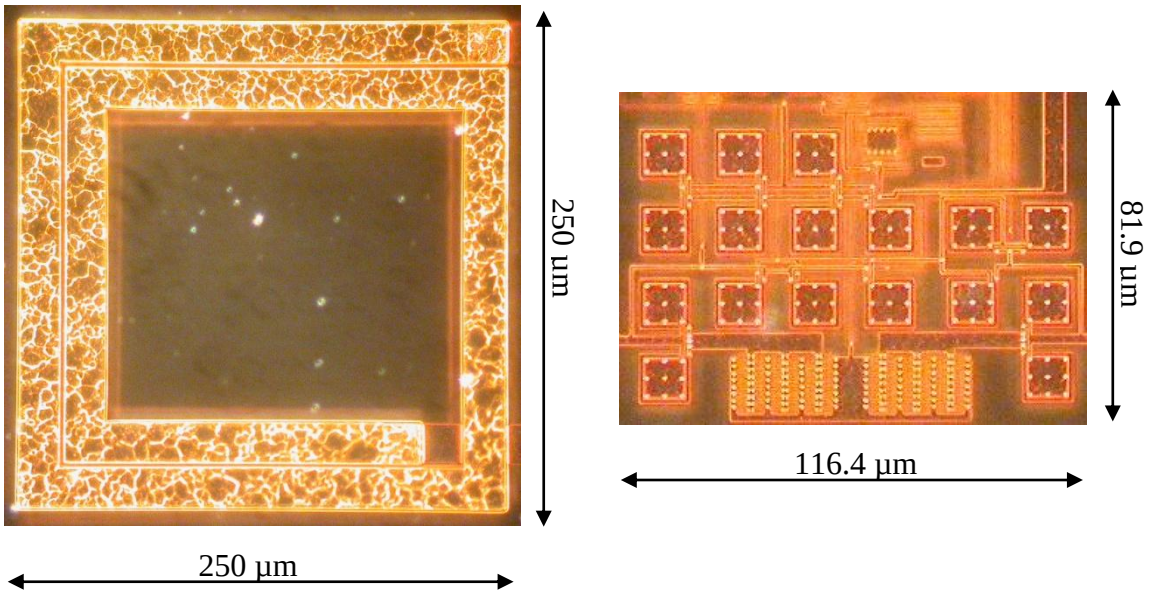


Figure B.26. Relative size of inductors compared to active circuit.

The relative size of the SP015S250T inductor compared to the active circuitry of VCO 1 is presented in Figure B.26. Refer to Figure B.4 for the Tanner® Tools® L-Edit® layout representation of VCO 1 to compare with this photograph of the circuit, and to Figure B.21 for a complete photograph of VCO 1 where the inductor is seen relative to the active circuit.

A figure of the bonding wires of the IC is given in Figure B.27.

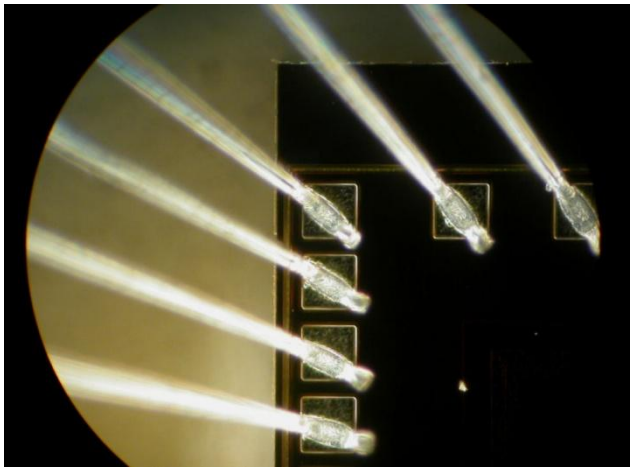


Figure B.27. Bonding wires of IC.

As discussed in Section 3.5, the reason for choosing the QFN package type was the fact that these packages provide a common ground terminal on the bottom of the package. This has the advantage that the ground leads are shorter as the leads can be connected anywhere on the surface of the IC. This is depicted in Figure B.28.

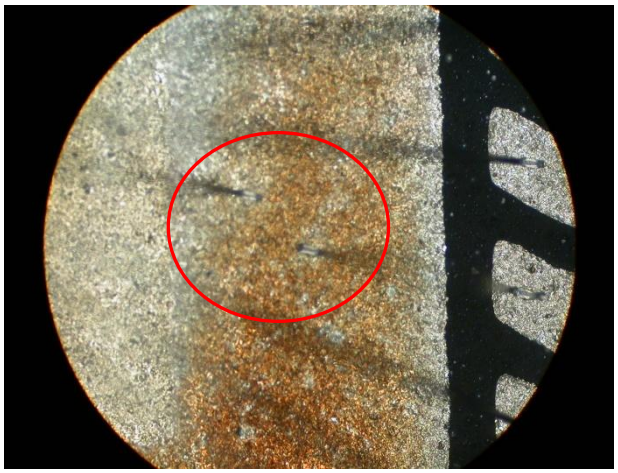


Figure B.28. Bonding wires of IC connected to common ground on package.

From Figure B.28, the red circle highlights the section on the package bottom surface, where the ground leads are connected. The ground lead therefore only extends from the bonding pad on the right in Figure B.28, a small distance towards the connector pins, where it is then commonly grounded, therefore reducing lead length, and thus reducing the effect of coupling capacitances or inductances that may occur due to long leads. In this way, current flow will occur along the path of least impedance.