THE DESIGN OF AN ELECTRO-OPTIC CONTROL INTERFACE FOR PHOTONIC PACKET SWITCHING APPLICATIONS WITH CONTENTION RESOLUTION CAPABILITIES

by

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SUMMARY

THE DESIGN OF AN ELECTRO-OPTIC CONTROL INTERFACE FOR PHOTONIC PACKET SWITCHING APPLICATIONS WITH CONTENTION RESOLUTION CAPABILITIES

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Keywords: Contention Resolution, Complex Programmable Logic Device, Electronic Header Processing, Optical Cross-point Switch, Optical Switch, Photonic Packet Switching, Re-circulating Buffer, Transparency, Variable Length Packets and Vertical Active Coupler.

The objective of the research is to design an electro-optic control for the Active Vertical Coupler-based Optical Cross-point Switch (OXS). The electronic control should be implemented on Printed Circuit Board (PCB) and therefore the design will include the PCB design as well. The aim of the electronic control board is to process the headers of the packets prior to entering the OXS to be switched and from the information in the headers, determine the state that the OXS should be configured in. It should then configure the optical cross-point accordingly. The electronic control board should show flexibility in the sense that it can handle different types of traffic and resolve possible contention that may occur.

The research seeks to understand the problems associated with Photonic Packet Switching (PPS) networks. Two of the main problems identified in a PPS network are contention resolution and the lack of variable delays for storing optical packets. The OXS was analyzed and found to meet the requirements for future ultra-high speed PPS network technology with its high extinction ratio, wide optical bandwidth, ultra-fast switching speed and low crosstalk levels.

Photonic packets were generated with 4-bit, 8-bit or 16-bit headers at a bit rate of 155 Mbit/s followed by a PRBS (Pseudo Random Bit Sequence) payload at 10 Gbit/s. Different scenarios were created with these types of packets and the electro-optic control and OXS were subjected

to these scenarios with the aim of testing the flexibility of the electro-optic control to control the OXS. These scenarios include:

- Fixed length packets arriving synchronously at one input of the OXS. Some packets are destined for output 1, some are destined for output 2 and some are destined for output 3, therefore realizing a 1-to-3 optical switch.

- Eight variable length packets arriving synchronously at the OXS at one input, all of them destined for one output. The electro-optic control should open the switch cell for the correct amount of time.

- Three variable length packets arriving synchronously and asynchronously at one input of the OXS. Some packets are destined for output 1 while other packets are destined for output 2. The electro-optic control should open the correct switch cell for the correct amount of time.

- Two fixed length packets arriving at the OXS synchronously on different input ports at the same time, both destined for the same output port. The electro-optic control should detect the contention and switch the packets in such a way as to resolve the contention.

The electro-optic control and OXS managed to switch all these types of data traffic (scenarios) successfully and resolve the contention with an optical delay buffer. The success of the results was measured in two ways. Firstly it was deemed successful if the expected output sequence was measured at the corresponding output ports. Secondly it was successful if the degradation in quality of the packet was not drastic, meaning the output packets should have an BER (Bit Error Rate) of less than 10^{-9}. The quality of the packets was measured in the form of eye diagrams before and after the switching and then compared.

The research resulted in the design and implementation of a flexible electro-optic control for the OXS. The problem of contention was resolved for fixed length synchronous packets and a proposal is discussed to store packets for variable lengths of time by using the OXS. This electro-optic control has the potential to control the OXS for traffic with higher complexities and make the OXS compatible with future developments.

SAMEVATTING

DIE ONTWERP VAN ’n ELEKTRO-OPTIESE BEHEERSTELSEL VIR FOTONIESEPAKKIE-SKAKELINGDOELEINDES MET KONTENSIE-OPLOSSINGSVERMOË.

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Graad: M.Ing. (Elektroniese Ingenieurswese)
Sleutelwoorde: Deursigtigheid, Elektroniese Hoofprosessering, Hersirkulerende Buffer, Kontensie-oplossing, Komplekse Programmeerbare Logiese Toestel, Optiesekruispunt-skakelaar, Optiese Skakelaar, Fotoniesepakkie-skakeling, Verskeielengte-pakkies, Vertikale Aktiewe Koppelaar

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Die doel van die navorsing is om ’n elektro-optiese beheerstelsel te ontwerp vir die aktiewe vetikale koppelaar-gebaseerde Optiese-Kruispunt-Skakelaar (OKS). The elektro-optiese beheer moet op ’n stroombaanbord gebou word en dus sluit die ontwerp ook dié van ’n stroombaanbord in. Die doel van die elektro-optiese beheer is om die hoofde van die pakkies te prosesseer net voordat hulle in die OKS ingaan om geskakel te word, sodat die staat waarin die OKS gestel moet word, bepaal kan word. Die elektro-optiese beheer moet dan die OKS soos volg skakel: die elektroniese beheer moet buigsaamheid toon in die sin dat dit verskeie tipes verkeer kan hanteer en ook kontensie oplos wat mag opduik.

Die navorsing probeer vasstel wat die probleme met Fotoniesepakkieskakeling- (PPS) netwerke is. Twee van die belangrikste probleme is kontensie en die realisering van verskeie lengte vertragings om fotoniese pakkies te stoor. Die OKS is geanaliseer en daar is bevind dat dit aan die vereistes voldoen van toekomstige ultra-hoë PPS netwerktegnologie met sy hoë ekstinksieverhouding, wye optiese bandwydte, ultra-vinnnige skakelingspoed en lae kruisspraakvlakke.

Fotoniese pakkies word gegenereer met hoofde van 4 bisse, 8 bisse of 16 bisse teen ’n bis-tempo van 155 Mbis/s, wat gevolg word deur ’n PRBS vrag teen 10 Gbis/s. Verskillende

scenarios word beplan en die elektro-optiese beheer en OKS word dan blootgestel aan die scenarios met die doel om die doeltreffendheid van die elektro-optiese beheer en OKS te toets. Die schenarios sluit in:

- Vastelengte-pakkies wat sinchronies by inset 1 van die OKS aankom. Sekere van die pakkies moet na uitset 1 gaan, ander moet na uitset 2 gaan en sekere pakkies moet na uitset 3 gaan. Dus word ’n 1-tot-3 optiese skakelaar gerealiseer.
- Agt verskilende lengte pakkies wat sinchronies by inset 1 van die OKS aankom. Almal word na uitset 1 geskakel. Die elektro-optiese beheer moet dan die skakelsel oopskakel vir die regte hoeveelheid tyd.
- Drie verskilende lengte pakkies wat sinchronies en asinchronies by inset 1 van die OKS aankom. Sekere pakkies moet na uitset 1 gaan en die ander pakkies moet na uitset 2 gaan. Die elektro-optiese beheer moet dan die regte skakelsel oopskakel vir die regte hoeveelheid tyd.
- Twee vastelengte-pakkies kom gelyktydig by die OKS aan op twee verskillende insette. Beide van hulle moet na uitset 1 geskakel word. Die elektro-optiese beheer moet dan die kontensie waarneem en die pakkies so skakel dat die kontensie opgelos word.

Die elektro-optiese beheer en OKS het suksesvol al die tipes scenarios hanteer en die kontensie opgelos met ’n verlengde vessel. Sukses word op grond van twee aspekte gemeet. Eerstens is die eksperimentele resultate suksesvol as die uitsetstroom-pakkies dieselfde is as wat verwag is. Tweedens is die resultate suksesvol as die kwaliteit van die sein nie noemenswaardig versleg nie, wat beteken dat die BFT (Bis Fout Tempo) vir die pakkies minder as 10^{-9} moet wees. Die oogdiagram van die pakkies word geneem, voor en na die OKS, om die kwaliteit van die pakkies te meet voor en na skakeling en dit dan te vergelyk.

Die navorsing het gelei tot die ontwerp van ’n doeltreffende elektro-optiese beheerstelsel vir die OKS. Die kontensieprobleem is opgelos vir vastelengte-pakkies wat sinchronies vervoer word en ’n voorstel om pakkies vir verskilende lengtes te stoor, word bespreek. Die elektro-optiese beheer het die potensiaal om die OKS vir meer ingewikkelde verkeer ook te beheer en sal dus die OKS verenigbaar maak met toekomstige ontwikkelinge.

LIST OF ABBREVIATIONS

ATM	Asynchronous Transfer Mode
AVC	Active Vertical Coupler
AWG	Arrayed Waveguide Grating
BER	Bit Error Rate
BPF	Band Pass Filter
CPLD	Complex Programmable Logic Device
EDFA	Erbium Doped Fibre Amplifier
FTTH	Fibre To The Home
GEPON	Gigabit Ethernet Passive Optical Network
InGaAs	Indium Gallium Arsenide
MOD	Modulator
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
OOK	On-off Keying
OXS	Optical Cross-point Switch
PC	Polarization Controller
PON	Passive Optical Network
PPG	Pulse Packet Generator
PPS	Photonic Packet Switching
PRBS	Pseudo Random Bit Sequence
SDH	Synchronous Digital Hierarchy
SLALOM	Semiconductor Laser Amplifier in Loop Optical Mirror
SOA	Semi-conductor Optical Amplifier
SONET	Synchronous Optical Network
TTL	Transistor-transistor Logic
VOA	Variable Optical Attenuator

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CHAPTER 1: INTRODUCTION

1.1 Background

Today's optical networks offer many types of services. These services are connection orientated in the sense that data is being transported across an underlying network between two or more parties. The bandwidth of the connection as well as the type of network with which this connection is supported has a significant impact on the quality of the service offered [1]. The three types of networks include circuit switched, packet switched and burst switching networks.

In a circuit switched network the connection has a guaranteed amount of bandwidth all the time. Circuit switching networks lack the ability to handle bursty data traffic efficiently [2]. Packet switching was invented to increase the efficiency of transporting bursty traffic across the network. In packet switching networks, the data are broken up into packets. Packets from all sources share the network at the same time. A packet consists of a header and payload. The header carries information about the destination of the payload and is used to route the packet through the network. Burst switching is very similar to packet switching in the sense that many packets with the same destination are grouped together, forming a burst, and are sent across the network at one time. An example of a packet based switching network is the Internet with Internet Protocol (IP) based packets being routed across the telecommunication network.

Optical fibre technologies are widely used in telecommunication networks today and have the ability to manage and support all three these types of connections. SONET/SDH networks deploy optical interfaces and play a major part in metro and long-haul transport networks. The role of optics today is only limited to the realization of transport functions. The overhead, control and management functions are performed in the electronic domain. Next generation networks might perform switching and control functions directly in the optical domain [3]. In order to exploit the tremendous capacity provided by optical fibre, the switching functions must be implemented in the optical domain [4]. Photonic packet switching technologies are still in the experimental stage in research laboratories and require maturity before prototypes

will become commercially available. In an optical packet switching network, also known as a photonic packet switching network, packets are switched across the network while in the optical domain without any optical-electrical-optical conversion.

1.2 Motivation

With the telecommunication network's bandwidth increasing at a very fast rate, the future telecommunication network should be able to handle and manage this traffic load efficiently, fast and without error and to be compatible with future development and a further increase in the telecommunication network's traffic. Optical fibre networks most certainly have this capability, with technologies such as DWDM (Dense Wavelength Division Multiplexing), PPS (Photonic Packet Switching), Optical Burst Switching and OTDM (Optical Time Division Multiplexing). Photonic packet switched networks combine the high capacity of optical technology with the flexibility of packet switching and are regarded as a promising future solution for all-optical networks [2], [5]-[6]. Owing to the high bandwidth demand, bandwidth efficiency is of the utmost importance in optical fibre networks and photonic packet/burst switching networks manages high bandwidth more efficiently.

In the last 20 years, novel optical technologies, such as distributed feedback lasers, advanced designs of passive and active optical fibres, erbium-doped and Raman optical amplifiers, high-speed optical modulators and wavelength division multiplexing have revolutionized the transport of information by moving data transport from the electronic domain to the optical domain. With the advent of reconfigurable optical add-drop multiplexers, the need for optical-electrical-optical conversion and electronic processing was pushed further away from the network core towards the edge of an increasingly all-optical network.

The full potential of optical communication networks is compromised (not utilized to its full potential) in networks that convert the data to the electronic domain. If information is converted to the electronic domain, an electronic bottleneck is formed owing to the limitation of electronic processing and high bandwidth capabilities (+40Gbits/s per channel) of optical fibre networks. Currently optical networks still depend on the electronic domain to assist in data transport. In photonic packet switching networks the packets can be kept in the optical domain but by tapping off some optical power, the header can be processed electronically to

perform control functions. Therefore the need for fast and flexible control circuitry is of the utmost importance in PPS networks. While the processing is being done, the packet needs to be buffered in a fibre delay line and therefore transparency is preserved. Transparency can easily be implemented in circuit switching networks but is more complex in packet and burst switching networks.

Because photonic packet switching technology is being developed in research laboratories [2], problems and difficulties can be identified at this stage and be dealt with before the product becomes commercially available.

1.3 Nature of problem

A typical optical fibre network is shown in Figure 1.1. The access networks for example, audio/video streaming, PDA mobile gateway, sensor networks, FTTH networks and wireless networks, all connect to the metro optical network. All the different metro networks are connected to a core or backbone network over which optical packets must be routed. Optical packets arrive at the input of the node and need to be switched to a specific output of the node in order to reach their destination.

It is at these nodes that some problems with photonic packet switching are identified. The first problem is the need for a fast and flexible control mechanism and optical switch to route optical packets from the input of these nodes to the outputs. The second problem occurs when two or more packets on the same wavelength enter the node from different input ports and are destined for the same output port at the same time and in the same space. If this contention of input packets is not resolved, it will result in loss of data due to interference of light with these two packets. This is a problem in photonic packet switching networks and needs to be taken into account when designing optical fibre networks, otherwise it will result in a dramatic decrease in quality of service.

According to [7] contention resolution belongs to a realm of higher-level routing control and should be dealt with by more complicated control and according to [8], contention resolution is a fundamental difficulty with all optical packet switch designs due to a lack of optical memory.

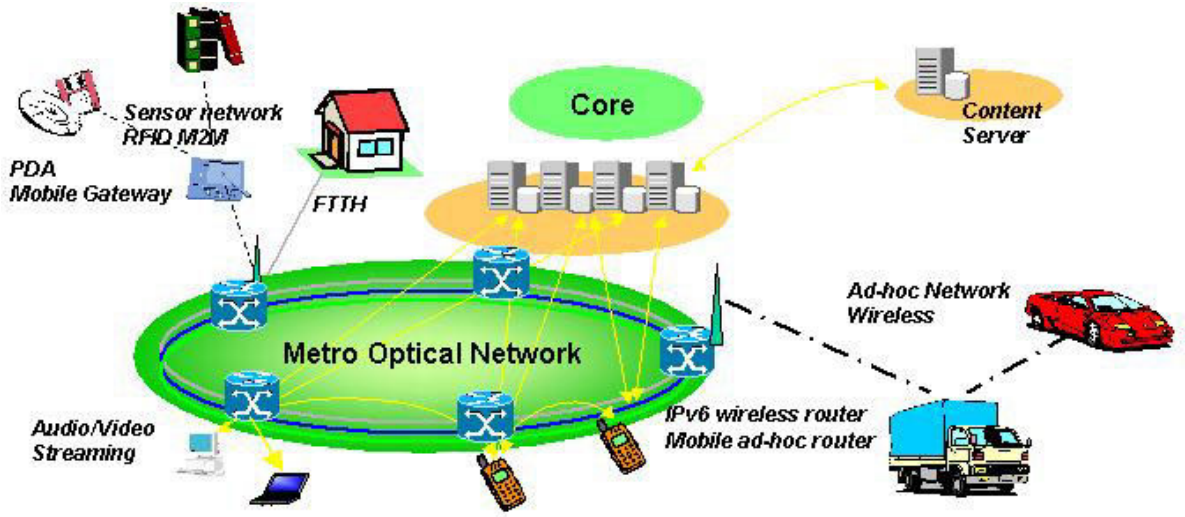


Figure 1.1

An overview of an optical network from [9]. The access networks connect to the metro optical network. The core optical network connects different metro optical networks.

Because of the processing that needs to be done or contention that needs to be resolved, a third problem arises: these optical packets need to be "stored" for some time while the processing is being done or contention is being resolved. No optical RAM is available and therefore fibre delay lines are used to "store" the optical packets for a fixed duration of time. Sometimes there is a need for variable length delay and this requires more complicated buffering strategies.

1.4 The aim of the research

The objective of this research is to identify a potential optical switch to be used in photonic packet switching networks. The aim is then to develop an electro-optic control interface to manage and control this optical switch very fast (in the order of 10 ns) in order to demonstrate errorless photonic packet switching with the capability to detect when contention occurs as well as to resolve it successfully. The electronic control should show flexibility in the sense that various types of data traffic can be switched.

CHAPTER 2: LITERATURE STUDY

2.1 Introduction

The research will focus mainly on photonic packet switching functionality. The technologies within optical networks that need to be studied include

- photonic packet switching,
- optical switches,
- contention resolution techniques,
- optical buffering of packets (fixed and variable length),
- optical and electronic header processing, and
- the nature of data traffic in these types of networks.

Photonic packet switching has emerged as an attractive way to overcome the electronic bottleneck in today's fast-growing communication network. Identifying the needs and requirements for photonic packet switching networks will give insight into the design of the electro-optic control interface. As more bandwidth is provided in these systems, issues such as processing, optical buffering, scalability and contention remain the key design challenges for the switching networks. The goal of photonic packet switching networks is to provide the same services as those of electronic packet switched networks but at much higher speeds. Although optical packet switching networks offer extremely high data rates, transparency and high switching speed, their performance depends strongly on optical device technology [10].

A typical optical fibre network is shown in Figure 2.1. The network consists of three main interconnected networks: the core network, the metropolitan network and the access network. The core or long-haul network carries the highest amount of data and basically connects all the metropolitan networks. The access network is the connection point of all the clients to the optical network. The dominating optical network for the access network is the PON (Passive Optical Network) or GEPON (Gigabit Ethernet Passive Optical Network). The metropolitan and core networks basically consist of nodes interconnected by fibre cables. These nodes and fibres are connected in a ring, star or mesh topology. It is at these nodes that data need to be

switched from one specific input fibre to another specific output fibre. This switching is done with a photonic switching element.

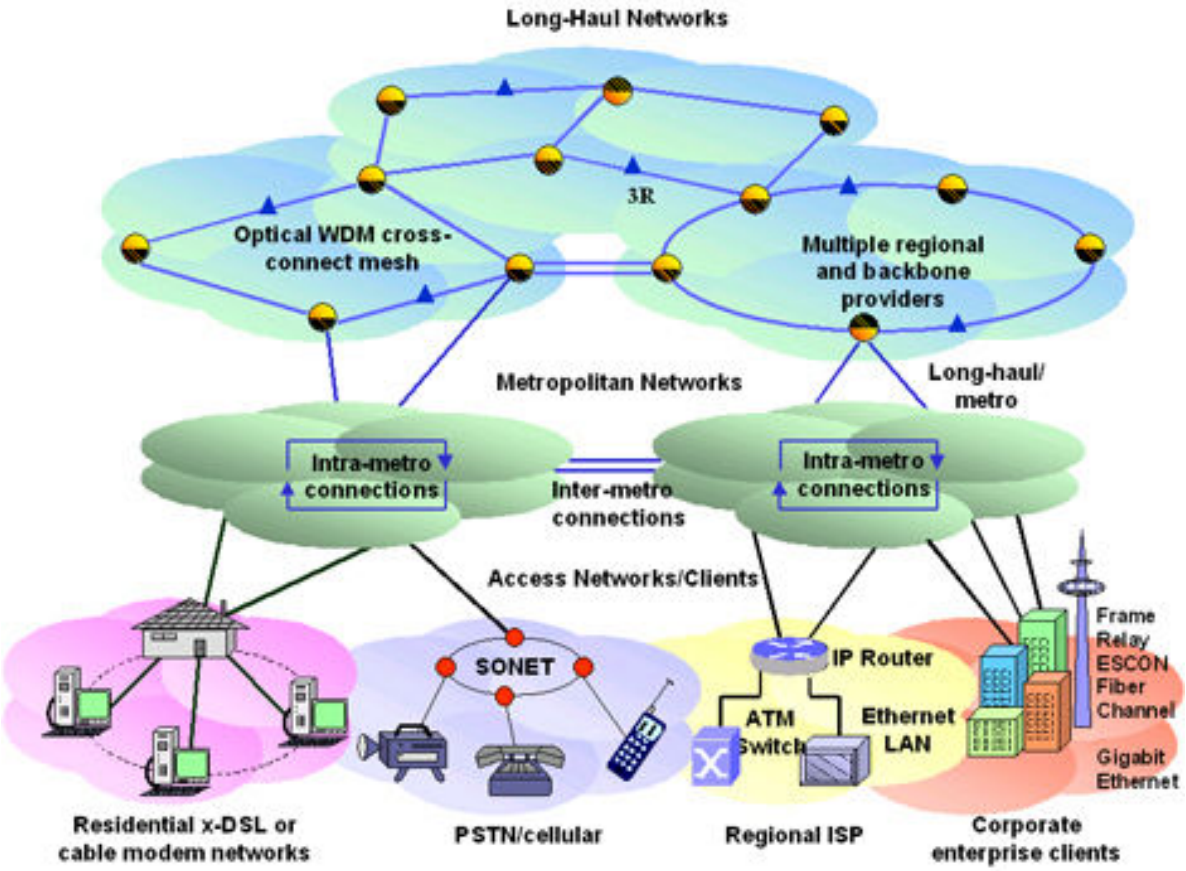


Figure 2.1

Diagram illustrating how different optical network layers are interconnected. Access network such as x-DSL, cellular, ISP and Gigabit Ethernet are connected to the metropolitan network. Long-haul networks connect all the metropolitan networks to form the backbone optical network. Picture taken from [11].

The basic building blocks of such a switching node will be studied and various problems that may occur at these photonic packet switching nodes will be addressed. Recent experimental results from different sources will also be investigated.

2.2 Elements of a photonic packet switching node

The function of the node is to make and break connections between inputs and outputs. A

typical node will have 4-16 input fibres with about 16 channels (different wavelengths) carried on each input. The data entering the node must be switched optically to the correct output port, depending on the information in the header. Figure 2.2 shows such a generic node with N input fibres and *n* wavelength channels in each fibre. The first function is to demultiplex the wavelengths from the different inputs so that only one specific wavelength, from the N different inputs, travels through a synchronization, buffer and optical switching block. Synchronization is done to align packets in time before entering the optical switch because packets arrive at the node out of synchronization due to different routes travelled. The buffer stores the packet for a fixed amount of time in order for the processing to be done and optical switch to be set up correctly. The optical switch will be an N×N switch. There are different blocks for each wavelength since different information is carried on different wavelengths and is destined for different outputs. All the packets from these different blocks are then again multiplexed onto one fibre at each output port. Although a wavelength routing technique also exist to implement a generic node, this dissertation will focus on the generic node structure from Figure 2.2.

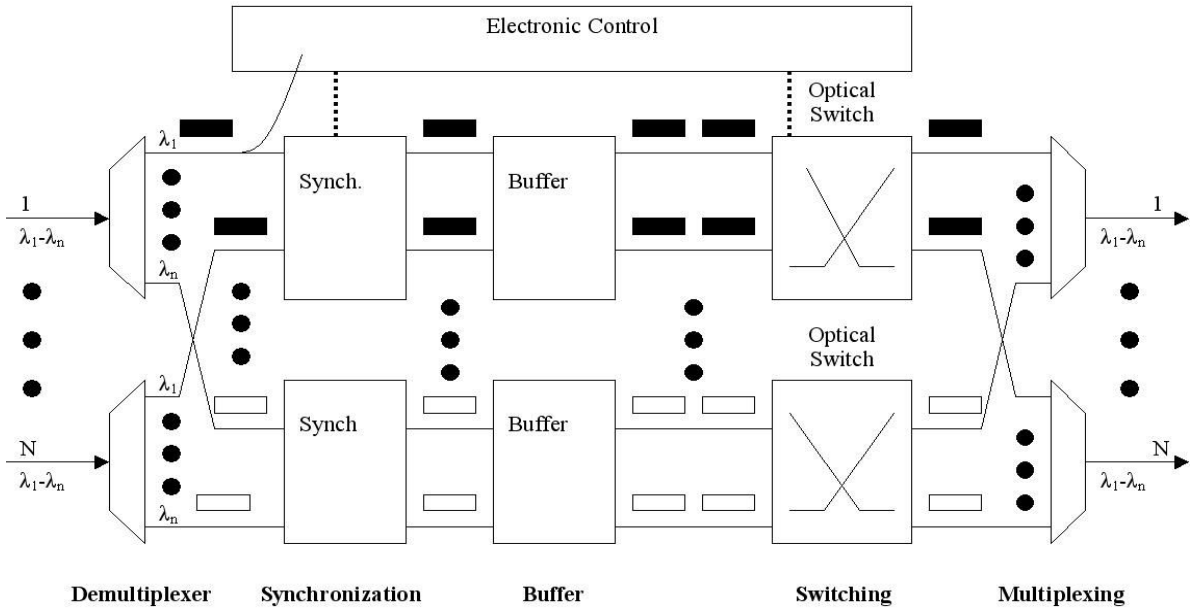


Figure 2.2

A generic node found in the core and metro optical networks. It has N input and output fibres each with *n* wavelengths. The packets need to be synchronized and buffered before they can be switched. Each optical switch handles only one specific wavelength [2], [5].

Packet switching structures are compared on a number of parameters; one such figure of merit is the loss probability or blocking probability [12]. The functioning of such a generic node is strongly dependent on the type of data. One of the most important components in photonic packet switching networks is the optical switch. This component should be able to route optical packets within a few nanoseconds from the input to the correct output port.

Switching is an essential operation in communication networks [13]. A switch is a device that establishes and releases connections among transmission paths in a communication network. Fibre-optic communication networks can transport data at a rate of 2.5 Terabits/s on one fibre. This rate is achieved by WDM and OTDM. At these high data rates, very fast photonic switches are essential. Types of optical switches include: Optical MEMS (Micro-Electro-Mechanical System), thermo-optical, electro-optical, opto-optical, acousto-optical and magneto-optical [13], [14]. Optical MEMS are miniature devices with optical, electrical and mechanical functionalities at the same time. Thermal optical switches are based on waveguide thermo-optic effect or thermal phenomena of materials. Electro-optical switches realize optical switching by using the electro-optic effect. Opto-optical switches realize switching functions relying on the intensity-dependent nonlinear optic effect in optical waveguides. The efficiency and performance of these optical switches depend on the following characteristics:

- Size - This is the number of inputs and outputs that the switch supports.
- Direction – The ability to transfer light across the switch in one or two directions.
- Switching speed - The time it takes to be reconfigured from one state to another.
- Propagation delay time - The time it takes the light from the input to the output.
- Throughput - The maximum data rate that can flow through the switch when it is connected.
- Switching energy - The energy needed to activate and deactivate the switch.
- Power dissipation - The energy dissipated per second in the process of switching.
- Insertion loss - The loss in optical power introduced by the connection.
- Crosstalk – The undesired power leakage to other ports.
- Physical dimensions – The size of the switch architecture.
- Bandwidth – The band of wavelengths that the optical switch supports.
- Transparency – The independence of the switch from the bit-rate or protocol of the data.

The different types of optical switches are compared on the basis of these characteristics and the comparisons are given in [14]. One important characteristic that needs to be pointed out is that the fastest optical switch is the SOA based switch that is an electro-optic switch with switching speed in the order of 200 ps.

Another optical switch that is being developed in the research laboratories is the SLOB (Switch with Large Optical Buffers) [10]. The SLOB has a very simple architecture and very large buffer depth, ideally for bursty traffic. This switch is limited by optical power loss, noise and crosstalk when the number of input and output ports is high. The ALCATEL ATM switch [10] is limited by the splitting and combining losses. Optical amplifiers can increase the performance by increasing the optical power but also introduce more noise. The ALCATEL ATM switch is limited to 16 inputs. The ULPHA (Ultra-Fast Photonic ATM) switch is similar to the ALCATEL ATM but utilizes ultra-short optical pulses. It has many electronic devices that result in the electronic bottleneck effect. The ULPHA is a very large architecture but with a relatively simple routing algorithm.

The most common limitation in optical switches is the optical splitting and combining losses. To solve this problem, an AWG (Arrayed Waveguide Grating) is used. The AWG switch takes the optical input power, consisting of a number of wavelengths, and switches the specific wavelengths to specific output ports by interference. Owing to the wavelength dependence of the AWG, it is also very popular in resolving contention in the wavelength domain. The AWG has a typical power penalty in the order of 1.54dB for 32 inputs.

The European Keys to Optical Packet Switching project (KEOPS), described in [8], [15] focuses on the development and assessment of optical packet switching and routing networks capable of providing transparency to the payload bit rate. They seek to combine packet switching with WDM transmission techniques to yield WDM optical packet switching. They use a WRS (Wavelength Routing Switch) that relies on dynamic wavelength conversion at the packet level to perform the routing of packets. The WRS includes demultiplexers based on the AWG. The switch is under the control of an electronic unit.

Fewer components result in less noise and crosstalk and therefore it is desirable to build such a photonic packet switching node with as few components as possible. These will also reduce

the cost of the network. A very attractive optical switch is the AVC (Active Vertical Coupler-Based) OXS (Optical Crosspoint Switch), an electro-optical switch, which will be discussed in greater detail in the next section.

2.3 The Active Vertical Coupler Based Optical Crosspoint Switch

The AVC OXS was developed and built by researchers in the Department of Electrical and Electronic Engineering at the University of Bristol in the United Kingdom. The OXS has four optical inputs and four optical outputs. The top view of the OXS can be seen in Figure 2.3. Each of the four inputs consists of a passive waveguide separated by 500 µm from one another to guide the light into the OXS.

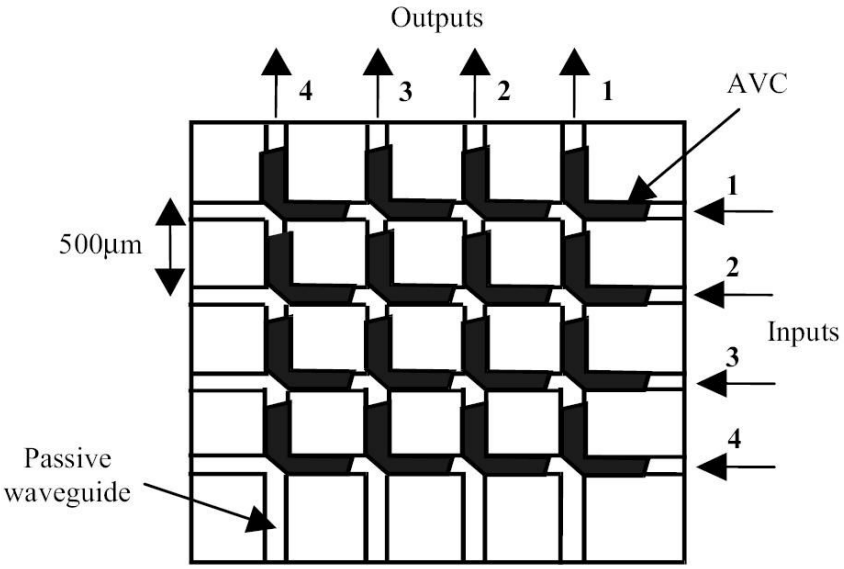


Figure 2.3

The 4x4 AVC OXS seen from the top. Four passive input and output waveguides intersect at the 16 cross points. Sixteen AVCs are grown at these cross points [4].

The four outputs also consist of passive waveguides separated by 500 µm that intersect perpendicularly with the input waveguides. These passive waveguides are made from InGaAsP. These four input and output waveguides are deposited on top of an InP substrate and intersect in 16 places.

A three-dimensional picture of a 2x2 OXS is shown in Figure 2.4. On top of each of these waveguide crosses, an active layer is deposited that together with the passive lower waveguide forms an active vertical coupler. Active refers to the fact that the waveguide has either a significant loss or gain of the optical signal concerned. External power is required to perform the coupling operation. This loss or gain and refractive index can be modulated by current injection. Two of these active vertical couplers are made, one with the input passive waveguide and the other one with the output passive waveguide. A total internal reflection mirror vertically penetrates the active waveguide at an angle of 45° with respect to the two couplers' directions. This intersection, or crosspoint, is called a switch cell.

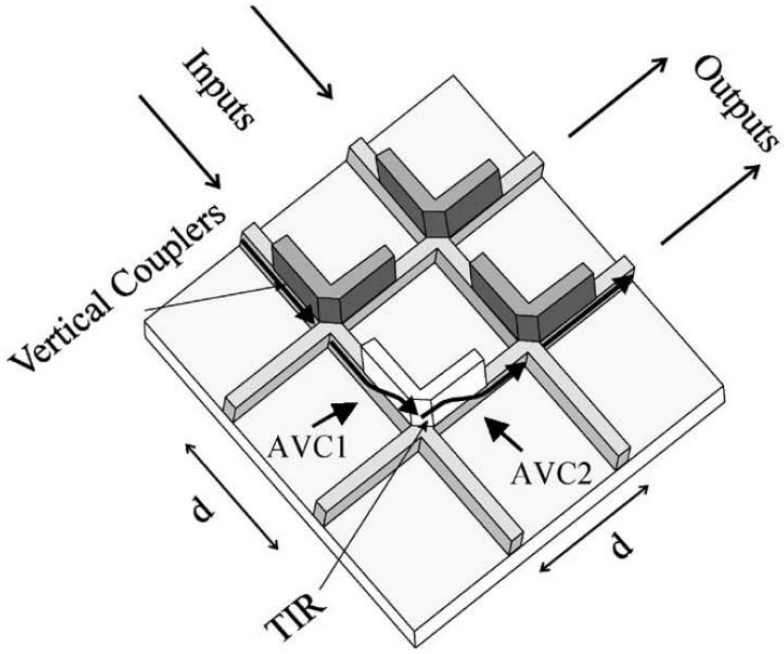


Figure 2.4

A 3D view of a 2x2 OXS. The arrows indicate the direction and how light travels through the OXS when in the ON state. TIR: Total Internal Reflection, AVC: Active Vertical Coupler [16].

A single switch cell is shown in Figure 2.5. The switch cell can be operated in one of two states. The injection of carriers into the active region turns the device to the "ON" state. Applying current to the active region causes the injection of carriers into this region. It generates gain and reduces the refractive index of the active upper waveguide to match the corresponding refractive index value of the bottom passive waveguide. Therefore in the "ON"

state, the travelling input light signal, injected into the input passive lower waveguide, couples with the active upper waveguide at the first active vertical coupler and is steered by the total internal reflection mirror into the second active vertical coupler waveguide. The light is then coupled down to the bottom passive waveguide to exit the OXS via the specific passive output waveguide.

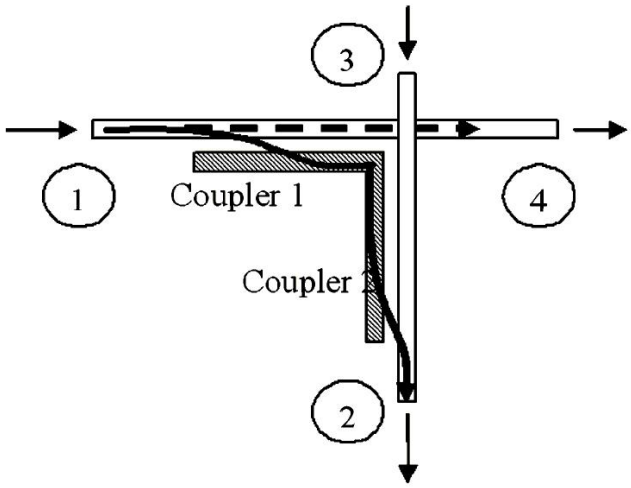


Figure 2.5

One of the switch cells is shown here. In the OFF state light travels in the passive waveguide from 1 to 4, in the ON state light travels from 1 to 2 via the AVC [17].

When in the "OFF" state the OXS is not biased and therefore the input optical signal only travels along the input lower passive waveguide. The optical signal in the passive waveguide does not interact with the active layer and travels straight through to the next switch cell. Any residual coupling into the active layer is absorbed by its high loss and therefore very little of the signal (leakage) appears on the output. When operated in a point-to-point switching application, up to four input signals can be simultaneously switched through the matrix if they are not contending with each other. The electronic control will control the states of these switch cells by supplying current to the corresponding switch cell.

One of the main problems with the OXS is to package it or connect the OXS chip, Figure 2.6, with optical fibres and electrical connections. Four input and four output optical fibres are needed as well as 16 electrical connections, one for each switch cell. The coupling strategy, to connect optical fibres to the waveguides or OXS chip, is discussed in [18]. The fibres need to

be coupled with minimum optical coupling loss. Since the OXS chip is an active device, heat will be generated and thermal management is required to keep the chip operating at environmental temperatures. The packaged case has dimensions of 30 x 30 x 9 mm (L x D x H). Two sides are used for optical fibre access. The other two sides are used for electrical connections. Refer to Figure 2.6 that demonstrates this packaging.

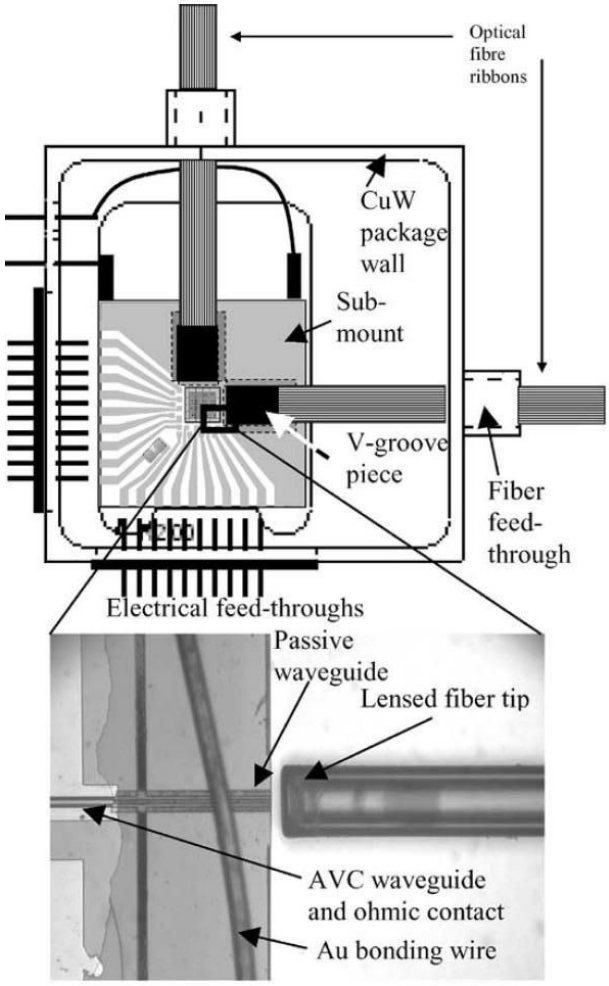


Figure 2.6

Diagram illustrating the packaged OXS chip [18].

Fibre array alignment and fixation are the two most critical issues in the packaging process. The fibre ends need to be micro-machined into lenses with the proper shape to achieve high coupling efficiency. Wedge lenses are used instead of conical lenses because of limitations in the micro-machining process. The fibre tips are machined by a high-powered laser beam into wedge-shaped fibre lenses with a focal distance of about 9 μm.

Various experiments have been done with the AVC OXS to demonstrate the flexibility of the OXS as optical switching mechanism. A continuous data stream was sent into the OXS and short packet type control signals were sent to the switch cell, resulting in packets being generated [4], [17]. The ON-OFF extinction ratio was 70 dB and crosstalk levels of smaller than –65 dB were achieved. Each switch cell was tested and experimented with separately. A power penalty of less than 1 dB at a BER of 10^{-11} was measured between the longest and shortest path. The longer paths suffered higher power penalties.

All experiments above use the OOK external modulation scheme. By using a DPSK (Differential Phase Shift Keying) payload, the pattern effect was reduced and this is demonstrated in [19]. Timeslot interchange was demonstrated through which the order of the arriving packets is rearranged into a more desirable order for specific applications such as time division multiplexing [20]. A re-circulating buffer of one timeslot was used to store packets for a fixed time. Multiple re-circulations through the optical buffer were demonstrated. The packets are 60 ns long and consist of a PRBS at 10 Gbit/s.

Optical multicasting experiments have also been done with the OXS and results are discussed in [21], [22]. In optical multicasting experiments one packet is sent into the input port and exits all four output ports. Switching the switch cell on with a higher current than that used in normal packet switching operations can achieve this multicasting. In [23] packets with different optical powers are sent to the OXS and switched to the output at equal power levels. To achieve this power equalization, processing is needed to determine the power level and make a decision on how much current to use to switch on the switch cells, since the current is proportional to the optical power loss across the switch cell.

In all these experiments the current is controlled (switch cell being switched ON and OFF) by a signal from the PPG. This signal is deterministic, meaning that before the experiment is conducted, a plan is set up to determine which switch cells should be opened and for how long they should be opened. The signal from the PPG is a 16-bit code that includes a header detection code and the address of the switch cell to open. In a more realistic situation, this approach will not work because of the undetermined nature of data traffic, and therefore a header signal is needed before the payload that carries information about the packet.

The experiments in [7], [23] have this form of header or optical label. A guard time of 103 ns is used between the header and payload to allow time for processing and switching the switch cell from the OFF state to the ON state. No input buffer is therefore needed. In [7] the header is sent on λ_1 and the packet's payload is sent on λ_2, 103 ns later. The optical header is converted to the electronic domain, processed and the corresponding switch cell is opened. When the payload arrives at the OXS it can be switched directly without being buffered. Variable length packets are generated and switched across the OXS. The label or header is a 14-bit sequence at 155 Mbit/s, indicating which switch cell needs to be switched open for its packet and for how long the switch cell must be opened. This approach of transmitting the switch cell's address to be used in the header is not very good. It does not take into account what happens on the other input ports of the same OXS. A better approach is to indicate the desired output port of the packet in the header. The electronic control should detect from which input the packets are coming, which output port they are destined for and then compare this information with the current status of the OXS. The electronic control then decides which switch cell to switch open for the packets. In PPS or OBS networks that run synchronously or in a slotted approach, the status can be determined at the beginning of each timeslot, but with packets arriving asynchronously at the switch, real time status needs to be used.

2.4 Contention-resolving techniques

A fundamental issue in packet switching networks is contention resolution [24], [25]. Contention occurs at a switching node whenever two or more packets try to leave the switch fabric on the same output port, on the same wavelength and at the same time. When designing a photonic packet switching network with contention resolution capabilities the nature of the data traffic is of the utmost importance. These characteristics include fixed length packets versus variable length packets or bursts and whether the data arrive at the optical switch synchronously or asynchronously.

The three main solutions used to resolve contention include:

1. In the time domain by using a fibre delay line as a buffer to store the contending packet for a fixed amount of time.

2. In the space domain by deflection routing whereby the contending packet is switch via another route to its destination to resolve the contention.

3. In the wavelength domain by converting the contending packet to another wavelength that is available.

The type of contention-resolving technique is dependent on the characteristics of the data being sent across the network. All three these solutions have been demonstrated and results were all successful [24], [26]-[34]. Both wavelength conversion and optical buffering require extra hardware. This includes wavelength converters, lasers and demultiplexers. Optical fibres and extra switching ports are needed when implementing buffering to resolve the contention. Deflection routing requires extra control software and can cause latency, packets arriving in the wrong order at the destination.

The main aim is not to select one contention resolution technique to implement in the network, but rather to try integrating all three techniques, resulting in much more depth of the network's ability to handle contention. For example, the authors from [27] simulate and investigate the effect of combining the three contention resolution schemes. Their rule of which scheme to use is as follows: A packet that loses the contention will first seek a vacant wavelength on the preferred output port. If no such wavelength exists, it seeks a vacant delay line. If no delay line is available it seeks a vacant wavelength on the deflection port. If all three schemes fail, the packet is dropped.

In [12] the authors suggest using the staggering switch. It assumes all packets are of fixed length, time is slotted and the arrival of packets is synchronized. The system has n inputs and n outputs and consists of two stages, the scheduling and switching stage. The scheduling stage is connected to the switching stage by m delay lines, d_i (i=1to m). The delay of the d_i delay line equals i packets. The scheduling stage distributes packets to the delay lines in such a way that, in any timeslot, no two packets arrive at the switching stage destined for the same output. In other words, the output collisions that occur at the inputs are resolved by delaying the colliding packets by different numbers of timeslots, so that when they arrive at the switch's output there are no output collisions. The scheduling and switching are done by electronic control. The control receives header information from all arriving packets and allocates them

to the delay lines. Therefore the electronic control should have knowledge of the content of the delay lines at any time. This requires quite a lot of electronic processing. The performance of the staggering switch is measured in terms of packet loss probability.

Contention is mainly found in the core and metropolitan networks since that is where optical switching is implemented. In [35] the authors suggest moving away from the core and focussing more on the edge or access part of the network in order to resolve, or in this case, reduce contention. They propose enhanced edge routers with a traffic-shaping function. This means that packets are sent from the edge nodes in such a way as to avoid contention occurring at the core routers. A similar scheme is proposed in [24] and is called contention aware slot shifting. In this scheme core switches collect slot information and calculate possible contending slots during a period *T,* then notify the edge nodes, which are responsible for the computationally intensive task of slot shifting. Therefore, the core node processing time for each slot is not affected (header processing and forwarding are not changed) and no extra hardware is required at the core switch. A time slot interchange system is also demonstrated in [20] by using the VAC OXS. This approach changes the order of packets to avoid contention.

N×1 contention resolution is demonstrated in [36] by using a N×1 (multi-stage) buffer for asynchronous variable length packets. The system consists of N fibre delay lines with different lengths. The outputs of all these fibre delay lines are coupled into one fibre. Therefore any input (N) could be switched to the output with a specific delay, by allowing it to pass through the corresponding fibre delay line. This is very similar to the staggering switch.

How contention is resolved has a great influence on network performance [26]. The network's performance is based on packet loss probability and quality of service. Packets are only dropped if all possible contention-resolving techniques are being used and no other contention resolution technique is available.

When one looks at Figure 2.2, the generic photonic packet switching node, one notices that at a single optical switch, the N inputs all carry the same wavelength. Other wavelengths are switched at other optical switches. Therefore, contention should first be resolved in the wavelength by using buffering and secondly (if a buffer is full) the contention can be resolved using a second wavelength.

In [37] the authors demonstrate an all-optical sub-system performing on-the-fly contention resolution in both space and wavelength domains. Error-free operation was obtained for 10 Gb/s NRZ and 40 Gb/s RZ packets but the system lacks a header in the packets, uses a 2x1 network and is very bulky and therefore not flexible at all.

The next problem occurs because variable length packets need to be stored while in the optical domain. No optical RAM is available and some solutions to store variable length optical data are discussed next.

2.5 Buffering variable length packets

Switching and buffering of variable length packets optically is a demanding task [33]. The use of a re-circulating buffer serves as a variable delay in [38]. A fixed delay length, T, is chosen and by passing the packet x times through this buffer, a delay of xT can be realized. The variable delay is set up by all-optical processing technology using an optical threshold function and a wavelength converter. This buffering concept is good for fixed length packets but suffers some problems when using variable length packets. With a combination of switches and different fixed length fibres between the switches, a more flexible variable optical buffer can be realized [1]. The VAC OXS can also be set up to deliver variable delays as discussed in [19].

A totally different method is slowing light down in the optical fibre. This can be realized by using a vertical cavity surface-emitting laser [39]. By varying the bias current around the lasing threshold researchers achieve variable delay of intensity-modulated signal input. In [40] the authors also propose building a variable optical buffer by slowing light down. The buffering effect is achieved by slowing down the optical signal using an external control light source to vary the dispersion characteristics of the medium via an electro-magnetically induced transparency effect.

2.6 The nature of data traffic

The packet starts with a header. The header is usually at a lower bit rate than the payload for electronic processing purposes. In some cases the header and payload has the same data rate.

The header has information about the destination of the packet, the length of the payload and some recognition bits to identify the header. The payload follows the header. They are usually separated by some guard time. The payload contains the data and is at very high bit rates. The payload can be either a fixed length for all packets on the network or of variable lengths for different types of data. Packets are sent across a network either synchronously or asynchronously.

Synchronously means that the timescale is divided into fixed length timeslots within which packets can be sent (slotted). In slotted networks all packets usually have the same length. Asynchronously means that the packets, usually of variable length, arrive at the optical switch randomly (un-slotted). Un-slotted networks have lower overall throughput than slotted networks because of the increased packet contention probability [28].

2.7 Header-processing techniques

The most common approach is to transmit the header in front of the payload at a bit rate that the photodiodes and processing electronics can support. By tapping optical power from the input fibres, the header is converted to the electronic domain to be processed to configure the optical switch as required. The header is normally a NRZ (Non Return to Zero) OOK modulated signal but according to [19], [41] when using a DPSK decoding scheme for the header or payload, enhanced performance with respect to extinction ratio and alleviation of the pattern effect is observed. In DPSK modulation the header information is encoded on the phase of a pulsed optical level. Higher header processing rates are possible when using DPSK modulated headers because of higher header extraction efficiency [41]. Higher header bit rates can also be achieved if optical header processing is implemented.

It is important to realize that electronic control does not imply an e-bottleneck, since the data (payload) are kept in the optical domain. In electronic processing the header is 4-16 bits long at speeds ranging from 155 Mbit/s to 622 Mbit/s. In optical header processing the header is only 2 or 4 bits long at a bit rate of 10 Gbit/s. More bits in the header mean more information can be stored but this also occupies more time. In optical header processing the header occupies much less time but the experimental set-ups are bulky and network and protocol

specific. In both cases the packet is optically stored in a buffer while the header is being processed.

The authors from [5] demonstrate a 1x2 all-optical packet switch. The header processing is done in the optical domain by employing the two-pulse correlation principle in a semiconductor laser amplifier in loop optical mirror (SLALOM). This process does not require optical clock recovery and therefore reduces the complexity of the header recognition system. A disadvantage is that the structure only works for well-chosen header patterns and Manchester encoding is required for the payload to ensure that the header's bits do not repeat in the packets payload. However, the system is bit rate transparent for both header and payload. The system is based on wavelength routing principles and can only handle one packet at any given time. If two packets arrive, one of them needs to be buffered to avoid packet contention. Although the header is processed optically, the packet still needs to be delayed to compensate for the time taken to carry out the optical header processing functions. The header is at 2.5 Gbit/s and the payload at 10 Gbit/s.

A demonstration of a 4-bit optical header processing system using a wavelength label switch based on optical digital to analogue conversion is discussed in [6]. In the wavelength label switch the digital optical header is converted to a single analogue pulse with different amplitude to discriminate the header pattern difference. This amplitude is used to select a wavelength of an electronically tunable laser. Depending on the header, the packet is then converted to a specific wavelength and switched accordingly. If the header is 1111 it exits on wavelength 1552.8 nm, if the header is 1010 it exits on wavelength 1553.6 nm and if the header is 1110 it exits on wavelength 1558.9 nm. These three wavelengths then exit the optical switch via an arrayed waveguide grating, each one on a separate output port. The electronic domain is used to control the tunable laser, but no processing is done in the electronic domain. The disadvantage of such a system is the limit (four) in the number of bits in the header and also that there are no contention resolution capabilities.

A unique all-optical 1×2 self-routed optical switch is discussed in [42]. The header bits (three) are optically processed in parallel to route optical packets from one input to one of two possible outputs. This parallel processing increases the switching speed.

2.8 Transparency in optical networks vs. all-optical networks

Transparency can be realized in optical networks and has far-reaching consequences for expanding and upgrading the future optical network [12]. Transparency and "all-optical networks" are not synonyms [43]. Transparency refers to the fact that the network is bit rate and protocol independent. This means that many different types of data can be sent across the network without any concern about meeting specific speeds or network protocols. For transparency to be realized the data have to remain in the optical domain all the time from source to destination because if the data are converted to the electronic domain, processing and control functions are required, which require the data to be in a specific protocol and bit rate. To route the data across the network, a header at a specific speed and protocol is used, converted to the electronic domain to perform the control and switching functions at the nodes.

'All-optical networks' means that everything happens in the optical domain. Signal processing, packet switching and other control function are all realized in the optical domain. There is no need for the electronic domain in an all-optical network.

2.9 Ultra-high speed optical packet switching

Very high and fast (160 Gb/s up to 320 Gb/s) all-optical switching is demonstrated in [44] [45]. These high rates are achieved by WDM and ultra-fast modulation techniques. The principle of the system is very similar to general photonic packet switching, as has been discussed. The packets are generated, split (with coupler) and one part is delayed while the other part is processed to control the optical switch. At this high speed optical flip-flop memory is used to assist in the switching function. These systems do not have a very high number of input and output ports, typically one or two input and output ports.

CHAPTER 3: ELECTRONIC CONTROL DESIGN

3.1 Introduction

The VAC OXS has an electronic control circuit consisting of a XC9572XL Complex Programmable Logic Device (CPLD) and 16 separate current control circuits. This electronic circuit forms part of the OXS package and therefore if one wants to control the OXS electronically, it needs to be done via this current control circuitry. Each one of these current control circuits controls the flow of current through the corresponding switch cell. In the previous experiments on the OXS, it was electronically controlled by control signals sent directly from the PPG to this current control circuitry. Optical packets are sent to the OXS and at the same time, pre-determined control signals are sent to the electronic control to open the correct switch cells for these packets. This approach to controlling the OXS can be seen as pre-determined switch cell operation and cannot be implemented in a realistic photonic packet switching network because of the random nature of data on the network.

A new approach is needed through which the OXS is electronically controlled depending on the input packets arriving at the OXS. In order to control the OXS without any knowledge about the sequence or occurrence of the data, an electronic control is needed that can determine the state of the PPS network at the OXS and make a decision on how to configure the OXS, for example which switch cells to switch open and how long to keep the corresponding switch cell open. In order to determine the state of the PPS network, processing is needed, and therefore the optical packets need to be converted to the electronic domain. In the electronic domain the headers of these packets are processed and the current state of the PPS network is determined. The header of the optical packets should have information on the length and desired output port of the packet.

3.2 Aims of the electro-optic control interface

The aim is to design a new electronic control circuit that monitors the packets just before entering the OXS in order to determine the state that the OXS should be in. This new electronic control should interface with the existing current control electronics. Tapping some of the optical power from the input optical fibres and converting the packets from the optical

domain to the electronic domain should be done just before the packets enter the OXS. Only the header part of the packet is used for the processing. Depending on the input received and information processed, control signals are sent to the OXS's current control electronics to configure the OXS's switch cells.

The requirements and specifications for the new electronic control circuit include:

- It must have four photodiodes, one for each input, to convert the packets from the optical to the electronic domain.
- Conversion of the packets from the optical to the electronic domain at a bit rate of 155Mbit/s.
- The design of an interface from the photodiode's output to the CPLD's input port. The CPLD requires digital signals with transistor-transistor logic standard voltage signals. This is 0 V for low and 3.3 V for high.
- A fast CPLD to do the processing. It should have a clock input at 155MHz, be able to receive, process and send signals at 155 Mbit/s. It should have enough input and output ports. It should also have enough memory (macrocells) so that it can be programmed to control the OXS.
- A packet format or protocol will be established and processing will be done based on the information in the packet's header.
- The electronic circuit must be implemented on a printed circuit board (PCB).
- The control signals from the new electronic control must be sent via PCB mounted SMA connectors to the existing electronic control of the OXS. The existing electronic control also has PCB mounted SMA connectors and therefore the two circuits' boards will be connected with an SMA cable.
- The CPLD on the new electronic control board must be programmed using the JTAG connector.
- The PCB must be supplied with sufficient power for all the components.

3.3 The existing current control circuitry

A switch cell on the OXS is switched on by a flow of current through the active coupler. There are 16 separate switch cells, each with its own electronic circuit to switch it on or off. The

current control circuit for one switch cell is shown in Figure 3.1. The current through the switch cell can be controlled manually or electronically. Variable resistor R2 can be manually selected to control the flow of current supplied by the LM317. In the off state (R2 = 0 Ω) no current is supplied to the switch cell irrespective of the control signal from the CPLD. In the on state (R2 = 1 kΩ) current is supplied to the switch cell only if the control signal from the CPLD is low. If the control signal from the CPLD is high, the p-channel MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is off and no current flows through the switch cell.

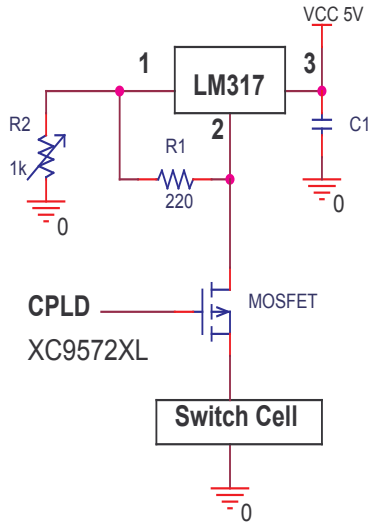


Figure 3.1

The existing current control circuit for one switch cell. The switch cell can be manually switched on or off with resistor R2 or electronically via the CPLD input.

All 16 switch cells are controlled with control signals from the XC9572XL CPLD via its specific current controlled circuit. Sixteen output ports forming the XC9572XL CPLD are connected to the 16 control circuits. The XC9572XL CPLD has four inputs; one is for a clock input and in previous experiments, the other inputs were used for control signals from the PPG. With this new electronic circuit board, three of these inputs will be used as interfaces from the new electronic control board. The clock signal is supplied by the PPG to the new electronic control board. The clock signal is then also sent to the existing electronic circuit from the new control circuit board.

3.4 Circuit diagram for the new electronic control

The functional block diagram is given in Figure 3.2. Firstly the four optical inputs are converted to the electronic domain. These four inputs represent the four inputs to the OXS and will carry the header signals of the packets. When converted to the electronic domain, they need to be reshaped before entering the processing unit. The processing is done and will require some DC power levels, a clock signal and a communication link to be programmed with. After the processing has been done, six output interfaces are required to send control signals to the OXS.

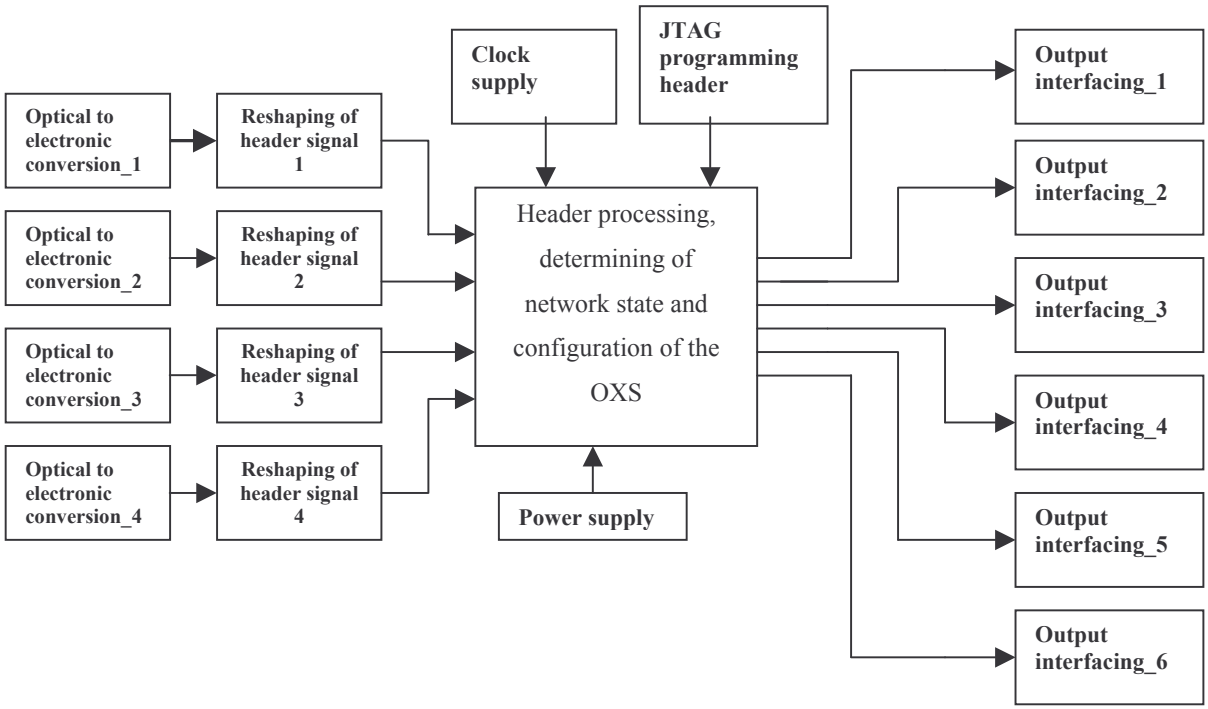


Figure 3.2

Functional block diagram of the electro-optic control interface

3.4.1 The PINFETs

The term PINFET (p-intrinsic-n Field-Effect Transistor) indicates the integration of a PIN photodiode with a high-performance trans-impedance amplifier. The PINFET is constructed of InGaAs (Indium Gallium Arsenide) with a high responsivity in the 1100 nm to 1600 nm wavelength range. Light is coupled into the detector through a single mode optical fibre

pigtail. The fibre pigtail is actively aligned with the detector and soldered in place to provide a stable coupling mechanism.

The PINFET photodiode was chosen over the PIN photodiode because of its low sensitivity of –35 dBm, high bandwidth of 350 Mbits/s, responsivity of 0.95 A/W at 1550 nm and typical output voltage level of 2.5V, DC coupled. The PIN, on the other hand, has similar specifications, can support a bandwidth up to 2.5 Gbits/s and with typical output voltage levels of 0.5V, AC coupled. The main reason for choosing the PINFET was its high output DC coupled voltage level. Although the PIN photodiode has a bandwidth of 2.5 Gbit/s, its output voltage is too low and electronic processing of signals at this high data rate is not required. The output voltage characteristic of the PINFET photodiode was tested at a reverse detector bias of –5 V and supplying the trans-impedance amplifier with only +3.3 V. The results are shown in Figure 3.3. The PINFETs are supplied in a 14-pin dual in-line package offering high reliability.

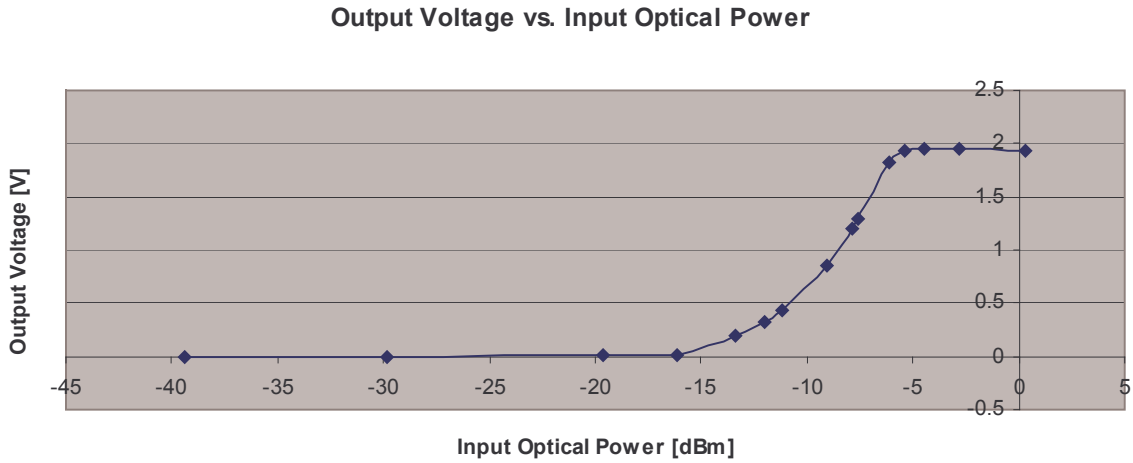


Figure 3.3

The output voltage characteristics of the PINFET [46]

The experiment was done by increasing the current through a 1550 nm laser diode and connecting the output of the laser to a 3 dB coupler. One of the coupler's outputs was connected to the optical power meter while the other output was connected to the PINFET. The results clearly show that if an optical input power level of about –5 dBm (for high) and optical input power of –20 dBm (for low) enter the PINFET, the resulting output voltage is 1.95 V for a high or '1' and 0 V for a low or '0'.

By supplying the trans-impedance amplifier with a negative supply voltage, the output voltage's low level was measured at –0.7 V. This signal needs to be processed by a CPLD whose minimum input voltage is –0.3 V and therefore the negative supply of the trans-impedance amplifier was grounded. Four PINFETs were chosen, one for each input to the OXS. Figure A.1 shows the schematic diagram of the biasing of the four PINFETs and the electronic circuit for interfacing the PINFET's output to the CPLD.

Pin 1 of the PINFET is the detector bias input and is supplied with –5 V. Pin 10 is the trans-impedance amplifier's positive supply and is connected to the 3.3 V DC supply. A 0.1 µF bypass capacitor is connected between pin 1 and ground and also pin 10 and ground to reduce any potential voltage ripples from the power supplies. Pin 7 is the output from the trans-impedance amplifier and is fed to the positive input of the voltage comparator. This output is seen as an analogue signal and is converted to a digital signal by the comparators. Pins 3, 4, 5 and 8 are grounded. The name of the ground is AGND, referring to the analog ground plane. A 110 Ω (refer to section 3.5.4 for the calculations) resistor matches the PINFET's output to the PCB's track impedance. These resistors are named M15, M16, M17 and M18. Pins 2, 6, 9, 11-14 are not connected. The blue lines on Figure A.1 represent the single mode optical fibres entering the PINFETs.

3.4.2 The voltage comparators

The output from the PINFET needs to be converted/interfaced to the input port of a CPLD so the signal can be processed. The CPLD accepts inputs with a low voltage level at 0 V and a high voltage level at 3.3 V. Therefore the 0 V to 1.95 V signal from the PINFET needs to be converted to a 0 V to 3.3 V signal. The two ways of doing this at 155 Mbits/s include the use of an ultra-fast voltage comparator or voltage amplifier with high gain causing saturation at 3.3 V. The output from the PINFETS, although it is digital information, is regarded as an analog signal. Therefore analog-to-digital conversion, or to be more precise, reshaping of the analog signal, should also be done to ensure the input to the CPLD is a high-quality digital signal. The best-suited component for this job was defined as the AD8611 – ultra-fast single supply voltage comparator. The AD8611 has a rise time of 2.5 ns and a fall time of 1.1 ns and is therefore capable of supporting digital signals at a bandwidth of 155 Mbits/s. The schematic diagram of these four AD8611 microchips interfacing with the PINFETS is shown in Figure

A.1. The input from the PINFET is connected to pin 2 (+IN) of the AD8611. The negative input (-IN) of the AD8611 is biased with a reference voltage of 0.97 V. A simple voltage division circuit created this 0.97 V. A 10 kΩ resistor, connected to 5 V, in series with a 2400 Ω resistor, connected to ground, results in 0.97 V between the two resistors and is supplied to (-IN). The 0.97 V was chosen as the reference since it is halfway between the minimum and maximum voltage that will enter the AD8611 from the PINFET. Pins 4, 5 and 6 are grounded. Pin 1 is connected to the positive power supply of 5 V.

A 1 µF bypass capacitor is placed between the positive power supply pin and ground. Another 10 nF ceramic capacitor is placed as close as possible to the device in parallel with the 1 µF bypass capacitor. The 1 µF capacitor will reduce any potential voltage ripples from the power supply and the 10 nF capacitor acts as a charge reservoir for the comparator during high frequency switching. Pin 8, an inverse of the output, is left unconnected. Pin 7 is the output with a voltage level of 0 V for a low and 3.3 V for a high. This output is connected to the CPLD as input. Two 100 Ω resistors, one at the AD8611 side and one at the CPLD side, provide matching to the PCB track of 110 Ω.

3.4.3 The CPLD

A CPLD was chosen to do the processing. It is defined as the industry's best and fastest CMOS CPLD. The Xilinx CoolRunner-II CPLDs are fabricated on 0.18 micron process technology. CoolRunner-II CPLDs employ a design technique that makes use of CMOS technology in both the fabrication and design methodology. This design technology, also known as RealDigital, employs a cascade of CMOS gates to implement the sum of products instead of traditional sense amplifier methodology.

A Xilinx CoolRunner-II XC2C32 CPLD in a VQ44 package has a 3 ns pin-to-pin logic delay and can support system frequencies up to 333 MHz. It has 33 input/output pins and was identified as the best CPLD for the design. The other two types of packages included the PC44 and CP56. The VQ44 with its surface mount pins promised to be the best solution. The schematic diagram of the CPLD with its connections to the rest of the schematic diagram is show in Figure A.2.

The CPLD is clocked in one of two ways. The user can select the option by selecting the correct configuration for header J4. Refer to the schematic diagram in Addendum B, Figure B.1. The first option is the on-board 1.8432 MHz clock mostly used for testing the board and low-speed applications. The second option is an external clock via the SMA1 connector that uses pin GCK2 of the CPLD. This option will be used to connect an external 155 MHz clock signal to the circuit.

The main power supply to the CPLD is the 1.8V supplied to pin VCC. The VCCOIA and VCCOIB power pins are supplied with 3.3 V and define the input and output voltage levels for the CPLD. The VAUX pin is also supplied with 3.3 V and is also known as the JTAG supply voltage. Each of these four power pins is supplied with a 0.047 µF capacitor that serves as a charge reservoir for the CPLD during high-frequency switching. The reset pin (GSR) is connected to a push button. It is always high but when pressed, makes pin GSR low, resulting in a reset. Four LEDs and one other push button are also connected to the CPLD to assist in debugging and testing of the CPLD. The JTAG programming header also connects to the CPLD on the corresponding pins. The CPLD is programmed from a computer. The computer needs a parallel port. The JTAG programming cable acts as the interface between the computer and the circuit with its parallel connector and 6-pin header connector.

3.4.4 Power supply

The CPLD is supplied with a different power source than the PINFETs and comparators. The reason is that different voltage levels are required and it is necessary to reduce the noise from different parts of the circuit (analogue and digital side). For the CPLD an LM-1117-3.3 V regulator is used together with an LM-1117-1.8 V regulator. The PINFETs and comparator are supplied with 5 V from an LM7805CT, with 3.3 V from an LM-1117-3.3 V and with –5 V from an LM7905CV regulator. All the regulators have 10 µF bypass capacitors connected just before the input of the regulator to reduce any potential voltage ripples from the main power supplies. A 10 µF tantalum capacitor on the output port of the regulator is for proper operation and to improve high frequency load regulation. A high-quality tantalum capacitor was used to ensure that the ESR (effective series resistance) is less than 0.5 Ω.

3.4.5 The SMA output ports

The circuit has seven SMA connector outputs connected directly from six of the CPLD's output ports. The seventh one is used for the 155 MHz clock and is connected to the CPLD's GCK2 port. Space is reserved for two matching resistors, one on the CPLD's side and one on the SMA's side. These are to ensure the circuit is matched to the transmission line. The circuit diagram of the SMA outputs is shown in Figure A.3.

3.5 Printed circuit board design

The schematic diagram of the electronic circuit was physically implemented onto a PCB. Owing to the high-speed (155 Mbit/s) requirement of the control electronics, the physical characteristics of implementing the design onto the PCB contributes to the behaviour of the circuit just as much as the parts of the electrical design that are included in the schematics. Physical characteristics such as impedance matching, transmission line propagation, delay, characteristic impedance (Z_o), PCB material, relative permittivity or dielectric constant (ε_r), size, stack-up, placement of components, packaging and grounding are not all included in the schematic diagram and must be taken care of when designing the PCB from the schematic diagram. If not seriously considered they will lead to problems with signal integrity. The main concern in PCB design is the characteristic impedance of the high-speed signal tracks, how many layers will be used in the PCB and how will they be stacked on top of one another.

The two losses of greatest concern are caused by signal reflections, due to impedance mismatch or impedance changes and the loss of signal energy into the dielectric of the material. The loss tangent (tan (δ)) is a measure of how much of the signal pulse (electromagnetic wave) propagating down the PCB transmission line will be lost in the dielectric region (insulating material between copper layers). Relative permittivity (ε_r) is a measure of the effect an insulating material has on the capacitance of a conductor embedded in the material or surrounded by it. It is also a measure of the degree to which an electromagnetic wave is slowed down as it travels through the insulating material. The higher the relative permittivity, the slower a signal travels on a trace. The amount of signal loss in a circuit is not only a function of material type but is also a function of frequency and line length in or on the PCB.

Frequency must be viewed differently in digital circuits than in analog circuits. Analog signals consist of sine waves and variations of sine waves. When a sine wave is launched into a transmission line, the frequency of the sine wave propagates unchanged but the amplitude will drop off owing to the effects of loss tangent. Since analog signals are sine wave in nature, loss tangent causes a reduction in signal amplitude as the signals propagate. The further a signal travels, the greater the reduction in amplitude. In contrast digital signals are square waves, which consist of a series of embedded sine waves called harmonics. When a digital signal propagates through a transmission line, each of the sine wave harmonics in the rising and falling edge lose amplitude, as the signal propagates, due to loss tangent, with the highest frequency harmonics suffering the highest losses. The loss of amplitude of the harmonics is manifested as a degradation of rise and fall time of the signal. This can seriously affect timing of level-sensitive signals and can affect both timing and circuit performance of edge driven signals (clocks, enables, resets, etc.).

The electronic signals, converted by the PINFET from the optical domain to the electrical domain, are analogue signals. It is still seen as an analog signal when it enters the voltage comparators. The input and output of the CPLD are however seen as digital signals. To avoid the analog and digital signals affecting one another, the analog was designed on the left-hand side of the PCB while the digital signal tracks were designed on the right-hand side of the PCB. The CPLD was placed in the middle of the PCB. They were also designed on different ground planes to assist with reducing the crosstalk.

3.5.1 The layer stacks

The layer stack specifies the arrangement of circuit board layers, the dielectric constant of the substrate and the spacing between layers. Because of the complexity of the schematic design, a four-layered PCB was chosen. The top and bottom layer are reserved for high-speed signal traces. The second layer will be used to route the power supply tracks and the third layer is reserved for the continuous ground planes. Figure 3.4 shows the side view of the PCB with the relevant layers and their thickness. (These heights and layer stacks are recommended in [47].)

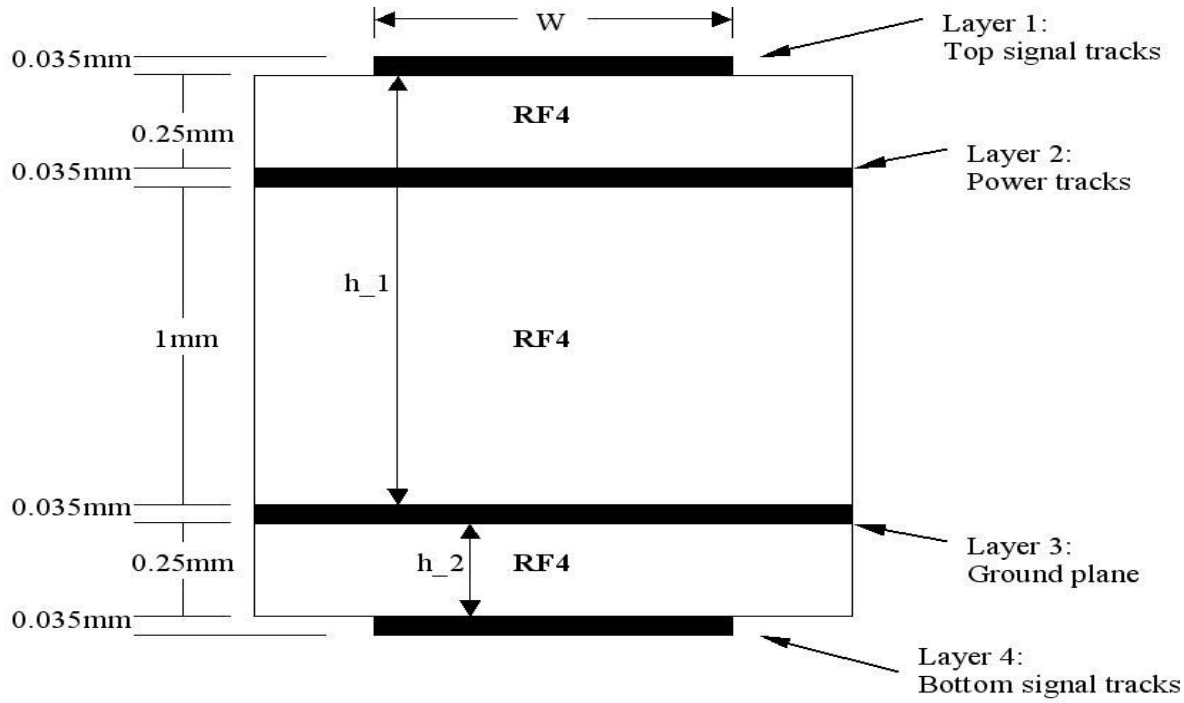


Figure 3.4

The layer stack (side view of the PCB)

The dielectric layer or substrate is chosen as RF4 with a dielectric constant of 4.4. Copper is used as the conducting material to build and route the signals. The thickness of the copper is fixed at 0.035 mm. The total board thickness is 1.64 mm. The inner power and ground layers are 0.25 mm below the surface and are separated from one another by 1 mm. For the impedance calculations the height of the signal traces above ground plays an important role. For the top signal trace the height above the ground plane is defined as h_1 and for the bottom traces the height below the ground planes is defined as h_2.

3.5.2 Component layout and packaging

The Coolrunner II CPLD is placed in the middle of the PCB. EAGLE 4.11 software was used to design the PCB layout. Refer to Figure A.4 for a top view of the PCB layout. The PCB measures 23.88 x 113.93 mm. The PINFETs and comparators are placed on the left-hand side of the board and six of the SMA connectors used as the outputs are placed on the right-hand side. The power supplies and power connectors are placed at the bottom of the board. The SMA for the 155 MHz clock is placed at the top of the board, closest to the GCK2 pin. The

on-board clock is also in the top half of the board with the test LEDs and pushbutton. The JTAG header is placed just below the CPLD.

Most of the components are in the surfaced mount package because of the high-speed operation and easier routing. Only the PINFETs, in the 14-pin dual in-line package, and the SMA (right-angled PCB mounted) connectors are not in the surfaced mount package. They are connected to the PCB by drilling holes in the PCB and placing (soldering) their pins to the lower tracks of the PCB. These tracks are then simply routed to the top layer with a via.

The high-speed tracks are routed from component to component by avoiding right-angle bends because a right-angle bend looks like a capacitive load attached to the transmission line [47]. Bending at 45 degrees causes fewer reflections and signal rise-time degradation, and was therefore implemented.

3.5.3 The analog and digital ground

A continuous ground plane in the PCB on layer 3 was designed allowing only breaks in the plane for necessary vias. At high frequencies the return currents follow the path of least inductance, not the path of least resistance. The lowest inductance return path lies directly under a signal conductor. The ground plane provides a low inductive current return path for the signals, thus eliminating any potential differences at different ground points throughout the circuit board caused by “ground bounce.” A ground plane will also minimize the effects of stray capacitance on the board, provide a stable reference voltage for exchanging digital signals and control the crosstalk between signals.

Figure 3.5 shows the top view of the PCB with the analog ground on the left-hand side and the digital ground plane on the right-hand side. The white line where the two ground planes are separated can be seen clearly. The two ground planes are connected only at one point, at the bottom of the PCB between the two power supplies.

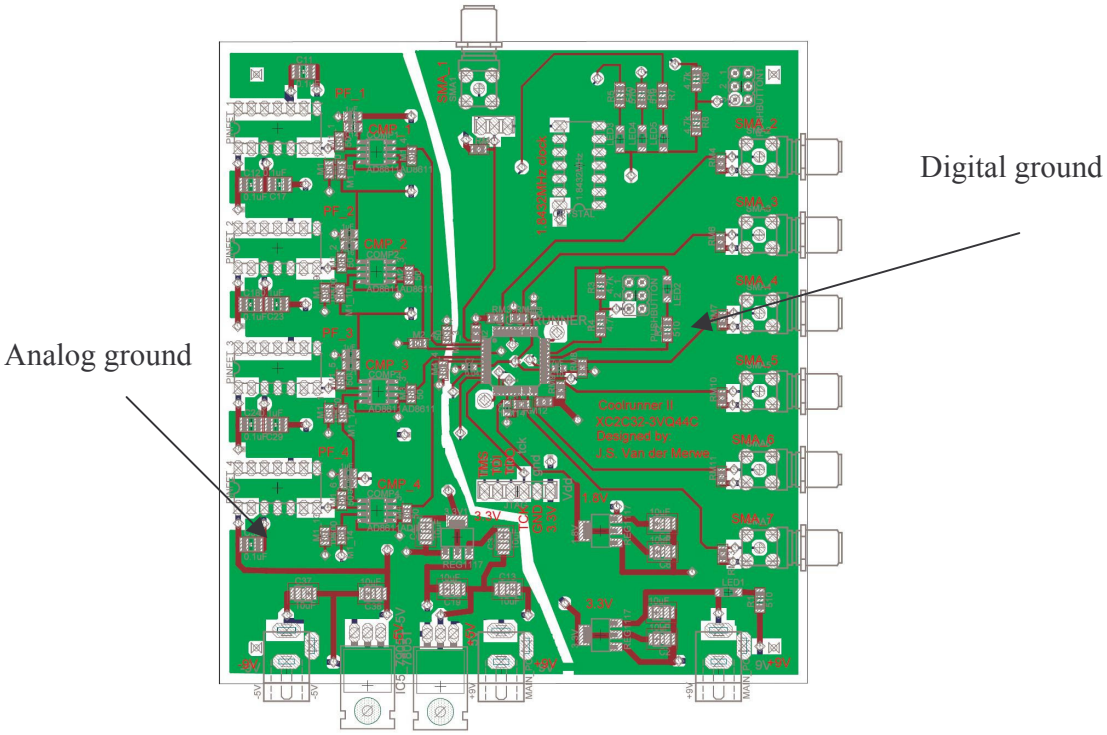


Figure 3.5

The top view of the PCB showing the two ground planes

3.5.4 Track impedance calculation

Dielectric thickness and trace width both play a key role in transmission line impedance. Correct calculation of each is necessary during the design of the PCB. Copper thickness *t* plays a minor role in the impedance of a transmission line. A 20% change in copper thickness will cause only a 3% change in characteristic impedance, Zo. The thickness of the copper is 0.035 mm. The characteristic impedance is mostly influenced by the *w/h* ratio, with *w* being the track width and *h* being the height above ground.

The output impedance of the PINFET, the input and output impedance of the comparator and the input impedance of the CPLD are all 1kΩ. Therefore the three areas where the track impedance needs to be calculated in order to provide matching is on the high speed connections between the PINFETs and voltage comparators, the voltage comparators and the CPLD, as well as between the CPLD and the SMA outputs. These connections are physically implemented on the top layer as a track. For the top layer the height, *h_1* above the ground plane is 1.285 mm and the width of the track is 0.4 mm. The bottom tracks are only used for

control signal routing and minor signal routing and owing to the slow speeds of these signals, no impedance matching is needed, therefore no impedance calculations. The RF4's dielectric constant is: ε_r=4.4. Using equation 3.1 from [48], which takes into effect the tracks' width and height about ground, the impedance of the lines is calculated as Z_0 = 110.98Ω.

$$Z_0 = \frac{87}{\sqrt{(\varepsilon_r + 1.41)}} \ln\left[\frac{5.98h}{0.8w + t}\right] \quad [\Omega] \tag{3.1}$$

Using equation 3.2 from [49], which ignores the thickness of the copper track but requires the effective relative permittivity (ε_{eff}), the impedance was calculated as 113.2 Ω and verifies that of equation 3.1. Effective permittivity is calculated as 2.97 from equation 3.3.

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \quad [\Omega] \tag{3.2}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + 12\,h/w}} \tag{3.3}$$

The impedance is then matched by placing a 110 Ω resistor between the copper track and ground at the output pin of the PINFET to match the output of the PINFET to the transmission line. 110 Ω resistors were also placed at the output of the voltage comparators and the CPLD to match those signals to the transmission line as well.

3.6 The electronic control's response to a packet with a 155 Mbit/s header and 10 Gbit/s payload

Packets were generated and sent to the electronic control to test the response of the electronic circuit to these packets. A typical packet with 155 Mbit/s header, 12.8 ns guard time and 140 ns long payload at 10 Gbit/s was used for the tests. Figure 3.6 shows this packet in the optical domain. The header is a four-bit sequence: 1010. The payload is a random PRBS.

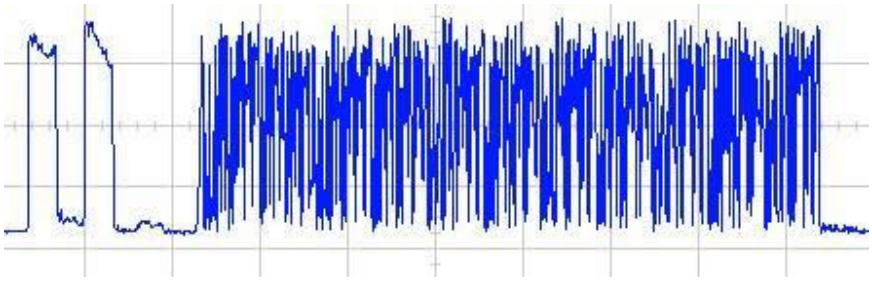


Figure 3.6

A packet, in the optical domain, used to test the electronic control [20ns/div]

The average optical input power was measured at –10 dBm. A VOA (Variable Optical Attenuator was placed in front of the PINFETs to adjust the optical power level. The electronic signal was then measured just before the CPLD with the VOA set at different attenuations. The results, electronic signals measured on the PCB, are shown in Figure 3.7.

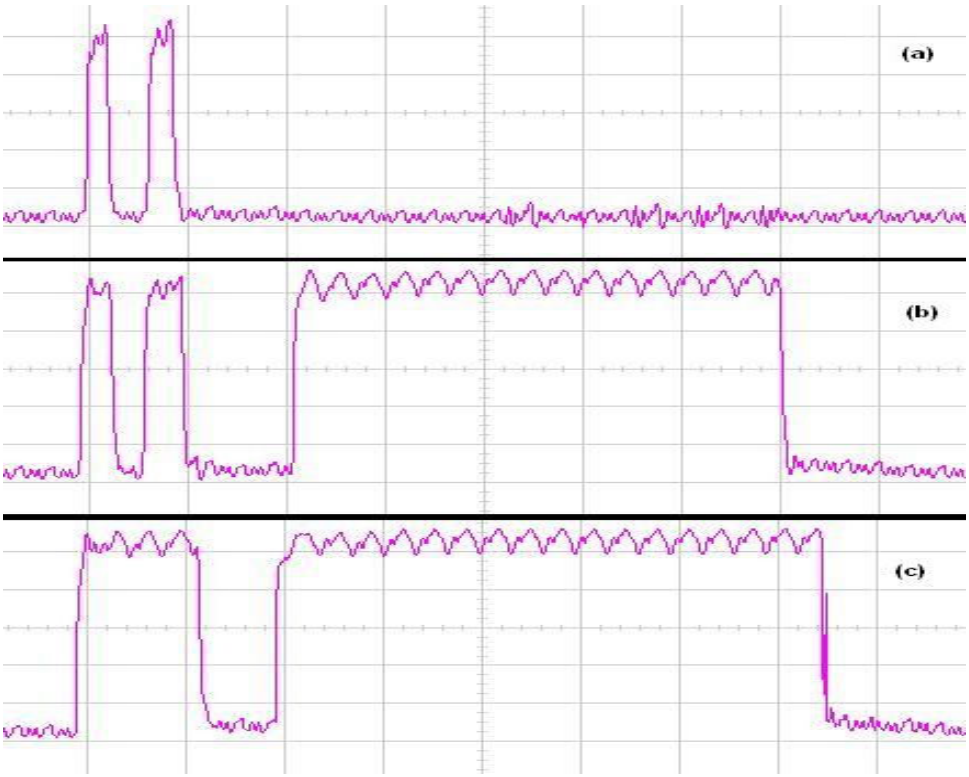


Figure 3.7

The packets measured on the PCB just before the CPLD (in the electronic domain) with (a) the VOA at 8.5 dB, (b) the VOA at 6.1 dB and (c) the VOA at 4.2 dB. The time scale is 20 ns/div.

With the VOA set at above 10 dB, no signal was measured because the optical power entering the PINFET was too low. With the VOA at 8.5 dB the electronic signal starts to be detected. Only the header is recovered, shown in Figure 3.7 (a). If the VOA's attenuation is decreased to 6.1 dB, meaning more optical power enters the PINFET, the payload is also detected but because of the high speed of the payload, it is only seen as a continuous high, as shown in Figure 3.7 (b). With the VOA's attenuation set even lower, at 4.2 dB, the header also becomes continuously high (refer to Figure 3.7 (c)) and therefore it is very important to control this optical input power to the PINFETs to ensure that the header is perfectly recovered and can be processed by the CPLD.

These tests prove that the electronic control is working as planned. Now the optical network has to be set up to implement this electronic control and demonstrate its flexibility in photonic packet switching.

CHAPTER 4: EXPERIMENTAL SET-UP

4.1 Introduction

The aim with the optical network design is to generate various types of packets and send them to the OXS, thus subjecting the crosspoint switch to different photonic packet switching scenarios. Some of these scenarios include sending packets from one input to multiple outputs and sending different length packets to show the flexibility of the electronic control. The output port and length of the packets are encoded in the header information and therefore the corresponding switch cell can be switched open for the desired length. Before the design of the optical network, the OXS needs to be characterized in order to determine which switch cells are the best ones to use.

The length of the header will also be increased from 4 bits to 8 bits and 16 bits to show the flexibility of the electronic control in processing more complex headers once again. The main aim will also be addressed. This includes subjecting the crosspoint to a contention resolution scenario in which the electronic control should detect the contention and successfully resolve it.

4.2 Characteristics of the VAC OXS

The switch cells are characterized by the amount of optical power lost, by the packet being switched at the corresponding switch cell, from the input optical fibre to the output optical fibre. The characterization experiment was set up as described below. A continuous stream of PRBS data was used as the input. A variable optical attenuator was placed in front of the OXS and set in such a way as to ensure that the average optical power entering the crosspoint switch was 0 dBm. The switch cells were then switched open by sending a control signal from the pulse packet generator to the control circuitry of the OXS. This pulse is always high (3.3 V) and only becomes low (0 V) every 1.107 μs for 220 ns, resulting in a duty cycle of about 20%. Adjusting the variable resistor in the control circuitry manually controls the current through each individual switch cell. Therefore the switch cells are opened and closed as one opens and closes the variable resistor. This results in an output pulse at the output of the corresponding switch cell. This output pulse has optical power pulses of about 170 ns at every

1.107 µs. This optical power increases as more current is sent through the switch cell. All 16 switch cells were tested by connecting the input power to the four inputs of the OXS and then measuring the output optical power at the output port of the switch cell under testing. The polarization was kept constant. All 16 these transfer characteristics are plotted on a graph in Figure 4.1. The results were the same for sending optical power in both directions through the OXS, showing that the OXS is not dependent on the direction of optical power flow. This means using W, X, Y, Z as input and 1, 2, 3, 4 as output is the same as using 1, 2, 3, 4 as input and W, X, Y, Z as output. The results resemble those of the packaged OXS characteristics of [18].

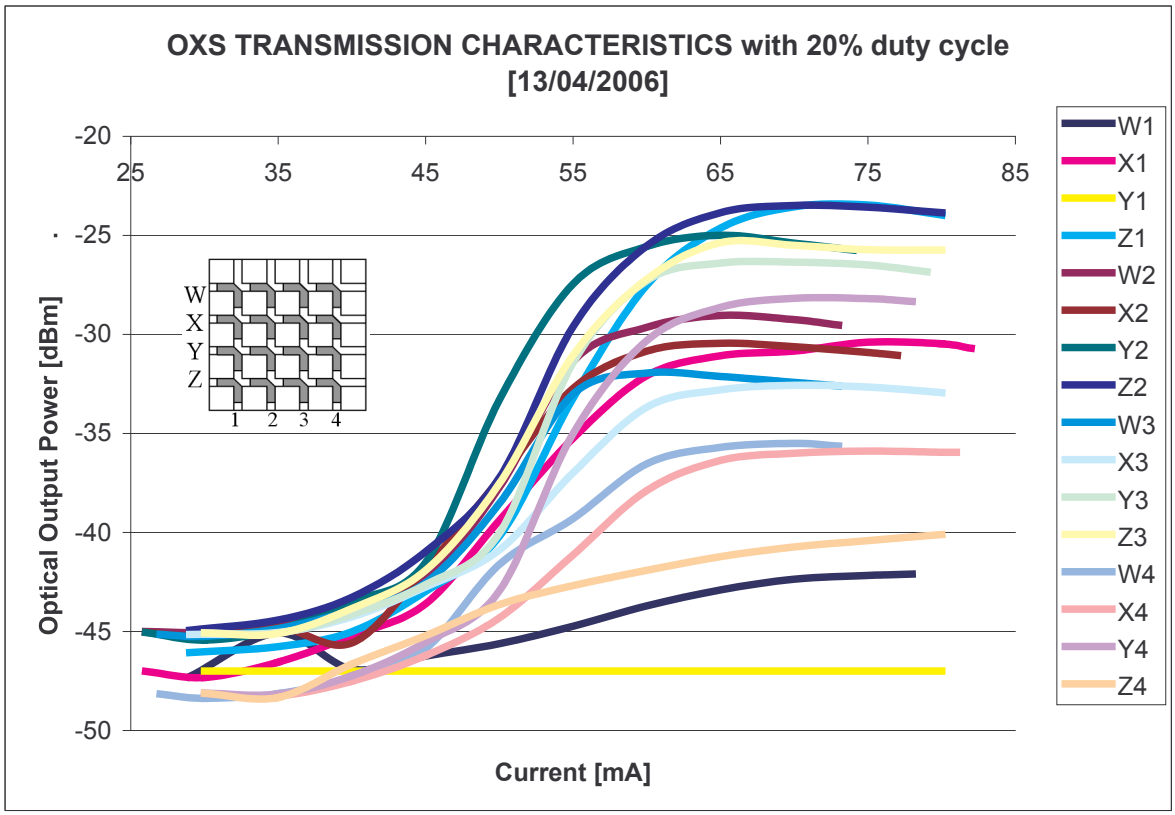


Figure 4.1

The transmission characteristics of all 16 switch cells of the OXS

The results revealed that when the switch cells are in the OFF state, 25-35 mA of current flows through the switch cell and about –47 dBm of optical power is measured. The maximum optical output power, about –24dBm to –33dBm, was measured when the current was increased to 70 mA. Above 70 mA the switch cell showed a slight decrease in optical output power. This is where multicasting starts, as demonstrated in [21], [22]. This current is only a

5th of the real current value owing to the 20% duty cycle switching window. This 20% duty cycle was required to avoid damage to the switch cell by overheating.

The two best switch cells are Z2 and W3. They have a loss of about 23 dB. Switch cell Y1 is clearly broken. On average a switch cells causes an optical power loss of about 25-30 dB.

4.3 A typical packet

The optical network is dependent on the type of packets used. From the research finding one sees that previous experiments had the header and payload on different wavelengths separated by 103 ns guard time. In a network that carries a lot of traffic, this will increase the strain on the management. The researcher proposes a different way of transmitting the header and payload. Figure 4.2 shows an example of such a packet. The header and payload will be on the same wavelength and separated by 12.8 ns (guard time). The header for the experiments will either be a 4-bit or 8-bit code at 155 Mbit/s, depending on how much information needs to be encoded in the header. The payload, a PRBS, will be about 100 ns-300 ns long. Packets will be sent at the beginning of each timeslot (1.107 μs).

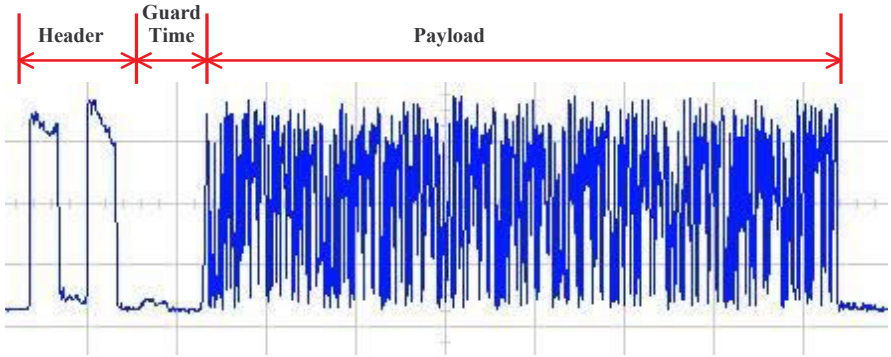


Figure 4.2

A typical packet used in the experiments. The header (a 4-bit code: 1010 at 155 Mbit/s) is in front, followed by a 12.8 ns guard time and the PRBS payload at 10 Gbit/s.

4.4 Determining the rise and fall time of the OXS

By sending continuous 10 Gbit/s data into the OXS and controlling the switch cell with a 20% duty cycle switching window, a very important characteristic was determined. This is the rise

and fall times for the switch cell. It is the time taken from when the switching window control signal is sent to the switch cell until the optical output power is stabilized at maximum (switch cell in ON state). The fall time is the time it takes the switch cell to be switched from the ON state to the OFF state, when about –45d Bm of optical power is measured. Figure 4.3 (a) shows the inverted switching window. The packet, Figure 4.3 (b), was measured on the same oscilloscope screen (the optical channel) but experienced an 80 ns delay relative to the switching window due to the length of fibre used for measuring and oscilloscope measuring delay. The switching window, SW, is drawn on top of the packet. The switching window is 220 ns long but the packet is only 170 ns long and this is due to the slow rise time response of the switch cell. The rise time, R, is measured on Figure 4.3 (b) as 75 ns.

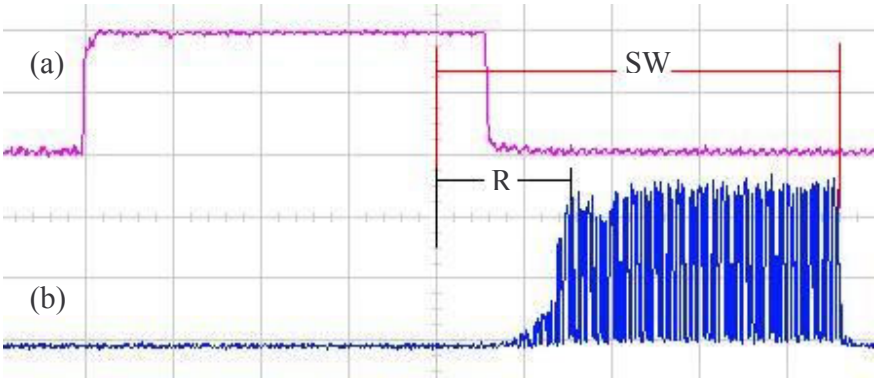


Figure 4.3

Rise time determination. The switching window (a) and the optical power being switched (b) are shown. SW is the switching window redrawn over the "optical packet". R is the rise time. The scale is 50 ns/div.

To measure the fall time, the time division was set to 1 ns/div to zoom into the end of the packet. Figure 4.4 shows the fall time, F. It is measured as 2.2 ns. These rise and fall times are a very important consideration when designing the optical network because no data can be switched during this time. The packet that is being switched must fall in the time when the switch cell is fully opened.

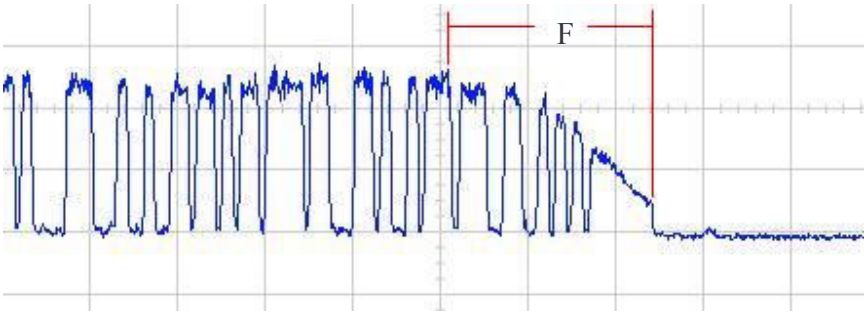


Figure 4.4

Fall-time determination. F is the fall time, measured as 2.2 ns, and is the time it takes the switch cell to switch from the ON state to the OFF state. The scale is at 1 ns/div.

4.5 Packet generation

The packets that were used in the experiments all had the same basic structure. These packets' specifications varied for the different experiments. Programming the PPG (Pulse Pattern/Packet Generator) (Anritsu MP1758A) with the specified sequence generated the packets in the electronic domain. The clock signal of the pulse packet generator is 10 Gbit/s and therefore the 155 Mbit/s header was created by 64 consecutive ones for a '1' at 155 Mbit/s and 64 consecutive zeros for a '0' at 155 Mbit/s. At 10 Gbit/s, the period for one bit is 100 ps and therefore 100 ps * 64 are equivalent to a period of 6.4 ns, corresponding to a bit rate of 156.25 Mbit/s to be exact.

This information from the PPG is then sent to the modulator (MOD) with an SMA cable. The modulator used is a 10 Gbit/s integrated amplitude Mach-Zehnder modulator built with Lithium niobate material and with an "X-cut, Y-propagating" crystal orientation. Using Agilent's tunable laser source, the "8164A Lightwave Measurement System", a continuous light wave at 1552.52 nm, was sent into single mode fibre. Figure 4.5 shows the optical spectrum of this output measured with the optical spectrum analyzer. This light is at 4.6 dBm of optical power and is then passed through a polarization controller before it enters the modulator. The polarization controller was adjusted so that the light enters the modulator with the correct polarization for the most efficient modulation. The packets from the PPG then exit the modulator in the optical domain. At that stage the average optical power is about –13 dBm to –15 dBm, depending on the polarization settings, voltage levels from the PPG as well as biasing voltage levels set at the modulator.

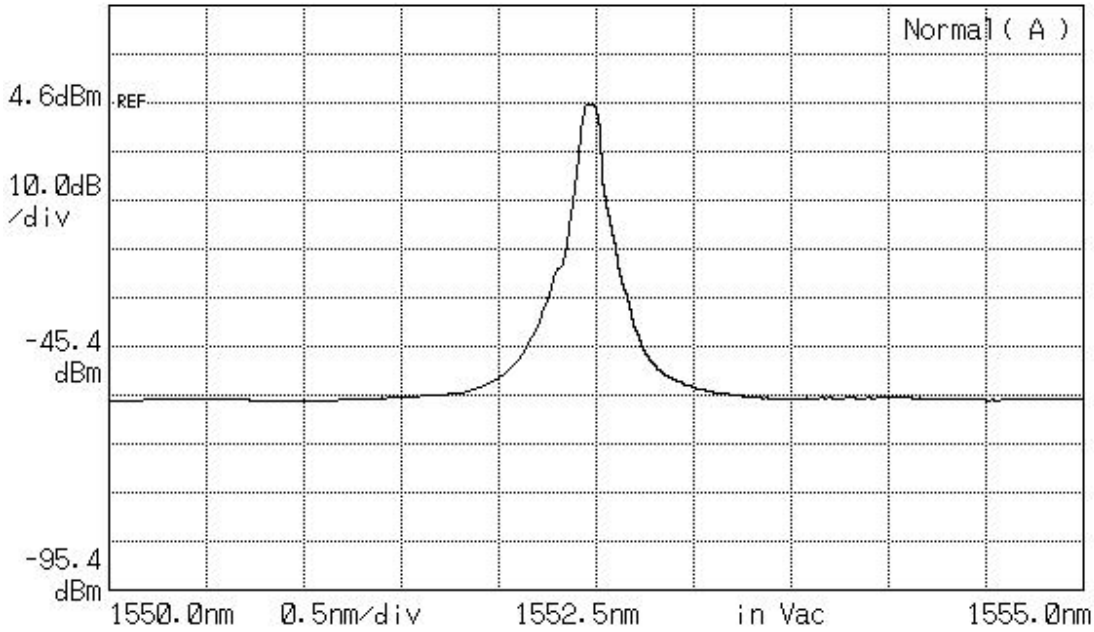


Figure 4.5

The spectrum of the optical channel used in the experiments

The set-up for the packet generation as well as for the whole photonic packet switching experiment is shown in Figure 4.6. The optical input power entering the crosspoint switch needs to be in the order of 0 dBm to 5 dBm. Since some optical power still needs to be tapped off, the signal exiting the modulator needs to be amplified by about 15 dB-20 dB. An EDFA, EDFA_1, shown in Figure 4.6, is used for the amplification. A tunable band pass filter is placed directly after the EDFA to filter out the spontaneous emission noise produced by the EDFA. The EDFA is set to provide a gain of 16 dB. The output optical power after the band pass filter is at 1 dBm. A 30:70 coupler is used to tap some power off to the electronic control. The 70% output is fed into the OXS and the 30% output goes to the electronic control. The tapped-off power loses 5.2 dB of power owing to the 30:70 coupler and arrives at the electronic control at about –4d Bm. A variable optical attenuator is then used to adjust the power level so that the PINFETs can recover the header signal correctly. The whole optical network is built with (9/125/250) single mode fibre. All the optical components have FC/APC connectors and are connected to one another with FC/APC-FC/APC adaptors.

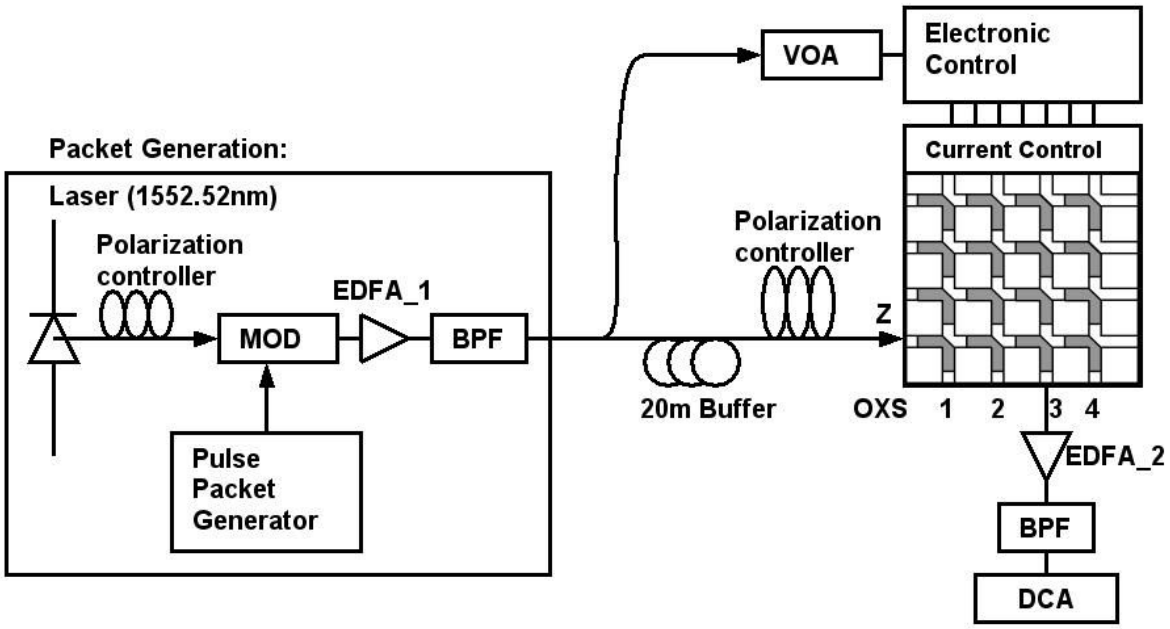


Figure 4.6

The set-up for photonic packet switching experiments [46]. MOD: Modulator, EDFA: Erbium Doped Fibre Amplifier, BPF: Band Pass Filter, VOA: Variable Optical Attenuator, OXS: Optical Crosspoint Switch, DCA: Digital Communications Analyzer.

Before the optical signal enters the OXS it passes through another polarization controller to adjust the polarization for minimum signal loss as it travels through the OXS. Because of the time taken for the header processing and correct switch cell to open, the packet will arrive at the OXS too early. Figure 4.7 shows the output signal as a result of this. The packet is already at the switch cell when the switch cell starts to open and does not switch the first part of the packet to the output. The packet used is similar to the one in Figure 4.2.

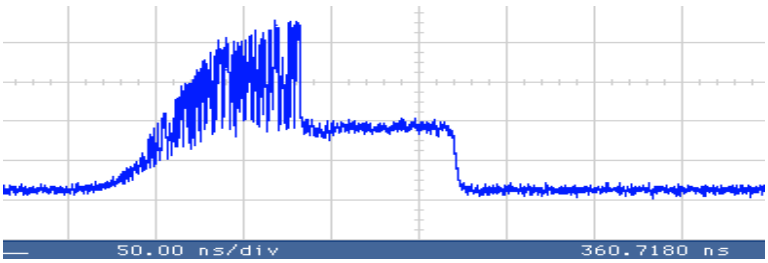


Figure 4.7

The packet at the output of the OXS when no input buffer is used

The header part (beginning of the packet) cannot be seen at the output. To solve this problem, an input buffer is needed to store the packets before going into the OXS. The buffer is built from a length of fibre. This buffer then stores the packet optically for a fixed length of time while the header processing is being done and the switch cell being switched open fully.

4.6 Input buffer length calculation

The length of the buffer will be dependent on the header processing time, therefore the length of the header and the time it will take to send a control signal to the switch cell to switch it open. It is also dependent on the rise time (75 ns) of opening the switch cell, since the packet must only arrive at the switch cell when it is fully opened. The header processing takes six clock cycles or 6×6.4 = 38.4 ns. Therefore the total time of delay required is about 114 ns (75 ns + 38.4 ns). The speed of light in silica fibre is about 2 x 10^8 m/s [1]. This corresponds to 5 ns for 1 m of fibre. To realize a 114 ns delay, 22.8 m of fibre is required. This 22.8 m buffer was built using a 20 m length of fibre and 3 m length of polarization controller and was measured (verified) using the DCA (Digital Communications Analyzer). The results are shown in Figure 4.8. Figure 4.8 (a) shows a packet measured just before entering the buffer and Figure 4.8 (b) show the same packet, with the DCA set to trigger at the same time, after the polarization controller. The time scale is set on 20 ns/div and from the DCA the delay is measured as 117 ns.

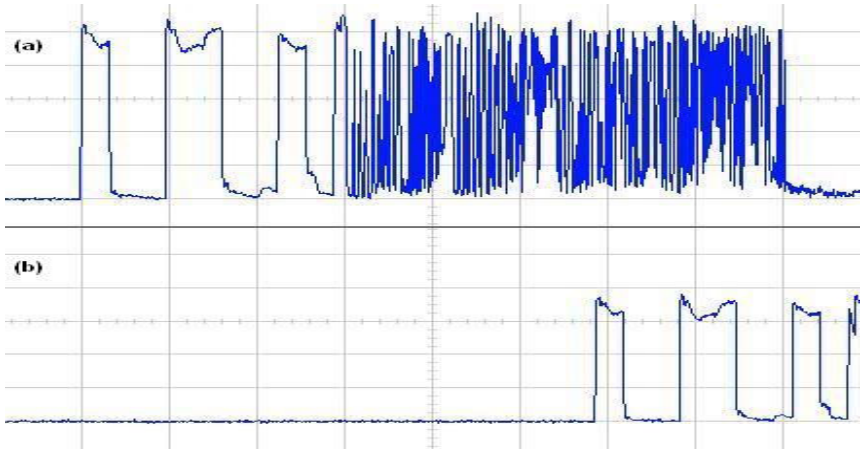


Figure 4.8

Measuring the length of the input buffer [20ns/div]. The packet at (a) is the input to the buffer and (b) the output of the buffer. The time delay is 117 ns.

4.7 The band pass filter

The packet loses about 25 dB, depending on the specific switch cell used, of optical power when being switched by the OXS. Therefore the output power when exiting the OXS is in the range of –25 dBm to –30 dBm. To measure the quality of the output signal, in the form of an eye diagram, the output is amplified again by using a second EDFA, EDFA_2, and passed through another tunable band pass filter. The importance of the band pass filter can be seen in Figure 4.9. When using no band pass filter, the output packet has a lot of noise, unwanted frequency components. This noise arises from the ASE process in the EDFAs and the ASE process from the active layer in the OXS. Figure 4.9 (a) shows a packet at the output of the OXS when no filters have been used. The noise causes the signal's top to be uneven. Ideally one wants a flat-topped signal, meaning the optical power levels for a one bit is the same everywhere along the packet. Figure 4.9 (b) displays the output when band pass filters have been placed after the EDFAs. The flat top is clearly visible.

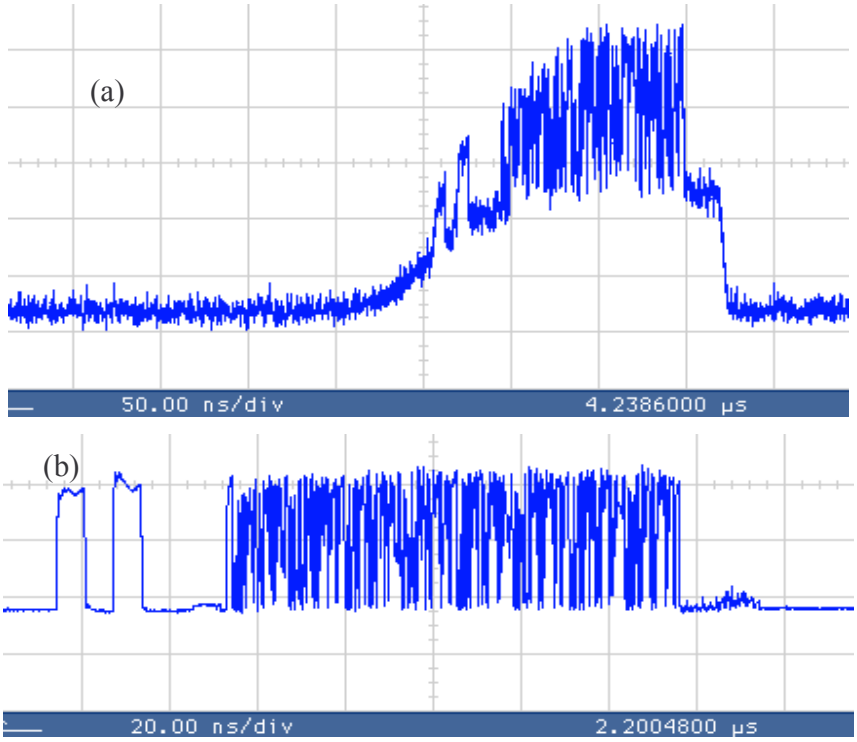


Figure 4.9

The output packets with (a) No band pass filter and (b) a band pass filter

Hewlett Packard's "83480A DCA" was used to display the output waveforms. This will confirm the correct operation of the experiment as well as measure the quality of the packets.

4.8 The experimental set-up for the contention resolution experiment.

A problem in photonic packet switching networks is contention resolution. To demonstrate that the new electronic control can resolve contention, a possible contention scenario has been created. There are two ways to create a contention scenario where two packets arrive at the OXS at the same time on different input ports, both destined for the same output port. Firstly, one can use two different channels on the PPG. Each channel generates packets destined for output 1 and sends them out at the same time. Both of them are modulated, with separate modulators, unto the same wavelength. Both are then also amplified, filtered and some power is tapped off for processing. Separate amplifiers, filters and taps are needed but should create the same time delay and ensure that the packets arrive at the OXS at exactly the same time. If one fibre has more delay, the two packets will not arrive at the electronic control at the same time, causing asynchronous behaviour.

The second way is to use only one channel from the pulse packet generator. The same packet-generating process as in Figure 4.6 can be used. This packet is then split with a 50:50 coupler, creating two identical packets on two fibres. Optical power is tapped off from both of them for the headers to be processed. This process requires fewer components and offers a higher guarantee that the packets will arrive at the OXS and electronic control at exactly the same time. Figure 4.10 shows the schematic diagram of this set-up. Once again, since 4-bit headers are used, the inputs need to be buffered for 114 ns before they can enter the OXS to be switched. Two 22.8 m buffers are used, one for each input to the crosspoint. Variable optical attenuators are also used just before the electronic control to adjust the optical power for header processing.

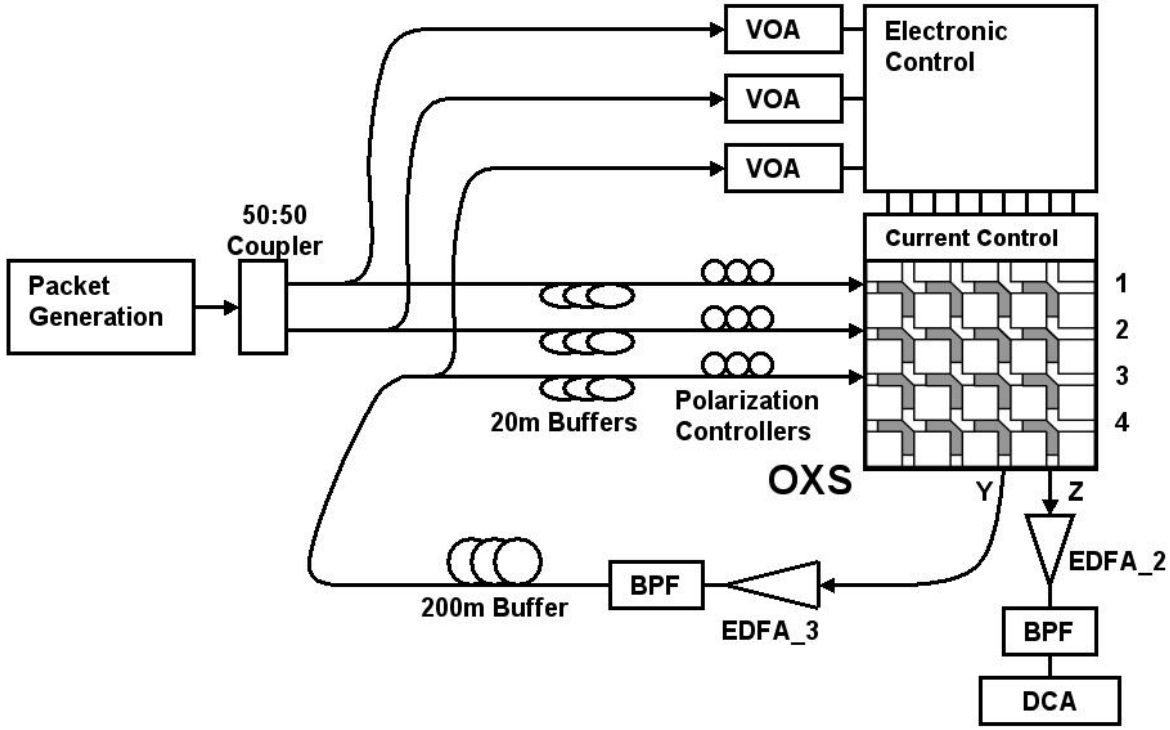


Figure 4.10

The experimental set-up of the contention resolution experiment [46]. MOD: Modulator, EDFA: Erbium Doped Fibre Amplifier, BPF: Band Pass Filter, VOA: Variable Optical Attenuator, OXS: Optical Crosspoint Switch, DCA: Digital Communications Analyzer.

Output Z is the desired output for packets from both input 1 and input 2. Output Y is used as a delay buffer. If contention occurs at the OXS, the packet from input 1, with higher priority, is normally switched to its desired output, Z, by activating switch cell Z1. Packets from input 2 are also destined for the same output but cannot be switched to output Z since the packets are at the same wavelength than packets from input 1 and will result in interference and loss of data if switched to output Z. Packets from input 2 are then switched to output Y and buffered for one timeslot. They are however amplified (EDFA_3) and filtered before passing through the 200 m delay buffer. This amplifier, filter and 200 m delay buffer cause a time delay equivalent to one timeslot, 1.107 μs. The buffered packets enter the OXS again via input port 3. Some optical power is again tapped off for the header to be processed and a 22.8 m input buffer stores the packets before entering the OXS. Packets are sent from the packet generator every second timeslot. Therefore in the first timeslot, two packets arrive at the OXS on inputs

1 and 2; in the second timeslot only one packet from input 3, the delay buffer input, enters the OXS. This packet is still destined for output Z and is switch there by activating switch cell Z3.

4.9 The delay buffer

The delay buffer is a 200 m roll of fibre. 200 m of fibre causes a 1 µs delay. This 1 µs delay was verified by measuring the packet at the input and output of the delay buffer with the DCA. Figure 4.11 (a) shows the packet at the input to the delay buffer and Figure 4.11 (b) shows the packet just after the delay buffer. The delay is verified as 1 µs.

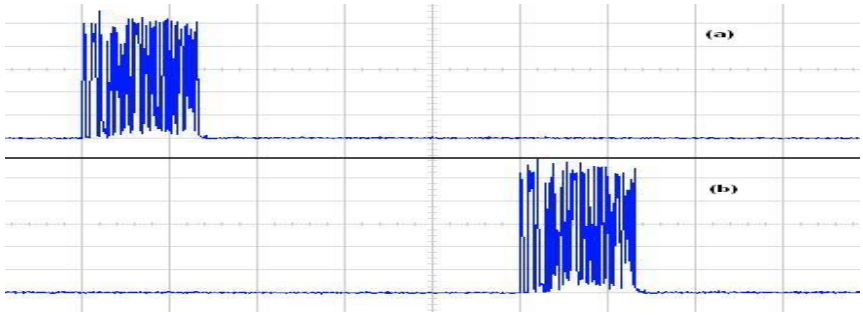


Figure 4.11

Measuring the delay for the 200 m optical buffer. The difference in time from the (a) input to the (b) output is measured as 1 µs. The scale is 200 ns/div.

4.10 The influence of crosstalk in the OXS

The OXS has crosstalk levels of less than –60 dB [4], [17]. This means that if one switches optical power from one input to one output, the power levels of this switched signal are 60 dB lower at the preceding output ports. The reason for these low crosstalk levels is the high absorption in the vertical active coupler when in the OFF state. A weak coupling (leakage) still exists, but is almost completely absorbed in the active layer. The crosstalk in the OXS presents a problem when a re-circulating buffer is used with the OXS. VPI transmission software was used to simulate the crosstalk effect and compare the effect of crosstalk when using one re-circulation with using 10 re-circulations. The crosstalk level is set to –30 dB as well as –60 dB and the results are clearly visible. The eye diagrams for the –30 dB simulation are shown in Figure 4.12 and the eye diagrams for the –60 dB crosstalk level are shown in Figure 4.13.

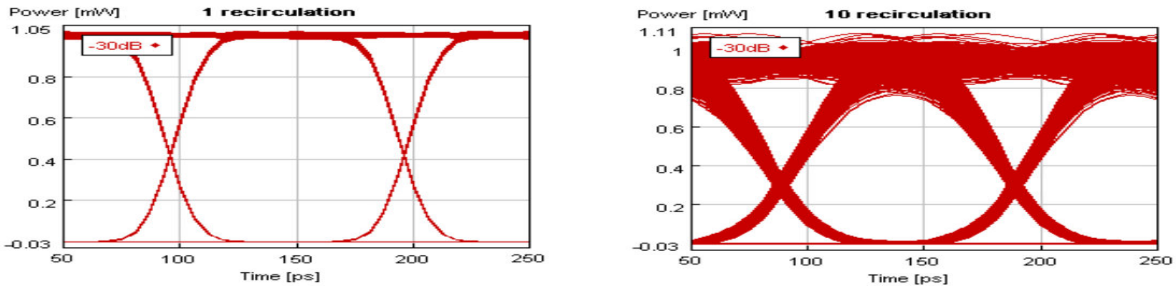


Figure 4.12

The difference in signal quality with increasing number of re-circulations for an OXS with crosstalk of –30dB can be seen here.

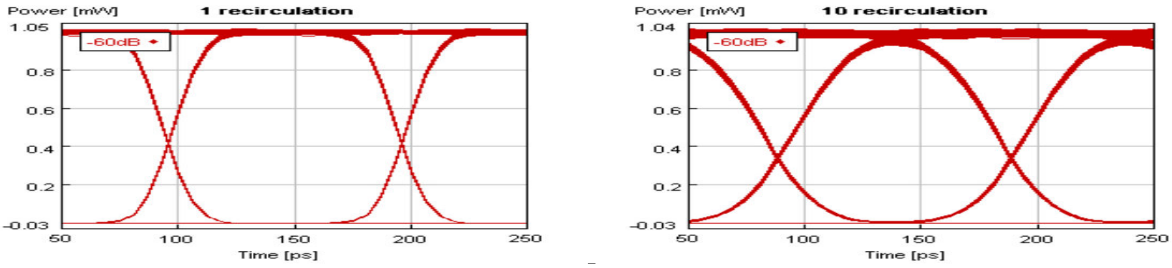


Figure 4.13

The difference in signal quality with increasing number of re-circulations for an OXS with crosstalk of –60dB can be seen here.

It is clearly visible that the output signal gets weaker if the number of re-circulations increases. For the higher crosstalk level of –30 dBs the weakening is much more intense and the BER is measured as $1e^{-55}$ with the received power at –10 dBm. After ten re-circulations, with the crosstalk level on –60 dBs, the output is still very good and the BER is measured as $1e^{-90}$ with received power at –10 dBm. For these experiments the researcher will only use one re-circulation (when contention occurs) but will require more re-circulations when the traffic load increases and the crosstalk will only start critically influencing the results then. The signal-to-noise ratio due to crosstalk, of the OXS, is modelled with the mathematical formula from 4.1. The crosstalk of the switch is 10 *log(x)* measured in dB and the number of input/output ports is *N*.

$$\frac{1-(N-1)x}{(N-1)x} \qquad (4.1)$$

4.11 Synchronization with clock

The clock signal is sent to the electronic control board with an SMA cable. The header signal (1010) arrives at the electronic control from the optical fibre. These two signals should be synchronized so that the clock's rising edge corresponds to the centre of the bits in the header. To do this, the current situation needs to be analysed. This is for the experimental set-up from Figure 4.6. The clock signal was measured just before entering the CPLD on the electronic control board and displayed in Figure 4.14 (b). The header signal, just before entering the CPLD, is also measured and displayed in Figure 4.14 (a). The clock rising edges are extended upwards to see how they correspond to the header. The rising edges do not fall in the middle of the header signal. The period of a bit in the header signal is 6.4 ns and the clock rising edges fall in the first nanosecond of this period. This is not desired because a fluctuation in the header signal due to temperature changes can cause these two signals to lose synchronization very easily.

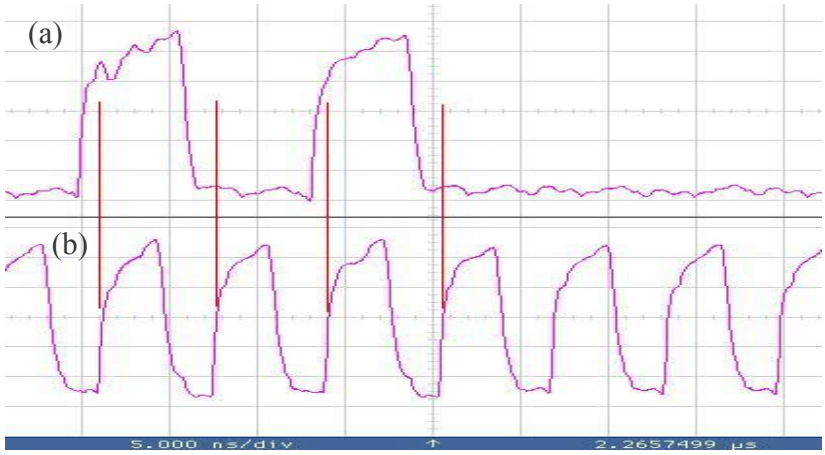


Figure 4.14

Synchronizing the (a) header signal with the (b) clock signal. The clock's rising edge is compared to the 1010 header signal.

A 2 m piece of fibre was inserted just after the band pass filter of the first amplifier. This resulted in the header signals arriving 10 ns later at the electronic control and the same measurements were taken. The results are shown in Figure 4.15. The rising edges of the clock signal, Figure 4.15 (b), are extended upwards and now fall almost in the middle of the period of the header bits. This will result in a more stable system because synchronization will not be

lost so easily. This 2 m of fibre is not needed for the contention resolution experiment depicted in Figure 4.10 because here a 50:50 coupler is used, which is 2 m and therefore the synchronization in that set-up is working well.

Figure 4.15

Synchronizing the (a) header signal with the (b) clock signal after adding 2 m of fibre. The clock's rising edge is compared to the 1010 header signal and shows better synchronization.

4.12 Discussion of experiments

With these two set-ups as in Figure 4.6 and 4.10, various experiments were done. The logic design for the CPLD was done first and simulated on the computer to verify correct operation before the experiment was done physically. In the first experiment a 4-bit header packet was used to demonstrate photonic packet switching from one input to three outputs of the OXS. The information in the header contains only the output port to which the packet needs to be switched. In the second part of the first experiment, a 4-bit header packet was used to switch eight variable length packets from one input to one output port of the OXS. This time the header has information about how long the corresponding packet is and the electronic control needs to process the header in order to determine for how long the switch cell should be opened.

In the second experiment, 8-bit header packets were used to demonstrate photonic packet switching of three variable length packets from one input to two outputs of the OXS. Because

of the 8-bit header, more information can be stored in the header and therefore higher flexibility is achieved. The experimental set-up as in Figure 4.6 was used for this experiment except that the input buffer was increased to 45.6 m for a 228 ns delay. This was done because the 8-bit header takes longer to be processed than the 4-bit header. Packets were sent synchronously and asynchronously to the OXS to demonstrate flexibility of the electronic control in handling both synchronous and asynchronous data once again.

In the third experiment, the problem of contention resolution in photonic packet switching networks was addressed. The OXS was subjected to a contention scenario, as in Figure 4.10. All the packets have a fixed length and a 4-bit header that has information about the desired output port of the packet. The last experiment uses 16-bit header packets to demonstrate the flexibility of the electronic control to handle such large headers. A basic one-to-one photonic packet switch was demonstrated with the header being "1010101010101010". The same set-up of Figure 4.6 was used for this last experiment except that longer input buffers were used. A summary of the four experiments is given in Table 4.1.

Experiment	**Header size**	**Inputs**	**Outputs**	**Packet length**	**Synchronous or asynchronous**
1A	4 bits	1	3	fixed	Synchronous
1B	4 bits	1	1	8 variable lengths	Synchronous
2	8 bits	1	2	3 variable lengths	Synchronous and asynchronous
3	4 bits	2	1	fixed	Synchronous
4	16 bits	1	1	fixed	Synchronous

Table 4.1

A summary of the four experiments.

In the next chapter these four experiments are carried out and the results are discussed. The logic design and simulated results for the CPLD are also given and discussed.

CHAPTER 5: EXPERIMENTAL RESULTS

5.1 Introduction

The aim of the four experiments is to demonstrate the flexibility of the new electronic control to realize photonic packet switching of fixed length packets, variable length packets, synchronous and asynchronous mode transfer of packets by controlling the OXS. The electronic control should also show potential to resolve contention that may occur at the OXS. The first step in implementing the experiments is to design the logic of the control CPLD, simulate it in software and if it is successful, program the CPLD chip with the code and get physical results. More detail about each experiment, for example header information, length of packets and logic design, will be given and discussed under each experiment.

The results are given in three forms. The first part is the simulation results. The ModelSim XE III 6.0d software was used to simulate the logic designs of the CPLDs. Only if the logic design's simulation proved to be running without error, was the CPLD programmed and the experiment conducted physically. In the physical experiments, the results include the packet stream before and after the OXS to prove successful switching. The quality of the output data is also noted in the form of an eye diagram. The Q-factor and BER are calculated. The output eye diagram is compared to the input eye diagram to see how the signal's quality was affected when being switched through the OXS.

5.2 The clock signal

Before each experiment was done, the clock's duty cycle was adjusted to 50%. It is very important for the clock to have a 50% duty cycle since the CPLD's program depends on the rising edge of the clock signal. Figure 5.1 shows the clock signal measured (with SMA cable) directly from the PPG. This clock was fed into the electro-optic control board to clock the Coolrunner II CPLD. A duty cycle of 50% was measured and the frequency was verified as 155.16 MHz. The clock signal also needs to be supplied to the current control circuitry. One of the electro-optic control board's SMA outputs was assigned with the clock signal and fed to the current control circuit of the OXS via an SMA cable. Figure 5.2 shows the clock signal at this SMA output, after passing through the Coolrunner II CPLD.

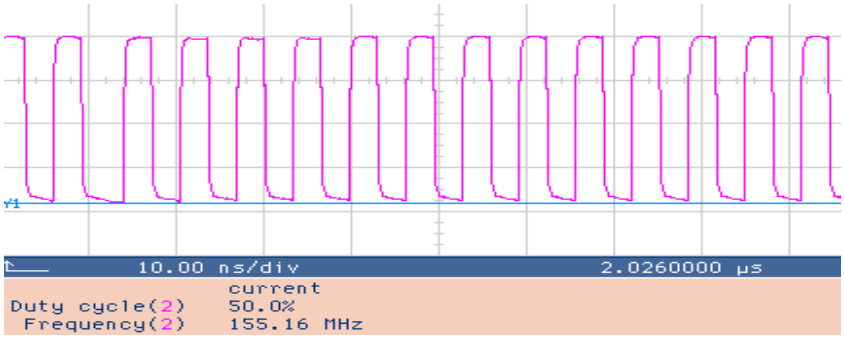


Figure 5.1

The clock signal measured with SMA cable directly from the PPG. This clock signal is fed into the Coolrunner II CPLD. A 50% duty cycle was measured and the frequency was 155.16 MHz.

Figure 5.2

The clock signal measured after passing through the Coolrunner II CPLD

The duty cycle of the output clock is 49.5%. This proves that the Coolrunner II CPLD has the ability to cope with this high speed of 155 MHz and should not show any problems processing the 155 Mbit/s header signals.

5.3 The PRBS payload

The payload that was used for the experiments was a 2^7-1 PRBS at 10 Gbit/s. Figure 5.3 and Figure 5.4 show this payload on a scale of 200 ps/div and 500 ps/div respectively. At 10 Gbit/s the period for one bit is 100 ps and therefore in Figure 5.3 one will find two bits per division. They are indicated on top of the diagram. In Figure 5.4 one will find five bits per division and this is also shown on top of the signal.

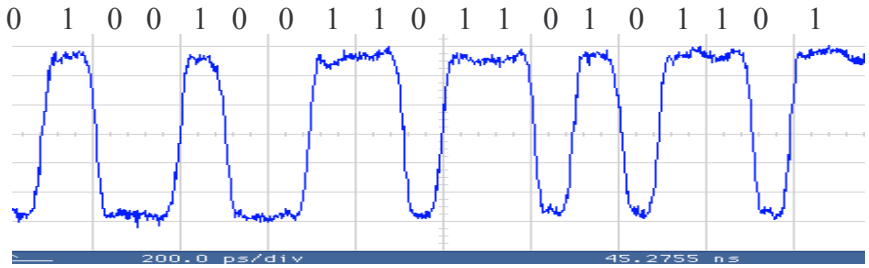


Figure 5.3

Part of the NRZ 10 Gbit/s payload at 200 ps/div is shown here. The bit sequence is shown on the top and corresponds to two bits per division.

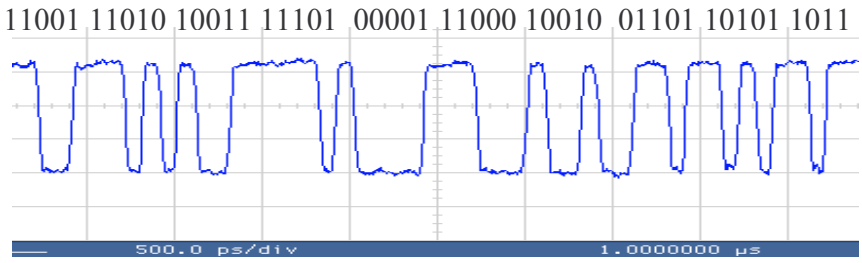


Figure 5.4

Part of the NRZ 10 Gbit/s payload at 500 ps/div is shown here. The bit sequence is shown on the top and corresponds to five bits per division.

This payload was measured directly after the modulator. The modulator needed to be set correctly to achieve this high-quality signal. The quality of the signal was measured by displaying the eye diagram on the DCA directly after the band-pass filter and EDFA_1, ensuring that the eye was widely opened with Q-factor exceeding 18. The eye diagram measurements were also taken at the input to the OXS and compared to the eye diagram at the output of the OXS to study the degradation in signal quality as the packet is switched by the OXS.

5.4 Measuring Q-factor and bit error rate

The performance of a digital communications system is measured by the probability of error per bit, which is referred to as the bit error rate (BER). If p_1 is the probability of mistaking '1'

for '0' and p_0 is the probability of mistaking '0' for '1' and if the two bits are equally likely to be transmitted, then BER = ½ p_1 + ½ p_0. The acceptable BER is 10^{-9} (one error every 10^9 bits) as given by [13]. The DCA has the capability to calculate Q-factors of 10 and higher. Since most of the experiments' Q-factor was lower than 10, the Q-factor had to be estimated. The formula for [13] was used to estimate the Q-factor and is given by 5.1.

$$Q = \frac{I_1 - I_0}{\sigma_0 + \sigma_1} \tag{5.1}$$

The Q-factor is also known as the SNR in units of voltage or current, since it is a measure of the difference between the mean current or voltage level for a '1' and '0' divided by the root mean square of the noise levels for a '1' and '0'. The Q-factor was estimated for all the eye diagram results and the BER was calculated by using the formula from [13] given in 5.2.

$$BER = \frac{1}{\sqrt{2\pi}Q}\exp\left(\frac{-Q^2}{2}\right) \tag{5.2}$$

The estimated BER values are calculated for each eye diagram and discussed in section 5.10.

5.5 Experiment 1A: Using 4-bit header packets for photonic packet switching from one input to three outputs

5.5.1 The logic design and simulation results

The aim with this first experiment is to realize 1-to-3 photonic packet switching. This was done by creating a stream of packets. Some of these packets will be destined for the first output, some of them will be destined for the second output and some will be destined for the third output and they are sent synchronously to one input of the OXS. The destined output port is encoded in the information in the header. A simple protocol was established to determine what the information in the header represents. The protocol for the first experiment is as described below. The header is a 4-bit sequence. The first, most significant bit is always a one, representing the beginning of the packet. The last bit or least significant bit is always zero. The information is only carried in the two bits in the middle of the header. If the header is 1010 the

packet is destined for output 1. If the header is 1100 the packet is destined for output 2 and if the header is 1110 the packet is destined for output 3.

To do this processing, Xilinx ISE 7.1i software was used to design the logic for the Coolrunner CPLD. Refer to Addendum B for the logic diagrams. The top schematic design is given in Figure B.1. The three inputs are the clock (external 155MHz), the reset and the input packet stream. The packets enter the first component, “Prosesseer” serially. The schematic diagram of this “Prosesseer” component is given in Figure B.2. The first component here is the shift register, SR4CE. The four bits of the header are serially shifted to the output of the shift register, Q0, Q1, Q2 and Q3. If Q3 becomes high, which means the full header should be on the output, input CE becomes low. If CE becomes low the current information on the outputs is kept on these outputs until the SR4CE components are reset. This also causes the output “pakkie” to become low. If “pakkie” becomes low the state machine is activated. The state machine is shown in Figure B.3. The state machine, when reset, waits in state “WAG” until “pakkie” becomes low. When “pakkie” becomes low, the counter, “teller”, is activated, as well as the switching window “skakelVenster”. The output, “skakelVenster” enables the output ports of the Coolrunner II CPLD. The counter component can be seen in Figure B.1. It counts up to 31 before the state machine goes back to the “WAG” state to wait for the next packet. When the counter has finished counting, “iHerstel” is activated, which is the internal reset that resets the shift register, SR4CE.

The counter is set to count 31 times because at a clock speed of 155 MHz this represents a time of 198.4 ns, which is the time needed to active the switch cell to switch the packets. During this time the logic of the “Prosesseer” component processes the header and activates output “een”, “twee” or “drie”, depending on the information in the header. They correspond to output 1, 2 and 3 respectively. These outputs are however only activated if the switching window signal, “skakelVenster” is also high. These outputs are connected to the current control of the OXS.

This logic design was simulated with the following input: 1010, 1100, 1110, 1000, 1010, 1100, 1110, 1110, 1100, 1010. These 4-bit headers were sent every 1 µs and can be seen in Figure 5.5 as signal: “/toetsbank/z”. Figure 5.5 also displays the clock signal at the top and the three output signals for output 1, output 2 and output 3.

To see the specific header signals more clearly a zoomed-in picture of the first three headers is shown in Figure 5.6(a) –(c). In Figure 5.6(a) the input is the header 1010 that corresponds to output 1. From the results it is clear that only output 1 (/toetsbank/een) is activated. This output is connected to switch cell Z1 (output 1). Switch cell Z1 is only opened when this signal becomes low. In Figure 5.6(b) the input is the header signal 1100 that corresponds to output 2 or switch cell Z2. From the results only output 2 (/toetsbank/twee) is activated. Figure 5.6(c) shows the result when the input is 1110, corresponding to output 3 and only output "toetsbank/drie" (output 3) is activated. These results prove that the logic design is working perfectly. From Figure 5.5 one can also see what happens when a different signal than that from the header is sent to the logic, for example at 3 µs, signal 1000 is sent but nothing happens.

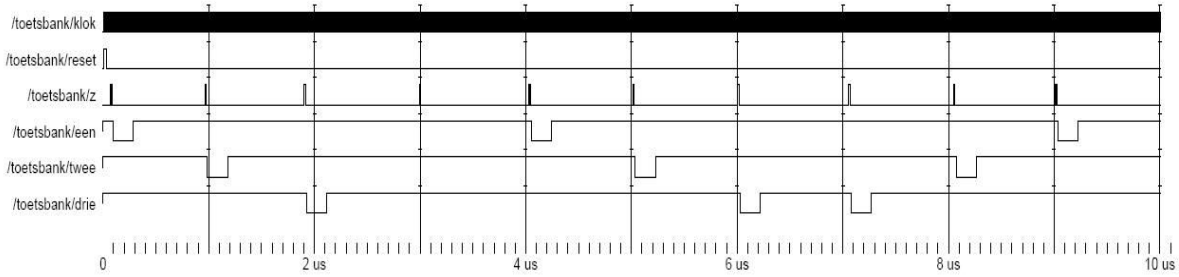
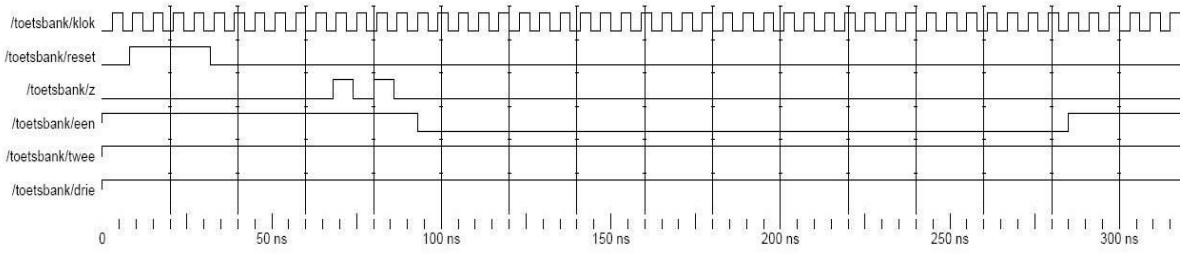


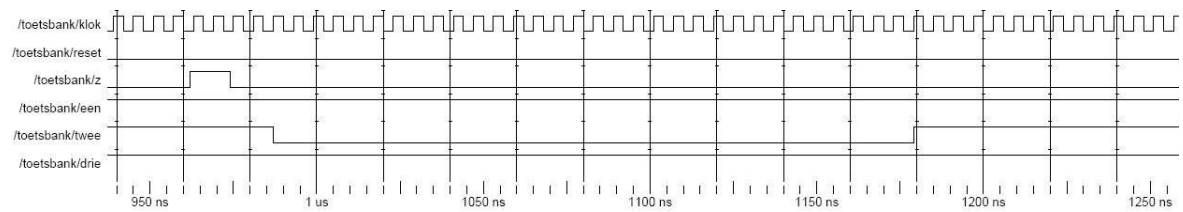
Figure 5.5

The simulation results of the logic diagram from Figure B.1, for experiment 1A. Signal "/toetsbank/z" is the input, "/toetsbank/een" is output 1, "/toetsbank/twee" is output 2 and "/toetsbank/drie" is output 3.

(a)



(b)



(c)

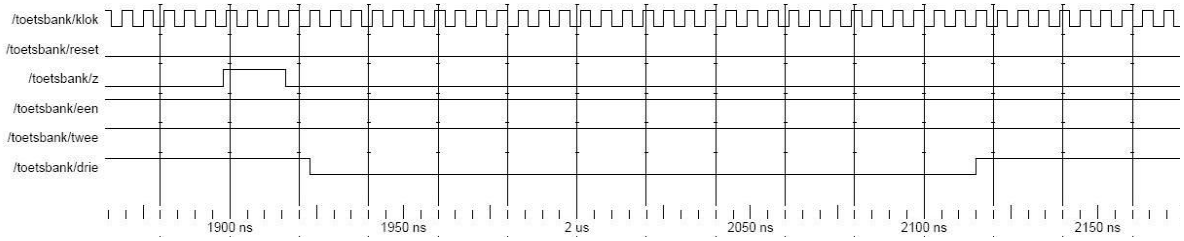


Figure 5.6

The simulation results for (a) the 1010 header, (b) the 1100 header and (c) the 1110 header. One can clearly see that if a 1010 header is received, only output 1 is activated, if a 1100 header is received, only output 2 is activated and if header 1110 is received only output 3 is activated.

5.5.2 The experimental results

With the logic design's simulations proven to be successful, the Coolrunner II CPLD was programmed with this logic design (Figure B.1) and the experiment carried out physically. The PPG was programmed to generate these 4-bit header signals with a payload of 140 ns. The generated packets in the optical domain as well as electronic domain can be seen in Figure 5.7.

Figure 5.7(a) shows the packet with header 1010 in the optical domain and Figure 5.7(d) shows the same packet in the electronic domain just before the CPLD. Figures 5.7(b) and (e) show the 1100 header packet in the optical and electronic domain respectively and Figures 5.7(c) and (f) show the 1110 header packet in the optical and electronic domain respectively. Notice the payload is just noise in the electronic domain.

Four separate tests were done. Firstly only packets destined for output 1 were sent to the OXS, secondly only packets destined for output 2 were sent to the OXS, thirdly only packets destined for output 3 were sent to the OXS and lastly packets destined for output 1, 2 and 3 were sent to the OXS.

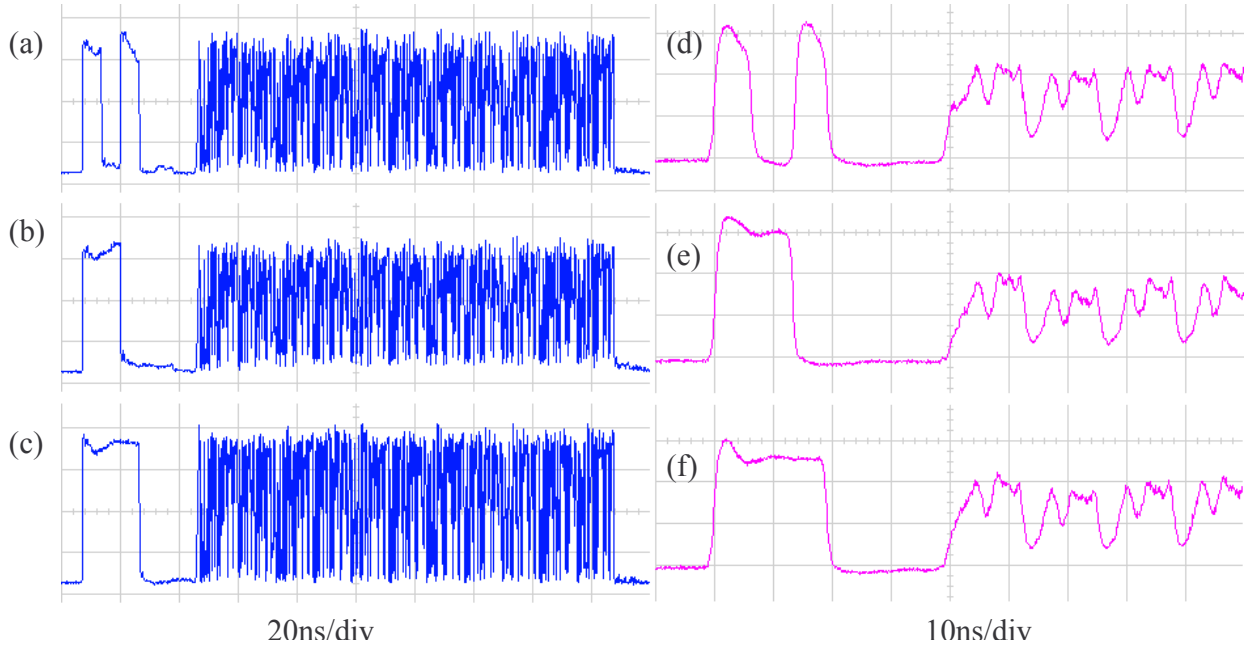


Figure 5.7

The packets used for experiment 1A. In (a) to (c) the packets with headers 1010, 1100 and 1110 are shown respectively in the optical domain while in (d) to (f) the same packets are shown in the electronic domain. The packets have a fixed payload length of 140 ns.

The eye diagram of the input packet stream just before entering the OXS is shown in Figure 5.8. The DCA measured a Q-factor of 10.10 and this value was verified by equation 5.1 as 10. From equation 5.2 the BER is 2.79×10^{-24}.

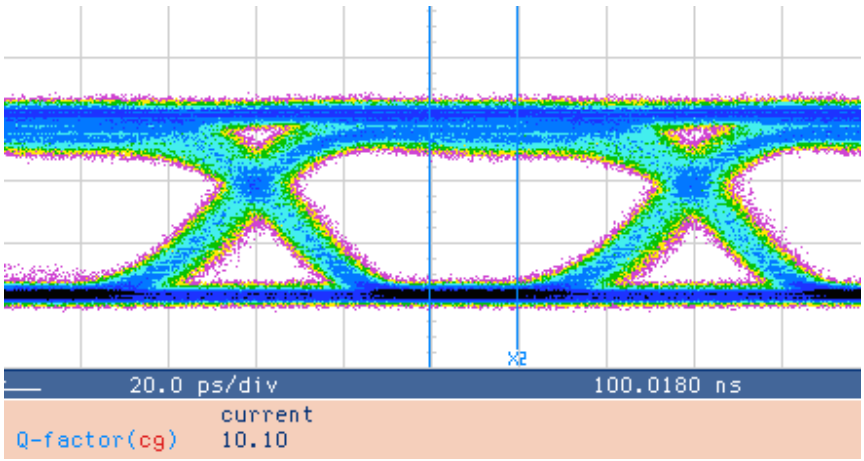


Figure 5.8

The eye diagram measured before entering the OXS. It has a Q-factor of 10.10.

For the first test, only packets with headers 1010 were sent to the OXS. The packets were sent every 1.107 µs resulting in a synchronous stream of packets. The switched output stream can be seen in Figure 5.9(b). The electronic control signal sent to switch cell Z1 is also shown in Figure 5.9(a) to verify that the Coolrunner detected the header and did the processing correctly. The output eye diagram was measured and is shown in Figure 5.9(c). The input optical power entering the OXS is 1.3 dBm. The eye diagram was measured at an average optical power of –7.6 dBm and shown in Figure 5.9(c). The Q-factor was estimated (from equation 5.1) to be 6.9118 and the BER was calculated from the Q-factor using equation 5.2 as 2.44×10^{-12}.

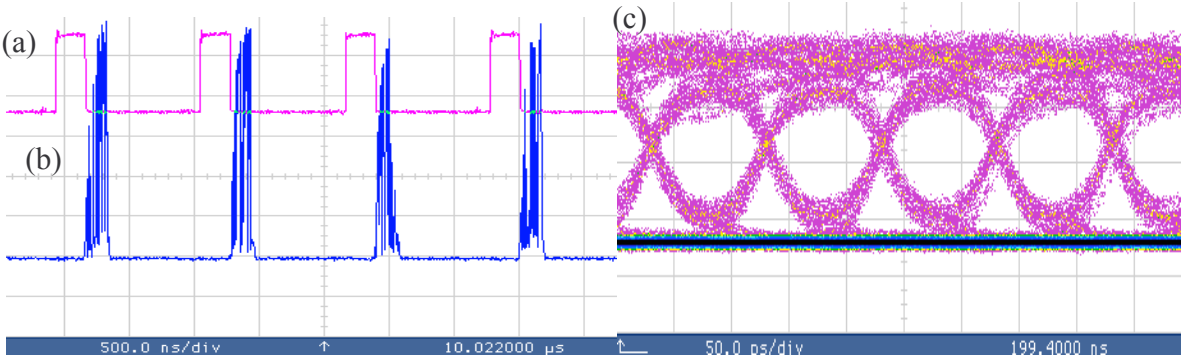


Figure 5.9

In (a) the electronic control signal sent to switch cell Z1 was measured, in (b) the optical power from output 1 was measured and the eye diagram is given in (c).

The packet stream being generated from the PPG was then changed to only packets with 1100 headers representing packets destined for output 2 only. These packets were also sent every 1.107 µs. No optical power was measured at outputs 1 and 3. The optical power measured at output 2 is displayed in Figure 5.10 (b). It verifies that switching was done correctly. Figure 5.10(a) shows the electronic control signal sent to switch cell Z2. The eye diagram of the output packets is displayed in Figure 5.10(c). This eye diagram was measured at an average optical power of -8.1dBm. The Q-factor was estimated (from equation 5.1) as 6.765 and the BER calculated (from equation 5.2) as 6.81947×10^{-12}.

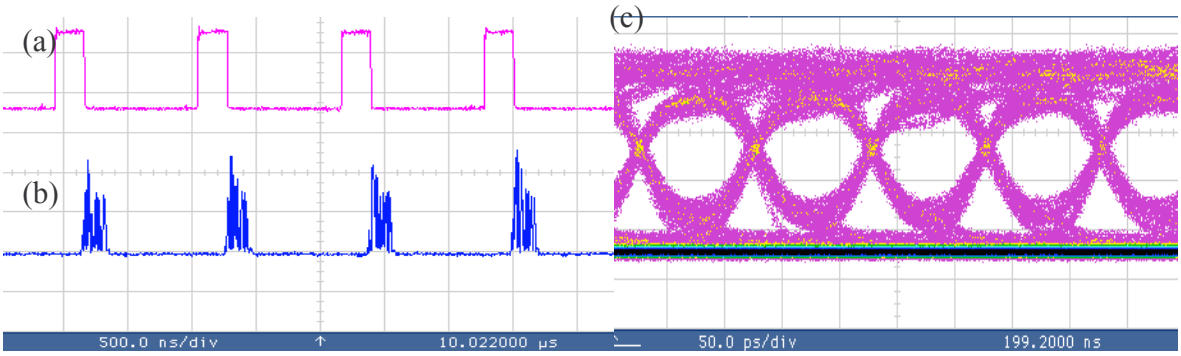


Figure 5.10

In (a) the electronic control signal sent to switch cell Z2 was measured, in (b) the optical power from output 2 was measured and the eye diagram is given in (c).

The packet stream is now changed into packets destined only for output 3. They have headers 1110. These packets are also sent every 1.107 µs. The electronic signal sent to switch cell Z3 is measured and displayed in Figure 5.11(a). The optical power from output 3 is measured, Figure 5.11(b), and the eye diagram is displayed in Figure 5.11(c). This confirms that the experiment was successful since all the packets destined for output 3 were present at output 3. This eye diagram was taken at an average optical power level of –8.7dBm. The Q-factor was estimated from equation 5.1 as 6.3095 and the BER calculated (from equation 5.2) as 1.43327×10^{-10}.

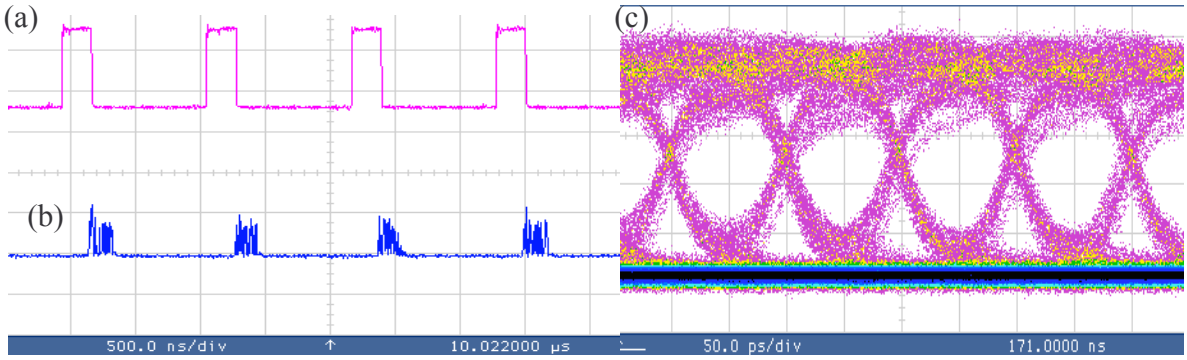


Figure 5.11

In (a) the electronic control signal sent to switch cell Z3 was measured, in (b) the optical power from output 3 was measured and the eye diagram is given in (c).

For the final test, packets were generated as follows: first packet destined for output 1, second packet destined for output 2 and third packet destined for output 3. The packets were sent every 1.107 µs and this sequence was repeated. Figure 5.12 shows the results. The switching

window for all three switch cells, Z1, Z2 and Z3, was measured and displayed in Figure 5.12(a). This was done to confirm the presence of the other packets on the input. The optical power at output 2 (from switch cell Z2) was measured and displayed in Figure 5.12(b). This result confirms that photonic packet switching is working as planned. There is one packet present, then in the next two time slots no packets but there is a switching window. This means a packet was detected in that timeslot but was switched to either output 1 or output 3. The same type of measurement was obtained at output port 1 and 3, with packets only present every third timeslot. The eye diagram is displayed in Figure 5.12(c) with an estimated Q-factor of 6.7647 (from equation 5.1) and BER of 6.81947×10^{-12} (calculated from equation 5.2). This BER value is similar to the BER value of the eye diagram from Figure 5.10(c) that also represented switch cell Z2, confirming that the BER is dependent on the switching quality of the corresponding switch cell.

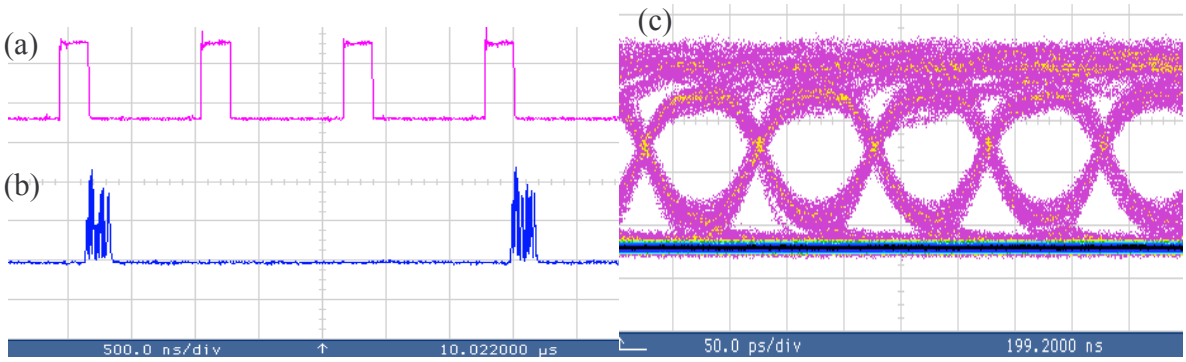


Figure 5.12.

The output measurement when input packets are destined for output 1, output 2, output 3 and repeated in this sequence. In (a) the switching window for switch cells Z1, Z2 and Z3 is measured, in (b) the optical power from output 2 is measured and the eye diagram is given in (c).

All four input sequences were switched correctly with good quality eye diagrams measured. The three outputs have different power levels due to different optical losses of the different switch cells. Switch cell Z1 has the least amount of optical power loss and has resulted in the highest optical power measurement. Switch cell Z3 has most optical power loss and the weakest optical power was measured from output 3. This is confirmed by Figure 4.1, where the switch cell's optical power losses were measured. Switch cell Z3 has most optical loss followed by switch cell Z2 and switch cell Z1 has least optical power loss.

5.6 Experiment 1B: Using 4-bit header packets for eight variable length photonic packets switching from one input to one output

5.6.1 The logic design and simulation results

In this experiment only one switch cell is used. The Coolrunner II CPLD is reprogrammed with the schematic diagram from Figure B.4. Eight variable length packets are generated with their lengths encoded in their 4-bit header. They are sent into the OXS at input 1 and are all destined for output 1. The most significant bit is always a one, indicating the start of a packet. The next three bits have information about the length of the payload. A summary of the header address, payload length, switching window length required and the number of counts the counter has to count to realize the switching length is given in Table 5.1. Note that the switching window is set in such a way as to switch only the payload. The whole packet can be switched by increasing the count of the counter, thus increasing the switching window and allowing the whole packet to be switched.

Header:	Payload length:	Switching length:	Counter count for:
1000	32 ns	64 ns	10 counts
1001	64 ns	96 ns	15 counts
1010	96 ns	128 s	20 counts
1011	128 ns	160 ns	25 counts
1100	160 ns	192 ns	30 counts
1101	192 ns	224 ns	35 counts
1110	224 ns	256 ns	40 counts
1111	256 ns	288 ns	45 counts

Table 5.1

The eight 4-bit headers with the payload length they represent are shown here. The switching window length required as well as the number of counts that the counter must count to realize this switching length is also given.

The aim of the electro-optic control is now to process these headers and determine how long the switch cell needs to be opened to switch the packet. Figure B.4 shows the top schematic diagram of the logic design. Packets enter via port “inlaat”. The other inputs are the clock and main reset. The inside of component “processing” is shown in Figure B.5. It also has the SR4CE shift register component to shift the header input to the output ports, Q0, Q1, Q2 and Q3. If the packet is fully shifted into the shift register so that the header bits appear on the

output, the CE input becomes low because of the NOT gate from Q3. The first bit of the header is one, therefore if the header is fully read into the shift register, Q3 will be high. The header is now fixed on the output of the shift register. Output "pakkie" becomes high and triggers the state machine.

The state machine is shown in Figure B.6. The state machine, "masjien", waits in STATE2 until "pakkie" becomes high, then goes into STATE0 were the counter is started. The logic of the "processing" component processes the header's bits, currently on the output of the shift register and makes one of the eight outputs, nrr1, nrr2, nrr3, nrr4, nrr5, nrr6, nrr7 or nrr8, high. This output corresponds to one of the eight packets with its specific length. The state machine has these outputs from the "processing" component as inputs and depending on which one is high, goes into one of the eight blue states (from Figure B.6) and waits for the counter to finish counting. Only one of the eight inputs can be high at a time, therefore no multiple highs will be experienced. These eight blue states (in Figure B.6) will each respond at a different value from the counter. This value to which it responds determines the length of time the switching window is opened because while in these blue states, the switching window is opened.

If the counter reaches the corresponding value, the state machine moves to the next state. Here the counter and shift register are reset with signal "iRESET", the switching window is closed and the state machine moves into the waiting state to wait for the next packet. The output of the whole logic design is just the switching window signal that is connected to the correct switch cell for the packets to be switched. This switching window signal will switch the switch cell open for the correct length of time to switch the payload of the packet.

The logic design was simulated with ModelSim XE III 6.0d and the results are shown in Figure 5.13. The input stream is all the possible header signals from the shortest one up to the packet with the longest length. These header signals are sent every 1 µs and the whole sequence repeats itself. It is clearly visible from the results that the switching window signal, "/t/sw/" in Figure 5.13, is opened for a different length of time for each header. This time corresponds to the length of the payload that needs to be switched.

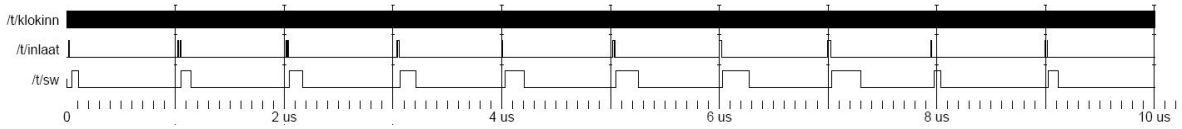


Figure 5.13

The ModelSim results for the logic design of Figure B.4. The input stream, "/t/inlaat" is the 4-bit header signals from Table 5.1. The output is the switching window, "/t/sw", which corresponds to the length of the payload for that specific header.

5.6.2 The experimental results

The PPG was programmed to generate these eight packets with the 4-bit headers and specific length of payload corresponding to the header according to Table 5.1. Figure 5.14 shows these eight different packets separately in the optical domain (blue).

The pink signals opposite the blue ones are measured just before entering the Coolrunner II CPLD to verify how the electronic control detects these packets correctly. Each packet is sent out every 1 µs. The sequence of packets is sent so that the shortest one is sent out first and the longest one is sent out last. This sequence repeats itself. It is clearly visible that only the header is being detected by the PINFETs and that for all eight signals, the payload is not detected at all.

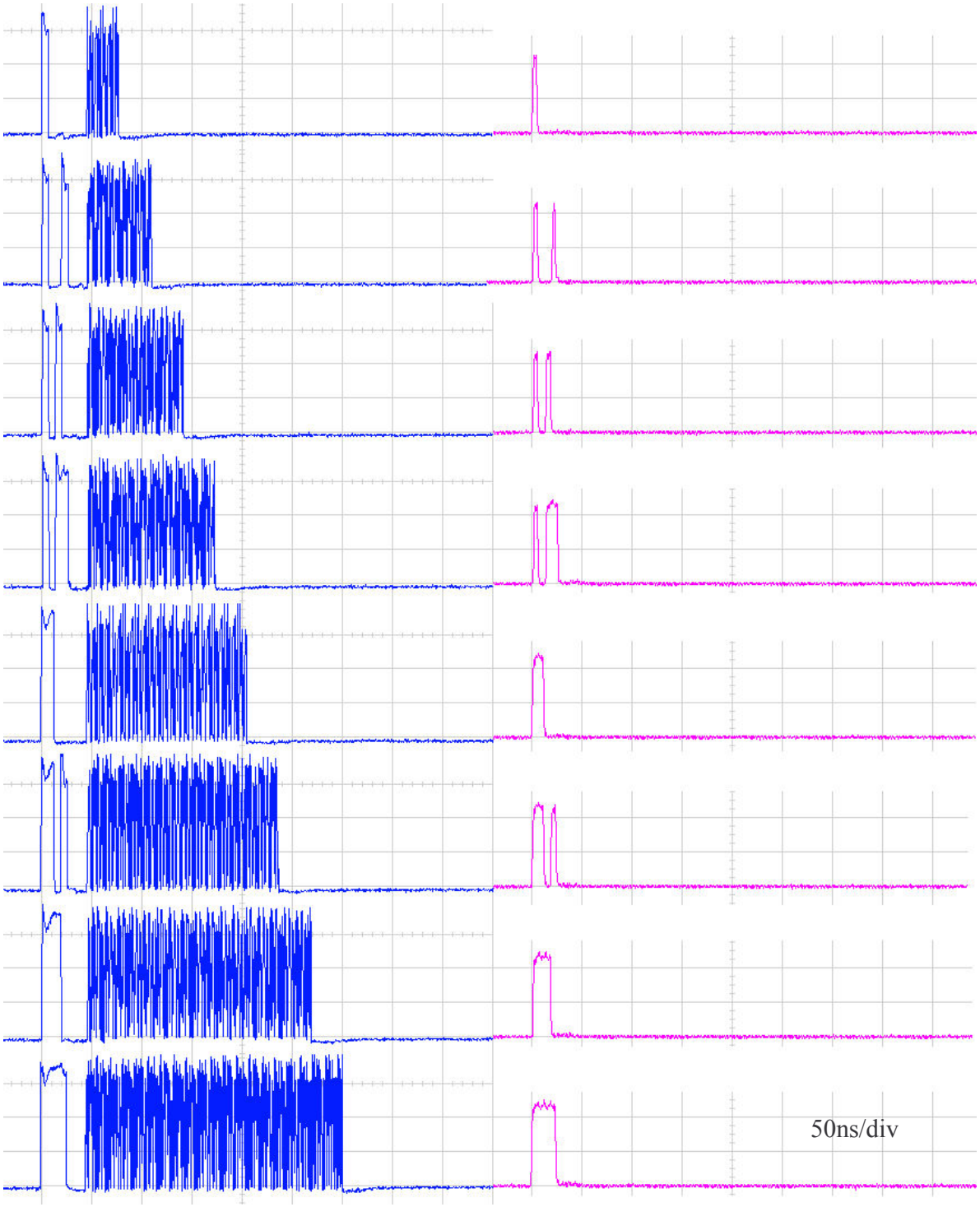


Figure 5.14

The eight input packets used for experiment 1B. The packets in the optical domain are shown on the left-hand side (blue) and the electronic measurement of these signals, just before entering the CPLD is, is shown on the right-hand side in pink.

The Coolrunner II CPLD was programmed with the logic design of Figure B.4 and the experimental set-up of Figure 4.6 was used. To verify that the experiment was a success, the input stream was measured, the output from output port 1 and the electronic control signal sent to control the switch cell. The results are shown in Figure 5.15. The headers were successfully processed by the CPLD. This can be seen in the length that the switching window is open, Figure 5.15(a), that corresponds to the length of the payload, Figure 5.15(b). The output sequence, Figure 5.15(c), is the same as the input sequence and therefore the switching was successful.

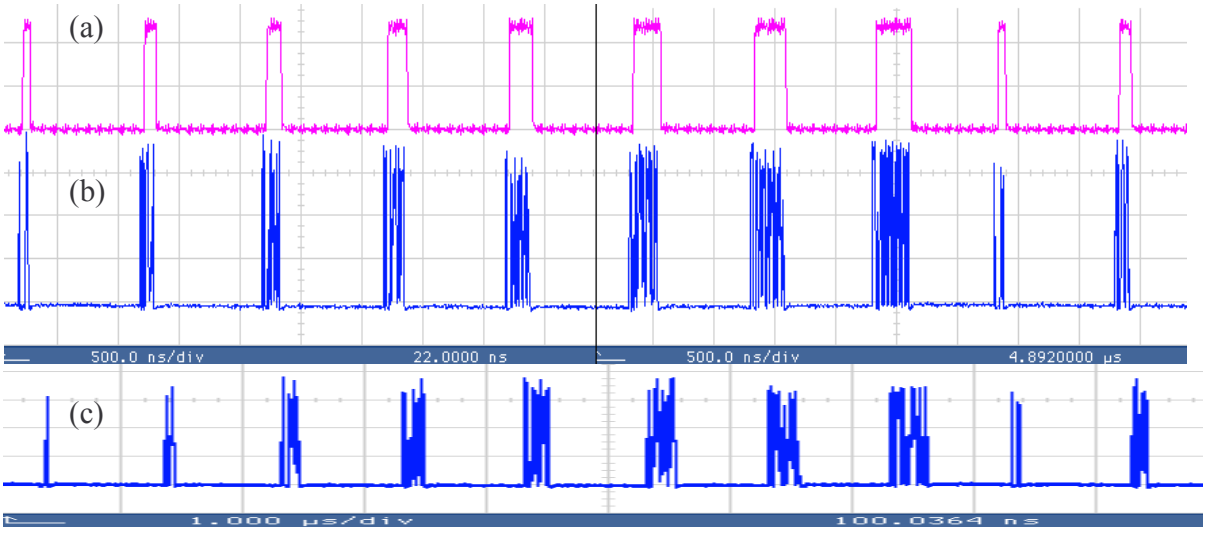


Figure 5.15

The results for experiment 1B. The length that the switching window (a) is opened corresponds to the length of the packets received (b). The output from the OXS is seen in (c) and corresponds to the input sequence.

To determine the quality of the switched packets, the eye diagram of the output packet sequence, Figure 5.16, was measured and compared to the input eye diagram from Figure 5.8. The Q-factor is estimated to be 7.75 from equation 5.1 and the BER is calculated (from equation 5.2) as 4.66877×10^{-15} . The output eye diagram was measured at an average optical power level of –6.3 dBm.

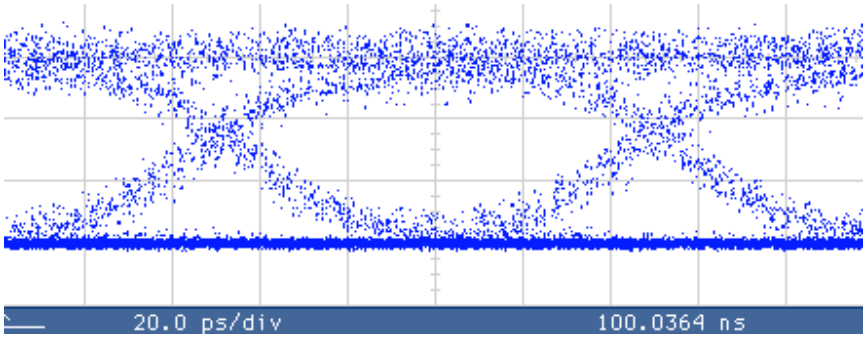


Figure 5.16

The output eye diagram for experiment 1B.

5.7 Experiment 2: Using an 8-bit header packet for photonic packet switching of three variable length packets from one input to two outputs.

5.7.1 The logic design and simulation results

The next experiment combines the aims of the previous two experiments and therefore requires more information in the header. The aim is now to send three variable length packets from one input to either one of two outputs. The three lengths of the payloads are 100 ns, 200 ns and 300 ns. The header encodes this information in 8-bits as described below. The first four most significant bits are used for the output port information. The next four bits, the least significant bits in the header, are used for information about the length of the payload. Table 5.2 summarizes the header bits with the output port and length classification.

Header:	Output port:	Length of payload:
10011001	One	100 ns
10011010	One	200 ns
10011100	One	300 ns
10101001	Two	100 ns
10101010	Two	200 ns
10101100	Two	300 ns

Table 5.2

A summary of the header of the packets used in experiment 2 with the information encoded in them

From Table 5.2, bits one and five are always one. If bit four is a one the packet is destined for output 1 and if bit three is a one the packet is destined for output port 2. The payload is 100 ns if bit eight is one, 200 ns if bit seven is one and 300 ns if bit six is one.

The logic design to do the processing of these 8-bit headers is shown in Figure B.7. There are three inputs, the clock, the reset and serial input stream. The first component, “agtbit”, is shown in Figure B.8. It uses an 8-bit shift register. An incoming header will be shifted to the eight output ports of this shift register. If the first bit of the header, which is always a one, reaches output Q7, the shift register is stopped and the whole header is present on the output, Q[0:7]. The logic then does the processing of the header signal and results in either O1 or O2 being high, corresponding to output 1 and output 2 respectively. Also one of outputs L100, L200 or L300 becomes high, which corresponds to the length of the payload. The sixth output is “pakkie”, which becomes low when a header has been received.

The state machine (“masjien”), Figure B.9, waits for this “pakkie” signal to become low and as soon as it becomes low, enables the counter, CB8CE. The state machine also has three inputs, L100, L200 and L300, which are the outputs of component “agtbit” and correspond to the length of the packets. The state machine then goes into one of three states depending on the configuration of these three input signals. Only one of them can be high, therefore only one state can be selected. In this state the signal “SW” becomes high and stays high for the duration of that state.

If L100 is high the state machine goes to state “PACKET_100 ns” and stays in this state until the counter reaches 47 counts corresponding to “SW”, the switching window, to be high for 300 ns. If L200 is high, the state machine goes to the “PACKET_200 ns” state and stays in this state until the counter reaches 63 counts corresponding to the switching window, SW, being high for 403 ns. If L300 is high the state machine goes to state “PACKET_300 ns” and stays in this state until the counter reaches 78 counts, corresponding to “SW”, the switching window, to be high for 500 ns. After the counter reaches one of these counts, the state machine goes into an internal reset state where the 8-bit shift register is cleared, the counter is cleared and the state machine goes back to the state where it waits for the next packet.

The switching window signal "ENSW" from "masjien" in Figure B.7 is then supplied as an input to two AND gates. The other input to these AND gates are the outputs O1 and O2 from the "agtbit" component. The output of these two AND gates is also the outputs of the CPLD and is called SW_1 and SW_2. SW_1 is connected to Z1 and will only be high if the input packet is destined for output one. It will also only be high for the length of time needed to switch the packet with a specific length. SW_2 is connected to Z2 and will only be high for the correct length of time required to switch the packet of specific length if the packet is destined for output two.

This logic design was simulated with ModelSim XE III 6.0d and the results are given in Figure 5.17. The input stream that was used (only header information) was as follows: 10011001--------1 µs--------10011010-------1 µs-------10011100-------1 µs-------10101001-------1 µs-------10101010-------1 µs-------10101100-------1 µs-------11111111------1 µs------10101010-------1 µs-------10011001-------1 µs-------10101100. The results were successful. The output, "/toets/switchingwindow1", became high only if there was a packet destined for output one and opened for the correct length of time. The second output, "/toets/switchingwindow2", also only became high if the packet was destined for output two and was opened for the correct length of time as well.

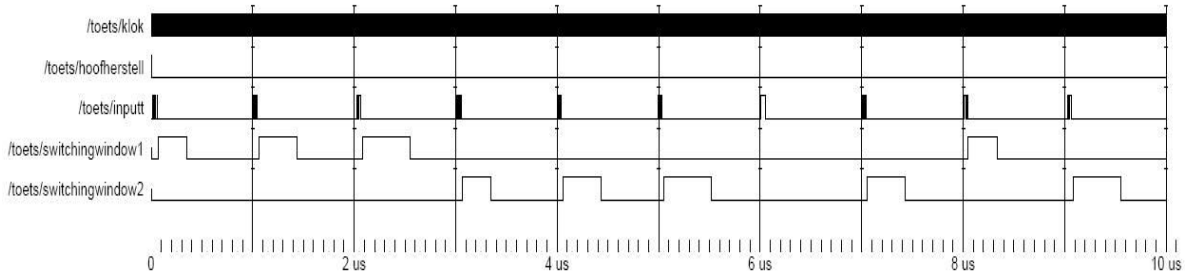


Figure 5.17

The results of simulating the logic design from Figure B.7 with different input signals. More detail about each input signal and the result it has on the two outputs are given in Figure 5.18.

More detail of the first six input signals is given in Figure 5.18(a)-(f). These figures show the header signal more clearly and show the effect on output 1 and output 2. The simulation was run with a clock speed of 166 MHz that represents a period of 6 ns (3 ns high, 3 ns low).

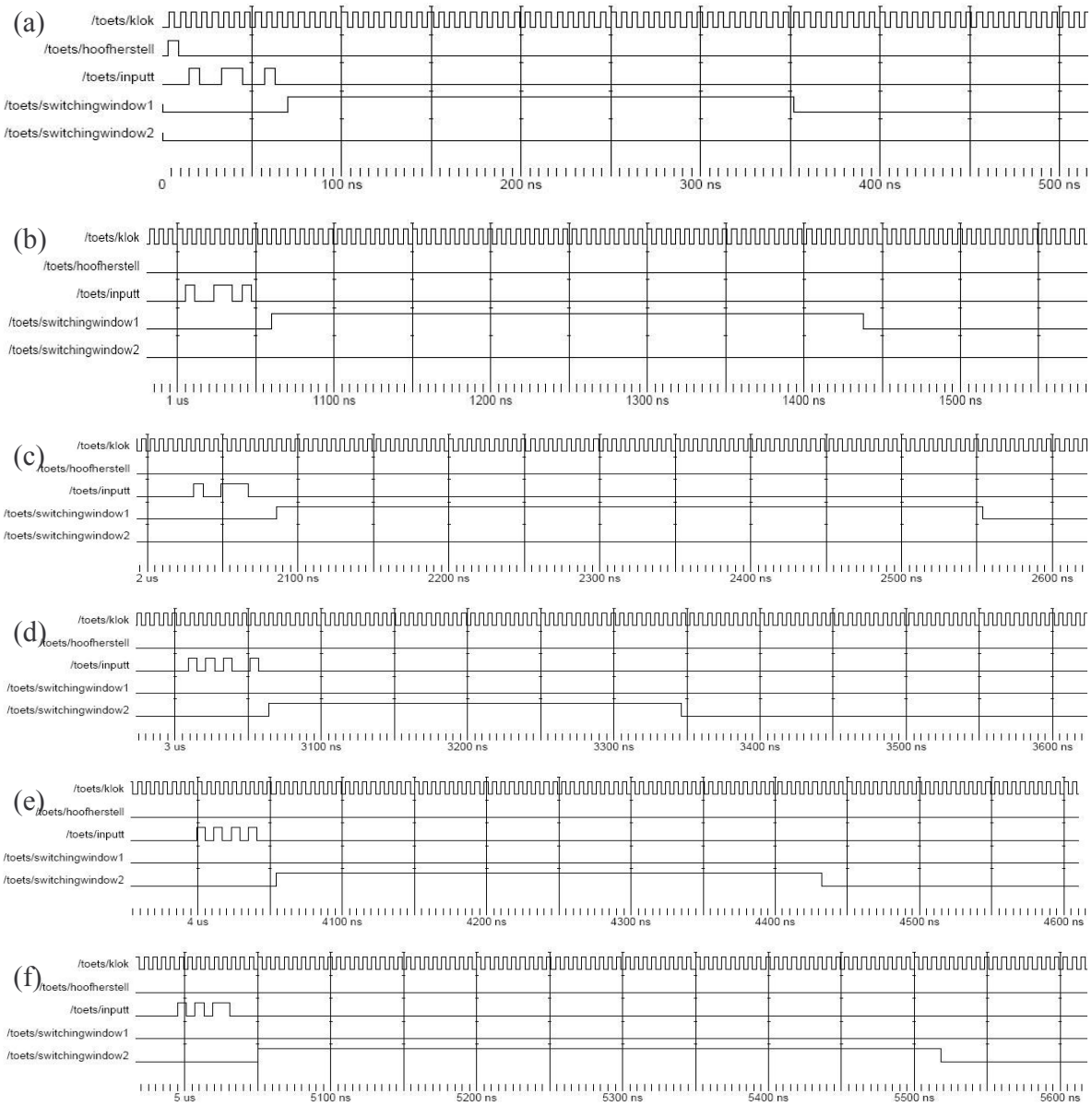


Figure 5.18

(a) A header signal of 10011001 causes output 1 to become high for 282 ns, (b) a header signal of 10011010 causes output 1 to become high for 378 ns, (c) a header signal of 10011100 causes output 1 to become high for 468 ns, (d) a header signal of 10101001 causes output 2 to become high for 282 ns, (e) a header signal of 10101010 causes output 2 to become high for 378 ns, (f) a header signal of 10101100 causes output 2 to become high for 468 ns.

5.7.2 The experimental results

The simulations were successful and the Coolrunner II CPLD was programmed with the logic design from Figure B.7. The experimental set-up of Figure 4.6 was used, except that at this stage longer input buffers were used because it takes longer to process the 8-bit headers. The three packets that were used for the physical experiment are shown in Figure 5.19. Packet one has a payload length of 100 ns and is destined for output 1, packet two has a payload of 200 ns and is destined for output 2 and packet three has payload length of 300 ns and is destined for output 3.

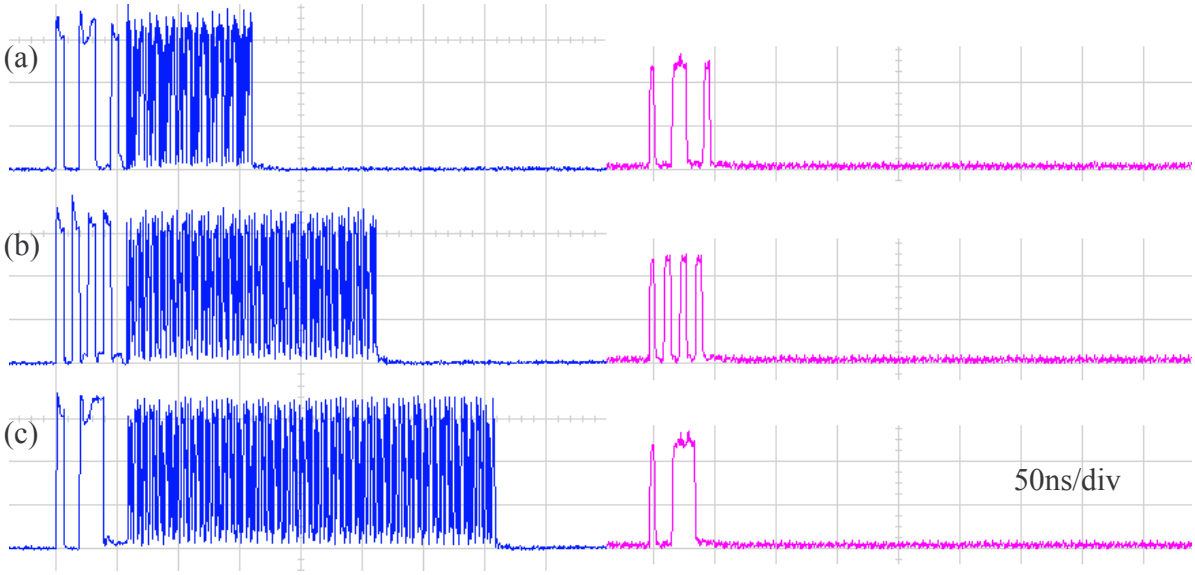


Figure 5.19

The three packets used in experiment 2 are shown here in the optical (blue) and electrical (pink) domain. The first packet (a) has header 10011001 (100 ns payload and destined for output 1), the second packet (b) has header 10101010 (200 ns payload and destined for output 2) and the third packet has header 10011100

Owing to the long switching window for packet three (500 ns) and the duty cycle of 20% that needs to be maintained, these three packets were sent every 2 μs. The input packet stream is shown in Figures 5.20(b) and (d). One can clearly see the short packet (100 ns) in the beginning (left) followed by the longer one (200 ns). The third packet is the longest (300 ns) of them all and this sequence repeats itself. In Figure 5.20(a) the electronic signal (switchingWindow_1) sent to switch cell Z1 is shown. It only opens when a 100 ns or 300 ns

packet arrives at the OXS. This proves that the logic design of the CPLD is functioning correctly. The electronic signal (switchingWindow_2) that is sent to Z2 is shown in Figure 5.20(d) and only becomes high when a 200 ns packet needs to be switched.

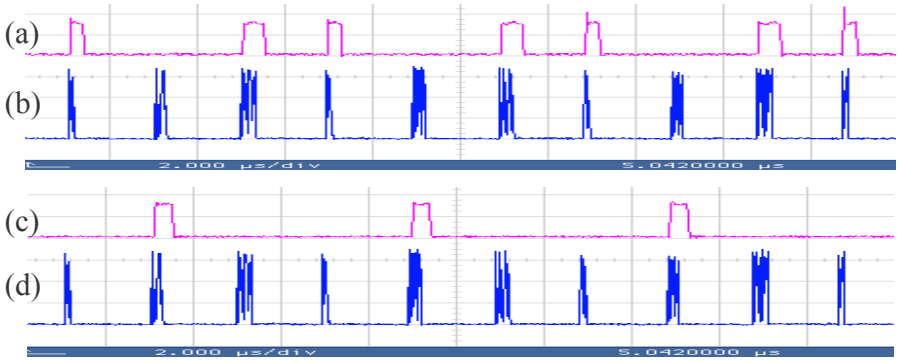


Figure 5.20

The input sequence used in experiment 2 (b), (d). The electronic signal sent to switch cell Z1 (output 1) is shown in (a) and the electronic signal sent to switch cell Z2 (output 2) is shown in (c). [2 µs/div]

The output expected at output port 1 is only packets of length 100 ns and 300 ns. They will be separated by 4 µs (100 ns-300 ns) and 2 µs (300 ns-100 ns). The output packet stream from output port 2 should only have packets of length 200 ns separated by 4 µs each. Figure 5.21(b) shows the input packet stream on a 500 ns/div scale. The black line separates the two screen shots taken on two parts of the packet stream. The screen shot on the left is for output 1 and the screen shot on the right is for output 2.

The graph from Figures 5.21(a) and (c) is the electronic control signal sent to the switch cells. Figure 5.21(d) shows the output stream and confirms that the experiment is working as planned. Figure 5.21(d) on the left is the optical signal measured from output 1 with only 100 ns and 300 ns packets. The corresponding switching windows, shown directly above them, are 300 ns and 500 ns respectively. Figure 5.21(d) on the right is the optical output measured from output 2 and contains only packets of 200 ns. These packets' switching window is shown directly above them as well and is 403 ns long.

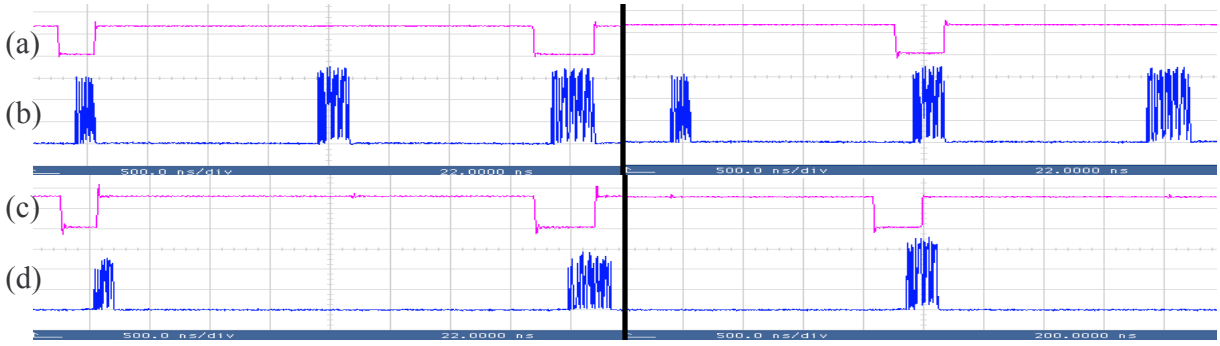


Figure 5.21

The left part of the figure corresponds to switch cell Z1 and output 1. The right part of the figure corresponds to switch cell Z2 and output 2. In (a) and (c) the electronic control signal sent to the switch cells is shown. In (b) the input packet stream is shown and in (d) the output packet stream is shown.

The experiment was successful. Packets destined for output 1 were sent to output 1 and packets destined for output 2 were sent to output 2. The length of the packet was detected and the switch cell was opened accordingly. To measure the degradation in quality of the signal the output eye diagram was displayed. For these packets with 8-bit headers the modulator needed to be adjusted so the input eye diagram was measured again for this experiment. The eye diagram for the input packets is shown in Figure 5.22. The DCA measured the Q-factor as 18.76 (BER = 8.043×10^{-79}). The packets entered the OXS with an average optical power level of 1.1 dBm. The average optical power at output 1 (after the EFDA and band pass filter) is –6.5 dBm and at output 2 is –7.9dBm. It is at these power levels that the output eye diagrams were measured.

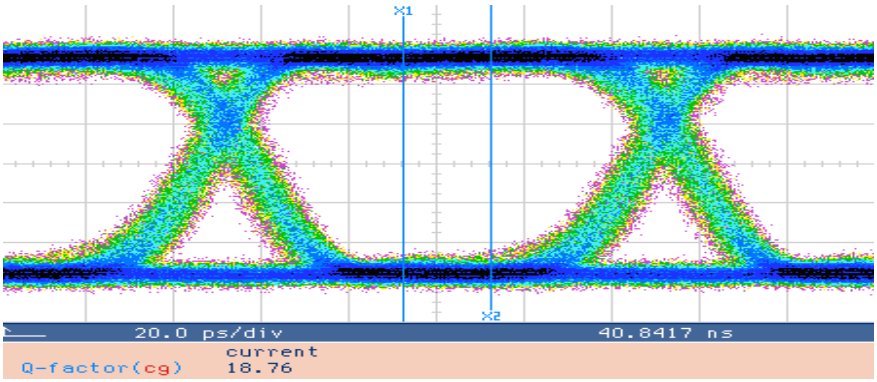


Figure 5.22

The eye diagram for the input packet stream for experiment 2

The eye diagram for output 1 is shown in Figure 5.23(a) and the Q-factor is estimated (from equation 5.1) as 8.7878 corresponding to a BER of 7.7222×10^{-19} (from equation 5.2). For output 2 the Q-factor (from equation 5.1) is estimated as 7.8472 and the BER was calculated (from equation 5.2) as 2.16065×10^{-15} .

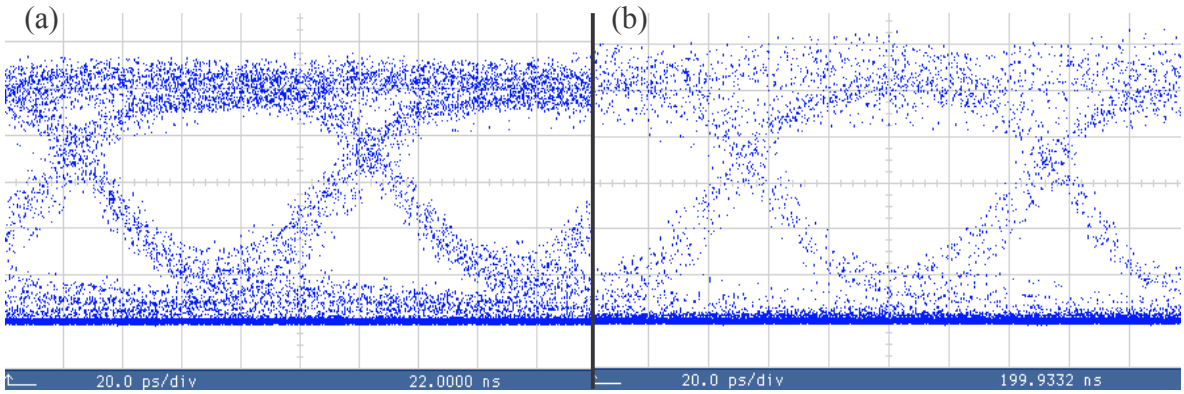


Figure 5.23

The eye diagrams for experiment 2 at (a) output 1 and (b) output 2

5.7.3 Asynchronous packet stream

The PPG was programmed to generate these packets from experiment 2 asynchronously. This had no influence on the system's performance and correct switching was measured. The electronic control has the capability to handle asynchronous traffic because the logic design of the Coolrunner II CPLD supports it. The logic design works in such a way that if it has finished sending the switching window control signal to the OXS, the whole circuit is reset and waits for the next packet. Therefore the next packet can arrive at the OXS at any time directly after the current packet has been switched.

5.8 Experiment 3: Using a 4-bit header packet to demonstrate contention resolution in a photonic packet switching network from two inputs to one output.

5.8.1 The logic design and simulation results

For the third experiment, the problem of contention was addressed. Two packets of the same length and on the same wavelength arrive at the OXS at exactly the same time on input 1 and input 2. The schematic diagram of the logic design's top view is shown in Figure B.10. The

design has five inputs, the clock, the reset, input 1, input 2 and the input from a buffer. Input 1(IN1), input 2 (IN2) and the buffer input (BUF) enter the component "DETERMINE STATE". Each one of them is processed separately because they represent information from different inputs of the OXS. The logic of "DETERMINE STATE" is shown in Figure B.11. Each input enters the SLI port of an SR4CE shift register. The input is shifted to the output ports, Q0, Q1, Q2 and Q3, of the shift register.

Because the header's first bit is a one, if the header has been shifted into the shift register fully, port Q3 will be high. The three Q3 ports are fed into a NOR3 component that is connected to the CE ports of the shift registers. If any one or three of the Q3 ports becomes high, the all three shift registers' CE port becomes low, resulting in the output port remaining constant with their current value. The information on the output port should now be the headers. Three AND gates are then used per shift register to determine what information is encoded in the header. Once again a 4-bit header is used with only output information. In the next step, four 9-input AND gates determine the state of the three inputs. The first output of the 9-input AND gate becomes high only if input 1 and input 2 have packets destined for output Z. The second 9-input AND gate becomes high if only input 1 has a packet destined for output Z. The third 9-input AND gate becomes high if only input 2 has a packet destined for output Z and the fourth 9-input AND gate becomes high only if the buffer input has a packet for output Z.

The output of "DETERMINE STATE" has six outputs corresponding/connected to the six SMA outputs of the electro-optic control board. SMA2 is connected to switch cell Z1, SMA3 is connected to switch cell Y2, SMA4 is connected to switch cell Z2 and SMA5 is connected to switch cell Z3. The other two SMA outputs, SMA6 and SMA7, are always high and are not used in this experiment. In "DETERMINE STATE" the last set of logic gates relates the state of the OXS (output bits of four 9-input AND gates) to one of the four switch cells, depending on which switch cell is required to switch the packets for that state correctly. These output are controlled by the "ENSW" signal from the state machine. This signal represents the time that the switch cell must be switched on. The last output of "DETERMINE STATE" is "packet" that becomes low if a packet has been received on any of the three input ports. This "packet" signal is fed into the state machine.

The state machine, "SHELL_SM" is shown in Figure B.12. It waits in state, "waiting" the whole time until "packet" becomes low. It then moves to state "active", thus activating the counter and switching window. The state machine stays in this state until the counter reaches 46 counts corresponding to 294.4 ns, enough time to switch the 140 ns long packets. After 46 counts, the state machine resets the counter and the three shift registers from "DETERMINE STATE" to be ready for the next headers. Synchronous timing is of the utmost importance in this experiment to ensure that the headers of input 1 and input 2 arrive at exactly the same time.

This logic design is then simulated with ModelSim XE III 6.0d. The input packet stream is set so that the four possible situations are repeated the whole time. These four situations are a packet from input 1 only, a packet from input 2 only, packets from input 1 and input 2 at the same time and a packet from the buffer input only. The results are shown in Figures 5.24 and 5.25.

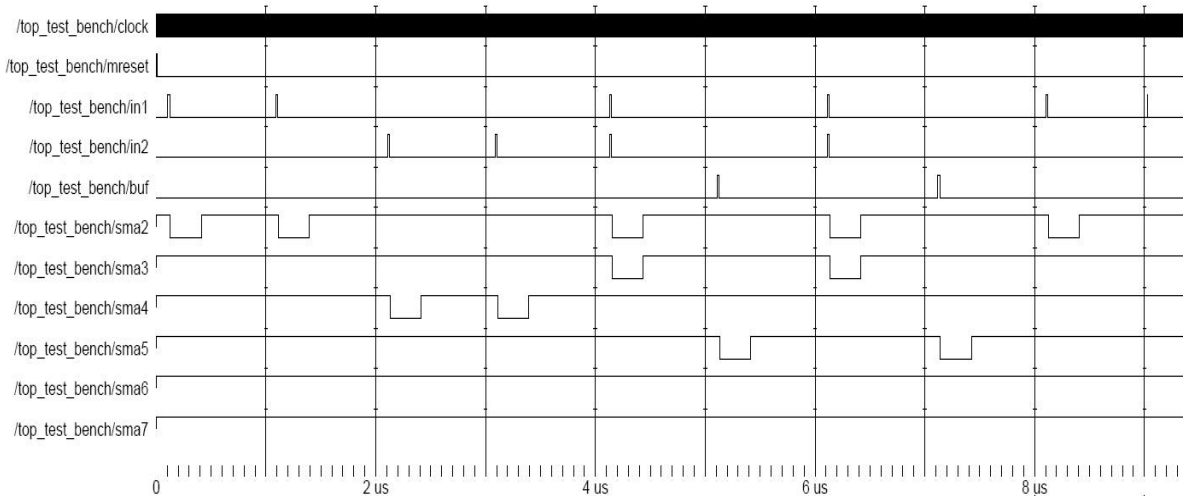


Figure 5.24

ModelSim simulation results for the logic design of Figure B.10. Packets are switched from two inputs to one output. Contention occurs after 4 µs and after 6 µs. The logic sent control signals to the OXS via its SMA ports with sma2 = Z1, sma3 = Y2, sma4 = Z2 and sma5 = Z3.

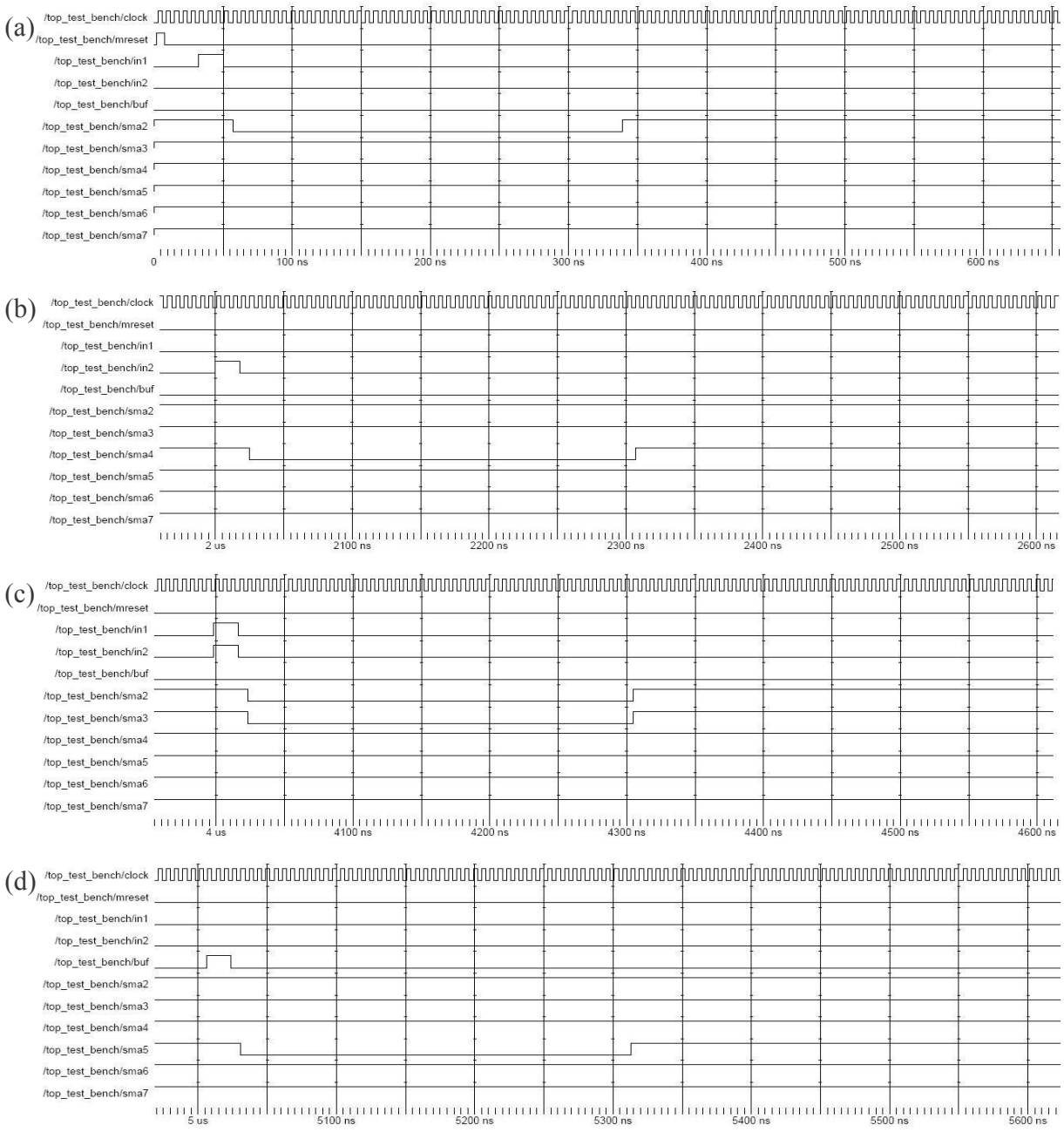


Figure 5.25

A closer look at the simulation results for experiment 3: In (a) a packet is switched from input 1 to output Z by activating only switch cell Z1 (sma2). In (b) a packet is switched from input 2 to output Z by activating only switch cell Z2 (sma4). In (c) contention occurs and the packet from input 1 is switch to output Z (by switch cell Z1 (sma2)) while the packet from input 2 is switched to output Y (by switch cell Y2 (sma3)), the buffer. In (d) the packet from the buffer is switched to output Z by activating only switch cell Z3 (sma5).

The simulation results were successful and the Coolrunner II CPLD was programmed with this design (Figure B.10).

5.8.2 The experimental results

The experimental set-up of Figure 4.10 was used for experiment 3. The PPG was programmed to generate packets with 4-bit headers, 12.8 ns guard time and 140 ns payload. These packets were sent every second timeslot, a timeslot being 1.107 µs. This was done so that every second timeslot was an open timeslot. The contending packet would be switched to this open timeslot. The input sequence is shown in Figure 5.26.

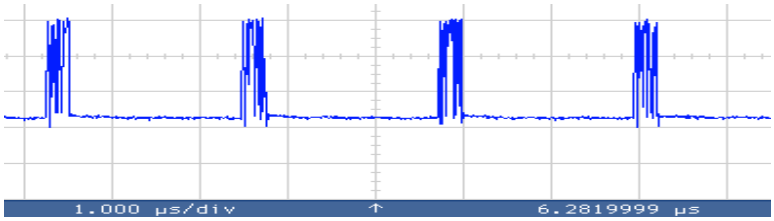


Figure 5.26

The input sequence for experiment 3 is shown here. Fixed length packets are sent every second timeslot, a timeslot being 1.107 µs.

This input sequence was passed through a 50:50 coupler to create two identical input packet sequences. These two packet sequences then enter the OXS via input 1 and input 2. Optical power is tapped from both inputs with 30:70 couplers. The electronic control processes these two headers at the same time, detect the contention and switch open switch cells Z1 and Y2 to switch the packet from input 1 to output Z (the destined output of packets from input 1 and input 2) and the packet from input 2 to output Y. Output Y is a delay buffer of 1.107 µs long. Figure 5.27(b) shows the packet sequence from output Z. Packets are present every second timeslot. These are the packets from input 1.

Figure 5.27(a) shows the electronic control signal sent to switch cell Z1 and Figure 5.27(c) shows the control signal sent to switch cell Y2. In Figure 5.27(d) the packet sequence exiting the 1.107 µs are displayed. These packets are the packets that entered the OXS via input 2, being switched by switch cell Y2 to the buffer. There are packets present every second timeslot. If one compares it to Figure 5.27(b), it is clear that these packets have been delayed

by one timeslot. Optical power is once again tapped of, the header is processed again and since in this timeslot only one packet enters the OXS (from the buffer) and is destined for output Z, the electronic control switch opens switch cell Z3 to switch these packets to output Z.

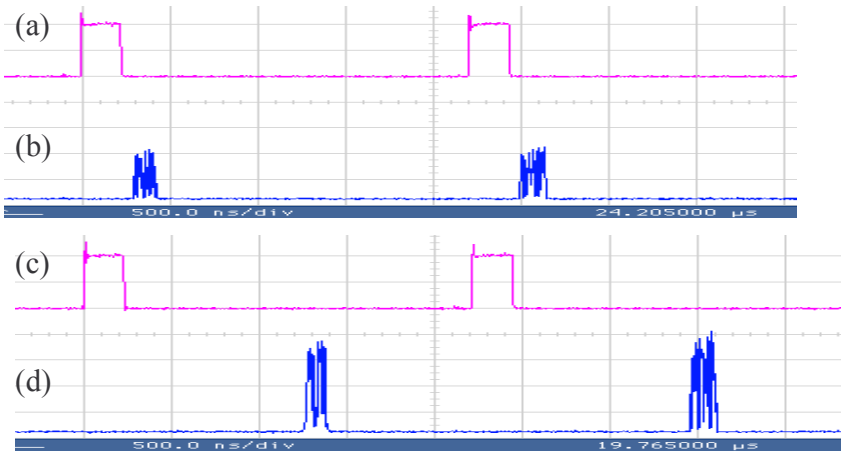


Figure 5.27

The electronic control signals being sent to switch cell (a) Z1 and (c) Y2 are shown here. The packet sequence exiting output Z is shown in (b) and the packet sequence exiting the buffer is shown in (d).

Therefore the final output sequence will contain a packet in every timeslot. Figure 5.28(b) shows the final output sequence from output Z with the electronic control signal sent to switch cell Z3 shown in Figure 5.28(a).

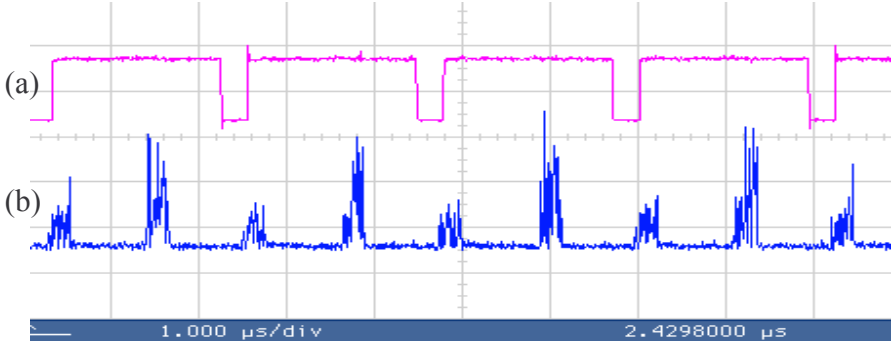


Figure 5.28

The electronic control signal being sent to switch cell Z3 is shown in (a) and the final output from output port Z is shown in (b).

Note the power level difference in the output sequence. The packets with higher optical power are those being switched only from input 1 to output Z. The packets with lower optical power are those from input 2, being switched to the buffer and then again being switched to output Z. Because of this difference in optical power levels, the eye diagrams for the output packets were determined separately. The input eye diagram is the same one as in Figure 5.8. The buffer was disconnected, resulting in only packets from input 1 being present at output Z. Their eye diagram was measured and is shown in Figure 5.29. The Q-factor was estimated (from equation 5.1) to be 5.8511 and the BER calculated from equation 5.2 to be 2.50932×10^{-9} .The eye diagram was measured at an average optical power level of –11.2 dBm.

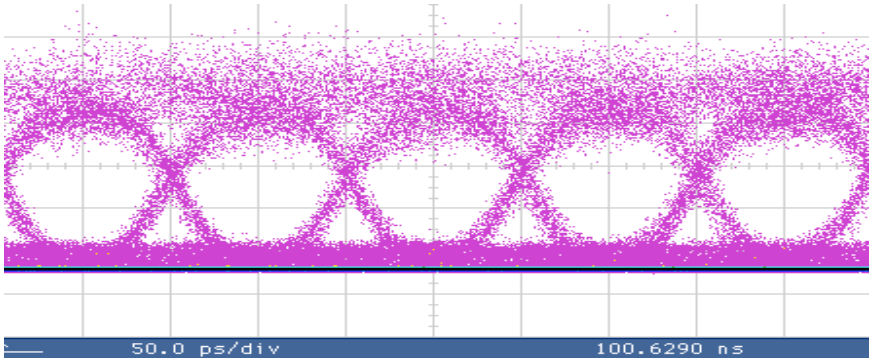


Figure 5.30

The eye diagram for packets from input 1 to output Z taken at output Z after the EDFA and band pass filter

The buffer was connected again and switch cell Z1 was manually closed. This resulted in only packets from input 2 via the buffer being present at output Z. The eye diagram is shown in Figure 5.31. The quality of these packets is much lower than the quality of packets from input 1 at output Z. The Q-factor, determined from equation 5.1, is 4.2949 corresponding to a BER of 9.17113×10^{-6} calculated from equation 5.2. This eye diagram was measured at an average optical power level of –15.2Bm.

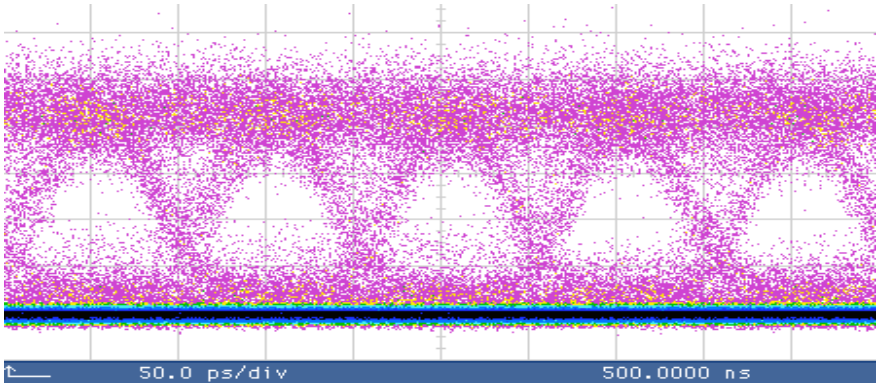


Figure 5.31

The eye diagram of the contending packets from input 2 to output Z at output Z.

The noise levels on the packets from input 2 are high owing to the packets being switched via two switch cells. The packets arrive at input 1 with an average optical power level of –2.7dBm and at input 2 with an average optical power level of –2.3dBm. The packets from the buffer arrive at the OXS at an average optical power level of –4.1dBm. This optical input power entering the OXS is too low and will result in high signal degradation when switched by the OXS, as can be seen from the eye diagram of Figure 5.31. This eye diagram was measured at –15.2dBm average optical power, after the EDFA and band pass filter. The eye diagram from Figure 5.30 (for the packets from input 1) is measured at –11.2 dBm average optical power.

5.9 Experiment 4: Using a 16-bit header for 1-to-1 photonic packet switching

5.9.1 The logic design and simulation results

For the last experiment the aim is to test the flexibility of the electronic control to process 16-bit headers at 155 Mbit/s. Packet with headers of '1010101010101010' and payloads of 300 ns long were generated. The logic design is shown in Figure B.13. The design has three inputs, clock, reset and "input16" with one output "uitset". The 16-bit header is fed into the first component, "readin". The schematic diagram of "readin" is shown in Figure B.14.

A 16-bit shift register, "SR16CE", is used to convert the serial header to the 16 output ports of the shift register, Q[15:0]. If the header is fully read in, when "uit(15)" becomes one and CE therefore becomes zero, the shift register keeps the current output information on its output port. This is then the header: '1010101010101010' and is processed by five AND gates to

output "OUT". "OUT" will only become high if this header sequence has been received. For any other 16-bit header sequence, "OUT" will stay low. When CE becomes low, so does output "pakkie" and this results in the start of the state machine. The state machine goes from the waiting state "wagVIRpak" to the "determine" state. In the "determine" state the whole system is reset if the output from "readin" (correct) is low. If the output from "readin" (correct) is high, meaning the correct header was detected, the state machine enables the counter and switching window signal, "yes". The counter counts for 70 counts corresponding to 448 ns. The switching window is opened during this 448 ns. After 70 counts the whole state machine and shift register are reset and wait for the next packet to arrive.

Figure 5.32 shows the ModelSim XE III 6.0d simulation results. A 16-bit header, '1010101010101010' was sent to "input16" and the output "uitset" switched high for 448 ns. The Coolrunner II CPLD was programmed with this logic design and the physical experiment is described next.

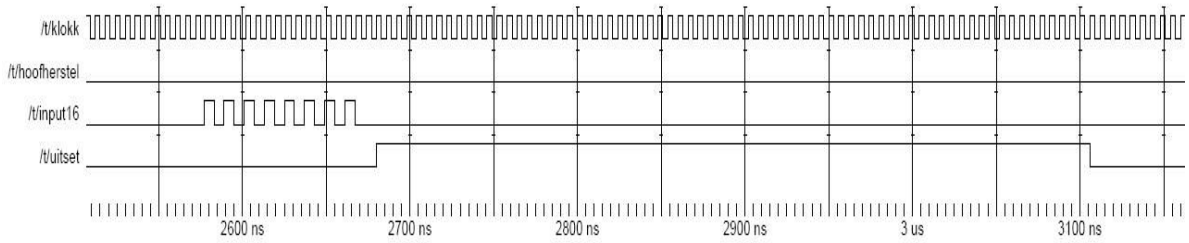


Figure 5.32

The simulation results for experiment 4. The input header sequence is shown next to "/t/input16" and the output of the logic design from Figure B.13 is shown next to "/t/uitset"

5.9.2 The experimental results

The same set-up as in Figure 4.6 was used for the experiment. The input buffer was increased to twice the one used for the 4-bit headers. An input buffer length of 183.8 ns (18×6.4 ns (processing time) + 75ns (switch cell rise time) is required but this buffer length is 234 ns, which will be sufficient. The packet in the optical domain is shown in Figure 5.33(b). The electronic control signal measured just before the Coolrunner II CPLD is shown in Figure

5.33(a). The quality of the electronic header signal is good and the Coolrunner II CPLD should not have a problem to process the header.

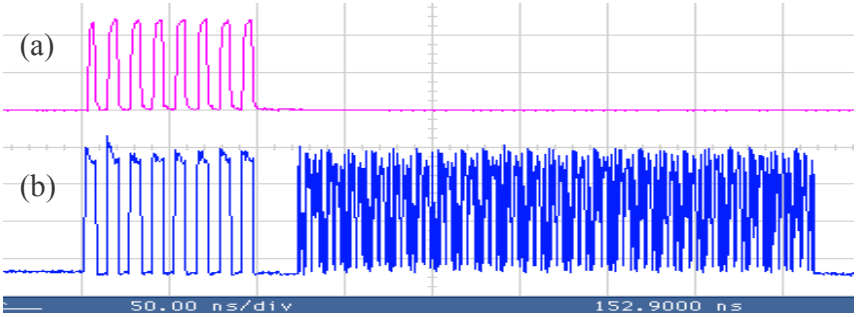


Figure 5.33

The packet used for experiment 4 in the (a) electronic domain and (b) optical domain

Figure 5.34(b) shows the input packet stream. Packets are sent every 1 μs and the duty cycle for this experiment was 45%. The control signal sent to switch cell Z1 is shown in Figure 5.34(b) and serves as proof that the electronic control did successfully process the 16-bit header. The switching window signal only becomes high for 448 ns if the input header signal is '1010101010101010'.

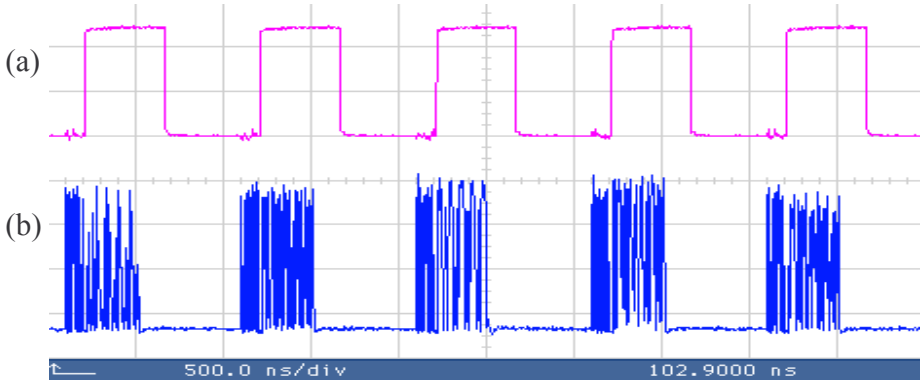


Figure 5.34

The switching window is shown in (a) with the input packet stream shown in (b).

A new input eye diagram was taken because the PPG was programmed with a different program for generating a 16-bit header and this results in a different setting for the 10 Gbit/s optical modulator. The input eye diagram was taken just before entering the OXS and is shown in Figure 5.35. The average optical input power is 2 dBm and the Q-factor is estimated to be 8.9423 (from equation 5.1) with a BER of 1.92904×10^{-19} from equation 5.2.

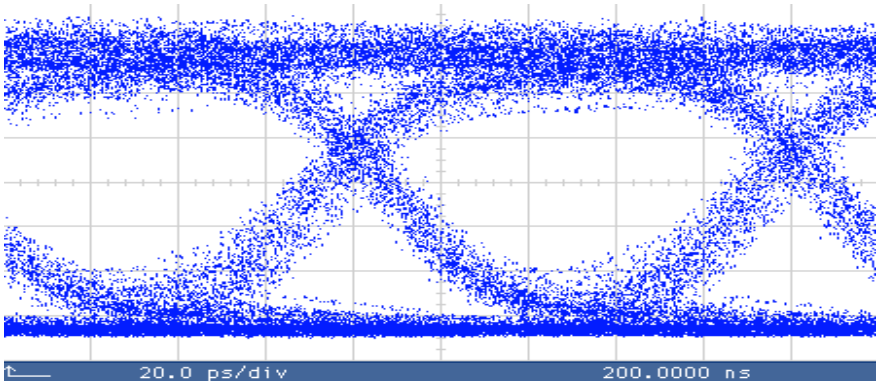


Figure 5.35

The eye diagram of the input packet sequence

The output eye diagram is shown in Figure 5.36. The average optical power was measured at –6.8 dBm. The reason for the lower quality is the duty cycle that was increased to 45% instead of the normal 20%. The switch cell was switched on for longer and more frequently in this experiment, resulting in higher temperatures of operation. The Q-factor was estimated at 6.5833 (from equation 5.1) corresponding to a BER of 2.35147×10^{-11} calculated from equation 5.2.

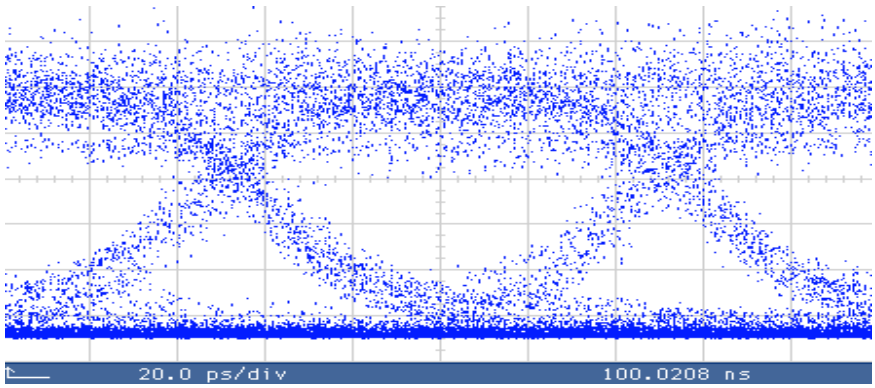


Figure 5.36

The eye diagram of the output packet stream

5.10 Discussion of experimental results

The discussion of the experiments will focus on the BER values that were calculated from equation 5.2 using the estimated Q-factor. The three main causes of degradation in packet

quality (higher BER values) are related to the input power entering the OXS, the specific switch cell transmission characteristic and thermal conditions.

A summary of the results and measurements is given in Table 5.3. The experiment number is referred to, as well as the figure of the corresponding eye diagram. The logarithmic (base 10) value of the BER is also given for better comprehension when making comparisons.

#	Figure	Experi-ment	Switch cell	Input power	Duty cycle	Output power	BER	Log_{10}(BER)
A	5.9c	1a	Z1	1.3dBm	23%	-7.6dBm	2.44E-12	-11.61
B	5.10c	1a	Z2	1.3dBm	23%	-8.1dBm	6.82E-12	-11.17
C	5.11c	1a	Z3	1.3dBm	23%	-8.7dBm	1.43E-10	-9.84
D	5.16	1b	Z1	0.7dBm	10-30%	-6.3dBm	4.67E-15	-14.33
E	5.23a	2	Z1	1.1dBm	17%	-6.5dBm	7.72E-19	-18.11
F	5.23b	2	Z2	1.1dBm	9%	-7.9dBm	2.16E-15	-14.67
G	5.30	3	Z1	-2.7dBm	11%	-11.2dBm	2.51E-09	-8.60
I	5.31	3	Y2, Z3	-2.3dBm, -4.12dBm	11%	-15.2dBm	9.17E-06	-5.04
J	5.36	4	Z1	2dBm	45%	-6.8dBm	2.35E-11	-10.63

Table 5.3

A comparison of the results from all experiments

The effect of the switch cell's transmission characteristic is clearly visible from the results of experiment 1a. According to Figure 4.1, switch cells Z1 and Z2 have optical power loss of 23 dB. Switch cell Z3 has an optical power loss of 26 dB. The BER of packets being switch from switch cell Z3 is higher than the BER of packets switched by switch cell Z1 and Z2. The input optical power for all three switch cells is 1.3 dBm but the output, after being amplified by EDFA_3 and passed through a band pass filter, is the lowest for switch cell Z3. Therefore the higher the loss of the specific switch cell, the lower output power will be measured, resulting in higher BER values.

Looking only at the results of switch cell Z1, if the input optical power is higher than 0.7 dBm, the output optical power will be in the range of –6.3 dBm to –7.6 dBm optical power. However if the input is –2.7 dBm, the output is lower than –10 dBm and the acceptable BER is reached. Therefore higher BERs are measured for lower input power.

In experiments 1b and 2 the BER rate for using switch cell Z1 is much lower than that of using switch cell Z1 for experiment 1a. These three experiments were compared because they have similar input powers and they all use switch cell Z1. In experiment 1a the switch cell's duty cycle is about 23% and in experiment 1b the switch cell's duty cycle changes from 10% to 30%. In experiment 2 the duty cycle of Z1 is 17%, resulting in the lowest (best) BER. Therefore the lower the duty cycle, the lower the BER. At these duty cycles the switch cell does not get hot (>70ºC).

In experiment 4, also high input optical power (2 dBm), the duty cycle is 45% and switch cell Z1 (the best one) is used. The BER rate is higher than expected, which is due to the switch cell's temperature increase because of the high duty cycle. Although the BER is high, it is still within the acceptable range according to [13].

Figure 5.37 compares the output eye diagrams' BER with the average optical power at which they were determined for all the experiments. The higher optical power received, the lower BER was achieved.

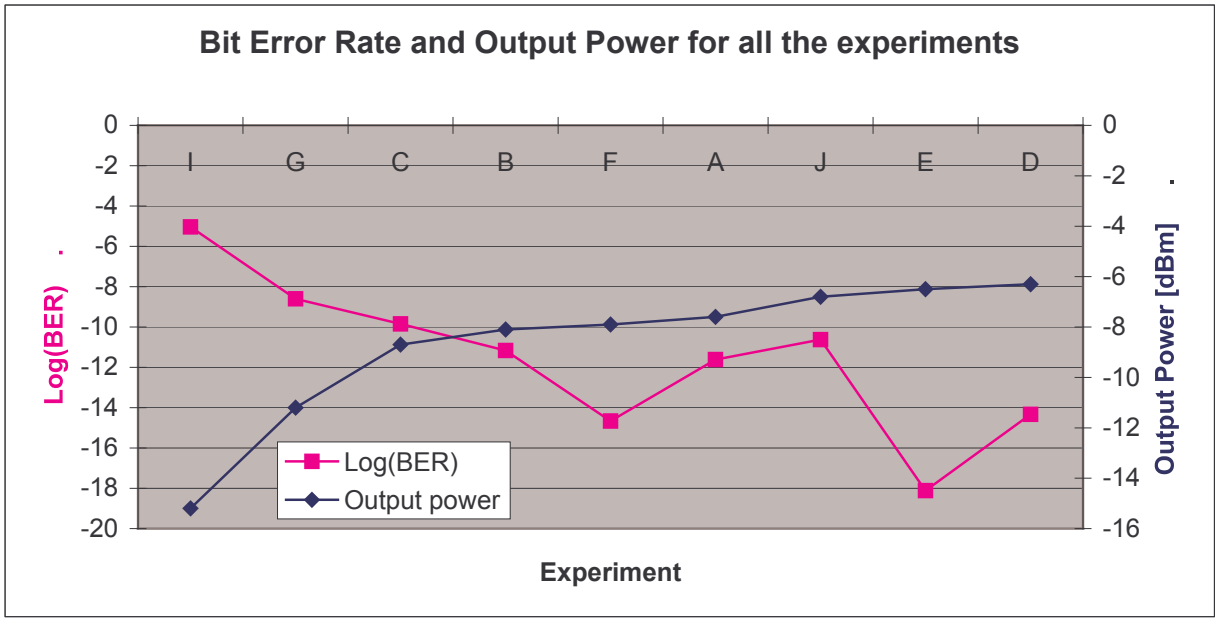


Figure 5.37

Comparison of the BER at the output power at which they were determined

Jitter was not observed at the output eye diagram. The distance over which the input and output eye was measured was no more than 5 m. Jitter will only have an effect over longer distances due to dispersion in the optical fibre.

The electro-optic control interface managed to process the 155 Mbit/s headers successfully. The control signals sent to the current control were of high quality. No excessive overshoot or undershoot was detected and the rise and fall time of the electronic control signal was lower than 2 ns.

To conclude, the following three specifications are advised when operating the OXS in a photonic packet switching network to obtain BER of less than 10^{-9} :

- The average optical input power to the OXS should be higher than 0dBm.
- A switch cell with optical power loss of not more than 30 dB should be chosen.
- The switching duty cycle of the switch cell should be less than 45%.

CHAPTER 6: DISCUSSION AND CONCLUSION

6.1 Discussion of research results

The problem addressed in this research was the control of an electro-optic switch and the implementation of this switch for fixed and variable length synchronous and asynchronous packet switching. This was done using a control interface design that incorporated photodiodes as well as a CPLD for an electronic processor so that the packet headers could be analyzed. The electronic control interface controlled the OXS, switching packets according to the information provided in the header.

Contention resolution was also addressed and successfully resolved for a 50% traffic load. The packet contention was detected and resolved by using a re-circulation loop buffer in combination with a 4x4 OXS matrix. If the traffic capacity increases, the contention can be resolved by 'open' slot detection and multiple re-circulations in this configuration. This would be subject to limitations of traffic density and maximum number of re-circulations due to SNR limitation. Up to nine re-circulations with reasonable signal quality have been demonstrated [20] and this scheme should be able to deal with traffic with 90% maximum density.

The research resulted in the design and implementation of an electron-optic control interface for the VAC-based OXS. PPS networks were studied and contention resolution was defined as a major problem in these networks. Experiments were set up and typical packets, used in everyday networks, were generated and sent to the OXS, thus subjecting the OXS to possible real life traffic scenarios. The experiments achieved successful photonic packet switching of fixed length packets, variable length packets and packets arriving at the OXS synchronously or asynchronously. The electro-optic control showed potential as a very flexible control system to configure the OXS for all these types of scenarios. It has the potential to process 4-bit headers, 8-bit headers and 16-bit headers. The electro-optic control also detected contention and was able to resolve this contention by configuring the OXS in such a way as to switch one contending packet to a delay buffer. This contending packet then re-enters the OXS in the next timeslot.

It was found that the main contribution to optical power loss in the experimental set-up was connecting the optical fibres to the waveguides of the OXS. This loss in optical power is about 25 dB-30 dB when the input power to the OXS is 0 dBm. The aim should be to have optical input power levels of between 0 dBm and 5 dBm. Fibre pigtailed components were used throughout the whole experiment, required a large working area and introduced quite a lot of optical power loss due to the physical connections that needed to be made. Results will improve if one should implement photonic integration. Most of the components have the potential to be integrated into waveguides.

6.2 Recommendations for future work

The applications made possible with the development of an electro-optic control interface for the OXS as described in this dissertation, have emphasized various areas that may require work in future:

6.2.1 Label/header swapping

In optical burst switching nodes, label swapping is required to update label information. No label/header swapping was done in the experiment. However, the label swapping function with a scalable, high-performance solution that meets power and size constraint is a key requirement for realizing a photonic packet switching network, according to [50]. The authors from [50] demonstrate label swapping at 10 Gbit/s by using the self-clocked OCTA (Optically Clocked Transistor Array). Introducing label/header swapping into the OXS network is a very good future application and has potential for future research.

6.2.2 Header content

With the potential to process 16-bit headers, as shown in this dissertation, the electro-optic control has the potential to introduce more complex information in the header, such as security, type of service and error-correcting codes.

6.2.3 Technology interfacing

One of the main aims for the future is to integrate the optical network fully with other transport media/networks, such as wireless and satellite. At the beginning of 2000, fibre manufacturers encouraged carriers to adapt their fibre infrastructure gradually to 40 Gb/s, by replacing their legacy G.652 fibres with new and efficient G.655 fibres, nearly three times more expensive. However the events of recent years have clearly shown that the question was not well posed. Indeed, in practice the 40 Gbit/s technology has been adapted to presently installed fibre infrastructure, not the opposite. Therefore one might have to look at the network traffic requirement of these other transport media and adapt the optical network traffic to them.

6.2.4 Asynchronous operation

According to [3] the future optical network will have ATM (Asynchronous Transfer Mode) type packets. The authors from [36] support this by stating that asynchronous variable length packets are a desirable feature for the infrastructure for the Internet in the future. The designers of future optical networks should keep this in mind when designing optical networks. In the future it is anticipated that a growing part of the core network will be based mainly on two layers, the IP and optical layers [2]. “The core network is evolving to encompass a growing IP layer that will work mainly on top of an optical circuit-switching based layer. This evolution will likely dominate the network migration scene in the next few years”. So one sees that researchers predict IP based traffic of variable length travelling asynchronously across an optical network.

6.2.5 Storing variable length packets

Chapter 5 described the OXS’s capability of switching variable length packets. Buffering these variable length packets has not been demonstrated. A set-up as in Figure 6.1 is proposed to introduce variable delays into the photonic packet switching network, using the OXS. Here two OXS are inter-connected. The first one serves as a normal 3×3 optical switch with the fourth output leading to the second OXS. This second OXS can be configured to supply variable delays ranging from a few nanoseconds up to a few milliseconds if the correct length

of fibre is used as delays d_1, d_2 and d_3. The output of this second OXS is again fed back to the first OXS as the fourth input.

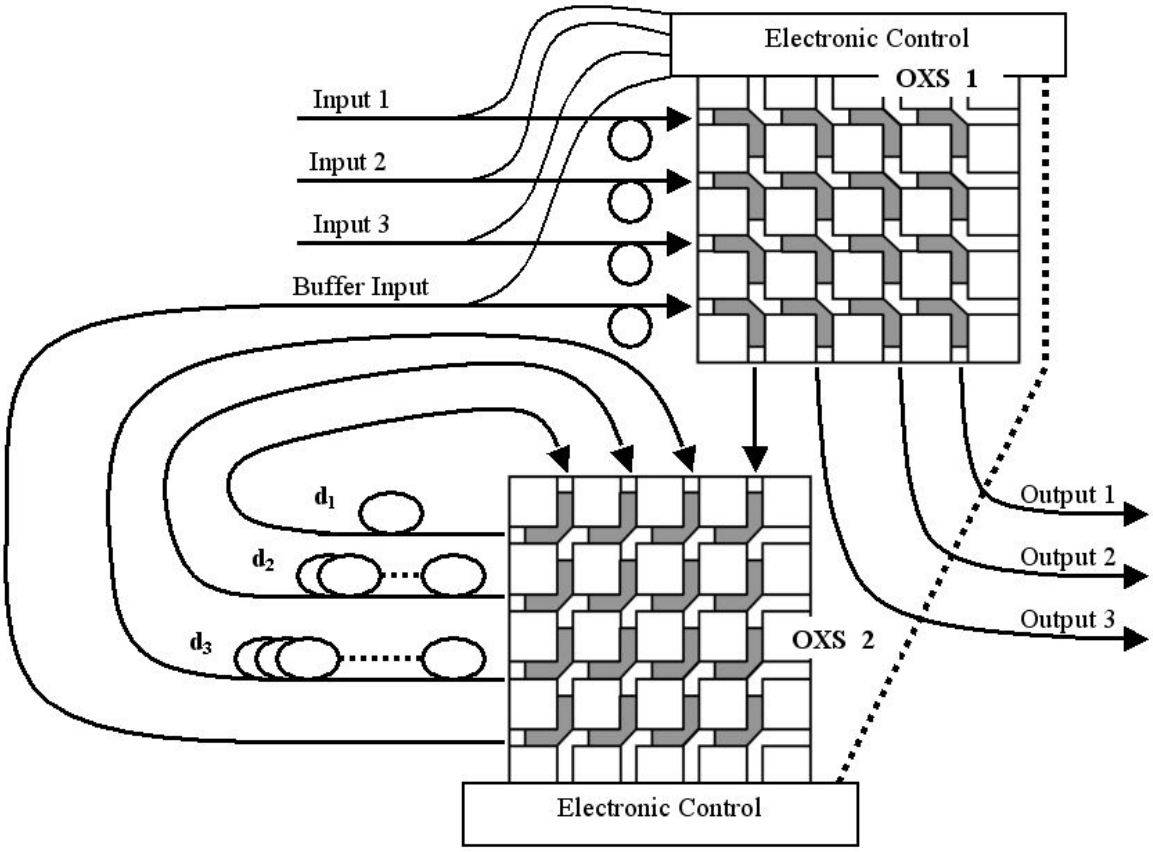


Figure 6.1

Using the OXS to store variable length packets. OXS 1 is operated as a normal 3×3 optical switch. The fourth input and output connect to the second OXS configured as a variable delay buffer. Packets from OXS 1 can be stored for a variable time when OXS 2 is configured accordingly.

The work described in this dissertation has emphasized the application flexibility of the OXS by showing that it can be used for fixed or variable length packets, for synchronous or asynchronous switching, and that effective optical contention resolution is possible owing to the OXS's low crosstalk capabilities. These results show that the OXS is a promising technological solution for future optical networks that require high capacity throughput, optical transparency and network agility.

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ADDENDUM A:

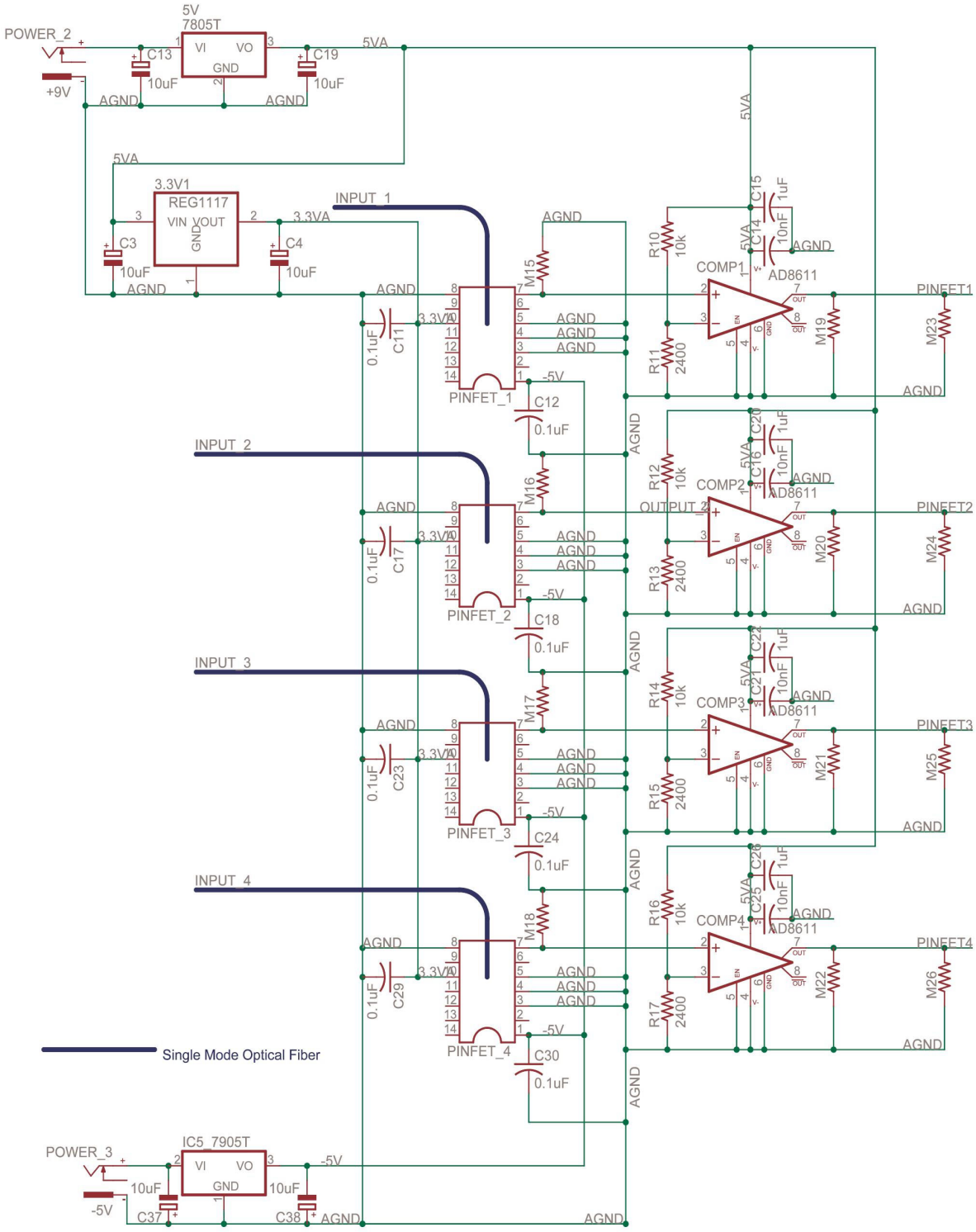

Figure A.1

The schematic diagram of the analog part of the electro-optic control circuit

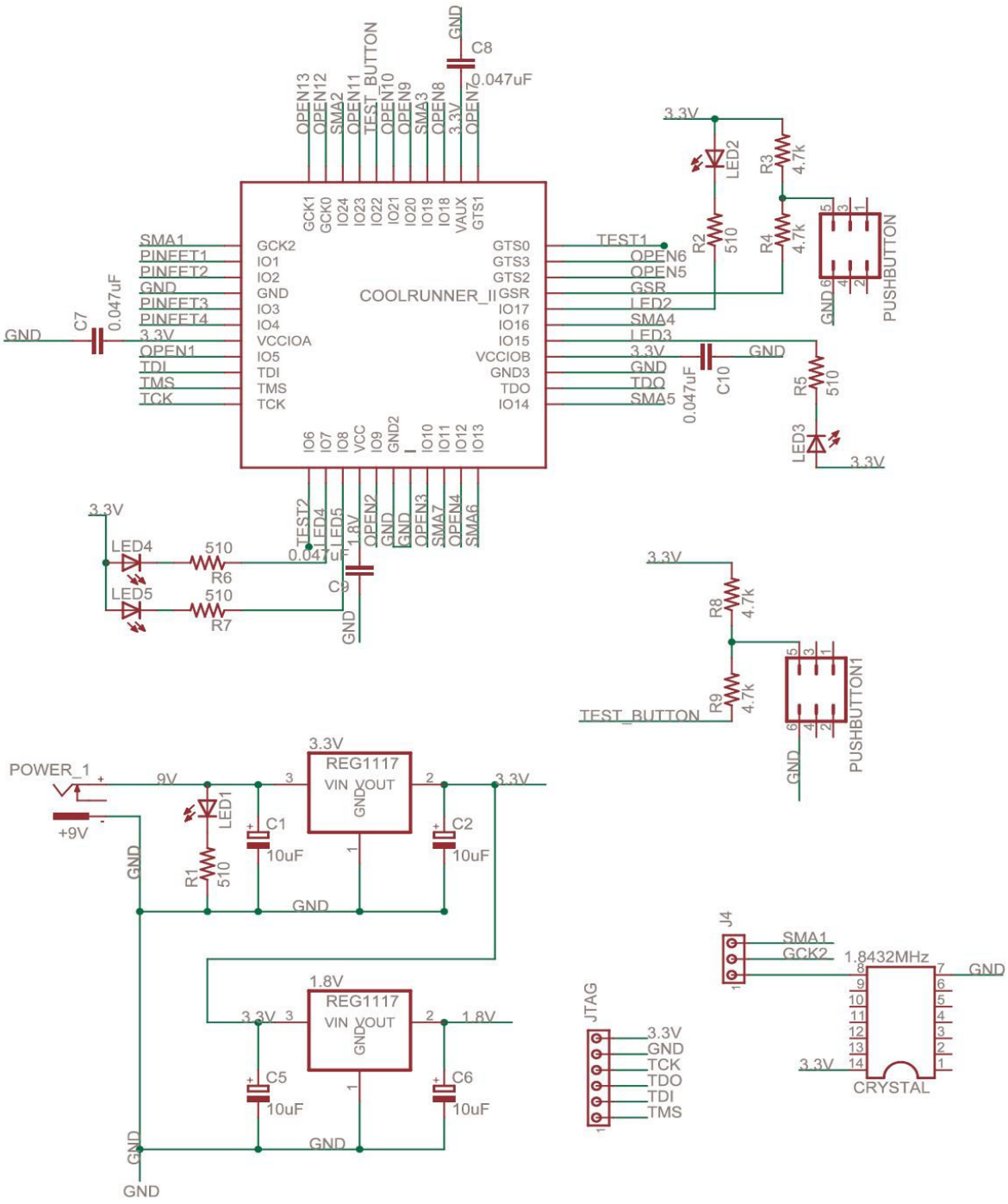

Figure A.2

The schematic diagram of the Xilinx Coolrunner II CPLD with its interfaces to the rest of the circuit

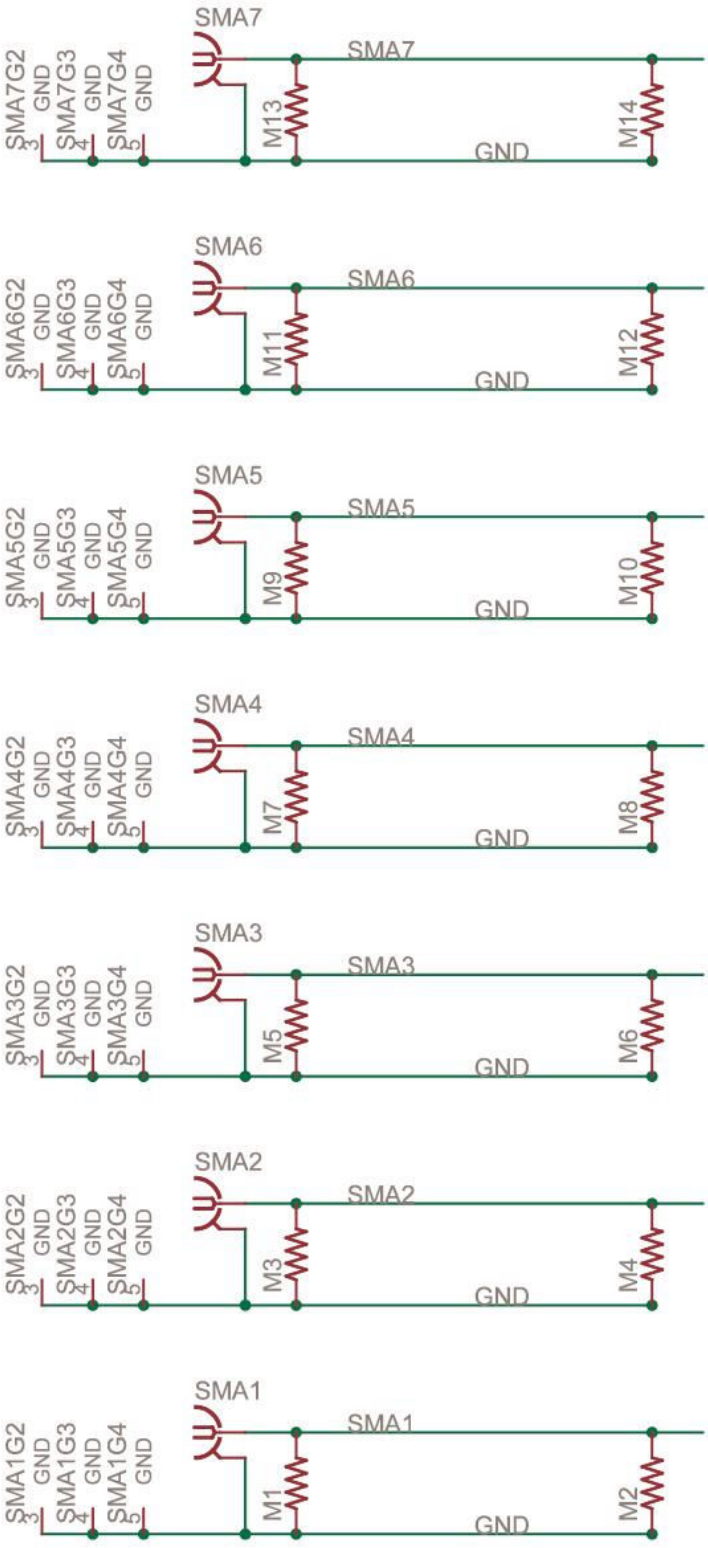

Figure A.3

The schematic diagram of the SMA connectors

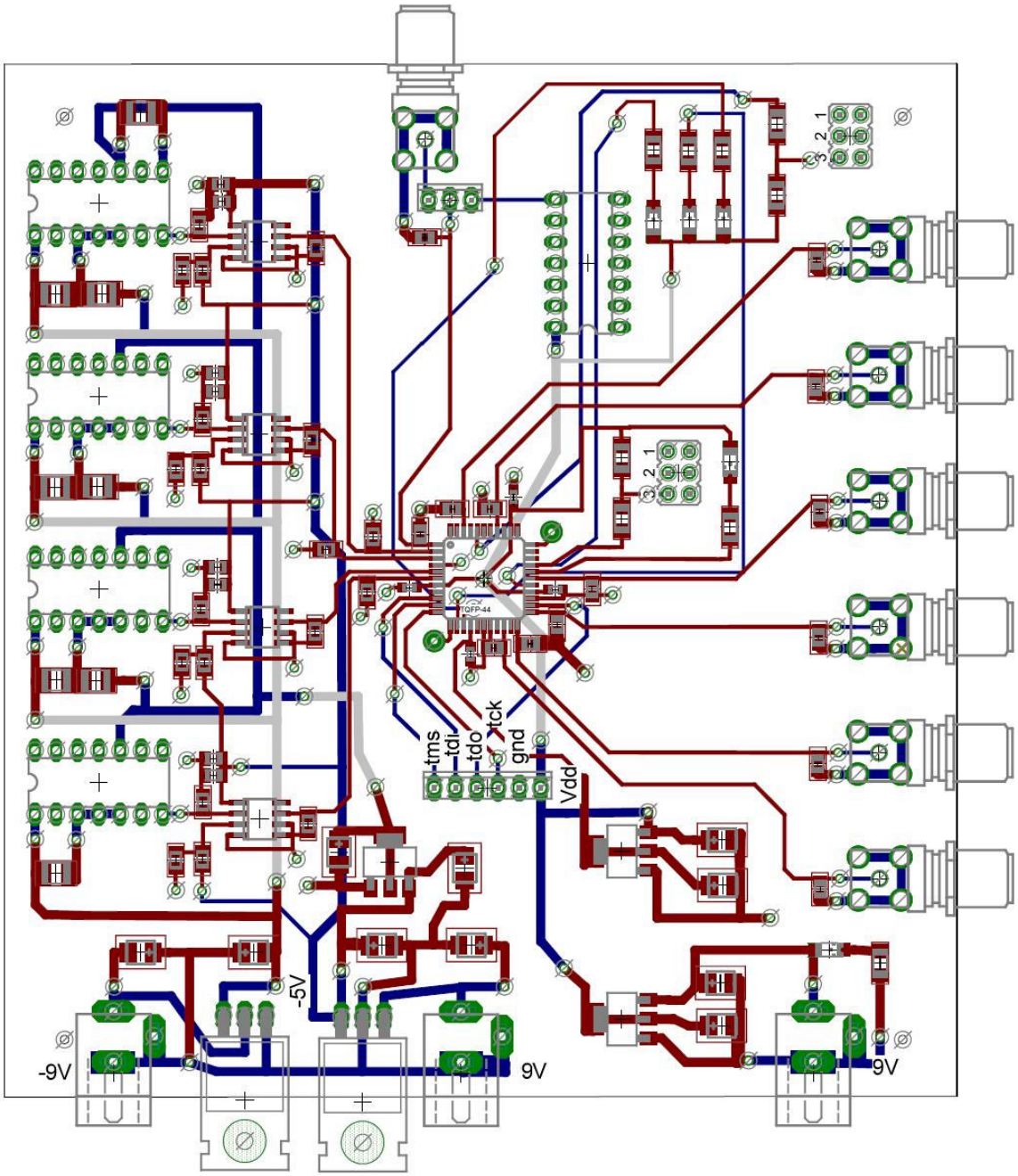

Figure A.4

The layout and packaging of the components on top of the electro-optical control PCB

ADDENDUM B:

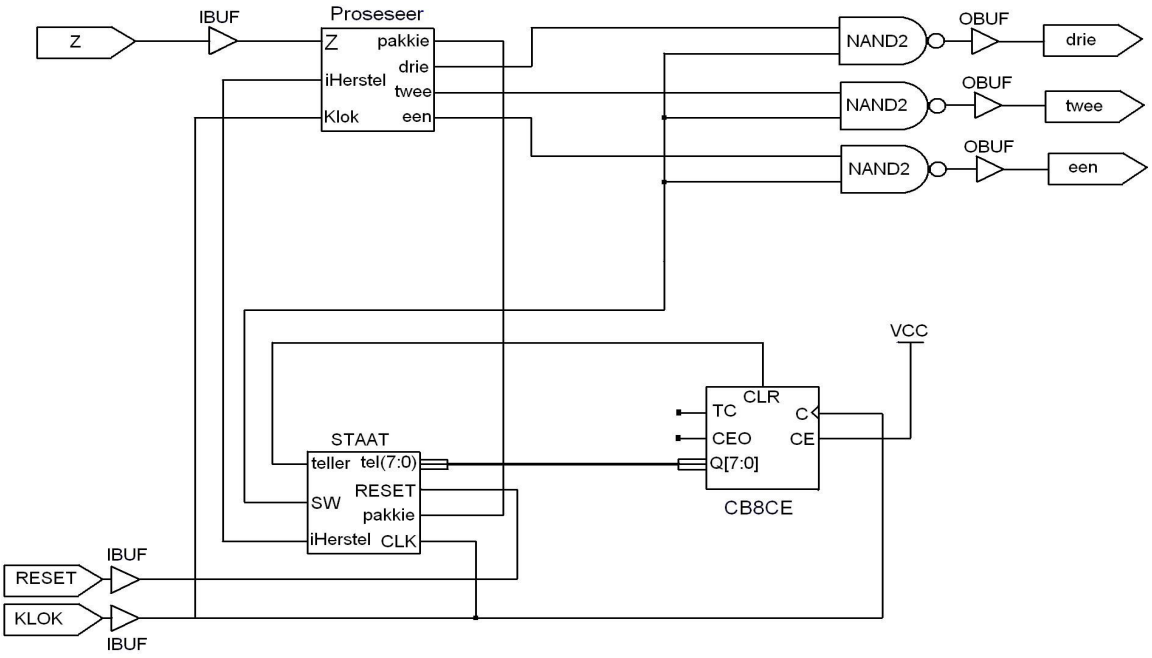

Figure B.1

Experiment 1a: The schematic diagram of the top-level design of the CPLD

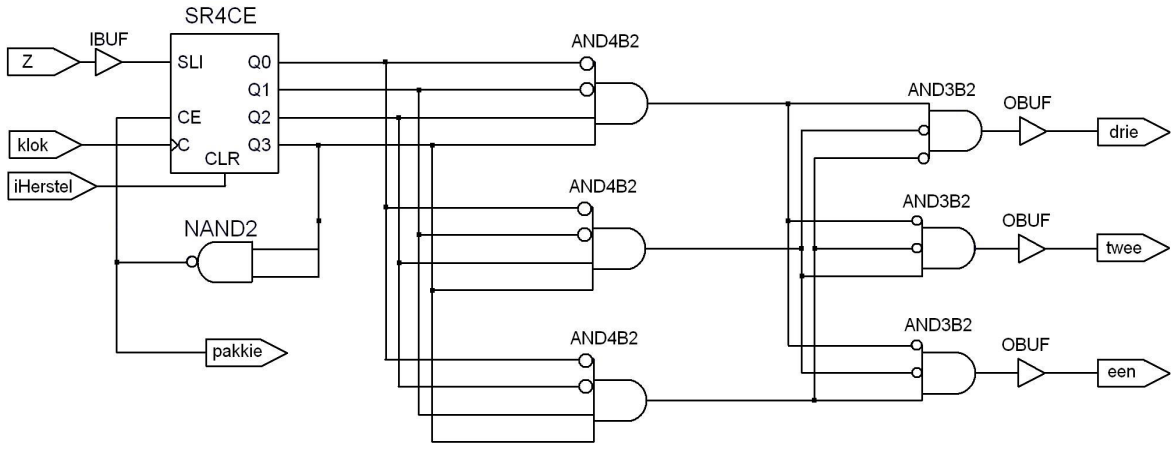

Figure B.2

Experiment 1a: The schematic diagram of the "Proseseer" part of the top-level design

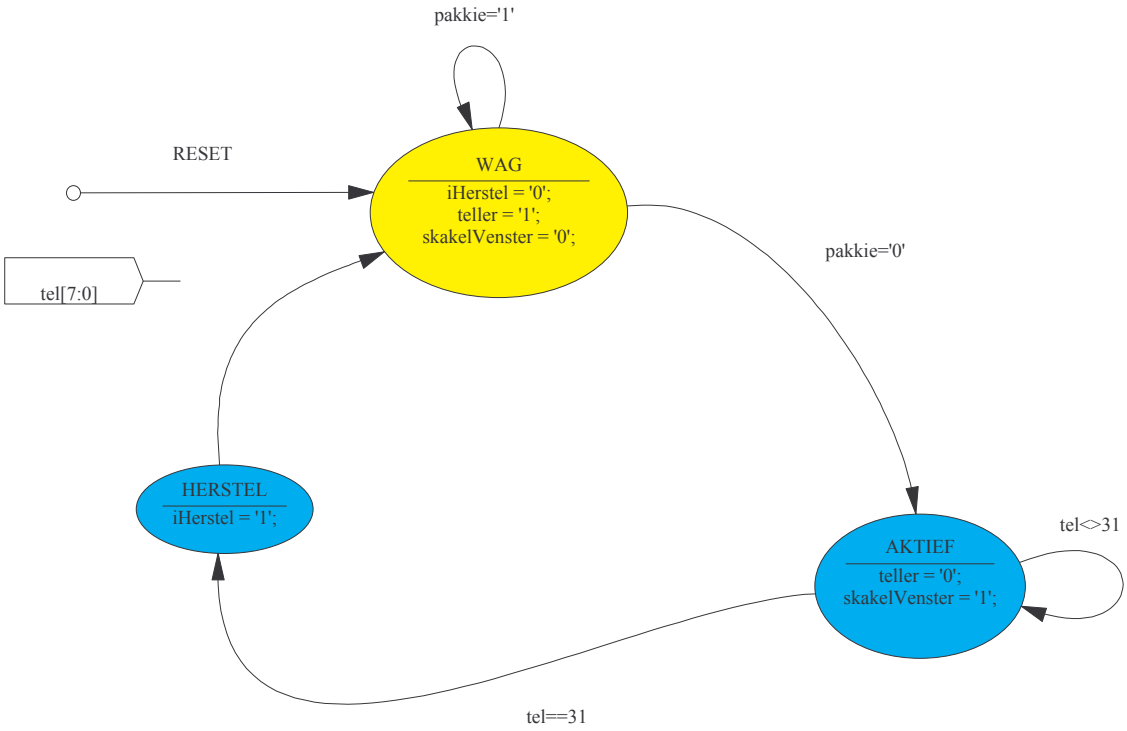

Figure B.3

Experiment 1a: The state diagram

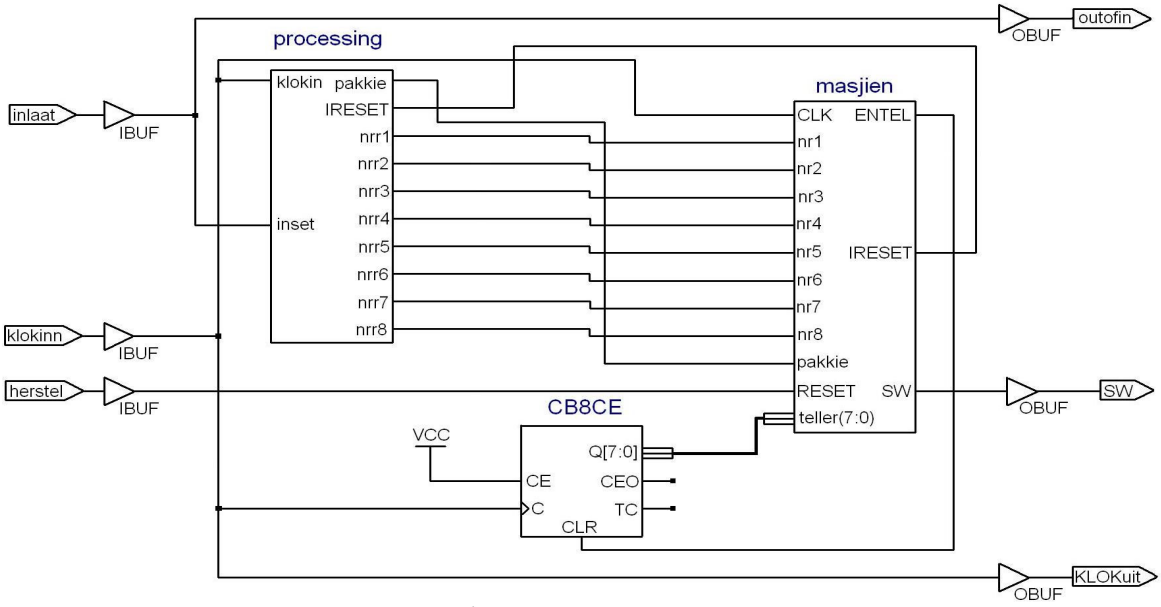

Figure B.4

Experiment 1b: The schematic diagram of the top level design of the CPLD

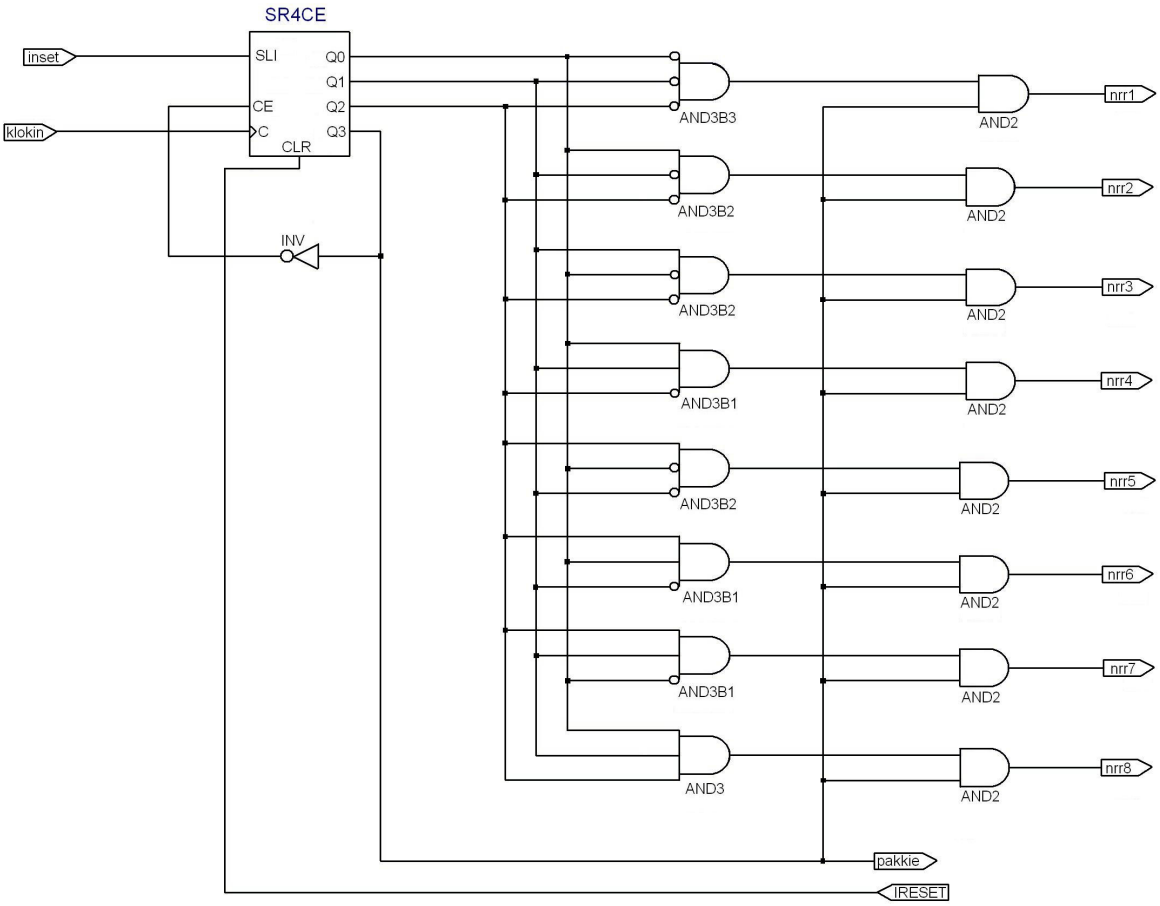

Figure B.5

Experiment 1b: The "Processing" component from the top level schematic design

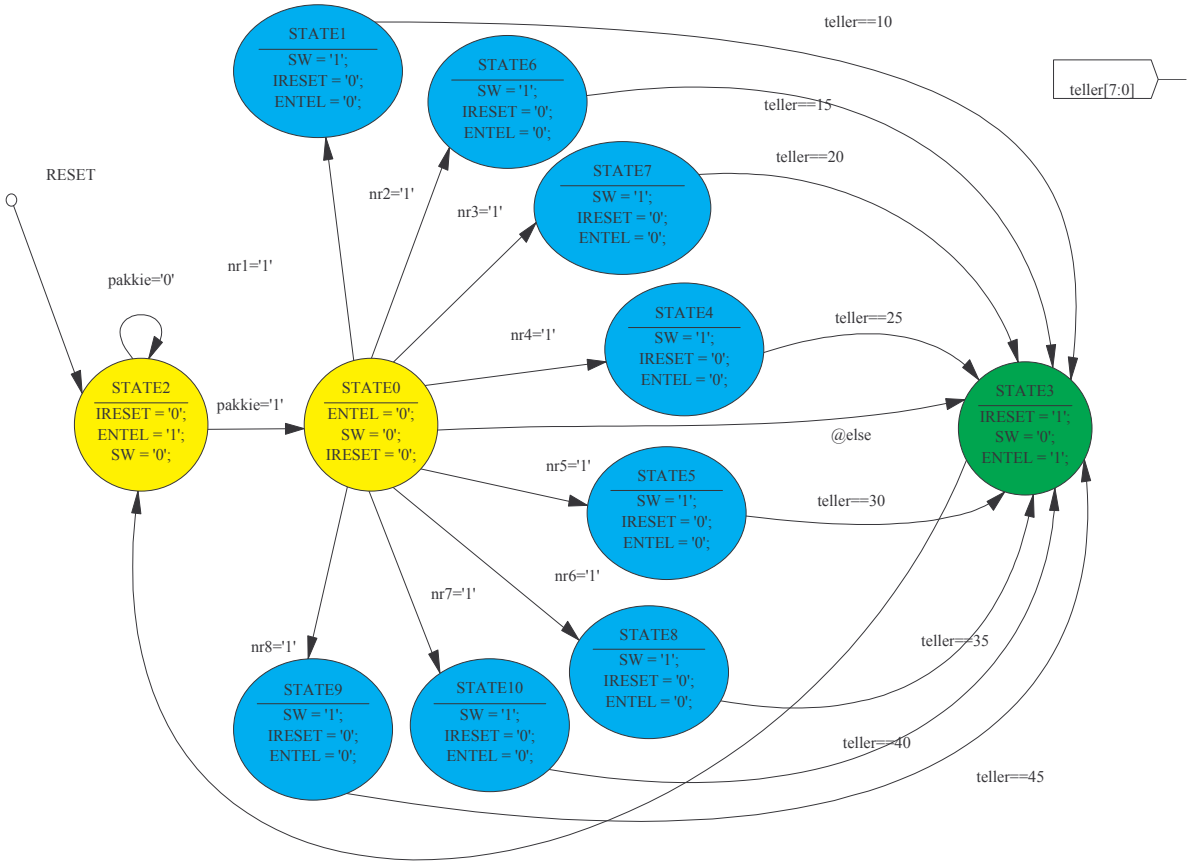

Figure B.6

Experiment 1b: The state diagram

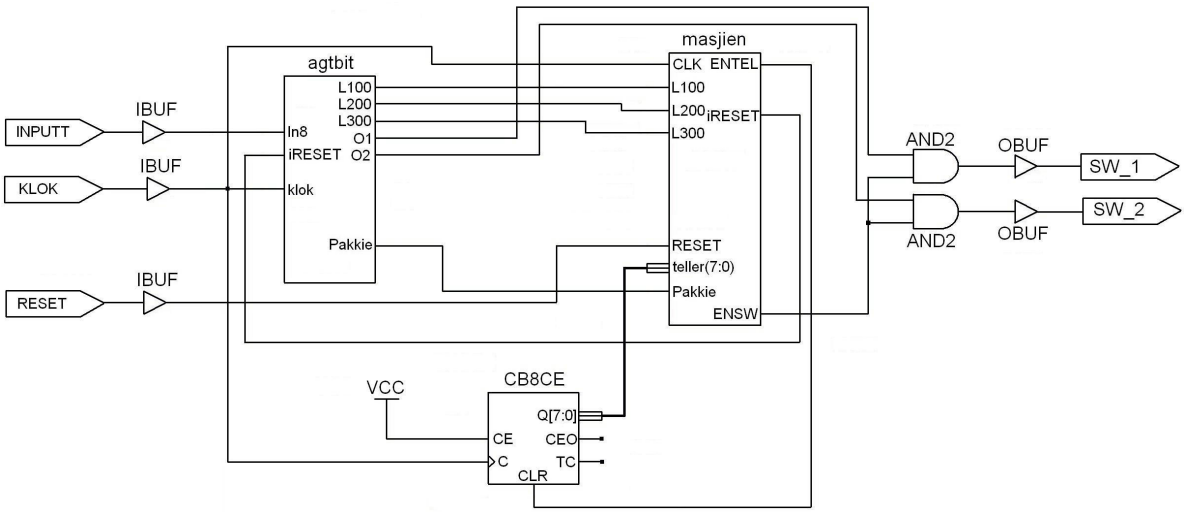

Figure B.7

Experiment 2: The schematic diagram of the top level design of the CPLD

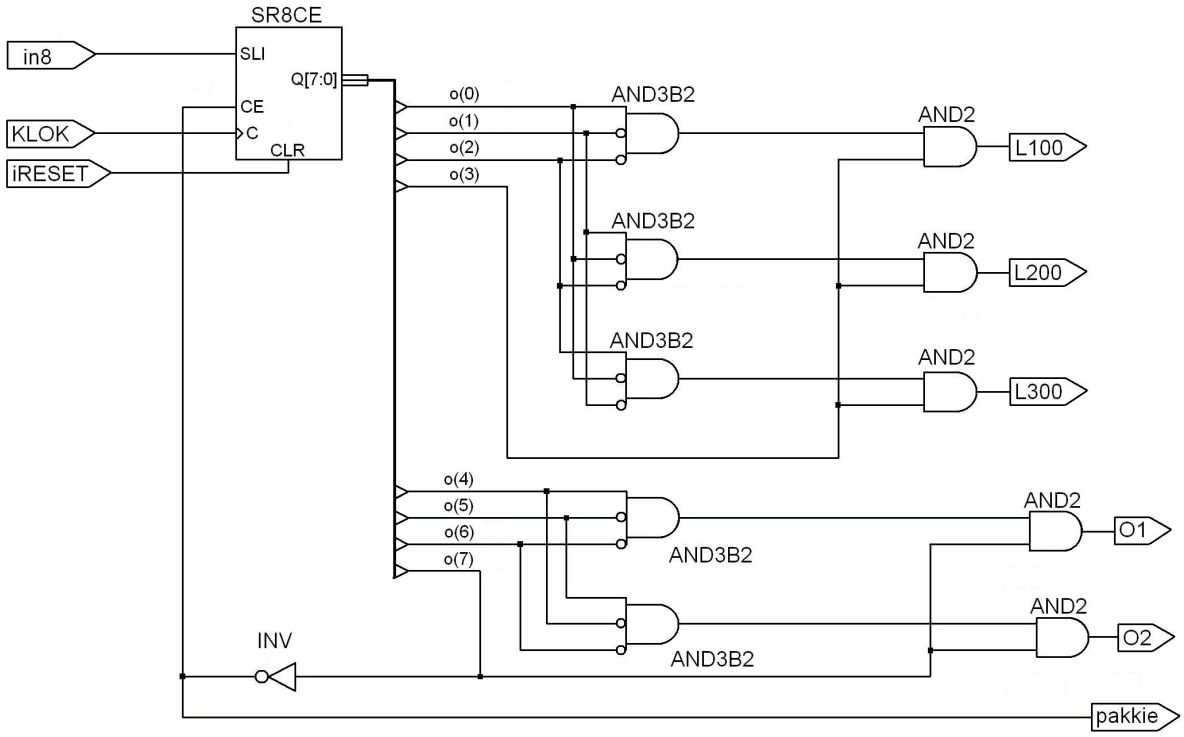

Figure B.8

Experiment 2: The "agtbit" component from the top-level schematic design.

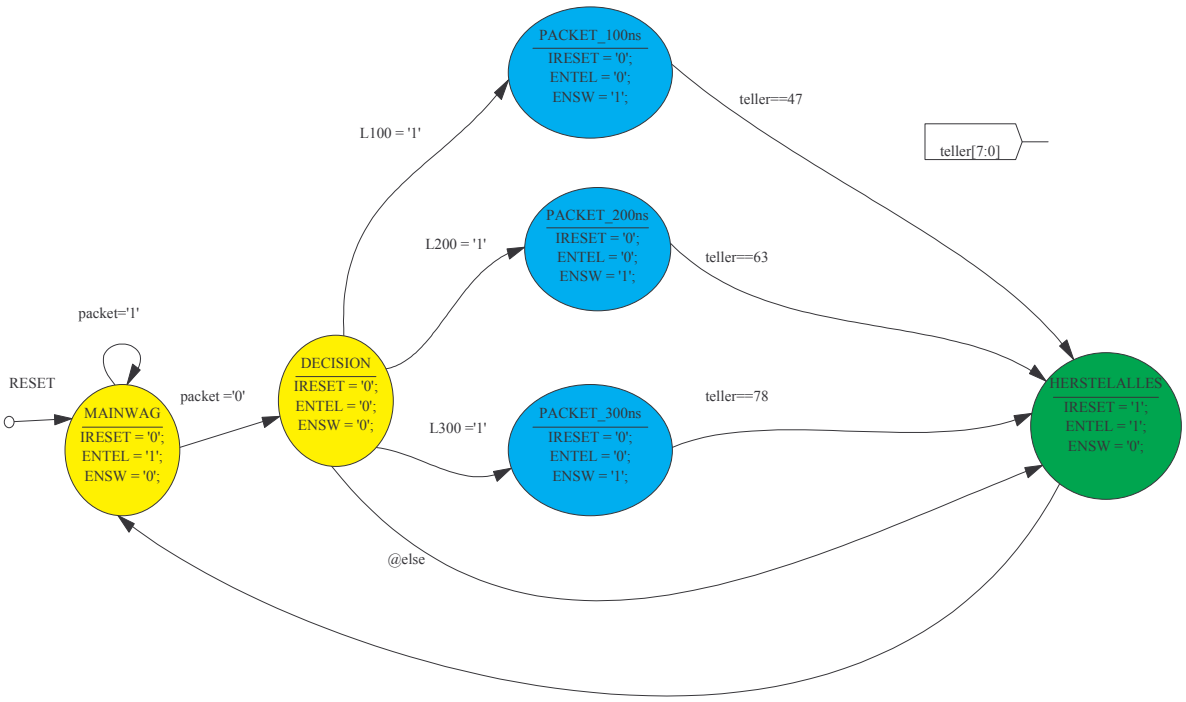

Figure B.9

Experiment 2: The state diagram

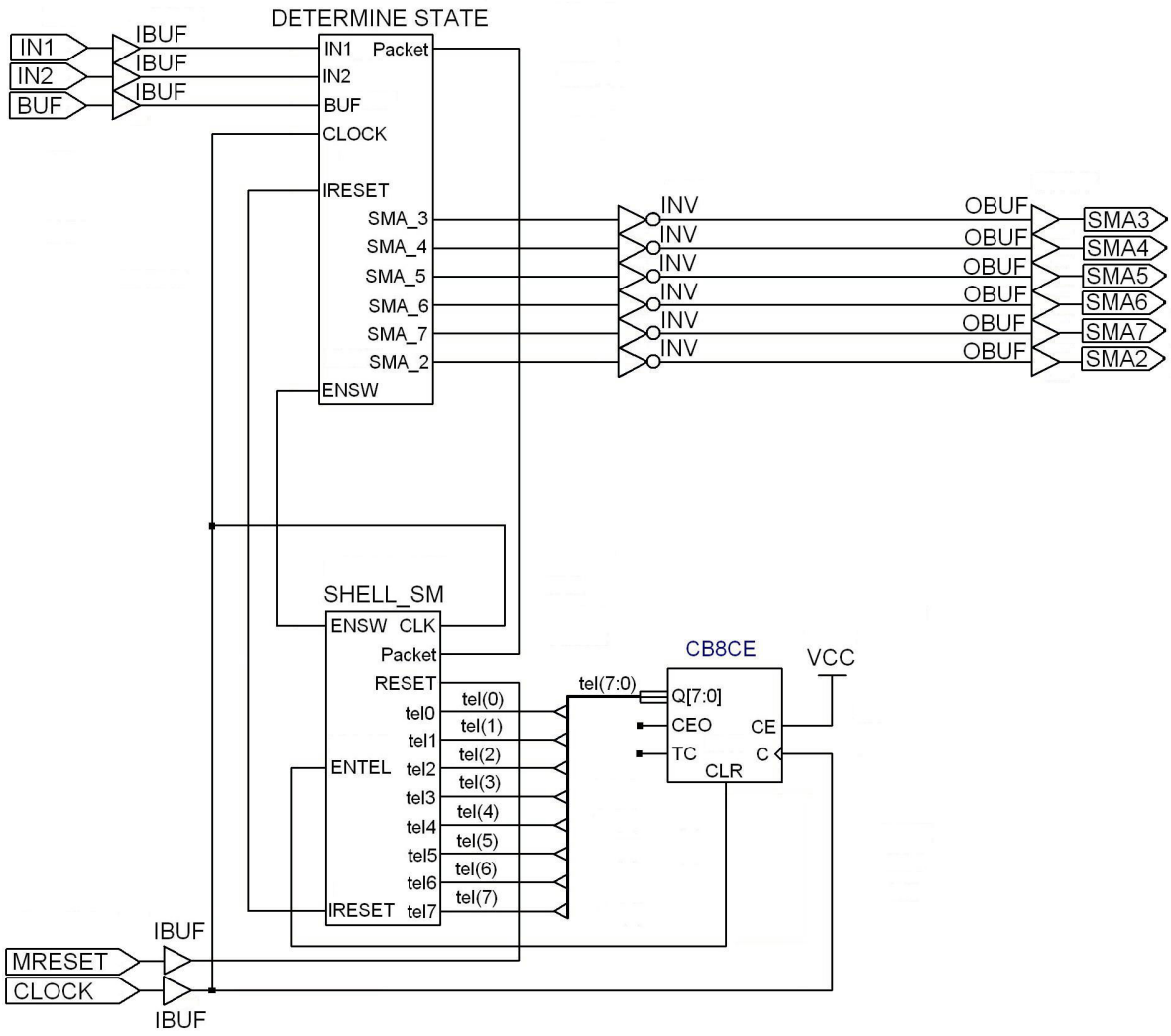

Figure B.10

Experiment 3: The schematic diagram of the top-level design of the CPLD

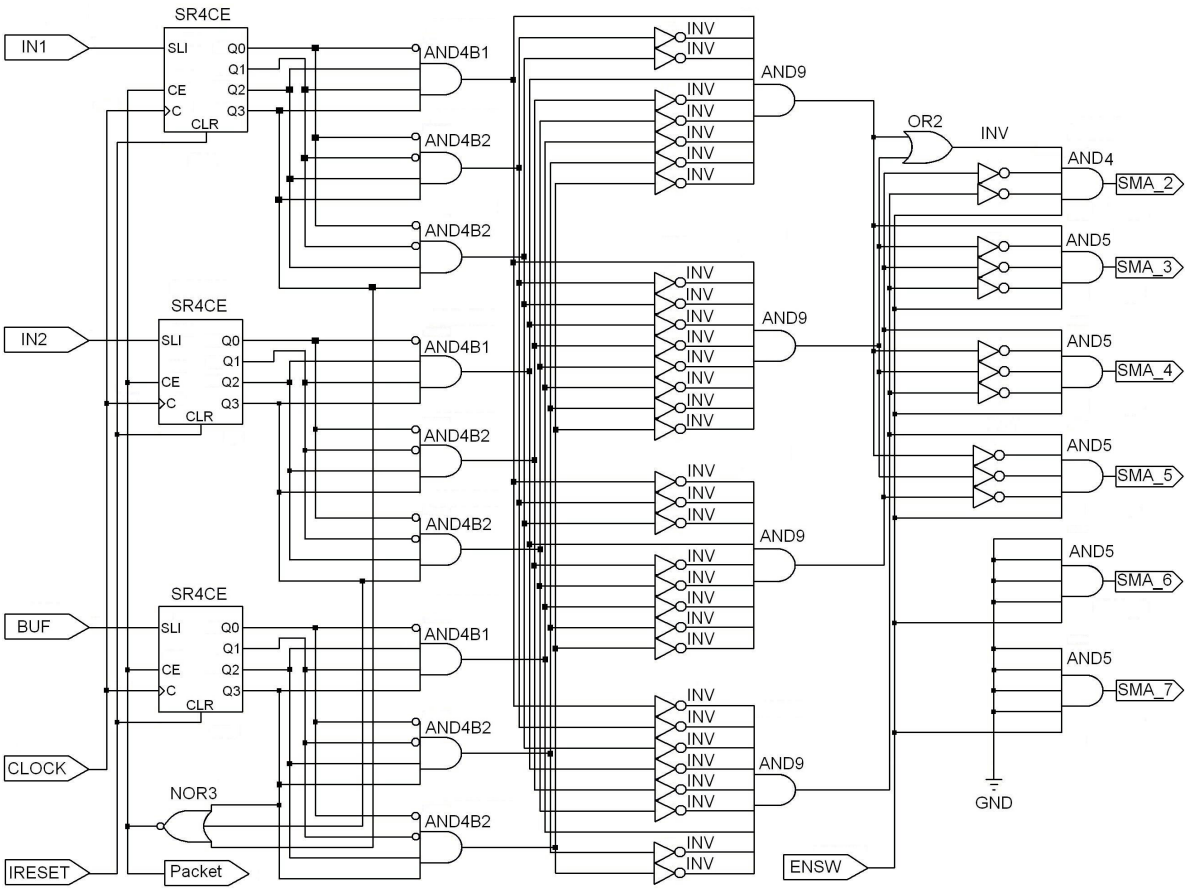

Figure B.11

Experiment 3: The "DETERMINE STATE" component from the top-level design

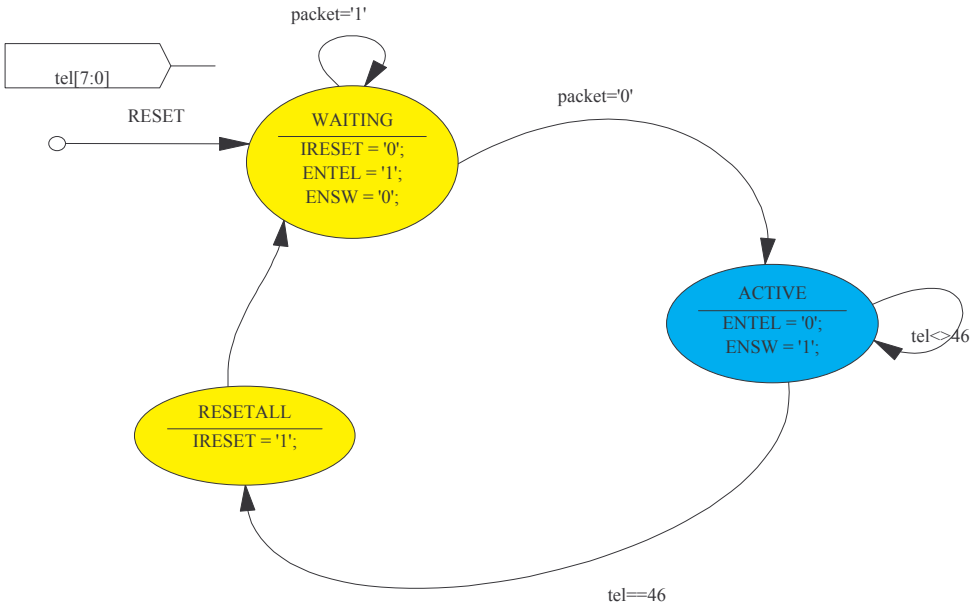

Figure B.12

Experiment 3: The state diagram

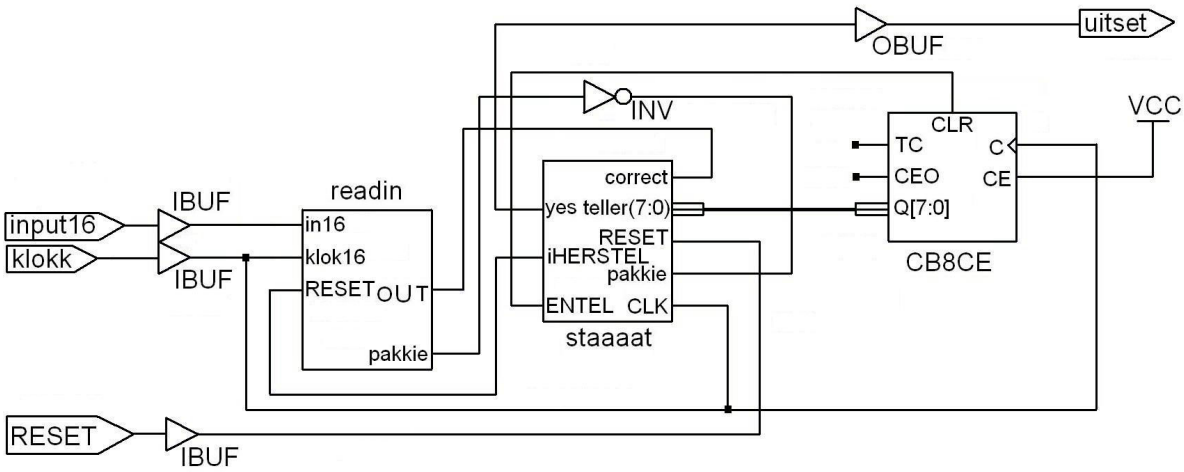

Figure B.13

Experiment 4: The schematic diagram of the top-level design of the CPLD

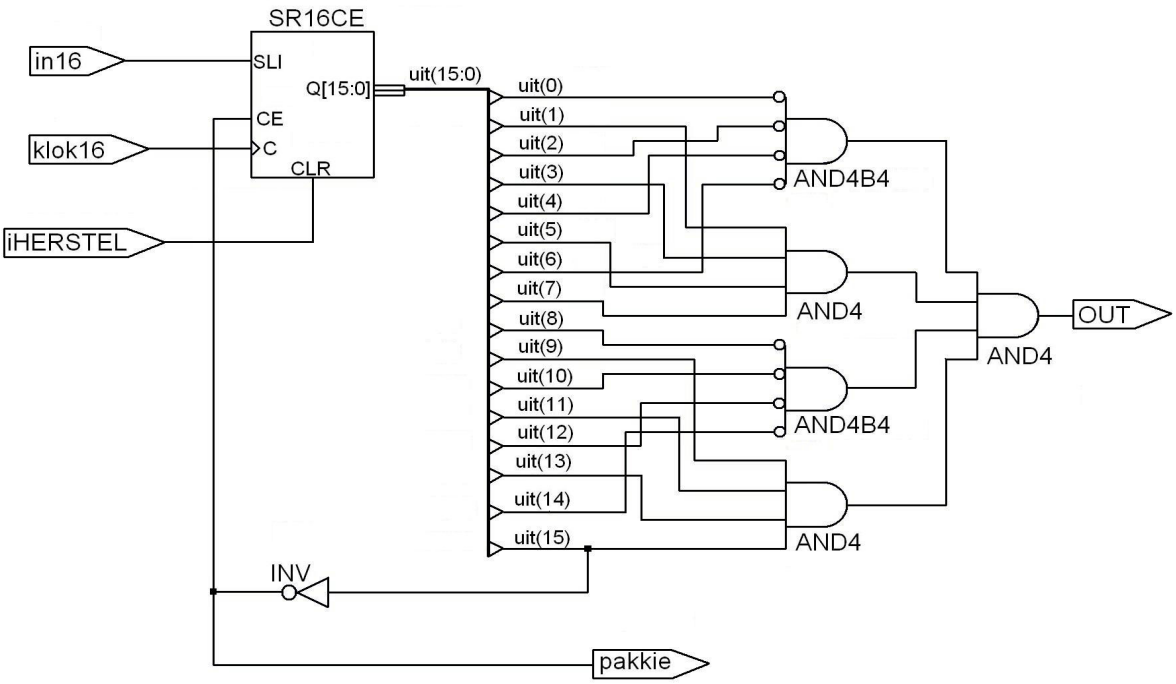

Figure B.14

Experiment 4: The "readin" component from the top level design

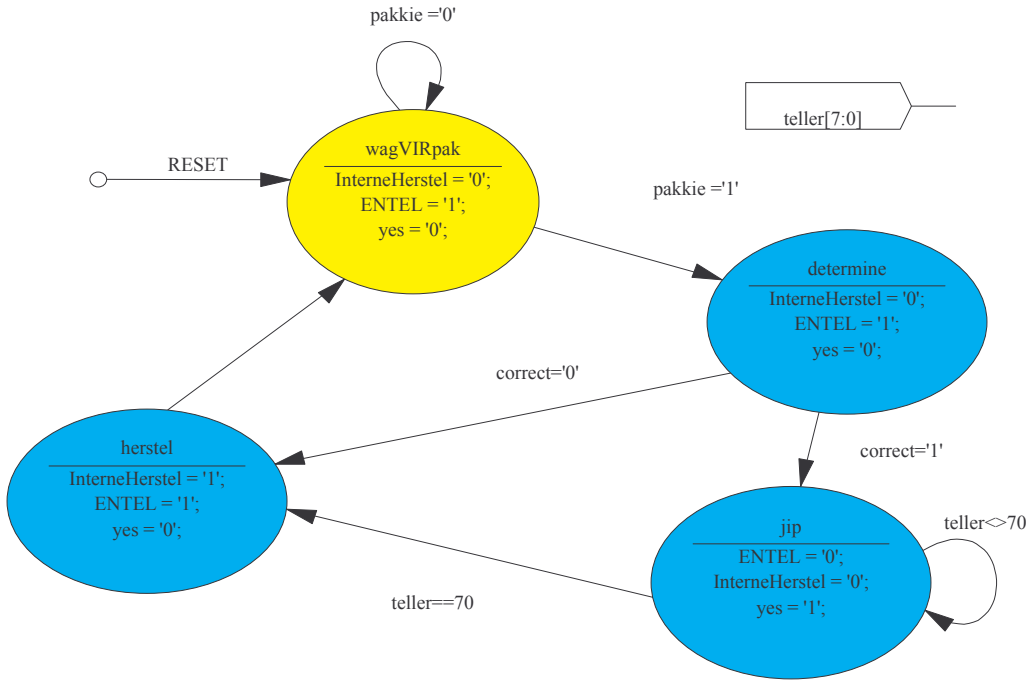

Figure B.15

Experiment 4: The state diagram