AN SRAM SYSTEM BASED ON A REDUCED-AREA FOUR-TRANSISTOR CMOS SRAM CELL

by

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ABSTRACT

Keywords: SRAM systems, reduced-area SRAM cell, SRAM static noise margins, threshold voltage reference, constant transconductance biasing, low-impedance driver, analogue design, clamped bit line latching current sense amplifier, current transporting circuit, asynchronous control.

The traditional method of implementing SRAM in CMOS is via a six-transistor cell and five routing lines. If the number of transistors and the number of wires could be reduced, the packing density of the memory cells could be increased, and the area reduced.

This document describes the design of an SRAM system based on a new four-transistor SRAM cell. The primary design goal was to create a functional system, so that the relationship between reduced cell area and a potentially reduced system area could be investigated.

A new write method and associated array structure has been used, and the design of the system parameters was accomplished using static noise margin theory. The power dissipation and percentage reduction in cell area have been improved over previous designs.

The circuits to achieve the access to the cell have been designed and simulated. These include low-impedance driver circuits, that allow the power supply of the cell's devices to be individually modified to read and write the cell, and a current sense amplifier system to convert the output current to a digital voltage. These circuits allow complete and accurate control to be achieved, but a price is paid for the complexity in terms of layout area. The SRAM system emulates a standard SRAM, and could therefore be used to replace current SRAM implementations.

The design was simulated on a system level, and found to operate correctly. Although it is outperformed by its six-transistor cell counterpart in terms of power dissipation, speed and layout area, the groundwork for defining further research and improving the characteristics of further designs has been laid.

UITTREKSEL

Sleutelwoorde: Statiese lees skryf geheue (SLSG) stelsels, verminderde-area SLSG sel, SLSG statiese ruisgrense, drempelspanningsverwysing, konstante transkonduktansie-voorspanning, lae-impedansie drywer, analoog ontwerp, geklampte bislyn gegrendelde stroom-monster versterker, stroom oordrag netwerk, asinkrone beheer.

Die tradisionele implementering van statiese geheue in CMOS geskied deur middel van 'n ses-transistor geheuesel wat vyf elektriese verbindings het. Indien die aantal transistors en lyne verminder kan word, sou dit moontlik wees om die pakkingsdigtheid van die geheueselle te verhoog en die oppervlakte te verklein.

Hierdie dokument beskryf die ontwerp van 'n stelsel wat op 'n nuwe vier-transistor sel gebaseer is. Die primêre ontwerpsdoel was om 'n funksionele stelsel te skep sodat die verband tussen verminderde seloppervlakte en 'n potensieël verminderde stelseloppervlakte ondersoek kon word.

'n Nuwe metode om die sel te skryf binne 'n raamwerk van 'n matriks-struktuur is gebruik, en die ontwerp van stelselparameters is deur middel van statiese ruisgrensanalise gedoen. Die drywingdissipasie en die persentasie vermindering in seloppervlakte is verbeter in vergelyking met vorige ontwerpe.

Stroombane wat nodig is om die sel te beheer is ontwerp en gesimuleer. Dit sluit lae-impedansie drywers in, wat toelaat dat die toevoerspanning van die sel se nodes onafhanklik varieër kan word vir die doeleindes van lees en skryf. 'n Stroomsensor is ook ontwerp om die uitsetstroom van die sel na 'n digitale spanning te verander. Hierdie stroombane laat korrekte en volledige beheer toe, maar die prys word in terme van oppervlakte betaal. Na buite lyk die stelsel soos enige standaard statiese geheue stelsel, en kan dus gebruik word om huidige implementerings te vervang.

Die ontwerp is op stelselvlak gesimuleer en funksioneer korrek. Dit kompeteer egter nie met 'n ekwivalente ses-transistor stelsel in terme van drywingdissipasie, spoed en oppervlakte nie. Dit het egter die beginsels vir opvolgende navorsing en 'n volgende ontwerpsiterasie gedefinieër.

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