# ACTIVE CONVERTER BASED ON THE VIENNA RECTIFIER TOPOLOGY INTERFACING A THREE-PHASE GENERATOR TO A DC-BUS

by

**Jacobus Hendrik Visser**

Submitted in partial fulfillment of the requirements for the degree
Master of Engineering (Electrical)
in the
Faculty of Engineering, the Built Environment and Information Technology
UNIVERSITY OF PRETORIA

March 2007

Active converter based on the VIENNA rectifier topology interfacing a three-phase generator to a DC-bus

by

Jacobus Hendrik Visser

Supervisor: prof. M.N. Gitau

Department: Electrical, Electronic and Computer Engineering

Degree: M.Eng. (Electrical)

## SUMMARY

AC-DC converters find application in every day life as a front-end to DC-DC and DC-AC converters. Active three-phase converters shape the three-phase input current to be sinusoidal and to be in-phase with the input voltage, as well as to provide a steady DC output voltage. This thesis investigates various active three-phase rectifier and control topologies and identifies a rectifier and control topology most suitable for use in converting a variable voltage variable frequency generator output to a DC voltage. In this dissertation, design relations are derived for determining the plant transfer response (for the suitable topology/controller), design equations are derived for designing/choosing the filter components, and guidelines are derived that will assist in choosing the right semi-conductor components and to give an estimation of expected system efficiency. The dissertation investigates the implementation of both analogue and digital control and provides implementation methodologies for both controllers. Expected results are verified by simulation and a build-up prototype.

It was shown that the VIENNA rectifier is able to convert a generator type input, with variable input voltage amplitude and variable frequency, to a constant DC-bus voltage whilst controlling the input current to be sinusoidal and in phase with the input voltage. The rectifier was able to maintain a constant DC voltage at the output for input voltages as low as half the rated input voltage and for an equivalent output power of half the rated output power.

This suggests that the VIENNA rectifier, controlled as a dual-boost rectifier, is suitable for applications that require power factor corrections and simultaneously operate from a wide input voltage range.

**Keywords:** VIENNA; rectifier; DC-voltage; generator; three-phase; constant frequency; analogue control; digital control; derating; modal analysis; Power Factor Correction.

Active converter based on the VIENNA rectifier topology interfacing a three-phase generator to a DC-bus

deur

Jacobus Hendrik Visser

Studieleier: prof. M.N. Gitau

Departement: Elektriese, Elektroniese en Rekenaar Ingenieurswese

Graad: M.Ing. (Elektries)

# OPSOMMING

Wisselspanning-na-gelykspanning gelykrigters word in toepassings gebruik as voor-reguleerders vir gelykspanning-na-gelykspanning omsetters asook gelykspanning-na-wisselspanning omsetters. Aktiewe drie-fase gelykrigters skakel die insetstroom om sinusodaal en in fase met die insetspanning te wees en terselfdertyd 'n konstante uitsetspanning te verskaf. Hierdie verhandeling ondersoek kwantitatief verskeie aktiewe drie-fase gelykrigters en identifiseer die gelykrigter mees geskik om 'n generator-tipe inset, wat wissel in beide spanning en frekwensie, om te skakel na 'n konstante uitsetspanning. In hierdie verhandeling word ontwerpsvergelykings afgelei wat die stelsel se frekwensie gedrag wiskundig sal beskryf, wat noodsaaklik is in die ontwerp van 'n geskikte beheerder vir die topologie. Ontwerpsvergelykings word ook afgelei vir die ontwerp van die inset-en-uitsetfilters en hulpriglyne word gestel waarvolgens halfgeleier komponente gekies kan word en waarvolgens omsetter-effektiwiteit geskat kan word. Die verhandeling ondersoek die gebruik van beide digitale en analoog beheerders en verskaf implementasie metodologië vir beide tipe beheerders. Verwagte resultate word geverifiëer deur van simulasies en 'n prototipe gebruik te maak.

In hierdie verhandeling word daar aangetoon dat die VIENNA gelykrigter 'n generator-tipe inset, wat wissel in beide spanningsamplitude en frekwensie, kan omskakel na 'n konstante gelykspanning en terselfdertyd die insetstroom beheer om sinusvormig en in fase te wees met die insetspanning. Die gelykrigter was ook instaat om 'n konstante gelykspanning te handhaaf vir insetspannings so laag as die helfte van die nominaal gespesifiseerde insetspanning en vir 'n ekwivalente uitsetdrywing van die helfte van die maksimum gespesifiseerde uitsetdrywing.

Dit dui dus daarop dat die VIENNA gelykrigter, beheer as 'n dubbel-opkap gelykrigter, geskik is vir toepassings wat arbeidsfaktorkorreksie vereis en terselfdertyd oor 'n wye insetspanningsbereik moet werk.

**Sleutelwoorde:** VIENNA; gelykspanning; generator; drie-fase; konstante frekwensie; analoog beheer; digitale beheer; model-analise; arbeidsfaktorkorreksie.

# TABLE OF CONTENTS

# NOMENCLATURE

| Symbol | Description | Unit |
|---|---|---|
| $\alpha$ | phase angle for a give phase, i.e. a | ° |
| $\eta$ | system efficiency | % |
| E | average mid-point capacitor voltage | V |
| $V_{LL}$ | line-to-line rms voltage, for a 3-phase source | V |
| $V_{LL,max,rms}$ | maximum line-to-line rms voltage, for a 3-phase source | V |
| $V_{phase,peak}$ | peak phase line-to-neutral voltage, for a 3-phase source | V |
| $V_{phase,rms}$ | rms phase line-to-neutral voltage, for a 3-phase source | V |
| $V_p$ | positive rail voltage, referenced to neutral | V |
| $V_n$ | negative rail voltage, referenced to neutral | V |
| $V_{ripple,p-p}$ | voltage ripple, peak-to-peak | V |
| $I_p$ | positive rail current | A |
| $I_n$ | negative rail current | A |
| $i_a$ | rms phase current for phase a | A |
| $i_{phase,rms}$ | rms phase current | A |
| $i_{phase,peak}$ | peak phase current | A |
| $T_{SW}$ | switching period | s |
| $I_{OUT}$ | average output current | A |
| $i_{ripple\_c}(t)$ | time varying ripple current through the output capacitor | A |

# CHAPTER 1

# INTRODUCTION

## 1.1 MOTIVATION

AC-DC converters find application in everyday-life as a front-end to DC-DC and DC-AC converters. In low power with low cost applications, the AC to DC conversion is very often merely a diode bridge rectifier with capacitor voltage filter. However, bridge rectification inherently draws non-sinusoidal current from the mains, which make it inadequate for high power applications due to the strict regulations on conducted EM (electromagnetic) energy, as well as the high current stress on components. For high power applications, the sinusoidal current must be actively shaped by using either a boost type front-end converter or by complex EM filtering at the input. Research and development of the latter has ceased mainly due to the cost and size associated with EM filters.

For medium power converters, a single-phase input is adequate and the front-end is usually a single-switch non-isolated boost topology that boosts the unregulated mains input to a voltage higher than the rectified line voltage. The switch is controlled in such a manner that the current drawn from the mains source is in phase with the mains voltage (effectively sinusoidal). The zero phase angle, between the mains voltage and the current, translates into a high power factor which, in turn, ensures that the source is not loaded reactively. For higher power outputs it is advantageous to use a three-phase input to lower the component stresses and to reduce component size (e.g. the filter capacitor). The three-phase active rectifier is based on the concept of the single-phase active rectifier and draws sinusoidal current from all three phases.

As wind generators as an energy source and electric vehicles as transportation medium becomes more popular, the need arises to efficiently convert the energy provided to a usable source and the same time conserve energy by reducing reactive power consumption. The interface developed as part of this dissertation will serve as a possible solution for fulfilling this need.

## 1.2 BACKGROUND

Controlled rectifiers are classified as being either isolated or non-isolated. For three-phase rectifiers, the non-isolated topologies are derived from the isolated topologies with the magnetic coupling (and thus isolation) achieved by the use of split inductors. However,

under most circumstances the large, low frequency output voltage ripple is intolerable for direct use. A DC-DC converter is usually used as second stage to the AC-DC converter and isolation is achieved in the second stage. For this reason it is unnecessary to use an isolated AC-DC front-end converter. Currently research is done on three topologies of three-phase active rectifiers. The first topology is a one quadrant, three-phase, single-switch, two-level converter. This topology shapes the input current using a single switch and the output is a single positive voltage. The second topology is a four quadrant, three-phase, six-switch, two-level converter with, as the operation implies, bi-directional current flow capability. Six switches are used to shape the input current and the output is also a single positive rail. The third topology is a one quadrant, three-phase, three-switch, three-level topology. Input current waveforms are controlled by three switches and the output is a positive split DC rail. The third topology mentioned is also known as the VIENNA rectifier and most of the current research focuses on this type of rectifier and variants.

## 1.3 PROBLEM STATEMENT

The objective of this research is to develop an interface between a three-phase AC generator operating at variable speed (e.g. wind generators, microhydro generators) and a constant voltage DC-bus. The interface is required to ensure high energy efficiency by reducing reactive power consumption, as well as maintaining a constant DC-bus voltage. The rectifier must thus ensure that a power factor of close to 1 is achieved at the source input. This implies that the input current is both sinusoidal and in-phase with the input voltage, assuming that the input voltage is also sinusoidal. The interface is to be based on the VIENNA rectifier.

## 1.4 CONTRIBUTION

The major contribution made by this research is the development of an interface between variable speed three-phase generators and a DC-bus. This type of interface has uses in wind generation systems employing AC generators and also in the proposed electrical power systems in automobiles. The research for this dissertation also adds mathematical control and plant models to current literature base available and enables the determination of performance characteristics of VIENNA based rectifier topologies. Furthermore the

research performed for this dissertation enables the design of an equivalent three-phase active rectifier, with the inputs and outputs to the system given.

## 1.5 THESIS APPROACH

The steps undertaken during the thesis are shown in flowchart form in figure 1.1.

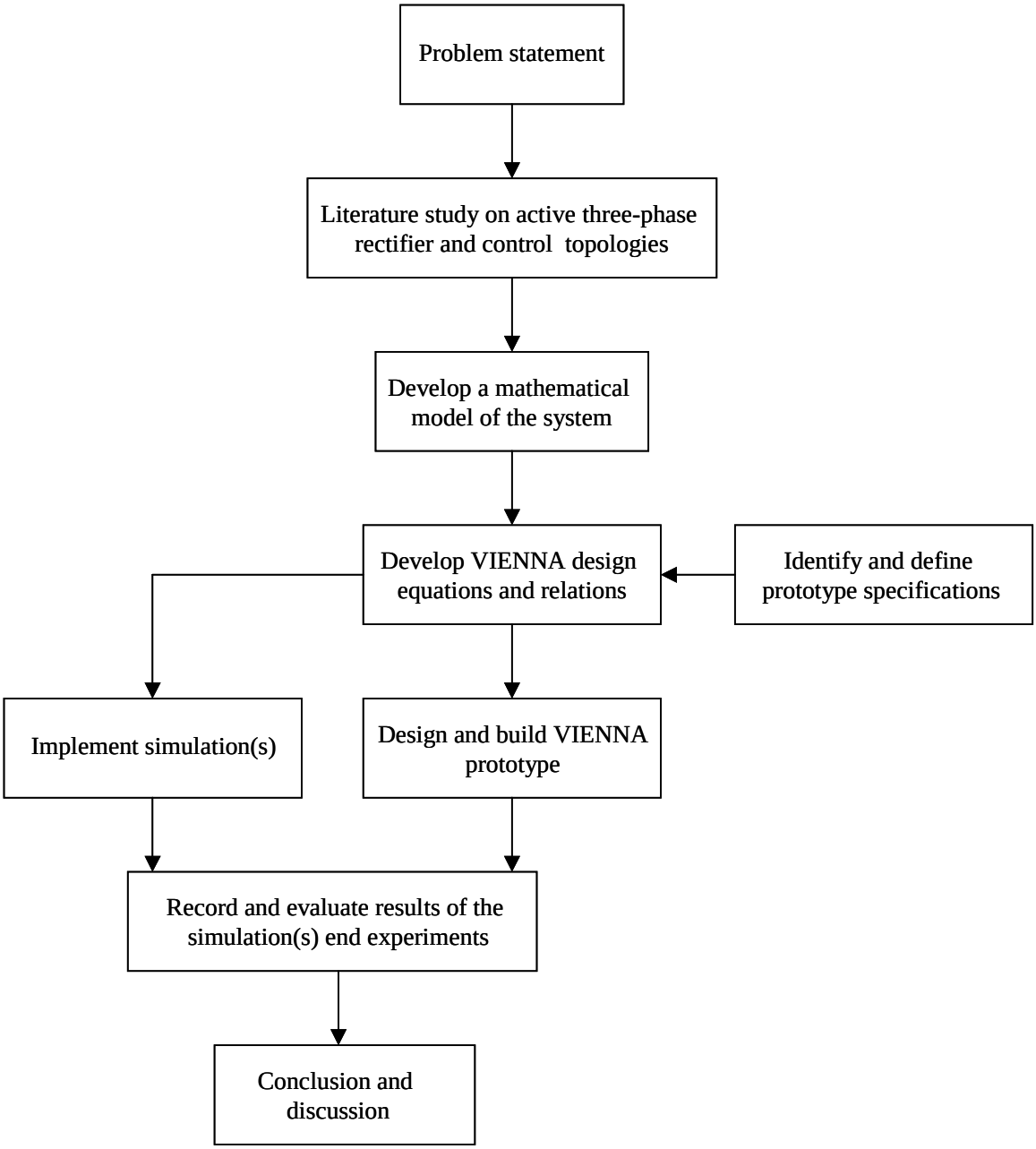



**Figure 1.1.** Steps that were followed during the dissertation.

The first step of research is to identify and define the research problem, and also to define the specific research goals. The problem statement in section 1.3 is the result of this first step and provides the specific research goals as well.

The literature study is performed to gain insight into active three-phase rectifier operation, and also to study the various topologies available. The model derived for the VIENNA rectifier is based on a control implementation and therefore the various control strategies

available for the control of three-phase rectifiers are also discussed. The literature study is restricted to non-isolated boost-type topologies.

The rectifier and control topologies are modelled and characterized in mathematical terms. The mathematical model provides the basis for controller design. The model derived is as an accurate model as possible.

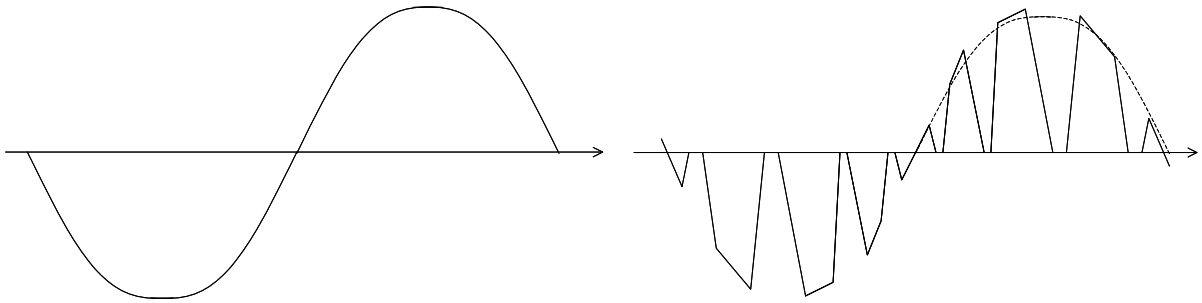
The next steps involve the design of the VIENNA rectifier. Equations are derived for the design of the filter components and guidelines are established whereby the inductors, capacitors and semi-conductor components must adhere to. The evaluation criteria are also established: The results of the simulations and experimental prototype will be evaluated against the specifications set to determine the accuracy of the model and also the various design equations.

Following the design and modelling of the VIENNA rectifier is the build and testing of an experimental prototype. The results of the simulations and experiments are recorded and compared to the evaluation criteria. Comparisons and deviations from the evaluation criteria are discussed and commented upon, and from this it can be decided if the VIENNA rectifier meets the required operational capability.

## 1.6 LIMITATIONS OF THE RESEARCH

The following limitations apply to experimental prototype and the research performed in general:

- The model derived for the VIENNA rectifier is only valid for continuous current at the input, for instance as shown in figure 1.2;
- The rectifier is designed to strictly drive a linear load only – no provision is made on the experimental prototype to drive non-linear loads such as DC-DC converters;
- and, Testing of the rectifier is performed under laboratory conditions and no attempt is made to control the temperature, humidity and/or pressure.



(a) Continuous current (b) Discontinuous current

**Figure 1.2.** Comparison between continuous and discontinuous current.

## 1.7 THESIS OVERVIEW

Chapter 2 is a literature study on active three-phase rectifiers. The literature study investigates the advantages and disadvantages of various rectifier topologies, specifically compared to the VIENNA rectifier. The focus of the literature study is to compare system performance versus complexity of the various topologies. Issues to be discussed include controller complexity, size of the filter components, output bus voltage ripple, input current distortion, switching frequency, boost ratio and efficiency of the various topologies. The latter will be used to identify the most suitable VIENNA rectifier based topology for converting a generator type input to a constant DC-bus voltage.

In Chapter 3, a modal analysis is performed on the VIENNA rectifier, thus obtaining a small-signal frequency response model of the rectifier. The small-signal model is used in controller compensator design to stabilize the system.

Chapter 4 and Chapter 5 cover basic converter design practices and include filter design, compensator design, component electrical stress analysis, component selection and system efficiency calculations.

Chapter 6 is a summary of simulation results and tests performed on an experimental prototype. All results are discussed and analyzed in detail and any deviation from the expected result is discussed.

The conclusion of this thesis is covered in Chapter 7 and is remarked upon.

Simulation models, photographs of the experimental prototype, MATLAB scripts and prototype schematics are attached in the Appendices for reference purposes.

# CHAPTER 2

# LITERATURE STUDY ON ACTIVE THREE-PHASE RECTIFIERS

## 2.1 INTRODUCTION

The objective of this research is to develop an interface between a three-phase AC generator operating at variable speed and a constant voltage DC-bus. The interface is required to ensure high energy efficiency by reducing reactive power consumption, as well as maintain a constant DC-bus voltage.

Various active three-phase rectifier topologies and control techniques are discussed in this Chapter. The various advantages and disadvantages of the different converter topologies and control techniques are compared, to identify the most suitable topology for converting a three-phase input, from a generator type input (variable input voltage/variable frequency), to a constant DC voltage output. It is self evident that a boost topology must be used instead of a buck topology [1] because of the nature of the three-phase input that will be low when the generator rotational speed is low. In addition, since voltage isolation can be achieved in DC-DC converters it implies that the three-phase rectifier front-end can be non-isolated. Since a generated input is converted to a DC output and not *vice versa* where a DC source drives a motor, only unidirectional converters are considered for implementation [1].

The aim of this literature study is to establish the current status of active three-phase rectifiers. The focus of the literature study will be to compare system performance versus complexity of the various topologies. Issues to be discussed include controller complexity, size of the filter components, output bus voltage ripple, input current distortion, switching frequency, output bus voltage and efficiency of the various topologies.

A laboratory prototype of the most suitable rectifier, for converting a three-phase AC generator input to a constant DC-bus voltage, shall be designed, built and tested. The testing of the system includes various measurements to determine and verify the performance of the experimental system.

## 2.2 TWO-LEVEL OUTPUT CONVERTERS

### 2.2.1 Unidirectional single-switch discontinuous-mode boost rectifier

The unidirectional single-switch discontinuous-mode boost rectifier is shown in figure 2.1.

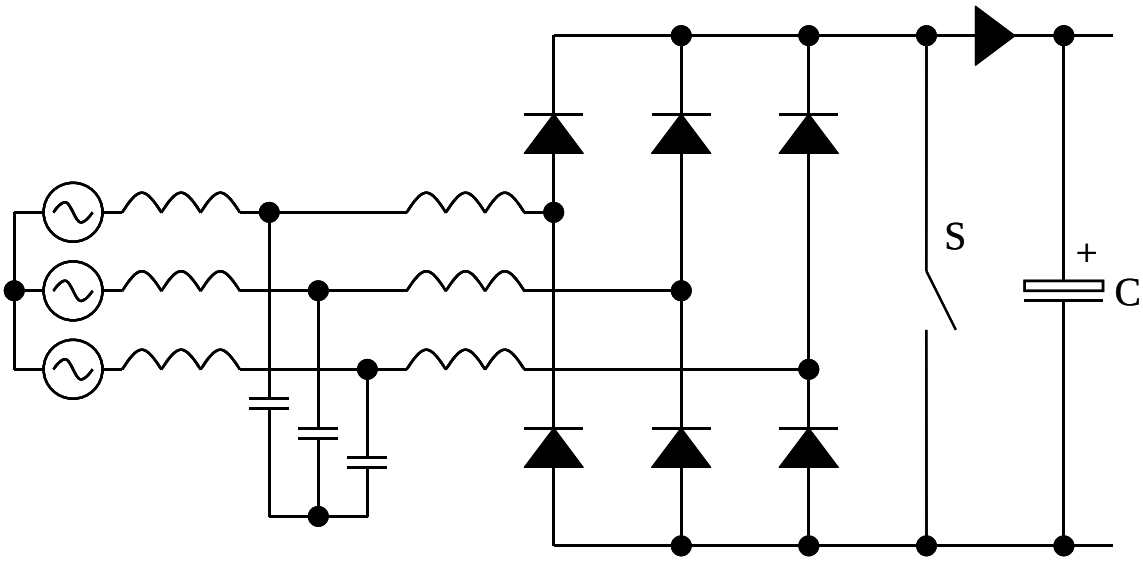



**Figure 2.1.** Unidirectional Single-Switch Boost Rectifier [2].

For this rectifier the single switch is closed to charge the input inductors. When the switch is released the energy from the input inductors is transferred to the output capacitor. Since only two of the diodes in the diode bridge can conduct at any given time, a discontinuous current at the input results [2]. An additional LC-type filter is required at the input for EMI requirements, due to the discontinuous nature of the input line current [3]. This three-phase rectifier is a development of the three-phase diode bridge with step-up converter (shown in figure 2.2). The main advantages of the DC inductor rectifier over the AC inductor rectifier is the single inductive element required (as can be seen in figure 2.1), as well as the lesser output capacitor current stress [2]. The input current, however, is highly discontinuous (again mainly due to fact that only two diodes conduct) [2]. Since there is no reactive filtering on the input, the input current will be zero for 60° blocks. Thus no filtering can be added to the input to smooth out the input current. The total harmonic distortion of the unidirectional single-switch discontinuous-mode boost rectifier will be less than that from a three-phase diode bridge with step-up converter, as can be expected, but inferior to other three-phase rectifier topologies [2, 4]. Low component count and low control effort [2] renders these rectifiers suitable for low power applications [1].

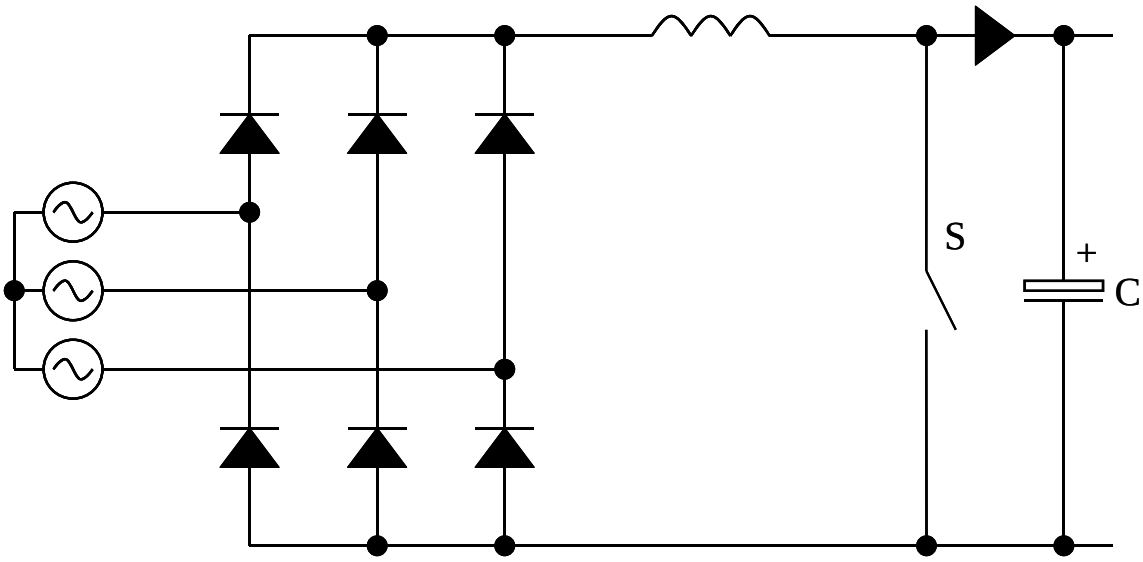



**Figure 2.2.** Unidirectional Single-Switch Boost Rectifier, DC-side filtering [5].

An added advantage of this topology over multi-level rectifier topologies is the ability to boost to a voltage almost equal to rectified input, or $1.414V_{LL}$ [6].

The unidirectional single-switch boost rectifier, with DC-side filtering, shown in figure 2.2, has high line current total harmonic distortion of approximately 32% [2, 7]. In comparison the AC-side filtered version, shown in figure 2.1, has line current distortion of approximately 20% [2].

### 2.2.2 Three-switch boost rectifiers

A three-switch continuous conduction topology for a three-phase active rectifier is presented by [8]. Figure 2.3 shows a delta-connected three-switch configuration. The star-connected switch configuration is shown in figure 2.4.

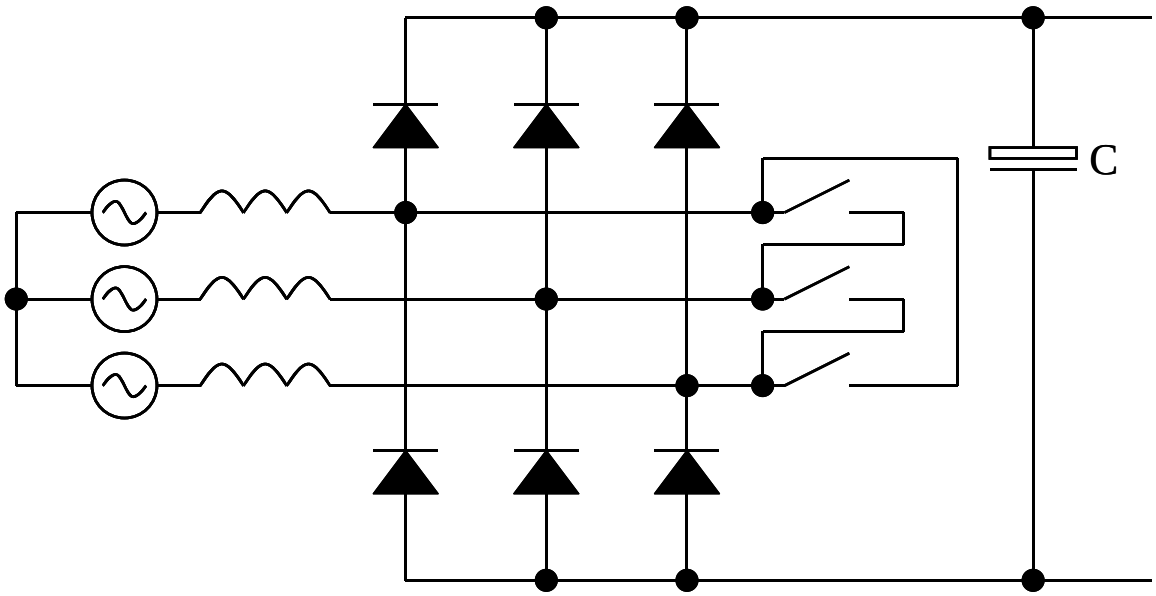



**Figure 2.3.** Three-phase delta-connected three-switch rectifier [5].

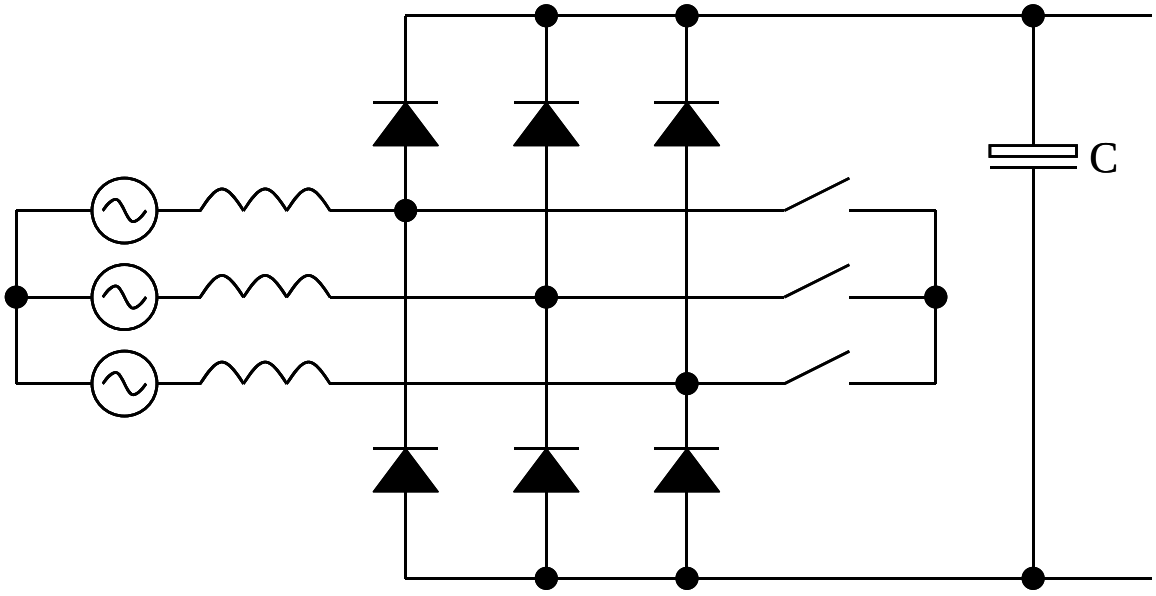



**Figure 2.4.** Three-phase star-connected three-switch rectifier [5].

The main advantage of this topology over the topologies mentioned in section 2.1 is the continuous nature of the input current and, thus, the absence of the input LC-filter. The control-effort, however, is considerably higher than that required for the previous rectifier since three-switches require isolated gate drives as can be seen in figures 2.3 and 2.4. However, as shown by [8], the rectifier can be controlled with a constant switching frequency without requiring a multiplier (as is required by the previously mentioned rectifier for forcing the current to be sinusoidal). For both switch-configurations, the switch voltage stress will be the same as for the unidirectional single-switch discontinuous-mode

boost rectifier but, since the three-switch topology operates in continuous-conduction mode, the switch current stress will be less.

The difference between the two switch configurations is that the star-connected topology will have higher conduction losses than an equivalent power rated delta-connected topology, but lower switching losses [1]. The star-connected topology also has the option of driving a three-level output [1], transforming it into the VIENNA rectifier.

Control effort for these topologies will be the same as for the other three-switch rectifier topologies, but considerably less than an H-bridge. An advantage of this topology is the ability to boost to a voltage almost equal to rectified input, or $1.35V_{LL}$ [1], whereas the multi-level rectifier topologies (i.e. three-level converter topologies) need to boost to an output voltage considerably higher [1]. Due to the continuous nature of the input current the ripple current stress on the output capacitor will be less than the single-switch boost rectifier and comparable to the H-bridge rectifier [2].

[8] indicates that these rectifiers can be controlled with a constant switching frequency.

The greatest disadvantage of this type of topology, as well as many other multi-switch topologies, is the number of diodes required [2]. The main reason for the high number of diodes is the realization of the bi-directional switches, which requires four diodes per switch. Figure 2.5 shows a typical implementation for bi-directional switching [9].

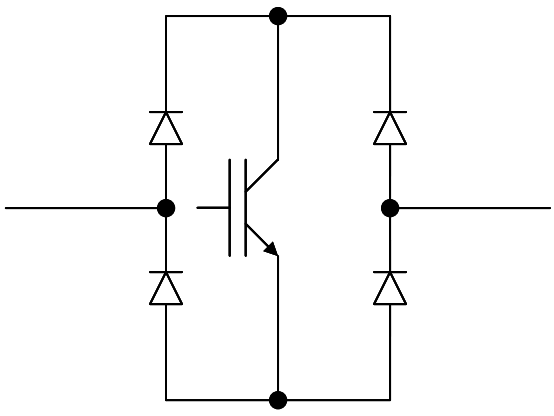


**Figure 2.5.** Implementation for a Unidirectional switch [9].

[8] also presents what is referred to as a 3-phase boost rectifier with an inverter network. This rectifier is shown in figure 2.6. Although this rectifier features six control switches, it

can be seen that it is in fact a combination of the star-connected and delta-connected switch configurations. It offers the same performance as the topologies mentioned above [1], but at the expense of a higher component count and higher control effort.

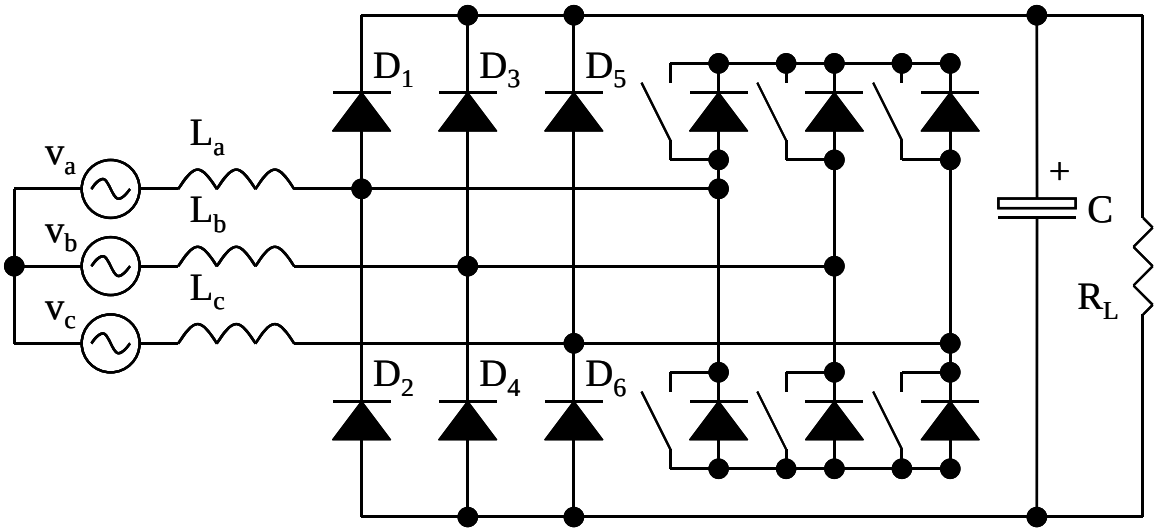



**Figure 2.6.** 3-phase boost rectifier with an inverter network [8].

[8] indicates an achievable total harmonic distortion (THD) of 6.1% for the delta connected three-switch rectifier, as shown in figure 2.3. [7] indicates similar THD performance for the delta- and star-connected three-switch rectifier topologies and thus it is a valid assumption that the THD of the input line-current for the star-connected topology will be close to 6.1%. [7] only states that the THD for the topology shown in figure 2.6 (3-phase boost rectifier with an inverter network) is low.

### 2.2.3 H-bridge boost rectifier

A three-phase H-bridge topology is shown in figure 2.7. It can be seen in figure 2.7 that, by adding the diode to the DC rail, the rectifier power flow will be in one direction only. Thus the operation will then be unidirectional only.

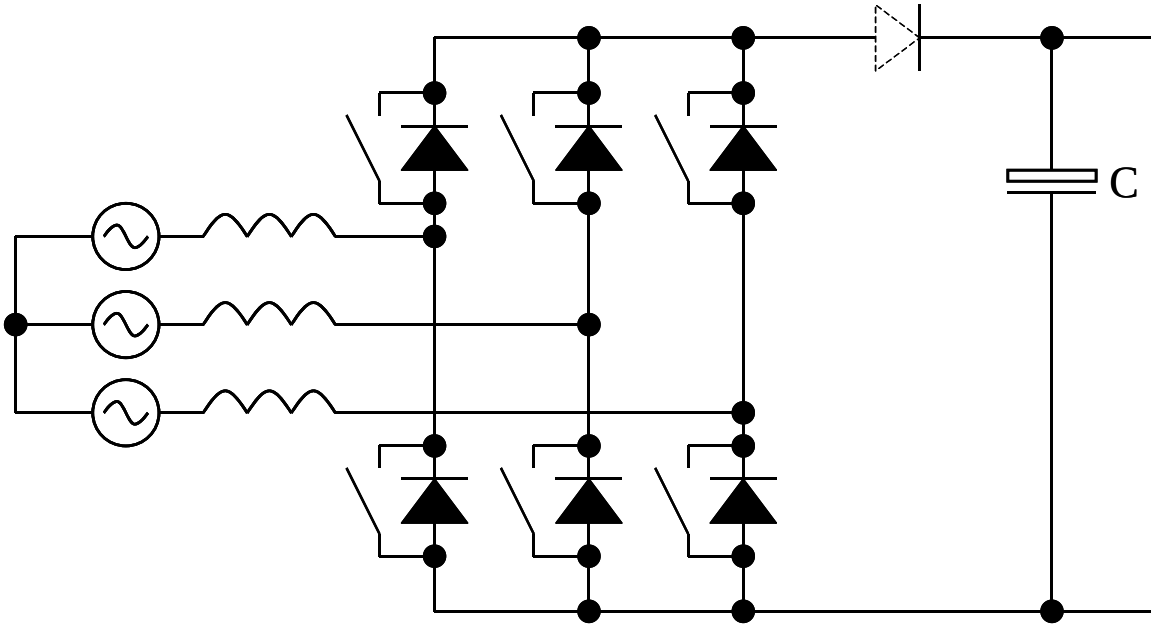



**Figure 2.7.** Unidirectional H-bridge converter [8].

The control effort and complexity for the H-bridge is considerably greater than for the previous topologies discussed [2]. [2] states that the input current can be shaped to be sinusoidal by the pulsing of only two bridge legs, effectively transforming the H-bridge rectifier into a two-switch high-frequency rectifier. (Operation of the H-bridge is the same as for the three-switch topologies)

The main disadvantage of this rectifier compared to the three-switch and single-switch topologies is higher transistor losses [2], high switch electrical stresses [1] and low reliability factors [1]. The diode conduction losses are, however, lower compared to three-switch and single-switch rectifiers [2]. An advantage, compared to three-level rectifiers, is that the minimum boost voltage is $1.35V_{LL}$ [1]. Output capacitor ripple current stress is almost the same for the H-bridge and the three-switch variants. This topology can be controlled with a constant switching frequency [27].

[2] states an approximate achievable THD for the line current of 8.2%, for the H-bridge rectifier.

### 2.2.4 Series-connected dual-boost converters

[5, 10] presents a dual boost topology that employs two high frequency (PWM) switches to shape the input current, as shown in figure 2.8. [5] also presents a variation on this topology with the DC-Link diode omitted, as shown in figure 2.9.

The series-connected dual boost converter (figure 2.8) features low current stress for all of the switches, as well as overall low electrical stresses and zero-voltage switching for the bi-directional switches. The minimum output voltage is $1.5V_{LL}$ [5]. The switching frequency for the bi-directional switches is double that of the line frequency [5]. [10] indicates that this topology can be controlled with a constant switching frequency.

The inverter-leg version, shown in figure 2.9, offers a minimum achievable output voltage of $1.35V_{LL}$, whilst also offering lower electrical losses and on-state losses than the topology shown in figure 2.8 [5].

Control effort of these rectifier topologies are considerably greater than that of the single switch and three-switch rectifier topologies, because of the high number of isolated gate drives required. As can be seen from figure 2.8 and figure 2.9, all switches except one require an isolated gate drive. This makes the implementation of this topology more difficult than all of the other topologies mentioned above including the H-bridge that only require isolated gate-drives for three switches.

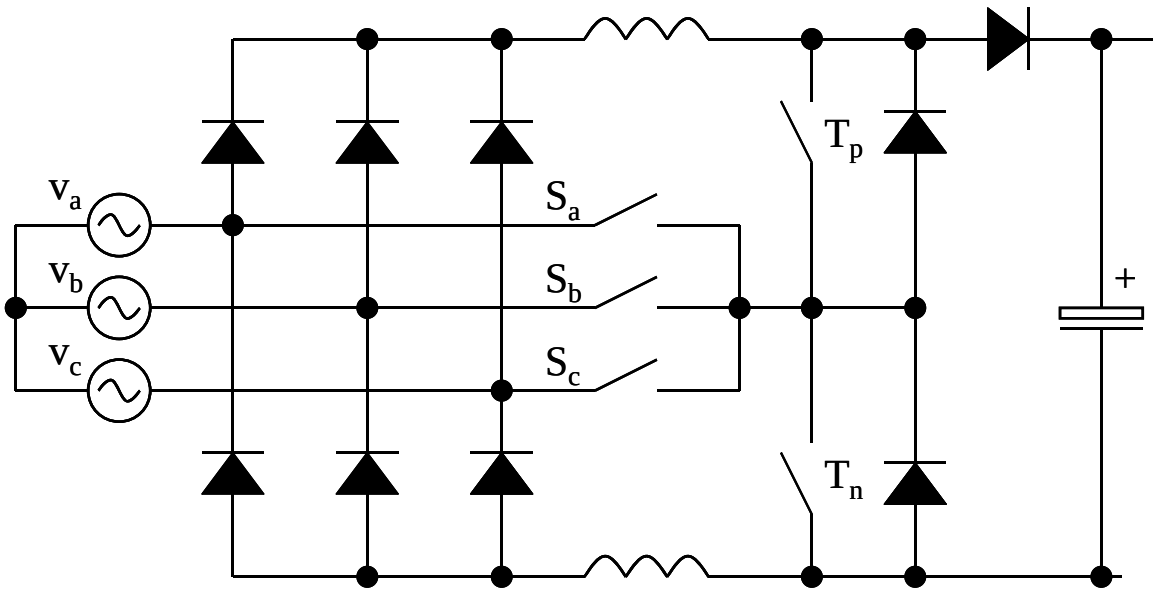



**Figure 2.8.** Series-connected dual-boost converter [5, 10].

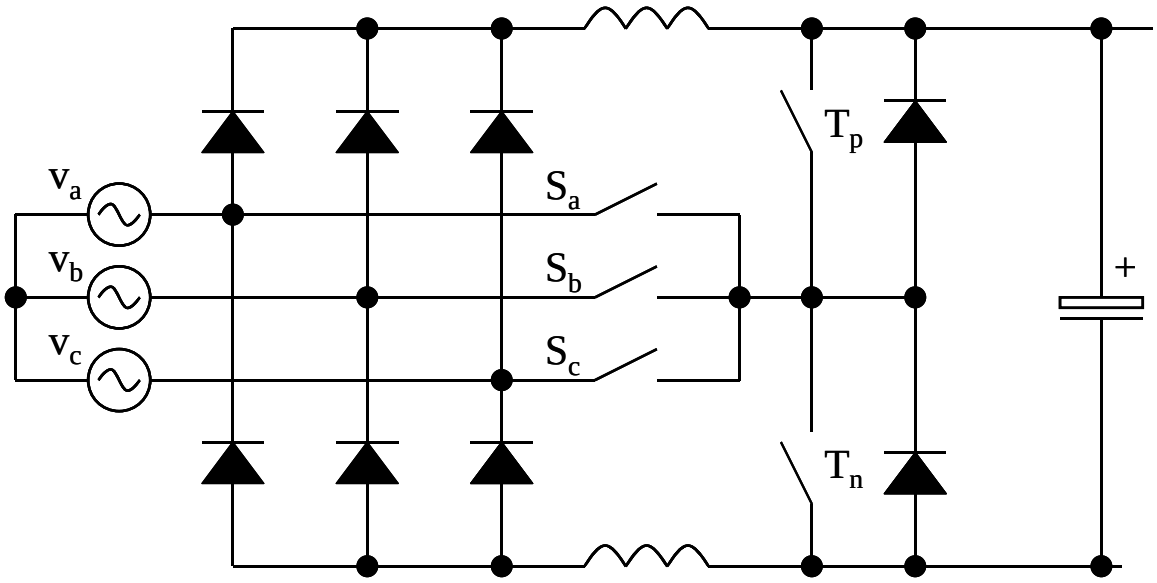



**Figure 2.9.** Series-connected dual-boost converter with inverter leg [5].

### 2.2.5 Asymmetrical half-bridge

[5, 11] presents a single DC output topology utilizing DC inductors and only two high frequency switches. From [5] it is known that the line current harmonic distortion is below 5%.

An added advantage of this rectifier, as can be seen from figure 2.10, is that there are only two switches of which only one requires an isolated gated drive. This makes this topology's control effort far less than the other topologies discussed above, with the exception of the single switch rectifier. The minimum output voltage is $1.41V_{LL}$ [6].

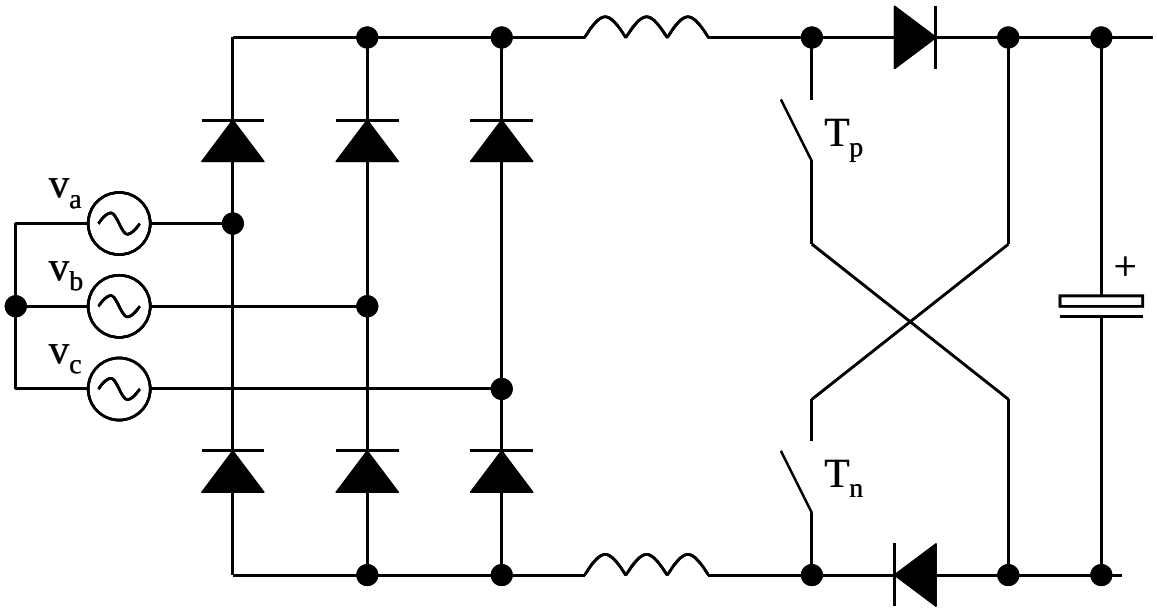



**Figure 2.10.** Asymmetrical half-bridge [5].

## 2.3 THREE-LEVEL OUTPUT CONVERTERS

### 2.3.1 Dual-boost three-level output converters

[6] shows that three-phase AC can be converted to a split DC rail with two-controlled switches. Figure 2.11 shows the implementation of the topology with AC side inductors and in figure 2.12 the implementation with DC side inductors.

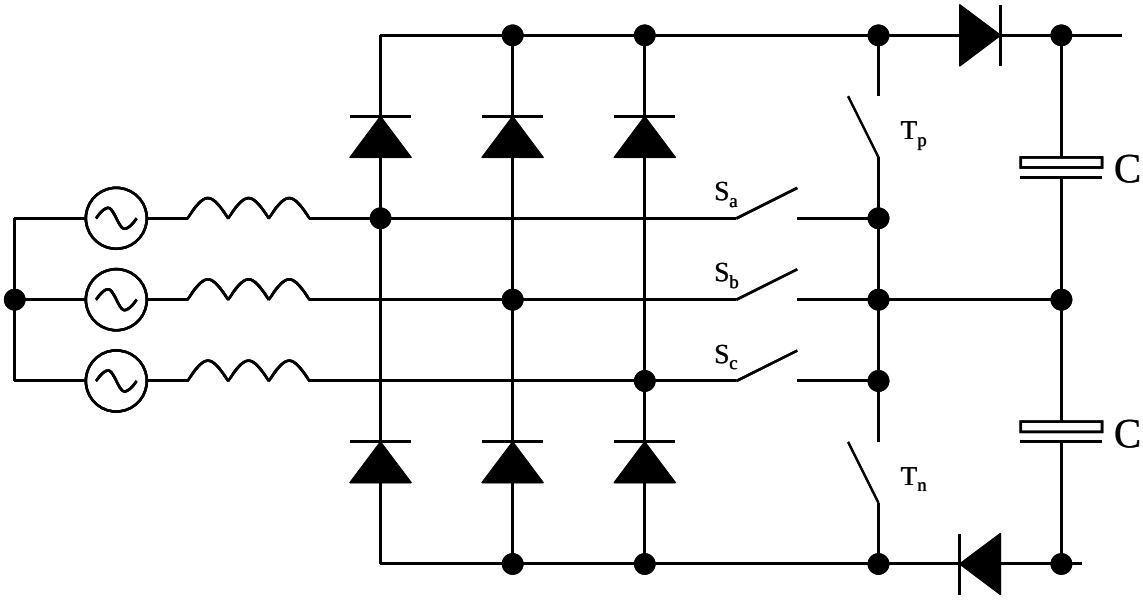



**Figure 2.11.** Two-switch boost converters with AC-side inductors and dual DC-rail [6].

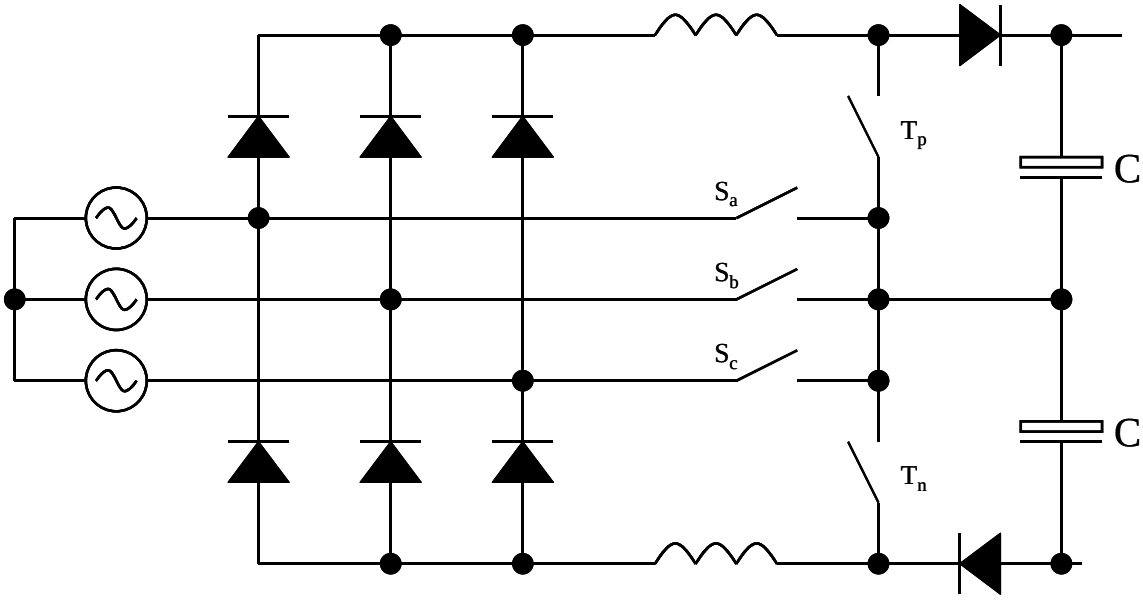



**Figure 2.12.** Two-switch boost converters with DC-side inductors and dual DC-rail [6].

The topologies shown in figures 2.11 and 2.12 feature two high frequency control switches $T_p$ and $T_n$. Switches $S_a$, $S_b$ and $S_c$ are used for the selective injection of the current into the three-phase AC supply. The state of these line switches is turned over every 60°, corresponding to when the corresponding phase voltage is within ±30° of its zero crossover. Switching frequency of the line switches is thus twice than that of the line frequency [6].

As can be seen from figure 2.11 and figure 2.12, all switches except one ($T_n$) require an isolated gate drive. This makes the implementation of this topology more difficult than all of the other topologies mentioned, including the H-bridge rectifier that only require isolated gate-drives for three switches.

A significant disadvantage of this topology is the high output voltage required. Since one of the selector switches ($S_a$, $S_b$ and $S_c$) will be closed at all times [10], the result is that the minimum voltage over each capacitor shall be the peak input line-to-line voltage. Thus the minimum boost voltage is equal to twice the rectified line-to-line voltage, or $2.45V_{LL}$ [6].

This topology can be controlled with a hysteresis type controller [6] and with a constant switching frequency [10].

A variation on the rectifier presented in figure 2.12 is presented by [7]. Here a center tap switch can be used to disconnect or connect the capacitor neutral point, and allows operation for a wide range of inputs [7], such as variable voltage generator type inputs.

The line current THD for the topology shown in figure 2.12 (two-switch boost converters with DC-side inductors with dual dc-rail) is below 5% [11].

Both rectifiers shown in figure 2.12 and figure 2.13 feature low line current distortion and very low electrical switch stresses and current stress [5].

The greatest disadvantages of both rectifiers are the high control effort (especially the topology shown in figure 2.13 that requires additional logic and an isolated gate drive to control the centre-tap switch) and the high output voltage.

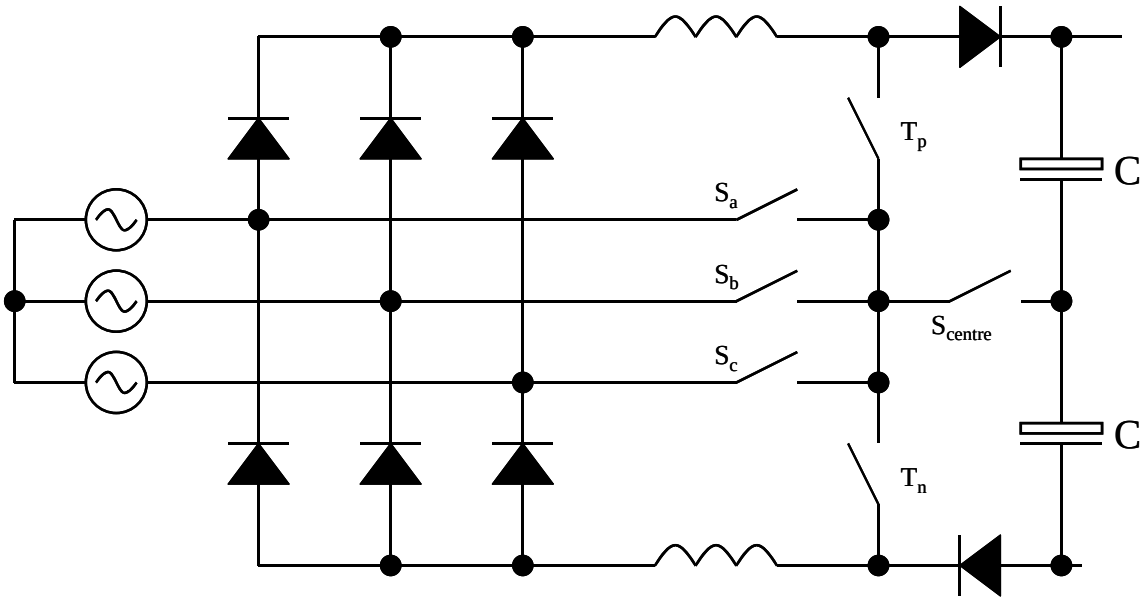



**Figure 2.13.** Two-switch boost converters with DC-side inductors and dual dc-rail output featuring a center tap switch [5].

### 2.3.2 Three-phase three-level centre-tap switch rectifier topologies

[5] presents two three-level rectifiers with split DC-Inductors, as shown in figure 2.14 and figure 2.15. The output voltage for both of these rectifiers is greater than $2.45V_{LL}$ [6]. Both rectifiers shown in figure 2.14 and figure 2.15 feature low line current distortion of 5-10% [5]. The topology shown in figure 2.14 features a single high frequency switch ($S_{centre}$), with very low current stress [5]. The star-connected switches feature very low electrical stresses [5]. One significant disadvantage of the topology shown in figure 2.15 is that it suffers from low frequency 360Hz ripple components superimposed on the line currents, for a line frequency of 60Hz [5].

As can be seen from figure 2.14 and figure 2.15 all the switches require an isolated gate drive, for a total of four isolated gate drives.

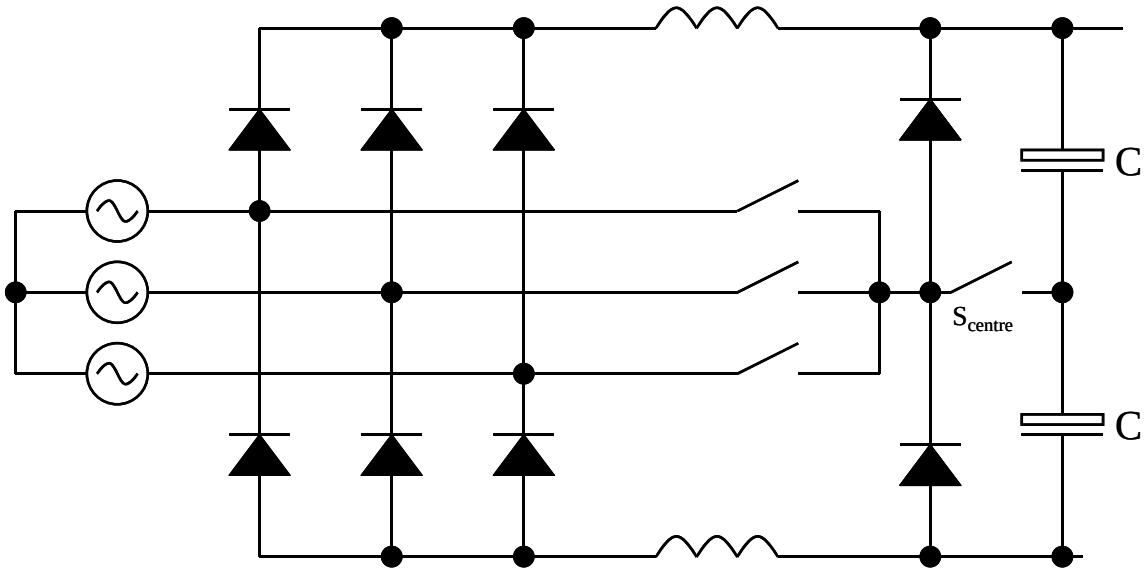



**Figure 2.14.** Three-level center-tap switch rectifier [5].

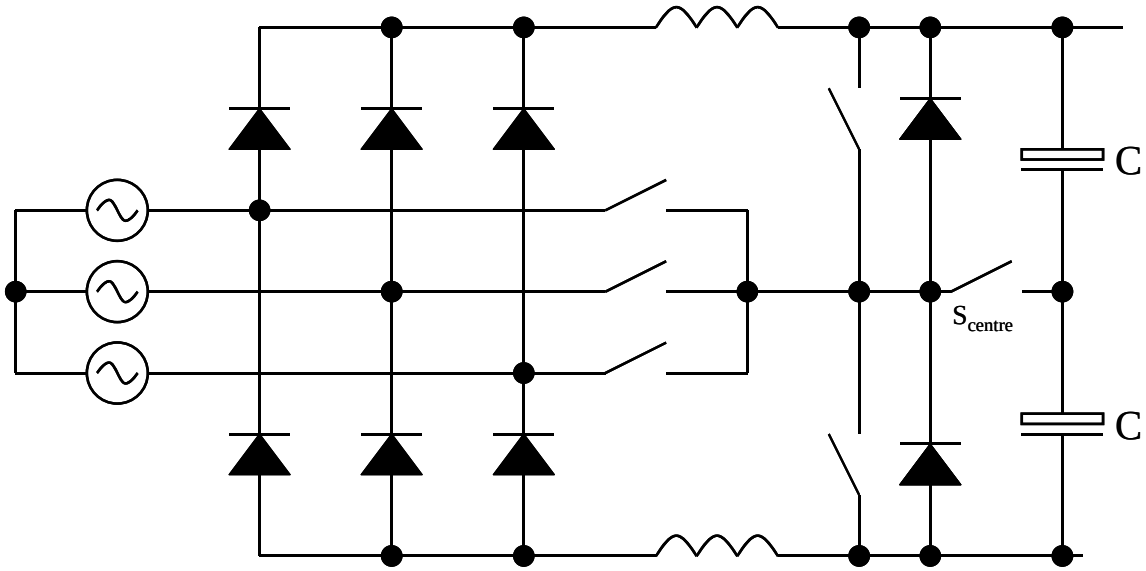



**Figure 2.15.** Three-level inverter-leg and center-tap switch rectifier [5].

Line current distortion for the topologies shown in figure 2.14 and figure 2.15 is 5-10% [5, 7].

### 2.3.3 Three-level asymmetrical half-bridge topologies

[10] presents two split DC rail topologies that employ two PWM switches, connected asymmetrically, to shape the input current. Both of these topologies employ star-connected switches for selectively injecting current [6], and features low electrical stresses on the bi-directional switches [11]. Both of these rectifiers can also be controlled with a fixed switching frequency [10]. The input line current distortion is below 5% [11].

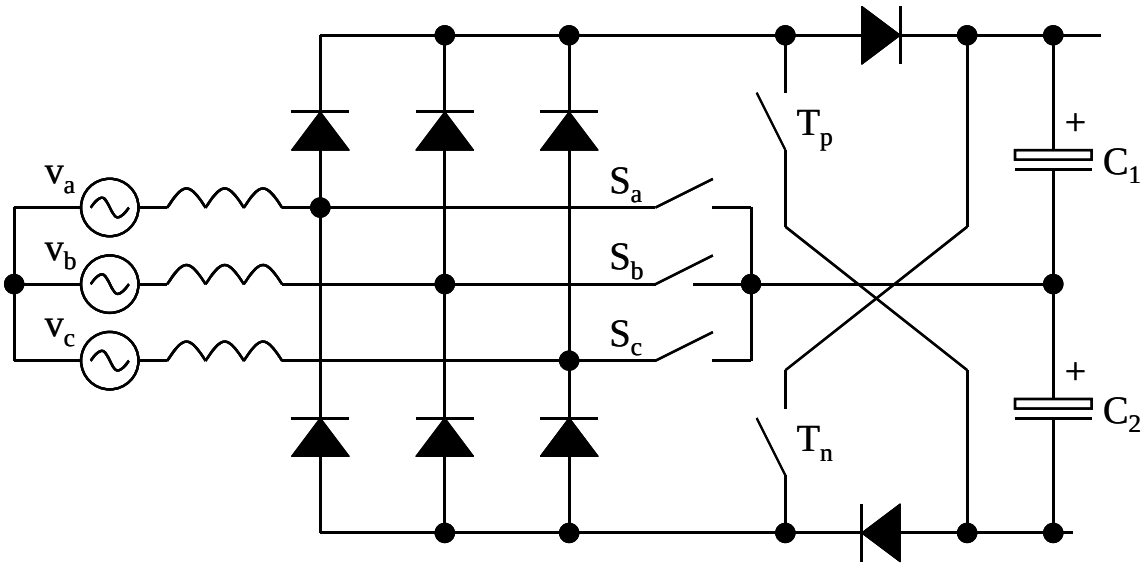



**Figure 2.16.** 3-phase boost rectifier with AC inductors and an asymmetric half bridge [10].

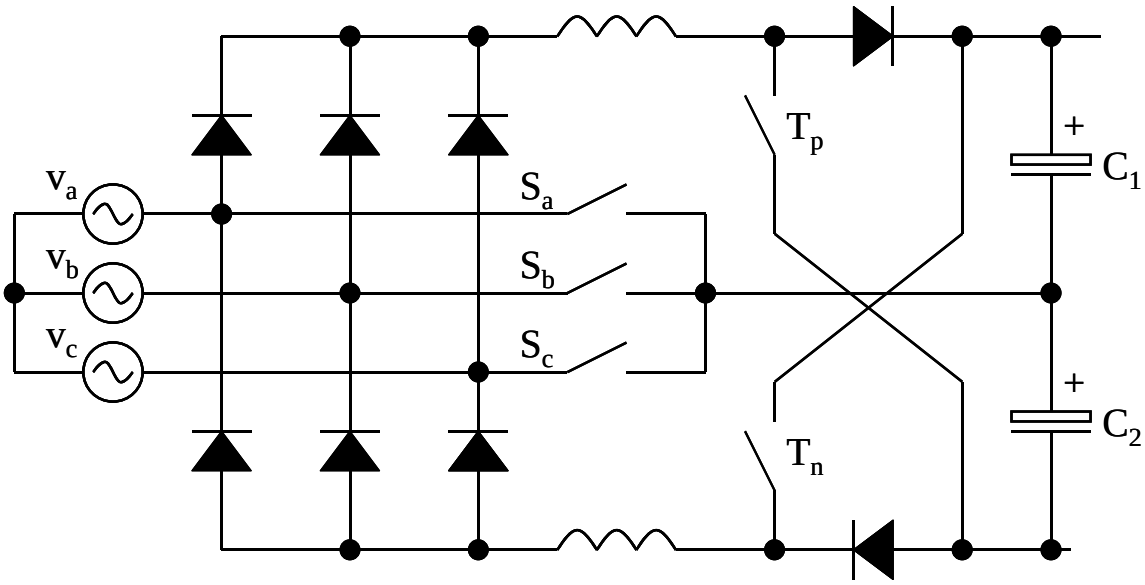



**Figure 2.17.** 3-phase boost rectifier with DC inductors and asymmetric half bridge [10, 11].

As can be seen from figure 2.16 and figure 2.17, all the switches require an isolated gate drive, for a total of five isolated gate drives. This renders the implementation of this topology more difficult than topologies mentioned in the previous sections, including the H-bridge that only require isolated gate-drives for three switches. Since this is a three-level output, the minimum boost voltage is $2.45V_{LL}$ [6].

[11] states the line current distortion for the 3-phase boost rectifier with DC inductors and asymmetric half bridge, shown in figure 2.17, is below 5% [11]

### 2.3.4 VIENNA rectifier

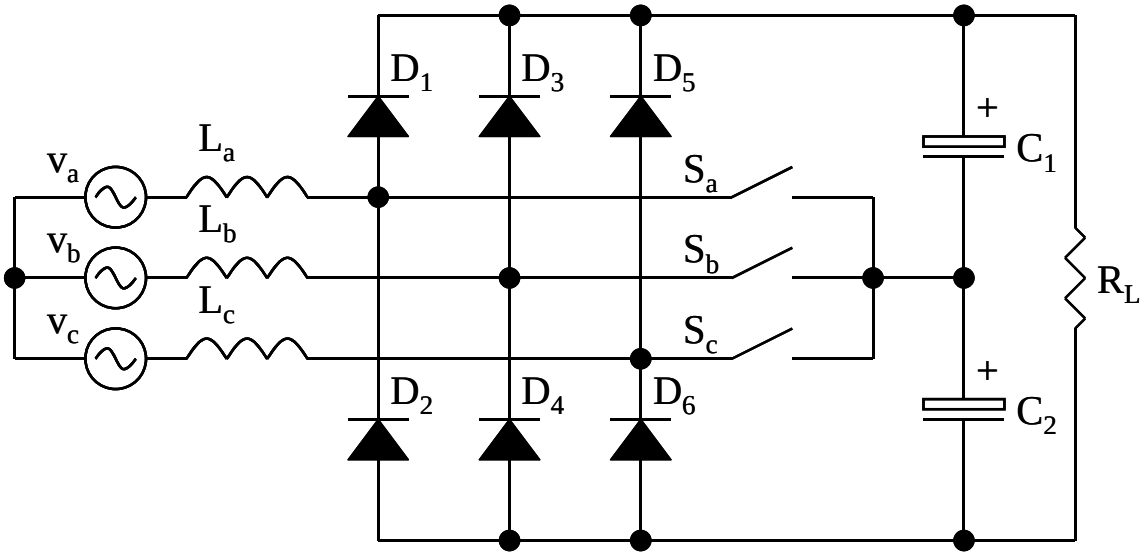



**Figure 2.18.** The VIENNA rectifier (three-switch three-level three-phase rectifier) [5].

The VIENNA rectifier is a three-switch rectifier (only) that features a split output DC-rail. Control is only required for three switches, which makes it a far easier implementation than the two switch-rectifiers (five floating switches) and the H-bridge (three floating switches, three switches referenced to ground). Control effort is still significantly higher than the single switch implementations, but the input current distortion of the VIENNA rectifier, of approximately 8.2%, is far less than that of the single-switch implementations [2] and is on par with the H-bridge and the two-switch and three-switch implementations [2].

The most significant disadvantage of the VIENNA rectifier is the high boost ratio and hence, the high output voltage required (as discussed in the previous section). The

VIENNA rectifier basically functions as a two-switch boost rectifier (for the dual-boost constant switching frequency controller), with one of the switches switched at the line frequency and two switches switched at high frequency. With one switch permanently on for a 60° control block [6], the VIENNA rectifier can be seen as two independent boost rectifiers, one for boosting $C_1$ and the other for boosting $C_2$. Thus it can be seen that the minimum boost voltage over $C_1$ and $C_2$ will be the maximum line-to-line voltage of the input. The equivalent representation for a 60° control block (one switch "on") is shown in figure 2.19.

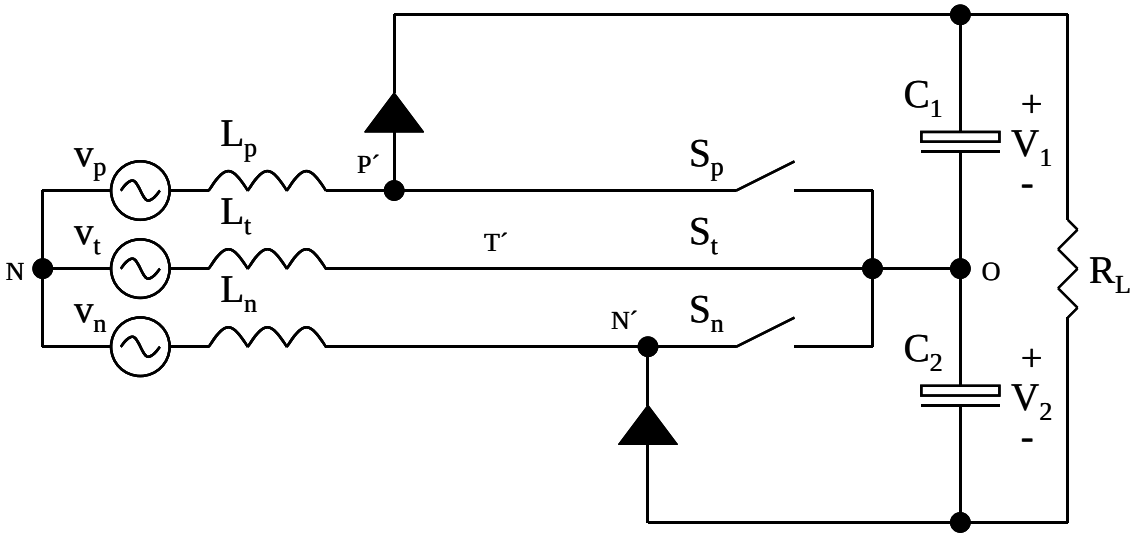



**Figure 2.19.** Equivalent model for the VIENNA rectifier for a 60° control block (one switch closed) [12].

[6] points out that the VIENNA rectifier has lower switch and diode currents than all of the other dual-boost rectifiers. [2] states that the switch losses and diode losses for the H-bridge and the VIENNA rectifier are comparable, with both rectifiers having the same harmonic distortion.

An added advantage of the VIENNA rectifier is that modules are available where all of the semiconductors of a power stage bridge leg are present [13].

## 2.4 CONTROL OF THE VIENNA RECTIFIER

**Table 2.1.** Advantages and disadvantages of the different control methods.

| | **Control Method** | |
|---|---|---|
| | **Constant Frequency** | **Hysteresis control** |
| **Advantages** | Easier EMI filtering because of single switching frequency | EMI distributed over a wide spectrum |
| | Simple control implementation [10, 14] | Inherent current protection |
| | Single control loop for controlling output voltage and input current [10, 14] | |
| | Automatic balancing of output capacitor bank [10] | |
| **Disadvantages** | Input voltage state sensing required (when operated as a dual-boost rectifier). Thus higher sensing effort [10] | More stringent EMI filtering (EMI distributed over a wide spectrum, because of varying frequency) |
| | | Input voltage sensing required [16] |
| | | Second control loop required for balancing output capacitor bank [16] |
| | | Control algorithm more difficult [16] |

### 2.4.1 Hysteresis control

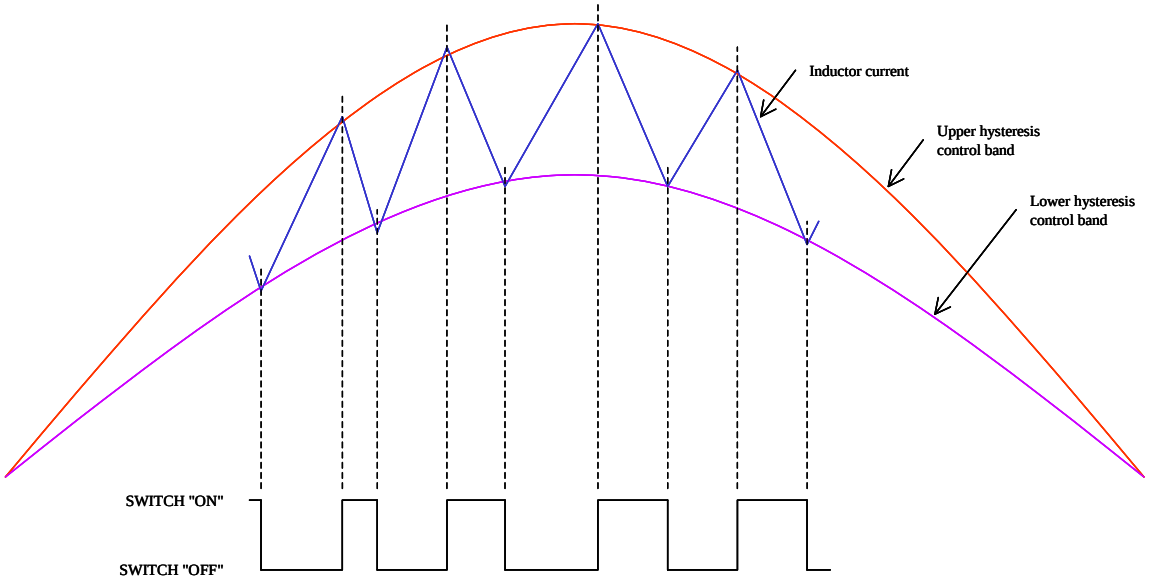



**Figure 2.20.** Hysteresis control of three-phase active rectifiers [15].

Figure 2.20 shows the basic control concept of the hysteresis type control. Two current bands, a lower and an upper band, are set-up. The current is controlled by means of on-off switching of the switch, to be within the boundaries set-up by the control bands. The range of the switching frequency can be controlled by increasing/decreasing the current control bands. The major disadvantage of this type of controller is the complexity. This type requires a second control loop for balancing the two output capacitors, although the centre point voltage is naturally stable [16]. Furthermore, the controller also requires various multipliers for scaling the input current to set up the control bands. The one major advantage of hysteresis type control, compared to a constant switching type control, is that the power harmonics are distributed over a wide frequency range due to the time-varying frequency [15]. Constant frequency control might require a small EMI filter at the input to comply with conducted EMI regulations [15].

### 2.4.2 Constant frequency control

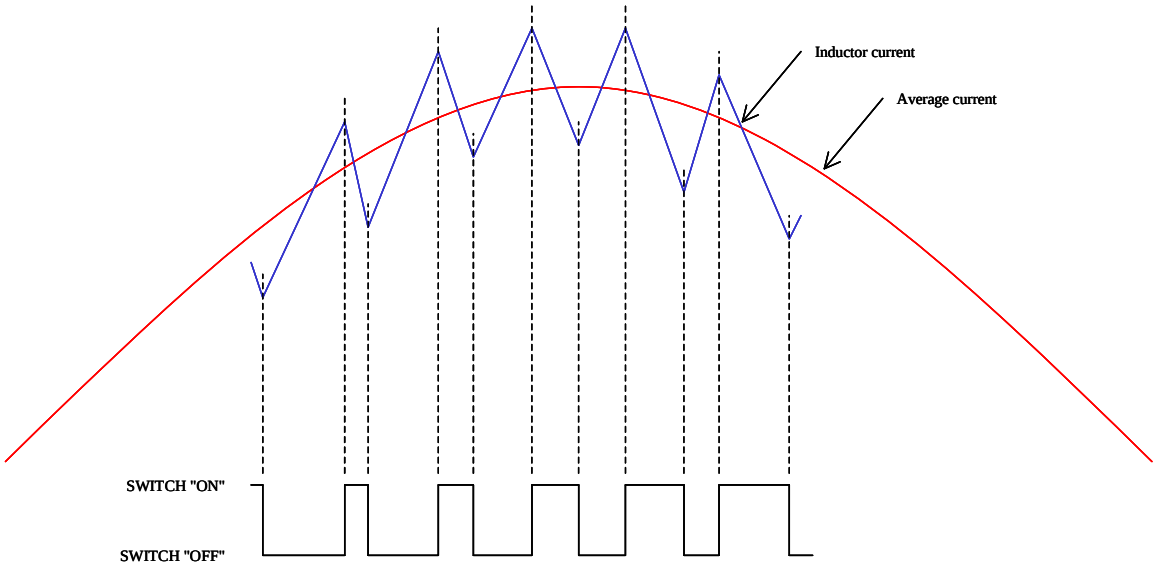



**Figure 2.21.** Constant switching frequency control of three-phase active rectifiers.

Figure 2.21 shows the basic control concept of constant switching frequency type control. Each control switch is switched at a constant frequency. The duty cycle for each switch is the inverse relationship of the filtered output to the input currents [14]. The switching frequency stays constant, while only the pulse width is varied.

**Table 2.2.** Advantages and disadvantages of the different constant switching frequency control methods.

| | **Control Method** | |
|---|---|---|
| | **Unified constant-frequency Integration controller** | **Dual-boost general PFC controller** |
| **Advantages** | No 3-phase voltage sensing required | Only 2 switches switching at high frequency. Significant reduction in switching losses |
| | Simple control | Mathematical model (Control model for the plant) much simpler for dual-boost controller |
| | Less distortion of the input current | |
| **Disadvantages** | Switching losses more | Control circuitry requires multipliers and additional control logic |
| | Complex mathematical model. | 3-phase voltage sensing required |

#### 2.4.2.1 Unified constant-frequency integration controller

For unified constant-frequency integration control [14], each switch is controlled independently in accordance with the corresponding input current. For this type of control, the rectifier can be seen as three independent converters [14]. The main advantage of this type of control is that the sensing effort is much less than the dual boost control since no input voltage sensing is required. Furthermore, the control effort is much less since no multipliers and other control logic are required. The main disadvantage of this control method is to obtain the control model. Since all three currents are controlled, the plant and control models will include an extra state, compared to the dual boost controller, making it very difficult to obtain and to solve the problem at hand. The second disadvantage that makes the dual-boost controller more suitable is the fact that switching currents are greater for the unified constant-frequency integration control, due to the fact that three switches are switched at a high frequency.

For the unified constant-frequency integration controller, each phase current is compared independently to the error amplifier to generate the PWM output, as shown in figure 2.22. There is latch at the output of each comparator to prevent switching due to noise.

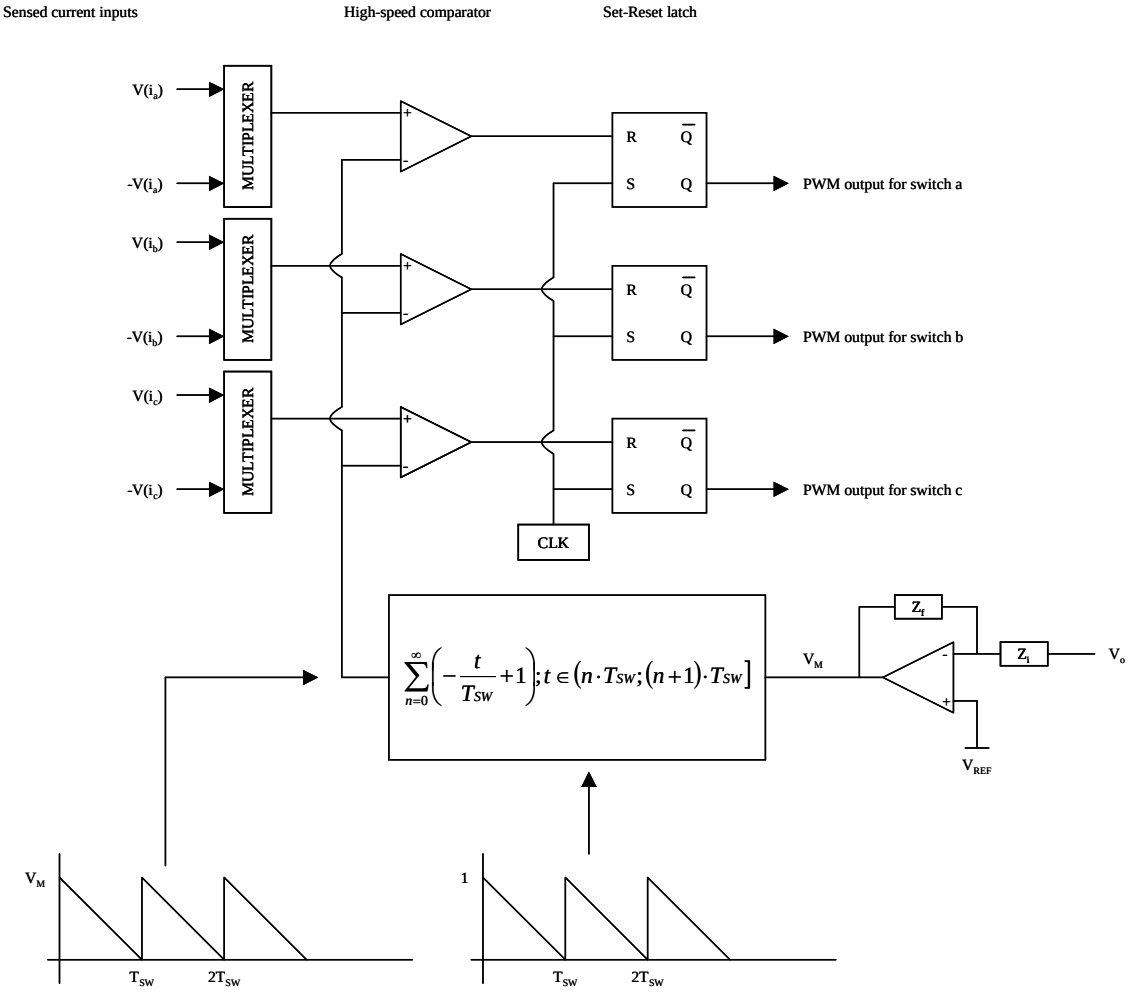



**Figure 2.22.** Unified constant-frequency integration controller [14].

### 2.4.2.2 General PFC controller for dual-boost topologies

For the dual-boost controller [10], the rectifier functions as two converters: one converter for converting one input (line-to-line, and not phase input) to one-half of the output e.g. the output over $C_1$, and the other for converting the alternate input to the output over $C_2$. There are two major disadvantages in this type of controller. Firstly, the controller is more complex than the unified constant-frequency integration controller since it requires multipliers and some added control logic. Secondly, where the unified constant-frequency integration features automatic current limiting, it is not possible for the dual-boost controller due to the fact that only two currents are sensed at any given time.

For the dual-boost controller there are only two comparators, where the signal compared to the error amplifier is the sum of two times the most positive sensed phase current and the most negative sensed phase current, as shown in figure 2.23. There is latch at the output of each comparator to prevent switching due to noise [10].

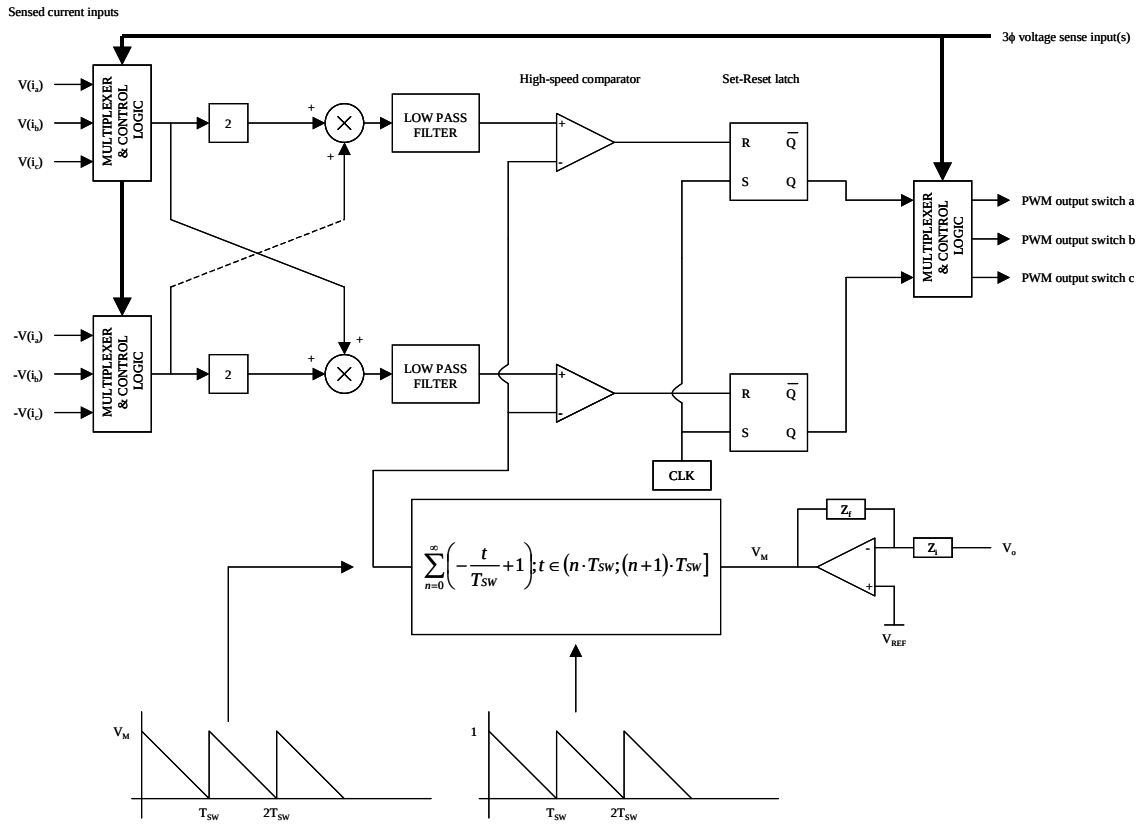



**Figure 2.23.** General PFC controller for dual-boost type topologies [10].

## 2.5 CONCLUSION AND SUMMARY

Table 2.3 summarizes the topology study and compares the various rectifier topologies with respect regarding: number of switching elements; number of floating gate drives; number of inductors; voltage output type (two-level or three-level); input current harmonic distortion; control type; and advantages and disadvantages of every topology.

From the topologies discussed the VIENNA rectifier offers the best compromise in terms of performance, component count and controllability. It offers the same or better performance (harmonic distortion) as most multi-switch topologies, whilst utilizing fewer switches. With the dual-boost constant switching frequency controller, the VIENNA rectifier is easy to control and it's just as easy to set-up an equivalent control model for the VIENNA rectifier. If the control is implemented digitally, the effort for implementation of the dual-boost controller shall be the same as for unified constant-frequency integration controller, whilst offering lower switching losses.

**Table 2.3.** Quantitative comparison of different converters

| | Unidirectional single-switch boost rectifier | Unidirectional single-switch boost rectifier, DC-side filtering | Three-phase delta-connected three-switch rectifier |
|---|---|---|---|
| Figure Reference | 2.1 | 2.2 | 2.3 |
| Number of PWM switches | 1 | 1 | 2 (effectively) |
| Number of bi-directional switches | - | - | 1 (effectively) |
| Number of switches that requires isolated gate drive | 0 | 0 | 3 |
| Number of ac-side inductors | 3 | - | 3 |
| Number of dc-side inductors | - | 1 | - |
| Output voltage type | Single | Single | Single |
| Minimum output voltage | $>1.35V_{LL}$ | $>1.35V_{LL}$ | $>1.35V_{LL}$ |
| Harmonic distortion | ~20% | ~32% | ~6.1% |
| Control type | Hysteresis, Constant Switching Frequency | Hysteresis, Constant Switching Frequency | Hysteresis, Constant Switching Frequency |
| EMI filtering | Yes, high filtering effort | Yes, high filtering effort | Yes, low filtering effort |
| Input current | Discontinuous | Discontinuous | Continuous |
| Advantages | • Single switch<br>• Low overall component count | • Single switch<br>• Low overall component count | • Low harmonic distortion<br>• Low output voltage<br>• Low switch conduction loss<br>• Only 3 switches |
| Disadvantages | • Discontinuous input current<br>• High component stresses | • Discontinuous input current<br>• High component stresses | • High component count<br>• High component stresses |

**Table 2.3 (cont.).** Quantitative comparison of different converters

| | Three-phase star-connected three-switch rectifier | 3-phase boost rectifier with an inverter network | H-bridge boost rectifier |
|---|---|---|---|
| Figure Reference | 2.4 | 2.6 | 2.7 |
| Number of PWM switches | 2 (effectively) | 12 | 6 |
| Number of bi-directional switches | 1 (effectively) | 6 | 6 |
| Number of switches that requires isolated gate drive | 3 | 6 | 3 |
| Number of ac-side inductors | 3 | 3 | 3 |
| Number of dc-side inductors | - | - | - |
| Output voltage type | Single | Single | Single |
| Minimum output voltage | $>1.35V_{LL}$ | $>1.35V_{LL}$ | $>1.35V_{LL}$ |
| Harmonic distortion | ~6.1% | Low (i.e. <10%) | ~8.1% |
| Control type | Hysteresis, Constant Switching Frequency | Hysteresis, Constant Switching Frequency | Hysteresis, Constant Switching Frequency |
| EMI filtering | Yes, low filtering effort | Yes, low filtering effort | Yes, low filtering effort |
| Input current | Continuous | Continuous | Continuous |
| Advantages | • Low harmonic distortion<br>• Only 3 switches | • Low harmonic distortion | • Low harmonic distortion<br>• Possible 4-quadrant operation |
| Disadvantages | • High component count<br>• High component stresses | • Very high component count<br>• Six control switches | • Very high component count<br>• Six control switches |

**Table 2.3 (cont.).** Quantitative comparison of different converters

| | Series-connected dual-boost converter | Series-connected dual-boost converter with inverter leg | Asymmetrical half-bridge |
|---|---|---|---|
| Figure Reference | 2.8 | 2.9 | 2.10 |
| Number of PWM switches | 2 | 2 | 2 |
| Number of bi-directional switches | 3 | 3 | - |
| Number of switches that requires isolated gate drive | 4 | 4 | 2 |
| Number of ac-side inductors | - | - | - |
| Number of dc-side inductors | 2 | 2 | 2 |
| Output voltage type | Single | Single | Single |
| Minimum output voltage | $>1.5V_{LL}$ | $>1.35V_{LL}$ | $>1.414V_{LL}$ |
| Harmonic distortion | Low (i.e. <10%) | Low (i.e. <10%) | <5% |
| Control type | Hysteresis, Constant Switching Frequency | Hysteresis, Constant Switching Frequency | Hysteresis, Constant Switching Frequency |
| EMI filtering | Yes, low filtering effort | Yes, low filtering effort | Yes, low filtering effort |
| Input current | Continuous | Continuous | Continuous |
| Advantages | • Low harmonic distortion<br>• Low switch stresses | • Low harmonic distortion; only 2 inductors<br>• Only 2 high-freq. switches | • Low harmonic distortion<br>• Low component count |
| Disadvantages | • High component count<br>• 4 isolated gate drives | • High component count<br>• 4 isolated gate drives | • No bi-directional switches – no flexibility |

**Table 2.3 (cont.).** Quantitative comparison of different converters

| | Two-switch boost converters with AC-side inductors and dual dc-rail output | Two-switch boost converters with DC-side inductors and dual dc-rail output | Two-switch boost converter with DC-side inductors and dual dc-rail, with center tap switch |
|---|---|---|---|
| Figure Reference | 2.11 | 2.12 | 2.13 |
| Number PWM switches | 2 | 2 | 2 |
| Number of bi-directional switches | 3 | 3 | 4 |
| Number of switches that requires isolated gate drive | 5 | 5 | 6 |
| Number of ac-side inductors | 3 | - | - |
| Number of dc-side inductors | - | 2 | 2 |
| Output voltage type | Dual | Dual | Dual |
| Minimum output voltage | $>2.45V_{LL}$ | $>2.45V_{LL}$ | $>2.45V_{LL}$ |
| Harmonic distortion | Low (i.e. <10%) | <5% | Low (i.e. <10%) |
| Control type | Hysteresis, Constant Switching Frequency | Hysteresis, Constant Switching Frequency | Hysteresis, Constant Switching Frequency |
| EMI filtering | Yes, low filtering effort | Yes, low filtering effort | Yes, low filtering effort |
| Input current | Continuous | Continuous | Continuous |
| Advantages | • Low harmonic distortion<br>• Only 2 high-freq. switches | • Low harmonic distortion; only 2 inductors<br>• Only 2 high-freq. switches | • Low harmonic distortion<br>• Only 2 high-freq. Switches<br>• Flexible topology |
| Disadvantages | • Very high component count<br>• 5 isolated gate drives<br>• High output voltage | • Very high component count<br>• 5 isolated gate drives<br>• High output voltage | • High component count<br>• 5 isolated gate drives<br>• High output voltage |

**Table 2.3 (cont.).** Quantitative comparison of different converters

| | Three-level center-tap switch rectifier | Three-level inverter-leg and center-tap switch rectifier | Three-phase boost rectifier with AC inductors and an asymmetric half bridge |
|---|---|---|---|
| Figure Reference | 2.14 | 2.15 | 2.16 |
| Number of PWM switches | 1 | 2 | 2 |
| Number of bi-directional switches | 3 | 4 | 3 |
| Number of switches that requires isolated gate drive | 4 | 4 | 5 |
| Number of ac-side inductors | - | - | 3 |
| Number of dc-side inductors | 2 | 2 | - |
| Output voltage type | Dual | Dual | Dual |
| Minimum output voltage | $>2.45V_{LL}$ | $>2.45V_{LL}$ | $>2.45V_{LL}$ |
| Harmonic distortion | 5-10% | 5-10% | Low (i.e. <10%) |
| Control type | No reference | No reference | Constant Switching Frequency |
| EMI filtering | Yes, high filtering effort | Yes, low filtering effort | Yes, low filtering effort |
| Input current | Continuous | Continuous | Continuous |
| Advantages | • Low harmonic distortion<br>• Only 2 high-freq. switches | • Low harmonic distortion<br>• Only 2 high-freq. switches | • Low harmonic distortion<br>• Only 2 high-freq. switches |
| Disadvantages | • 4 isolated gate drives<br>• 360Hz distortion (input current)<br>• High output voltage | • Very high component count<br>• 4 isolated gate drives<br>• High output voltage | • High component count<br>• 5 isolated gate drives<br>• High output voltage |

**Table 2.3 (cont.).** Quantitative comparison of different converters

| | Three-phase boost rectifier with DC inductors and an asymmetric half bridge | The VIENNA rectifier (three-switch three-level three-phase rectifier) |
|---|---|---|
| Figure Reference | 2.17 | 2.18 |
| Number of PWM switches | 2 | 3 (2 effectively) |
| Number of bi-directional switches | 3 | 3 |
| Number of switches that requires isolated gate drive | 5 | 3 |
| Number of ac-side inductors | - | 3 |
| Number of dc-side inductors | 2 | - |
| Output voltage type | Dual | Dual |
| Minimum output voltage | $>2.45V_{LL}$ | $>2.45V_{LL}$ |
| Harmonic distortion | <5% | ~8.2% |
| Control type | Constant Switching Frequency | Hysteresis, Constant Switching Frequency |
| EMI filtering | Yes, low filtering effort | Yes, low filtering effort |
| Input current | Continuous | Continuous |
| Advantages | • Low harmonic distortion<br>• Only 2 high-freq. switches | • Low harmonic distortion<br>• Only 2 high-freq. switches |
| Disadvantages | • Very high component count<br>• 5 isolated gate drives<br>• High output voltage | • High component count<br>• High output voltage |

# CHAPTER 3

# MODAL ANALYSIS OF THE VIENNA RECTIFIER

## 3.1 INTRODUCTION

From the various converter/control topologies discussed in Chapter 2 the VIENNA rectifier with constant switching frequency dual-boost type controller was chosen as the suitable rectifier for converting a generator type input, due to following grounds:

- The VIENNA rectifier offers the same or less input current harmonic distortion than the other topologies;
- The VIENNA rectifier, with its three-level output, allows any DC-DC converter to be used at the rectifier output (half-bridge, full-bridge or any other topology) and, with constant switching frequency control, no additional circuitry is required to balance the two output capacitors. The high boost voltage of $2.45V_{LL}$ might be a disadvantage, but the three-level output allows the designer some flexibility in his design;
- The VIENNA rectifier has only three switches, which are significantly fewer than other active rectifiers with the same performance (in terms of harmonic distortion);
- The VIENNA rectifier requires less control effort (in terms of the number of isolated gate drives required) than other active rectifier topologies with comparable performance (in terms of harmonic distortion);
- With constant switching frequency dual-boost control sufficient sensing effort is provided to implement dual-boost control or unified one-cycle control if needed but not *vice versa*;
- Implementation of the VIENNA rectifier is eased by the availability of single bridge leg modules [13];
- and, Dual-boost constant frequency control is not dependant on a fixed line frequency, making it ideal for variable frequency type inputs.

In this Chapter mathematical models are derived that describes the VIENNA rectifier "plant" in state-space as well as the VIENNA rectifier constant frequency "control" in state-space. These mathematical models provide the gain and phase frequency response of the VIENNA rectifier for constant switching frequency operation and are used to design a suitable compensator for stable control operation.

In this section the VIENNA rectifier will be analyzed in detail and models will be derived describing the transfer functions of the plant, controller and control compensator. The VIENNA rectifier is illustrated in figure 2.18.

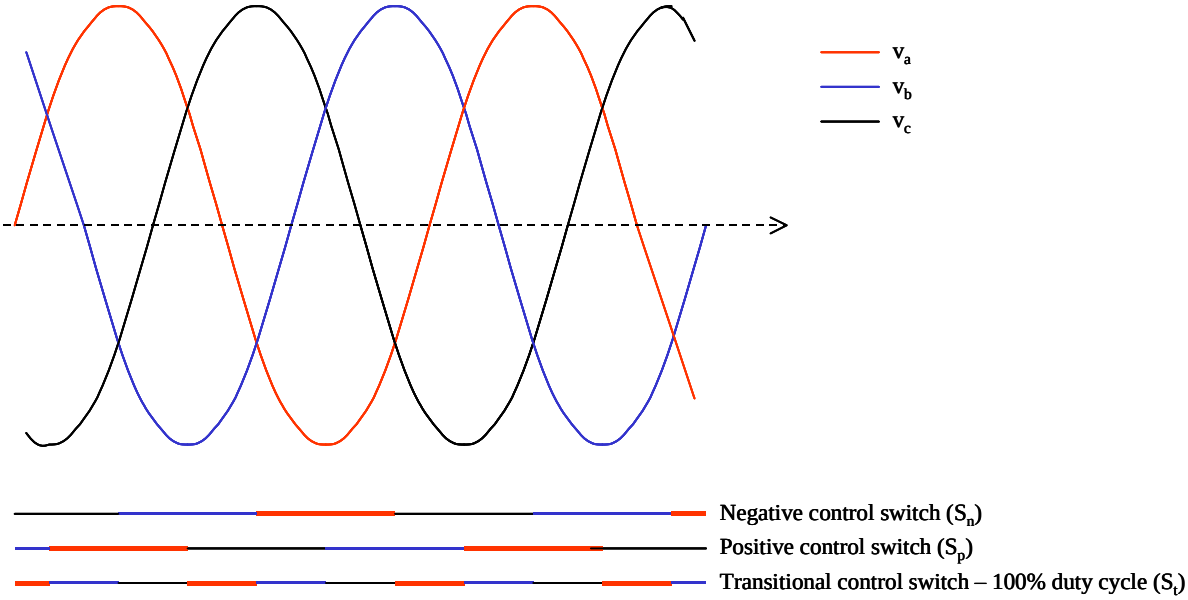



**Figure 3.1.** Three-phase source referenced to neutral.

Figure 3.1 gives an illustration of the phase voltages for a three-phase source [10]. For the purpose of the model analysis, it is assumed that the phase-currents are in phase with the respective phase voltages. The constant switching frequency dual-boost control algorithm is described in detail in [10]. As illustrated in figure 3.1 the control is rotated every 60°. During each 60° period one of the controlled switches is switched "on" for the duration of the 60° period (transitional switch), whereas the other two switches' duty cycles are varied according to the relative phase currents. With reference to figure 3.1, and assuming the phase currents are in phase with the phase voltages and current ripple is negligible, it can be seen that the integrated area product of the phase voltage and the phase current will be equal for both the positive boost rectifier and the negative boost rectifier during the 60° control period. Analysis of the VIENNA rectifier in this Chapter will show that the positive boost rectifier will transfer its energy to $C_1$, while the negative boost rectifier will transfer its energy to $C_2$. As a result of the power transferred to $C_1$ and $C_2$ being equal, the split capacitor bank comprising of $C_1$ and $C_2$ will be in balance. An example is taken from figure 3.1 for the period -30° to 30°. Switch $S_a$ is switched on during the entire period and the duty cycles of switches $S_b$ and $S_c$ varied. For $(\alpha=\omega_L t) \equiv [-30°;0°)$, $|i_c| > |i_b|$ and thus will $d_C < d_B$ (where $d_C$ is the duty cycle of switch C and $d_B$ the duty cycle of switch B). Capacitor $C_1$ will be charged more than capacitor $C_2$ (because of the difference in duty

cycles). This will result in a variation in the distribution of the output voltage across the two capacitors with $V_1 > V_2$. For $\alpha = 0°$, $|i_c| = |i_b|$ and $d_C=d_B$. At this point $V_1$ is at a maximum and $V_2$ at a minimum. For $\alpha \equiv (0°;30°]$, $|i_c| < |i_b|$ and thus will $d_C > d_B$. Capacitor $C_2$ will be charged more than capacitor $C_1$ (because of the difference in duty cycles). This will result in a variation in the distribution of the output voltage across the two capacitors, but still with $V_1 > V_2$. At the end of the 60° period the energy transferred to $C_1$ over the 60° period will equal the energy transferred to $C_2$ over the 60° period and as a result $V_1 = V_2$. Voltages $V_1$ and $V_2$ will vary at a frequency of three times the line-to-neutral frequency, but at the beginning and end of each 60° period will be equal to voltage $V_1$. However, the average voltage over one cycle is constant. This property of constant switching frequency control to automatically equalize the voltages $V_1$ and $V_2$ [10], eliminates the need for a second loop necessary to equalize $V_1$ and $V_2$ as required by hysteresis control [16].

The equivalent model for constant frequency control is shown in figure 3.2. Table 3.1 lists the control algorithm for constant frequency control. A p-subscript denotes parts associated with the positive rail, a n-subscript denotes parts associated with the negative rail and a t-subscript denotes parts associated with a transitional period (for example where the current transition from negative to positive or *vice versa*).

The small-signal model is firstly derived for a negative duty cycle larger than the positive duty cycle, $d_N > d_P$. Secondly the process is repeated for the positive duty cycle larger than the negative duty cycle, $d_P > d_N$. From the two state space-space models it should be possible then to associate common parts to the respective switch cycle off periods, $(1-d_N)$ and $(1-d_P)$. Time $t_0$ indicates the start of the switching period $T_{SW}$. The technique for deriving the models is as described by [17] and [18].

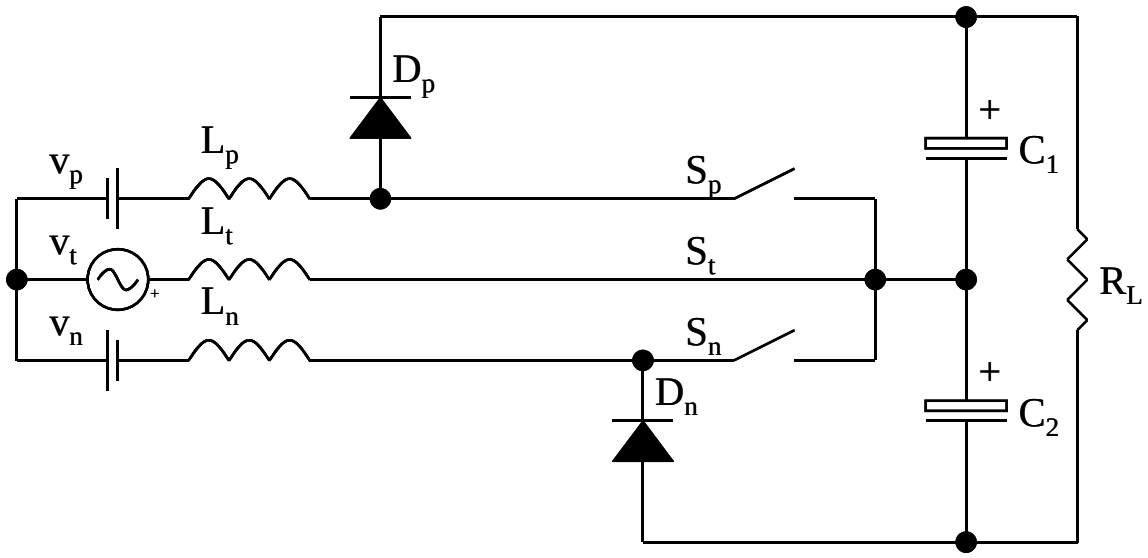



**Figure 3.2.** Equivalent model for the VIENNA rectifier for constant frequency, dual-boost control.

$V_t$ is represented in figure 3.2 as an AC-source since it can be either negative or positive. In comparison $V_p$ and $V_n$ can be modelled as fixed positive and/or negative DC-sources.

**Table 3.1.** Control algorithm for the VIENNA rectifier.

| $\alpha=\omega_L t$ | p | t | n |
|---|---|---|---|
| -30° to 30° | c | a | b |
| 30° to 90° | a | c | b |
| 90° to 150° | a | b | c |
| 150° to 210° | b | a | c |
| 210° to 270° | b | c | a |
| 270° to 330° | c | b | a |

## 3.2 VIENNA RECTIFIER PLANT TRANSFER FUNCTION

### 3.2.1 Model analysis for $d_N > d_P$

*I. Model analysis for $t \in [t_0 ; t_0 + d_P T_{SW})$, $d_N > d_P$*

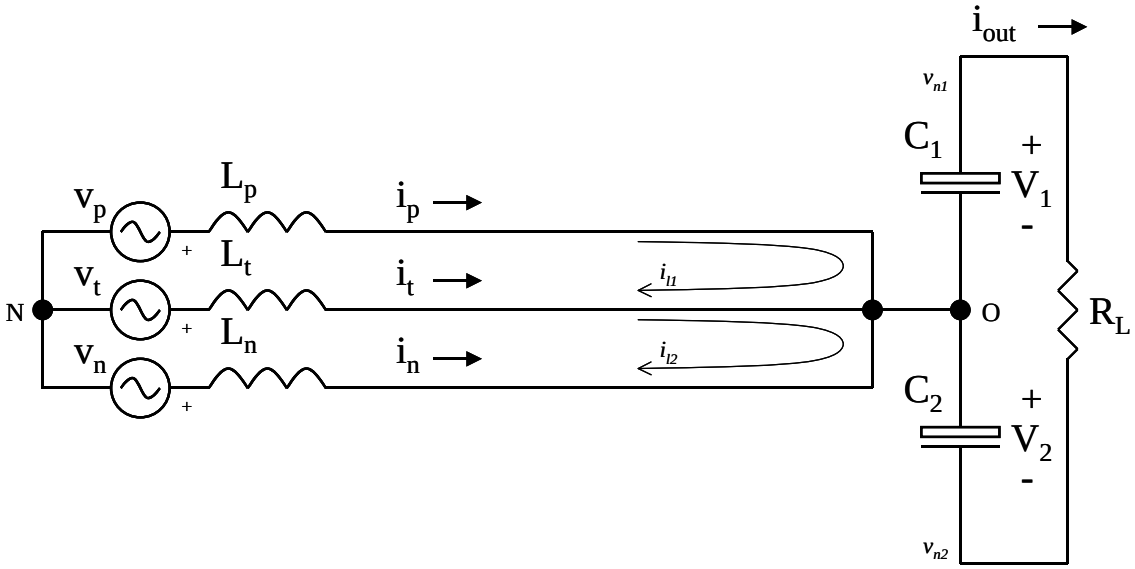



**Figure 3.3.** Model of the VIENNA rectifier for the period $t \in [t_0 ; t_0 + d_P T_{SW})$.

For this time interval all the switches are on. It is assumed that the system is in balance prior to this switching period. S-domain voltage equations for the two current loops $i_{l1}$ and $i_{l2}$ are obtained as follow:

$$-V_p + sLi_p - sLi_t + V_t = 0 \tag{3.1}$$

$$-V_t + sLi_t - sLi_n + V_n = 0 \tag{3.2}$$

Since it is assumed that the system is in balance, the following conclusion is valid:

$$V_t + V_p + V_n = 0 \tag{3.3}$$

$$i_t + t_p + i_n = 0 \tag{3.4}$$

From Theorem 1 from [19] it is known that the Laplace transforms of (3.3) and (3.4) are also in balance or:

$$sV_t + sV_p + sV_n = 0 \tag{3.5}$$

$$si_t + si_p + si_n = 0 \tag{3.6}$$

Substituting (3.3) and (3.4) in (3.1) and (3.2), and eliminating $si_t$, $sV_t$, $V_t$ and $i_t$, yields:

$$si_p = \frac{V_p}{L} \tag{3.7}$$

$$si_n = \frac{V_n}{L} \tag{3.8}$$

With reference to the voltage node $v_{n1}$ the following voltage equation (in Laplace form) is obtained:

$$0 = sv_1 CR_L + v_1 + v_2 \tag{3.9}$$

From figure 3.3 it can be seen that the current through $C_1$ and $C_2$ will be equal. Thus solving for $sv_1$ yields:

$$sv_1 = -\frac{v_1}{CR_L} - \frac{v_2}{CR_L} \tag{3.10}$$

$$sv_2 = sv_1 = -\frac{v_1}{CR_L} - \frac{v_2}{CR_L} \tag{3.11}$$

Also from figure 3.3 it can be seen that the output voltage is the summation of $v_1$ and $v_2$:

$$v_{out} = v_1 + v_2 \tag{3.12}$$

From [20] a continuous-time linear time-invariant state space model takes the form:

$$\begin{aligned} sx &= ax + bu \\ y &= cx + du \end{aligned}, \tag{3.13}$$

where x is the state vector, u the control vector and y the system output. For this analysis the state vector is defined as:

$$x = \begin{bmatrix} i_p & i_n & v_1 & v_2 \end{bmatrix}^T \tag{3.14}$$

Substituting (3.14), (3.11), (3.10), (3.8) and (3.7) into (3.13) yields an expression for the state coefficient matrix:

$$a_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \\ 0 & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \end{bmatrix} \tag{3.15}$$

An expression for the source coefficient matrix is obtained as:

$$b_1 u = \begin{bmatrix} \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 \end{bmatrix}^T \tag{3.16}$$

Substituting (3.12) into (3.13) yields:

$$c_1 = \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \tag{3.17}$$

Again, it is assumed that the system is in balance and thus $V_t$ and $i_t$ are indirectly included into equations (3.15) to (3.17), since $V_t$ is the sum of $-V_p$ and $-V_n$ and $i_t$ is the sum of $-i_p$ and $-i_n$.

*II. Model analysis for $t \in [t_0 + d_P T_{SW}\,;\, t_0 + d_N T_{SW})$, $d_N > d_P$*

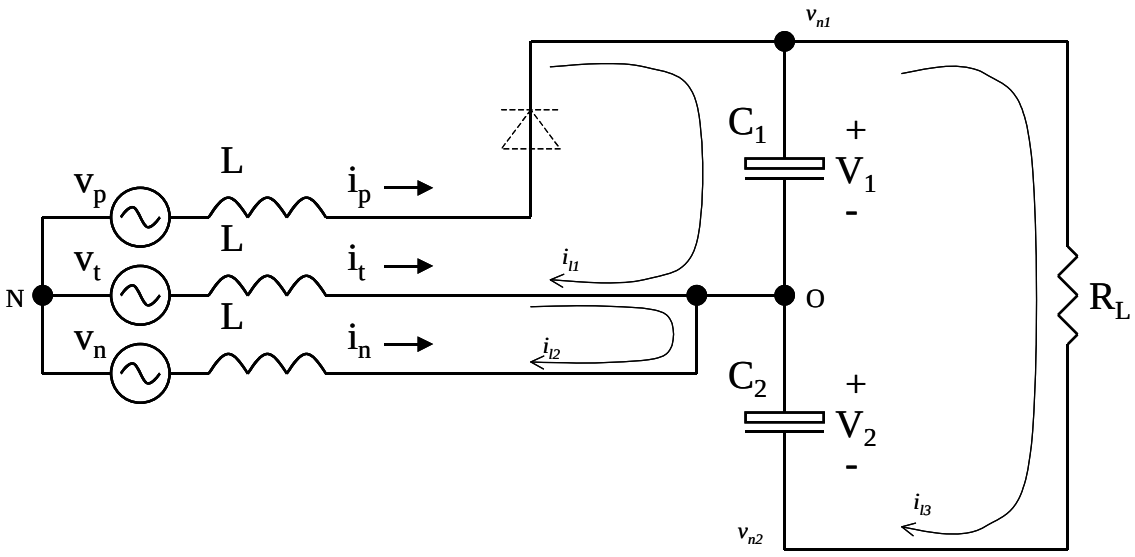



**Figure 3.4.** Model of the VIENNA rectifier for the period $t \in [t_0 + d_P T_{SW}\,;\, t_0 + d_N T_{SW})$.

For this time interval switches $S_t$ and $S_n$ are on, and $S_p$ is open. Diode $D_p$ is conducting, transferring the energy stored in the inductors ($L_p$ and $L_t$) during the previous cycle to $C_1$. S-domain voltage equations for the two current loops $i_{l1}$ and $i_{l2}$ are obtained as follow:

$$-V_p + sLi_p - sLi_t + V_t + v_1 = 0 \tag{3.18}$$

$$-V_t + sLi_t - sLi_n + V_n = 0 \tag{3.19}$$

Substituting (3.3) and (3.4) into (3.18) and (3.19), and eliminating $si_t$, $sV_t$, $V_t$ and $i_t$, yields:

$$si_p = -v_1\frac{2}{3L} + \frac{V_p}{L} \tag{3.20}$$

$$si_n = v_1\frac{1}{3L} + \frac{V_n}{L} \tag{3.21}$$

With reference to voltage node $v_{n1}$ the following equation (in Laplace form) is obtained:

$$i_p + sCv_1 = i_{l3} \tag{3.22}$$

With reference to current loop $i_{l3}$ the following equation (in Laplace form) is obtained:

$$v_1 + v_2 = i_{l3}R_L \tag{3.23}$$

Substituting (3.23) into (3.22) and solving for $sv_1$ yields:

$$sv_1 = i_p\frac{1}{C} - \frac{v_1}{CR_L} - \frac{v_2}{CR_L} \tag{3.24}$$

From figure 3.4 it can be seen that the current through $C_2$ will be equal to $i_{l3}$. Thus, from equation (3.23) the state variable equation for the voltage over capacitor $C_2$ will be:

$$\begin{aligned} sv_2 &= \frac{i_{l3}}{C} \\ &= \frac{\frac{(v_1 + v_2)}{R_L}}{C} \\ &= -\frac{v_1}{CR_L} - \frac{v_2}{CR_L} \end{aligned} \tag{3.25}$$

Substituting (3.14), (3.25), (3.24), (3.21) and (3.20) into (3.13) yields an expression for the state coefficient matrix:

$$a_2 = \begin{bmatrix} 0 & 0 & -\frac{2}{3L} & 0 \\ 0 & 0 & \frac{1}{3L} & 0 \\ \frac{1}{C} & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \\ 0 & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \end{bmatrix} \tag{3.26}$$

An expression for the source coefficient matrix is obtained as:

$$b_2u = \begin{bmatrix} \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 \end{bmatrix}^T \tag{3.27}$$

From figure 3.4 it is evident that (3.12) is still valid, thus:

$$c_2 = c_1 \tag{3.28}$$

*III. Model analysis for $t \in [t_0 + d_N T_{SW}\,;\, t_0 + T_{SW})$, $d_N > d_P$*

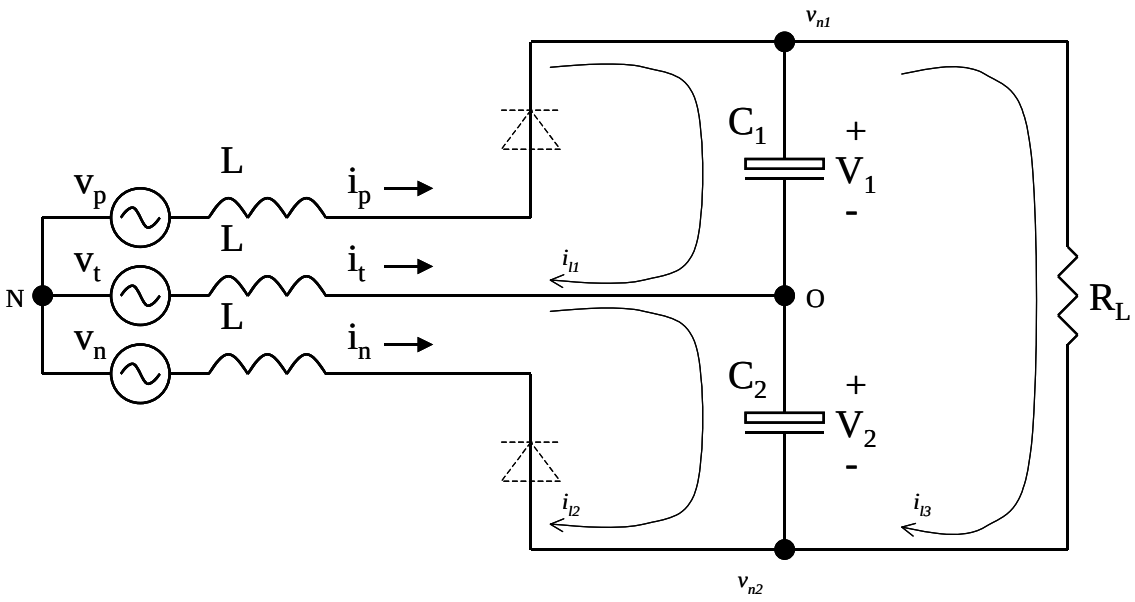



**Figure 3.5.** Model of the VIENNA rectifier for the period $t \in [t_0 + d_N T_{SW}\,;\, t_0 + T_{SW})$.

For this time interval only switches $S_t$ is on, and both $S_n$ and $S_p$ are open. Diodes $D_p$ and $D_n$ are conducting, transferring the energy stored in the inductors during the previous cycles to $C_1$ and $C_2$ respectively. S-domain voltage equations for the two current loops $i_{l1}$ and $i_{l2}$ are obtained as follow:

$$-V_p + sLi_p - sLi_t + V_t + v_1 = 0 \tag{3.29}$$

$$-V_t + sLi_t - sLi_n + V_n + v_2 = 0 \tag{3.30}$$

Substituting (3.3) and (3.4) in (3.29) and (3.30), and eliminating $si_t$, $sV_t$, $V_t$ and $i_t$, yields:

$$si_p = -v_1\frac{2}{3L} - v_2\frac{1}{3L} + \frac{V_p}{L} \tag{3.31}$$

$$si_n = v_1\frac{1}{3L} + v_2\frac{2}{3L} + \frac{V_n}{L} \tag{3.32}$$

With reference to voltage node $v_{n1}$ the following equation (in Laplace form) is obtained:

$$i_p - sCv_1 = i_{l3} \tag{3.33}$$

With reference to voltage node $v_{n2}$ the following equation (in Laplace form) is obtained:

$$i_n + sCv_2 = -i_{l3} \tag{3.34}$$

Equation (3.23) is also valid and holds for this time interval. Substituting (3.33) into (3.23) again yields the same result as in (3.22):

$$sv_1 = i_p \frac{1}{C} - \frac{v_1}{CR_L} - \frac{v_2}{CR_L} \tag{3.35}$$

Substituting (3.32) into (3.21) and solving for $sv_2$ yields:

$$sv_2 = -i_n \frac{1}{C} - \frac{v_1}{CR_L} - \frac{v_2}{CR_L} \tag{3.36}$$

Substituting (3.14), (3.36), (3.35), (3.31) and (3.32) into (3.13) yields an expression for the state coefficient matrix:

$$a_3 = \begin{bmatrix} 0 & 0 & -\frac{2}{3L} & -\frac{1}{3L} \\ 0 & 0 & \frac{1}{3L} & \frac{2}{3L} \\ \frac{1}{C} & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \\ 0 & -\frac{1}{C} & -\frac{1}{CR_L} & -\frac{1}{CR_L} \end{bmatrix} \tag{3.37}$$

An expression for the source coefficient matrix is obtained as:

$$b_3 u = \begin{bmatrix} \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 \end{bmatrix}^T \tag{3.38}$$

From figure 3.5 it is evident that (3.12) is still valid, thus:

$$c_3 = c_1 \tag{3.39}$$

### 3.2.2 Model analysis for $d_P > d_N$

*I. Model analysis for $t \in [t_0 ; t_0 + d_N T_{SW})$, $d_P > d_N$*

For this period both switches are closed and the resulting model shall be the same as derived in section I of paragraph 3.2.1:

$$a_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \\ 0 & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \end{bmatrix} \tag{3.40}$$

and

$$b_1 u = \begin{bmatrix} \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 \end{bmatrix}^T \tag{3.41}$$

Substituting (3.10) into (3.11) yields:

$$c_1 = \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \tag{3.42}$$

*II. Model analysis for $t \in [t_0 + d_N T_{SW} ; t_0 + d_P T_{SW})$, $d_P > d_N$*

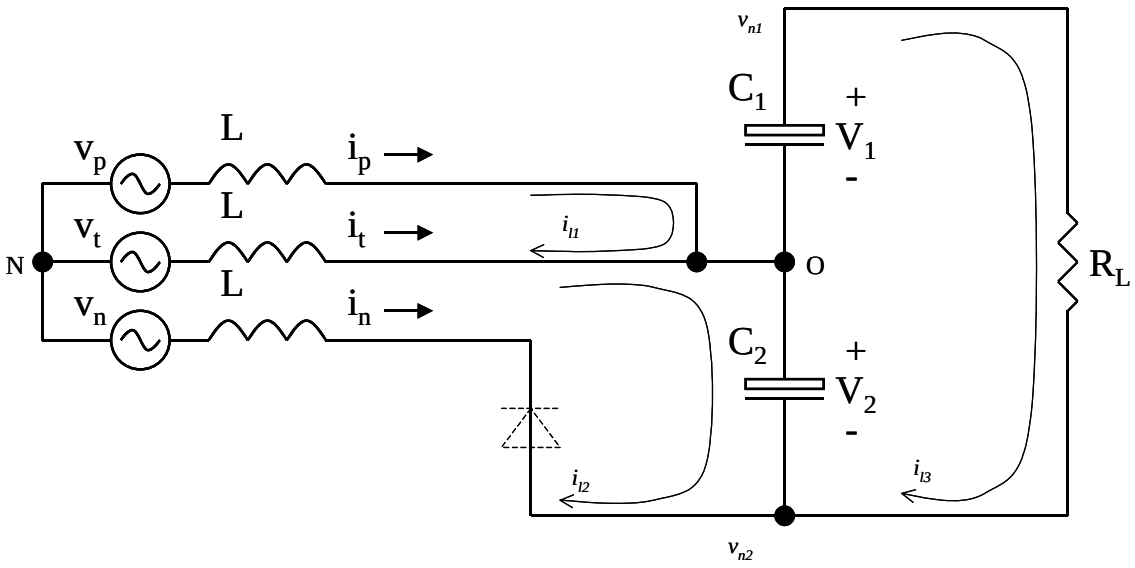



**Figure 3.6.** Model of the VIENNA rectifier for the period $t \in [t_0 ; t_0 + d_N T_{SW})$.

For this time interval switches $S_t$ and $S_n$ are on and $S_p$ is open. Diode $D_p$ is conducting, transferring the energy stored in the inductors ($L_p$ and $L_t$) during the previous cycle to $C_1$. S-domain voltage equations for the two current loops $i_{l1}$ and $i_{l2}$ are obtained as follow:

$$-V_p + sLi_p - sLi_t + V_t = 0 \tag{3.43}$$

$$-V_t + sLi_t - sLi_n + V_n + v_2 = 0 \tag{3.44}$$

Substituting (3.3) and (3.4) in (3.43) and (3.44), and eliminating all off $si_t$, $sV_t$, $V_t$ and $i_t$, yields:

$$si_p = -v_2\frac{1}{3L} + \frac{V_p}{L} \tag{3.45}$$

$$si_n = v_2\frac{2}{3L} + \frac{V_n}{L} \tag{3.46}$$

With reference to voltage node $v_{n2}$ the following equation (in Laplace form) is obtained:

$$-i_n - sCv_2 = i_{l3} \tag{3.47}$$

With reference to current loop $i_{l3}$ the following equation (in Laplace form) is obtained:

$$v_1 + v_2 = i_{l3}R_L \tag{3.48}$$

Substituting (3.48) into (3.47) and solving for $sv_2$ yields:

$$sv_2 = -i_n\frac{1}{C} - \frac{v_1}{CR_L} - \frac{v_2}{CR_L} \tag{3.49}$$

From figure 3.6 it can be seen that the current through $C_1$ will be equal to $i_{l3}$. Thus the state variable equation for the voltage over capacitor $C_1$ will be (substituting equation (3.48)):

$$\begin{aligned} sv_1 &= \frac{-i_{l3}}{C} \\ &= \frac{\frac{(v_1+v_2)}{R_L}}{C} \\ &= -\frac{v_1}{CR_L} - \frac{v_2}{CR_L} \end{aligned} \tag{3.50}$$

Substituting (3.50), (3.49), (3.45), (3.46) and (3.14) into (3.13) yields an expression for the state coefficient matrix:

$$a_2 = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{3L} \\ 0 & 0 & 0 & \frac{2}{3L} \\ 0 & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \\ 0 & \frac{1}{C} & -\frac{1}{CR_L} & -\frac{1}{CR_L} \end{bmatrix} \tag{3.51}$$

An expression for the source coefficient matrix is obtained as:

$$b_2 u = \begin{bmatrix} \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 \end{bmatrix}^T \tag{3.52}$$

From figure 3.6 it is evident that (3.12) is still valid, thus:

$$c_2 = c_1 \tag{3.53}$$

*III. Model analysis for $t \in [t_0 ; t_0 + d_N T_{SW})$, $d_P > d_N$*

For this period both switches are open and the resulting model shall be the same as derived in section III of paragraph 3.2.1:

$$a_3 = \begin{bmatrix} 0 & 0 & -\frac{2}{3L} & -\frac{1}{3L} \\ 0 & 0 & \frac{1}{3L} & \frac{2}{3L} \\ \frac{1}{C} & 0 & -\frac{1}{CR_L} & -\frac{1}{CR_L} \\ 0 & -\frac{1}{C} & -\frac{1}{CR_L} & -\frac{1}{CR_L} \end{bmatrix} \tag{3.54}$$

and

$$b_3 u = \begin{bmatrix} \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 \end{bmatrix}^T \tag{3.55}$$

From figure 3.5 it is evident that (3.12) is still valid, thus:

$$c_3 = c_1 \tag{3.56}$$

## 3.3 AVERAGING, LINEARIZATION, DC-ANALYSIS AND AC-ANALYSIS

*Averaging of state space models*

Before any analysis can be performed on the models obtained in section 3.2.1 and section 3.2.2, a weighted average in terms of the duty cycles must be derived that combines the models obtained in section 3.2.1 and section 3.2.2 into a single model.

When comparing (3.15), (3.26), (3.37), (3.40), (3.51) and (3.54), it is observed that the following part is common only to the positive off-period (1-$d_P$) of the state coefficient matrix of the complete system:

$$a_{(1-d_P)} = \begin{bmatrix} 0 & 0 & -\frac{2}{3L} & 0 \\ 0 & 0 & \frac{1}{3L} & 0 \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.57}$$

When comparing (3.15), (3.26), (3.37), (3.40), (3.51) and (3.54), it is observed that the following part is common to the negative off-period (1-$d_N$) only:

$$a_{(1-d_N)} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{3L} \\ 0 & 0 & 0 & \frac{2}{3L} \\ 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C} & 0 & 0 \end{bmatrix} \tag{3.58}$$

When comparing (3.15), (3.26), (3.37), (3.40), (3.51) and (3.54), it is observed that the following part is common to the whole period:

$$a_{wp} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{R_L C} & -\frac{1}{R_L C} \\ 0 & 0 & -\frac{1}{R_L C} & -\frac{1}{R_L C} \end{bmatrix} \tag{3.59}$$

In combining the models described by equations (3.57) to (3.59), the resulting average model for the state coefficient matrix is obtained as:

$$a = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{R_L C} & -\frac{1}{R_L C} \\ 0 & 0 & -\frac{1}{R_L C} & -\frac{1}{R_L C} \end{bmatrix} + (1-d_N) \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{3L} \\ 0 & 0 & 0 & \frac{2}{3L} \\ 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C} & 0 & 0 \end{bmatrix} +$$

$$(1-d_P) \begin{bmatrix} 0 & 0 & -\frac{2}{3L} & 0 \\ 0 & 0 & \frac{1}{3L} & 0 \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0 & -\frac{2}{3L}(1-d_P) & -\frac{1}{3L}(1-d_N) \\ 0 & 0 & \frac{1}{3L}(1-d_P) & \frac{2}{3L}(1-d_N) \\ \frac{1}{C}(1-d_P) & 0 & -\frac{1}{R_L C} & -\frac{1}{R_L C} \\ 0 & -\frac{1}{C}(1-d_N) & -\frac{1}{R_L C} & -\frac{1}{R_L C} \end{bmatrix} \tag{3.60}$$

From (3.16), (3.27), (3.38), (3.41), (3.52) and (3.55) it is observed that, for the input-state gain matrix, there are no components common to off-periods only, thus so the averaged model for the source coefficient matrix is obtained as:

$$bu = \begin{bmatrix} \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 \end{bmatrix}^T \tag{3.61}$$

From (3.17), (3.27), (3.39), (3.42), (3.53) and (3.56) it is observed that, for the output-state gain matrix, there are no components common to off-periods only, thus the averaged model for the output coefficient matrix is obtained as:

$$c = \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \tag{3.62}$$

*Linearization of state space models*

To analyze the model presented by equations (3.60) to (3.62), it is assumed that the model is under control and is also controllable. To be able to control the system, we are only interested in the small-signal component, or AC-component, of the model presented in equations (3.60) to (3.62). The conditions for oscillation [21] of a system are an open loop

gain of 1 and phase of 180º. It is thus logical that, if the system is prevented from being 180º out of phase and with sufficient gain, the system can be prevented from oscillating. Furthermore if the small-signal component of the model is sufficiently filtered (or compensated), there will be no impact on the DC-component of the system. However to obtain an accurate small-signal model of the system, the system must be under control and thus the analysis must be done at a certain DC level (the input and output constants when the system is or will be under control).

To linearize the system, as described by [18], the state equations are separated into DC and AC terms:

$$\begin{aligned} x &= X + \tilde{x} \\ u &= U + \tilde{u} \\ d &= D + \tilde{d} \end{aligned}, \tag{3.63}$$

and substituted into the model equation (equations (3.60) to (3.62)) respectively.

*DC-analysis of the VIENNA rectifier*

Substituting (3.63) into (3.60), and solving for DC (i.e. all state variable derivatives are zero) yields:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{2}{3L}(1-D_P) & -\frac{1}{3L}(1-D_N) \\ 0 & 0 & \frac{1}{3L}(1-D_P) & \frac{2}{3L}(1-D_N) \\ \frac{1}{C}(1-D_P) & 0 & -\frac{1}{R_L C} & -\frac{1}{R_L C} \\ 0 & -\frac{1}{C}(1-D_N) & -\frac{1}{R_L C} & -\frac{1}{R_L C} \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} \frac{V_p}{L} \\ \frac{V_n}{L} \\ 0 \\ 0 \end{bmatrix} \tag{3.64}$$

Solving equation (3.64) yields:

$$\frac{-2(1-D_p)}{3L}V_1-\frac{(1-D_n)}{3L}V_2=-\frac{V_p}{L} \tag{3.65}$$

$$\frac{(1-D_p)}{3L}V_1+\frac{2(1-D_n)}{3L}V_2=-\frac{V_n}{L} \tag{3.66}$$

$$\frac{(1-D_p)}{C}I_p-\frac{(V_1+V_2)}{R_LC}=0 \tag{3.67}$$

$$\frac{(1-D_n)}{C}I_n-\frac{(V_1+V_2)}{R_LC}=0 \tag{3.68}$$

Rearranging equation (3.65) and substituting into (3.66), and solving yields:

$$V_1=\frac{(2V_p+V_n)}{(1-D_p)} \tag{3.69}$$

$$V_2=-\frac{(V_p+2V_n)}{(1-D_n)} \tag{3.70}$$

Equations (3.69) and (3.70) give the relationship between the input voltages and the output voltages. It can be seen that $D_p$ will be at a minimum when $V_p$ is at a maximum, $V_{p,peak}$, and $V_n = -{}^1/_2 V_{p,peak}$. The minimum output voltage that can be boosted with the VIENNA rectifier (assuming $V_1$ and $V_2$ to be nearly equal) will be when $D_p = 0$:

$$V_{out(\min)} \approx 2\left(2V_{p,\,peak}-\tfrac{1}{2}V_{p,\,peak}\right)=3V_{p,\,peak} \tag{3.71}$$

The equations for the steady state line currents are (from equations. (3.67), (3.68) and (3.4)):

$$I_p=\frac{(V_1+V_2)}{R_L(1-D_p)};\quad D_p\neq 1 \tag{3.72}$$

$$I_n=\frac{(V_1+V_2)}{R_L(1-D_n)};\quad D_n\neq 1 \tag{3.73}$$

By substituting equation (3.72) and equation (3.73) into (3.4), the current for the transitional current $I_t$ is obtained as:

$$I_t=-\frac{(V_1+V_2)}{R_L}\left(\frac{1}{(1-D_p)}+\frac{1}{(1-D_n)}\right) \tag{3.74}$$

From equation (3.72) and (3.73) it is evident that the positive input current $I_p$ is controlled only by $D_p$ and the negative input current $I_n$ only by $D_n$. An important property that emerges from equation (3.69) and equation (3.70) is that the duty cycle for all switches will vary between a lower limit and 1 or, in other words, $D \in [D_{min}, 1)$.

[10] states that the phase voltage can be rewritten in terms of the phase current and an equivalent phase resistance ($R_E$):

$$V_p = I_p R_E, \tag{3.75}$$

$$V_n = I_n R_E, \tag{3.76}$$

If it is assumed that $V_1 = V_2 = E$, and (3.75) and (3.76) is substituted into (3.69) and (3.70) respectively, then it yields:

$$\begin{bmatrix} 1-D_p \\ 1-D_n \end{bmatrix} = \frac{R_E}{E} \begin{bmatrix} 2 & 1 \\ -1 & -2 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \end{bmatrix} \tag{3.77}$$

From [10] the control voltage $V_m$ (output from the error amplifier) can be described as:

$$V_m = \frac{E R_S}{R_E}, \tag{3.78}$$

where $R_S$ is the current sensing resistor. Rearranging (3.78) and substituting into (3.77) yields [10]:

$$\begin{bmatrix} 1-D_p \\ 1-D_n \end{bmatrix} = \frac{R_S}{V_m} \begin{bmatrix} 2 & 1 \\ -1 & -2 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \end{bmatrix} \tag{3.79}$$

Equation (3.79) is the same as derived by [10] and validates the DC-analysis performed. Equation (3.79) also provides the control output for the PWM controller and describes each PWM output in terms of the sensed input currents. By rearranging (3.57) the control voltage is found in terms of the input currents and duty cycles (which is not valid for $D_p$ and $D_n$ equal to 1):

$$V_m = R_S \frac{2I_p + I_n}{1-D_p}; \quad D_p \neq 1 \tag{3.80}$$

$$V_m = R_S \frac{-I_p - 2I_n}{1-D_n}; \quad D_n \neq 1 \tag{3.81}$$

With reference to equations (3.69) and (3.70), it is seen that the automatic equalization of the output capacitor bank theory holds, since the voltage over capacitor $C_1$ is only dependant on the duty cycle $D_p$, and the voltage over $C_2$ is only dependant on the duty cycle $D_n$. Any variation on $I_p$ will result in a change in the duty cycle, which will, in turn, result in a change in $V_1$, for example if $V_1$ is low, but the output voltage is fine. From (3.69) it is evident that the positive duty cycle will increase to compensate for the low bank

voltage. In turn, from (3.72), this will result in an increase in $I_p$. In turn this will result in $C_1$ being boosted more during the next cycle and thus increasing $V_1$.

*AC-analysis of the VIENNA rectifier*

The ac-analysis is the frequency analysis of the system for small signals. As already described above (Section on Linearization), the transfer function obtained with small signal analysis shall provide a basis as to how to control the plant effectively.

From [22] the general form of the system for AC-analysis is given by (with c and bu constant):

$$s\tilde{x} = ca\left(D + \tilde{d}\right)\left(X + \tilde{x}\right) \tag{3.82}$$

$$\therefore \tilde{x} = c\left[sI - A\right]^{-1}\tilde{a}X \tag{3.83}$$

The state coefficient matrix A is the DC component of equation (3.60) with equation (3.63) substituted, and is equal to:

$$A = \begin{bmatrix} 0 & 0 & \frac{-2(1-D_p)}{3L} & \frac{-(1-D_n)}{3L} \\ 0 & 0 & \frac{(1-D_p)}{3L} & \frac{2(1-D_n)}{3L} \\ \frac{(1-D_p)}{C} & 0 & \frac{-1}{R_L C} & \frac{-1}{R_L C} \\ 0 & \frac{-(1-D_n)}{C} & \frac{-1}{R_L C} & \frac{-1}{R_L C} \end{bmatrix} \tag{3.84}$$

The state coefficient matrix a is the AC component of equation (3.60) with equation (3.43) substituted, and is equal to:

$$\tilde{a} = \begin{bmatrix} 0 & 0 & \frac{2\tilde{d}_p}{3L} & \frac{\tilde{d}_n}{3L} \\ 0 & 0 & -\frac{2\tilde{d}_p}{3L} & -\frac{2\tilde{d}_n}{3L} \\ \frac{-\tilde{d}_p}{C} & 0 & 0 & 0 \\ 0 & \frac{-\tilde{d}_n}{C} & 0 & 0 \end{bmatrix} \tag{3.85}$$

The state coefficient matrix X is the DC component of equation (3.61) with equation (3.63) substituted, and is equal to:

$$X = \begin{bmatrix} I_p & I_n & V_1 & V_2 \end{bmatrix}^T \tag{3.86}$$

It will be shown later how to derive the DC constants used in equation (3.86).

From [23] the inverse of a matrix can be calculated as follows:

$$[sI - A]^{-1} = \frac{adj(sI - A)}{\det(sI - A)} \tag{3.87}$$

Substituting (3.84) into (3.87) and solving yields:

$$[sI - A]^{-1} = G\frac{\begin{vmatrix} \gamma_{11} & \gamma_{12} & \gamma_{13} & \gamma_{14} \\ \gamma_{21} & \gamma_{22} & \gamma_{23} & \gamma_{24} \\ \gamma_{31} & \gamma_{32} & \gamma_{33} & \gamma_{34} \\ \gamma_{41} & \gamma_{42} & \gamma_{43} & \gamma_{44} \end{vmatrix}}{\Delta}, \tag{3.88}$$

where

$$G = 3C^2L^2R_L$$

$$\Delta = s^4\left(3C^2L^2R_L\right) + s^3\left(4CLR_L + \right) + s^2(4LR_LC - 4LD_pR_LC - 4LD_nR_LC + 2LD_n{}^2R_LC + 2LD_p{}^2R_LC) + s(2L - 2LD_p - 2LD_n + 2LD_n{}^2 + 2LD_p{}^2 - 2LD_nD_p) + (R_L + 4R_LD_nD_p - 2R_LD_p - 2R_LD_n + R_LD_n{}^2 - 2R_LD_n{}^2D_p - 2R_LD_p{}^2D_n + R_LD_n{}^2D_p{}^2 + R_LD_p{}^2)$$

$$\gamma_{11} = \frac{s^3(3C^2LR_L) + s^2(6CL) + s(2R_LC - 4D_nR_LC + 2D_n{}^2R_LC)}{3C^2LR_L} + \frac{(1 + D_p - 3D_n - D_nD_p + 2D_n{}^2R_LC + 2D_n{}^2)}{3C^2LR_L}$$

$$\gamma_{12} = \frac{-1 + D_n}{3C^2LR_L}\frac{s(-R_LC + D_nR_LC) + (1 - 2D_p + D_n)}{1}$$

$$\gamma_{13} = \frac{s^2(-2LR_LC + 2LD_pR_LC) + s(-2LR_LC - L + 2LD_p - LD_n)}{3CL^2R_L} + \frac{(-RL + R_LD_p + 2R_LD_n - 2R_LD_nD_p - R_LD_n{}^2 + R_LD_n{}^2D_p)}{3CL^2R_L}$$

$$\gamma_{14} = \frac{s^2(-R_LC + D_nR_LC) + s(1 - 2D_pD_n)}{3CLR_L}$$

$$\gamma_{21} = \frac{-1 + D_p}{3C^2LR_L}\frac{s(-R_LC + D_pR_LC) + (1 - 2D_n + D_p)}{1}$$

$$\gamma_{22} = \frac{s^3(3C^2LR_L) + s^2(6CL) + s(2R_LC - 4D_pR_LC + 2D_p{}^2R_LC) + (1 - 3D_p + D_n + 2D_p{}^2 - D_nD_p)}{3C^2LR_L}$$

$$\gamma_{23} = -\frac{s^2(-R_L C + D_p R_L C) + s(1 + D_p - 2D_n)}{3CLR_L}$$

$$\gamma_{24} = \frac{s^2(-2LR_L C + 2LD_n R_L C) + s(-L - LD_p + 2LD_n)}{3CL^2 R_L} + \frac{(-R_L + R_L D_n + 2R_L D_p - 2R_L D_n D_p - R_L {D_p}^2 + R_L D_n {D_p}^2)}{3CL^2 R_L}$$

$$\gamma_{31} = -\frac{-1 + D_p}{3C^2 LR_L} \frac{s^2(3LR_L C) + s(3L) + (2R_L - 4R_L D_n + 2R_L {D_n}^2)}{1}$$

$$\gamma_{32} = -\frac{-1 + D_n}{3C^2 LR_L} \frac{s(3L) + (R_L - R_L D_n - R_L D_p + R_L D_n D_p)}{1}$$

$$\gamma_{33} = \frac{s^3(3LR_L C) + s^2(3L) + s(2R_L - 4R_L D_n + 2R_L {D_n}^2)}{3CLR_L}$$

$$\gamma_{34} = -\frac{s^2(3L) + s(R_L - R_L D_n - R_L D_p + R_L D_n D_p)}{3CLR_L}$$

$$\gamma_{41} = \frac{-1 + D_p}{3C^2 LR_L} \frac{s(3L) + (R_L - R_L D_n - R_L D_p + R_L D_n D_p)}{1}$$

$$\gamma_{42} = \frac{-1 + D_n}{3C^2 LR_L} \frac{s^2(3LR_L C) + s(3L) + (2R_L - 4R_L D_p + 2R_L {D_p}^2)}{1}$$

$$\gamma_{43} = -\frac{s^2(3L) + s(R_L - R_L D_n - R_L D_p + R_L D_n D_p)}{3CLR_L}$$

$$\gamma_{44} = \frac{s^3(3LRLC) + s^2(3L) + s(2R_L - 4R_L D_p + 2R_L {D_p}^2)}{3CLR_L}$$

Substituting (3.88), (3.86) (3.85) and (3.62) into (3.83) and solving yields:

$$T_{p2} = \tilde{v}_2 \begin{bmatrix} \tilde{d}_p \\ \tilde{d}_n \end{bmatrix}^{-1} = \frac{1}{\Delta} \left[ \left( \frac{-\gamma_{43} I_p}{C} + \frac{2\gamma_{41} V_1}{3L} - \frac{\gamma_{42} V_1}{3L} \right) \quad \left( \frac{\gamma_{44} I_n}{C} + \frac{\gamma_{41} V_2}{3L} - \frac{2\gamma_{42} V_2}{3L} \right) \right] \tag{3.89}$$

$$T_{p1} = \tilde{v}_1 \begin{bmatrix} \tilde{d}_p \\ \tilde{d}_n \end{bmatrix}^{-1} = \frac{1}{\Delta} \left[ \left( \frac{-\gamma_{33} I_p}{C} + \frac{2\gamma_{31} V_1}{3L} - \frac{\gamma_{32} V_1}{3L} \right) \quad \left( \frac{\gamma_{34} I_n}{C} + \frac{\gamma_{31} V_2}{3L} - \frac{2\gamma_{32} V_2}{3L} \right) \right] \tag{3.90}$$

$T_{p2}$ is the small-signal plant transfer function for $v_2$ (Capacitor $C_2$) for duty cycle $d_p$ and $d_n$ respectively. $T_{p1}$ is the small-signal plant transfer function for $v_1$ (Capacitor $C_1$) for duty cycle $d_p$ and $d_n$ respectively. The overall plant transfer function is given by $T_{p1} + T_{p2}$, and is equal to:

$$T_p(s) = \tilde{v}_o \begin{bmatrix} \tilde{d}_p \\ \tilde{d}_n \end{bmatrix}^{-1} = \frac{1}{\Delta} \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} \left( \frac{-\gamma_{43} I_p}{C} + \frac{2\gamma_{41} V_1}{3L} - \frac{\gamma_{42} V_1}{3L} \right) & \left( \frac{\gamma_{44} I_n}{C} + \frac{\gamma_{41} V_2}{3L} - \frac{2\gamma_{42} V_2}{3L} \right) \\ \left( \frac{-\gamma_{33} I_p}{C} + \frac{2\gamma_{31} V_1}{3L} - \frac{\gamma_{32} V_1}{3L} \right) & \left( \frac{\gamma_{34} I_n}{C} + \frac{\gamma_{31} V_2}{3L} - \frac{2\gamma_{32} V_2}{3L} \right) \end{bmatrix} \quad (3.91)$$

## 3.4 PWM CONTROLLER TRANSFER FUNCTION

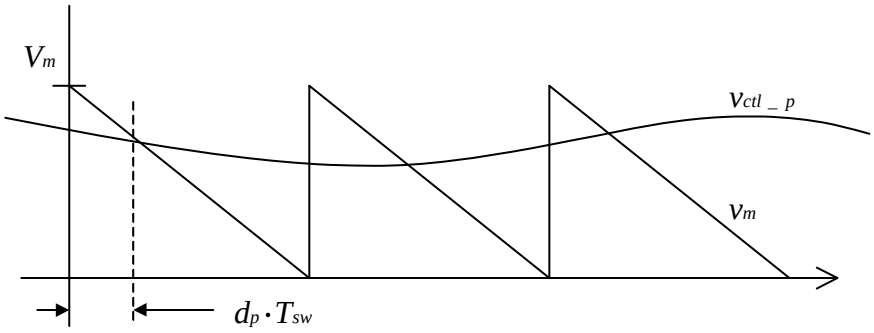



**Figure 3.7.** Duty cycle generator for positive side.

The controller, as described by [10], is shown in figure 3.7. The figure only shows the positive duty cycle generator, but the negative duty cycle generator works on the same principle. It is assumed that there is no variation on $v_m$, the error amplifier output. From figure 3.7 the following expressions are obtained:

$$\frac{v_{ctl\_p}}{(1-d_p)T_{sw}} = \frac{v_m}{T_{sw}}$$
$$\therefore d_p = 1 - \frac{v_{ctl\_p}}{v_m} \tag{3.92}$$

If equation (3.92) is linearized the AC-component is obtained as:

$$D_p + \tilde{d}_p = 1 - \frac{V_{ctl\_p} + \tilde{v}_{ctl\_p}}{V_m}$$
$$\therefore \tilde{d}_p = -\frac{\tilde{v}_{ctl\_p}}{V_m} \tag{3.93}$$

Similarly, the AC component for the negative duty cycle output is obtained as:

$$\therefore \tilde{d}_n = -\frac{\tilde{v}_{ctl\_n}}{V_m} \tag{3.94}$$

where $v_{ctl\_p}$ and $v_{ctl\_n}$ are equal to [10]:

$$v_{ctl\_p} = R_S(2i_p + i_n) \tag{3.95}$$
$$v_{ctl\_n} = R_S(-i_p - 2i_n) \tag{3.96}$$

Equations (3.95) and (3.96) are linear for both AC and DC analysis.

To estimate the currents $i_p$ and $i_n$ equation (3.83) must be recalculated for a corresponding output coefficient matrix, c. For the purpose of this analysis it is assumed that any filtering of the input current signals does not interfere with this analysis (for the filtering not to have an effect on the loop gain/phase, the –3dB cut-off frequency of the filter must be at least an order up on the cross-over frequency and the filter DC-gain must be equal to 1). The controller compensator must also be designed with this in mind. To estimate $i_p$, c is set equal to c = [1 0 0 0]. This yields (from equation (3.83)):

$$\tilde{i}_p \begin{bmatrix} \tilde{d}_p \\ \tilde{d}_n \end{bmatrix}^{-1} = \frac{1}{\Delta}\left[\left(\frac{-\gamma_{13}I_p}{C} + \frac{2\gamma_{11}V_1}{3L} - \frac{\gamma_{12}V_1}{3L}\right) \quad \left(\frac{\gamma_{14}I_n}{C} + \frac{\gamma_{11}V_2}{3L} - \frac{2\gamma_{12}V_2}{3L}\right)\right] \tag{3.97}$$

To estimate $i_n$, c is set equal to c = [0 1 0 0]. This yields (from equation (3.83)):

$$\tilde{i}_n \begin{bmatrix} \tilde{d}_p \\ \tilde{d}_n \end{bmatrix}^{-1} = \frac{1}{\Delta}\left[\left(\frac{-\gamma_{23}I_p}{C} + \frac{2\gamma_{21}V_1}{3L} - \frac{\gamma_{22}V_1}{3L}\right) \quad \left(\frac{\gamma_{24}I_n}{C} + \frac{\gamma_{21}V_2}{3L} - \frac{2\gamma_{22}V_2}{3L}\right)\right] \tag{3.98}$$

Substituting (3.98) and (3.97) into (3.96) and (3.95) yields:

$$\begin{bmatrix} \tilde{v}_{ctl\_p} \\ \tilde{v}_{ctl\_n} \end{bmatrix} \times \begin{bmatrix} \tilde{d}_p \\ \tilde{d}_n \end{bmatrix}^{-1} = \frac{R_S}{\Delta}\begin{bmatrix} 2\tilde{i}_p + \tilde{i}_n \\ -\tilde{i}_p - 2\tilde{i}_n \end{bmatrix} \tag{3.99}$$

From (3.99) the transfer function of the modulator will be:

$$T_m(s) = \begin{bmatrix} \tilde{d}_p \\ \tilde{d}_n \end{bmatrix} \times \begin{bmatrix} \tilde{v}_{ctl\_p} \\ \tilde{v}_{ctl\_n} \end{bmatrix}^{-1} = \left[\frac{R_S}{\Delta}\begin{bmatrix} 2\tilde{i}_p + \tilde{i}_n \\ -\tilde{i}_p - 2\tilde{i}_n \end{bmatrix}\right]^{-1} \tag{3.100}$$

## 3.5 OPEN-LOOP TRANSFER FUNCTION

The feedback gain of the system is inversely proportional to the output voltage and proportional to the reference voltage ($V_{ref}$), and is thus obtained as:

$$T_{fb}(s) = \frac{V_{ref}}{V_{OUT}} \tag{3.101}$$

By multiplying (3.101), (3.100) and (3.91) (as illustrated by [17]), the uncompensated open-loop transfer function of the system is obtained as:

$$T_{ol}(s) = T_{fb}(s)T_p(s)T_m(s) \tag{3.102}$$

A MATLAB script is given in Appendix B for calculating the uncompensated open-loop transfer function. Figure 3.8 shows a block diagramme of the control loop for the VIENNA rectifier. $T_c(s)$ represents the controller compensator used for stabilizing the system.

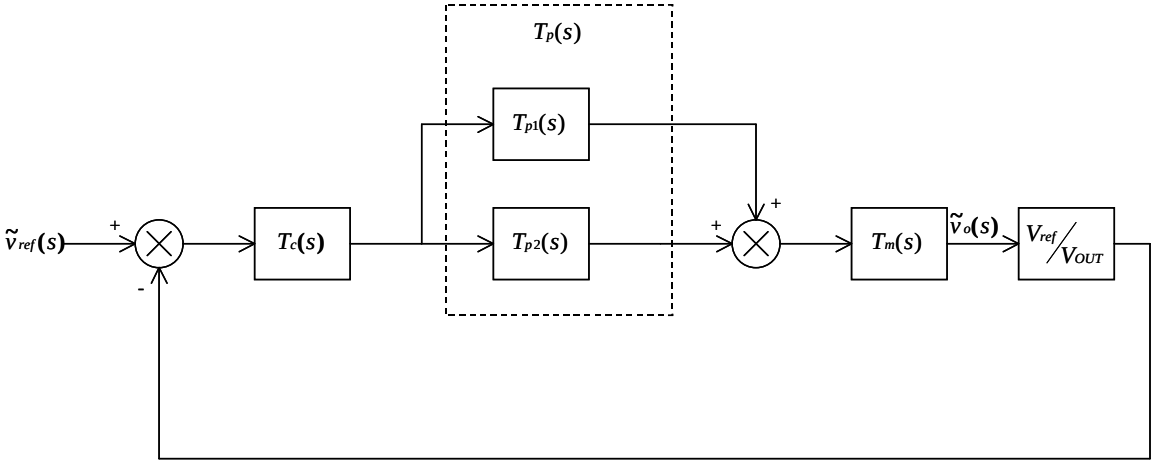



**Figure 3.8.** Controller flow diagram.

## 3.6 APPLICATION OF THE UNCOMPENSATED OPEN-LOOP TRANSFER FUNCTION IN COMPENSATOR DESIGN

The transfer function derived in equation (3.102) will be used to design a compensator to optimally control the VIENNA rectifier. The compensator design used in this thesis will be based on frequency response design techniques [24]. All frequency response design techniques revolve around the control of the phase margin of the compensated open-loop transfer. The relationship between the phase-margin and the transient response will be shown in this section.

Figure 3.9 shows a typical uncompensated bode plot of the open-loop transfer function of a VIENNA rectifier. From this bode-plot it can be seen that the drop-off between 200 rad/s and 10 krad/s is approximately -20dB/decade. This frequency range is identified as being ideal for implementing the crossover (where the compensated open-loop gain is equal to 0dB), since the gain drop-off is –20dB/decade (which makes it ideal for a Type II compensator [25]).

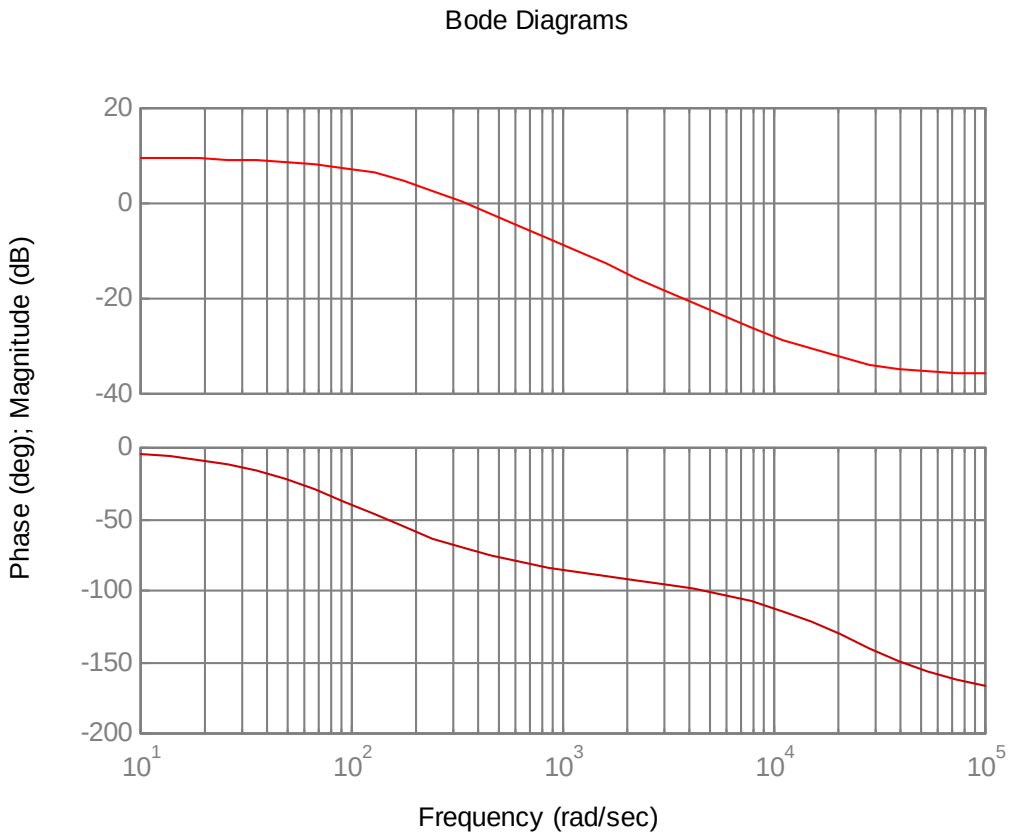



**Figure 3.9.** Uncompensated open-loop transfer function of a VIENNA rectifier, operating with a constant switching frequency.

[24] states that an optimal control design will be for a phase margin (PM) of 45º-60º, and a gain margin of more than 6dB. [25] states that the crossover frequency must be chosen at least an order below the switching frequency which is, in this case, 50kHz. The crossover frequency was chosen to be 1 krad/s, and the required phase margin 60º. The phase response will change as the output load changes and thus the choice of crossover frequency will have an impact on system performance. For illustration purposes the crossover frequency was simply chosen to be 1 krad/s.

From [25] a suitable controller will be a Type II, since the uncompensated open-loop drop-off is –20dB/decade. The required compensator phase boost, for a Type II compensator, is calculated to be [17]:

$$boost = -\left(90 - PM + \phi_{ol}\right), \tag{3.103}$$

where $\phi_{ol}$ is the phase of the uncompensated open-loop transfer function.

From figure 3.6 $\phi_{ol}$ = -87.5° at the desired crossover frequency. Thus, the required phase boost from equation (3.103) is equal to 57.5°. From [25] it is also clear that a Type II compensator will be sufficient for compensating the system, since a Type II compensator can only boost the phase up to 90°. The design of a compensator will be discussed in more detail in the next Chapter. The resulting compensator gain and phase response (bode plots) are, however, shown in figure 3.10.

The compensated open-loop transfer function is given by:

$$T_{ol}(s) = T_{fb}(s)T_p(s)T_m(s)T_c(s) \tag{3.104}$$

The compensated open-loop gain and phase response is shown in figure 3.11. From figure 3.11 it can be seen that the phase margin will be approximately 59.5º, with a crossover frequency of 962.7 rad/s. The gain margin of 27.1dB is more than the 6dB required for stability and, thus, the system will be stable.

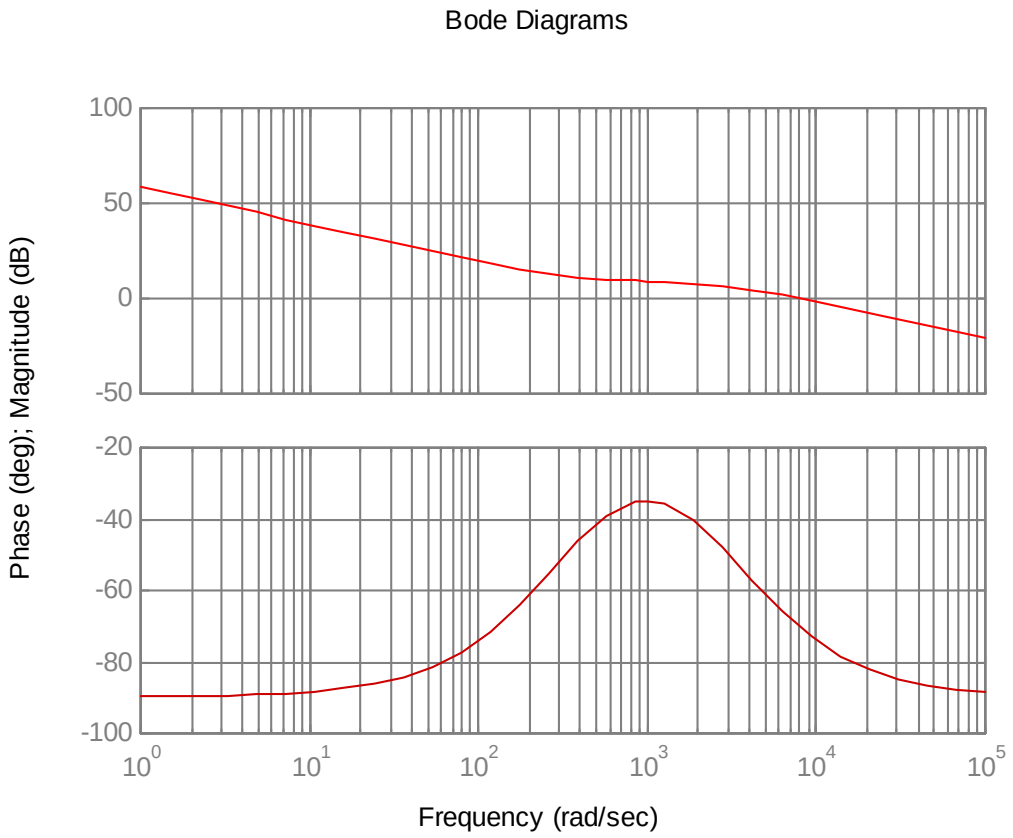



**Figure 3.10.** Bode-plot of compensator transfer function.

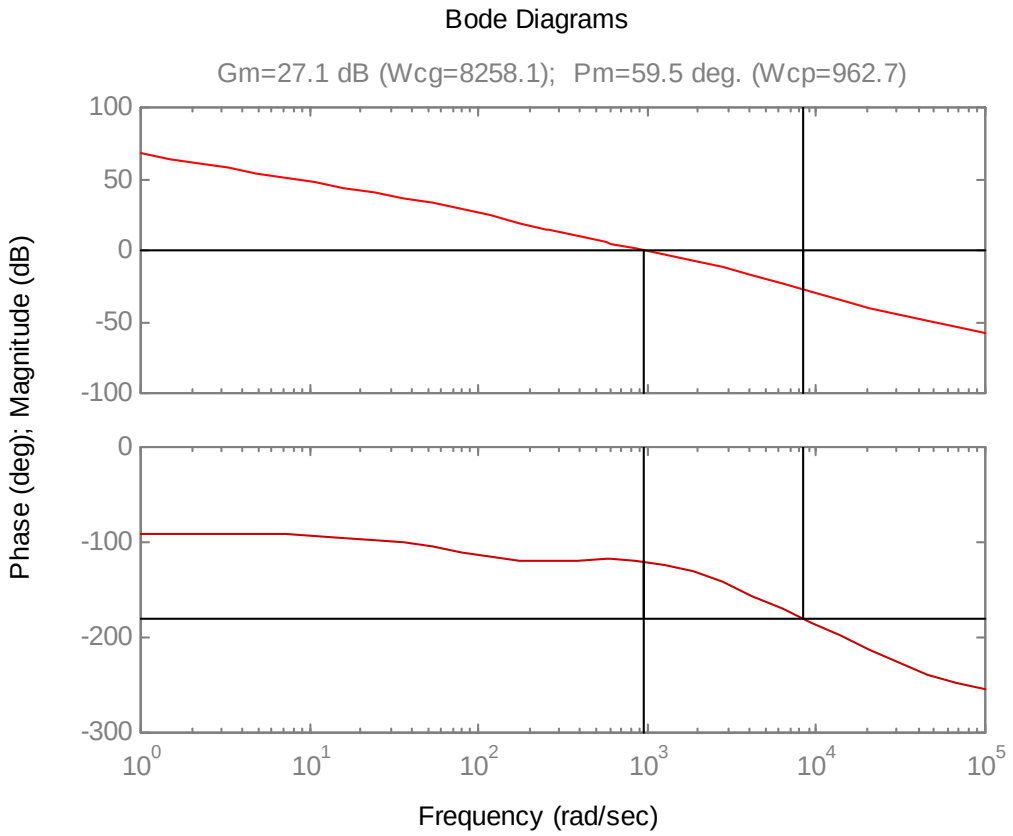



**Figure 3.11.** Compensated open-loop function of a VIENNA rectifier, operating with a constant switching frequency.

A digital simulation was performed on the sample system, with the following specifications:

- L = 3.15mH
- C = 66µF
- Input voltage = 176V line-to-line
- Full load on output = 1kW
- Output voltage = 700V

A 50% load step (from half loading on the output to full loading) was introduced into the system at 20ms, after the output voltage had settled, and the voltage overshoot recorded. The resulting graph of the output is shown in figure 3.12.

For figure 3.12 the voltage overshoot for the load change was approximately -40V or equal to:

$$\%OS = \frac{|-40|}{700} \times 100 = 5.714\% \tag{3.105}$$

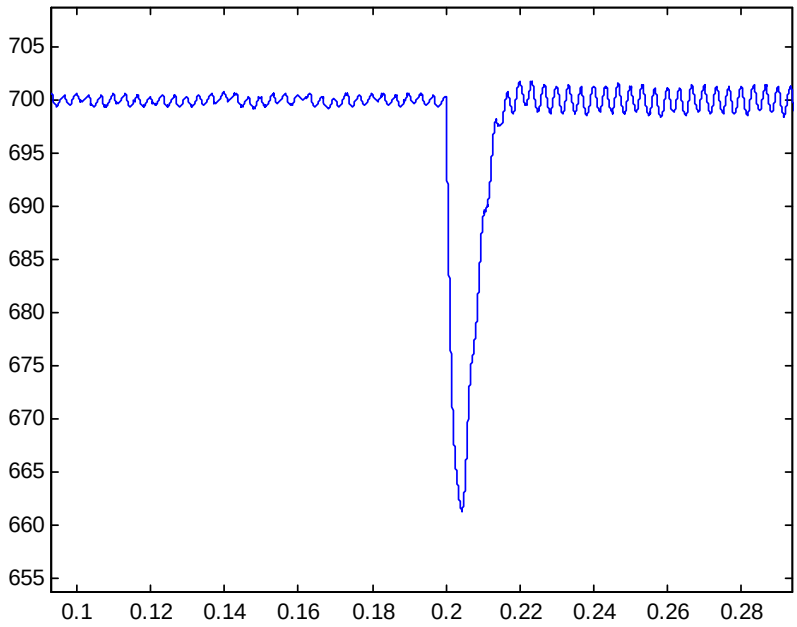



**Figure 3.12.** Simulated output of the VIENNA Rectifier.

From [26], if the overshoot/undershoot of the system output is known the damping ratio can be calculated as:

$$\begin{aligned}\zeta &= \frac{-\ln\left(\frac{\%OS}{100}\right)}{\sqrt{\pi^2 + \ln^2\left(\frac{\%OS}{100}\right)}} \\ &= 0.673\end{aligned} \tag{3.106}$$

Also from [19], if the damping ratio of the system is known the phase margin can be calculated as:

$$\begin{aligned}\Phi_M &= \tan^{-1}\frac{2\zeta}{\sqrt{-2\zeta^2 + \sqrt{1+4\zeta^4}}} \\ &= 63.68°\end{aligned} \tag{3.107}$$

From the above results it can be seen that, by designing the control loop using frequency response techniques and for a given phase margin, the transient output of the system can be predicted and *vice versa*.

# CHAPTER 4

# DESIGN OF THE VIENNA RECTIFER

## 4.1 FILTER DESIGN: INPUT INDUCTOR

For the purpose of the inductor analysis it is assumed that $D_p > D_n$. This implies that the positive side inductance ($L_p$) is charged for the period $D_pT_{sw}$ and discharged for the period $(1\text{-}D_p)T_{sw}$. The waveform for the current through $L_p$ is shown in figure 4.1. This waveform was obtained by considering the time-domain behaviour of the VIENNA rectifier model as discussed in section 3.1 of Chapter 3. The VIENNA rectifier is shown in figure 2.18 for reference purposes. Figure 4.2 shows the equivalent or plant control model for the VIENNA rectifier.

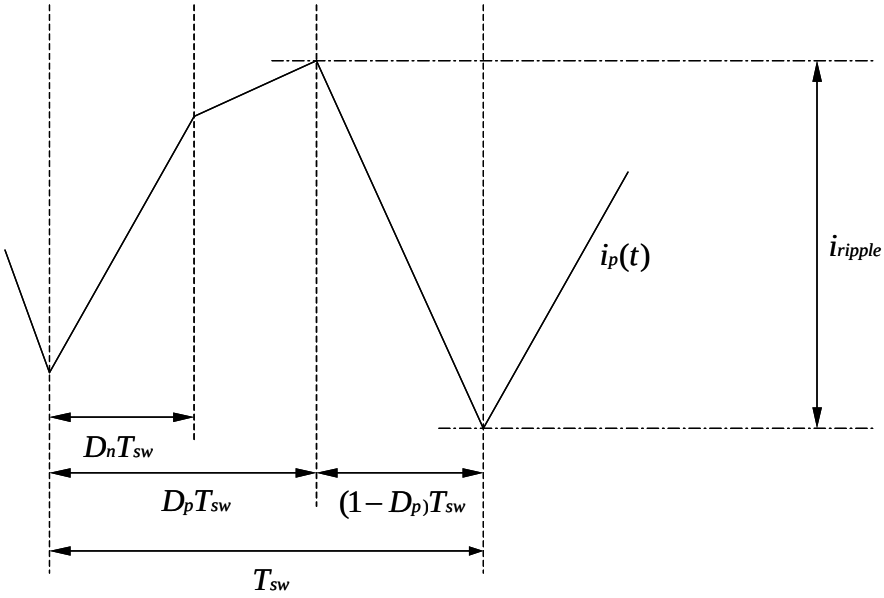



**Figure 4.1.** Positive side current waveform for $D_p > D_n$.

From figure 4.1 it can be seen that the current ripple is the current drop during the off cycle ($(1\text{-}d_p)\cdot T_{sw}$). From [27], with reference to figure 4.2, the node voltages are:

$$V_{P'O} = v_1 \tag{4.1a}$$

$$V_{N'O} = -v_2 \tag{4.1b}$$

$$V_{T'O} = 0 \tag{4.1c}$$

$$V_{P'N} = V_{P'O} - \tfrac{1}{3}\left(V_{P'O} + V_{T'O} + V_{T'O}\right) = \tfrac{2}{3}v_1 + \tfrac{1}{3}v_2 \tag{4.1d}$$

$$V_{N'N} = V_{N'O} - \tfrac{1}{3}\left(V_{P'O} + V_{T'O} + V_{T'O}\right) = -\tfrac{1}{3}v_1 - \tfrac{2}{3}v_2 \tag{4.1e}$$

$$V_{T'N} = V_{T'O} - \tfrac{1}{3}\left(V_{P'O} + V_{T'O} + V_{T'O}\right) = -\tfrac{1}{3}v_1 + \tfrac{1}{3}v_2 \tag{4.1f}$$

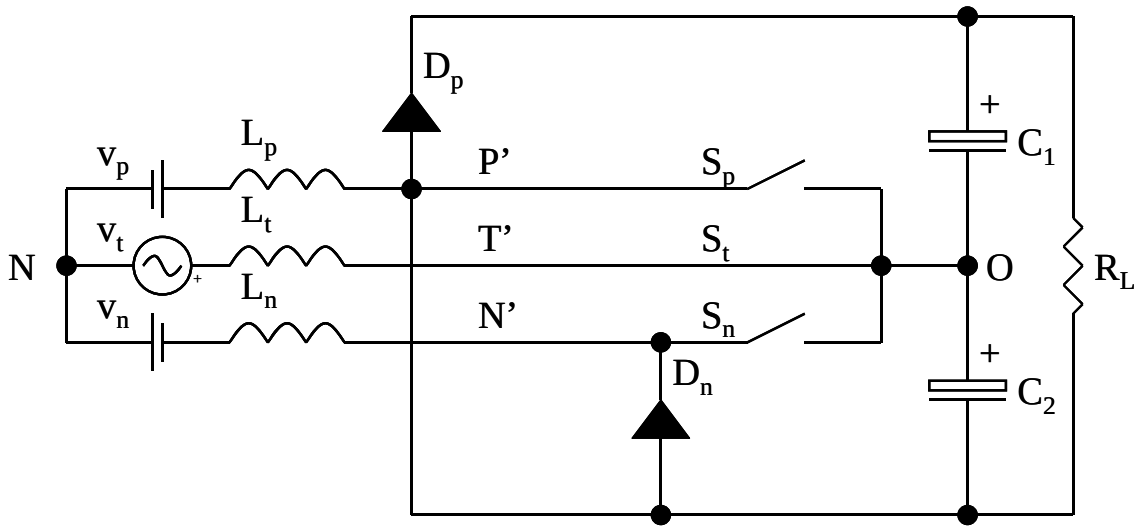



**Figure 4.2.** Equivalent model of the VIENNA rectifier for constant frequency operation.

Assuming that the voltage ripple is small (in other words C is large), the current waveform can be described mathematically during the off cycle, ((1-$D_p$)$T_{sw}$), as [28]:

$$\begin{aligned} i_p(t) &= i_{p0} + \frac{1}{L}\int_{D_pT_{sw}}^{T_{sw}} V_{differential}\,dt \\ &= i_{p0} + \frac{1}{L}\int_{D_pT_{sw}}^{T_{sw}} -\left(V_p(t) - E\right)dt \\ &= i_{p0} - \frac{\left(V_p(t) - E\right)\left(1 - D_p\right)T_{sw}}{L}, \end{aligned} \tag{4.2}$$

where $i_{p0}$ is the starting current (or referred to in the literature as the initial condition or initial current), and $V_{differential}$ is the voltage over the inductor.

The AC current ripple can be computed by substituting the time-period into (4.2):

$$i_{ripple}(t) = -\frac{(V_p(t) - E)(1 - D_p)T_{sw}}{L_p} \tag{4.3}$$

The positive rail voltage ($V_p$) can be mathematically described as (for a 60° control block, as shown in figure 4.3):

$$V_p = V_{\text{phase, peak}}\cos(k\omega t - 60°); \quad 0° \le \omega t < 120° \tag{4.4}$$

where k is an integer and $V_{phase,peak}$ is the peak phase-to-neutral voltage of the input source. Similarly, the negative side voltage ($V_n$) is:

$$V_n = -V_{\text{phase, peak}}\cos(n\omega t + 0°); \quad -60° \le \omega t < 60° \tag{4.5}$$

Considering the first 60° control block (k = 1 and n = 1) and substituting (4.4) and (4.5) into (3.69), and rearranging yields (for $V_1 = V_2 = E$; thus the system is under control):

$$(1-D_p) = \frac{2V_{\text{phase, peak}}\cos(\omega t - 60) - V_{\text{phase, peak}}\cos(\omega t)}{E} \tag{4.6}$$

Substituting (4.6) into (4.3), the maximum current ripple can be computed by solving the differential equation of (4.3) with respect to time:

$$\begin{aligned} 0 &= \frac{d}{dt}\left(i_{ripple}(t)\right) \\ &= \frac{d}{dt}\left(\frac{2V_{phase,\,peak}\cos(\omega t - 60) - V_{phase,\,peak}\cos(\omega t)}{E}\,\frac{(V_{phase,\,peak}\cos(\omega t - 60) - E)}{L}\right) \end{aligned} \tag{4.7}$$

When solving equation (4.7), (using MATLAB) it is found that the maximum current ripple will coincide with ωt = 30°, or equivalently:

$$V_p = 0.866V_{\text{phase, peak}} \quad \text{for all k}, \tag{4.8}$$

and also:

$$V_n = -0.866V_{\text{phase, peak}} \quad \text{for all n} \tag{4.9}$$

Substituting (4.6), (4.8) and (4.9) into (4.3) yields the maximum current ripple:

$$i_{ripple,\,\max} = -\frac{0.866V_{phase,\,peak}}{E}\,\frac{(0.866V_{phase,\,peak} - E)T_{sw}}{L} \tag{4.10}$$

When rearranging (4.10), the inductance needed for a certain amount of current ripple is thus:

$$L = -\frac{0.866V_{phase,\,peak}}{E}\,\frac{(0.866V_{phase,\,peak} - E)T_{sw}}{i_{ripple,\,\max}} \tag{4.11}$$

From equation (4.8), (4.9) and (4.10), it can be seen that the maximum ripple current will occur when the transitional voltage ($V_t$), and thus the transitional current ($I_t$), is equal to zero (refer to figure 3.1). From equation (4.11) the input inductance required could be calculated for a certain amount of current ripple at 0.866 of the peak phase voltage, where the peak-to-peak current ripple will be at a maximum.

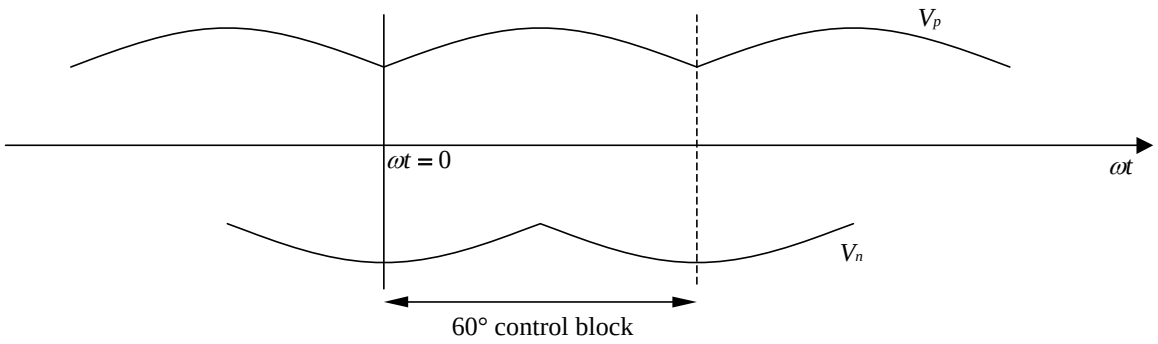



**Figure 4.3.** Positive and negative side voltages versus period.

## 4.2 FILTER DESIGN: OUTPUT CAPACITOR

For the capacitive output filter analysis the period ωt ≡ [-30°,0°) is considered (refer to figure 3.1). For the analysis the ESR of the output capacitors is assumed to be very small and thus that the line frequency ripple will be dominant. The analysis used in this section assume capacitors $C_1$ and $C_2$ are identical, with a capacitance equal to C.

For the period ωt ≡ [-30°,0°), $D_p < D_n$, and hence so will $|I_n| < |I_p|$. Assuming that the output current is constant (i.e. the load is not resistive), the voltage drop at 0° over the capacitors due to discharge will be [28]:

$$v_{C2,\,discharge} = v_{C1,\,discharge} = \frac{1}{C}\int_0^{T_L\frac{30}{360}} |I_{OUT}|dt = \frac{30}{360} I_{OUT} T_L\,, \tag{4.12}$$

where $T_L$ is the period of the input three-phase source, C the output capacitance and $I_{OUT}$ the output current. It is assumed that the input current waveforms are sinusoidal. For the period ωt ≡ [-30°, 0°) capacitor $C_2$ will be charged by the negative side input inductor current, and at 0° capacitor $C_2$ will be charged by:

$$v_{C2,\,charge} = \frac{1}{C}\left|\int_{t0+DnTsw}^{t0+Tsw} i_n(t)dt + \int_{t1+DnTsw}^{t2+Tsw} i_n(t)dt + \int_{t2+DnTsw}^{t2+Tsw} i_n(t)dt + \mathrm{K}\right|_{\omega t=-30°}^{\omega t=0°} \tag{4.13}$$

For the period ωt ≡ [-30°, 0°) the negative side current can be described mathematically as:

$$i_n(t) = -i_{\text{phase, peak}} \cos\left(\frac{2\pi}{T_L}\left(t - \frac{60T_L}{360}\right)\right), \tag{4.14}$$

where $i_{phase,peak}$ is the peak phase-to neutral current, and is equal to [29]:

$$i_{phase,\,peak} = \sqrt{2}\,\frac{P_{OUT}}{3V_{phase,\,rms}} \tag{4.15}$$

Substituting (4.14) into (4.13) yields an expression for the change in voltage of capacitor $C_2$ as:

$$v_{C2,\,charge} = \frac{-T_L}{2\pi C}\left[\begin{array}{l} -i_{phase,\,peak}\sin\left(\frac{2\pi}{T_L}\left(t-\frac{60T_L}{360}\right)\right)\Big|_{D_nT_{sw}}^{T_{sw}} \\ -i_{phase,\,peak}\sin\left(\frac{2\pi}{T_L}\left(t-\frac{60T_L}{360}\right)\right)\Big|_{T_{sw}+D_nT_{sw}}^{2T_{sw}} + \mathrm{K} \end{array}\right] \tag{4.16}$$

Simplifying (4.16) and also setting $t = xT_{sw}$ (thus assuming the switching frequency to be very high) yields:

$$v_{C2,\,charge} = \left|\frac{-T_L i_{phase,\,peak}}{2\pi C}\sum_{x=0}^{y}\left[\begin{array}{l} \sin\left(\frac{2\pi T_{sw}}{T_L}(x+1)-\frac{120\pi}{360}\right)- \\ \sin\left(\frac{2\pi T_{sw}}{T_L}x+\frac{2\pi D_n(x)T_{sw}}{T_L}-\frac{120\pi}{360}\right) \end{array}\right]\right| \tag{4.17}$$

where:

$$y = round\left(\frac{T_L\dfrac{30}{360}}{T_{sw}}\right) \tag{4.18}$$

At the end of the 30° period the voltage over $C_2$ will be equal to:

$$v_{C2} \approx E + v_{C2,\,\mathrm{charge}} - v_{C2,\,\mathrm{discharge}} \tag{4.19}$$

The voltage ripple, at the mid-point between the two capacitors, will be:

$$\begin{aligned} v_{ripple,\,p-p} &= 2\left|E - v_{C2}\right| \\ &= 2\left|v_{C2,\,discharge} - v_{C2,\,charge}\right| \end{aligned} \tag{4.20}$$

Substituting (4.12) and (4.17) into (4.20) yields an expression for the output capacitance in terms of input and output current, and voltage ripple:

$$C = \frac{2\left| I_{OUT}T_L\frac{30}{360} - \left| i_{phase,\,peak}\frac{T_L}{2\pi}\sum_{x=0}^{y}\left[\begin{array}{l}\sin\left(\frac{2\pi T_{sw}}{T_L}(x+1)-\frac{120\pi}{360}\right)- \\ \sin\left(\frac{2\pi T_{sw}}{T_L}x+\frac{2\pi D_n(x)T_{sw}}{T_L}-\frac{120\pi}{360}\right)\end{array}\right]\right|\right|}{v_{ripple,\,p-p}} \tag{4.21}$$

Figure 4.4 shows the voltage ripple as a function of ωt.

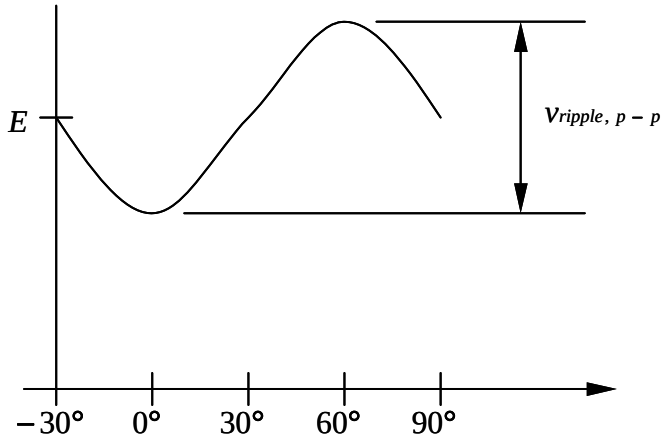



**Figure 4.4.** Voltage waveform over $C_2$ versus ωt.

With reference to figure 4.4 the voltage ripple can be described using the expression:

$$v_{ripple}(t) = -\frac{v_{ripple,\,p-p}}{2}\sin\left(\frac{t\pi}{T_L\frac{30}{360}}\right) \tag{4.22}$$

The voltage over capacitor $C_2$ will thus be:

$$V_2 = E - v_{ripple}(t) \tag{4.23}$$

For the period ωt ≡ [-30°, 0°), from equations (4.4) and (4.5):

$$V_p(t) = V_{phase,\,peak}\cos\left(t\frac{2\pi}{T_L}\right) \tag{4.24}$$

$$V_n(t) = -V_{phase,\,peak}\cos\left(\left(t - T_L\frac{60}{360}\right)\frac{2\pi}{T_L}\right) \tag{4.25}$$

Substituting (4.25), (4.24) and (4.23) into (3.69), and setting $t = xT_{sw}$ yields:

$$D_n(x) = 1 + \frac{-2V_{phase,\,peak}\cos\left(\left(xT_{sw} - T_L\frac{60}{360}\right)\frac{2\pi}{T_L}\right) + V_{phase,\,peak}\cos\left(\left(xT_{sw}\right)\frac{2\pi}{T_L}\right)}{E - \frac{v_{ripple,\,p-p}}{2}\sin\left(xT_{sw}\frac{360\pi}{30T_L}\right)} \tag{4.26}$$

One observation from figure 4.4 is that the voltage ripple (mid-point voltage) is at three times the line frequency.

## 4.3 VIENNA RECTIFIER: POWER STAGE DESIGN

A 1kW prototype rectifier is proposed with the following specifications:

- The prototype rectifier shall be able to supply rated power at $V_{LL}$ = 220V (line-to-line) input voltage, with a line frequency of 50Hz;
- To accommodate a generator type input the prototype rectifier shall be able to supply up to 500W output power at 110V (line-to-line) input voltage, linearly derated from an input voltage of 220V (line-to-line) and output power of 1kW (i.e. for an input of 154V, or 70% of 220V, the prototype rectifier shall be able to supply up to 700W);
- To accommodate non-generator inputs, the prototype shall be able to supply rated power at 220V (line-to-line) input with a ±20% variation in input voltage (i.e. the prototype shall be able to supply 1kW for an input of 176V up to 264V);
- The peak-to-peak input current ripple should be below 10% of the peak current current at rated output power and an input voltage of 176V (line-to-line).

With a 20% variation in input voltage, the peak line-to-neutral input voltage is equal to (reference [28]):

$$\begin{aligned} V_{phase,\,peak} &= \sqrt{2}\left(\frac{V_{LL,\,\max,\,rms}}{\sqrt{3}}\right) \\ &= \sqrt{2}\left(\frac{(220+220\times 0.2)}{\sqrt{3}}\right) \\ &= 215.55V \end{aligned} \tag{4.27}$$

Substituting (4.24) into (3.71), the minimum output voltage is:

$$\begin{aligned} V_{out,\,\min} &= 3V_{phase,\,peak} \\ &= 646.65V \end{aligned} \tag{4.28}$$

For convenience the output voltage is chosen as 700V. The minimum voltage that can be boosted by either bank is (from equation (3.69), assuming $D_p$ is allowed to be zero):

$$\begin{aligned} V_{1,\,\min} &= \frac{(2V_p + V_n)}{(1-D_p)} \\ &= \frac{(2V_{phase,\,peak} - 0.5V_{phase,\,peak})}{(1-0)} \\ &= 323.325V \end{aligned} \tag{4.29}$$

The allowable ripple voltage ripple for $V_1$ and $V_2$ (the capacitor bank mid-point voltage) is thus equal to (700–2(323.325)) = 53.35V. If the voltage ripple exceeds 53.35V the input diodes will work in forward rectification mode instead of freewheeling mode (i.e. duty cycle $D_p$ or $D_n$ will be zero for extended periods), distorting the input current. The rms phase input current is equal to [29]:

$$i_{phase,\,rms} = \frac{P_{OUT}}{3\left(\frac{V_{LL}}{\sqrt{3}}\right)} \tag{4.30}$$

For rated output power, the input current will be at maximum when the input voltage is at a minimum, or equal to $V_{LL}$ = 176V. Substituting $V_{LL}$ = 176V into (4.30) yields:

$$\begin{aligned} i_{phase,\,rms} &= \frac{1000}{3\times 101.61} \\ &= 3.28A \end{aligned} \tag{4.31}$$

The peak average (i.e. excluding the ripple current) phase input current is equal to:

$$\begin{aligned} i_{phase,\,peak} &= \sqrt{2} i_{phase,\,rms} \\ &= \sqrt{2}\times 3.28 \\ &= 4.64A \end{aligned} \tag{4.32}$$

If $V_{OUT}$ = 700V, then:

$$E = \frac{V_{OUT}}{2} = 350V \tag{4.33}$$

The minimum input voltage, for rated output power of 1000W, is equal to:

$$\begin{aligned} V_{phase,\,peak} &= \sqrt{2} V_{phase,\,rms} \\ &= \sqrt{2}\times 101.61 \\ &= 143.7V \end{aligned} \tag{4.34}$$

From equation (4.32), and the specification set for the maximum allowable input current ripple, it follows that the peak-to-peak current ripple is equal to:

$$\begin{aligned} i_{ripple,\,\max} &= 0.1\times 4.64 \\ &= 0.464A \end{aligned} \tag{4.35}$$

The switching frequency is arbitrarily chosen to be $f_{sw}$ = 50kHz which is about twice the highest audible frequency, or 25kHz. Thus the period of one switching cycle will be equal to $T_{sw} = 1/f_{sw}$ = 20µs. Substituting (4.35), (4.34) and (4.33) into (4.11) yields the desired inductance:

$$L \approx 3.15mH \tag{4.36}$$

Since the line frequency $f_L$ = 50Hz, $T_L = 1/f_L$ = 20ms. Substituting $T_L$ and $T_{sw}$ into (4.18) yields the number of discrete sampling periods per 30º:

$$\begin{aligned} y &= round\left(\frac{0.02\times\frac{30}{360}}{0.00002}\right) \\ &= round(83.33) \\ &= 83 \end{aligned} \tag{4.37}$$

The maximum output current of the rectifier will be:

$$\begin{aligned} I_{OUT} &= \frac{P_{OUT}}{V_{OUT}} \\ &= \frac{1000}{700} \\ &= 1.429A \end{aligned} \tag{4.38}$$

Substituting (4.38), (4.37), (4.34), (4.33) and $v_{ripple,p\text{-}p}$ = 53.35V into equations (4.26) and (4.21), and solving yields:

$$C \geq 46.842\mu F \tag{4.39}$$

A MATLAB script is given in Appendix C for determining the output capacitance of the VIENNA rectifier, as determined above.

From equation (4.20), it is known that the mid-point capacitor voltage ripple is proportional to the discharge current minus the charge current. The capacitor mid-point voltage ripple shall thus decrease, since the discharge current (or output current) decreases with the derated and lower input voltage. Thus with a generator connected at the output, the voltage ripple shall decrease as the input voltage is decreased to a voltage lower than the rated specified input voltage of 220V line-to-line and the output loading is also decreased in a linear manner to the input voltage. The resulting ripple voltage at a reduced input voltage and output loading will be calculated in the next Chapter.

Table 4.1 lists all the relevant parameters of the power stage design under line frequency operation. Since the output is symmetrical around both the positive and the negative duty cycle generators it is convenient to perform the plant analysis with either $D_n$ or $D_p$ set equal to 1. Since the control of this rectifier can be done digitally (i.e. DSP control), the reference voltage is chosen to be half of the operating voltage of the processor to allow for adequate output swing to both rails $V_{ref}$ = 3.3/2 = 1.65V. The equivalent sense resistance is chosen to be:

$$\begin{aligned} R_S &\leq \frac{V_{ref}}{i_{phase,\ peak} + \frac{i_{ripple,\ \max}}{2}} \\ &\leq \frac{1.65}{4.64 + \frac{0.464}{2}} \\ &\leq 0.34\Omega \end{aligned} \tag{4.40}$$

To ensure that there is sufficient headroom, the value for $R_S$ is halved and thus chosen to be 0.17Ω. If an analogue controller is used, a standard bandgap reference can be used with a reference voltage of 2.5V (e.g. the LM4040DIM3-2.5).

If input current sensors are used, the output should be scaled that a (1.65/2) = 0.825V output corresponds to the maximum input current or 4.64 + (0.464/2) = 4.872A.

**Table 4.1.** VIENNA rectifier low-frequency parameters.

| | $P_{OUT}$ | | | | | Comments |
|---|---|---|---|---|---|---|
| | **1kW** | **1kW** | **1kW** | **300W** | **500W** | |
| $V_{LL}$(rms) | 176V | 176V | 220V | 176V | 110V | |
| $V_{p,peak}$ | 143.7V | 124.44V | 179.6V | 143.7V | 89.81V | Equation (4.29) |
| $V_{n,peak}$ | -71.85V | -124.44V | -89.8V | -71.85V | -44.91V | See note 1 below |
| $D_p$ | 0.384 | 0.644 | 0.281 | 0.384 | 0.615 | See note 2 below |
| $D_n$ | 1 | 0.644 | 1 | 1 | 1 | |
| L | 3.15mH | 3.15mH | 3.15mH | 3.15mH | 3.15mH | |
| C | ≥46.842µF | ≥46.842µF | ≥46.866µF | ≥14.009µF | ≥22.519µF | |
| $R_L$ | 490Ω | 490Ω | 490Ω | 1633.33Ω | 980Ω | |
| $I_p$ | 4.64A | 4.018A | 3.711A | 0.984A | 3.711A | See note 3 below |
| $I_n$ | -2.32A | -4.018A | -1.856A | -0.492A | -1.856A | See note 4 below |
| $V_1$ | 350V | 350V | 350V | 350V | 350V | See note 5 below |
| $V_2$ | 350V | 350V | 350V | 350V | 350V | See note 5 below |
| $V_{ref}$ | 2.5V | 2.5V | 2.5V | 2.5V | 2.5V | Analogue controller used |
| $R_S$ | 0.17Ω | 0.17Ω | 0.17Ω | 0.17Ω | 0.17Ω | |
| $V_m$ | 1.92V | 1.918V | 1.32V | 0.407V | 2.456 | Equation (3.80); See note 6 below |
| $V_{OUT}$ | 700V | 700V | 700V | 700V | 700V | |
| Figure 4.5 reference | RED TRACE | | BLUE TRACE | GREEN TRACE | CYAN TRACE | |

Note 1: From equation (3.70) it can be seen that for $D_n$ approximately equal to 1:

$$V_n = -\frac{V_p}{2}.$$

Note 2: $D_p$ can be found by substituting $V_p$ and $V_n$ into equation (3.69). For $D_n = 1$, which is at the crossover of a control algorithm rotation, $V_1 = V_2 = E$. Thus will $D_p$ be equal to:

$$D_p = 1 - \frac{3V_p}{2E}.$$

Note 3: $I_p$ is the low frequency absolute positive phase current. If it is assumed that the input current follows the input voltage, judging by figure 3.1 $I_p$ should be at a maximum when $D_n = 1$. Thus will $I_p$ be the value determined in (4.32). For $V_t = 0$ (i.e. the results shown in the second column of table 4.1), equations (3.72) and (3.73) can be used to determine $I_p$ and $I_n$.

Note 4: In a similar manner as in note 1, and assuming that the input current follows the input voltage, the negative side current is:

$$I_n = -\frac{I_p}{2}.$$

Note 5: Assuming C to be large, the voltage ripple can be assumed to be zero. However, for $D_n = 1$ or $D_p = 1$, $V_1 = V_2$, independent of the size of C.

Note 6: If the value obtained for $V_m$, at maximum load conditions exceeds the range of the DSP (i.e. 3.3V), then $R_S$ should be lowered to avoid saturation.

For the purpose of this prototype the output capacitance is chosen to be three 22µF in parallel. Should the performance of the rectifier however be unsatisfactory, the capacitance can be increased further. Three capacitors are paralleled to ensure the ripple current does not exceed the maximum allowable for the output capacitor, and also to ensure that the capacitor ESR is significantly lower than the output impedance so that the model derived in Chapter 3 holds.

The parameters derived in table 4.1 were substituted into (3.102) and the associated bode diagramme derived. The bode diagramme for the uncompensated open-loop transfer function ($T_{ol}(s)$) is shown in figure 4.5.

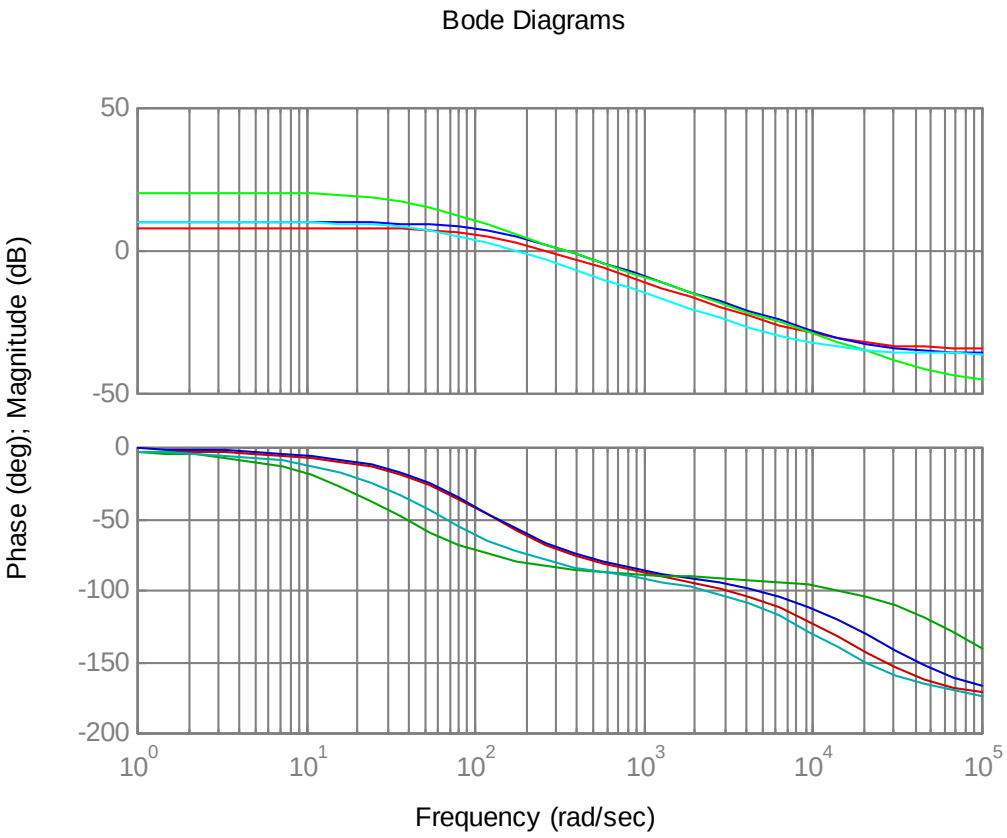



**Figure 4.5.** Uncompensated open-loop transfer diagrammes for different load and input voltages (refer to table 4.1).

As discussed in section 3.4 of Chapter 3 the system must be controlled (implementation of the compensator) where the slope of the magnitude bode plot is –20dB/decade It is observed from figure 4.5 that the gain does not change for different input voltages and/or power levels, except for a slight gain drop (equal to approximately 4dB) for operation at 110V. From figure 4.5 it is observed that the best frequency to implement the cross over will be ~ 1 krad/s. At this frequency there will be minimal phase shift for different power levels.

Pole-zero cancellation was performed on each of the bode plots shown in figure 4.5 to eliminate any unwanted disturbances due to rounding (as can be witnessed by the spikes on the bode diagramme). Figure 4.6 shows a comparison if pole-zero cancellation is performed (red trace) and if not performed (blue trace). The pole-zero cancellation eliminates unwanted non-linearities that might exist and that might show on the bode plot as spurious frequency spikes.

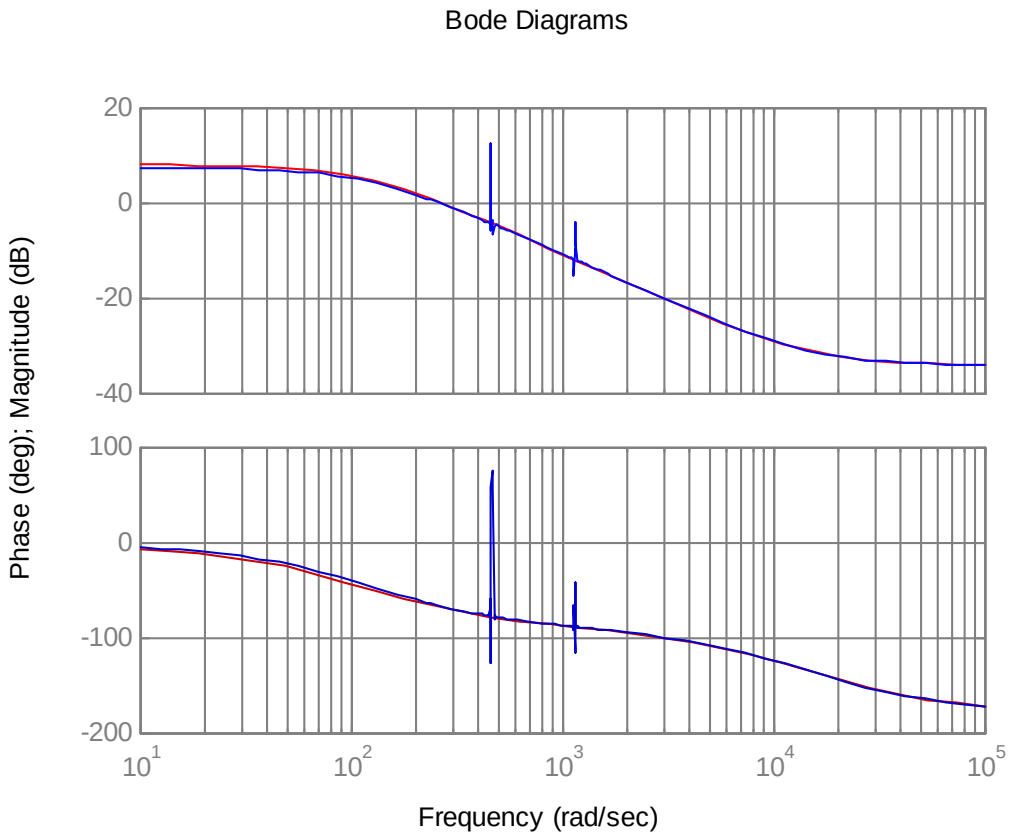



**Figure 4.6.** Uncompensated open-loop transfer diagrammes for pole-zero cancellation implemented (red trace) and not implemented (blue trace), for a $V_{LL}$ = 176V input and an output loading of 1kW.

Figure 4.7 shows a pole-zero map for the uncompensated open-loop transfer function for $P_{OUT}$ = 1kW, and $V_{LL}$ = 176V input voltage. The right hand plane zero is evident, which results in the 180° phase shift at approximately $\omega_0 = 1/\sqrt[4]{3L^2C^2}$ rad/s. The right hand plane zero is characteristic of boost type converters working in continuous inductor current mode, where the output voltage cannot immediately rise when the duty cycle is increased.

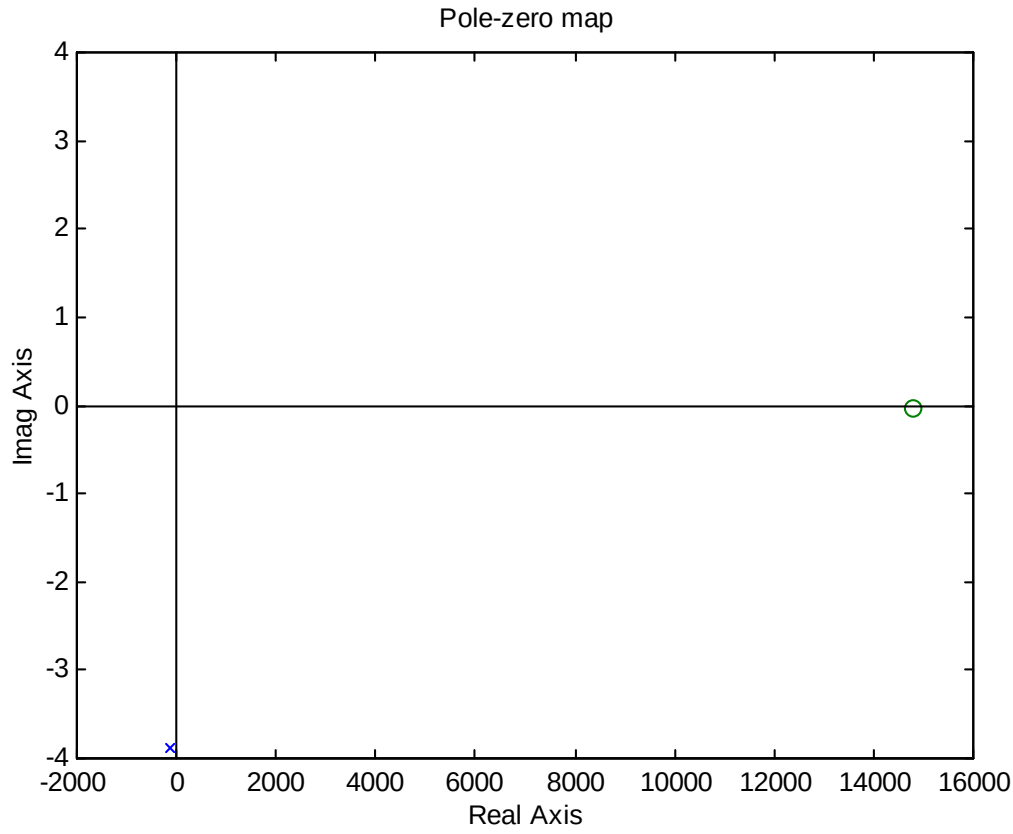



**Figure 4.7.** Pole-zero map of the uncompensated open-loop transfer function (X indicates a pole and O indicates a zero). The single pole is at –115-3.9i.

## 4.4 VIENNA RECTIFIER: CONTROLLER DESIGN

The condition for stability, as stated by [30], is as follows: A system will be stable if the compensated open-loop gain of the system is less than 0dB when the compensated open-loop phase angle is -180°. Another criteria for stability is that the compensated open-loop gain roll-off must be -20dB/decade at 0dB. From figure 4.6 it is evident that pure integration control cannot be used because the -90° phase angle shift will result in instability as the phase response is forced through -180° at the resonant frequency, $\omega_0 = 1/\sqrt[4]{3L^2C^2}$ rad/s (where the gain will still be positive and the gain roll off unpredictable). Integration control is necessary to ensure that the steady-state output error is zero. The controller proposed is a lag-lead type compensator [25], as shown in figure 4.8. This type of compensator is also referred to in the literature as a Type II compensator and is a single pole, single zero type compensator with a DC pole (integrator) to force the steady-state error to be zero (high DC gain, [31]).

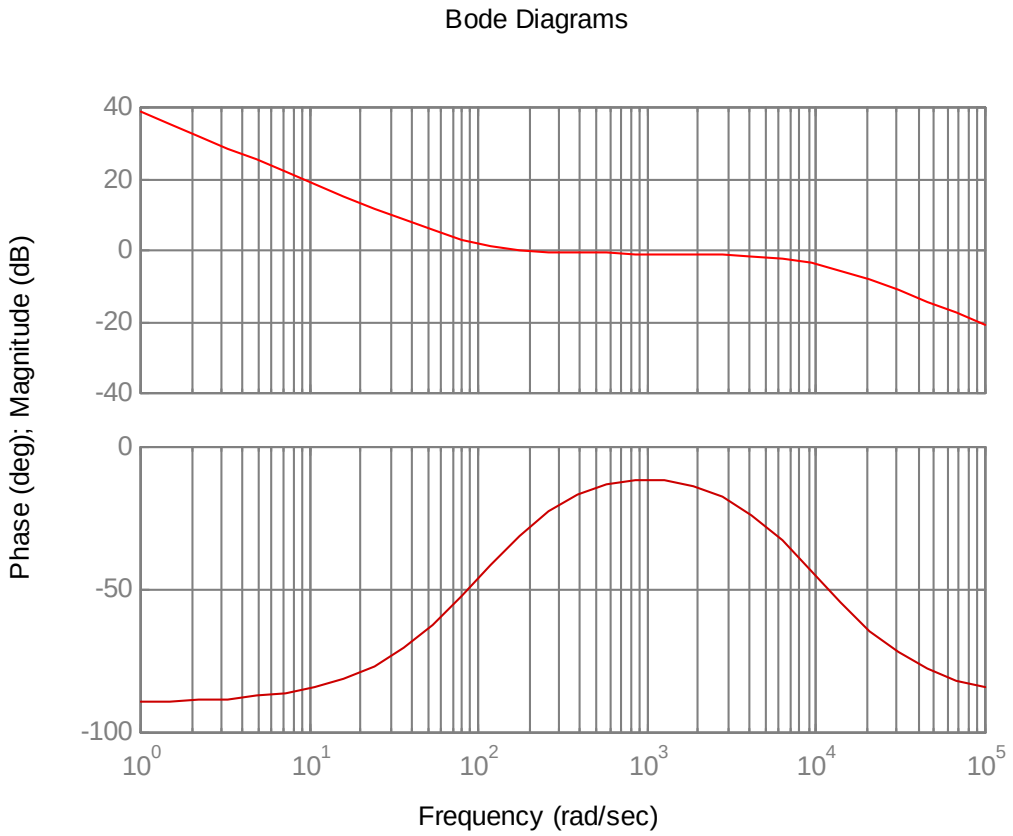



**Figure 4.8.** Type II compensator transfer function bode-plot.

The Type II compensator will provide a 0dB/decade slope change at the desired crossover frequency (for figure 4.6 this will be the frequency range 100 rad/s to 10 krad/s, where the frequency drop-off is –20dB/decade), as well as provide the necessary phase-boost to ensure a positive, adequate phase margin. [30] suggests a phase margin of 45º-60º as the stability requirement.

The compensator transfer function is of the form:

$$T_c(s) = A_G \frac{(s+\omega_z)}{s(s+\omega_p)} \tag{4.41}$$

With reference to figure 4.6 a suitable frequency range where compensation can be done is ω = 200 rad/s to ω = 10 krad/s. For this range of frequencies the gain roll-off for the uncompensated open-loop transfer is -20dB/decade, so the 0dB/decade compensation will result in stability. The major drawback of compensating in the range ω = [2; 10] krad/s is that the phase margin will change as the load changes but, as discussed in section 4.3,

implementing the crossover (the frequency where the compensated open-loop gain response will be 0db) at 1 krad/s the phase shift will be minimal over the full power range.

For the controller design the phase margin is chosen to be 60º as this will give optimum transient performance (refer to section 3.4 of this thesis). If the performance of the converter is however sluggish at lower power levels, the phase margin should be decreased, but to not less than 45° (as this will result in large overshoot).

For this converter the crossover frequency, where the compensated gain plot should be 0dB, is chosen to be $\omega_c$ = 1 krad/s ($\omega_c$ should be chosen at least an order lower than the switching frequency [25]). From figure 4.6 the uncompensated open-loop gain at the crossover frequency is:

$$\left|T_{ol}(s)\right|_{s\to j\omega_c} = -10.5dB\,, \tag{4.42}$$

and the uncompensated open-loop phase:

$$\angle T_{ol}(s)\big|_{s\to j\omega_c} = -87.5°\,, \tag{4.43}$$

From [17] the required compensator phase boost is (for PM = 60°, corresponding to approximately 5% overshoot at the output):

$$\begin{aligned} boost &= -(\angle T_{ol}(s)\big|_{s\to j\omega_c} + 90) + PM \\ &= -(-87.5 + 90) + 60 \\ &= 57.5° \end{aligned} \tag{4.44}$$

Since the boost required is lower than 90°, the system can be compensated with this type of compensator [25]. Should the boost required be higher than 90° the crossover frequency must be lowered, which will result in a lower controller bandwidth and hence slower response to step inputs. From [17] the phase plot is a tangent curve and the value of parameter K is:

$$K = \tan\left(45° + \frac{boost}{2}\right) = \tan\left(45° + \frac{57.5°}{2}\right) = 3.431 \tag{4.45}$$

$$\omega_z = \frac{\omega_c}{K} = 291.5\,rad/s \tag{4.46}$$

$$\omega_p = \omega_c K = 3430.8\,rad/s \tag{4.47}$$

The compensator gain at DC is:

$$\begin{aligned}\left|T_c(s)\right|_{s\to dc} &= -\left|T_{ol}(s)\right|_{s\to j\omega_c} + 20\log_{10}(\omega_z)\\ &= 10.5dB + 49.29dB\\ &= 59.79dB\\ &= 976.42\end{aligned} \tag{4.48}$$

The gain $A_g$ (for equation (4.41)) can subsequently be calculated as:

$$\begin{aligned}A_G &= \left|T_c(s)\right|_{s\to dc}\frac{\omega_p}{\omega_z}\\ &= 976.42\times\frac{3430.8}{291.5}\\ &= 11492.00\end{aligned} \tag{4.48}$$

By substituting (4.48), (4.47) and (4.46) into (4.41) the compensator transfer function is:

$$T_c(s) = 11492\frac{(s+291.5)}{s(s+3430.8)} \tag{4.49}$$

Figure 4.9 shows the bode diagramme for the compensator transfer function. It can be seen that the phase boost is 57.5° and the gain 10.5dB at $\omega_c$.

The bode diagramme for the compensated open-loop gain and phase response/bode plot ($T_{ol,comp}(s)$) is shown in figure 4.10, where:

$$T_{ol,\,comp}(s) = T_c(s)T_{ol}(s) \tag{4.50}$$

From the MATLAB analysis (figure 4.10), it can be seen that the calculated phase margin is 59.9° and the crossover frequency is $\omega_c$ = 979.7 rad/s. It is also observed that the roll-off of the gain plot is 20dB/decade at 0dB, and that the gain margin is positive.

A MATLAB script is provided in Appendix B for determining the uncompensated open-loop transfer function.

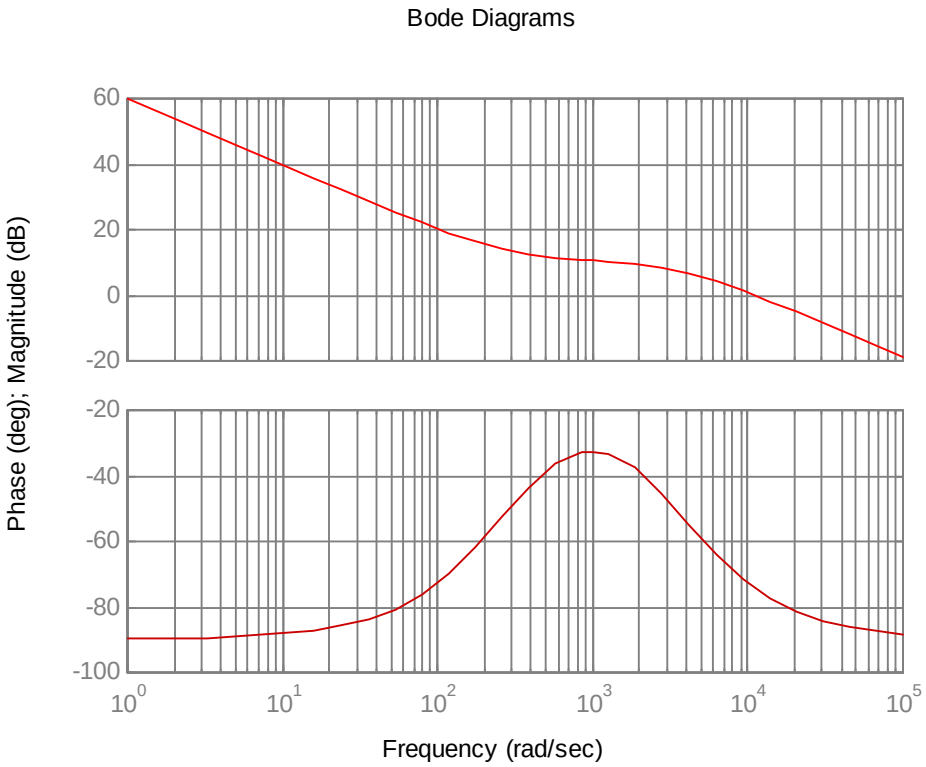



**Figure 4.9.** VIENNA Rectifier compensator transfer function bode plot.

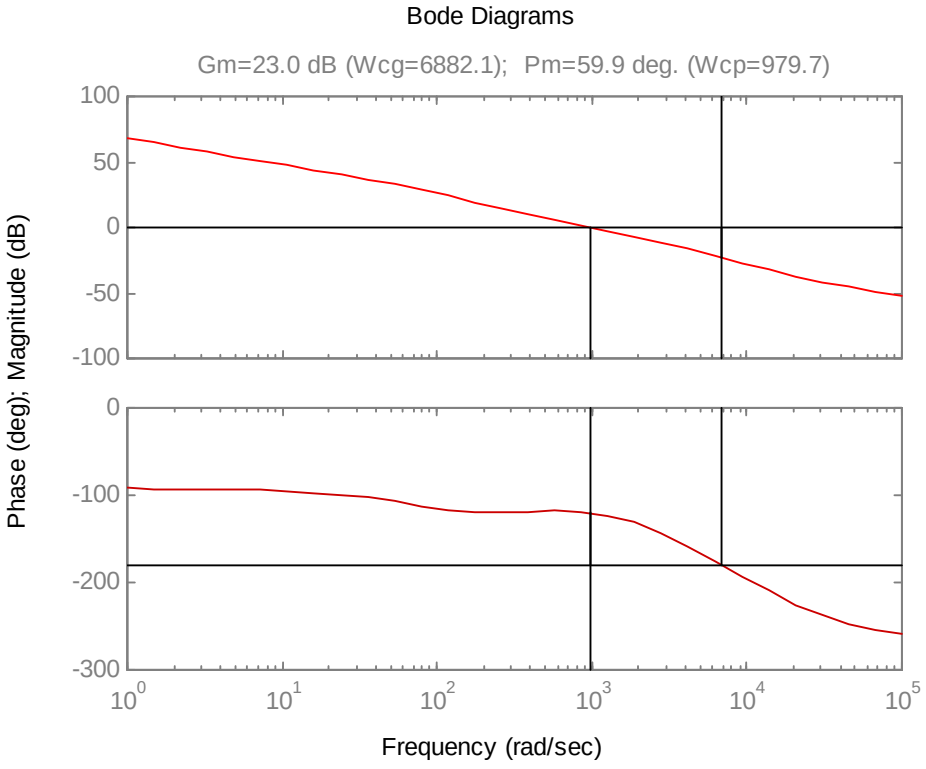



**Figure 4.10.** VIENNA Rectifier open-loop compensated system gain and phase plot.

It is shown by [17] that the compensator can be implemented by using an operational amplifier, as shown in figure 4.11.

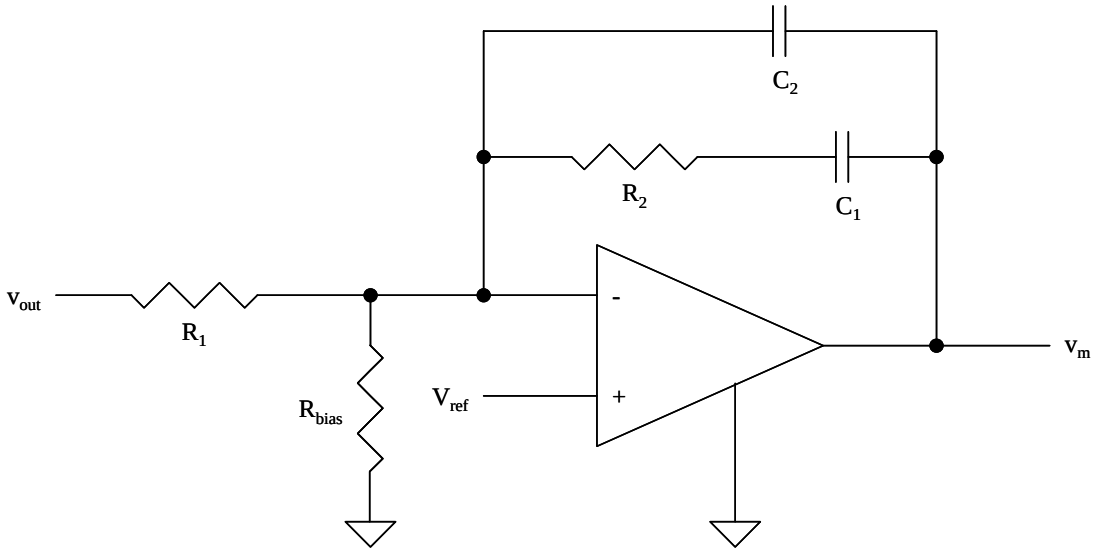



**Figure 4.11.** Operational amplifier implementation of a Type II compensator.

If $R_1$ is arbitrarily chosen to be 10kΩ, then:

$$\begin{aligned} C_2 &= \frac{\left|T_{ol}(s)\right|_{s\to j\omega_c}}{KR_1\omega_c} \\ &= \frac{10^{\frac{-10.5}{20}}}{3.431\times 10000\times 1000} \\ &= 8.70nF \approx 8.2nF \end{aligned} \tag{4.51}$$

and

$$\begin{aligned} C_1 &= C_2\left(K^2-1\right) \\ &= 8.7\times 10^{-9}\left(3.431^2-1\right) \\ &= 93.7nF \approx 100nF \end{aligned} \tag{4.52}$$

and

$$\begin{aligned} R_2 &= \frac{K}{\left(C_1\omega_c\right)} \\ &= \frac{3.431}{\left(93.7\times 10^{-9}\times 1000\right)} \\ &= 36.606k\Omega \approx 36.5k\Omega \end{aligned} \tag{4.53}$$

## 4.5 DIGITAL IMPLEMENTATION OF THE COMPENSATOR

For the proposed controller to be implemented on a DSP the compensator transfer function must be converted to its digital equivalent, or Z-transform, using a zero order hold discretization method. If the sampling frequency is not an order of magnitude higher than either of the poles or zeros, another discretization method should be considered for example "prewarp" or "tustin" discretization methods, otherwise the impact on the phase margin and system damping shall be noticeable. From [32] the zero order hold transfer function for $T_c$, in Laplace form, is:

$$T_{c,\,zoh}(s) = \left(1 - e^{-Ts}\right)\frac{T_c(s)}{s}, \tag{4.54}$$

where T is the sampling period of the DSP. If equation (4.54) is transformed into its Z-transform equivalent [32] the digital transfer function is given by:

$$T_c(z) = \left(1 - z^{-1}\right)Z\left\{\frac{T_c(s)}{s}\right\} = \frac{z-1}{z}Z\left\{\frac{A_G(s+\omega_z)}{s^2(s+\omega_p)}\right\} \tag{4.55}$$

Evaluating and simplifying (4.46) yields:

$$T_c(z) = \frac{a_1 + z^{-1}a_2 + z^{-2}a_3}{b_1 + z^{-1}b_2 + z^{-2}b_3} \tag{4.56}$$

$$= A_G\frac{(A+C) + z^{-1}\left(A\left(-1-e^{-\omega_p T}\right) + BT - 2C\right) + z^{-2}\left(Ae^{-\omega_p T} - BTe^{-\omega_p T} + C\right)}{1 + z^{-1}\left(-1-e^{-\omega_p T}\right) + z^{-2}\left(e^{-\omega_p T}\right)}, \tag{4.57}$$

where:

$$B = \frac{\omega_z}{\omega_p} \tag{4.58}$$

$$C = \frac{-(\omega_z - \omega_p)}{{\omega_p}^2} \tag{4.59}$$

$$A = \frac{\left((1+\omega_z) - B(1+\omega_p) - C\right)}{(1+\omega_p)} \tag{4.60}$$

From (4.56) the controller coefficients are:

$$a_1 = A_G(A+C) \approx 0 \tag{4.61}$$

$$a_2 = A_G\left(A\left(-1-e^{-\omega_p T}\right) + BT - 2C\right) \tag{4.62}$$

$$a_3 = A_G\left(Ae^{-\omega_p T} - BTe^{-\omega_p T} + C\right) \tag{4.63}$$

$$b_1 = 1 \tag{4.64}$$

$$b_2 = \left(-1-e^{-\omega_p T}\right) \tag{4.65}$$

$$b_3 = \left(e^{-\omega_p T}\right) \tag{4.66}$$

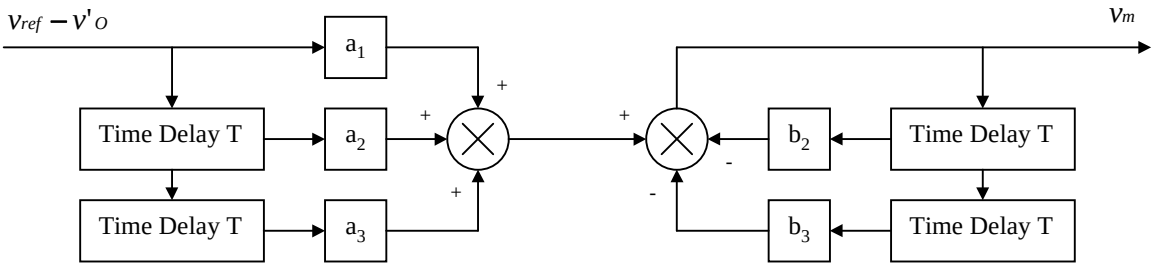



**Figure 4.12.** Flow diagramme for a digital lag-lead compensator.

Figure 4.12 shows the flow diagramme for digital implementation of the compensator [32]. For the proposed system from (4.61) to (4.66) and (4.49) the controller coefficients are calculated to be, for purely illustration purposes, for a sampling frequency of T = 5kHz (as a rule of thumb the sampling frequency is chosen to be at least two orders in magnitude higher than the line frequency, or tracking frequency):

$$a_1 = 0 \tag{4.67}$$
$$a_2 = 1.7171 \tag{4.68}$$
$$a_3 = -1.6201 \tag{4.69}$$
$$b_1 = 1 \tag{4.70}$$
$$b_2 = -1.5035 \tag{4.71}$$
$$b_3 = 0.5035 \tag{4.72}$$

An observation at this point is, as can be seen in figure 2.23, that the sensed input current control signals must be filtered in order to reject high frequency switching noise and thus obtaining a proper closed-loop system operation.

Figure 4.13 shows a comparison between the analogue compensator (blue trace) and the digital compensator (red trace). From figure 4.13 it can be seen that if the sampling frequency is not sufficiently high it can influence rectifier performance.

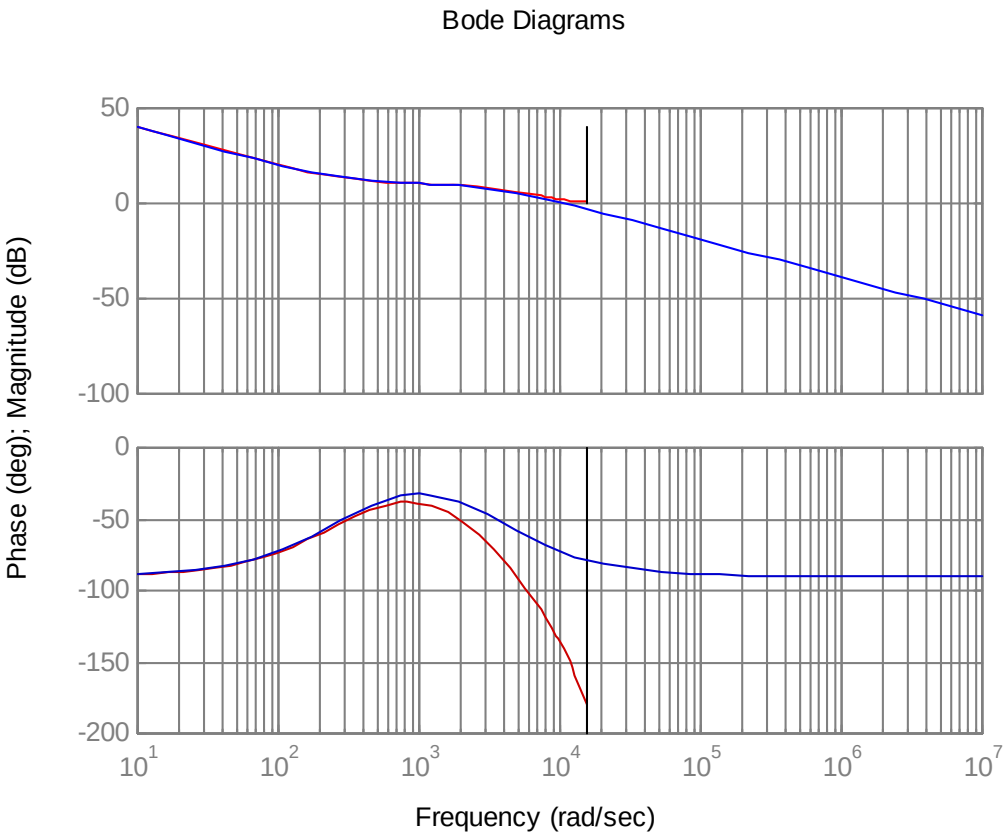



**Figure 4.13.** Analogue (blue trace) and digital (red trace) compensator comparison.

The plant transfer function, under rated output loading and an input voltage of 176V, for the proposed system was found to be (see Appendix B for the MATLAB script used to determine the transfer function):

$$T_{ol}(s) = \frac{-0.01994s + 294.2}{s + 114.6} \tag{4.73}$$

Using the MATLAB command c2d, the discrete plant transfer function for a sample frequency of 5kHz is:

$$T_{ol}(z) = \frac{-0.01994z + 2.587}{z} \tag{4.74}$$

Similarly the plant transfer function can be found for different sampling rates. Figure 4.14 shows the compensated open-loop transfer gain and phase plots for a sampling frequency of 5kHz (for illustration purposes). It is seen that the phase margin is 47.9º, the gain margin is positive and that the gain drop-off through 0dB is –20dB/decade and thus, from a pure control stability point of view, the system should be stable for a sampling frequency of 5kHz. Since the gain and phase frequency response shall improve for higher sampling

frequencies, it is assumed that the system will be stable for higher sampling frequencies. Any quantization effects [33] are not considered.

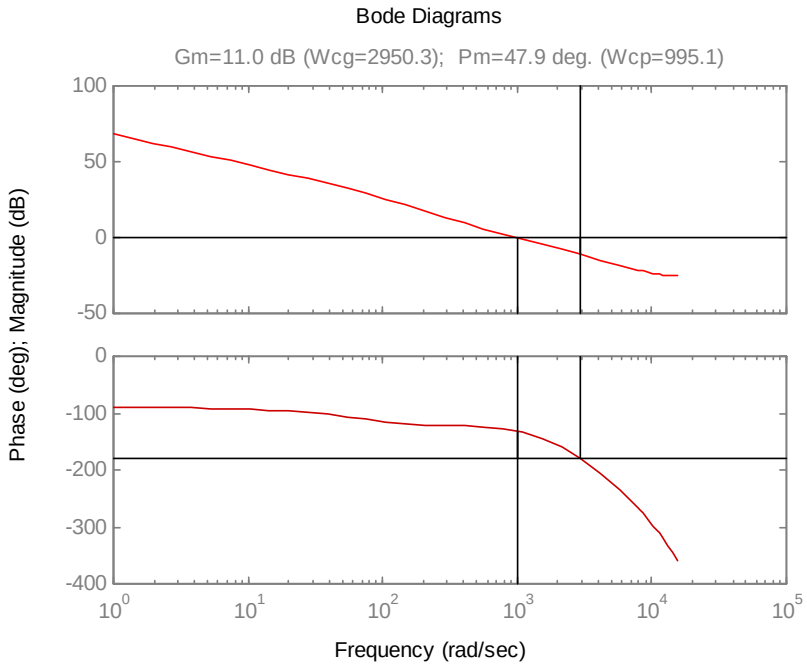



**Figure 4.14.** VIENNA Rectifier open-loop compensated system gain and phase plot.

## 4.6 DIGITAL IMPLEMENTATION OF A LOW PASS FILTER

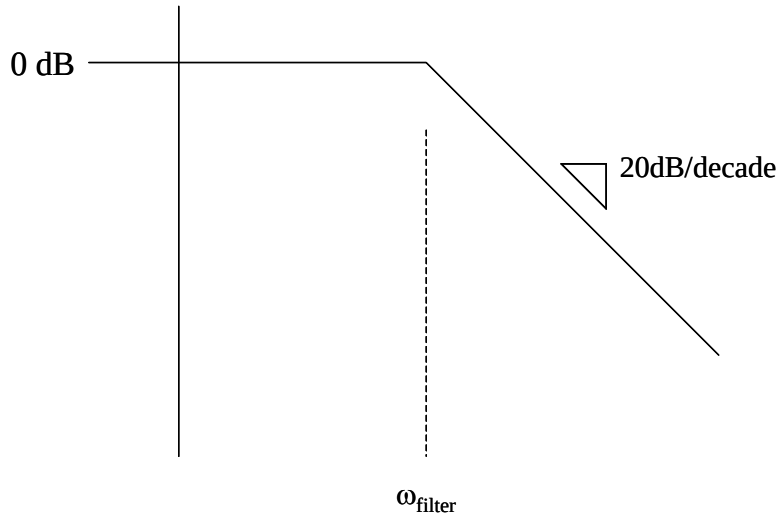



**Figure 4.15.** Bode gain plot for a digital low-pass filter.

The filter required for filtering the sensed input current signals calls for a low pass filter with a DC gain of 1, and a –3dB cut-off frequency at least in an order of magnitude higher than the cross-over frequency (equal to 1 krad/s for this implementation) but in an order of magnitude lower than the switching frequency. As a rule of thumb, the filter frequency is also chosen to be in an order of magnitude higher than the line frequency, but for this implementation the line frequency is lower than the crossover frequency.

The reason for a DC gain of 1 is not to change the gain response (or gain plot) obtained in Chapter 3. A change in gain will result in a change in phase margin and thus the model obtained in Chapter 3 will no longer accurately describe the system any more.

The choice of cut-off frequency is chosen to be an order of magnitude higher than the crossover frequency for reason that the filter phase is still in transition up to an order of magnitude below the cut-off frequency (due to the phase response following a tangent curve). Thus if the cut-off frequency is not chosen to be in an order of magnitude higher than the crossover frequency it will result in a change in the phase profile of the model obtained in Chapter 3, and thus the model obtained in Chapter 3 will no longer accurately describe the system. The filter frequency is also chosen to be in an order of magnitude lower than the switching frequency for the reason that the ripple current due to the switching must be attenuated otherwise it shall result in a distorted input current signal and also unwanted noise at the output.

The transfer model of the filter (in Laplace form) is given as [32]:

$$T_{filter}(s) = \frac{1}{\frac{s}{\omega_{filter}} + 1} \tag{4.75}$$

The equivalent z-transform for equation (4.75) is (with zero-order-hold) [32]:

$$T_{filter}(z) = \frac{z\omega_{filter}}{z - e^{-\omega filterT}} \tag{4.76}$$

$$= \frac{z^{-1}\left(1 - e^{-\omega filterT}\right)}{1 - z^{-1}e^{-\omega filterT}} \tag{4.77}$$

Comparing equation (4.77) with equation (4.56) the new coefficients are calculated as:

$$a_1 = 0 \tag{4.78}$$

$$a_2 = 1 - e^{-\omega_{filter} \cdot T_{sample}} \tag{4.79}$$

$$a_3 = 0 \tag{4.80}$$

$$b_1 = 1 \tag{4.81}$$

$$b_2 = -e^{-\omega_{filter} \cdot T_{sample}} \tag{4.82}$$

$$b_3 = 0 \tag{4.83}$$

For a sampling frequency of 5kHz, and a filter cut-off frequency of 1kHz (an order of magnitude lower than the switching frequency of 50kHz, but an order of magnitude higher than the line frequencies, that will not be higher than 50Hz), the coefficients are equal to:

$$a_{2,f} = 1 - e^{-2\pi \cdot 1000 \cdot (5000)^{-1}} = 0.7154 \tag{4.84}$$

$$b_{1,f} = 1 \tag{4.85}$$

$$b_{2,f} = -e^{-2\pi \cdot 1000 \cdot (5000)^{-1}} = -0.2846 \tag{4.86}$$

An f subscript was added to indicate filter operation.

Shown in figure 4.16 is a MATLAB generated bode plot of the digital filter. It can be seen that the –3dB cut off frequency is ~6 krad/s (~1kHz), and the DC-gain is 0dB.

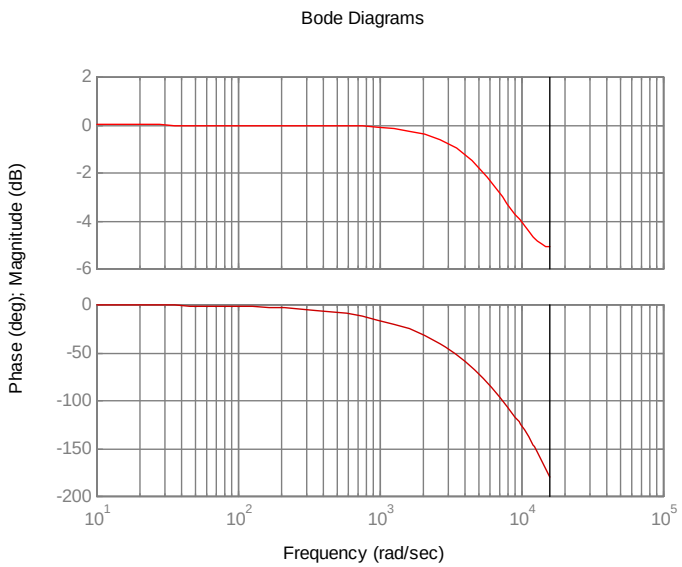



**Figure 4.16.** Bode plot of a digital low-pass filter for a sampling frequency of 5kHz (the vertical solid line is at half of the sampling frequency, or 15.71 krad/s).

## 4.7 DIGITAL CONTROLLER IMPLEMENTATION

Figure 4.17 shows a block diagramme for the proposed implementation of a digital controller on a DSP or similar controller. The digital implementation of the controller for the VIENNA rectifier is based on the controller proposed by [10] for fixed switching frequency control of the VIENNA rectifier.

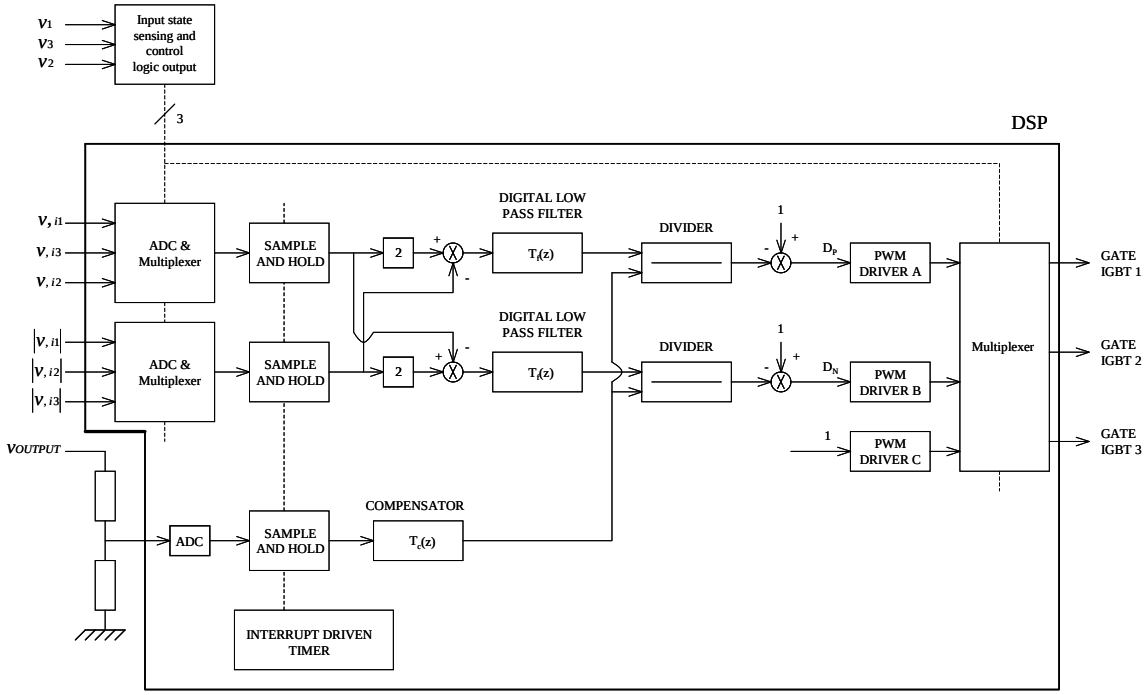



**Figure 4.17.** Block diagramme for the proposed implementation of a digital controller.

Shown in figure 4.18 is a flow diagramme of operations to be performed by the proposed controller. The flow diagramme is based on the flow operations as proposed by [34].

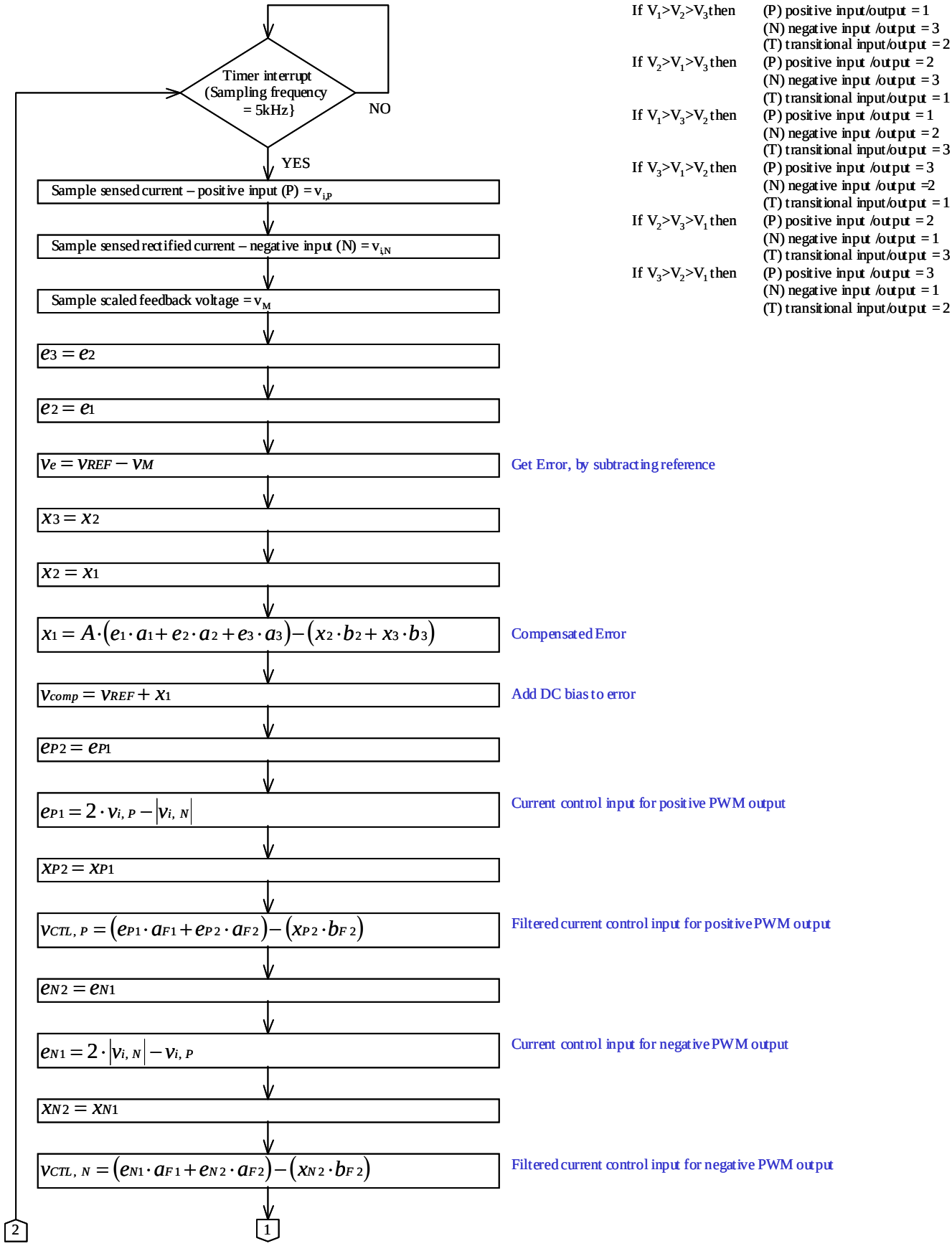



**Figure 4.18.** Flow diagramme for the proposed implementation of a digital controller.

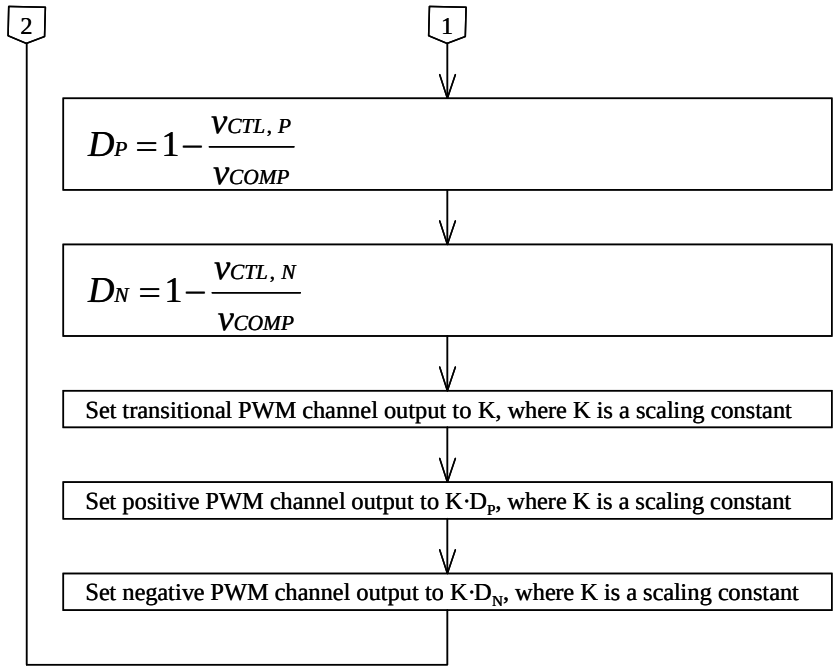



**Figure 4.18(cont.).** Flow diagramme for the proposed implementation of a digital controller.

## 4.8 DIGITAL AND ANALOGUE CONTROLLER SIMULATION

A digital simulation was performed on the sample system to study and examine the effect of sampling frequency on the current waveform shape (with a fixed input voltage, but various output loading). The specifications for the sample system are as follow:

- L = 3.15mH
- C = 66µF
- Input voltage = 176V line-to-line
- Full load on output = 1kW
- Output voltage = 700V
- Sensed current filter frequency = 1 kHz

Digital simulations (see Appendix D for the MATLAB script for the digital simulations) were performed for the following sampling frequencies: 5Khz, 10kHz, 12.5kHz and 25kHz. Listed in Table 4.2 are the controller parameters for the various sampling frequencies ($a_1 = 0$, $b_1 = 1$ and $b_{1,f} = 1$ for all sampling frequencies).

**Table 4.2.** Digital control parameters.

| | 5kHz | 10kHz | 12.5kHz | 25kHz |
|---|---|---|---|---|
| $a_2$ | 1.717 | 0.988 | 0.814 | 0.432 |
| $a_3$ | -1.620 | -0.959 | -0.795 | -0.427 |
| $b_2$ | -1.504 | -1.710 | -1.760 | -1.872 |
| $b_3$ | 0.504 | 0.710 | 0.760 | 0.872 |
| $a_{1,f}$ | 0.715 | 0.467 | 0.395 | 0.222 |
| $b_{2,f}$ | -0.285 | -0.533 | -0.605 | -0.777 |

Simulation results in figure 4.20 show the performance of the input current at various power levels for each sampling frequency and compared to analogue control simulation (see Appendix E for a schematic of PSpice simulation, used for the analogue control simulations).

Shown in figure 4.19, in comparison to digital control, is PSpice simulations featuring analogue control. It is obvious that input current for the PSpice simulations are of excellent quality for all power levels. It is observed in figure 4.19 that the shape of the input current waveform improves as the sampling frequency increases. It is also seen that the input current is only at a usable quality level at a sampling frequency of 25kHz or more (when compared to the PSpice simulations). Thus, as an observation, for digital control of the VIENNA rectifier, the sampling frequency must be in the order of 50 times higher than the compensator pole!

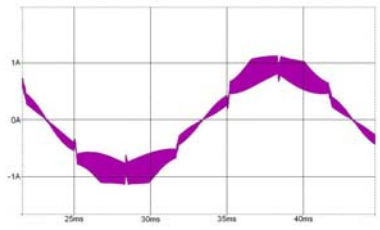
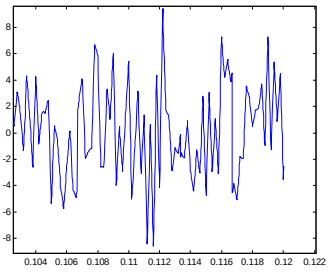
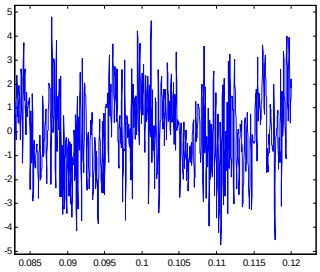
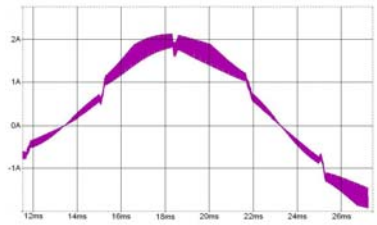
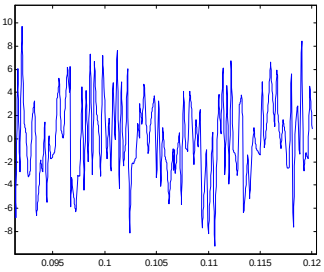
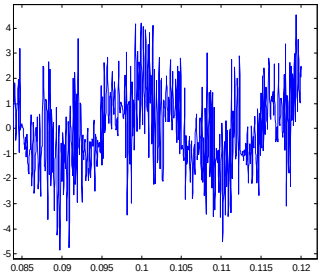
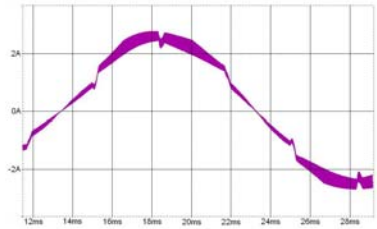
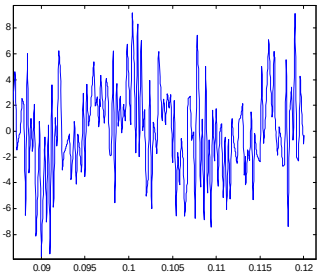
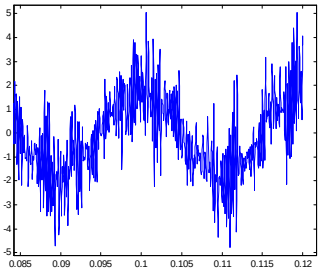
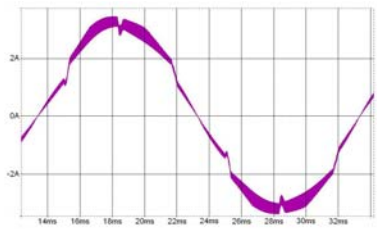
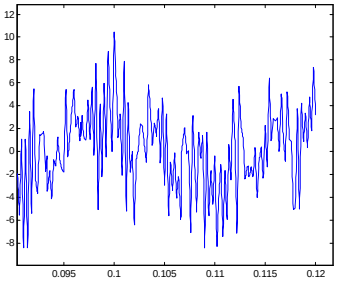
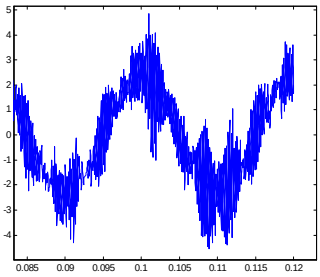
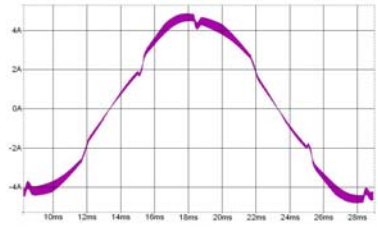
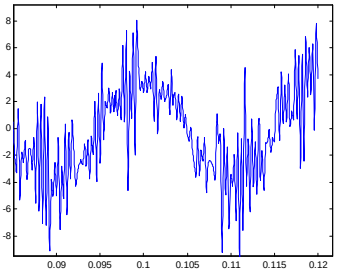
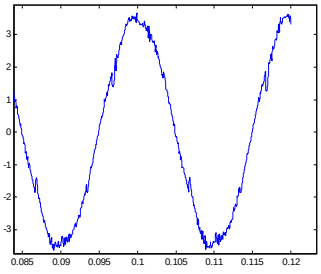
| Power level | Analogue controller | Digital controller – sampling frequency | |
|---|---|---|---|
| | | 5kHz | 10kHz |
| 200W |  |  |  |
| 400W |  |  |  |
| 550W |  |  |  |
| 700W |  |  |  |
| 1kW |  |  |  |

**Figure 4.19.** Analogue and digital control simulated current waveforms, for various power levels and sampling frequencies (digital control).

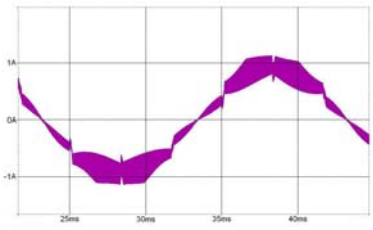
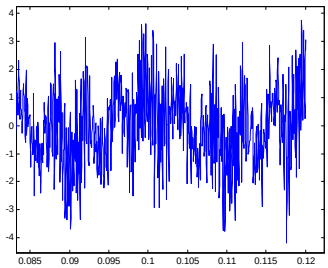
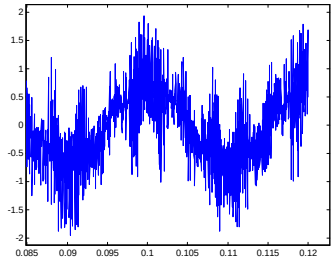
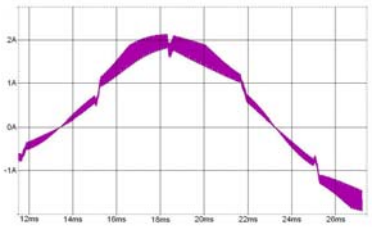
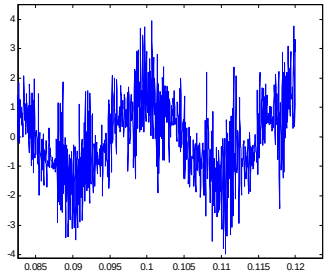
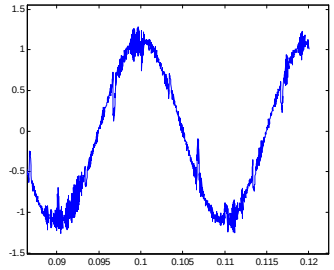
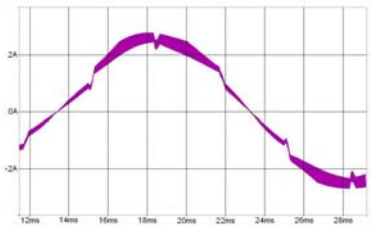
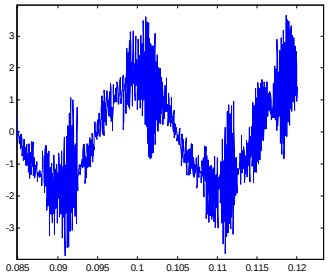
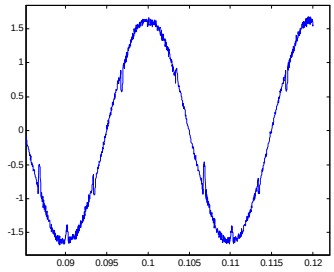
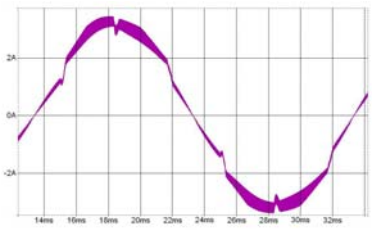
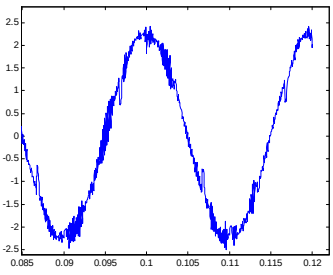
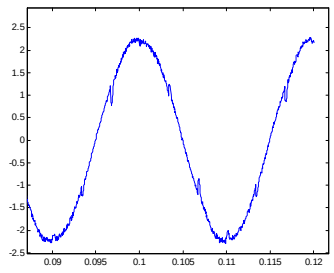
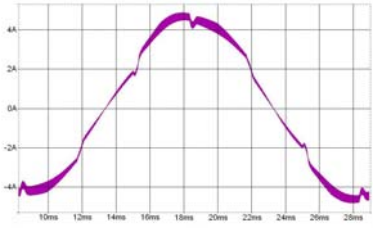
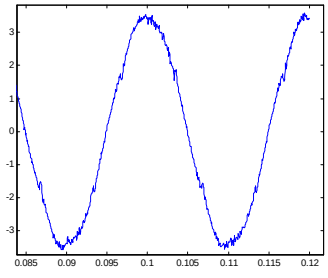
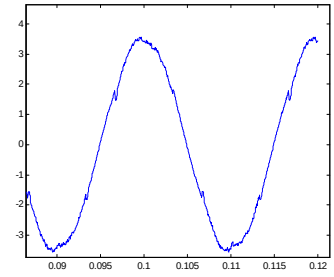
| Power level | Analogue controller | Digital controller – sampling frequency | |
|---|---|---|---|
| | | 12.5kHz | 25kHz |
| 200W |  |  |  |
| 400W |  |  |  |
| 550W |  |  |  |
| 700W |  |  |  |
| 1kW |  |  |  |

**Figure 4.19(cont.).** Analogue and digital control simulated current waveforms, for various power levels and sampling frequencies (digital control).

## 4.9 CHAPTER CONCLUSION

In this Chapter the procedure for choosing filter components for the VIENNA rectifier was developed and the influence of these components on performance of the system was shown. It was also shown how to design the compensator for given performance criteria and also how to implement the compensator. With the possibility of implementing an analogue or digital compensator, it allows the designer to be flexible in his design. Should cost be the driving factor the designer can opt for an analogue solution, where a digital solution allows the designer the option of easier system integration. One of the clear advantages of digital control is the ability to include supervisory functionality into the controller without adding any hardware. Supervisory functions shall typically include over-current protection, over-voltage protection and telemetry feedback. Another advantage of the digital controller is the implementation of adaptive controllers where gain, poles and zeros can be adjusted for various load/line conditions. Simulations were performed on the effect of the sampling frequency on the rectifier control and it was found that a sampling frequency of 25kHz or more might be needed for implementing the controller digitally. With the added burden of current sensing filtering and maybe soft-start implementations, it might be difficult to implement such a high sampling frequency on a fixed-point arithmetic DSP. It was also observed from figure 4.19 that three-significant digits in the control parameters are sufficient for digital control purposes.

# CHAPTER 5

# PHYSICAL REALIZATION OF THE VIENNA RECTIFIER

## 5.1 SELECTING THE OUTPUT CAPACITOR

Figure 5.1 shows the expected ripple current of the output capacitor, assuming that the high frequency current ripple is negligible.

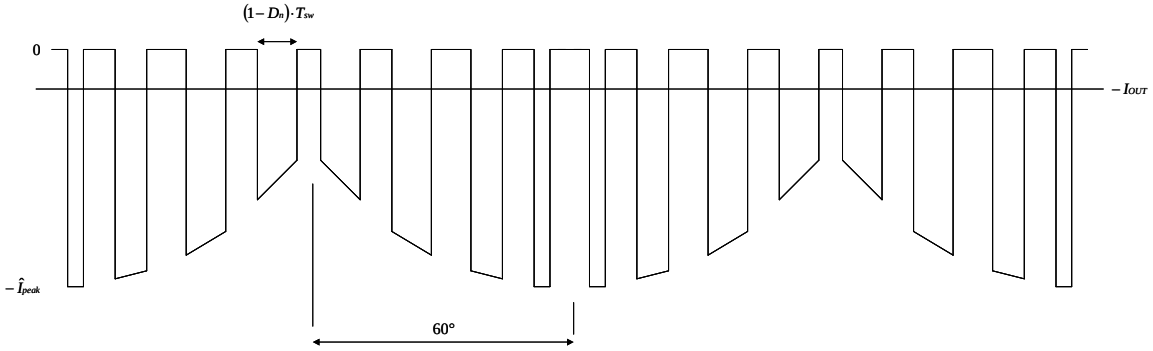



**Figure 5.1.** Expected current ripple through one half of the capacitor bank (capacitor $C_2$).

From [35] rms current can be calculated by the formula:

$$i_{rms} = \sqrt{\int i(t)^2 \, dt} \tag{5.1}$$

If equation (5.1) is translated to its discrete form:

$$i_{rms} = \sqrt{\sum_{all\ x} i(x)^2 \, \Delta t} \tag{5.2}$$

From figure 2.18, the flow of input and output current is defined as shown in figure 5.2.

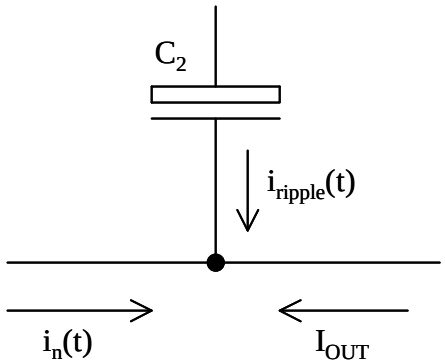



**Figure 5.2.** Flow of input and output current.

From figure 5.2 it can be seen that the AC capacitor ripple, $i_{ripple\_C}(t)$, is equal to:

$$i_{ripple\_C}(t) = -i_n(t)\left(1 - D_n(t)\right) - I_{OUT} \tag{5.3}$$

If equation (5.3) is translated to its discrete form:

$$i_{ripple\_C} = -i_n(x) - I_{OUT} \tag{5.4}$$

From figure 5.1 it can be seen that the ripple current only has to be evaluated for one 60º block and multiplied by six (there are six 60º blocks for a full 360º). When substituting equation (5.4) into equation (5.2), and also recognizing that from equation (5.3) that $\Delta t = (1\text{-}D_n(x))T_{SW}$, the rms ripple current flowing through the capacitor can be calculated as (again assuming that the output capacitance is large enough that all the AC-current flows through the capacitor):

$$\begin{aligned} i_{ripple\_C,rms} &= \sqrt{\frac{1}{T_L}\sum\begin{pmatrix}(current\ during\ off\ \ time)^2(1-D_n)T_{SW}\\ +(current\ during\ on\ time)^2 D_n T_{SW}\end{pmatrix}} \\ &= \sqrt{\frac{6}{T_L}\sum_{x=0}^{y}\left(\left(i_n(x)+I_{OUT}\right)^2\left(1-D_n(x)\right)T_{sw}+\left(-I_{OUT}\right)^2\left(D_n(x)\right)T_{sw}\right)}, \end{aligned} \tag{5.5}$$

where $I_{OUT}$ is the average output current and $D_n(x)$ is as defined in (4.26). The ripple current $i_n(x)$ is defined as (assuming the input current to be sinusoidal):

$$i_n(t) = -I_{p,\,peak}\cos\left(\frac{2\pi}{T_L}\left(t-\frac{60T_L}{360}\right)\right) \tag{5.6}$$

$$\therefore i_n(x) = -I_{p,\,peak}\cos\left(\frac{2\pi T_{sw}}{T_L}(x+1)-\frac{120\pi}{360}\right) \tag{5.7}$$

For the prototype suggested in section 4.3, equation (5.7) will be equal to:

$$\therefore i_n(x) = -4.64\cos\left(\frac{2\pi\times 0.00002}{0.02}(x+1)-\frac{120\pi}{360}\right) \tag{5.8}$$

Substituting (5.8) into (5.5) and solving for an input voltage of $V_{LL}$ = 176V yields:

$$i_{ripple\_C,rms} = 1.128A \tag{5.9}$$

Since a capacitor bank was chosen that consists of three capacitors in parallel (refer to section 4.3), each capacitor must be able to withstand $0.376A_{rms}$ ripple current at a frequency of 50Hz. The voltage rating of the capacitors must be half of the output voltage plus half of the voltage ripple (i.e. at least 377V will fall over the capacitor, thus a capacitor with at least a 400V rating must be chosen for the proposed prototype). The capacitor chosen for the prototype 1kW converter is the Evox-Rifa PEG 124 22uF 450V capacitor.

## 5.2 DESIGNING THE INPUT INDUCTOR

The peak energy that must stored by the inductor is [36]:

$$\begin{aligned} E &= LI^2 \\ &= L\hat{I}_p^{\,2} \\ &= 3.15\times10^{-3}\times4.64^2 \\ &= 0.0678J \end{aligned} \tag{5.10}$$

From figure 5.3 (figure 25 from the ferroxcube databook [36]) suitable magnetics for the input inductor will be an E65 core with at least a 3.5mm air gap. A 4mm air gap is chosen to allow for some losses in the converter. From [37] the effective permeability of a gapped core is calculated to be:

$$\mu_e = \frac{l_e\mu_i}{l_e + \frac{l_{gap}}{k}\mu_i}, \tag{5.11}$$

where $\mu_i$ is the initial permeability of the core, $l_e$ the effective length of the core and k an arbitrary constant. For an E65 core with a 4mm gap, made of 3F3 material, the effective permeability can be calculated as:

$$\begin{aligned} \mu_e &= \frac{147\times1900}{147 + \frac{4}{1.8}\times1900} \\ &= 63.92 \end{aligned} \tag{5.12}$$

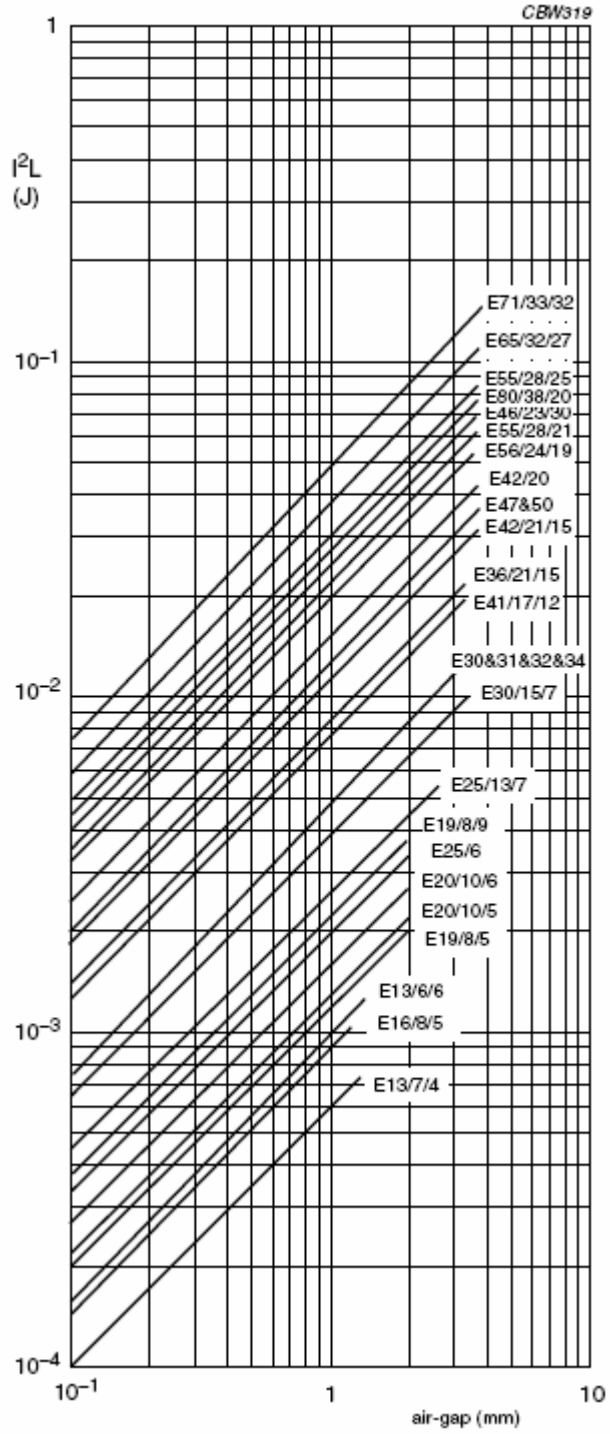



**Figure 5.3.** Inductor design curve for E-Type ferrite cores [36].

The $A_L$ value of the core can subsequently be calculated as [36]:

$$A_L = \frac{1.257\mu_e}{C_1} = \frac{1.257 \times 63.92}{0.28} = 286.97nH \quad (5.13)$$

The number of turns needed is thus calculated to be [36]:

$$N = \sqrt{\frac{L(nH)}{A_L}} = \sqrt{\frac{3150000}{286.97}} = 105 \text{ turns} \quad (5.14)$$

The skin depth of copper can be calculated as [38]:

$$\delta_{skin} = \sqrt{\frac{2}{\omega \mu_r \mu_0 \sigma}} = \sqrt{\frac{2}{2\pi f \times 0.777 \times 4\pi \times 10^{7} \times 5.8 \times 10^{7}}} = \sqrt{\frac{5.62}{f(kHz)}} \quad (5.15)$$

At a frequency of 50kHz the skin depth is:

$$\delta_{skin} = \sqrt{\frac{5.62}{50}} = 0.335mm \quad (5.16)$$

Thus will the optimal conductor wire diameter be 0.335×2 = 0.67mm. The optimal conductor area is calculated to be:

$$A_{Cu,\,opt} = 0.355^2 \pi = 0.353mm^2 \quad (5.17)$$

The inductor copper area needed, using a copper density of J=4A/mm$^2$, is:

$$A_{Cu} = \frac{I_{p,\,RMS}}{J} = \frac{3.28}{4} = 0.82mm^2 \quad (5.18)$$

Equations (5.18) and (5.17) implies that the optimal configuration will consist of (0.82/0.353) = 2.32 ≈ 3 strands of 0.67mm wire. However, since the ripple current is 10% of total current it is practical to reduce the number by the same factor or in this case just a single strand. The diameter for a single strand is calculated to be:

$$d = 2\sqrt{\frac{A_{Cu}}{\pi}}$$
$$= 2\sqrt{\frac{0.82}{\pi}}$$
$$= 1.02mm \quad (5.19)$$

The closest practical diameter is 1.12mm. For a copper fill factor of $k_{Cu}$=0.4 [38] the total winding area required is calculated as:

$$A_{Winding} = \frac{A_{Cu}N}{k_{Cu}}$$
$$= \frac{0.985 \times 105}{0.4}$$
$$= 258.56mm^2 \quad (5.20)$$

Since the winding area required is less than the winding area of the E65 bobbin, the windings will fit on to the E65 bobbin.

## 5.3 SELECTING THE POWER DIODES AND SWITCHES

Figure 5.4 shows the equivalent realization of one bridge leg. Diode $D_1$ of figure 5.4 corresponds to diodes $D_1$, $D_3$ and $D_5$ of figure 2.18 (VIENNA rectifier diagramme), and diode $D_2$ of figure 5.4 corresponds to diodes $D_2$, $D_4$ and $D_6$ of figure 2.18. Diodes $D_3$ to $D_6$ in figure 5.4 are used to rectify the input signal to a positive signal only for the switching element.

Figure 5.5 illustrates the current that will flow through each diode during a 360°. In Chapter 3 it was shown that each phase leg switch is controlled by the positive duty cycle output, $D_p$, for four 30° blocks. During these four blocks $D_1$ will act as a freewheeling diode. For the rest of the period $D_1$ will be off. It was also shown in Chapter 3 that each phase leg switch will be active (100% duty cycle) for four 30° blocks, two of which will be when the phase current is positive and the other two when the phase current is negative. In total diode $D_3$ will conduct for six 30° blocks (as indicated on figure 5.5). During the period 30° to 90° the current through D6 is equal to the input current, switched at a high frequency. It must be noted that during this period the switch is operating as the "positive" switch. For the period 90° to 120° the switch is operating as the "transitional" switch which

means the switch is "on" for the duration of this period (duty cycle is equal to 100%). Thus shall the current through D6 be equal to the switch current, which in turn is equal to the input current.

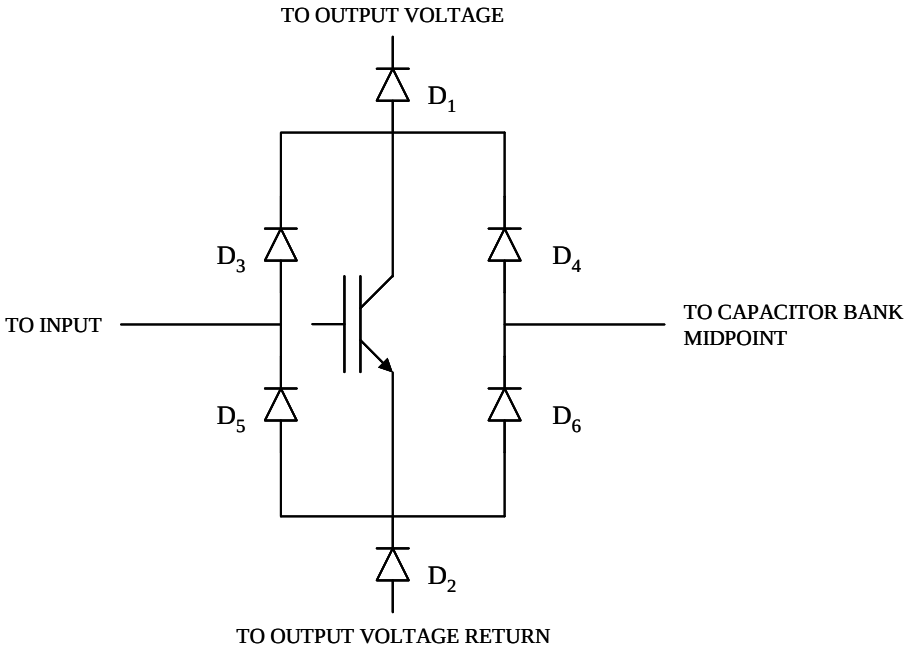



**Figure 5.4.** Single phase leg implementation.

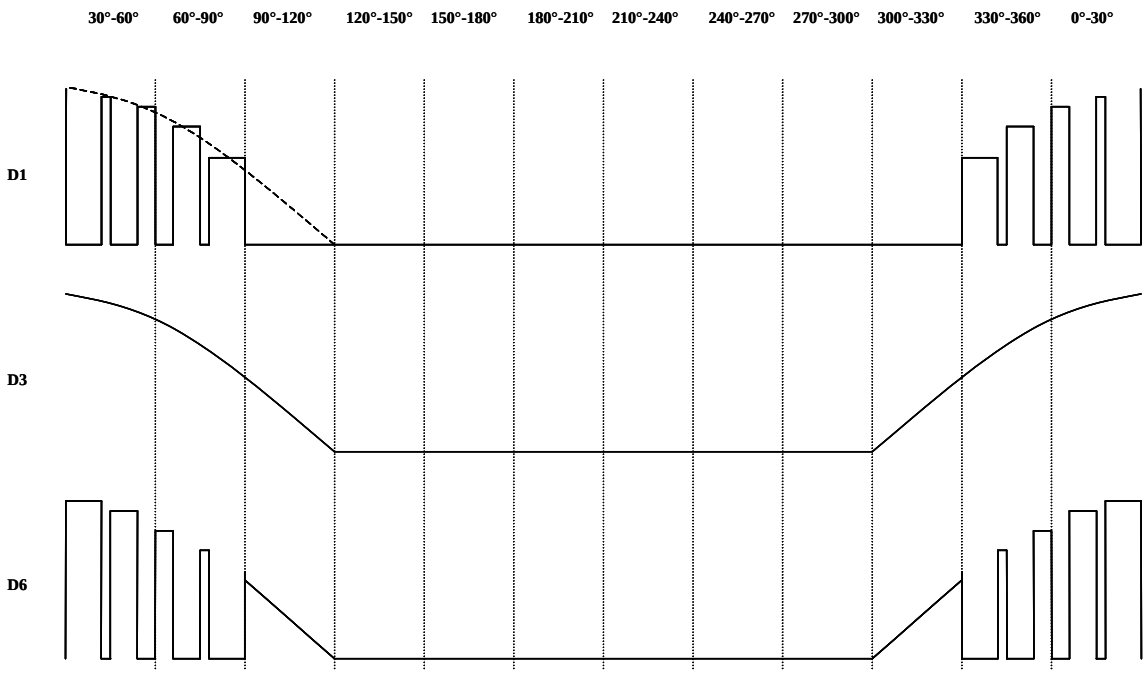



**Figure 5.5.** Diode currents for a line period.

The waveform for $i_{D3}$ was derived by observing that the current flow into $i_{D3}$ (or out of $i_{D5}$) must be equal to the input current and shall thus be sinusoidal (if the input current is sinusoidal). It is also observed that the current through diode $D_1$ shall be equal to the input

current when the switch is off – when the switch is on diode $D_1$ shall be off and the current shall be zero.

Similarly to equation (4.23), $D_p(x)$ is equal to:

$$D_p(x) = 1 - \frac{-V_{p,\,peak}\cos\left(\left(xT_{sw} - T_L\frac{60}{360}\right)\frac{2\pi}{T_L}\right) + 2V_{p,\,peak}\cos\left(\left(xT_{sw}\right)\frac{2\pi}{T_L}\right)}{E + \frac{v_{ripple,\,p-p}}{2}\sin\left(xT_{sw}\frac{360\pi}{30T_L}\right)} \tag{5.21}$$

The current waveform is a cosine waveform with a peak current of $i_{p,peak}$:

$$i_{D3}(t) = i_{p,\,peak}\cos\left(\frac{2\pi}{T_L}t\right) \tag{5.22}$$

$$\therefore i_{D3}(x) = i_{p,\,peak}\cos\left(\frac{2\pi}{T_L}xT_{sw}\right) \tag{5.23}$$

The rms diode current for $D_1$ is calculated for a 60° block and multiplied by 2. Since the current through $D_1$ is equal to the input current for the period $(1\text{-}D_p)$, the rms current can be calculated as:

$$i_{D1,\,rms} = \sqrt{2\left(\frac{1}{T_L}\sum_{x=0}^{y} i_{D3}(x)^2\left(1 - D_p(x)\right)T_{sw}\right)}, \tag{5.24}$$

where:

$$y = round\left(\frac{T_L\frac{60}{360}}{T_{sw}}\right) \tag{5.25}$$

Equating (5.24) for the prototype (see Appendix C for the MATLAB script for evaluating $i_{D1,rms}$, $i_{D3,rms}$ and $i_{D4,rms}$) yields:

$$i_{D1,\,rms} = 1.41A \tag{5.26}$$

It is observed in figure 5.5 that current waveform for $D_3$ is a cosine waveform for the period (30°; 120°] and (300°; 390°], and 0 otherwise. The rms current can thus be calculated for a 90° block and multiplied by 2. Thus substituting equation (5.22) into equation (5.1) yields:

$$i_{D3,\,rms} = \sqrt{\frac{2}{T_L}\int_0^{2\pi\frac{90}{360}} i_{D3}(t)^2}$$
$$= \sqrt{\frac{2}{50^{-1}}\int_0^{T_L\frac{90}{360}} \left(4.64\cos\left(\frac{2\pi t}{50^{-1}}\right)\right)^2}$$
$$= 2.32A \quad (5.27)$$

The rms diode current through $D_6$ is calculated to be:

$$i_{D6,\,rms} = \sqrt{\frac{2}{T_L}\left(\sum_{x=0}^{y} i_{D3}(x)^2 D_p(x) T_{sw} + \int_{2\pi\frac{60}{360}}^{2\pi\frac{90}{360}} i_{D3}(t)^2\right)}$$
$$= 1.76A \quad (5.28)$$

From symmetry the diode currents through diodes $D_2$, $D_5$ and $D_4$ will be:

$$i_{D2,\,rms} = i_{D1,\,rms} = 1.41A \quad (5.29)$$
$$i_{D5,\,rms} = i_{D3,\,rms} = 2.32A \quad (5.30)$$
$$i_{D4,\,rms} = i_{D6,\,rms} = 1.76A \quad (5.31)$$

By observing that the current through the transistor is equal to $i_{D6}$ for a positive input current and equal to $i_{D4}$ for a negative input current, the current through the transistor is calculated to be:

$$i_{T,\,rms} = \sqrt{2} \times i_{D4,\,rms} \quad (5.32)$$
$$= 2.49A \quad (5.33)$$

Table 5.1 lists the various diode and transistor currents comparatively for constant frequency control and hysteresis control, as calculated by using the equations as provided by [13].

**Table 5.1.** VIENNA rectifier diode and switch currents for different control schemes.

| | Constant switching frequency control | Hysteresis control [13] |
|---|---|---|
| $i_{D1,rms} = i_{D2,rms}$ | 1.41A | 1.37A |
| $i_{D3,rms} = i_{D5,rms}$ | 2.32A | 2.32A |
| $i_{D6,rms} = i_{D4,rms}$ | 1.76A | 1.87A |
| $i_{T,rms}$ | 2.49A | 2.65A |

The calculations for the hysteresis controller diode and switch rms currents are shown in Appendix A.

The reverse blocking voltage of the diodes must be half of E + $v_{ripple}/2$ or 368/2 = 184V. The diodes that were chosen for the prototype are STTD506F from SGS Thomson. The diodes have a reverse blocking voltage of 600V, and a forward voltage drop 1.5V. The power losses of the diodes can be computed as:

$$\begin{aligned} P_{loss,\,diodes} &= 3V_f\left(i_{D1,\,rms} + i_{D2,\,rms} + i_{D3,\,rms} + i_{D4,\,rms} + i_{D5,\,rms} + i_{D6,\,rms}\right) \\ &= 1.5\times 3\times\left(1.41+1.41+2.32+1.76+2.32+1.76\right) \\ &= 49.41W \end{aligned} \tag{5.34}$$

The blocking voltage of the switch must be E+$v_{ripple}/2$ or 368V (approximately half of the output voltage). The switches chosen for the prototype are IRG4BC20W IGBTs from International Rectifier. These switches have a 600V reverse blocking voltage. The losses of the power switch can be computed as [37]:

$$\begin{aligned} P_{loss,\,switches} &= 3\left(P_{conduction} + P_{switching}\right). \\ &= 3\left(i_{sw,\,rms}V_{ce,\,sat} + \frac{\left(t_r + t_f\right)i_{sw,\,rms}V_{sw}}{2}\right) \end{aligned} \tag{5.35}$$

Due to the finite "on" resistance of the switches there will be some losses if current flows through the switch. The conduction losses can be computed as [13]:

$$P_{conduction} = i_{sw,\,rms}V_{ce,\,sat}\,, \tag{5.36}$$

where $i_{sw,rms}$ the rms switch current, $V_{ce,sat}$ the switch saturation voltage.

The transistor switching losses are due to the finite current rise and fall times of the switches. During the rise and fall times the current operates in the active region (i.e.

$V_{sw}$ >>0 and $i_{sw}$ >> 0). When the switch is "off" the voltage over the switch will be approximately equal to E (assuming the voltage ripple to be zero). The switching losses can be computed as [13]:

$$P_{switching} = f_L(t_r + t_f) \sum_{all\ switching\ transients} \frac{i_{sw}(t)E}{2}, \tag{5.37}$$

where $t_f$ and $t_r$ are the current fall and rises time respectively.

Figure 5.6 illustrates the voltage over the switch. During the on cycles ($D_p$ and $D_n$) the voltage fall over the switch will be equal to $V_{ce,sat}$.

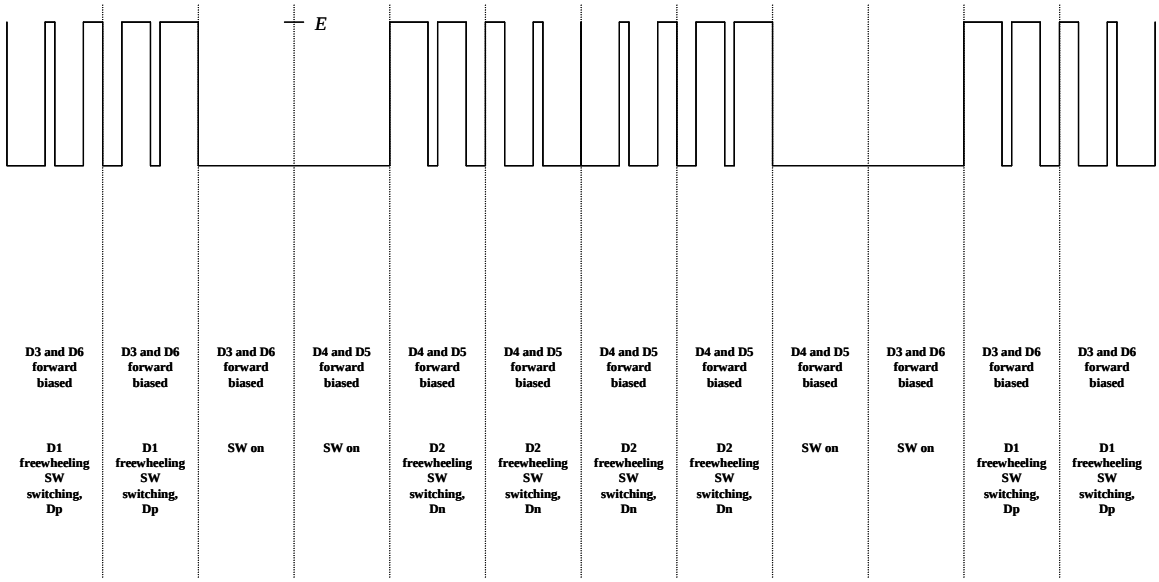



**Figure 5.6.** Transistor voltage for a line period.

For the prototype system the rms switch current was previously computed to be 3.20A. From the IRG4BC20W datasheet the switch voltage in saturation mode is approximately 2.16V. The conduction loss is then approximately (per switch):

$$\begin{aligned} P_{conduction} &= 3.20 \times 2.16 \\ &= 6.912W \end{aligned} \tag{5.38}$$

To compute the switching losses, equation (5.37) can be simplified to:

$$P_{switching} \approx 4(t_r + t_f)\frac{E}{2}\sum_{x=0}^{y} i_{D3}(x), \tag{5.39}$$

where y is equal to:

$$y = round\left(\frac{T_L \frac{60}{360}}{T_{sw}}\right) \tag{5.40}$$

Solving equation (5.37) yields:

$$P_{switching} \approx 50 \times 4\left(14 \times 10^{-9} + 96 \times 10^{-9}\right) \times \frac{350}{2} \times 643.79 = 2.48W \tag{5.41}$$

The total power loss for the switches (from (5.35)) is thus:

$$\begin{aligned} P_{loss,\,switches} &= 3 \times \left(6.912 + 2.48\right) \\ &= 3 \times 9.39 \\ &= 28.18W \end{aligned} \tag{5.42}$$

## 5.4 SYSTEM EFFICIENCY

From [38] the core loss for 3F3 type or equivalent material, of the inductor can be computed by the equation:

$$P_{loss,\,inductor\_core,\,v} = 1.5 \times 10^{-6} f^{1.5} B_{ac}{}^{2.5}, \tag{5.43}$$

where $B_{ac}$ is in mT and f in kHz. It is assumed that the input current is sinusoidal. From the Ferroxcube databook [36] the magnetic field intensity in the air gap is:

$$\begin{aligned} H_{gap} &= \frac{\hat{I}N}{gap} \\ &= \frac{i_{phase,\,peak}N}{gap} \\ &= \frac{4.64 \times 105}{4 \times 10^{-3}} \\ &= 121800At/m \end{aligned} \tag{5.44}$$

From [35] the maximum flux density is:

$$\begin{aligned} \hat{B} &= 4\pi 10^{-7} H_{gap} \\ &= 4\pi 10^{-7} \times 121800 \\ &= 153mT \end{aligned} \tag{5.45}$$

The peak-to-peak flux density can be computed as:

$$\begin{aligned} B_{ac} &= 2\hat{B} \\ &= 306mT \end{aligned} \tag{5.46}$$

Substituting (5.46) into (5.43) yields:

$$\begin{aligned} P_{loss,\,inductor\_core,\,v} &= 1.5\times10^{-6}\times\left(\frac{50}{1000}\right)^{1.5}\times306^{2.5} \\ &= 27.47mW/cm^3 \end{aligned} \tag{5.47}$$

From the Ferroxcube databook [36] the volume for an E65 core pair is 79cm$^3$. Multiplying the core volume with equation (5.47) yields:

$$\begin{aligned} P_{loss,\,inductor\_core} &= 27.47\times79 \\ &= 2.17W \end{aligned} \tag{5.48}$$

It was stated earlier that 1.12mm diameter wire is used. The resistance of wire can be estimated as [38]:

$$\begin{aligned} \Omega_{wire} &= \rho\frac{l}{A_{Cu}} \\ &= \rho\frac{Nl_{eff}}{A_{Cu}} \end{aligned} \tag{5.49}$$

where N is the number of turns, ρ the resistivity of the wire and equal to $2.2\times10^{-8}$ at 25°C [38], $l_{eff}$ the effective length of one turn and $A_{Cu}$ the copper area of the wire. From the Ferroxcube databook [36] $l_{eff} \approx 119$mm. The copper area of the wire, $A_{Cu}$, is equal to $\pi\cdot(1.2/2)^2 = 1.131$mm$^2$. Substituting the wire parameters into equation (5.49) yields:

$$\begin{aligned} \Omega_{wire} &= 2.2\times10^{-8}\frac{105\times119\times10^{-3}}{1.131\times10^{-6}} \\ &= 0.243\Omega \end{aligned} \tag{5.50}$$

The power loss due to the finite resistance of the wire can be computed as:

$$\begin{aligned} P_{loss,\,inductor\_winding} &= i_{rms}{}^2\Omega_{wire} \\ &= \left(\frac{i_{phase,\,peak}}{\sqrt{2}}\right)^2\Omega_{wire} \\ &= \left(\frac{4.64}{\sqrt{2}}\right)^2\times0.243 \\ &= 2.62W \end{aligned} \tag{5.51}$$

The total inductor loss for the system is calculated to be:

$$\begin{aligned} P_{loss,\,inductor\_system} &= 3\left(P_{loss,\,inductor\_core} + P_{loss,\,inductor\_winding}\right), \\ &= 3(2.17 + 2.62) \\ &= 14.37W \end{aligned} \tag{5.52}$$

The total power loss for the system is calculated to be, at full load:

$$P_{loss,\,system} > P_{loss,\,inductor\_system} + P_{loss,\,switches} + P_{loss,\,diodes} = 96.46W \tag{5.53}$$

The estimated efficiency of the system can be calculated as (at full load, and 176$V_{LL}$):

$$\begin{aligned} \eta &< 100 \times \frac{P_{load}}{P_{load} + P_{loss,\,system}}\% \\ &< 100 \times \frac{1000}{1000 + 96.46} \\ &\therefore \eta < 91.2\% \end{aligned} \tag{5.54}$$

## 5.5 IGBT GATE DRIVE CONSIDERATIONS

From [39] the maximum gate resistance needed for switching on the IGBT is:

$$R_{G,\,ON} = \frac{V_{BOOT\_SUPPLY} - 1.5V}{I_{OL,\,PEAK}}, \tag{5.55}$$

where $I_{OL,PEAK}$ is the peak gate current, and is chosen to be less than 500mA. Substituting into equation (5.55), with the bootstrap supply equal to 18V, yields:

$$R_{G,\,ON} = \frac{18V - 1.5V}{0.5} = 33\Omega \tag{5.56}$$

From [39] the maximum gate resistance needed for switching off the IGBT is:

$$R_{G,\,OFF} = \frac{V_{BOOT\_SUPPLY} - 1.5V}{I_{OL,\,PEAK}}, \tag{5.57}$$

where $I_{OL,PEAK}$ is the peak gate current, and is chosen to be less than 2.0A (the maximum sink current for the HCPL-316J IGBT gate driver). Substituting into equation (5.57), with the bootstrap supply equal to 18V, yields:

$$R_{G,\,OFF} = \frac{18V - 1.5V}{2} = 8.25\Omega \approx 8.2\Omega, \tag{5.58}$$

## 5.6 POWER DERATING OF THE VIENNA RECTIFIER PROTOTYPE FOR LOWER INPUT VOLTAGES

By using equations (5.24), (5.27) and (5.28), the diode current stress can be computed for lower input voltages if the input current does not exceed the maximum of $i_{peak,rms}$ (equal to approximately 3.3A for the proposed prototype). Shown in figure 5.7 to figure 5.12 are the relevant semiconductor, output and input voltages and/or currents for derated input voltage/output power. The MATLAB script for deriving the relevant graphs is given in Appendix C.

For use of the rectifier for converting a generator input to a DC voltage the maximum permissible output power is derated linearly with the input voltage, e.g. for a phase voltage of 63.5V (half of the minimum permissible input current for 1kW output loading) the maximum permissible output power shall be 500W, as shown in figure 5.7. All graphs are normalized for rated power (1000W) and rated line-to-line voltage (220V). Thus for example shall a normalized input voltage of 0.6 be equal to 132V. The derating curve shown in figure 5.7 was derived by keeping the input current fixed at 2.62A (rms), which is the input current for a 1000W output power at $V_{LL}$ = 220V input. This was done to ensure that none of the diodes or switches exceeds their specified current ratings.

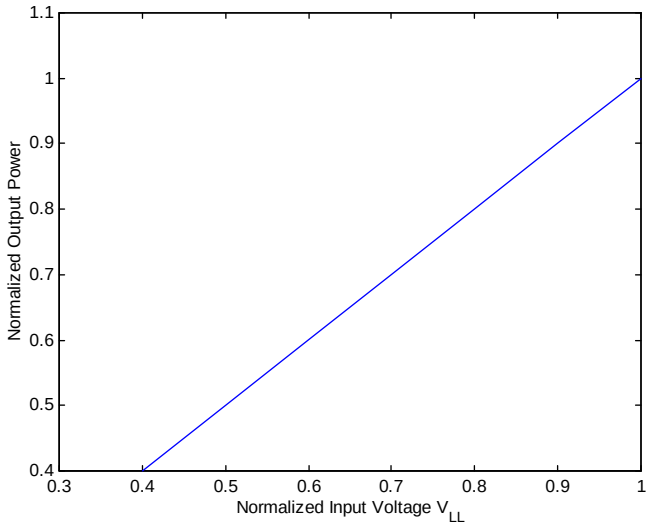



**Figure 5.7.** Output Power versus rms input voltage.

The largest portion of the current that will flow through $i_{D1,rms}$ is equal to the output current. It is thus understandable that the derated rms current will exhibit a waveform

similar to the derated voltage/power waveform, and shall decrease as the input voltage decreases.

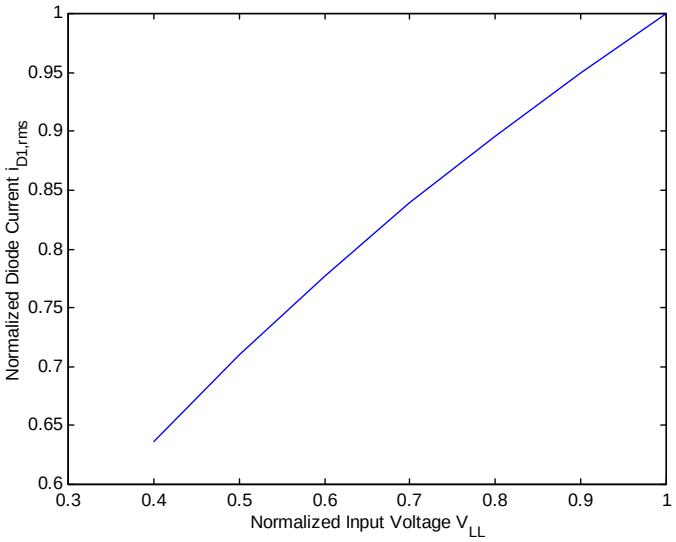



**Figure 5.8.** RMS current for diodes 1 and 2 versus rms input voltage.

Figure 5.9 is self explanatory, since it is observed that $i_{D3,rms}$ is proportionally equal to rms input current and the ratio $P_{OUT}/V_{IN}$ remains constant for all scaled inputs.

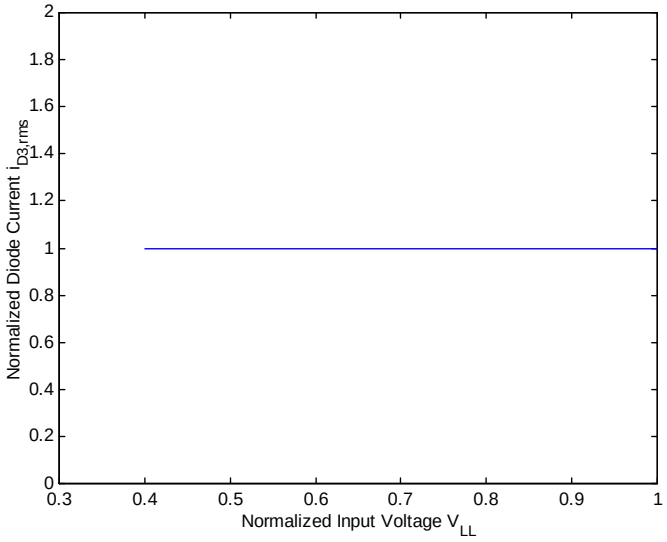



**Figure 5.9.** RMS current for diodes 3 and 5 versus rms input voltage.

From equation (5.32) it is known that $i_{D4,rms} \propto i_{T,rms}$. From figure 5.4 it is concluded that $i_{T,rms} \propto (i_{D3,rms}-i_{D1,rms})$. It has already been mentioned that $i_{D3,rms}$ stays constant for all derated Power/Voltage levels. Thus as the power/voltage level decreases, and $i_{D1,rms}$ decrease (which is approximately equal to the output current), the switch current $i_{T,rms}$ and thus also $i_{D4,rms}$ and $i_{D6,rms}$ will increase.

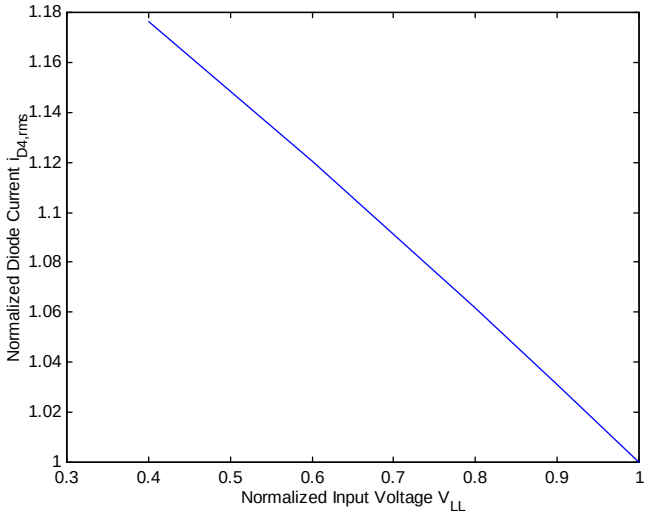



**Figure 5.10.** RMS current for diodes 4 and 6 versus rms input voltage.

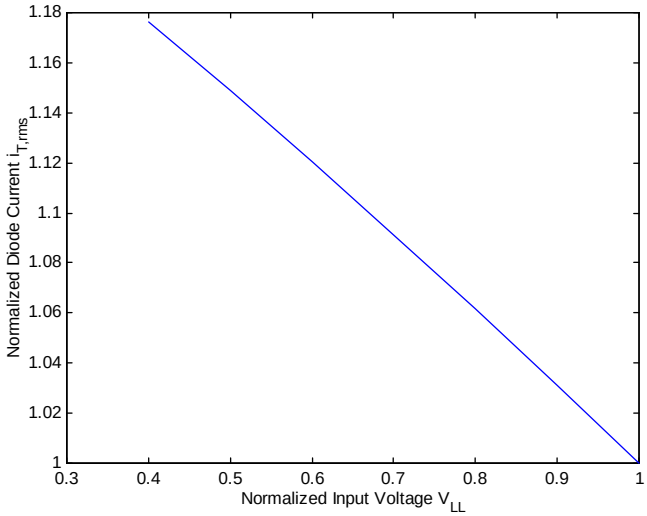



**Figure 5.11.** RMS current for the switch versus rms input voltage.

The capacitor ripple current is mainly dependant on the output current, thus the capacitor ripple current will decrease as the output power decreases, as shown in figure 5.12. The reason for the slight parabolic shape of the derating curve is because the current ripple component of $i_p(t)$ and $i_n(t)$ will remain at a fixed level independent of the input voltage or output current and thus shall some component of the capacitor ripple current not derate linearly as the output power levels decrease.

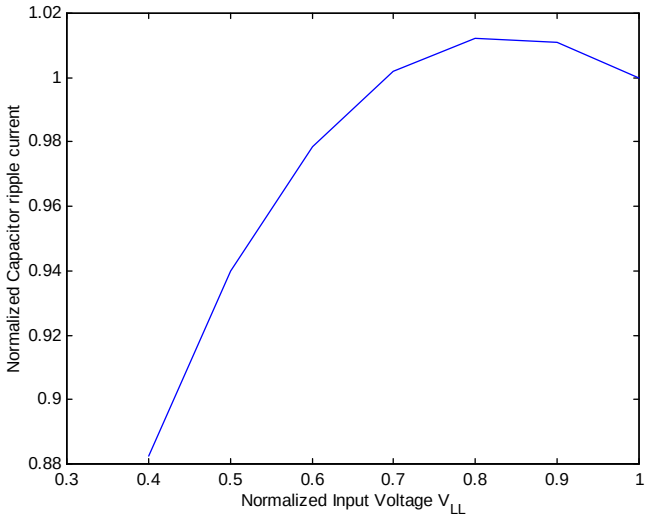



**Figure 5.12.** RMS capacitor ripple current versus rms input voltage.

From equation (4.20) it is known that the mid-point capacitor voltage ripple is proportional to the discharge current minus the charge current. The capacitor mid-point voltage ripple shall thus decrease, since the discharge current (or output current) decreases with the derated and lower input voltage, as shown in figure 5.13.

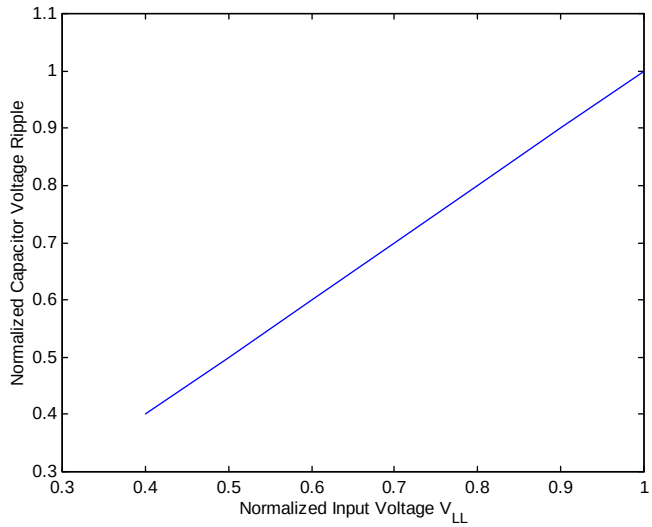



**Figure 5.13.** Output capacitor band mid-point voltage ripple versus rms input voltage.

## 5.7 CHAPTER CONCLUSION

This Chapter discussed in detail the power stage design of the VIENNA rectifier, which included the sizing of the output capacitors and the type of capacitors to be used; design of the input inductors and associated power loss; choice of the diodes to be used; and the choice of switch to be used. An efficiency calculation was also performed to determine the associated performance of the VIENNA rectifier in terms of power. Derating curves were also provided that shows the current and voltage stress of the VIENNA rectifier for lower input voltages (typically for generator inputs). Since all of the semiconductor components were suitably derated the proposed VIENNA rectifier will be able to operate at a derated input voltage with associated derated output power.

# CHAPTER 6

# RESULTS AND DISCUSSION

## 6.1 INTRODUCTION

A prototype was designed and built to verify the theoretical and predicted performance. In this Chapter simulated and experimental results are shown. Results were captured for very low (but still in continuous conduction mode of operation) to full loading on the outputs. The following results are presented:

- Input current waveforms;
- Harmonic distortion;
- Output voltage waveforms;
- Capacitor neutral voltage waveforms;
- Input current and input voltage phase displacement power factor;
- Output voltage load step response;
- and, System efficiency.

The digital simulations were performed for a sampling frequency of 25kHz, which was determined to be the lowest sampling frequency for acceptable performance (in Chapter 4).

It must be noted that the experimental prototype featured an analogue controller.

### 6.1.1. Experimental prototype

The experimental prototype designed and built is shown in figure 6.1.1.

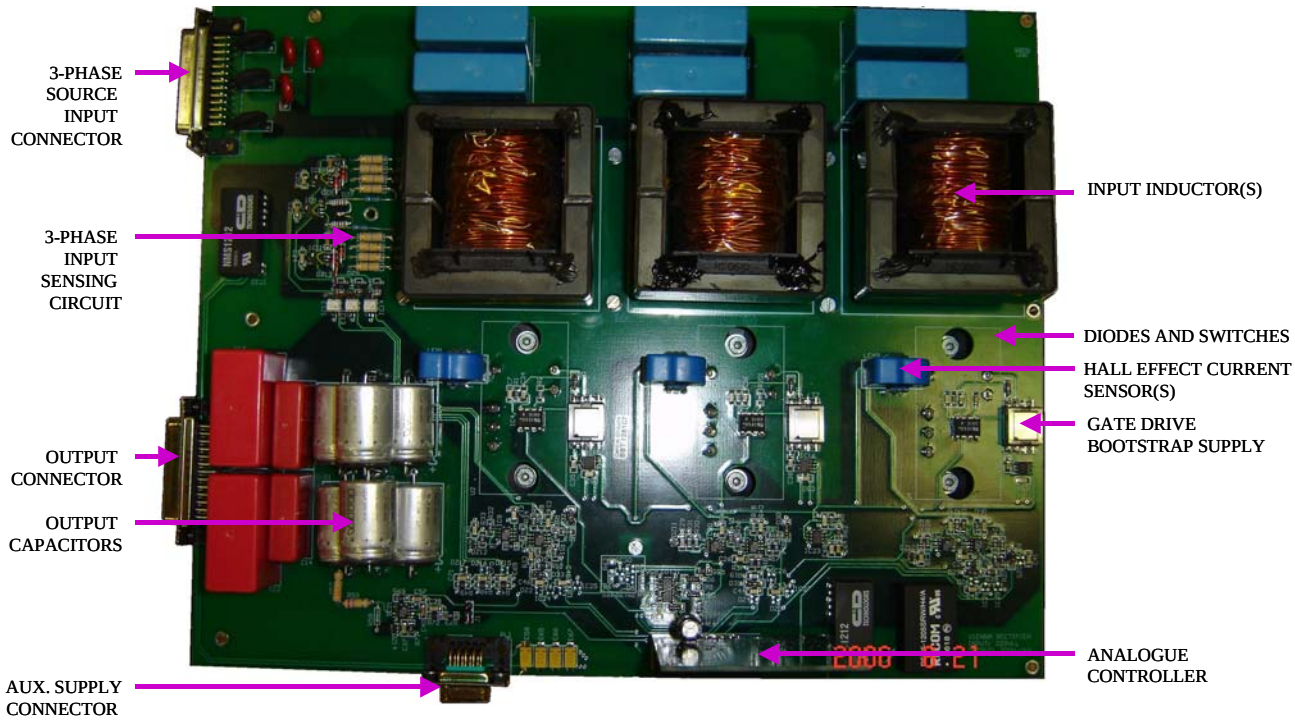
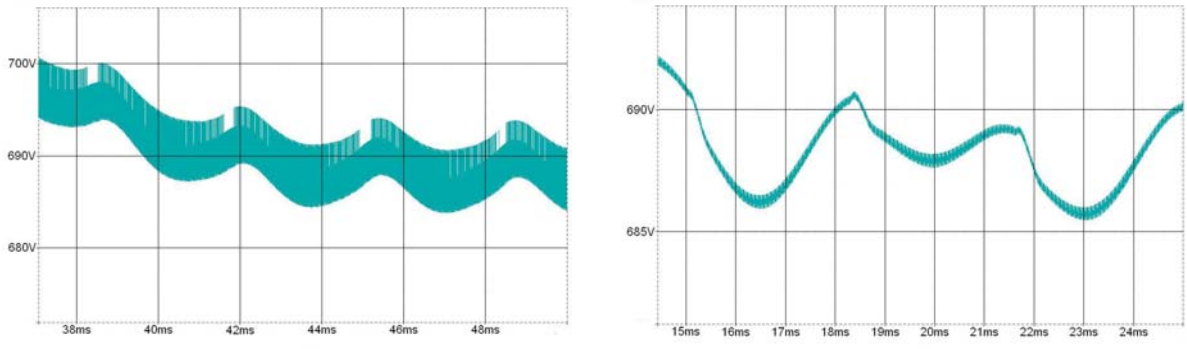



**Figure 6.1.1.** VIENNA rectifier experimental prototype.

### 6.1.2. Differences between PSpice simulation and MATLAB simulation

The ESR (equivalent series resistance) for the output capacitors was chosen to be at its maximum for the PSpice simulation (equal to 0.8Ω). Figure 6.1.2 show the output voltage waveforms for an ESR of 8Ω and 0Ω respectively. For the MATLAB simulation the ESR is equal to zero. It should also be noted that the average output voltage for the PSpice simulation is slightly less than 700V due to component tolerances.

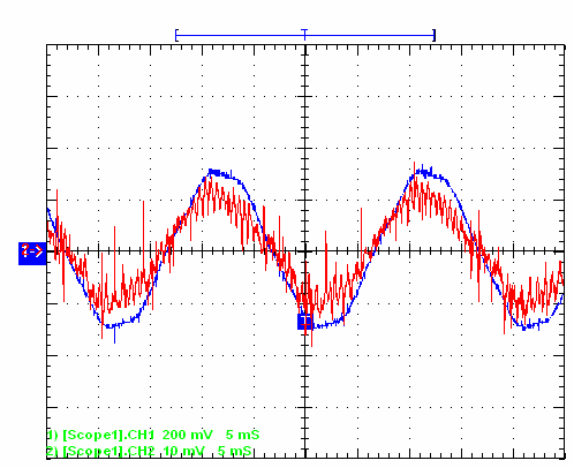



(a) ESR of 0.8Ω. (b) ESR of 0Ω.

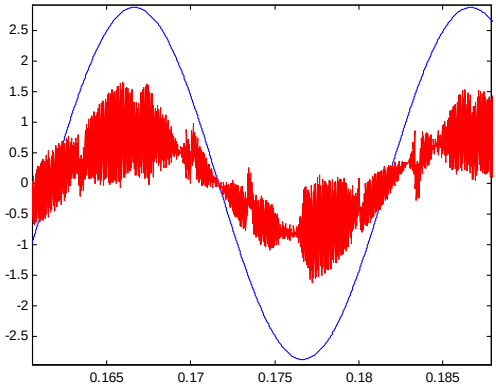
**Figure 6.1.2.** Effect of the ESR on the output voltage (shown for the PSpice simulation).

## 6.2 INPUT CURRENT AND INPUT VOLTAGE WAVEFORMS

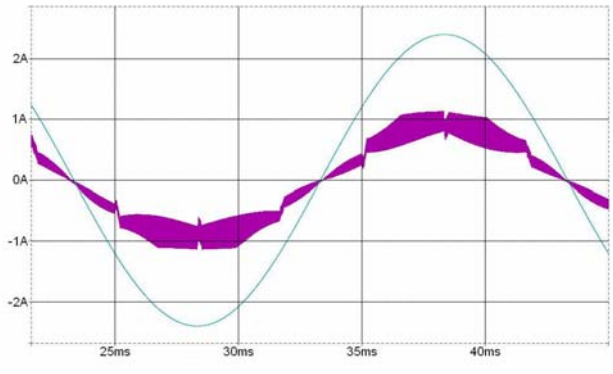
### 6.2.1 200W Output Power, $V_{LL}$ = 176V input voltage




(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 1A/div and time scale 5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).




(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

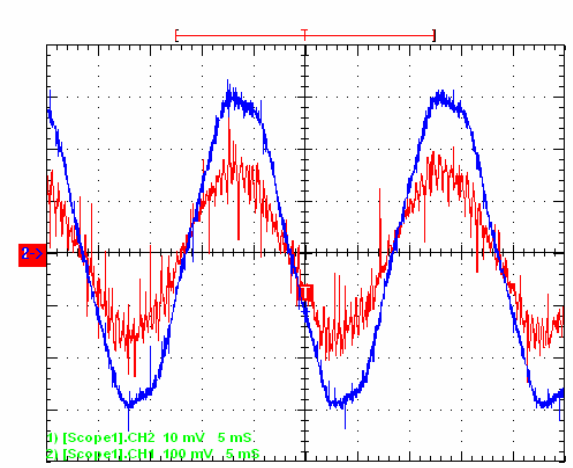
**Figure 6.2.1.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 200W.

Figure 6.2.1 shows the waveforms obtained for an output loading of 200W and an input voltage of 176V. The input current waveform obtained for the prototype (figure 6.2.1(a)) shows that the current is continuous. The ripple current is high in proportion to the current amplitude, as can be expected for low output power conditions. The prototype's measured waveform is similar to that obtained through the PSpice simulation. It can, however, be

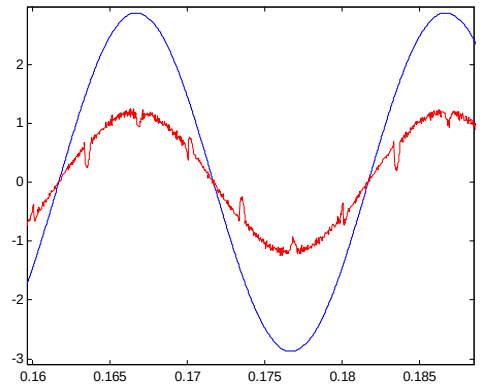
seen that simulated digital controlled rectifier has poor low power performance (i.e. higher ripple component as seen in figure 6.2.1(b)). It is observed from figure 6.2.1(a) that the peak-to-peak ripple current (high frequency ripple, i.e. not the 50Hz signal) is approximately 0.5A. This corresponds well to the designed-for ripple current of 0.46A (refer to section 4.3). This verifies the inductor design analysis performed in section 4.1 of Chapter 4.

From figure 6.2.1 it is evident that the input current is in phase with the input voltage. The displacement power factor, which is defined as the cosine of the displacement angle between the input current and input voltage, therefore approximates 1. This suggests that the VIENNA rectifier, with dual-boost constant switching frequency control, is suited for power factor correction applications. It is evident from figure 6.2.1(a) that the input current is in phase with the input voltage even at low power levels.

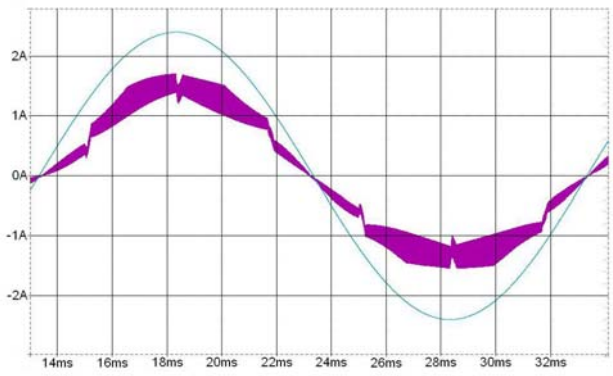
### 6.2.2 300W Output Power, $V_{LL}$ = 176V input voltage




(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 1A/div and time scale 5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).




(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

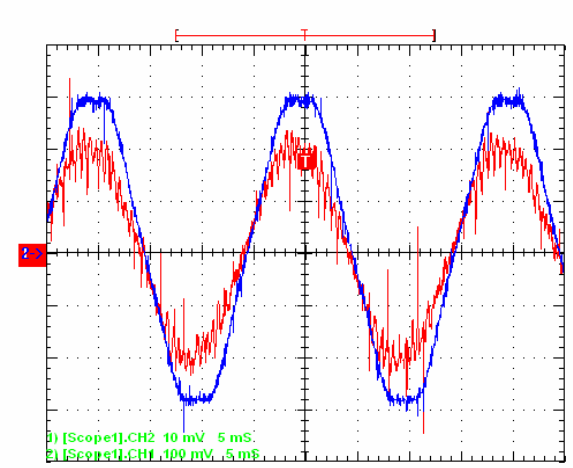
**Figure 6.2.2.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 300W.

Figure 6.2.2 shows the waveforms obtained for an output loading of 300W and an input voltage of 176V. The input current waveform obtained for the prototype (figure 6.2.2(a)) shows that the current is continuous, with the ripple current still high in proportion to the current amplitude. The prototype's measured waveform is similar to that obtained through the PSpice simulation. The current waveform for the simulated digital controlled rectifier is much improved compared with what it was for 200W output power loading and is now comparable to the current waveform captured for the analogue type controller. The ripple

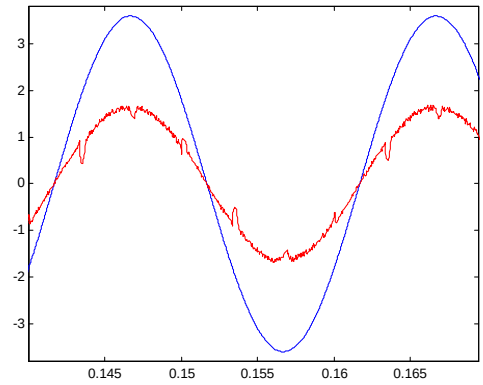
current amplitude is the same as for 200W loading, and is thus independent of output loading (as is to be expected from equation (4.11)).

From figure 6.2.2 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1.

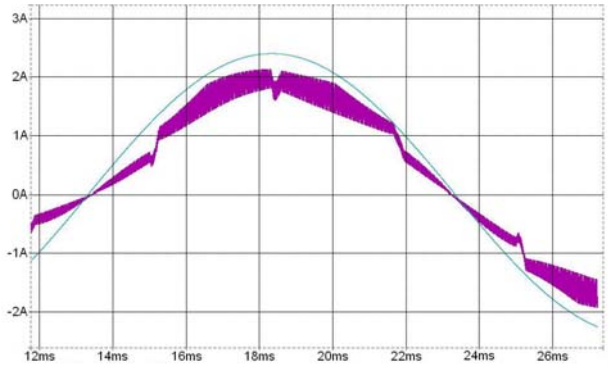
### 6.2.3 400W Output Power, $V_{LL}$ = 176V input voltage




(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 1A/div and time scale 5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).




(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

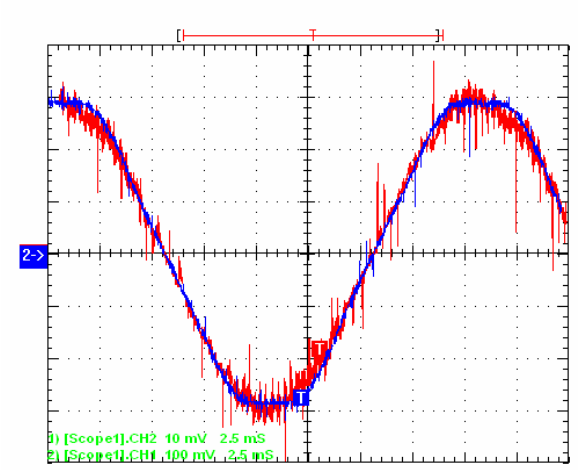
**Figure 6.2.3.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 400W.

Figure 6.2.3 shows the waveforms obtained for an output loading of 400W and an input voltage of 176V. The input current waveform obtained for the prototype (figure 6.2.3(a)) shows that the current is continuous, with the ripple current still fairly high in proportion to the current amplitude. The prototype's measured waveform is similar to that obtained through the PSpice simulation. The current waveform for the simulated digital controlled rectifier is much more improved compared with what it was for lower output power loadings and is now similar when compared to the analogue type controller prototype and

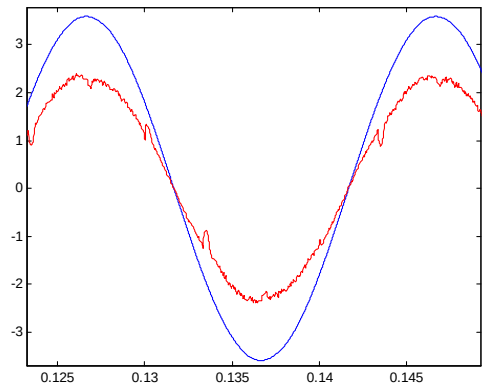
simulated waveforms. The current ripple is approximately 0.5A (peak-to-peak), as was measured for lower power levels at 176V.

From figure 6.2.3 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1.

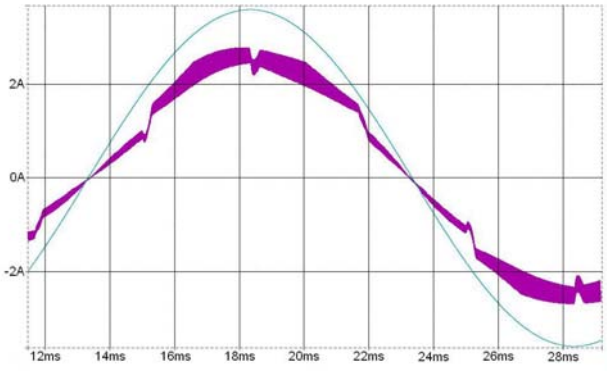
### 6.2.4 550W Output Power, $V_{LL}$ = 176V input voltage




(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 1A/div and time scale 2.5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).



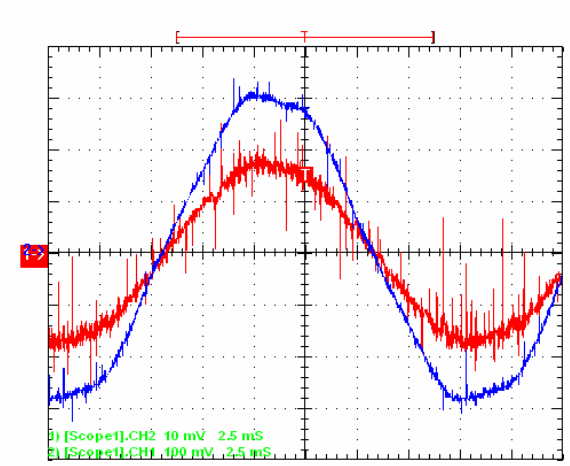

(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.2.4.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 550W.

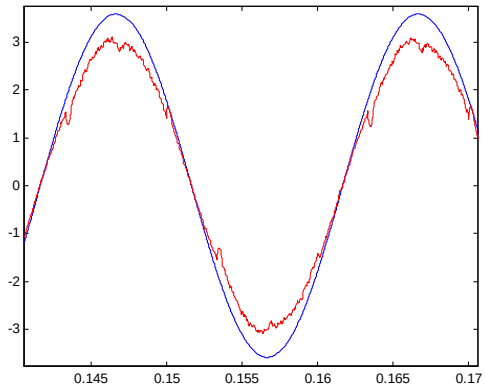
Figure 6.2.4 shows the waveforms obtained for an output loading of 550W and an input voltage of 176V. The input current waveform obtained for the prototype (figure 6.2.4(a)) shows that the current is continuous, with the ripple current low in proportion to the current amplitude. The prototype's measured waveform is similar to that obtained through the PSpice simulation. The current waveform for the simulated digital controlled rectifier is comparable to the analogue type controller prototype and simulated waveforms, in terms of ripple current and shape.

From figure 6.2.4 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1.

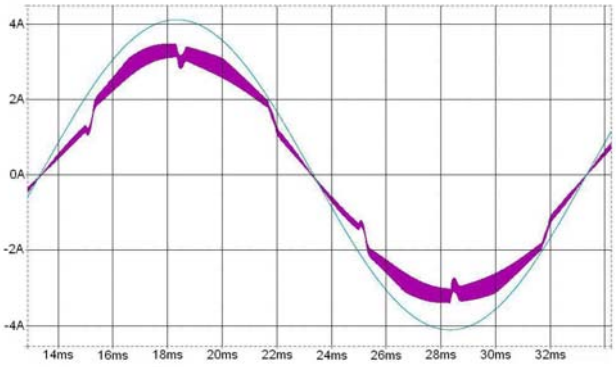
### 6.2.5 700W Output Power, $V_{LL}$ = 176V input voltage




(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 2A/div and time scale 2.5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).




(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

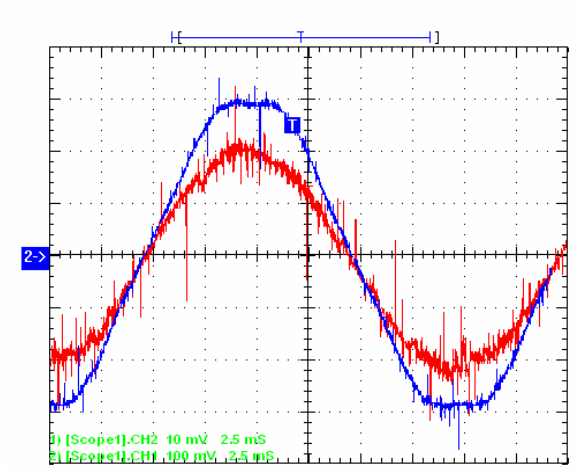
**Figure 6.2.5.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 700W.

Figure 6.2.5 shows the waveforms obtained for an output loading of 700W and an input voltage of 176V. The input current waveform obtained for the prototype (figure 6.2.5(a)) shows that the current is continuous, with the ripple current low in proportion to the current amplitude. EMI noise is more evident in the waveform for the prototype (figure 6.2.5(a)), than for the lower power levels. The prototype's measured waveform is similar to that obtained through the PSpice simulation. The current waveform for the simulated digital

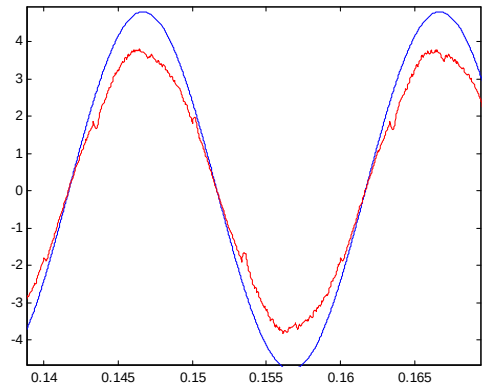
controlled rectifier is comparable to the analogue type controller prototype and simulated waveforms, in terms of ripple current and shape.

From figure 6.2.5 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1.

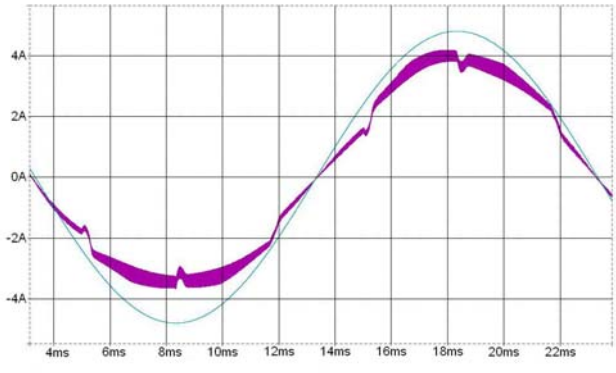
### 6.2.6 850W Output Power, $V_{LL}$ = 176V input voltage




(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 2A/div and time scale 2.5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).



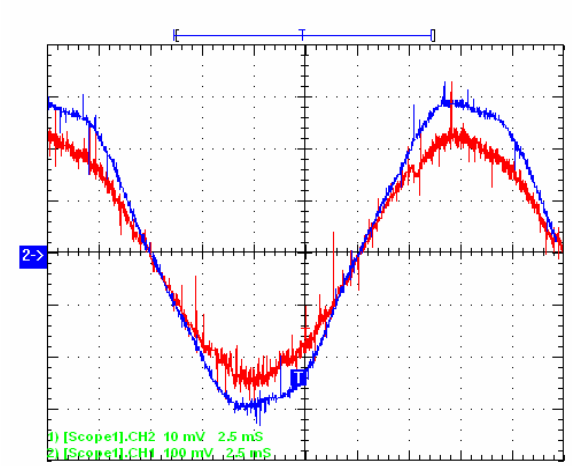

(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.2.6.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 850W.

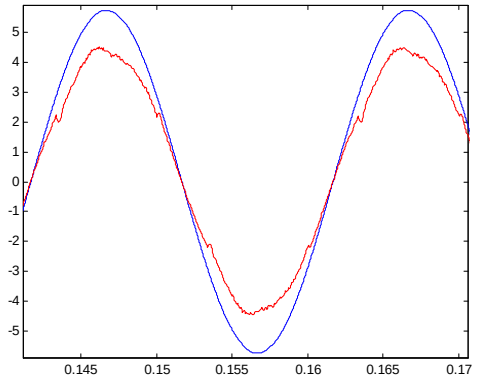
Figure 6.2.6 shows the waveforms obtained for an output loading of 850W and an input voltage of 176V. The input current waveform obtained for the prototype (figure 6.2.6a) shows that the current is continuous, with the ripple current low in proportion to the current amplitude. EMI noise is again fairly evident in the waveform for the prototype (figure 6.2.6a). The prototype's measured waveform is similar to that obtained through the PSpice simulation.

From figure 6.2.6 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1.

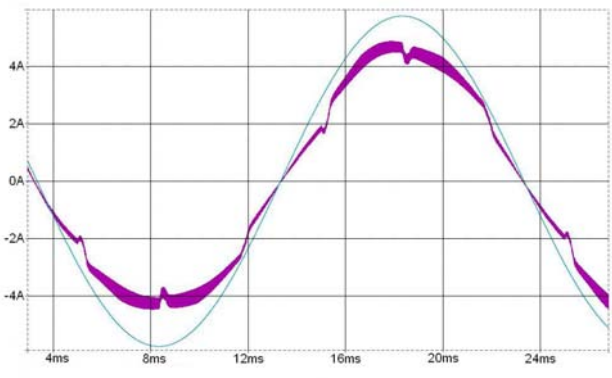
### 6.2.7 1000W Output Power, $V_{LL}$ = 176V input voltage




(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 2A/div and time scale 2.5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).




(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

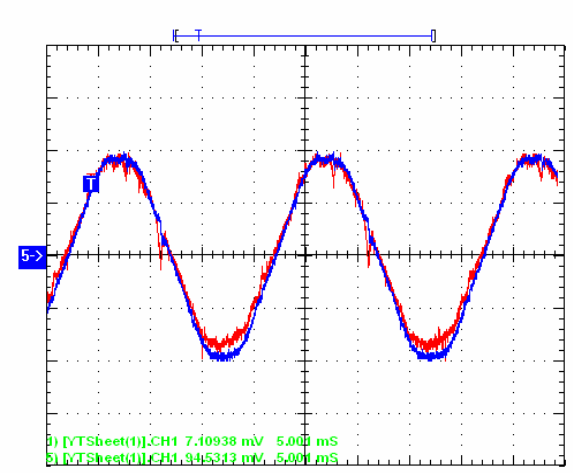
**Figure 6.2.7.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 1000W.

Figure 6.2.7 shows the waveforms obtained for an output loading of 1000W and an input voltage of 176V. The input current waveform obtained for the prototype (figure 6.2.7(a)) shows that the current is continuous, with the ripple current low in proportion to the current amplitude. EMI noise is again fairly evident in the waveform for the prototype (figure 6.2.7(a)). The prototype's measured waveform is similar to that obtained through the PSpice simulation. From the PSpice simulation it is evident that the current ripple (high frequency ripple) is 0.5A (peak-to-peak), as was measured for lower power levels at 176V.

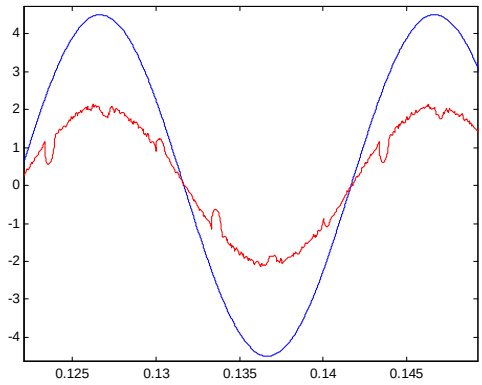
The shape of the current waveforms for the experimental prototype, PSpice simulation and MATLAB simulation are all similar.

From figure 6.2.7 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1. It is evident from figure 6.2.7(a) that the input current is in phase with the input voltage even at very high output loading.

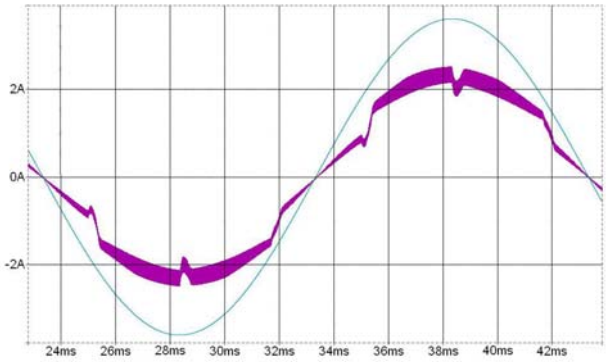
### 6.2.8 300W Output Power, $V_{LL}$ = 110V input voltage



(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 1A/div and time scale 5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).



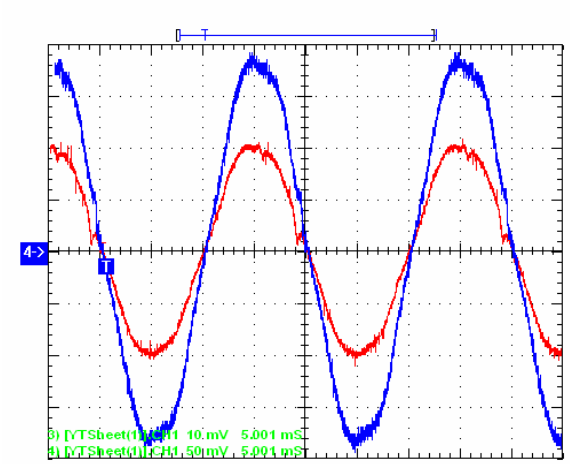

(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.2.8.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 110V and output load of 300W.

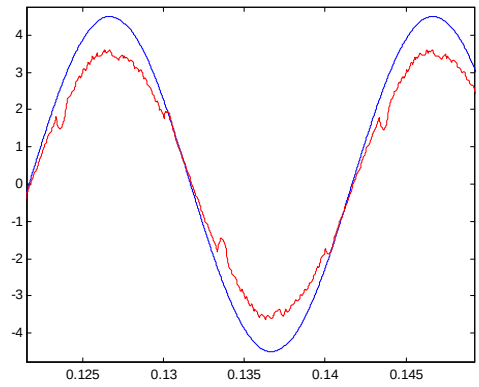
Figure 6.2.8 shows the waveforms obtained for an output loading of 300W and an input voltage of 110V. The input current waveform obtained for the prototype (figure 6.2.8(a)) shows that the current is continuous, with the ripple current low in proportion to the current amplitude. The prototype's measured waveform is similar to that obtained through the PSpice simulation. It is observed from figure 6.2.8(c) that the peak-to-peak ripple current (high frequency ripple) is approximately 0.4A. This corresponds well to the predicted ripple current of 0.384A (refer to section 4.3) for an 110V input voltage.

From figure 6.2.8 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1. This suggests that the VIENNA rectifier is suited for power factor correction applications for a derated input voltage and low output loading. It is evident from figure 6.2.8(a) that the input current is in phase with the input voltage even at derated input voltages and derated power levels.

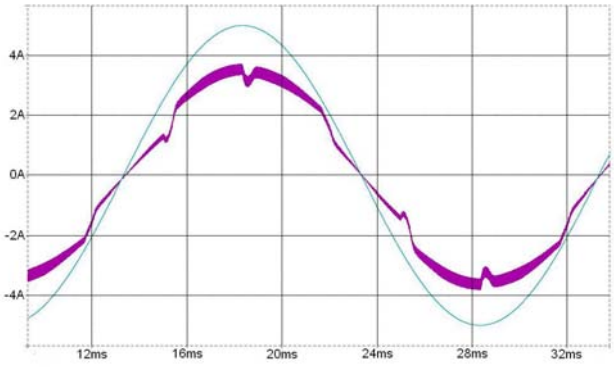
### 6.2.9 500W Output Power, $V_{LL}$ = 110V input voltage



(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 2A/div and time scale 5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).



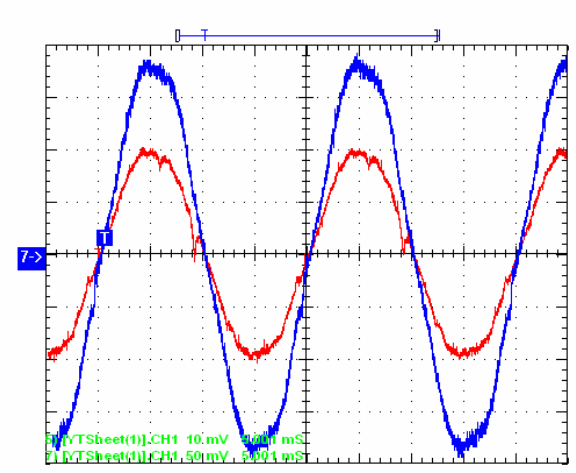

(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.2.9.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 110V and output load of 500W.

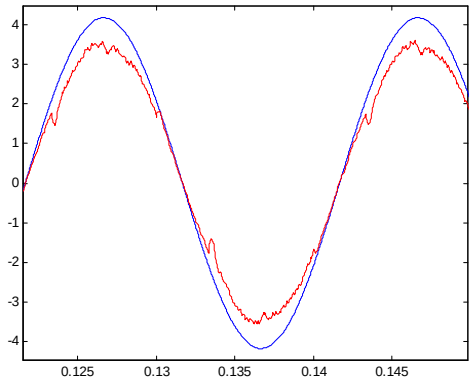
Figure 6.2.9 shows the waveforms obtained for an output loading of 500W and an input voltage of 110V. The input current waveform obtained for the prototype (figure 6.2.9(a)) shows that the current is continuous, with the ripple current low in proportion to the current amplitude. The prototype's measured waveform is similar to that obtained through the PSpice simulation. The ripple current is 0.4A, which is the same as for lower power levels (i.e. as observed in section 6.2.8). The current waveform is comparable and similar to the waveform captured for 1kW, 176V operation.

From figure 6.2.9 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1. This suggests that the VIENNA rectifier is suited for power factor correction applications for a derated input voltage and equally derated output loading (for instance the input voltage and the output loading is derated by 50%).

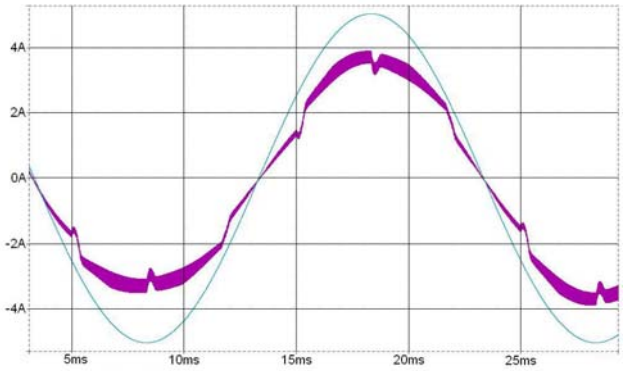
### 6.2.10 700W Output Power, $V_{LL}$ = 154V input voltage



(a) Experimental prototype input current (red trace) and scaled voltage (blue trace). Current amplitude scale is 2A/div and time scale 5ms/div.




(b) MATLAB simulated (digital controller) input current (red trace) and scaled input voltage (blue trace).




(c) PSpice simulated (analogue controller) input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.2.9.** Input current and input voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 110V and output load of 700W.

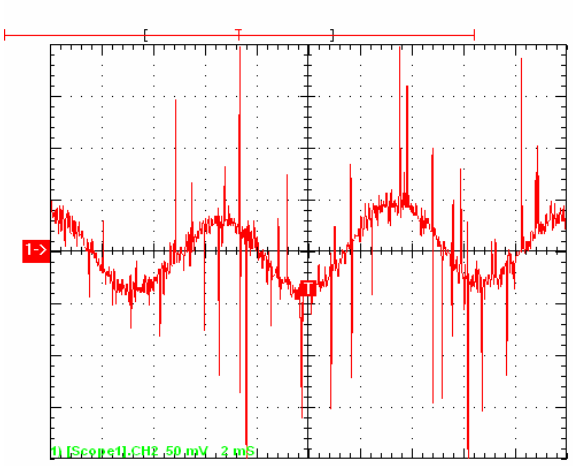
Figure 6.2.10 shows the waveforms obtained for an output loading of 700W and an input voltage of 154V. The input current waveform obtained for the prototype (figure 6.2.10(a)) shows that the current is continuous, with the ripple current low in proportion to the current amplitude. The prototype's measured waveform is similar to that obtained through the PSpice simulation. It is observed from figure 6.2.10(c) that the peak-to-peak ripple current (high frequency ripple, i.e. not the 50Hz signal) is approximately 0.5A. This corresponds

well to the predicted ripple current of 0.476A (refer to section 4.3) for a 154V input voltage.

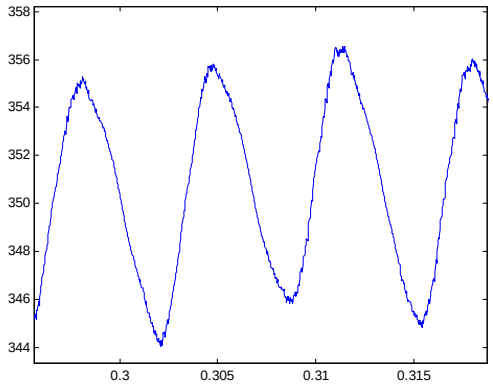
From figure 6.2.10 it is evident that the input current is in phase with the input voltage. The displacement power factor approximates 1. This suggests that the VIENNA rectifier is suited for power factor correction applications for a derated input and derated output.

## 6.3 OUTPUT CAPACITOR BANK NEUTRAL POINT VOLTAGE RIPPLE

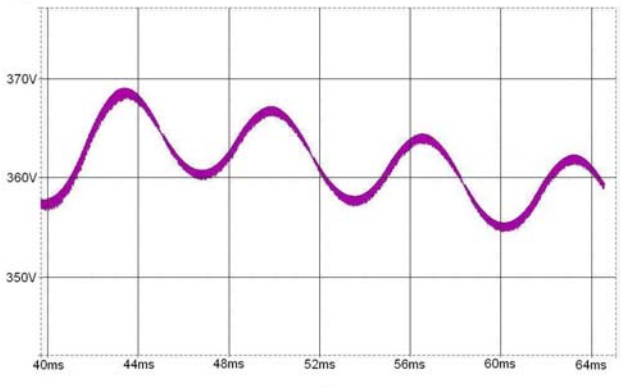
### 6.3.1 200W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 2ms/div. Average mid-point voltage of 349V.




(b) MATLAB Simulation (digital controller).

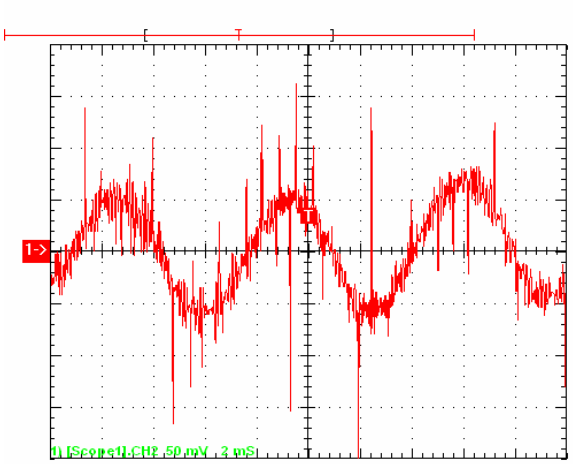



(c) PSpice Simulation (analogue controller).

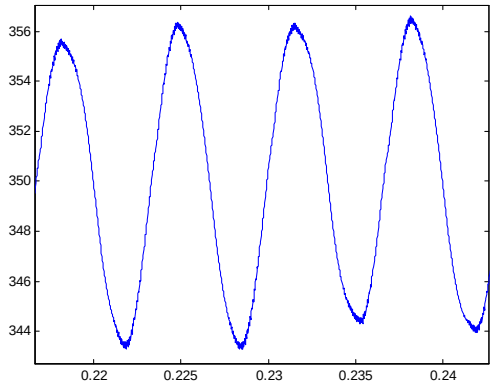
**Figure 6.3.1.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 200W.

Figure 6.3.1 shows the output capacitor bank neutral voltage for an output power level of 200W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of $7.475V_{p\text{-}p}$ (predicted using equation (4.20)), for an output power level of 200W. The high frequency noise that can be seen in figure 6.3.1(a) is due to radiated EMI noise that is picked up by the measurement probe. It is observed the mid-point voltage ripple is at three times the supply frequency, as was established in section 4.2.

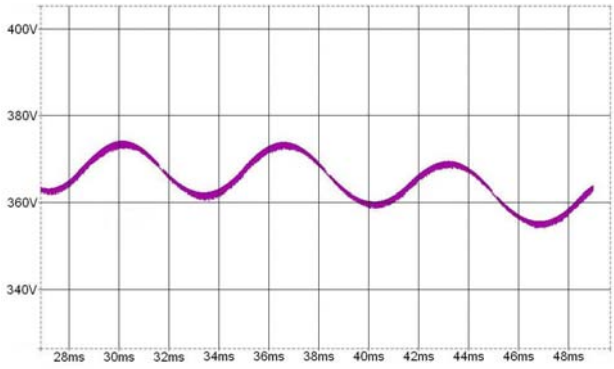
### 6.3.2 300W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 2ms/div. Average mid-point voltage of 349V.




(b) MATLAB Simulation (digital controller).

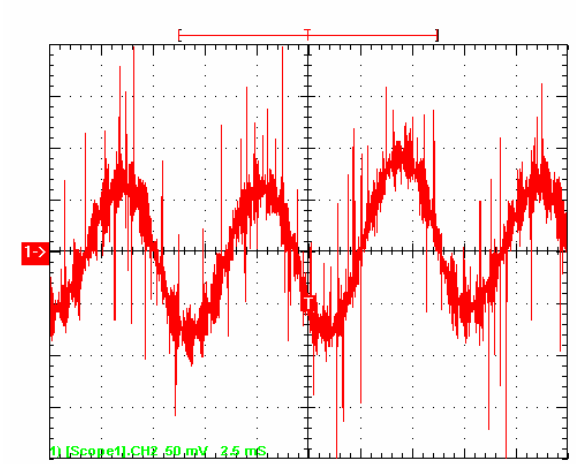



(c) PSpice Simulation (analogue controller).

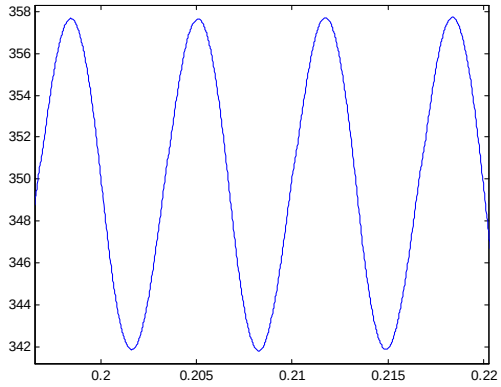
**Figure 6.3.2.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 300W.

Figure 6.3.2 shows the output capacitor bank neutral voltage for an output power level of 300W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of 11.192$V_{p\text{-}p}$ (predicted using equation (4.20)), for an output power level of 300W.

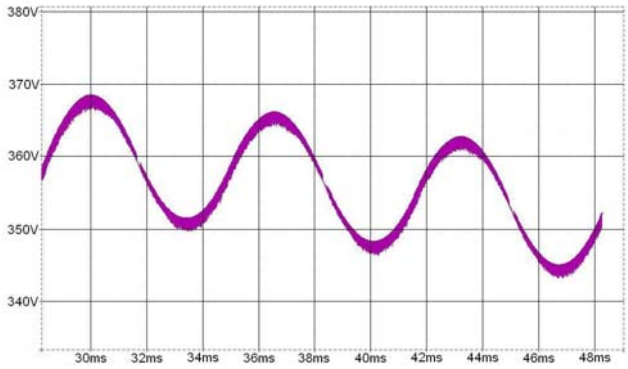
### 6.3.3 400W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 2.5ms/div. Average mid-point voltage of 348V.




(b) MATLAB Simulation (digital controller).

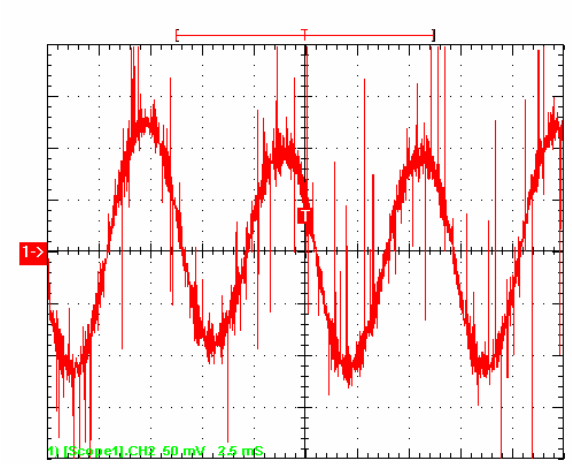



(c) PSpice Simulation (analogue controller).

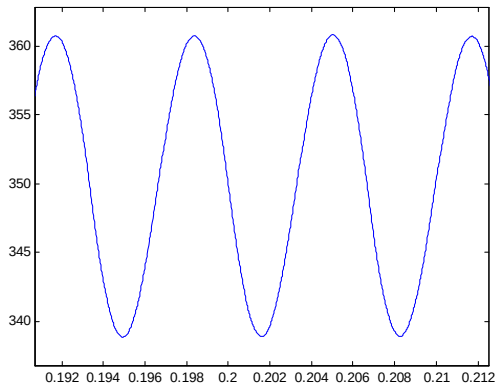
**Figure 6.3.3.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 400W.

Figure 6.3.3 shows the output capacitor bank neutral voltage for an output power level of 400W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of $14.914V_{p\text{-}p}$ (predicted using equation (4.20)), for an output power level of 400W.

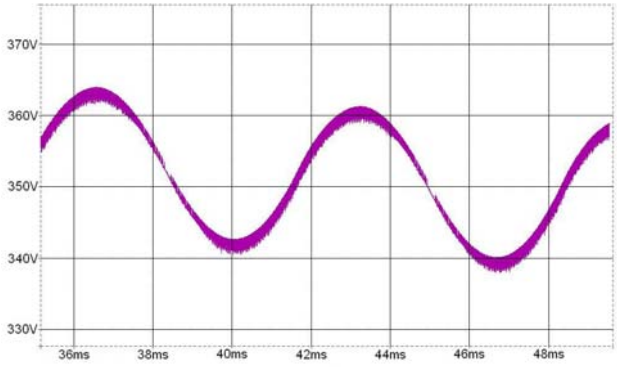
### 6.3.4 550W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 2.5ms/div. Average mid-point voltage of 349V.




(b) MATLAB Simulation (digital controller).

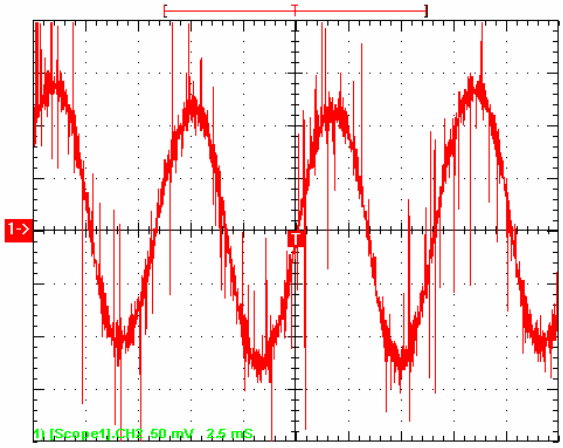



(c) PSpice Simulation (analogue controller).

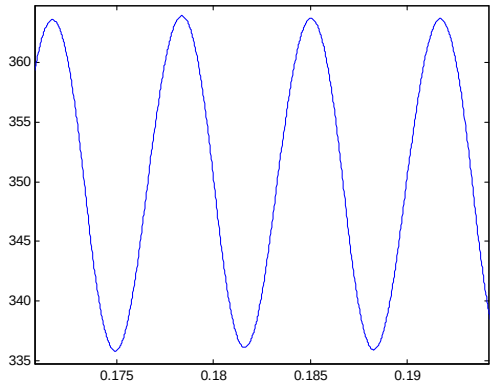
**Figure 6.3.4.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 550W.

Figure 6.3.4 shows the output capacitor bank neutral voltage for an output power level of 550W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of $20.525V_{p\text{-}p}$ (predicted using equation (4.20)), for an output power level of 550W.

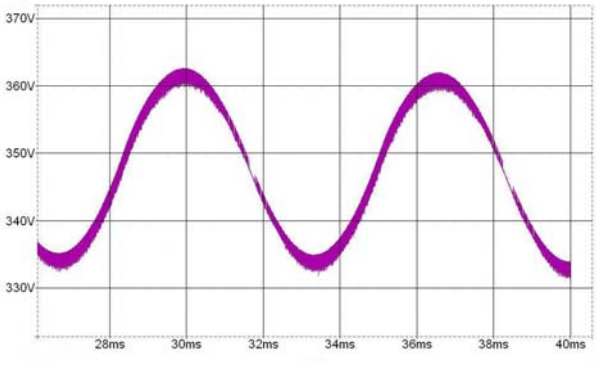
### 6.3.5 700W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 2.5ms/div. Average mid-point voltage of 347V.




(b) MATLAB Simulation (digital controller).

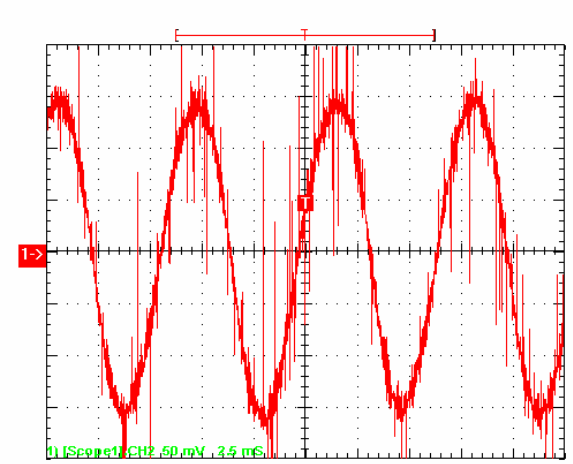



(c) PSpice Simulation (analogue controller).

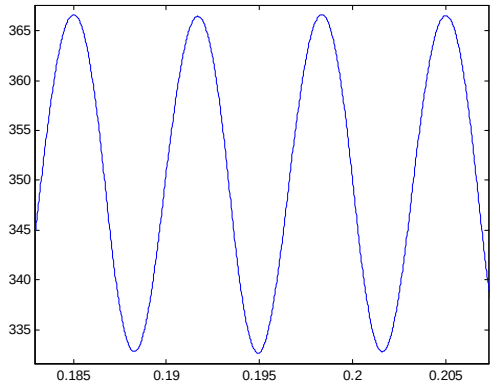
**Figure 6.3.5.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 700W.

Figure 6.3.5 shows the output capacitor bank neutral voltage for an output power level of 700W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of $26.105V_{p\text{-}p}$ (predicted using equation (4.20)), for an output power level of 700W.

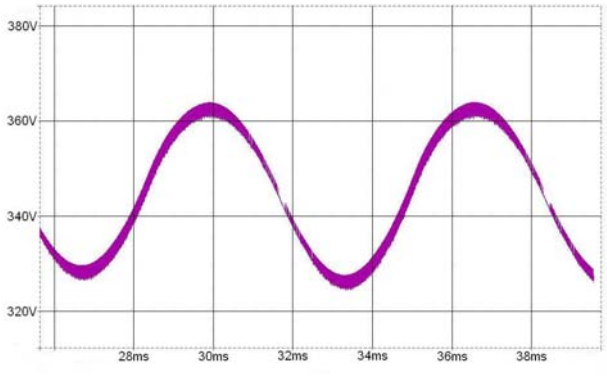
### 6.3.6 850W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 2.5ms/div. Average - point voltage of 348V.




(b) MATLAB Simulation (digital controller).

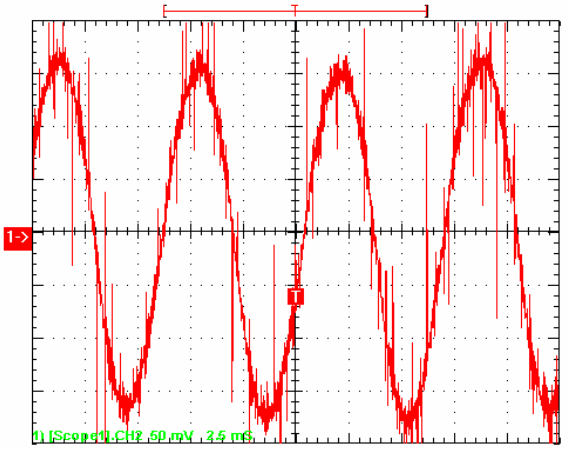



(c) PSpice Simulation (analogue controller).

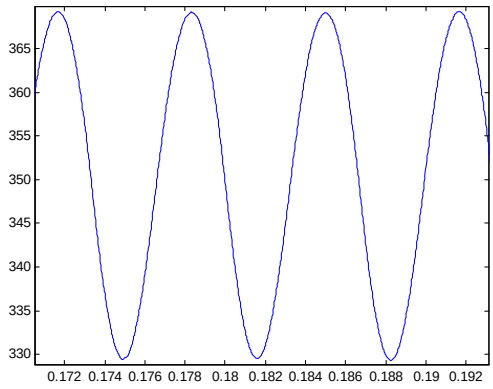
**Figure 6.3.6.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 850W.

Figure 6.3.6 shows the output capacitor bank neutral voltage for an output power level of 850W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of $31.737V_{p\text{-}p}$ (predicted using equation (4.20)), for an output power level of 850W.

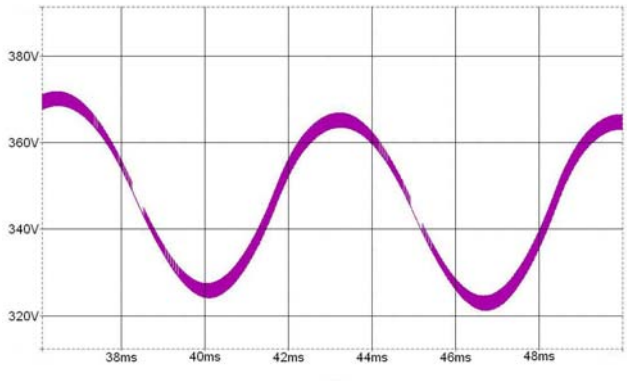
### 6.3.7 1000W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 2.5ms/div. Average mid-point voltage of 348V.




(b) MATLAB Simulation (digital controller).

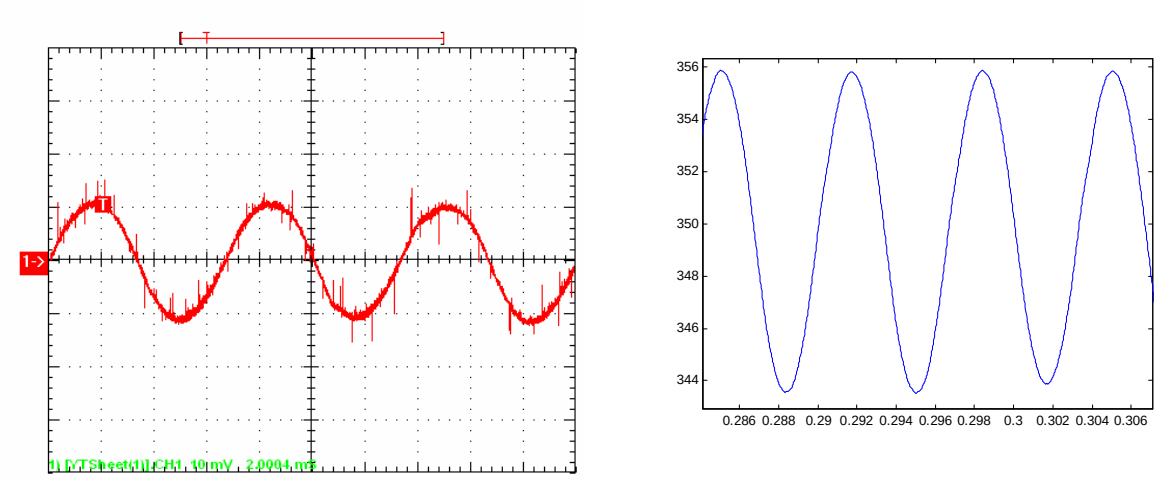



(c) PSpice Simulation (analogue controller).

**Figure 6.3.7.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 1000W.

Figure 6.3.7 shows the output capacitor bank neutral voltage for an output power level of 1000W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of 37.266$V_{p\text{-}p}$ (predicted using equation (4.20)), for an output power level of 1000W.

### 6.3.8 300W Output Power, $V_{LL}$ = 110V input voltage




(a) Experimental prototype. Amplitude scale 5V/div and time scale 2ms/div. Average mid-point voltage of 344V.

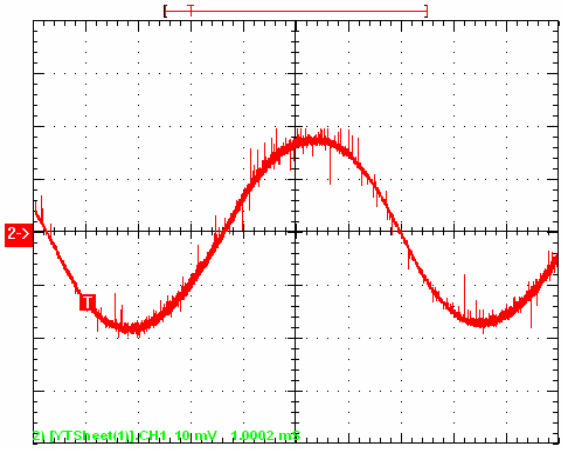
(b) MATLAB Simulation (digital controller).

(c) PSpice Simulation (analogue controller).

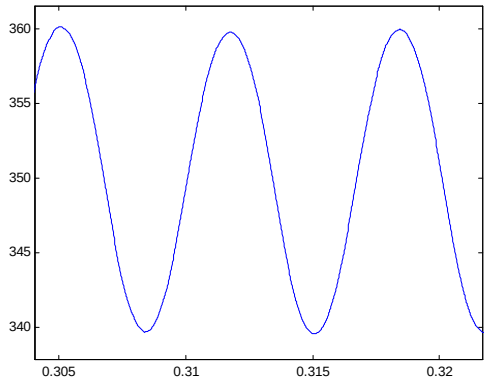
**Figure 6.3.8.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 110V and output load of 300W.

Figure 6.3.8 shows the output capacitor bank neutral voltage for an output power level of 300W and input voltage of 110V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of 11.192$V_{p\text{-}p}$ (predicted using equation 3.20), for an output power level of 300W. When compared to the results for 176V, it is observed that the voltage ripple is the same, which concludes that the mid-point voltage is dependant only on the output power and not dependant in any way on the input voltage.

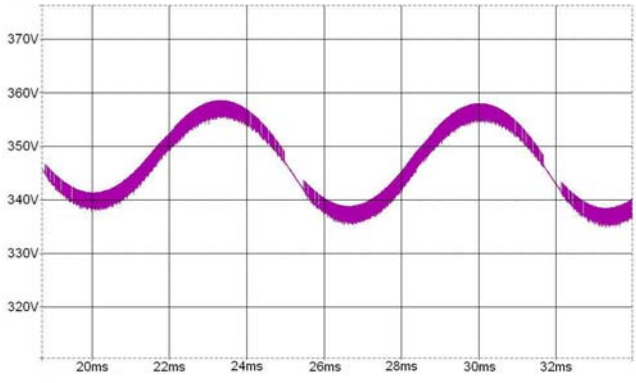
### 6.3.9 500W Output Power, $V_{LL}$ = 110V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 1ms/div. Average mid-point voltage of 344V.




(b) MATLAB Simulation (digital controller).

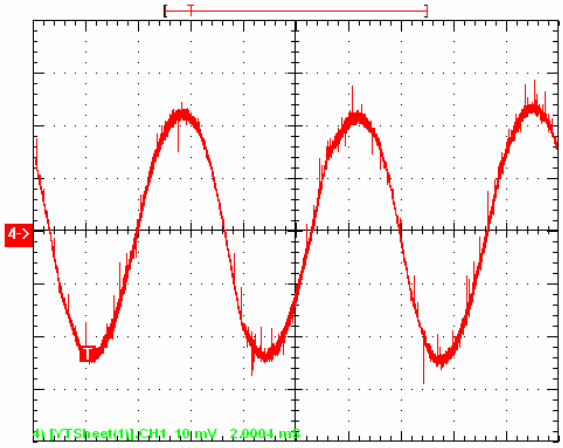



(c) PSpice Simulation (analogue controller).

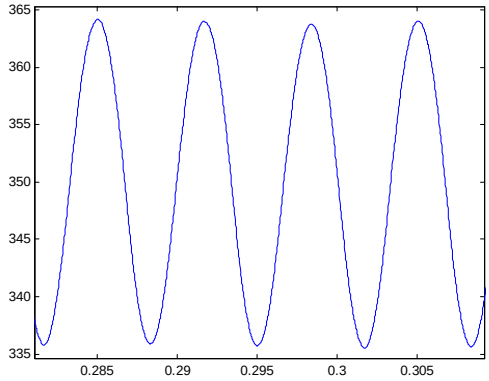
**Figure 6.3.9.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 110V and output load of 500W.

Figure 6.3.9 shows the output capacitor bank neutral voltage for an output power level of 500W and input voltage of 110V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of 18.203$V_{p\text{-}p}$ (predicted using equation 3.20), for an output power level of 500W.

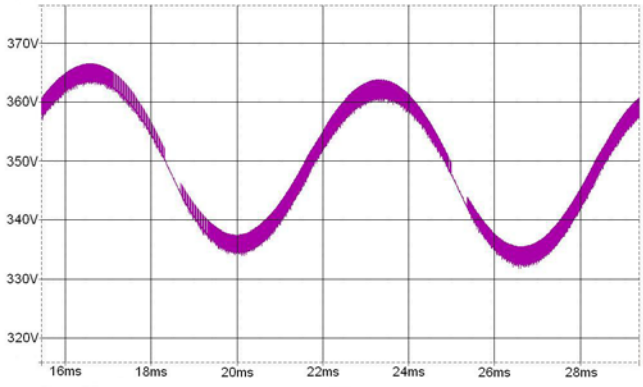
### 6.3.10 700W Output Power, $V_{LL}$ = 154V input voltage



(a) Experimental prototype. Amplitude scale 5V/div and time scale 2ms/div. Average mid-point voltage of 344V.




(b) MATLAB Simulation (digital controller).



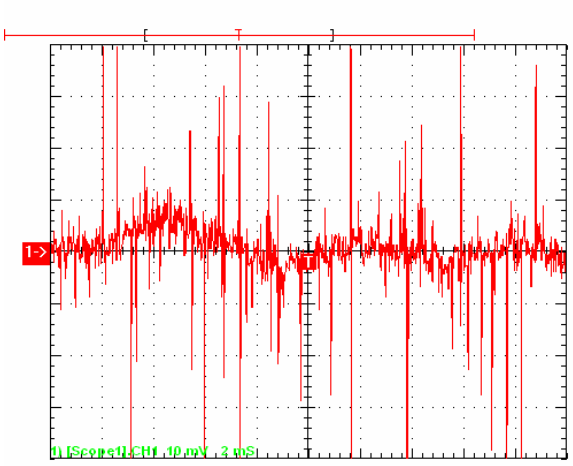

(c) PSpice Simulation (analogue controller).

**Figure 6.3.10.** Mid-point capacitor bank voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 154V and output load of 700W.

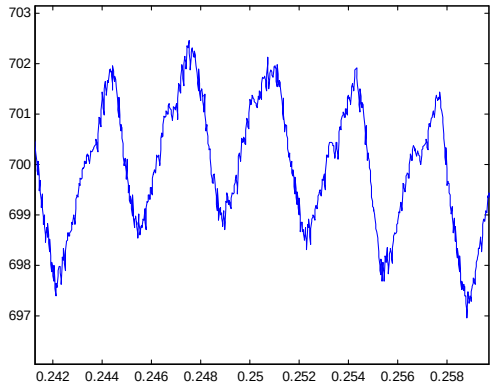
Figure 6.3.10 shows the output capacitor bank neutral voltage for an output power level of 700W and input voltage of 154V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms as well as to the predicted voltage ripple of 26.105$V_{p\text{-}p}$ (predicted using equation 3.20), for an output power level of 700W.

## 6.4 OUTPUT VOLTAGE RIPPLE

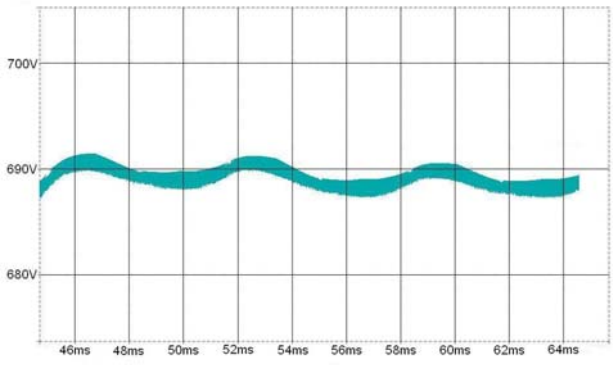
### 6.4.1 200W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 1V/div and time scale 2ms/div. Average output voltage of 704V.




(b) MATLAB Simulation (digital controller).

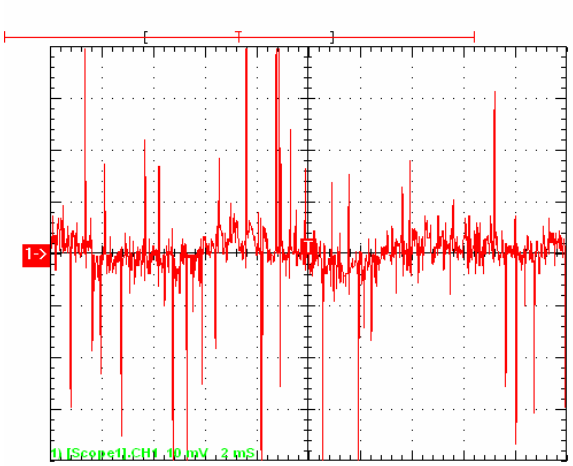



(c) PSpice Simulation (analogue controller).

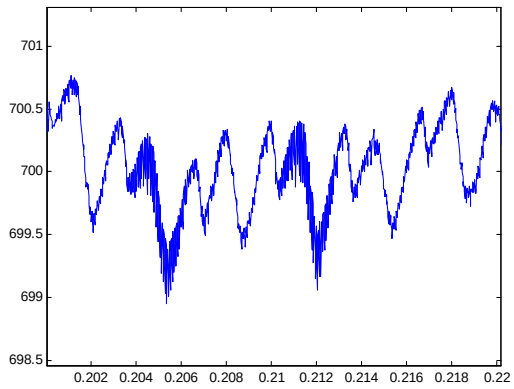
**Figure 6.4.1.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 200W.

Figure 6.4.1 shows the output voltage ripple for an output power level of 200W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The high frequency noise that can be seen in figure 6.4.1(a) is due to radiated EMI noise that is picked up by the measurement probe. The ripple frequency for the experimental prototype and PSpice simulation is 150Hz, whereas the MATLAB simulation indicates a ripple frequency of 300Hz. From [40] it is known that the output voltage ripple frequency shall be at six times the line frequency. It is however observed in figure 6.4.1(a) and figure 6.4.1(b) that the $6^{th}$ harmonic component is suppressed at low power operation.

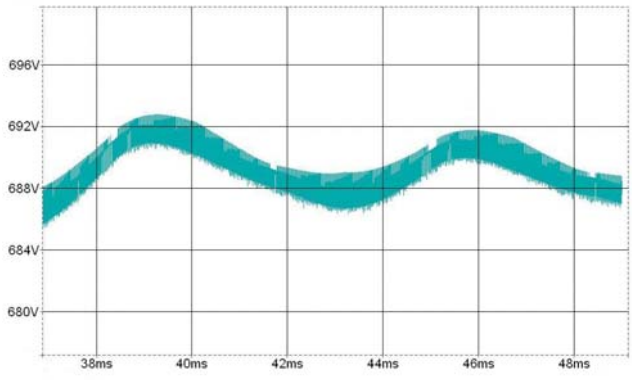
### 6.4.2 300W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 1V/div and time scale 2ms/div. Average output voltage of 704V.




(b) MATLAB Simulation (digital controller).

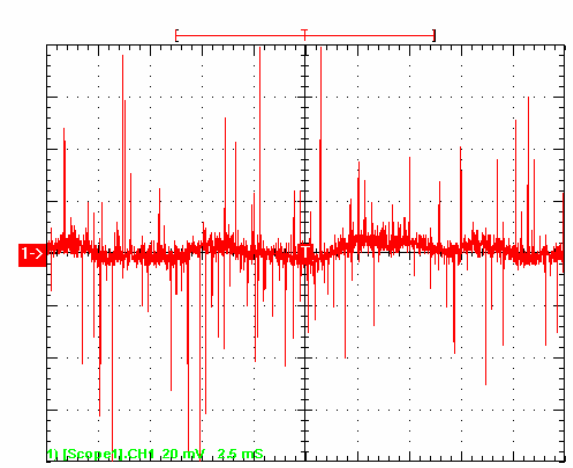



(c) PSpice Simulation (analogue controller).

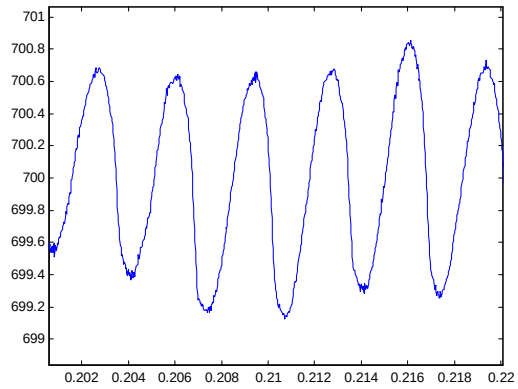
**Figure 6.4.2.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 300W.

Figure 6.4.2 shows the output voltage ripple for an output power level of 300W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The ripple frequency for the experimental prototype and PSpice simulation is 150Hz. The MATLAB simulation indicates a ripple frequency of 300Hz.

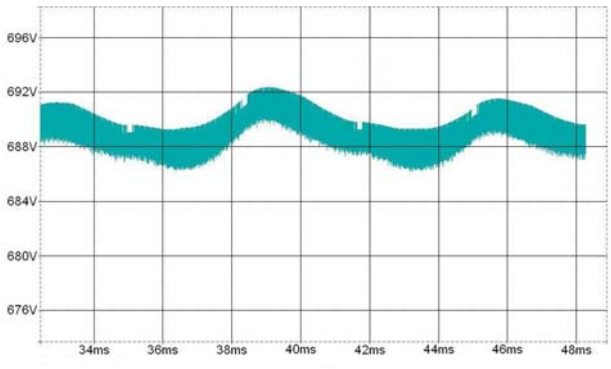
### 6.4.3 400W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 1V/div and time scale 2.5ms/div. Average output voltage of 704V.




(b) MATLAB Simulation (digital controller).

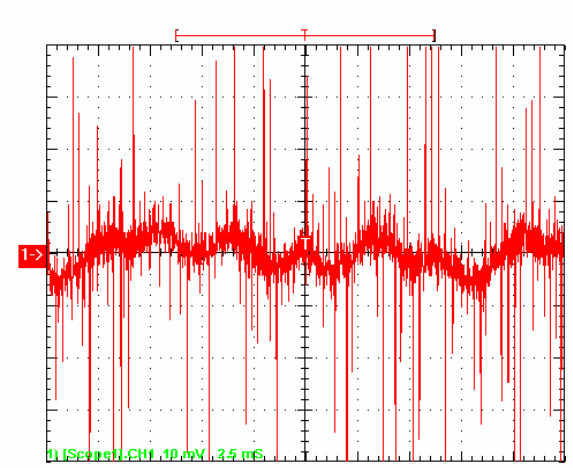



(c) PSpice Simulation (analogue controller).

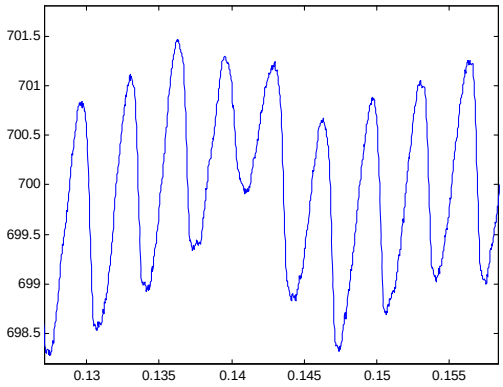
**Figure 6.4.3.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 400W.

Figure 6.4.3 shows the output voltage ripple for an output power level of 400W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The ripple frequency for the experimental prototype and PSpice simulation is 150Hz. The MATLAB simulation indicates a ripple frequency of 300Hz.

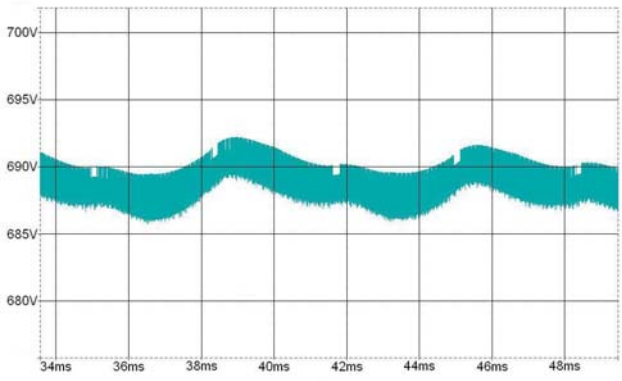
### 6.4.4 550W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 1V/div and time scale 2.5ms/div. Average output voltage of 704V.




(b) MATLAB Simulation (digital controller).

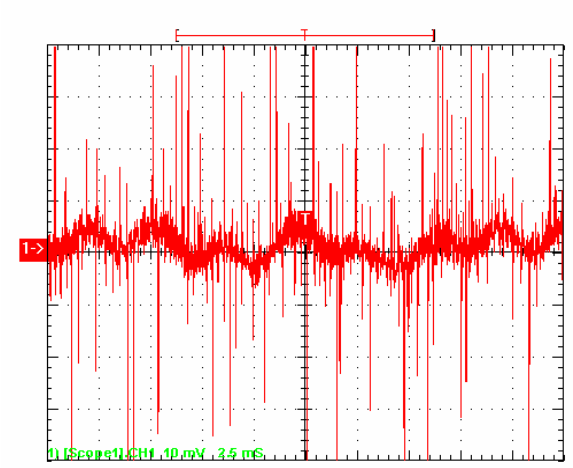



(c) PSpice Simulation (analogue controller).

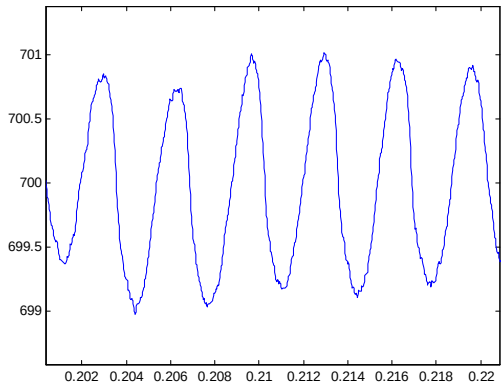
**Figure 6.4.4.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 550W.

Figure 6.4.4 shows the output voltage ripple for an output power level of 550W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The ripple frequency for the experimental prototype and PSpice simulation is 150Hz. The MATLAB simulation indicates a ripple frequency of 300Hz. The $6^{th}$ harmonic is however emerging in the experimental prototype and the PSpice simulation waveforms.

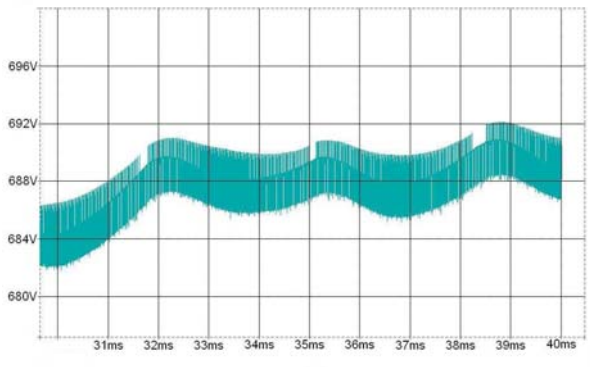
### 6.4.5 700W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 1V/div and time scale 2.5ms/div. Average output voltage of 704V.




(b) MATLAB Simulation (digital controller).

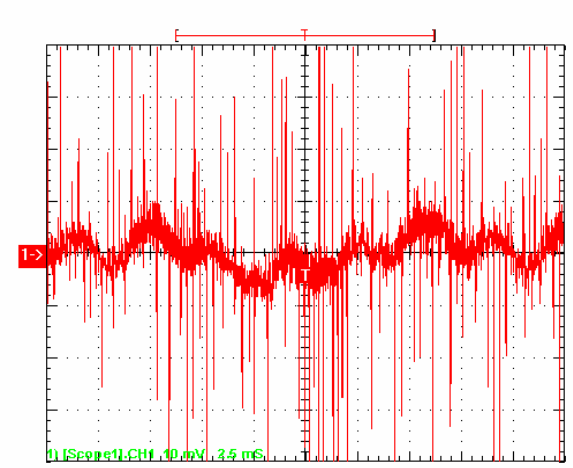



(c) PSpice Simulation (analogue controller).

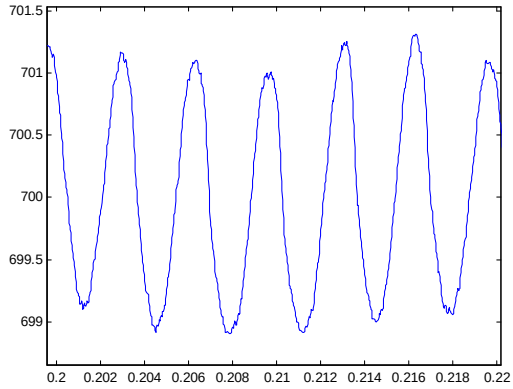
**Figure 6.4.5.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 700W.

Figure 6.4.5 shows the output voltage ripple for an output power level of 700W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The ripple frequency for the experimental prototype, PSpice simulation and MATLAB simulation is 300Hz, or six times the line frequency.

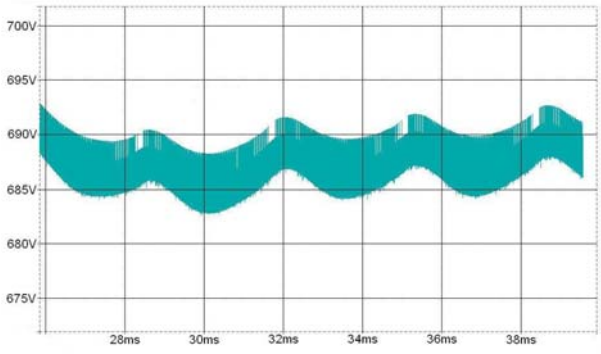
### 6.4.6 850W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 1V/div and time scale 2.5ms/div. Average output voltage of 704V.




(b) MATLAB Simulation (digital controller).

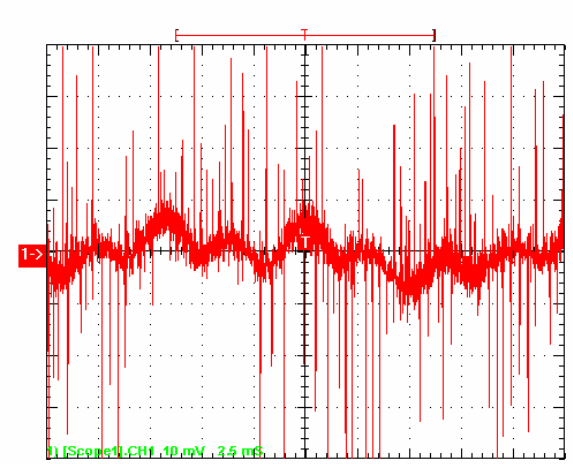



(c) PSpice Simulation (analogue controller).

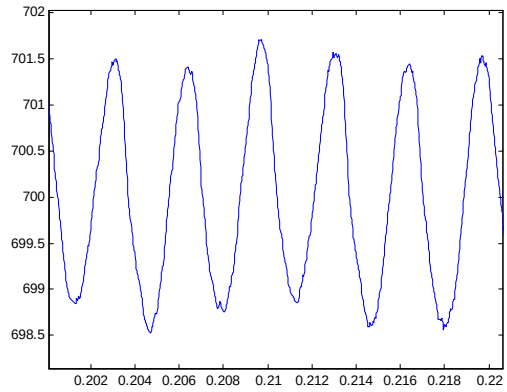
**Figure 6.4.6.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 850W.

Figure 6.4.6 shows the output voltage ripple for an output power level of 850W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The ripple frequency for the experimental prototype, PSpice simulation and MATLAB simulation is 300Hz.

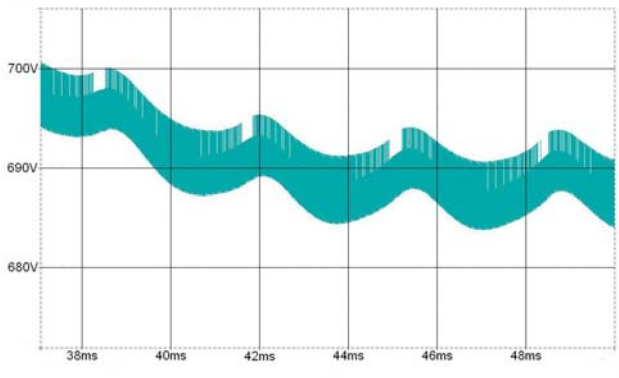
### 6.4.7 1000W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale 1V/div and time scale 2.5ms/div. Average output voltage of 704V.




(b) MATLAB Simulation (digital controller).

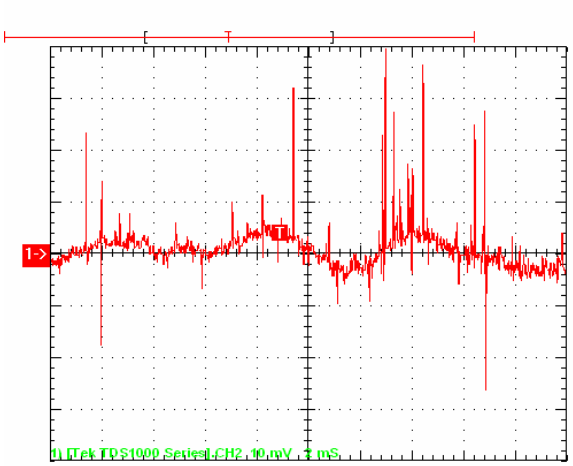



(c) PSpice Simulation (analogue controller).

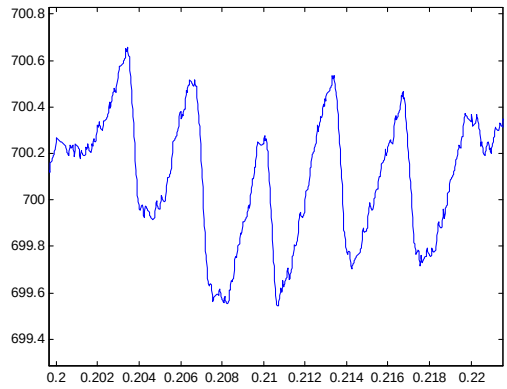
**Figure 6.4.7.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 176V and output load of 1000W.

Figure 6.4.7 shows the output voltage ripple for an output power level of 1000W and input voltage of 176V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The ripple frequency for the experimental prototype, PSpice simulation and MATLAB simulation is 300Hz.

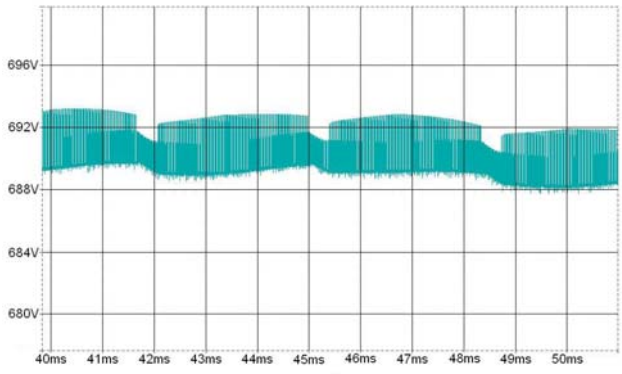
### 6.4.8 300W Output Power, $V_{LL}$ = 110V input voltage



(a) Experimental prototype. Amplitude scale 0.5V/div and time scale 2ms/div. Average output voltage of 692V.




(b) MATLAB Simulation (digital controller).

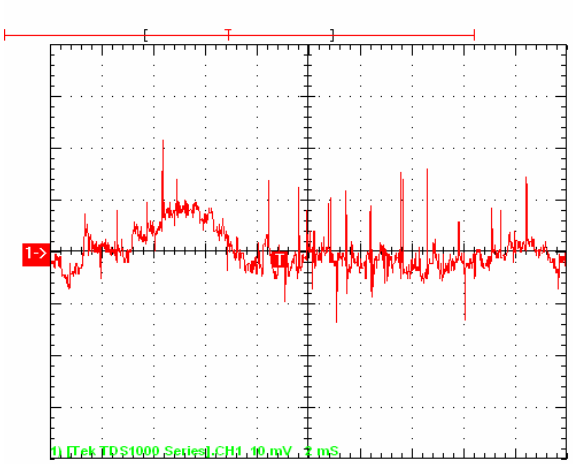



(c) PSpice Simulation (analogue controller).

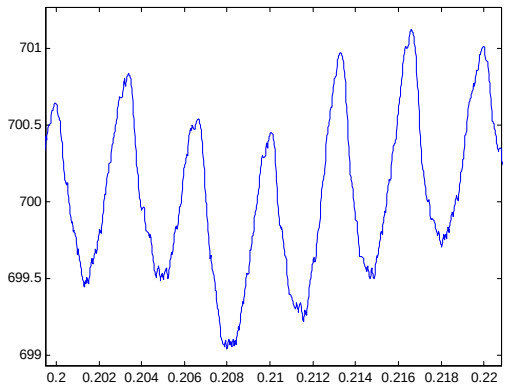
**Figure 6.4.8.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 110V and output load of 300W.

Figure 6.4.8 shows the output voltage ripple for an output power level of 300W and input voltage of 110V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The experimental result indicates that the design is able to supply the required power at this input voltage. This is confirmed by both the PSpice simulation and MATLAB simulation.

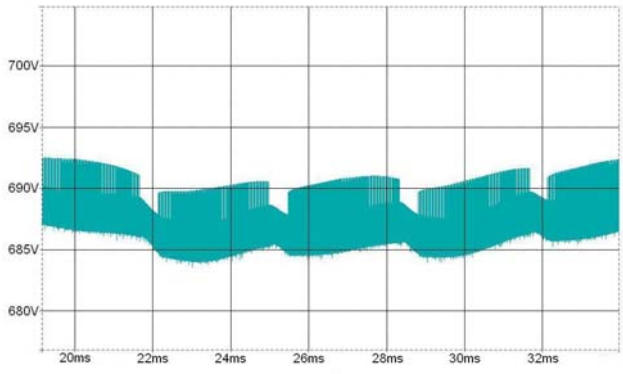
### 6.4.9 500W Output Power, $V_{LL}$ = 110V input voltage



(a) Experimental prototype. Amplitude scale 1V/div and time scale 5ms/div. Average output voltage of 692V.




(b) MATLAB Simulation (digital controller).

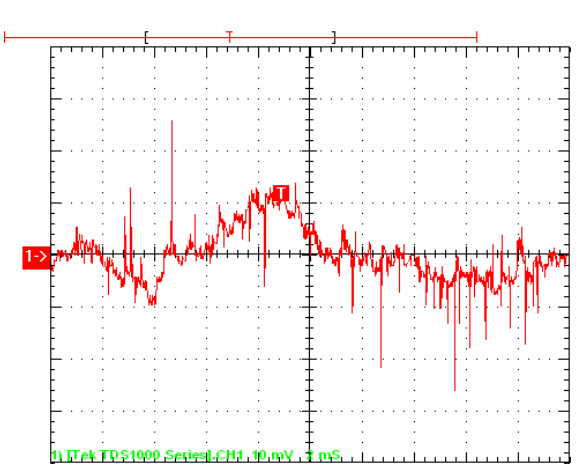



(c) PSpice Simulation (analogue controller).

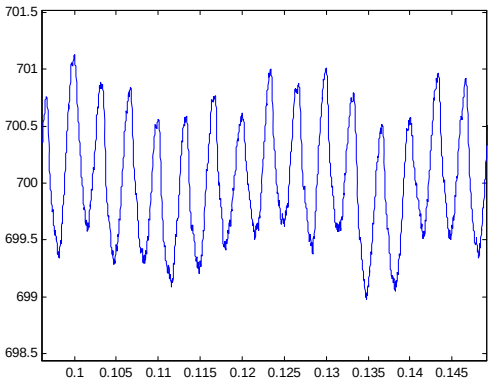
**Figure 6.4.9.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 110V and output load of 500W.

Figure 6.4.9 shows the output voltage ripple for an output power level of 500W and input voltage of 110V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms. The experimental result indicates that the design is able to supply the required (derated) power at this input voltage. This is confirmed by both the PSpice simulation and MATLAB simulation.

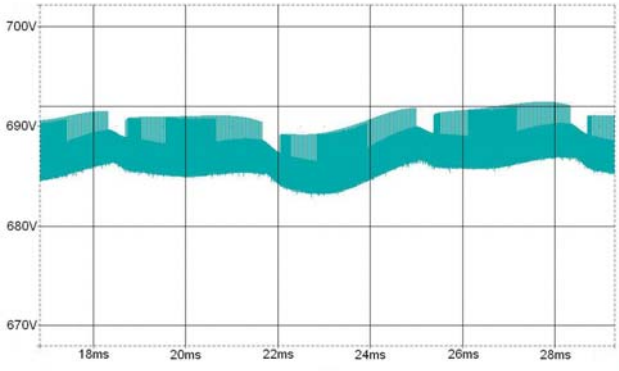
### 6.4.10 700W Output Power, $V_{LL}$ = 154V input voltage



(a) Experimental prototype. Amplitude scale 2V/div and time scale 5ms/div. Average output voltage of 692V.




(b) MATLAB Simulation (digital controller).



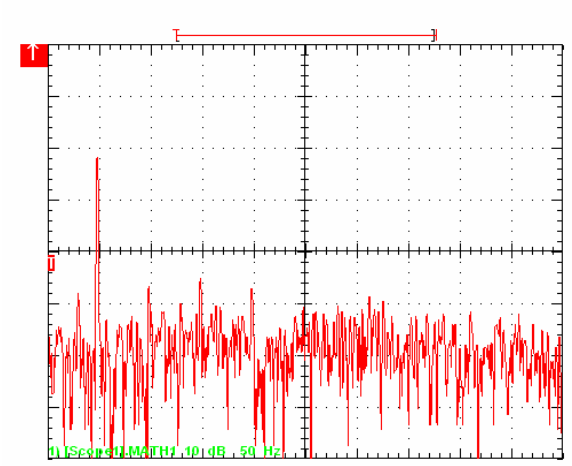

(c) PSpice Simulation (analogue controller).

**Figure 6.4.10.** Output voltage waveforms for the (a) Experimental prototype, (b) MATLAB simulation and (c) PSpice simulation, for an input voltage of 154V and output load of 700W.

Figure 6.4.10 shows the output voltage ripple for an output power level of 700W and input voltage of 154V. The voltage ripple measured for the prototype corresponds well to the simulated waveforms.

## 6.5 INPUT CURRENT HARMONIC SPECTRUM

### 6.5.1 200W Output Power, $V_{LL}$ = 176V input voltage



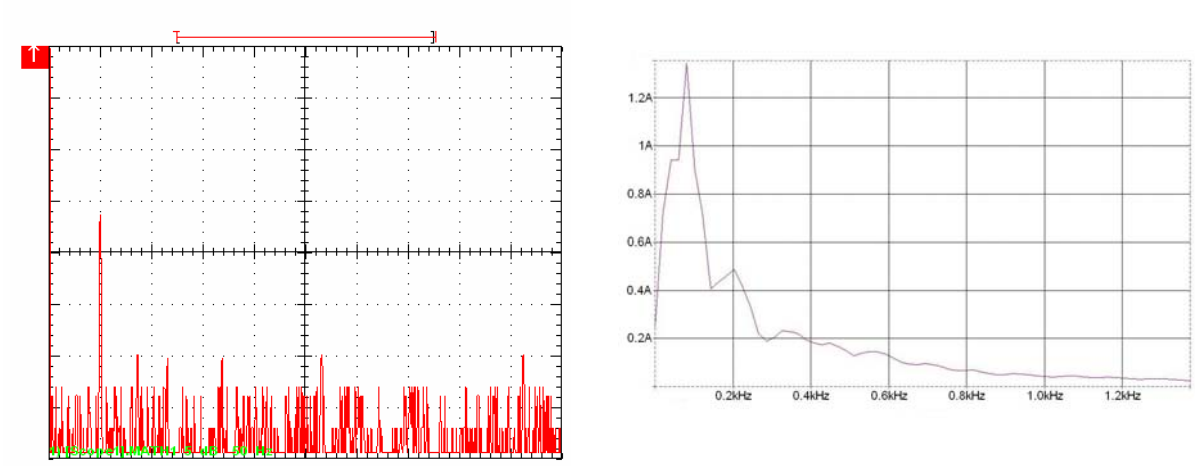
(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from –101dB to –21dB. Frequency range is from 0Hz to 500Hz.


(b) PSpice Simulation.

**Figure 6.5.1.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 176V and output load of 200W.

Figure 6.5.1 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $100A/10^{(dB/20)}$. Thus, for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $100\times10^{((-101dB+58dB)/20)}$ = 0.708A. From [41] it is known that, for the ideal three-phase rectifier, only nontriplen odd harmonics are present in the phase currents (in other words harmonics 5, 7, 11, 13, 17, 19 will be present), therefore it is to be expected that harmonics 5 and 7 will be the dominant harmonics. It can, however, be seen from both figure 6.5.1(a) and figure 6.5.1(b) that even harmonic 7 is already below the noise threshold, thus yielding low harmonic distortion even at this low power level. For the prototype the harmonic distortion was measured at 12.3%. An important observation from figure 6.5.1(a) is the presence of harmonics 2, 3 and 4, which is not expected in a three-phase rectifier. These harmonics are present mainly due to the dual-boost operation of the VIENNA rectifier, where the control is rotated ever 60°. This causes low frequency current distortion (at every transition), as can be seen in figure 6.2.1 to figure 6.2.10 in section 6.2.

### 6.5.2 300W Output Power, $V_{LL}$ = 176V input voltage



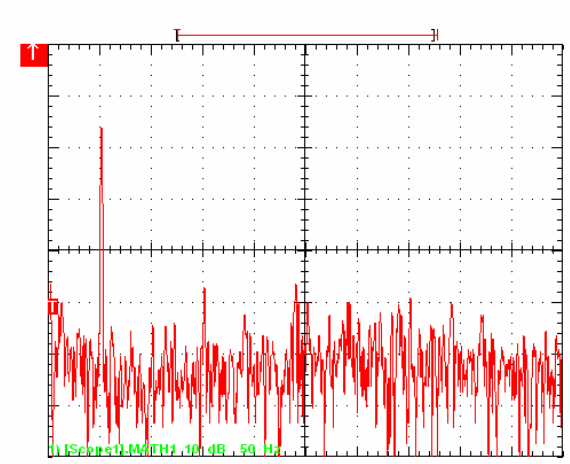

(a) Experimental prototype. Amplitude scale is 5dB/div and the frequency scale 50Hz/div. The amplitude range is from –78.6dB to –38.6dB. Frequency range is from 0Hz to 500Hz.

(b) PSpice Simulation.

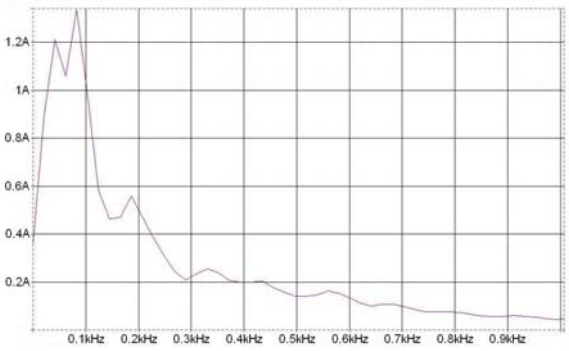
**Figure 6.5.2.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 176V and output load of 300W.

Figure 6.5.2 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $500A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $500\times10^{((-78.6dB+23dB)/20)}$ = 0.830A. It is again evident, from both figure 6.5.2(a) and figure 6.5.2(b), that harmonic 7 is already below the noise threshold, thus yielding low harmonic distortion at this low power level. For the prototype the harmonic distortion was measured to be below 6.63%. Harmonics 2, 3 and 4 are again observed at this power level, in figure 6.5.2.

### 6.5.3 400W Output Power, $V_{LL}$ = 176V input voltage



(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from –101.8dB to –21.8dB. Frequency range is from 0Hz to 500Hz.

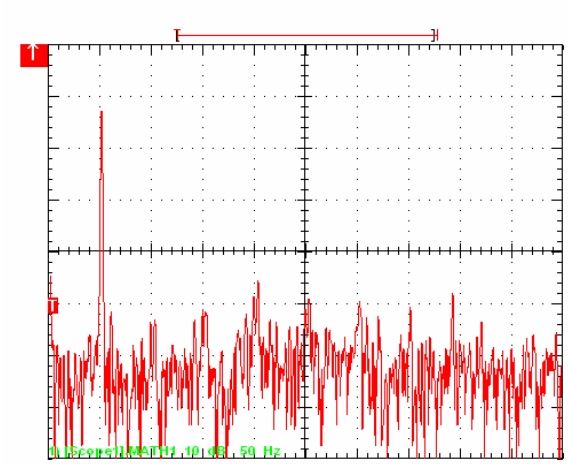



(b) PSpice Simulation.

**Figure 6.5.3.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 176V and output load of 400W.

Figure 6.5.3 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $100A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $100\times10^{((-101.8dB+64dB)/20)} = 1.288A$. It is observed in figure 6.5.3(a) that harmonic 7 is on the noise threshold. For the prototype the harmonic distortion was measured at 3.98%. Harmonics 2, 3 and 4 are again observed at this power level, but harmonic 5 is the most dominant sub-harmonic.

### 6.5.4 550W Output Power, $V_{LL}$ = 176V input voltage



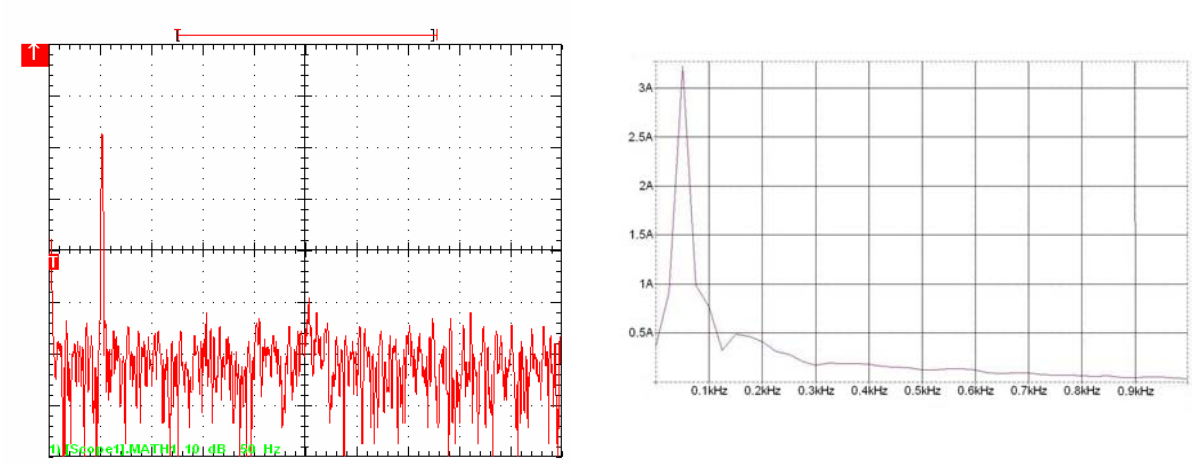
(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from –101.8dB to –21.8dB. Frequency range is from 0Hz to 500Hz.


(b) PSpice Simulation.

**Figure 6.5.4.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 176V and output load of 550W.

Figure 6.5.4 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $100A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $100\times10^{((-101.8dB+67dB)/20)} = 1.820A$. It is observed in figure 6.5.4(a) that harmonic 7 is on the noise threshold. For the prototype the harmonic distortion was measured at 3.67%. Harmonics 2, 3 and 4 are again observed at this power level with harmonics 5 and 7 dominant, but not the most dominant sub-harmonics.

### 6.5.5 700W Output Power, $V_{LL}$ = 176V input voltage



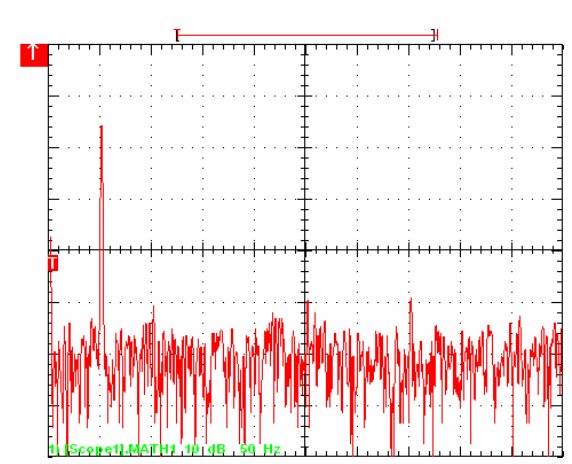

(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from –101.8dB to –21.8dB. Frequency range is from 0Hz to 500Hz.

(b) PSpice Simulation.

**Figure 6.5.5.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 176V and output load of 700W.

Figure 6.5.5 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $200A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $200\times10^{((-101.8dB+63dB)/20)} = 2.296A$. It is observed in figure 6.5.5(a) that harmonic 7 is below the noise threshold, thus all further harmonics will be below the noise threshold and will not yield a valid measurement for that particular harmonic. For the prototype the harmonic distortion was measured at 4.82%. Harmonics 3 and 4 are again observed at this power level but are almost on the noise level. For this power level harmonic 5 is the most dominant, as is to be expected with three-phase rectifiers.

### 6.5.6 850W Output Power, $V_{LL}$ = 176V input voltage



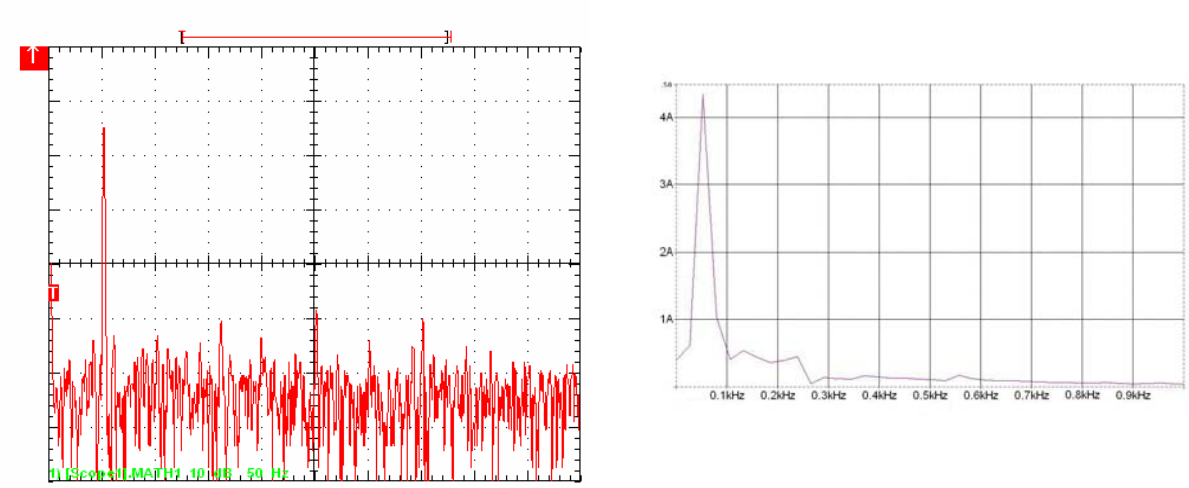
(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from –101.8dB to –21.8dB. Frequency range is from 0Hz to 500Hz.


(b) PSpice Simulation.

**Figure 6.5.6.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 176V and output load of 850W.

Figure 6.5.6 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $200A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $200\times10^{((-101.8dB+65dB)/20)}$ = 2.891A. For the prototype the harmonic distortion was measured at 3.75%. Only harmonic 2 is again observed at this power level but its level is low compared to harmonics 5 and 7 that are clearly dominant at this power level.

### 6.5.7 1000W Output Power, $V_{LL}$ = 176V input voltage



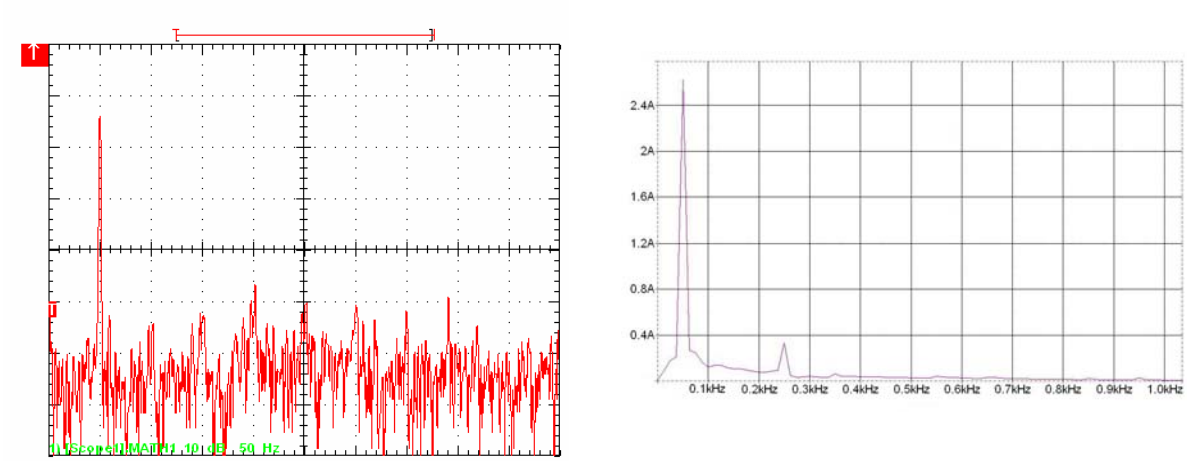

(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from –101.8dB to –21.8dB. Frequency range is from 0Hz to 500Hz.

(b) PSpice Simulation.

**Figure 6.5.7.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 176V and output load of 1000W.

Figure 6.5.7 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $200A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $200\times10^{((-101.8dB+66dB)/20)} = 3.243A$. For the prototype the harmonic distortion was measured at 2.67%. Harmonics 5 and 7 are clearly dominant at this power level.

### 6.5.8 300W Output Power, $V_{LL}$ = 110V input voltage



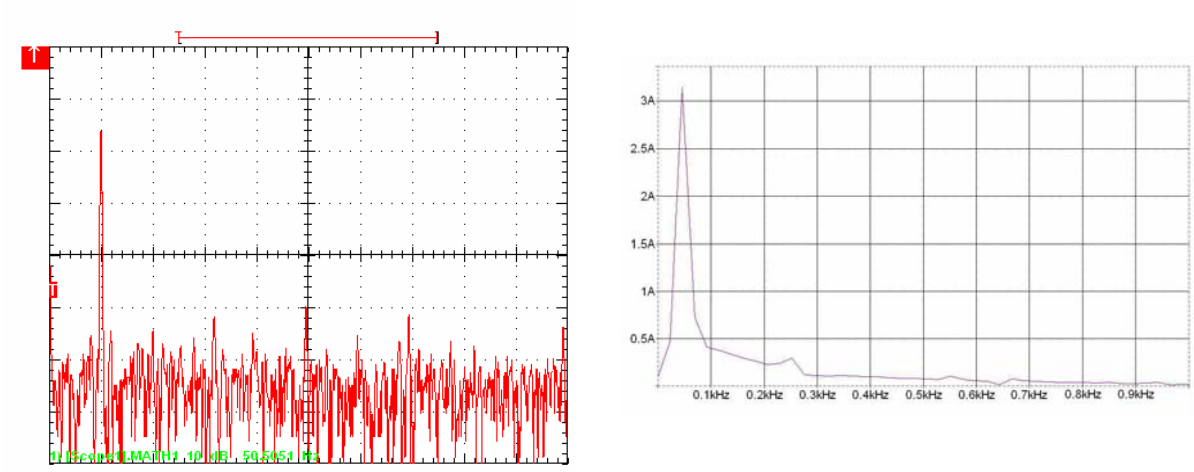

(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from -101.8dB to –21.8dB. Frequency range is from 0Hz to 500Hz.

(b) PSpice Simulation.

**Figure 6.5.8.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 110V and output load of 300W.

Figure 6.5.8 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $100A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $100\times10^{((-101.8dB+66dB)/20)}$ = 1.622A. For the prototype the harmonic distortion was measured at 3.81%. Harmonics 5 and 7 are clearly dominant at this power level. It is worthwhile to note that harmonic 5 and harmonic 7 are clearly observable on the PSpice simulation.

### 6.5.9 500W Output Power, $V_{LL}$ = 110V input voltage



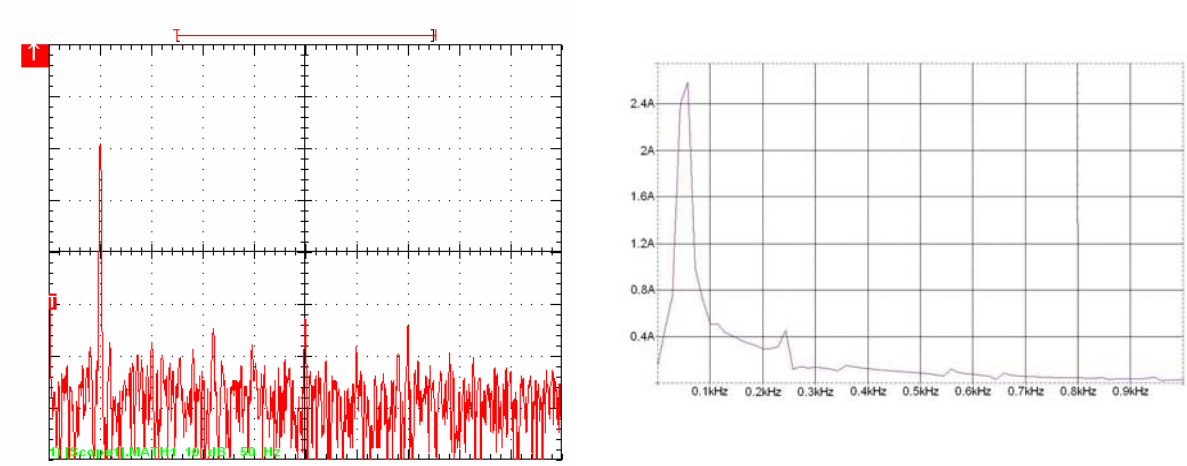

(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from –101.8dB to –21.8dB. Frequency range is from 0Hz to 500Hz.

(b) PSpice Simulation.

**Figure 6.5.9.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 110V and output load of 500W.

Figure 6.5.9 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $200A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $200\times10^{((-101.8dB+63dB)/20)}$ = 2.296A. For the prototype the harmonic distortion was measured at 2.76%. Harmonics 5 and 7 are clearly dominant at this power level. Harmonic 5 is clearly observable on the PSpice simulation.

### 6.5.10 700W Output Power, $V_{LL}$ = 154V input voltage




(a) Experimental prototype. Amplitude scale is 10dB/div and the frequency scale 50Hz/div. The amplitude range is from –99.6dB to–19.6dB. Frequency range is from 0Hz to 500Hz.

(b) PSpice Simulation.

**Figure 6.5.10.** Harmonic spectra for the (a) Experimental prototype and (b) PSpice simulation, for an input voltage of 154V and output load of 700W.

Figure 6.5.10 shows the prototype and simulated harmonic distortion spectra for the input current. The prototype measurement sensitivity is $200A/10^{(dB/20)}$. Thus for the fundamental harmonic (the harmonic at 50Hz), the equivalent harmonic in amperes is equal to $200\times10^{((-99.6dB+61dB)/20)}$ = 2.350A. For the prototype the harmonic distortion was measured at 2.71%. Harmonics 5 and 7 are clearly dominant at this power level. Harmonic 5 is clearly observable on the PSpice simulation.

## 6.6 TOTAL HARMONIC DISTORTION, EFFICIENCY, OVERSHOOT AND RIPPLE COMPARISON FOR A FIXED VOLTAGE INPUT OF 176V

### 6.6.1 Total harmonic distortion

Figure 6.6.1 shows the total harmonic distortion of the input current (THDi) as a function of the output power.

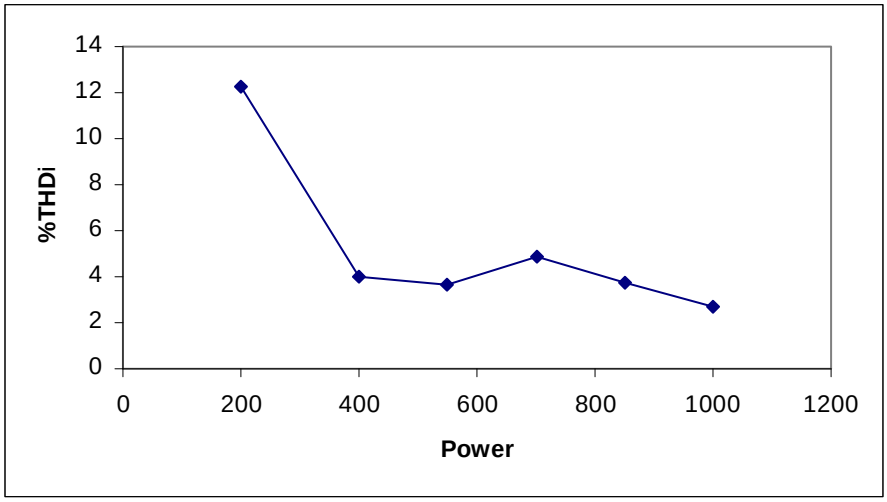



**Figure 6.6.1.** Total Harmonic Distortion versus power.

It is observed in figure 6.6.1 that the total harmonic distortion decreases as the output loading increases. From figure 6.6.1 it is evident that the THD is below the key figure of 10% for power levels above 400W. This implies that the VIENNA rectifier performance is at its best when the input current ripple to rms input current ratio is 0.4 or lower.

### 6.6.2 Efficiency

Shown in figure 6.6.2 is the efficiency of the system as a function of the output power.

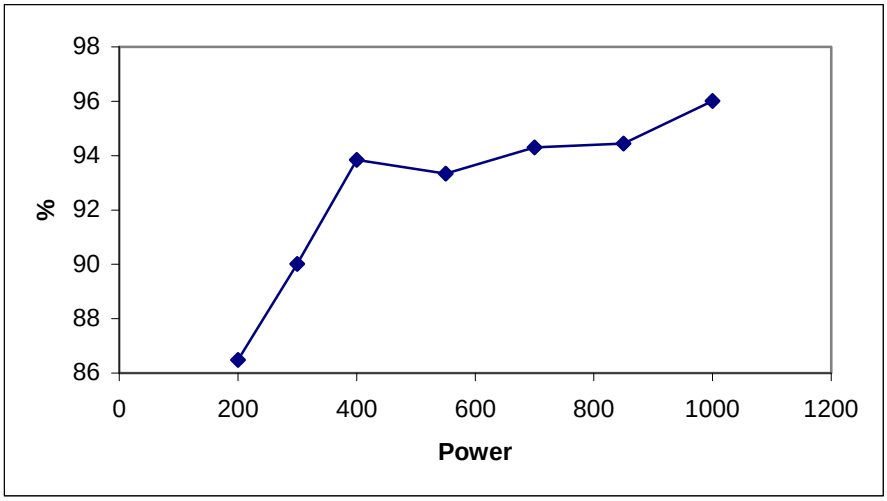



**Figure 6.6.2.** Efficiency versus power.

It is observed in figure 6.6.2 that the efficiency improves as the output loading increases. There is also a sharp increase in efficiency from 400W. Figure 6.6.2 implies that the VIENNA rectifier performs at its best, in terms of efficiency, when the output power to input voltage ratio is 2.27, or greater. The efficiency measured is better than the predicted efficiency ($\eta \leq 91.2\%$) in section 5.4 of Chapter 5. This implies, however not necessarily, that the efficiency of the VIENNA rectifier might be generally better than predicted for other VIENNA rectifier designs, should the same process for be used as outlined in section 5.4.

The efficiency measured for reduced input voltages were: 89% for operation at $V_{LL}$ = 110V, 300W output loading; 94% for operation at $V_{LL}$ = 110V, 500W output loading; and 96% for operation at $V_{LL}$ = 154V, 700W output loading. These results suggest that the VIENNA rectifier is still quite efficient, even for low input voltages and low output loading.

### 6.6.3 Output capacitor filter performance

Listed in table 6.1 is the predicted, simulated and measured performance of the output capacitor filter.

Table 6.1 shows that the predicted and the measured/simulated mid-point voltage ripple is comparable and in agreement. It can thus be concluded that the theoretical analysis

predicting the mid-point voltage ripple, as derived in section 4.2 of Chapter 4, provides an accurate estimate of the voltage ripple, provided that the ratio of the switching frequency to line frequency is high enough (for this design the ratio is 1000).

**Table 6.1.** Output capacitor filter performance

| Power (W) | Predicted (calculated) mid-point capacitor voltage ripple (peak-to-peak) from eq. (4.20) | Measured mid-point voltage ripple (peak-to-peak) | PSpice simulated mid-point voltage ripple (peak-to-peak) | MATLAB simulated mid-point voltage ripple (peak-to-peak) |
|---|---|---|---|---|
| 200 | 7.475 | 8 | 8 | 10.5 |
| 300 | 11.192 | 12 | 12 | 12 |
| 400 | 14.914 | 14 | 15 | 15.5 |
| 550 | 20.525 | 20 | 20 | 21 |
| 700 | 26.105 | 25 | 26 | 27 |
| 850 | 31.737 | 30 | 33 | 33 |
| 1000 | 37.266 | 35 | 40 | 39 |

Observed in table 6.1 is that the capacitor mid-point voltage ripple magnitude increases with increase in load power.

### 6.6.4 Load step transient response

A load step from half load to full load, or *vice versa*, was simulated utilizing PSpice and MATLAB simulations and subsequently measured on the VIENNA prototype.

*I. PSpice load step transient response simulation*

For the PSpice simulation a load step was introduced at 40ms, from a power level of 700W down to 350W, as shown in figure 6.6.4 (for an input voltage of 220V). The resulting current, output voltage and mid-point capacitor voltage waveforms are shown in figures 6.6.3 to 6.6.5

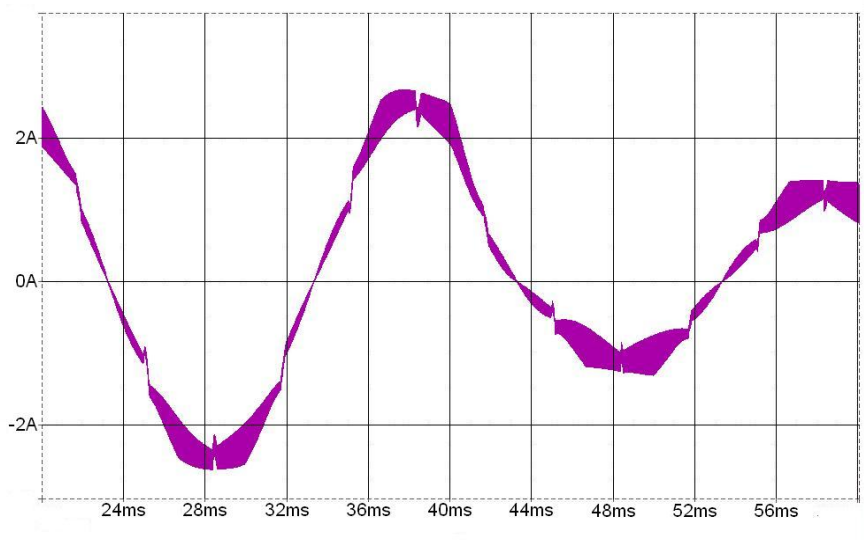



**Figure 6.6.3.** Input current for load step at output at 40ms.

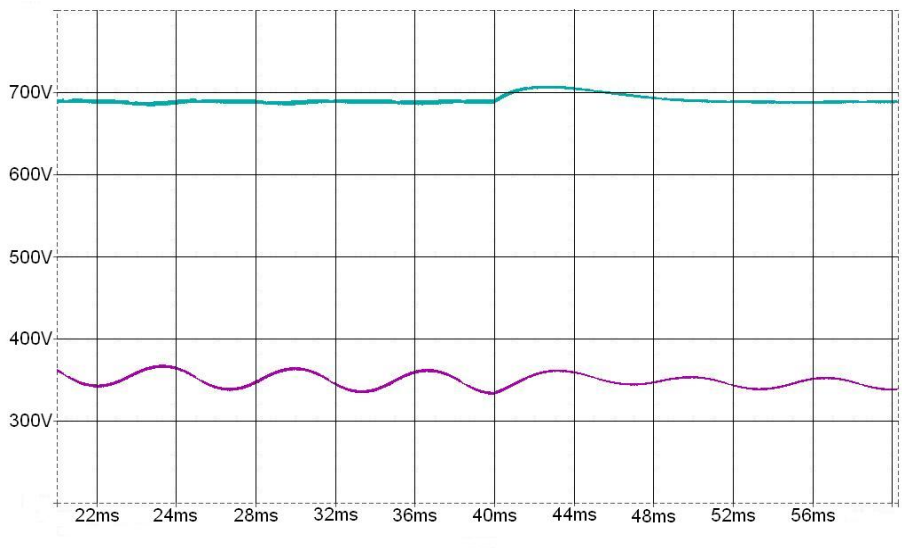



**Figure 6.6.4.** Output voltage (cyan trace) and mid-point voltage (purple trace) waveforms for load step at output at 40ms.

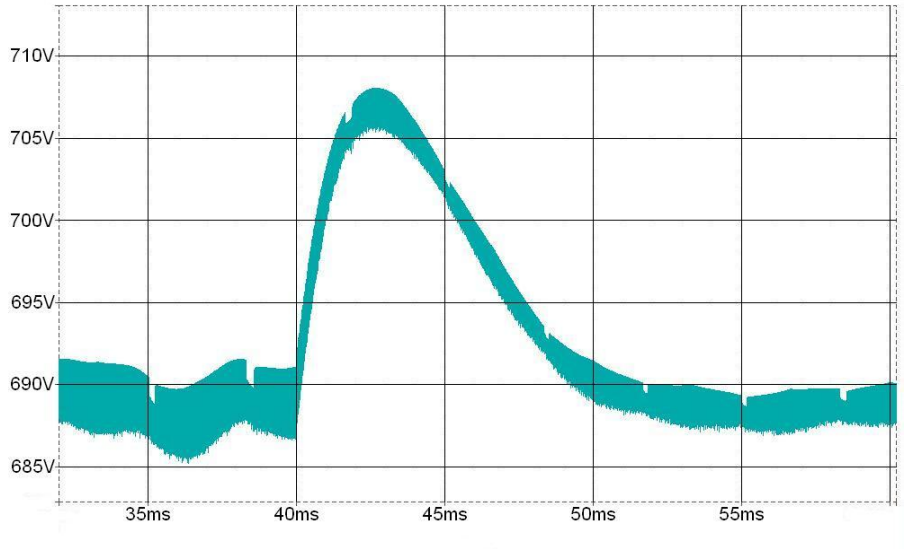



**Figure 6.6.5.** Output voltage waveforms for load step at output at 40ms.

Figure 6.6.4 shows the voltage waveforms for the PSpice simulation. The load step was introduced at 40ms. From figure 6.6.5 it is seen that the output voltage takes approximately 12ms, or half a supply cycle, to settle from the load-step disturbance. This is approximately twice the inverted cross-over frequency, or 2((1/160Hz)) = 12.5ms. Also observed in figure 6.6.4 is the lower mid-point ripple voltage after 40ms, due to the lower output loading. The decrease in input current amplitude after 40ms is also evident in figure 6.6.3. From figure 6.6.5 it can be seen that the overshoot of the output voltage is approximately 20V. From equations (3.105) to (3.107) the open-loop compensated phase margin for the system is calculated to be 67.55°, which compares very well to the 60° designed-for phase margin. This also implies that the model-analysis from Chapter 4 (section 4.3) is accurate in estimating the VIENNA rectifier small-signal frequency response. It also verifies the modelling of the VIENNA rectifier, performed in Chapter 3.

*II. MATLAB load step transient response simulation*

For the MATLAB simulation the output load was stepped down after 20ms, from 700W down to 350W (for an input voltage of 220V). The resulting current, output voltage and mid-point capacitor voltage waveforms are shown in figures 6.6.6 to 6.6.8.

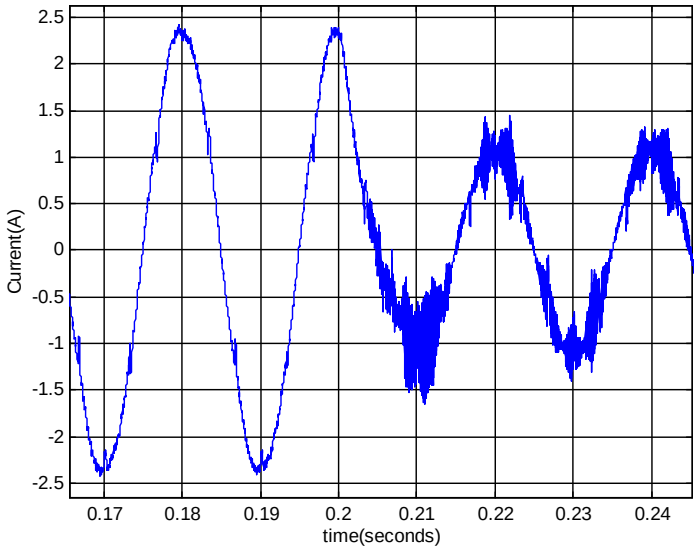



**Figure 6.6.6.** Input current for load step at output at 20ms.

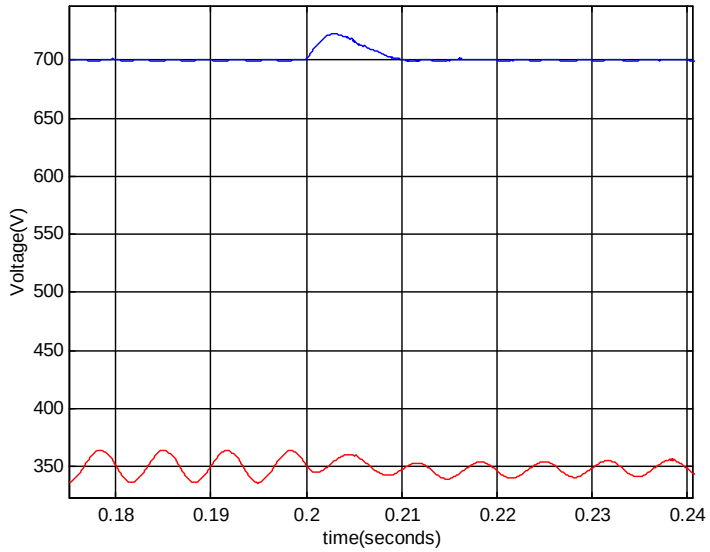



**Figure 6.6.7.** Output voltage (blue trace) and mid-point voltage (red trace) waveforms for load step at output at 20ms.

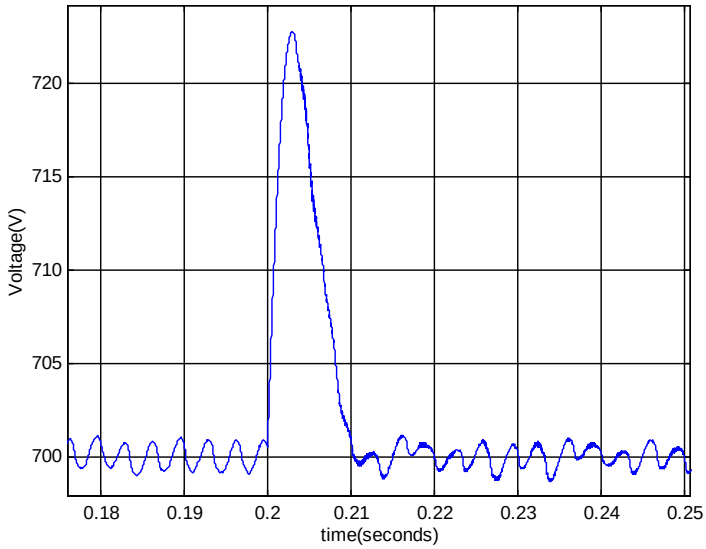



**Figure 6.6.8.** Output voltage waveforms for a load step at output at 20ms.

Figure 6.6.7 shows the voltage waveforms for the MATLAB simulation. The load step was introduced at 20ms. From figure 6.6.8 it is seen that the output voltage takes approximately 12ms (just less than half a supply cycle) to settle from the load-step disturbance. Observed in figure 6.6.7 is the lower mid-point ripple voltage after 20ms due to lower output loading. The decrease in input current amplitude after 20ms is also evident in figure 6.6.6. From figure 6.6.8 it can be seen that the overshoot of the output voltage is approximately 23V. From equations (3.105) to (3.107) the open-loop compensated phase margin for the system can be calculated to be 66.99°, which compares very well to the 60° designed-for phase margin. The phase margin estimates from the PSpice simulation and the MATLAB simulation are similar and agreeable and confirm that the small signal frequency response model, derived in Chapter 4 (section 4.3), is accurate and representative. This also verifies the modelling of the VIENNA rectifier, performed in Chapter 3.

*III. Experimental prototype load step transient response for a 220V input*

An output load step from 700W down to 350W, with an input voltage of 220V, was performed on the prototype. The resulting output voltage waveform is shown in figure 6.6.9. Shown in figure 6.6.10 is the bus voltages and in figure 6.6.11 the resulting input current waveform for the step-response.

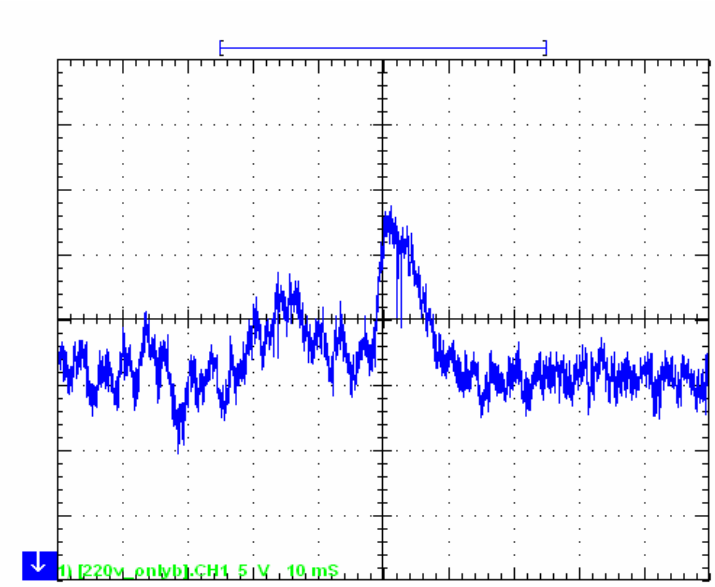



**Figure 6.6.9.** Output voltage for load step at output (amplitude scale 5V/div and time scale 10ms/div). Nominal output voltage is equal to 690V.

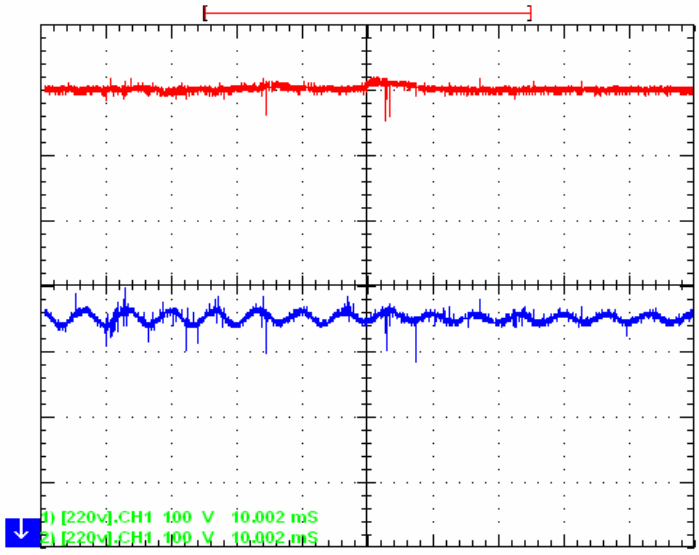



**Figure 6.6.10.** Experimental prototype output voltage (red trace) and mid-point voltage (blue trace) waveforms for load step (scale 100V/div).

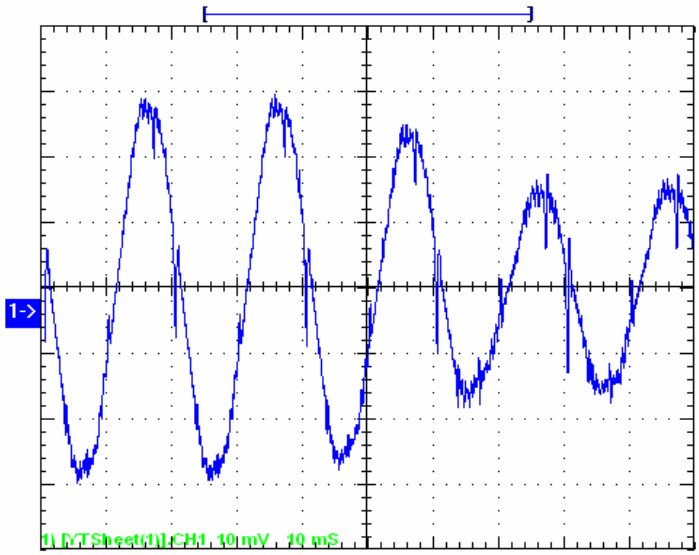



**Figure 6.6.11.** Experimental prototype input current waveform for load step (scale 1A/div).

From figure 6.6.9 it is seen that the output voltage takes approximately 15ms to settle from the load-step disturbance. Observed in figure 6.6.10 is the lower mid-point ripple voltage after the load-step disturbance, due to lower output loading. The decrease in input current amplitude after the load-step disturbance is also evident in figure 6.6.11. From figure 6.6.9 it can be seen that the overshoot of the output voltage is approximately 14V. From equations (3.105) to (3.107) the open-loop compensated phase margin for the system can be calculated to be 68.94°, which compares well to the 60° designed-for phase margin and very well to the simulated load step responses using MATLAB and PSpice. This confirms that the model-analysis from Chapter 4 is accurate in estimating the VIENNA rectifier small-signal frequency response. It again verifies the modelling of the VIENNA rectifier, performed in Chapter 3.

*IV. Experimental prototype load step transient response for a 154V input*

An output load step from 700W down to 350W, with the input voltage at 154V, was performed on the prototype. The resulting output voltage waveform is shown in figure 6.6.12. Shown in figure 6.6.13 is the bus voltages and, in figure 6.6.14, the resulting input current waveform for the step-response.

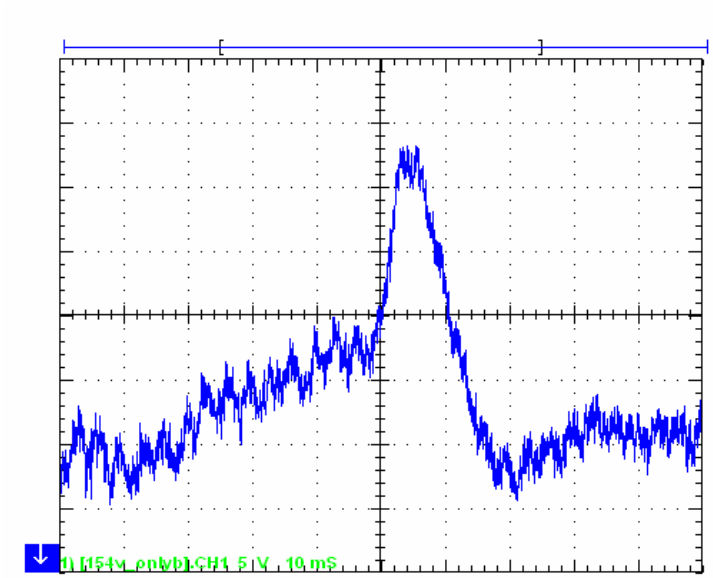


**Figure 6.6.12.** Output voltage for load step at output (amplitude scale 5V/div and time scale 10ms/div). Nominal output voltage is equal to 690V.

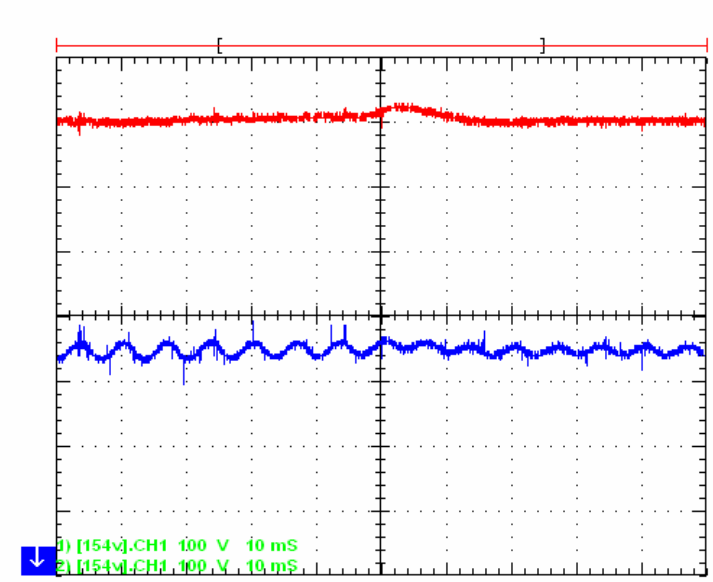



**Figure 6.6.13.** Experimental prototype output voltage (red trace) and mid-point voltage (blue trace) waveforms for load step (scale 100V/div).

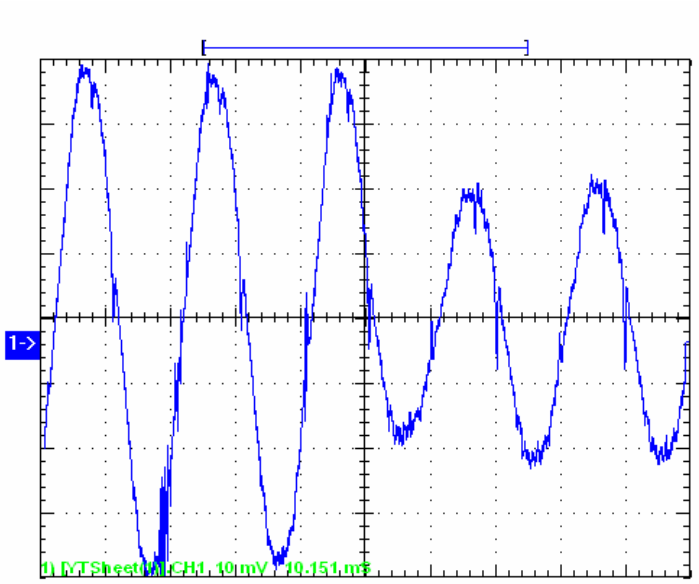


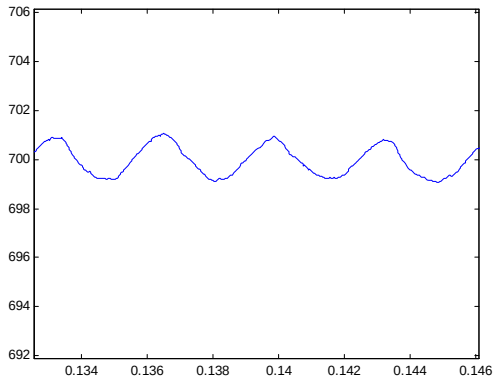
**Figure 6.6.14.** Experimental prototype input current waveform for load step (scale 1A/div).

From figure 6.6.12 it is seen that the output voltage takes approximately 15ms to settle from the load-step disturbance. Observed in figure 6.6.13 is the lower mid-point ripple voltage after the load-step disturbance, due to lower output loading. The decrease in input current amplitude after the load-step disturbance is also evident in figure 6.6.14. From figure 6.6.12 it can be seen that the overshoot of the output voltage is approximately 23V. From equations (3.105) to (3.107) the open-loop compensated phase margin for the system is calculated to be 66.91°, which compares well to the 60° designed-for phase margin and very well to the simulated load step responses using MATLAB and PSpice. This again confirms that the small-signal model, derived in Chapter 4 (modelled in Chapter 3), is an accurate and representative model of the VIENNA rectifier. It can be seen from the step-response results for a 220V input and a 154V input that the phase shift is minimal (less than 3°) for a change in input voltage and thus justifies the selected controller crossover frequency.

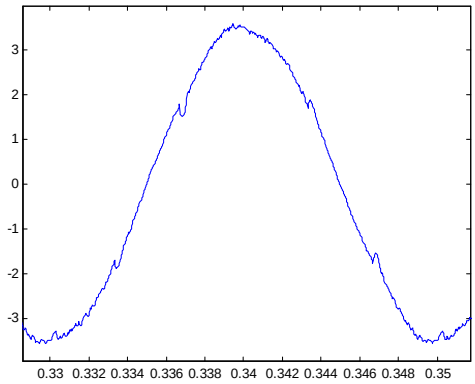
## 6.7 SIMULATED RESULTS – REDUCED INPUT VOLTAGE PREFORMANCE

The digital and analogue simulators were used to determine the performance, or specified output power capability, of the rectifier at reduced input voltages. The simulation was performed at input voltage ratios of 0.8, 0.7, 0.6, and 0.5 of the rated voltage of $V_{LL(rated)}$ = 220V with output loading of 612Ω , 700Ω, 817Ω, and 980Ω respectively. For each input voltage ratio the output loading was chosen to be linearly derated from 1000W in accordance to figure 5.7, i.e. for an input voltage of 132V ($0.6V_{LL(rated)}$) the output loading was chosen to be 817Ω (or equal to 0.6×1000W = 600W). From simulations the resulting output power can be derived for each corresponding input voltage. Shown in figures 6.7.1 to 6.7.5 are the simulation results for a derating of $0.8V_{LL(rated)}$ to $0.5V_{LL(rated)}$.

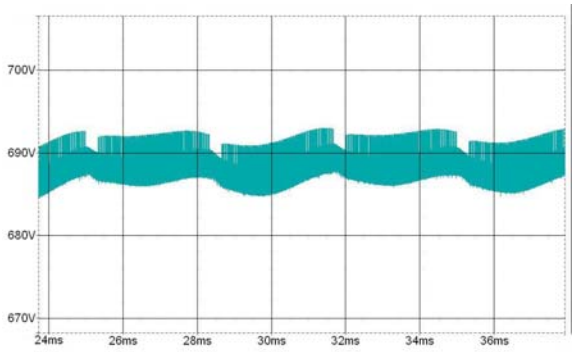
### *I. Input Voltage of $0.8V_{LL}$, Output Loading 612Ω (800W)*



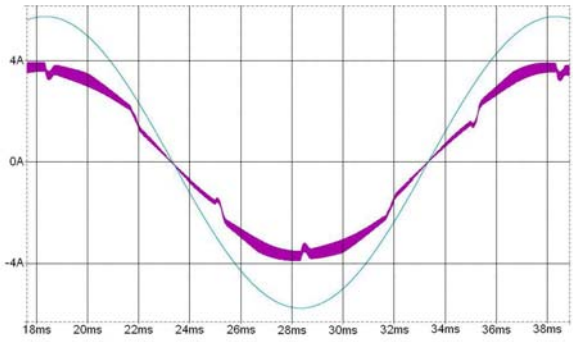

(a) MATLAB simulation output voltage.




(b) MATLAB simulation input current.



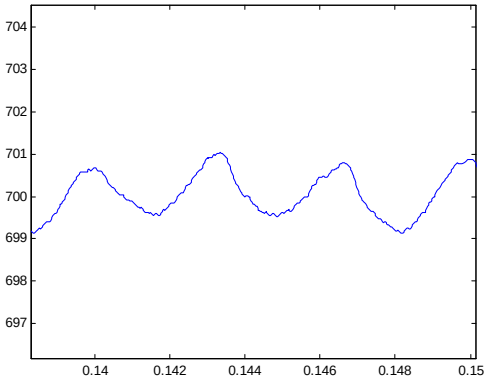

(c) PSpice simulation output voltage.



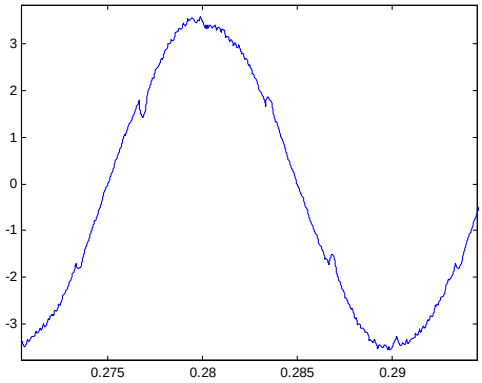

(d) PSpice simulation input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.7.1.** Digital (MATLAB) and analogue (PSpice) simulation output voltage and input current waveforms, for an input voltage of $0.8V_{LL}$ and output load of 612Ω.

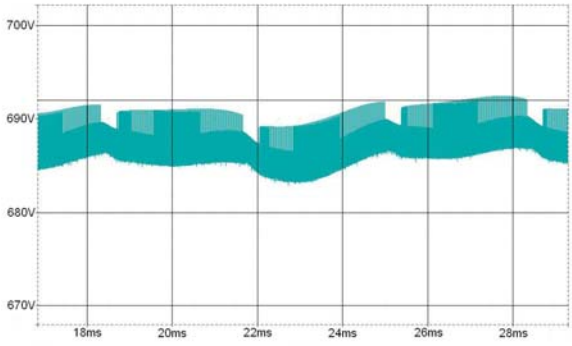
*II. Input Voltage of 0.7$V_{LL}$, Output Loading 700Ω (700W)*



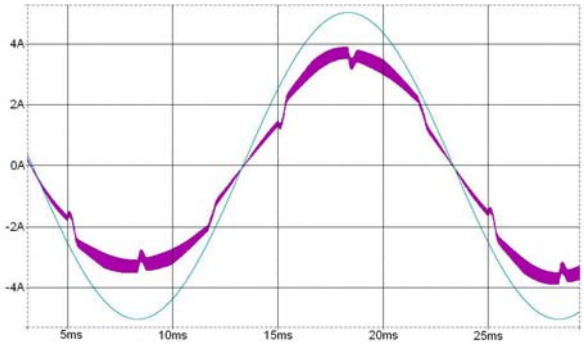

(a) MATLAB simulation output voltage.




(b) MATLAB simulation input current.



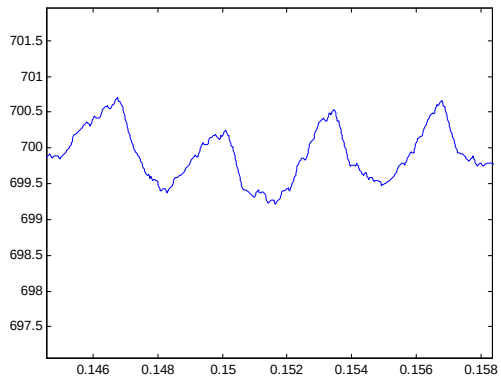

(c) PSpice simulation output voltage.



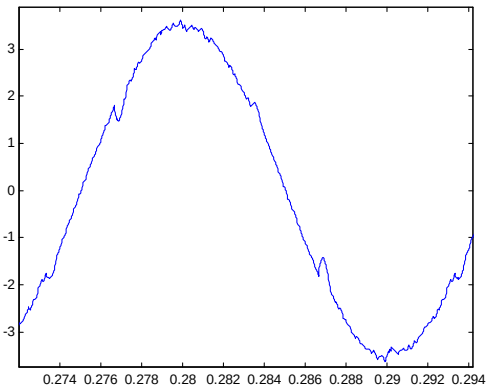

(d) PSpice simulation input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.7.2.** Digital (MATLAB) and analogue (PSpice) simulation output voltage and input current waveforms, for an input voltage of 0.7$V_{LL}$ and output load of 700Ω.

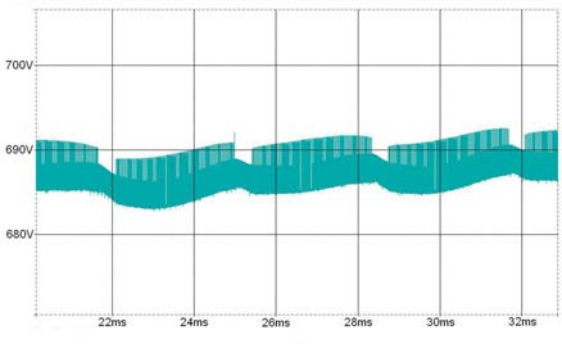
*III. Input Voltage of 0.6$V_{LL}$, Output Loading 817Ω (600W)*



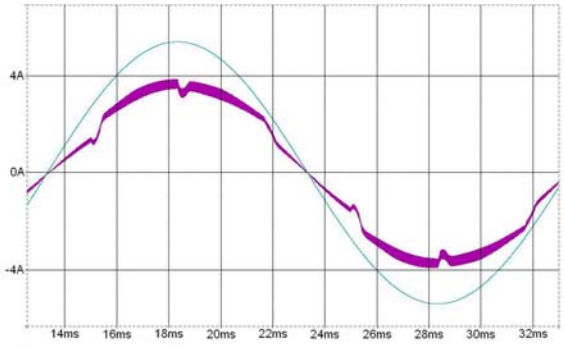

(a) MATLAB simulation output voltage.




(b) MATLAB simulation input current.



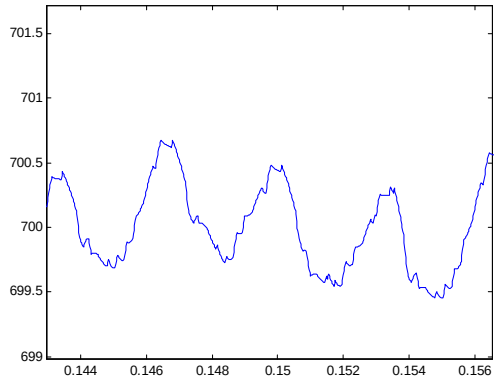

(c) PSpice simulation output voltage.



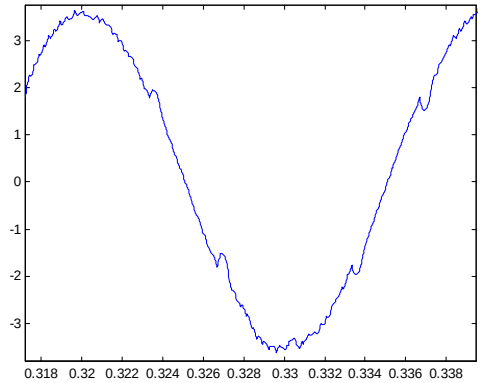

(d) PSpice simulation input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.7.3.** Digital (MATLAB) and analogue (PSpice) simulation output voltage and input current waveforms, for an input voltage of $0.6V_{LL}$ and output load of 817Ω.

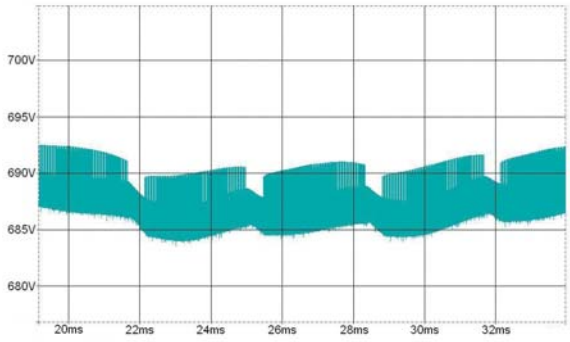
*IV. Input Voltage of $0.5V_{LL}$, Output Loading 980Ω (500W)*



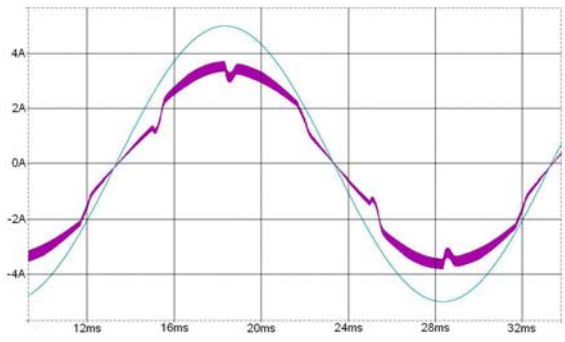

(a) MATLAB simulation output voltage.




(b) MATLAB simulation input current.




(c) PSpice simulation output voltage.




(d) PSpice simulation input current (purple trace) and scaled input voltage (cyan trace).

**Figure 6.7.4.** Digital (MATLAB) and analogue (PSpice) simulation output voltage and input current waveforms, for an input voltage of $0.5V_{LL}$ and output load of 980Ω.

It is clear from the simulations that the analogue and digital simulation-results are comparable and similar. Both simulations indicate that the rectifier is able to supply the derated power for a suitably derated input voltage, even though the digital simulation presents a pure theoretical simulation that does not take into account any component variations and limitations. The analogue simulation represents a much more pessimistic model and is thus more conservative in estimating the supplied power but still indicates that the output voltage remain at the required 700V for derated input voltages, supplying equivalent derated output power. For this reason the analogue simulation model is probably more suitable to use for determining performance at lower input voltages. Sections 6.2 to 6.5 include experimental results at lower input voltages, for as low as 50% the rated input voltage of 220V. From these results it is evident that the prototype results is as was predicted in figure 5.7, for instance at an input voltage of 60% of the rated voltage of 220V the rectifier is able to supply 60% of the rated output power, or 600W (for an output voltage of 700V). This confirms that figure 5.7 is suitable for determining the permissible output power for a derated input voltage. Section 6.5 shows the harmonic spectra at derated input voltages.

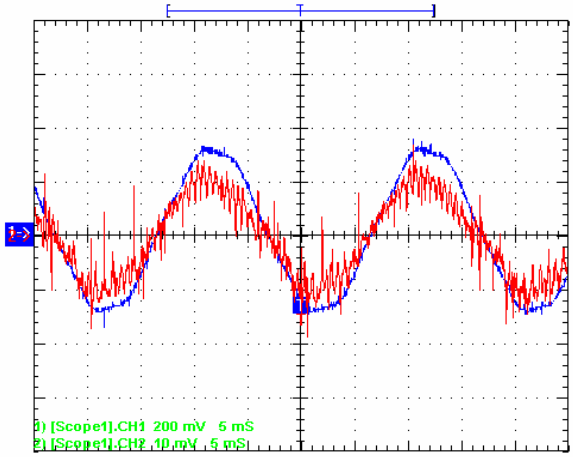
The derating curves derived in section 5.6 for determining the switch and diode currents are valid for the actual rectifier, since the prototype measurements and simulations represent the ideal case where the normalized input current is equal to the normalized input power.

The only obvious disadvantage of operating the VIENNA rectifier at derated (lower) input voltages, might be the inability of the rectifier to maintain the required output voltage of 700V due to the high boost ratio required (for an input of 110V the boost ratio is almost 5!). For future studies this should be seen as a caution for the use of this topology/controller for generator-to-DC type applications.

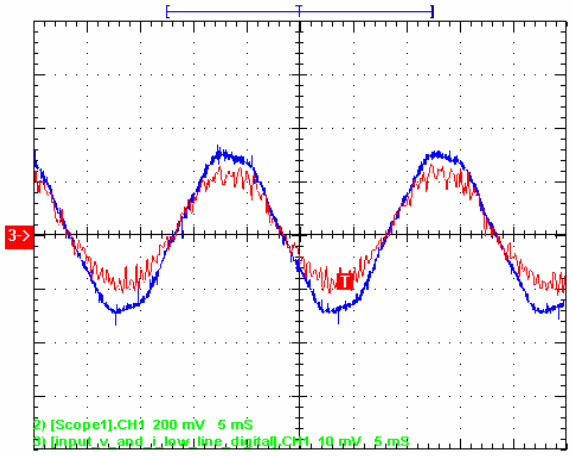
## 6.8 EXPERIMENTAL COMPARISON BETWEEN DIGITAL CONTROLLER AND ANALOGUE CONTROLLER

Shown in figure 6.8.1 are the input currents and scaled input voltages, for an analogue and a digital controller respectively, for an output power of 200W and input voltage of $176V_{LL}$. Shown in figure 6.8.2 is the input currents and input voltages for an output power level of 400W, again for an input voltage of $176V_{LL}$. In both figure 6.8.1 and 6.8.2 it is observed that the current waveforms are similar for the analogue controller and the digital controller. It is also seen that the input current is controllable and is also in phase with input voltage.

Figure 6.8.3 and figure 6.8.3 shows the output voltage waveforms for 200W and 400W respectively. For both the analogue and the digital controller implementations the output voltage is approximately 700V, thus concluding that the digital controller is able to control the output voltage.

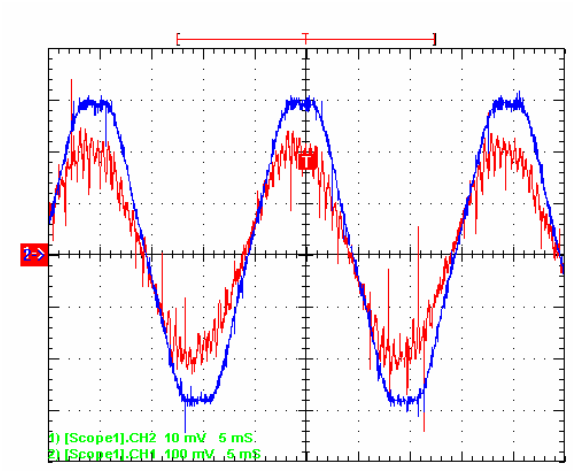



(a) Experimental prototype input current (red trace) and scaled voltage (blue trace) for an analogue controller. Current amplitude scale is 1A/div and time scale 5ms/div.

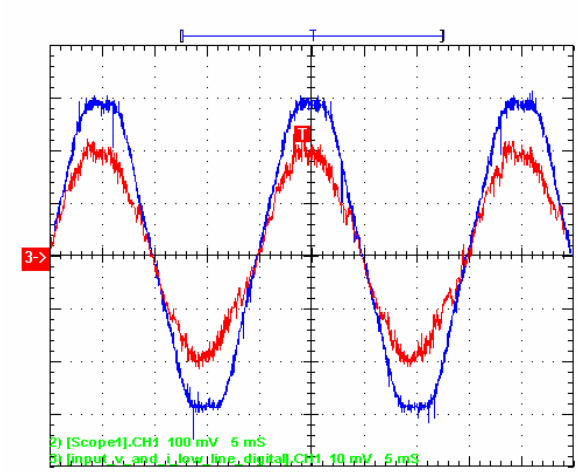



(b) Experimental prototype input current (red trace) and scaled voltage (blue trace) for a digital controller. Current amplitude scale is 1A/div and time scale 5ms/div.

**Figure 6.8.1.** Input current and input voltage waveforms for the (a) analogue controller and (b) digital controller for an input voltage of $176V_{LL}$ and an output loading of 200W.

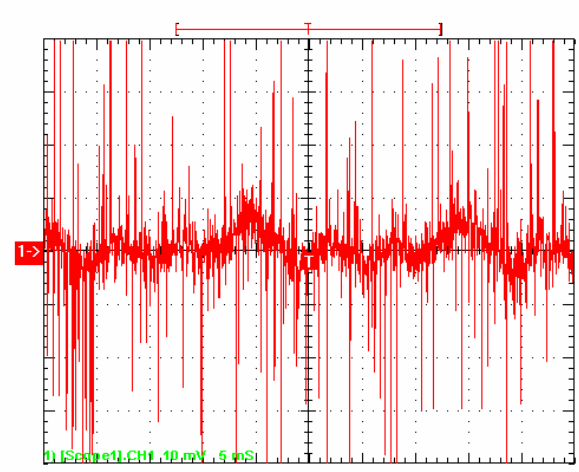



(a) Experimental prototype input current (red trace) and scaled voltage (blue trace) for an analogue controller. Current amplitude scale is 1A/div and time scale 5ms/div.

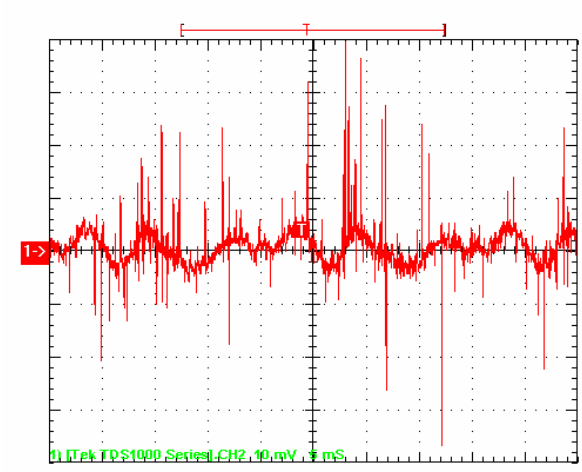



(b) Experimental prototype input current (red trace) and scaled voltage (blue trace) for a digital controller. Current amplitude scale is 1A/div and time scale 5ms/div.

**Figure 6.8.2.** Input current and input voltage waveforms for the (a) analogue controller and (b) digital controller for an input voltage of 176$V_{LL}$ and an output loading of 400W.

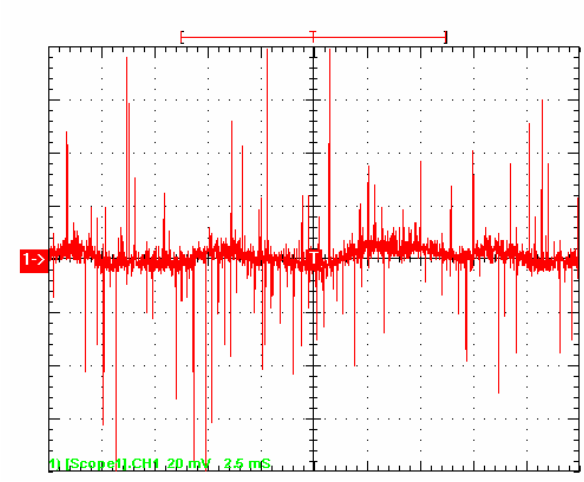



(a) Experimental prototype. Amplitude scale 1V/div and time scale 5ms/div. Average output voltage of 701V.

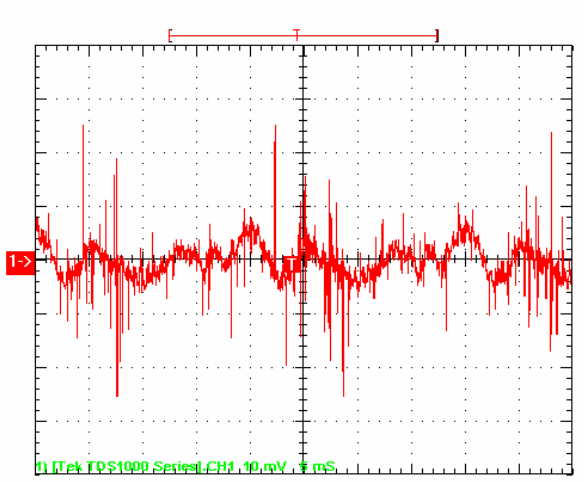



(a) Experimental prototype. Amplitude scale 1V/div and time scale 5ms/div. Average output voltage of 704V.

**Figure 6.8.3.** Output voltage waveforms for the (a) analogue controller and (b) digital controller for an input voltage of 176$V_{LL}$ and an output loading of 200W.



(a) Experimental prototype. Amplitude scale 1V/div and time scale 5ms/div. Average output voltage of 701V.



(a) Experimental prototype. Amplitude scale 1V/div and time scale 5ms/div. Average output voltage of 704V.

**Figure 6.8.4.** Output voltage waveforms for the (a) analogue controller and (b) digital controller for an input voltage of $176V_{LL}$ and an output loading of 400W.

# CHAPTER 7

# CONCLUSION AND REMARKS

## 7.1 SUMMARY

The results obtained through the digital and analogue simulations, as well as through the testing of the VIENNA rectifier prototype, confirmed the following:

- The model obtained for the VIENNA rectifier in Chapter 3 of this dissertation accurately describes the small-signal operation of the VIENNA rectifier when controlled as a dual-boost converter with a constant switching frequency (refer to section 6.6.4). Figure 6.6.9 and figure 6.6.12 shows load step-transient responses indicating a ~67° and ~69° phase margin which compares very well to the design-for phase margin of 60°, verifying the modelling process used in Chapter 2. In these figures it is also visible that there is no significant change in phase margin even at derated input voltage operation (figure 6.6.9 is for operation at $V_{in} = V_{LL}$, whereas figure 6.6.12 is for operation at $V_{in} = 0.7V_{LL}$);
- The equations obtained in Chapter 4 for the design of the input filter (input inductors) and for the design of the output filter (split output capacitor) are accurately obtained for the VIENNA rectifier in terms of the converter performance (refer to sections 6.2 and 6.3);
- The performance of the system is as was predicted/expected in Chapters 4 and 5 of this dissertation, in terms of output voltage ripple, input current ripple and system efficiency (refer to section 6.6.2 and section 6.6.3).
- The VIENNA rectifier is suitable for use in converting a generator type input, with variable voltage and frequency, to a constant DC-voltage output - It was shown in sections 6.2 to 6.5 that the rectifier is able to deliver derated power at derated input voltages (refer specifically to figure 6.4.8(a), figure 6.4.9(a) and 6.4.10(a) where it is observed that the rectifier is able to maintain a constant DC-bus voltage with a derated input voltage). It has also been shown that the rectifier is able to supply 50% of its rated output power even if the input is derated by 50% (of its rated input voltage), with the added advantage of lower peak-to-peak current ripple at lower input voltages (thus reducing filter requirements and lower EMI noise).
- The results in section 6.2 and section 6.5 indicate a power factor of approximately 1 for all input voltage and output power combinations.

## 7.2 CRITICAL EVALUATION OF OWN WORK

The system performed as expected as was shown in section 6.2, where it is seen that the current ripple meets the design specification and also in section 6.6.3 where it is shown that the mid-point capacitor voltage ripple meets the design specification. Step-responses performed on the rectifier (section 6.6.4) shows that the rectifier performed as expected in terms of the transient response of the rectifier. It is shown in this dissertation how to design a VIENNA rectifier (in particular the power stage design), how to obtain the transfer model for the VIENNA rectifier and how to implement the control compensator (digital and analogue) to control the output transient response (design for output overshoot).

The major contribution made by this research was the development of an interface between variable speed three-phase generators and a DC-bus. This type of interface has uses in wind generation systems employing AC generators and also in proposed electrical power systems in automobiles. Although [42] discusses a wide input voltage range converter (6-switch converter), the maximum-to-minimum input voltage ratio of 1.65625 for the converter of [42] is still significantly less than the ratio of 2 for the experimental prototype discussed in this dissertation, suggesting that the VIENNA rectifier might even be more suitable to convert a wide input voltage source to a DC output than a 6-switch topology. Furthermore, the maximum boost ratio achieved for the experimental prototype discussed in this dissertation is $6.36V_{LL}$ which is significantly more than the boost ratio of $2.5V_{LL}$ for the rectifier topology of [42], indicating that the VIENNA rectifier is suitable for boosting very low input voltages and still maintain a constant DC-bus voltage.

The research for this dissertation, in particular Chapter 3 adds mathematical control and plant models to the current available literature base and enables the ability to determine the performance characteristics of the VIENNA rectifier topology (all literature on the VIENNA rectifier focuses mainly on controller topologies and operation of the VIENNA rectifier, but does not include any analysis on the small-signal performance of the VIENNA rectifier [3, 6, 9, 10, 12, 13, 14, 15, 16]). The research for this dissertation (Chapter 4 of this dissertation) adds to current literature base methods to determine and size the filter components of the VIENNA rectifier, which was previously unavailable as seen in [3, 6, 9, 10, 12, 13, 14, 15, 16]. Furthermore, the research performed for this dissertation enables the design of an equivalent three-phase active rectifier, with the inputs and outputs to the system given, as illustrated in Chapter 4 and Chapter 5 Another

contribution made is the addition of a MATLAB simulator to easily predict the performance and to obtain performance outputs, without the need to build a prototype. The MATLAB (digital) simulator provides the user with the ability to effortlessly and quickly estimate and verify system parameters, including output voltage ripple, input current ripple and rectifier transient response, without the expense of building a prototype. In Chapter 5 derating curves were derived that will assist the designer in obtaining and determining the performance of the rectifier, as well as the stress levels of components.

This dissertation investigated the effects of using constant frequency control for actively controlling a three-phase three-switch three-level converter. This dissertation also investigated the use of both analogue and digital controllers. The advantages and disadvantages for each controller, as concluded in the dissertation, are as follow:

- The analogue controller requires less PCB space, but generally more components than the digital controller;
- Any changes in the compensator or the controller design (i.e. change from a PI controller to PID controller) requires a hardware change for the analogue controller, whereas for the digital controller it is a mere software change;
- The digital controller allows the user the flexibility to change controller topology, for example: with the sensing used for implementing the constant switching frequency dual-boost type controller (rectified current sensing on each input, and voltage state sensing), the digital controller can easily be adapted to implement a one-cycle type controller, which only requires current sensing inputs;
- To implement over-current and/or over-voltage protection on the analogue controller requires the addition of hardware, whereas with the digital controller a few lines of software coding is all that is required;
- Simulations performed in section 4.8 of Chapter 4 appear to indicate that a high sampling frequency is required to implement the digital controller, placing a strain on computing power (the DSP thus needs to perform computations at a very high speed).

## 7.3 FUTURE WORK

Although the experimental results obtained in this thesis represent that of a fully functional prototype, the following improvements are, however, suggested for future studies:

- An auxiliary power supply can be added so that the rectifier control circuitry and bootstrap supplies can operate without the need for an external power supply;
- The rectifier Printed Circuit Boards can be redesigned to incorporate a better noise design and also to include ground planes;
- For digital control much of the current-to-voltage amplifier circuitry can be omitted;
- Snubbers can be added to improve the overall efficiency and noise performance;
- Soft-switching techniques can be introduced to improve efficiency and to improve noise performance;
- Future studies can focus on the possible implementation of space-vector control of the VIENNA rectifier [42];
- Future studies can investigate the performance difference between a discrete design, such as implemented for this thesis, and a design using VIENNA rectifier single leg modules [13];
- Future studies can implement the digital controller on hardware and compare the results to that of the analogue controller;
- Future studies can investigate the use of only voltage control of the VIENNA rectifier and compare the performance to that of the constant switching frequency dual-boost controller [43];
- and, Future studies can focus on developing a better and more accurate model for the plant transfer response, by including the capacitor equivalent resistance and inductor series resistance.

# REFERENCES

[1] B. Singh, B.N. Singh, A. Chandra, K Al-Haddad, A. Pandey and D.P. Kothari, "A Review of Three-Phase Improved Power Quality AC-DC Converters", IEEE Transactions on Industrial Electronics, Vol. 51, No. 3, pp.641-660, June 2004.

[2] J.W. Kolar and H. Ertl, "Status of the Techniques of Three-Phase Rectifier Systems with Low Effects on the Mains", 21st INTELEC, Copenhagen, Denmark, pp.14.1 June 1999.

[3] E.H. Ismail and R Erickson, "Single-Switch 3φ PWM Low Harmonic Rectifiers", IEEE Transactions on Electronics, Vol. 11, No. 2, pp.338-346, March 1996.

[4] M. Tou, K. Al-Haddad, G. Olivier and V.R. Rajagopalan, "Analysis and Design of Single-Controlled Switch Three-Phase Rectifier with Unity Power Factor and Sinusoidal Input Current", IEEE Transactions on Electronics, Vol. 2, No. 4, pp.856-862, July 1997.

[5] J.C. Salmon, "Circuit topologies for pwm boost rectifiers operated from 1-phase and 3-phase ac supplies and using either single or split dc rail voltage outputs", Applied Power Electronics Conference and Exposition (APEC), Conference Proceedings, Vol. 1, pp. 473-479, 1995.

[6] J.C. Salmon, "Operating a Three-phase diode rectifier with a low-input current distortion using a series-connected dual boost converter", IEEE Transactions on Power Electronics, Vol. 11, Issue 4, pp.592-603, July 1996.

[7] J.C. Salmon, "Comparative evaluation of circuit topologies for 1-phase and 3-phase boost rectifiers operated with a low current distortion", Canadian Conference on Electrical and Computer Engineering, Conference Proceedings, Vol. 1, pp.30-33, September 1994.

[8] C. Qiao and K.M. Smedley, "A General Three-Phase PFC Controller Part I. for Rectifiers with a Parallel-Connected Dual Boost Topology", Conference Record of the 1999 IEEE Industry Applications Conference, Thirty-Fourth IAS Annual Meeting,Vol. 4, pp. 2504-2511, 1999.

[9] J. Miniböck and J.W. Kolar, "Comparative Theoretical and Experimental Evaluation of Bridge Leg Topologies of a Three-Phase Three-Level Unity Power Factor Rectifier", 32nd Power Electronics Specialists Conference, Conference Proceedings, Vol. 3, pp.1641-1646, June 2001.

[10] C. Qiao and K.M. Smedley, "A General Three-Phase PFC Controller Part II. for Rectifiers with a Series-Connected Dual Boost Topology", IEEE Transactions on Industry Applications, Vol. 38 Issue 1, pp.137-148, January/February 2002.

[11] J.C. Salmon, "3-phase pwm boost rectifier circuit topologies using 2-level and 3-level asymmetrical half-bridges", Applied Power Electronics Conference and Exposition (APEC), Conference Proceedings, Vol. 2, pp.842-848, 1995.

[12] T. Jin, J. Wen and K. Smedley, "Control and Topologies for Three-Phase Three-level Active Power Filters", Power Electronics and Motion Control Conference (IPEMC), The 4th International, Vol. 2, pp.450-455, August 2004.

[13] J.W. Kolar, H. Ertl, F.C. Zach, "Design and Experimental Investigation of a Three-Phase High Power Density High Efficiency Unity Power Factor PWM (VIENNA) Rectifier Employing a Novel Integrated Power Semiconductor Module", Applied Power Electronics Conference and Exposition (APEC) Conference Proceedings, Eleventh Annual, Vol. 2, pp.514-523, 1996.

[14] C. Qiao and K.M. Smedley, "Three-phase Unity-Power-Factor VIENNA Rectifier with Unified Constant-Frequency Integration Control", 7th IEEE International Power Electronics Congress, Conference Proceedings, pp.125-130, 2000.

[15] J.W. Kolar and F.C. Zach, "A Novel Three-Phase Utility Interface Minimizing Line Current Harmonics of High-Power Telecommunications Rectifier Modules", IEEE Transactions on Industrial Electronics, Vol. 44, Issue 4, pp.456-467, August 1997.

[16] L. Dalessandro, U. Drofenik, S.D. Round and J.W. Kolar, "A Novel Hysteresis Current Control for Three-Phase Three-Level PWM Rectifiers", IEEE Applied Power Electronics Conference and Exposition (APEC), Twentieth Annual, Conference Proceedings, Vol. 1, pp. 501-507, March 1995.

[17] N. Mohan, T.M. Undeland, W.P. Robbins, "Power Electronics – Converters, Applications and Design, Second Edition", Chapter 10, John Wiley & Sons, Inc., 1995.

[18] M.N. Gitau, "Mathematical Modeling of Analogue Controlled Voltage Source Converters for Improved Dynamic Response", Journal of Circuits, Systems, and Computers, Vol. 8, No. 4, pp.483-496, 1998.

[19] C.H. Edwards, Jr., D.E. Penney, "Elementary Differential Equations Third Edition", Chapter 4, John Wiley & Sons, Inc., 1995.

[20] G.C. Goodwin, S.F. Graebe and M.E. Salgado, "Control System Design", Chapter 17, Prentice Hall, 2001.

[21] I.K. Craig, Class notes for Automation EBT410, University of Pretoria, 2001.

[22] M.N. Gitau, Class notes for Power Electronics EED780, University of Pretoria, 2002.

[23] N.S. Nise, "Control Systems Engineering", Appendix G, John Wiley & Sons , Inc., 2000.

[24] N.S. Nise, "Control Systems Engineering", Chapter 11, John Wiley & Sons, Inc., 2000.

[25] G.C. Chryssis, "High-Frequency Switching Power Supplies", McGraw-Hill Companies; 2nd edition, March 1989.

[26] N.S. Nise, "Control Systems Engineering, Third Edition", Chapter 4, John Wiley & Sons, Inc., 2000.

[27] C. Qiao and K.M. Smedley, "Unified Constant-frequency Integration Control of Three-phase Standard Bridge Boost Rectifier", 7th IEEE International Power Electronics Congress, Conference Proceedings, pp.131-135, 2000.

[28] N. Mohan, T.M. Undeland and W.P Robbins, "Power Electronics – Converters, Applications and Design Second Edition", Chapter 3, John Wiley & Sons, Inc., 1995.

[29] N. Mohan, T.M. Undeland, W.P. Robbins, "Power Electronics – Converters, Applications and Design Second Edition", Chapter 5, John Wiley & Sons, Inc., 1995.

[30] N.S. Nice, "Control Systems Engineering, Third Edition", Chapter 10, John Wiley & Sons, Inc., 2000.

[31] N.S. Nice, "Control Systems Engineering, Third Edition", Chapter 7, John Wiley & Sons, Inc., 2000.

[32] N.S. Nice, "Control Systems Engineering, Third Edition", Chapter 13, John Wiley & Sons, Inc., 2000.

[33] G. Potter, "An Introduction to Digital Control of Switching Power Converters", Astec Power, 2004.

[34] W. Forsythe and R.M. Goodall, "Digital Control", Chapter 6, Macmillan Education, 1991.

[35] N. Mohan, T.M. Undeland and W.P Robbins, "Power Electronics – Converters, Applications and Design, Second Edition", Chapter 2, John Wiley & Sons, Inc., 1995.

[36] "Soft Ferrites and Accessories – 2002 Handbook", Ferroxcube, 2002.

[37] "Effect of an Air Gap – mmg-GappedCores.pdf", MMG Neosid, 2001.

[38] N. Mohan, T.M. Undeland and W.P Robbins, "Power Electronics – Converters, Applications and Design, Second Edition", Chapter 30, John Wiley & Sons, Inc., 1995.

[39] HCPL-316J Datasheet, "2.0 Amp Gate Drive Opto-Coupler with Integrated (VCE) Desaturation Detection and Fault Status Feedback", Agilent, 2004.

[40] T. Nussbaumer and J.W. Kolar, "Comparative Evaluation of Control Techniques for a Three-Phase Three-Switch Buck-Type AC-to-DC PWM Converter System", 3rd IEEE Nordic Workshop on Power and Industrial Electronics, Conference Proceedings, August 2002.

[41] N. Mohan, T.M. Undeland and W.P. Robbins, "Power Electronics – Converters, Applications and Design, Second Edition", Chapter 6, John Wiley & Sons, Inc., 1995.

[42] J. Miniböck and J.W. Kolar, "Wide Input Voltage Range High Power Density High Efficiency 10kW Three-Phase Three-Level Unity Power Factor PWM Rectifier", 33rd IEEE Annual Power Electronics Specialists Conference, Conference Proceedings, pp. 1642, 2002.

[43] B. Wang, G. Venkataramanan, A. Bendre, "Unity power factor control for three phase three level rectifiers without current sensors", Industry Applications Conference, Conference Proceedings, Fourtieth IAS Annual Meeting, Vol. 3, pp.1677-1683, October 2005.

[44] N. Mohan, T.M. Undeland and W.P Robbins, "Power Electronics – Converters, Applications and Design, Second Edition", Chapter 29, John Wiley & Sons, Inc., 1995.

# APPENDIX A

# DIODE RMS CURRENTS FOR HYSTERESIS TYPE CONTROL

From [13], the transformation ratio M is defined as:

$$M = \frac{U_0}{\sqrt{3}\hat{U}_N}, \quad \text{A.1}$$

where $U_0$ is the output voltage and equal to 700V (table 3.1 - $V_{OUT}$), and $U_N$ the peak input voltage and equal to 143.7V (table 3.1 – $V_{p,peak}$). Thus will M be equal to:

$$M = \frac{700}{\sqrt{3} \times 143.7} = 2.812 \quad \text{A.2}$$

From [13] the designation of the diodes are as follow:

$$D_1 = D_{F+} \quad \text{A.3}$$

$$D_2 = D_{F-} \quad \text{A.4}$$

$$D_3 = D_{N+} \quad \text{A.5}$$

$$D_5 = D_{N-} \quad \text{A.6}$$

$$D_4 = D_{M+} \quad \text{A.7}$$

$$D_6 = D_{M-} \quad \text{A.8}$$

From [13] the rms current for diodes $D_{F+}$ and $D_{F-}$ can be calculated as ($I_N$ is the peak input current and equal to 4.64A – from table 3.1):

$$i_{D1,rms} = i_{D2,rms} = i_{DF,rms} = \hat{I}_N \times \sqrt{\frac{4}{3\sqrt{3}\pi}\frac{1}{M}} = 4.64 \times \sqrt{\frac{4}{3\sqrt{3}\pi}\frac{1}{2.812}} = 1.37A \quad \text{A.9}$$

From [13] the rms current for diodes $D_{M+}$ and $D_{M-}$ can be calculated as:

$$i_{D4,rms} = i_{D6,rms} = i_{DM,rms} = \hat{I}_N \times \sqrt{\frac{1}{4} - \frac{4}{3\sqrt{3}\pi}\frac{1}{M}} = 4.64 \times \sqrt{\frac{1}{4} - \frac{4}{3\sqrt{3}\pi}\frac{1}{2.812}} = 1.76A \quad \text{A.10}$$

From [13] the rms current for diodes $D_{N+}$ and $D_{N-}$ can be calculated as:

$$i_{D3,rms} = i_{D5,rms} = i_{DN,rms} = \frac{1}{2}\hat{I}_N = \frac{1}{2} \times 4.64 = 2.32A \quad \text{A.11}$$

From [13] the rms current for the switch can be calculated as:

$$i_{T,rms} = \hat{I}_N \times \sqrt{\frac{1}{2} - \frac{8}{3\sqrt{3}\pi}\frac{1}{M}} = 4.64 \times \sqrt{\frac{1}{2} - \frac{8}{3\sqrt{3}\pi}\frac{1}{2.812}} = 2.65A \quad \text{A.12}$$

# APPENDIX B

# MATLAB SCRIPT FOR DETERMINING THE UNCOMPENSATED OPEN-LOOP TRANSFER FOR THE VIENNA RECTIFIER

```
% VIENNA rectifier analysis - state space

L=3.15e-3;                                                  %Filter Inductor
C=66E-6;                                                    %Filter Capacitor
rc=0.8;                                                     %Filter Capacitor ESR
Dp=0.384;                                                   %Positive duty cycle
Dn=1;                                                       %Negative duty cycle
RL=490;                                                     %Equivalent Output Load
vp=143.7;                                                   %Positive voltage
vn=-71.85;                                                  %Negative voltage
Ip=4.64;
In=-2.32;
Vref=2.5;                                                   %Reference voltage
Vout=700;                                                   %Output voltage
Rsense=0.17;                                                %Sensing resistance
Vm=1.92;
VLL=176;                                                    %RMS input voltage

% main program
syms s Dp Dn X30 X40

X10=Ip;
X20=In;

sI=[[s 0 0 0];[0 s 0 0];[0 0 s 0];[0 0 0 s]];

%(1-Dp) terms
A_1=[[0 0 -2/(3*L) 0];[0 0 1/(3*L) 0];[1/C 0 0 0];[0 0 0 0]];
B_1=[[0];[0];[0];[0]];
C_1=[0 0 0 0];

% (1-Dn) terms
A_2=[[0 0 0 -1/(3*L)];[0 0 0 2/(3*L)];[0 0 0 0];[0 -1/C 0 0]];
B_2=[[0];[0];[0];[0]];
C_2=[0 0 0 0];

% Constant terms
A_3=[[0 0 0 0];[0 0 0 0];[0 0 -1/(C*(2*rc+RL)) -1/(C*(2*rc+RL))];[0 0 -1/(C*(2*rc+RL)) -
1/(C*(2*rc+RL))]];
B_3=[[vp/L];[vn/L];[0];[0]];
C_3=[0 0 1 1];

S=solve( ((1-Dp)*A_1(1,:)+(1-Dn)*A_2(1,:)+A_3(1,:))*[[X10];[X20];[X30];[X40]]+(1-
Dp)*B_1(1)+(1-Dn)*B_2(1)+B_3(1), ((1-Dp)*A_1(2,:)+(1-
Dn)*A_2(2,:)+A_3(2,:))*[[X10];[X20];[X30];[X40]]+(1-Dp)*B_1(2)+(1-Dn)*B_2(2)+B_3(2), ((1-
Dp)*A_1(3,:)+(1-Dn)*A_2(3,:)+A_3(3,:))*[[X10];[X20];[X30];[X40]]+(1-Dp)*B_1(3)+(1-
Dn)*B_2(3)+B_3(3), ((1-Dp)*A_1(4,:)+(1-Dn)*A_2(4,:)+A_3(4,:))*[[X10];[X20];[X30];[X40]]+(1-
Dp)*B_1(4)+(1-Dn)*B_2(4)+B_3(4));

S.Dp=double(S.Dp(1));
S.Dn=double(S.Dn(1));
V1=double(S.X30(1));
V2=double(S.X40(1));
V1=Vout/2;
V2=Vout/2;

A=(1-S.Dp)*A_1+(1-S.Dn)*A_2+A_3;

sI_A=sI-A;
inv_sI_A=inv(sI_A);

X=[[Ip];[In];[V1];[V2]];

[N1,D1]=numden(inv_sI_A(1,1));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_11=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(1,2));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_12=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(1,3));
Npoly=sym2poly(N1);
```

```
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_13=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(1,4));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_14=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(2,1));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_21=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(2,2));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_22=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(2,3));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_23=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(2,4));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_24=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(3,1));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_31=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(3,2));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_32=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(3,3));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_33=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(3,4));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_34=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(4,1));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_41=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(4,2));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
```

```
Dpoly=Dpoly/Dpoly(1);
A_42=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(4,3));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_43=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(4,4));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_44=tf(Npoly,Dpoly);


ip=[(-A_13*Ip/C+2*A_11*V1/(3*L)-A_12*V1/(3*L)) (A_14*In/C+A_11*V2/(3*L)-2*A_12*V2/(3*L))];
in=[(-A_23*Ip/C+2*A_21*V1/(3*L)-A_22*V1/(3*L)) (A_24*In/C+A_21*V2/(3*L)-2*A_22*V2/(3*L))];

v2=[(-A_43*Ip/C+2*A_41*V1/(3*L)-A_42*V1/(3*L)) (A_44*In/C+A_41*V2/(3*L)-2*A_42*V2/(3*L))];
v1=[(-A_33*Ip/C+2*A_31*V1/(3*L)-A_32*V1/(3*L)) (A_34*In/C+A_31*V2/(3*L)-2*A_32*V2/(3*L))];

vo=v1+v2;

vctl_p=(Rsense)*(2*ip+in);
vctl_n=(Rsense)*(-2*in-ip);

Tfb=(Vref/Vout);
Out_matrix=[[v1];[v2]];
Ctl_matrix=[[vctl_p];[vctl_n]];
Ctl_matrix=minreal(Ctl_matrix);
det_Ctl_matrix=Ctl_matrix(1,1)*Ctl_matrix(2,2)-Ctl_matrix(2,1)*Ctl_matrix(1,2);
det_Ctl_matrix=minreal(det_Ctl_matrix);
inv_Ctl_matrix=(1/det_Ctl_matrix)*[[Ctl_matrix(2,2) -Ctl_matrix(1,2)];[-Ctl_matrix(2,1)
Ctl_matrix(1,1)]];
inv_Ctl_matrix=minreal(inv_Ctl_matrix);

%Open loop transfer function analysis
Out_matrix=minreal(Out_matrix);
inv_Ctl_matrix=minreal(inv_Ctl_matrix);
Tol=Tfb*[[2] [2]]*(Out_matrix*inv_Ctl_matrix);

Tol2=minreal((Tol(1)+Tol(2)),0.5);
bode(Tol2,{1;100E3});
```

```
% VIENNA rectifier analysis - state space

L=3.15e-3;                                                  %Filter Inductor
C=66E-6;                                                    %Filter Capacitor
rc=0.8;                                                     %Filter Capacitor ESR
Dp=0.281;                                                   %Positive duty cycle
Dn=1;                                                       %Negative duty cycle
RL=490;                                                     %Equivalent Output Load
vp=180;                                                     %Positive voltage
vn=-90;                                                     %Negative voltage
Ip=3.704;
In=-1.8519;
Vref=2.5;                                                   %Reference voltage
Vout=700;                                                   %Output voltage
Rsense=0.17;                                                %Sensing resistance
Vm=1.32;
VLL=220;                                                    %RMS input voltage

% main program
syms s Dp Dn X30 X40

X10=Ip;
X20=In;

sI=[[s 0 0 0];[0 s 0 0];[0 0 s 0];[0 0 0 s]];

%(1-Dp) terms
A_1=[[0 0 -2/(3*L) 0];[0 0 1/(3*L) 0];[1/C 0 0 0];[0 0 0 0]];
B_1=[[0];[0];[0];[0]];
C_1=[0 0 0 0];

% (1-Dn) terms
A_2=[[0 0 0 -1/(3*L)];[0 0 0 2/(3*L)];[0 0 0 0];[0 -1/C 0 0]];
B_2=[[0];[0];[0];[0]];
C_2=[0 0 0 0];

% Constant terms
A_3=[[0 0 0 0];[0 0 0 0];[0 0 -1/(C*(2*rc+RL)) -1/(C*(2*rc+RL))];[0 0 -1/(C*(2*rc+RL)) -
1/(C*(2*rc+RL))]];
B_3=[[vp/L];[vn/L];[0];[0]];
C_3=[0 0 1 1];

S=solve( ((1-Dp)*A_1(1,:)+(1-Dn)*A_2(1,:)+A_3(1,:))*[[X10];[X20];[X30];[X40]]+(1-
Dp)*B_1(1)+(1-Dn)*B_2(1)+B_3(1), ((1-Dp)*A_1(2,:)+(1-
Dn)*A_2(2,:)+A_3(2,:))*[[X10];[X20];[X30];[X40]]+(1-Dp)*B_1(2)+(1-Dn)*B_2(2)+B_3(2), ((1-
Dp)*A_1(3,:)+(1-Dn)*A_2(3,:)+A_3(3,:))*[[X10];[X20];[X30];[X40]]+(1-Dp)*B_1(3)+(1-
Dn)*B_2(3)+B_3(3), ((1-Dp)*A_1(4,:)+(1-Dn)*A_2(4,:)+A_3(4,:))*[[X10];[X20];[X30];[X40]]+(1-
Dp)*B_1(4)+(1-Dn)*B_2(4)+B_3(4));

S.Dp=double(S.Dp(1));
S.Dn=double(S.Dn(1));
V1=double(S.X30(1));
V2=double(S.X40(1));
V1=Vout/2;
V2=Vout/2;

A=(1-S.Dp)*A_1+(1-S.Dn)*A_2+A_3;

sI_A=sI-A;
inv_sI_A=inv(sI_A);

X=[[Ip];[In];[V1];[V2]];

[N1,D1]=numden(inv_sI_A(1,1));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_11=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(1,2));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_12=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(1,3));
Npoly=sym2poly(N1);
```

```
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_13=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(1,4));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_14=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(2,1));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_21=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(2,2));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_22=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(2,3));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_23=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(2,4));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_24=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(3,1));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_31=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(3,2));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_32=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(3,3));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_33=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(3,4));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_34=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(4,1));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_41=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(4,2));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
```

```
Dpoly=Dpoly/Dpoly(1);
A_42=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(4,3));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_43=tf(Npoly,Dpoly);

[N1,D1]=numden(inv_sI_A(4,4));
Npoly=sym2poly(N1);
Dpoly=sym2poly(D1);
Npoly=Npoly/Dpoly(1);
Dpoly=Dpoly/Dpoly(1);
A_44=tf(Npoly,Dpoly);


ip=[(-A_13*Ip/C+2*A_11*V1/(3*L)-A_12*V1/(3*L)) (A_14*In/C+A_11*V2/(3*L)-2*A_12*V2/(3*L))];
in=[(-A_23*Ip/C+2*A_21*V1/(3*L)-A_22*V1/(3*L)) (A_24*In/C+A_21*V2/(3*L)-2*A_22*V2/(3*L))];

v2=[(-A_43*Ip/C+2*A_41*V1/(3*L)-A_42*V1/(3*L)) (A_44*In/C+A_41*V2/(3*L)-2*A_42*V2/(3*L))];
v1=[(-A_33*Ip/C+2*A_31*V1/(3*L)-A_32*V1/(3*L)) (A_34*In/C+A_31*V2/(3*L)-2*A_32*V2/(3*L))];

vo=v1+v2;

vctl_p=(Rsense)*(2*ip+in);
vctl_n=(Rsense)*(-2*in-ip);

Tfb=(Vref/Vout);
Out_matrix=[[v1];[v2]];
Ctl_matrix=[[vctl_p];[vctl_n]];
Ctl_matrix=minreal(Ctl_matrix);
det_Ctl_matrix=Ctl_matrix(1,1)*Ctl_matrix(2,2)-Ctl_matrix(2,1)*Ctl_matrix(1,2);
det_Ctl_matrix=minreal(det_Ctl_matrix);
inv_Ctl_matrix=(1/det_Ctl_matrix)*[[Ctl_matrix(2,2) -Ctl_matrix(1,2)];[-Ctl_matrix(2,1)
Ctl_matrix(1,1)]];
inv_Ctl_matrix=minreal(inv_Ctl_matrix);

%Open loop transfer function analysis
Out_matrix=minreal(Out_matrix);
inv_Ctl_matrix=minreal(inv_Ctl_matrix);
Tol=Tfb*[[2] [2]]*(Out_matrix*inv_Ctl_matrix);

Tol2=minreal((Tol(1)+Tol(2)),0.5);
bode(Tol2,{1;100E3});
```

# APPENDIX C

# MATLAB SCRIPT FOR DETERMINING THE OUTPUT CAPACITANCE FOR THE VIENNA RECTIFIER

```
%MATLAB script to determine the capacitance needed for a VIENNA rectifier

Iout=1.429;                                %output current
Tl=1/50;                                   %period of line voltages
Tsw=1/50000;                               %period of switching frequency
E=350;                                     %average voltage over capacitor1 and capacitor2
Vpeak=143.7;                               %peak input voltage (line-to-neutral)
Ipeak=4.64;                                %peak input current (line-to-neutral)

vripple=53.35;                             %output ripple voltage (between capacitor banks)


%main script
y=round((Tl*30/360)/Tsw);

sum_of=0;
sum_of_rms=0;

%This part of the script determines the rms ripple current through the capacitor bank and
%the capacitance needed at the output
for l=1:y+1
   x=l-1;
   Dn=1+(-2*Vpeak*cos((x*Tsw-Tl/6)*2*3.14159/Tl)+Vpeak*cos(x*Tsw*2*3.14159/Tl))/(E-
(vripple/2)*sin(x*Tsw*3.14159/(Tl/12)));
   sum_of=sum_of+sin(((x+1)*Tsw-Tl/6)*2*3.14159/Tl)-sin((x*Tsw+Dn*Tsw-Tl/6)*2*3.14159/Tl);
   in=-Ipeak*cos(2*3.14159*Tsw*(x+1)/Tl-120*3.14159/360);
   sum_of_rms=sum_of_rms+(1-Dn)*Tsw*(in+Iout)^2+Dn*Tsw*Iout^2;
end

C1=2*abs(Iout*Tl/12-Ipeak*Tl*sum_of/(2*3.14159))/vripple
irms=sqrt(6*sum_of_rms/Tl)

%This part of the script determines the peak-to-peak voltage ripple for a given capacitance
Iout=1.428;                                %output current
Tl=1/50;                                   %period of line voltages
Tsw=1/50000;                               %period of switching frequency
E=350;                                     %average voltage over capacitor1 and capacitor2
Vpeak=143.7;                               %peak input voltage (line-to-neutral)
Ipeak=4.714;                              %peak input current (line-to-neutral)

C1=66E-6;
vripple=2*abs(Iout*Tl/12-Ipeak*Tl*sum_of/(2*3.14159))/C1

y=round((Tl*60/360)/Tsw);

sum_of=0;
sum_of_rms=0;

%This part of the script determines the rms current through D1
for l=1:y+1
   x=l-1;
   Dp=1-(-Vpeak*cos((x*Tsw-
Tl/6)*2*3.14159/Tl)+2*Vpeak*cos(x*Tsw*2*3.14159/Tl))/(E+(vripple/2)*sin(x*Tsw*3.14159/(Tl/1
2)));
   iD3=Ipeak*cos(2*3.14159*Tsw*(x)/Tl);
   sum_of=sum_of+iD3^2*(1-Dp)*Tsw;

end

iD1_rms=sqrt(2*sum_of/Tl)

sum_of=0;
sum_of_rms=0;
sum_of_iD3=0;

%This part of the script determines the sum of the currents through the switch (Chapter
4.3)
for l=1:y+1
   x=l-1;
   iD3=Ipeak*cos(2*3.14159*Tsw*(x)/Tl);
   sum_of=sum_of+iD3^2*(Dp)*Tsw;
   sum_of_iD3=sum_of_iD3+iD3;
    end

syms t;

temp=int(Ipeak*cos(2*3.14159*t/Tl)^2,t,Tl*60/360,Tl*90/360);
```

```
temp=double(temp);


iT_rms=sqrt((4/Tl)*sum_of+temp)
iD4_rms=sqrt((2/Tl)*sum_of+temp)
```

# APPENDIX D

# MATLAB SCRIPT FOR DIGITAL SIMULATION OF THE VIENNA RECTIFIER

```
% EIR 890 - Electrical dissertation
% VIENNA rectifier digital MATLAB simulation

iterations = 6;

%initial conditions & system parameters
fsw=50E3;                                                    %switching
frequency
fl=50;                                                       %line frequency
fsample=10E3;                                                %sampling frequency
Vamp=176;                                                    %Phase line to
neutral amplitude voltage
ia(1)=4*(-0.5);                                              %initial inductor
current through phase a
ib(1)=4*(-0.5);                                              %initial inductor
current through phase b
ic(1)=4;                                                     %initial inductor
current through phase c
E1=350;                                                      %initial voltage
across capacitor 1
E2=350;                                                      %initial voltage
across capacitor 2
E(1)=E1+E2;
EN(1)=E2;
Vph_a(1)=Vamp*(-0.5);                                        %constant (do not
change)
Vph_b(1)=Vamp*(-0.5);                                        %constant (do not
change)
Vph_c(1)=Vamp;                                               %constant (do not
change)
%Circuit values
Rs=0.17;                                                     %sensing resistance
La=3.15E-3;                                                  %phase a inductance
Lb=3.15E-3;                                                  %phase b inductance
Lc=3.15E-3;                                                  %phase c inductance
C1=66E-6;                                                    %Capacitor 1
C2=66E-6;                                                    %Capacitor 2
Iout=0.286;                                                    %Average output
current
Vout=700;                                                    %Output regulation
voltage
Rout=Vout/Iout;                                              %Equivalent output
resistance (do not change)
resolution=30;                                               %(Constant)
proc_V=3.3;


% Controller parameters

A=1;                                                         %Voltage loop
compensator gain

a1=0;
a2=0.988;
a3=-0.959;

b1=1;
b2=-1.710;
b3=0.710;

a4=0;
b4=0;

e1=0;
e2=0;
e3=0;
e4=0;

x1=0;
x2=0;
x3=0;
x4=0;


%average current filter
a11=0;
a12=0.467;
b11=1;
b12=-0.533;
```

```
a11=1;
a12=0;
b11=1;
b12=0;


ep1=ic(1);
ep2=ic(1);

en1=-ia(1);
en2=-ia(1);

xp1=ic(1);
xp2=ic(1);
xp3=ic(1);
xn1=-ia(1);
xn2=-ia(1);
xn3=-ia(1)


%*************************************************************************************************
*******************************
% MAIN PROGRAM
%*************************************************************************************************
*******************************
E_out(1)=E1+E2;
EN_out(1)=E2;
c_control(1)=0;
iripple=0;

tc=2;
t=(tc-1)*(1/fsw);
time(tc)=t;

Divider=Vout/2.5;

Vc=Vph_c(1);
Va=Vph_a(1);
Vb=Vph_b(1);
ip=ic(tc-1);
in=ib(tc-1);
it=ia(tc-1);

E=E1+E2;
EN=E2;
Iout=E/Rout;
Vo=E/Divider;
e3=e2;
e2=e1;
e1=2.5-Vo;
x3=x2;
x2=x1;
x1=A*(e1*a1+e2*a2+e3*a3)-(x2*b2+x3*b3);
VM=2.5+x1;

ip_s=2*ip*Rs+in*Rs;
in_s=-2*in*Rs-ip*Rs;

ep2=ep1;
ep1=ip_s;
xp3=xp2;
xp2=xp1;
xp1=(a11*ep1+a12*ep2)-(b12*xp2);
xp1=(a11*ep1+a12*ep2)-(b12*xp2);


en2=en1;
en1=in_s;
xn3=xn2;
xn2=xn1;
xn1=(a11*en1+a12*en2)-(b12*xn2);
xn1=(a11*en1+a12*en2)-(b12*xn2);

K=1;


for iter=1:iterations
```

```
   if (iter>3)
      Iout=0.286;                                                    %Average
output current
      Vout=700;                                                      %Output
regulation voltage
      Rout=Vout/Iout;                                                %Equivalent
output resistance (do not change)
   end



% ********** STATE 1 ********** -30~30
state=1
ip=ic(tc-1);
in=ib(tc-1);
it=ia(tc-1);


while (Vc>Va)

   if (K==(fsw/fsample))
         E=E1+E2;
         EN=E2;
         Iout=E/Rout;
         Vo=E/Divider;
         e4=e3;
         e3=e2;
         e2=e1;
         e1=2.5-Vo;
         x4=x3;
         x3=x2;
         x2=x1;
         x1=A*(e1*a1+e2*a2+e3*a3+e4*a4)-(x2*b2+x3*b3+x4*b4);
         VM=2.5+x1;
         if (VM>proc_V)
            VM=proc_V;
         elseif (VM<0)
            VM=0;
         end


         ip_s=2*ip*Rs+in*Rs;
         in_s=-2*in*Rs-ip*Rs;

         ep2=ep1;
         ep1=ip_s;
         xp3=xp2;
         xp2=xp1;
         xp1=(a11*ep1+a12*ep2)-(b12*xp2);

         en2=en1;
         en1=in_s;
         xn3=xn2;
         xn2=xn1;
         xn1=(a11*en1+a12*en2)-(b12*xn2);

         ip_s=xp1;
         in_s=xn1;

         if (ip_s>proc_V)
            ip_s=proc_V;
         elseif (ip_s<0)
            ip_s=0;
         end
         if (in_s>proc_V)
            in_s=proc_V;
         elseif (in_s<0)
            in_s=0;
         end

         K=1;
         t;
         %ip_s=2*ip*Rs+in*Rs;
         %in_s=-2*in*Rs-ip*Rs;

      else
         K=K+1;
      end
```

```
    for interval=1:resolution
    t=t+(1/(fsw*resolution));
    VM_int=VM*(1-interval/resolution);
    Va=Vamp*cos(t*fl*2*3.14159-0.66667*3.14159);
    Vc=Vamp*cos(t*fl*2*3.14159);
    Vb=Vamp*cos(t*fl*2*3.14159+0.66667*3.14159);
    VP=Vc;
    VN=Vb;
    VT=Va;

    Lp=Lc;
    Lt=La;
    Ln=Lb;

    if ((ip_s)<VM_int)
       if ((in_s)<VM_int)
          VPN=0;
          VTN=0;
          VNN=0;
          VP0=VPN-(VPN+VTN+VNN)/3;
          VT0=VTN-(VPN+VTN+VNN)/3;
          VN0=VNN-(VPN+VTN+VNN)/3;
          ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
          in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
          it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
          E1=E1-(1/(fsw*resolution))*Iout/C1;
          E2=E2-(1/(fsw*resolution))*Iout/C2;
       else
          VPN=0;
          VTN=0;
          VNN=-E2;
          VP0=VPN-(VPN+VTN+VNN)/3;
          VT0=VTN-(VPN+VTN+VNN)/3;
          VN0=VNN-(VPN+VTN+VNN)/3;
          ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
          in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
          it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
          E1=E1-(1/(fsw*resolution))*Iout/C1;
          E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
       end
    else
       if ((in_s)<VM_int)
          VPN=E1;
          VTN=0;
          VNN=0;
          VP0=VPN-(VPN+VTN+VNN)/3;
          VT0=VTN-(VPN+VTN+VNN)/3;
          VN0=VNN-(VPN+VTN+VNN)/3;
          ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
          in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
          it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
          E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
          E2=E2-(1/(fsw*resolution))*Iout/C2;
       else
          VPN=E1;
          VTN=0;
          VNN=-E2;
          VP0=VPN-(VPN+VTN+VNN)/3;
          VT0=VTN-(VPN+VTN+VNN)/3;
          VN0=VNN-(VPN+VTN+VNN)/3;
          ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
          in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
          it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
          E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
          E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
       end
    end
end
    ic(tc)=ip;
    ib(tc)=in;
    ia(tc)=-ip-in;
    c_control(tc)=ip_s;
    E_out(tc)=E1+E2;
    EN_out(tc)=E2;
    Vph_a(tc)=Va;
    Vph_c(tc)=Vc;
    Vph_b(tc)=Vb;
    time(tc)=t;
```

```
      tc=tc+1;
end                                                %END of STATE 1 simulation


% ********** STATE 2 ********** 30~90
state=2
while (Vc>Vb)

      if (K==(fsw/fsample))
         E=E1+E2;
         EN=E2;
         Iout=E/Rout;
         Vo=E/Divider;
         e4=e3;
         e3=e2;
         e2=e1;
         e1=2.5-Vo;
         x4=x3;
         x3=x2;
         x2=x1;
         x1=A*(e1*a1+e2*a2+e3*a3)-(x2*b2+x3*b3);
         VM=2.5+x1;
         if (VM>proc_V)
            VM=proc_V;
         elseif (VM<0)
            VM=0;
         end


         ip_s=2*ip*Rs+in*Rs;
         in_s=-2*in*Rs-ip*Rs;

         ep2=ep1;
         ep1=ip_s;
         xp3=xp2;
         xp2=xp1;
         xp1=(a11*ep1+a12*ep2)-(b12*xp2);

         en2=en1;
         en1=in_s;
         xn3=xn2;
         xn2=xn1;
         xn1=(a11*en1+a12*en2)-(b12*xn2);

         ip_s=xp1;
         in_s=xn1;

         if (ip_s>proc_V)
            ip_s=proc_V;
         elseif (ip_s<0)
            ip_s=0;
         end
         if (in_s>proc_V)
            in_s=proc_V;
         elseif (in_s<0)
            in_s=0;
         end

         K=1;
         %ip_s=2*ip*Rs+in*Rs;
         %in_s=-2*in*Rs-ip*Rs;
      else
         K=K+1;
      end

      for interval=1:resolution
      t=t+(1/(fsw*resolution));
      VM_int=VM*(1-interval/resolution);

      Va=Vamp*cos(t*fl*2*3.14159-0.66667*3.14159);
      Vc=Vamp*cos(t*fl*2*3.14159);
      Vb=Vamp*cos(t*fl*2*3.14159+0.66667*3.14159);
      VP=Va;
      VN=Vb;
      VT=Vc;

      Lp=La;
      Lt=Lc;
```

```
      Ln=Lb;

      if ((ip_s)<VM_int)
         if ((in_s)<VM_int)
            VPN=0;
            VTN=0;
            VNN=0;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*Iout/C1;
            E2=E2-(1/(fsw*resolution))*Iout/C2;
         else             VPN=0;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*Iout/C1;
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
         end
      else
         if ((in_s)<VM_int)
            VPN=E1;
            VTN=0;
            VNN=0;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*Iout/C2;
         else
            VPN=E1;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
         end
      end

end
      ic(tc)=-ip-in;
      ib(tc)=in;
      ia(tc)=ip;
      c_control(tc)=ip_s;
      E_out(tc)=E1+E2;
      EN_out(tc)=E2;
      Vph_a(tc)=Va;
      Vph_c(tc)=Vc;
      Vph_b(tc)=Vb;
      time(tc)=t;
      tc=tc+1;

end                                                  %END of STATE 2 simulation



% ********** STATE 3 ********** 90~150
state=3
while (Va>Vb)

      if (K==(fsw/fsample))
         E=E1+E2;
```

```
        EN=E2;
        Iout=E/Rout;
        Vo=E/Divider;          e4=e3;
        e3=e2;
        e2=e1;
        e1=2.5-Vo;
        x4=x3;
        x3=x2;
        x2=x1;
        x1=A*(e1*a1+e2*a2+e3*a3)-(x2*b2+x3*b3);
        VM=2.5+x1;
        if (VM>proc_V)             VM=proc_V;
        elseif (VM<0)
           VM=0;
        end


        ip_s=2*ip*Rs+in*Rs;
        in_s=-2*in*Rs-ip*Rs;

        ep2=ep1;
        ep1=ip_s;
        xp3=xp2;
        xp2=xp1;
        xp1=(a11*ep1+a12*ep2)-(b12*xp2);

        en2=en1;
        en1=in_s;
        xn3=xn2;
        xn2=xn1;
        xn1=(a11*en1+a12*en2)-(b12*xn2);

        ip_s=xp1;
        in_s=xn1;

        if (ip_s>proc_V)
           ip_s=proc_V;
        elseif (ip_s<0)
           ip_s=0;
        end
        if (in_s>proc_V)
           in_s=proc_V;
        elseif (in_s<0)
           in_s=0;
        end

        K=1;
        %ip_s=2*ip*Rs+in*Rs;
        %in_s=-2*in*Rs-ip*Rs;
    else          K=K+1;
    end

    for interval=1:resolution
    t=t+(1/(fsw*resolution));
    VM_int=VM*(1-interval/resolution);

    Va=Vamp*cos(t*fl*2*3.14159-0.66667*3.14159);
    Vc=Vamp*cos(t*fl*2*3.14159);
    Vb=Vamp*cos(t*fl*2*3.14159+0.66667*3.14159);
    VP=Va;
    VN=Vc;
    VT=Vb;

    Lp=La;
    Lt=Lb;
    Ln=Lc;

    if ((ip_s)<VM_int)
        if ((in_s)<VM_int)
           VPN=0;
           VTN=0;
           VNN=0;
           VP0=VPN-(VPN+VTN+VNN)/3;
           VT0=VTN-(VPN+VTN+VNN)/3;
           VN0=VNN-(VPN+VTN+VNN)/3;
           ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
           in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
           it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
           E1=E1-(1/(fsw*resolution))*Iout/C1;
```

```
            E2=E2-(1/(fsw*resolution))*Iout/C2;
         else
            VPN=0;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*Iout/C1;
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
         end
      else
         if ((in_s)<VM_int)
            VPN=E1;
            VTN=0;
            VNN=0;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*Iout/C2;
         else
            VPN=E1;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
         end
      end

end
      ic(tc)=in;
      ib(tc)=-ip-in;
      ia(tc)=ip;
      c_control(tc)=ip_s;
      E_out(tc)=E1+E2;
      EN_out(tc)=E2;
      Vph_a(tc)=Va;
      Vph_c(tc)=Vc;
      Vph_b(tc)=Vb;
      time(tc)=t;
      tc=tc+1;

end                                                    %END of STATE 3 simulation


% ********** STATE 4 ********** 150~210
state=4
while (Va>Vc)

      if (K==(fsw/fsample))
         E=E1+E2;
         EN=E2;
         Iout=E/Rout;
         Vo=E/Divider;
         e4=e3;
         e3=e2;
         e2=e1;
         e1=2.5-Vo;
         x4=x3;
         x3=x2;
         x2=x1;
         x1=A*(e1*a1+e2*a2+e3*a3)-(x2*b2+x3*b3);
         VM=2.5+x1;
         if (VM>proc_V)
            VM=proc_V;
         elseif (VM<0)             VM=0;
```

```
        end


        ip_s=2*ip*Rs+in*Rs;
        in_s=-2*in*Rs-ip*Rs;

        ep2=ep1;
        ep1=ip_s;
        xp3=xp2;
        xp2=xp1;
        xp1=(a11*ep1+a12*ep2)-(b12*xp2);

        en2=en1;
        en1=in_s;
        xn3=xn2;
        xn2=xn1;
        xn1=(a11*en1+a12*en2)-(b12*xn2);

        ip_s=xp1;
        in_s=xn1;

        if (ip_s>proc_V)
           ip_s=proc_V;
        elseif (ip_s<0)
           ip_s=0;
        end
        if (in_s>proc_V)
           in_s=proc_V;
        elseif (in_s<0)
           in_s=0;
        end

        K=1;
        %ip_s=2*ip*Rs+in*Rs;
        %in_s=-2*in*Rs-ip*Rs;
    else
        K=K+1;
    end


    for interval=1:resolution
    t=t+(1/(fsw*resolution));
    VM_int=VM*(1-interval/resolution);

    Va=Vamp*cos(t*fl*2*3.14159-0.66667*3.14159);
    Vc=Vamp*cos(t*fl*2*3.14159);
    Vb=Vamp*cos(t*fl*2*3.14159+0.66667*3.14159);
    VP=Vb;
    VN=Vc;
    VT=Va;

    Lp=Lb;
    Lt=La;
    Ln=Lc;

    if ((ip_s)<VM_int)
        if ((in_s)<VM_int)
            VPN=0;
            VTN=0;
            VNN=0;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*Iout/C1;
            E2=E2-(1/(fsw*resolution))*Iout/C2;
        else
            VPN=0;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*Iout/C1;
```

```
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
         end
      else
         if ((in_s)<VM_int)
            VPN=E1;
            VTN=0;
            VNN=0;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;                    E1=E1-
(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*Iout/C2;
         else
            VPN=E1;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
         end
      end

end
      ic(tc)=in;
      ib(tc)=ip;
      ia(tc)=-ip-in;
      c_control(tc)=ip_s;
      E_out(tc)=E1+E2;
      EN_out(tc)=E2;
      Vph_a(tc)=Va;
      Vph_c(tc)=Vc;
      Vph_b(tc)=Vb;
      time(tc)=t;
      tc=tc+1;

end                                                %END of STATE 4 simulation


% ********** STATE 5 ********** 210~270
state=5
while (Vb>Vc)

      if (K==(fsw/fsample))
         E=E1+E2;
         EN=E2;
         Iout=E/Rout;
         Vo=E/Divider;          e4=e3;
         e3=e2;
         e2=e1;
         e1=2.5-Vo;
         x4=x3;
         x3=x2;
         x2=x1;
         x1=A*(e1*a1+e2*a2+e3*a3)-(x2*b2+x3*b3);
         VM=2.5+x1;
         if (VM>proc_V)
            VM=proc_V;
         elseif (VM<0)
            VM=0;
         end


         ip_s=2*ip*Rs+in*Rs;
         in_s=-2*in*Rs-ip*Rs;

         ep2=ep1;
         ep1=ip_s;
         xp3=xp2;
         xp2=xp1;
         xp1=(a11*ep1+a12*ep2)-(b12*xp2);
```

```
   en2=en1;
   en1=in_s;
   xn3=xn2;
   xn2=xn1;
   xn1=(a11*en1+a12*en2)-(b12*xn2);

   ip_s=xp1;
   in_s=xn1;

   if (ip_s>proc_V)
      ip_s=proc_V;
   elseif (ip_s<0)
      ip_s=0;
   end
   if (in_s>proc_V)
      in_s=proc_V;
   elseif (in_s<0)
      in_s=0;
   end

   K=1;
   %ip_s=2*ip*Rs+in*Rs;
   %in_s=-2*in*Rs-ip*Rs;
else
   K=K+1;
end


for interval=1:resolution
t=t+(1/(fsw*resolution));
VM_int=VM*(1-interval/resolution);

Va=Vamp*cos(t*fl*2*3.14159-0.66667*3.14159);
Vc=Vamp*cos(t*fl*2*3.14159);
Vb=Vamp*cos(t*fl*2*3.14159+0.66667*3.14159);
VP=Vb;
VN=Va;
VT=Vc;

Lp=Lb;
Lt=Lc;
Ln=La;

if ((ip_s)<VM_int)
   if ((in_s)<VM_int)
      VPN=0;
      VTN=0;
      VNN=0;
      VP0=VPN-(VPN+VTN+VNN)/3;
      VT0=VTN-(VPN+VTN+VNN)/3;
      VN0=VNN-(VPN+VTN+VNN)/3;
      ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
      in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
      it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
      E1=E1-(1/(fsw*resolution))*Iout/C1;
      E2=E2-(1/(fsw*resolution))*Iout/C2;
   else
      VPN=0;
      VTN=0;
      VNN=-E2;
      VP0=VPN-(VPN+VTN+VNN)/3;
      VT0=VTN-(VPN+VTN+VNN)/3;
      VN0=VNN-(VPN+VTN+VNN)/3;
      ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
      in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
      it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
      E1=E1-(1/(fsw*resolution))*Iout/C1;
      E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
   end
else
   if ((in_s)<VM_int)
      VPN=E1;
      VTN=0;
      VNN=0;
      VP0=VPN-(VPN+VTN+VNN)/3;
      VT0=VTN-(VPN+VTN+VNN)/3;
      VN0=VNN-(VPN+VTN+VNN)/3;
      ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
```

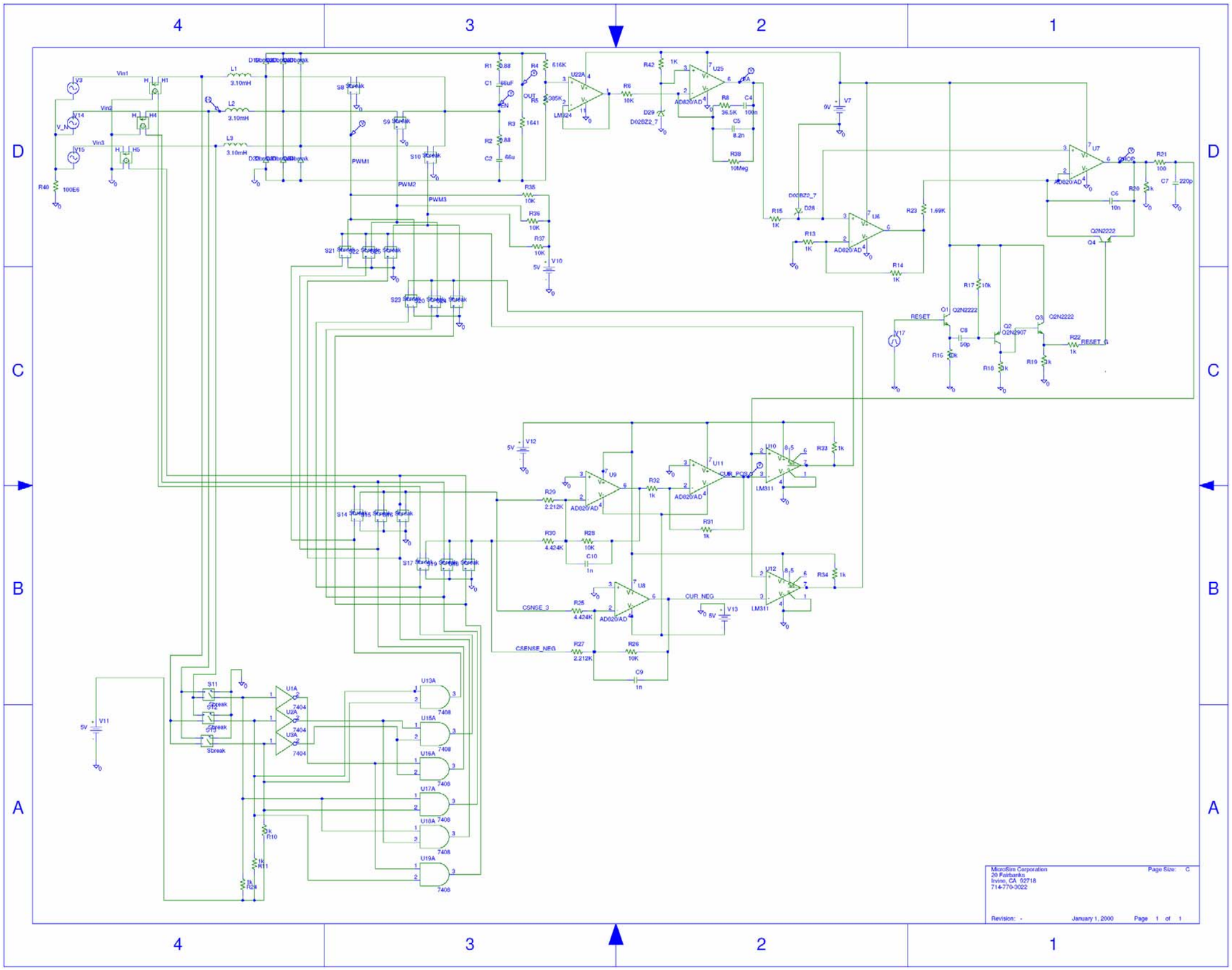
```
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*Iout/C2;
         else
            VPN=E1;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
         end
      end
end
      ic(tc)=-ip-in;
      ib(tc)=ip;
      ia(tc)=in;
      c_control(tc)=ip_s;
      E_out(tc)=E1+E2;
      EN_out(tc)=E2;
      Vph_a(tc)=Va;
      Vph_c(tc)=Vc;
      Vph_b(tc)=Vb;
      time(tc)=t;
      tc=tc+1;

end                                                    %END of STATE 5 simulation



% ********** STATE 6 ********** 270~330
state=6
while (Vb>Va)

      if (K==(fsw/fsample))
         E=E1+E2;
         EN=E2;
         Iout=E/Rout;
         Vo=E/Divider;
         e4=e3;
         e3=e2;
         e2=e1;
         e1=2.5-Vo;
         x4=x3;
         x3=x2;
         x2=x1;
         x1=A*(e1*a1+e2*a2+e3*a3)-(x2*b2+x3*b3);
         VM=2.5+x1;
         if (VM>proc_V)
            VM=proc_V;
         elseif (VM<0)
            VM=0;
         end


         ip_s=2*ip*Rs+in*Rs;
         in_s=-2*in*Rs-ip*Rs;

         ep2=ep1;
         ep1=ip_s;
         xp3=xp2;
         xp2=xp1;
         xp1=(a11*ep1+a12*ep2)-(b12*xp2);

         en2=en1;
         en1=in_s;
         xn3=xn2;
         xn2=xn1;
         xn1=(a11*en1+a12*en2)-(b12*xn2);

         ip_s=xp1;
         in_s=xn1;
```

```
        if (ip_s>proc_V)
           ip_s=proc_V;
        elseif (ip_s<0)
           ip_s=0;
        end
        if (in_s>proc_V)
           in_s=proc_V;
        elseif (in_s<0)
           in_s=0;
        end

        K=1;
        %ip_s=2*ip*Rs+in*Rs;
        %in_s=-2*in*Rs-ip*Rs;
    else
        K=K+1;
    end


    for interval=1:resolution
    t=t+(1/(fsw*resolution));
    VM_int=VM*(1-interval/resolution);

    Va=Vamp*cos(t*fl*2*3.14159-0.66667*3.14159);
    Vc=Vamp*cos(t*fl*2*3.14159);
    Vb=Vamp*cos(t*fl*2*3.14159+0.66667*3.14159);
    VP=Vc;
    VN=Va;
    VT=Vb;

    Lp=Lc;
    Lt=Lb;
    Ln=La;

    if ((ip_s)<VM_int)
        if ((in_s)<VM_int)
            VPN=0;
            VTN=0;
            VNN=0;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*Iout/C1;
            E2=E2-(1/(fsw*resolution))*Iout/C2;
        else
            VPN=0;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*Iout/C1;
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
        end
    else
        if ((in_s)<VM_int)
            VPN=E1;
            VTN=0;
            VNN=0;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*Iout/C2;
        else
            VPN=E1;
            VTN=0;
            VNN=-E2;
            VP0=VPN-(VPN+VTN+VNN)/3;
            VT0=VTN-(VPN+VTN+VNN)/3;
```

```
            VN0=VNN-(VPN+VTN+VNN)/3;
            ip=ip+(1/(fsw*resolution))*(VP-VP0)/Lp;
            in=in+(1/(fsw*resolution))*(VN-VN0)/Ln;
            it=it+(1/(fsw*resolution))*(VT-VT0)/Lt;
            E1=E1-(1/(fsw*resolution))*(Iout-ip)/C1;
            E2=E2-(1/(fsw*resolution))*(Iout+in)/C2;
         end
      end
   end
      ic(tc)=ip;
      ib(tc)=-ip-in;
      ia(tc)=in;
      c_control(tc)=ip_s;
      E_out(tc)=E1+E2;
      EN_out(tc)=E2;
      Vph_a(tc)=Va;
      Vph_c(tc)=Vc;
      Vph_b(tc)=Vb;
      time(tc)=t;
      tc=tc+1;

end                                                %END of STATE 6 simulation


end   %end number of iterations

ic(tc)=ic(tc-1);
ib(tc)=ib(tc-1);
ia(tc)=ia(tc-1);
c_control(tc)=c_control(tc-1);
time(tc)=time(tc-1);

E_out(tc)=E_out(tc-1);
EN_out(tc)=EN_out(tc-1);

Vph_a(tc)=Vph_a(tc-1);
Vph_c(tc)=Vph_c(tc-1);
Vph_b(tc)=Vph_b(tc-1);
finito=1
plot(time,ic);
```

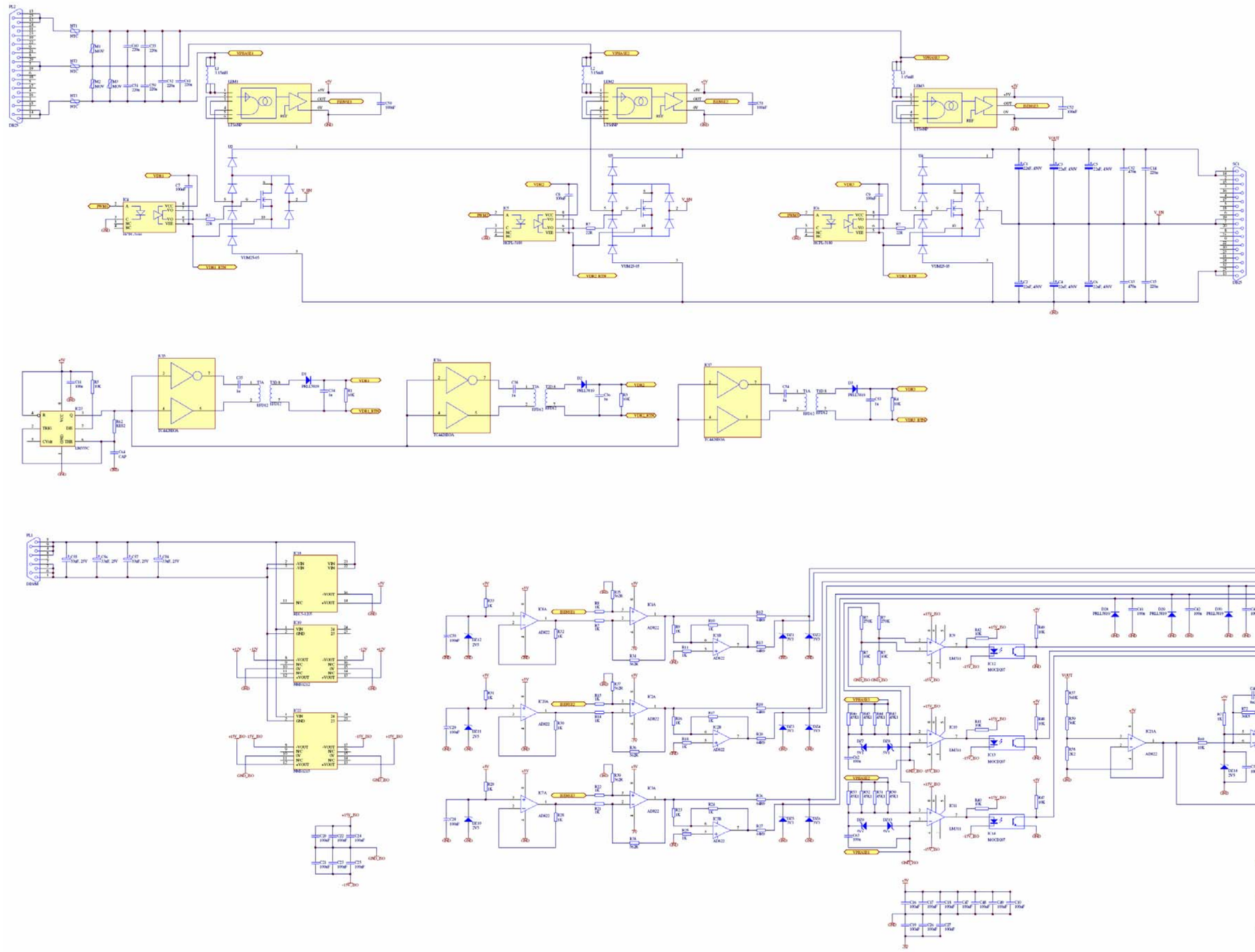
# APPENDIX E

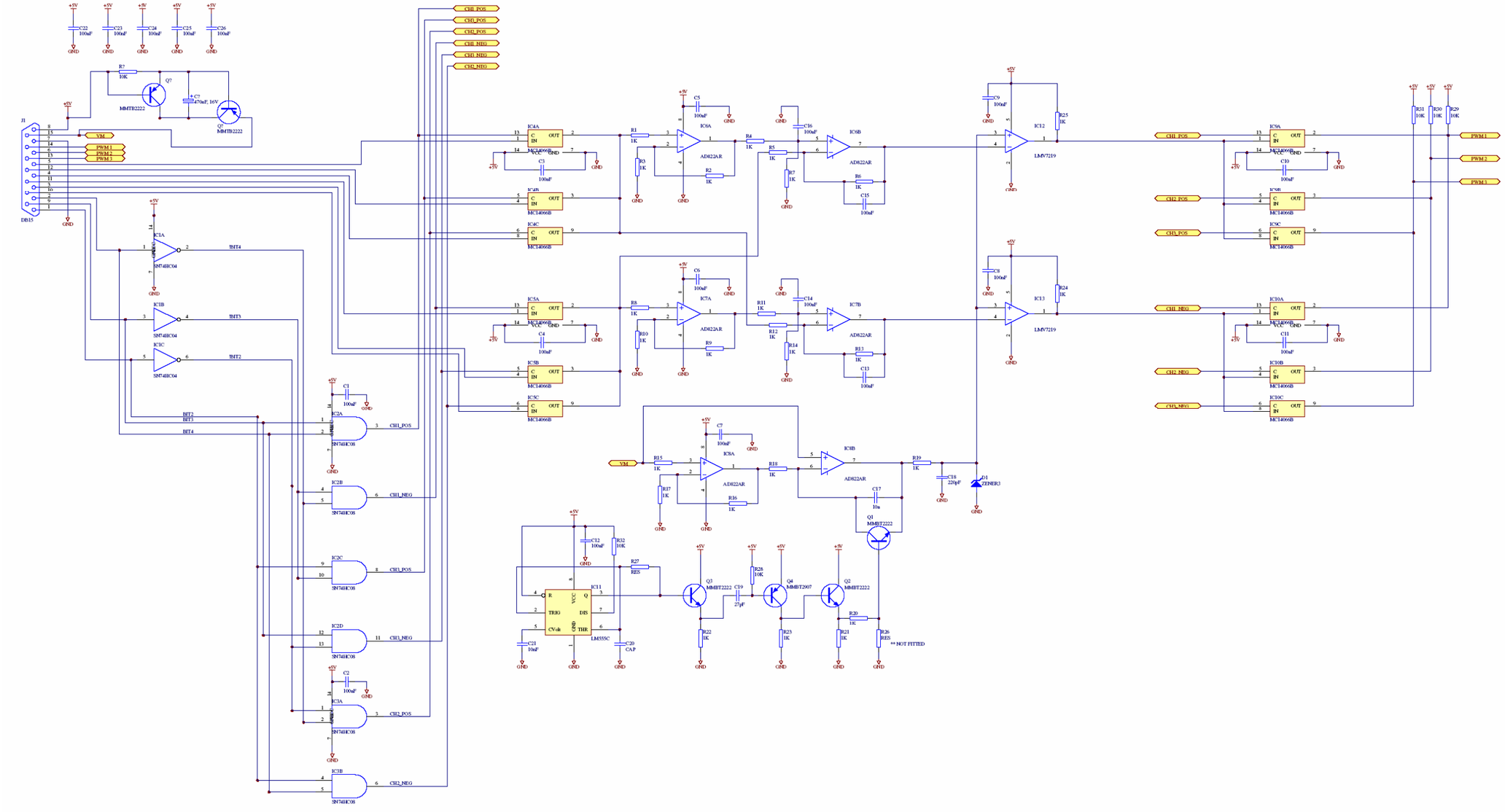
# PSPICE VIENNA RECTIFIER SIMULATION SCHEMATIC


4
3
2
1
D
C
B
A
Vin1
Vin2
Vin3
L1
3.10mH
L2
3.10mH
L3
3.10mH
R40
100E6
PWM1
PWM2
PWM3
R35
10K
R36
10K
R37
10K
5V
V10
R1
.88
C1
66uF
R2
.88
C2
66u
R3
1641
R4
616K
R5
385K
OUT
U22A
LM324
R6
10K
R42
1K
U25
AD820/AD
R8
36.5K
C4
100n
C5
8.2n
R38
10Meg
D29
D28
D15
D16
9V
V7
R15
1K
R13
1K
R14
1K
U6
R23
1.69K
U7
R21
100
C7
220p
R20
1k
C6
10n
Q2N2222
Q4
R17
10k
RESET
Q1
Q2N2222
C8
50p
R16
10k
Q2
Q2N2907
Q3
Q2N2222
R22
RESET_G
1k
R19
1k
R18
1k
V17
5V
V12
U9
R29
2.212K
R32
1k
U11
CUR_POS
U10
R33
1k
LM311
R31
1k
R30
4.424K
R28
10K
C10
1n
U12
R34
1k
CUR_NEG
V13
5V
U8
CSNSE_3
R25
4.424K
CSENSE_NEG
R27
2.212K
R26
10K
C9
1n
S11
S12
S13
Sbreak
5V
V11
U1A
U2A
U3A
7404
R10
1k
R11
1k
R24
1k
U13A
U15A
U16A
U17A
U18A
U19A
7408
7406
MicroSim Corporation
20 Fairbanks
Irvine, CA 92718
714-770-3022
Page Size: C
Revision: -
January 1, 2000
Page 1 of 1

# APPENDIX F

# VIENNA RECTIFIER PROTOTYPE SCHEMATICS




CH1_POS
CH1_POS
CH2_POS
CH1_NEG
CH1_NEG
CH2_NEG
+5V
C22 100nF
C23 100nF
C24 100nF
C25 100nF
C26 100nF
GND
R7 10K
Q7 MMBT2222
C7 470nF, 16V
Q7 MMBT2222
J1
DB15
VM
PWM 1
PWM 2
PWM 3
IC1A
IC1B
IC1C
SN74HC04
BIT4
BIT3
BIT2
BIT1
IC2A
IC2B
IC2C
IC2D
SN74HC08
CH1_POS
CH1_NEG
CH2_POS
CH2_NEG
C1 100nF
C2 100nF
IC3A
IC3B
IC4A
IC4B
IC4C
IC5A
IC5B
IC5C
MC14066B
C3 100nF
C4 100nF
R1 1K
R2 1K
R3 1K
R4 1K
R5 1K
R6 1K
R7 1K
R8 1K
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
C5 100nF
C6 100nF
C14 100nF
C15 100nF
C16 100nF
IC6A
IC6B
IC7A
IC7B
AD822AR
C9 100nF
IC12
IC13
LMV7219
R24 1K
R25 1K
IC8A
IC8B
R15 1K
R16 1K
R17 1K
R18 1K
R19 1K
C7 100nF
C17 10n
C18 220pF
D1 ZENER3
Q1 MMBT2222
C12 100nF
R32 10K
IC11
LM555C
R27 RES
C21 10nF
C20 CAP
Q3 MMBT2222
Q4 MMBT2907
Q2 MMBT2222
C19 27pF
R22 1K
R23 1K
R21 1K
R20 1K
R26 RES
** NOT FITTED
IC9A
IC9B
IC9C
IC10A
IC10B
IC10C
C10 100nF
C11 100nF
R31 10K
R30 10K
R29 10K

# PHOTOGRAPHS OF THE VIENNA RECTIFIER PROTOTYPE DURING LABORATORY TESTING

# APPENDIX G

# VIENNA RECTIFIER PROTOTYPE THERMAL ANALYSIS

All of the components used on the prototype rectifier (excluding the heatsink mounted components) have an upper ambient temperature specification of 70°C. It must therefore be ensured that the temperature does not exceed this limit. It can also be assumed that the environmental temperature (ambient) shall be no more than 25°C, since the experimental prototype will only be operated in a laboratory environment.

From [44] the thermal resistance of a heatsink is equal to:

$$R_{\theta,\,HS} = \frac{(T_S - T_A)}{P_{loss,\,components\_on\_HS}} = \frac{(T_S - T_A)}{P_{loss,\,switches} + P_{loss,\,diodes}}, \quad \text{G.1}$$

where $T_S$ is the heatsink temperature and $T_A$ the ambient temperature. Substituting (5.42) and (5.34) into (G.1) yields the required heatsink, in terms of thermal resistance:

$$R_{\theta,\,HS} = \frac{(70 - 25)}{77.59} = 0.58°C/W \quad \text{G.2}$$

The heatsink chosen is from Fischer Electronics and have a thermal resistance of 0.55°C/W, which is below the required resistance of 0.58°C/W.

For TO-220 packages (which all of the diodes and switches are) the thermal resistance for the junction-to-case is approximately $R_{\theta,JC}$ = 1.75°C/W and for the case-to-heatsink, which includes thermal grease and isolating material, approximately $R_{\theta,CS}$ = 1.75°C/W. For all the diodes and switches used the maximum allowable junction temperature is 175°C. The junction temperature for any of the switches or diodes can be computed as [44]:

$$T_{comp} = T_{HS} + (R_{\theta,\,JC} + R_{\theta,\,CS})P_{loss,\,comp} \quad \text{G.3}$$

For the switches the total power loss per switch is (6.912+2.48) = 9.39W (from (5.42)). Substituting the switch power loss into (G.3) yields the maximum junction temperature for the switches:

$$T_{j,\,sw} = 70 + (1.75 + 0.5) \times 9.39 = 91.1275°C \quad \text{G.4}$$

For diodes $D_1$ and $D_2$ (refer to figure 5.4) the power loss per diode is (1.5×1.41) = 2.1W. Substituting the diode power loss into (G.3) yields the maximum junction temperature for the diodes:

$$T_{j,D1} = 70 + (1.75 + 0.5) \times 2.1 = 74.725°C \quad \text{G.5}$$

For diodes $D_3$ and $D_5$ (refer to figure 5.4) the power loss per diode is (1.5×2.32) = 3.48W (from (5.34)). Substituting the diode power loss into (G.3) yields the maximum junction temperature for the diodes:

$$T_{j,D3} = 70 + (1.75 + 0.5) \times 3.48 = 77.83°C \quad \text{G.6}$$

For diodes $D_4$ and $D_6$ (refer to figure 5.4) the power loss per diode is (1.5×1.76) = 2.64W (from (5.34)). Substituting the diode power loss into (G.3) yields the maximum junction temperature for the diodes:

$$T_{j,D4} = 70 + (1.75 + 0.5) \times 2.64 = 75.94°C \quad \text{G.7}$$

From equations (G.4) to (G.7) it is observed that none of the semi-conductors mounted to the heatsink exceed their junction temperature of 175°C.