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A MULTI-DIMENSIONAL SPREAD SPECTRUM TRANSCEIVER

by

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SUMMARY

A MULTI-DIMENSIONAL SPREAD SPECTRUM TRANSCEIVER BY SAURABH SINHA

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The research conducted for this thesis seeks to understand issues associated with integrating a direct spread spectrum system (DSSS) transceiver on to a single chip. Various types of sequences, such as Kasami sequences and Gold sequences, are available for use in typical spread spectrum systems. For this thesis, complex spreading sequences (CSS) are used for improved cross-correlation and autocorrelation properties that can be achieved by using such a sequence.

While CSS and DSSS are well represented in the existing body of knowledge, and discrete bulky hardware solutions exist – an effort to jointly integrate CSS and DSSS on-chip was identified to be lacking. For this thesis, spread spectrum architecture was implemented focussing on sub-systems that are specific to CSS. This will be the main contribution for this thesis, but the contribution is further appended by various RF design challenges: high-speed requirements make RF circuits sensitive to the effects of parasitics, including parasitic inductance, passive component modelling, as well as signal integrity issues.

The integration is first considered more ideally, using mathematical sub-systems, and then later implemented practically using complementary metal-oxide semiconductor (CMOS) technology. The integration involves mixed-signal and radio frequency (RF) design techniques – and final integration involves several specialized analogue sub-systems, such as a class F power amplifier (PA), a low-noise amplifier (LNA), and LC voltage-controlled oscillators (VCOs). The research also considers various issues related to on-chip inductors, and also considers an active inductor implementation as an option for the VCO. With such an inductor a better quality factor is achievable. While some conventional sub-system design techniques are deployed, several modifications are made to adapt a given sub-system to the design requirements for this thesis. The contribution of the research lies in the circuit level modifications done at sub-system level aimed towards eventual integration. For multiple-access communication systems, where a number of independent users are required to share a common channel, the transceiver proposed in this thesis, can contribute towards improved data rate or bit error rate.

The design is completed for fabrication in a standard 0.35-µm CMOS process with minimal external components. With an active chip area of about 5 mm^2, the simulated transmitter consumes about 250 mW & the receiver consumes about 200 mW.

Keywords: complementary metal-oxide semiconductor (CMOS), spread spectrum (SS), complex spreading sequences (CSS), delay locked loop (DLL), Costa's loop, voltage controlled oscillator (VCO), mixer, on-chip inductors, class F power amplifier (PA).

SAMEVATTING

'N MULTIDIMENSIONELE SPREISPEKTRUM-SENDER-ONTVANGER DEUR SAURABH SINHA

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Die navorsing wat vir hierdie tesis onderneem is, beoog om kundigheid op te bou aangaande die kwessies wat met die integrasie van 'n direkte spreispektrumstelsel (DSSS) sender-ontvanger op 'n enkele skyfie verband hou. Verskeie tipes sekwensies, soos byvoorbeeld Kasami- en Gold-sekwensies, is vir gebruik in tipiese spreispektrumstelsels beskikbaar. Vir hierdie tesis is komplekse spreisekwensies (KSS) gebruik vir verbeterde kruis- en outokorrelasie-eienskappe wat bereik kan word deur so 'n sekwensie te gebruik.

Alhoewel DSSS en KSS reeds welbekend is, en diskrete hardeware oplossings reeds bestaan, is die vraag na gesamentlike geïntegreerde DSSS en KSS op een vlokkie geïdentifiseer. Vir hierdie tesis is spreispektrumargitektuur aangewend met die klem op KSS substelsels. Dit is dan ook die belangrikste bydrae van hierdie tesis, maar die bydrae gaan verder gepaard met verskeie RF-ontwerpuitdagings: hoëspoed-vereistes maak RF-stroombane sensitief vir die uitwerking van parasitiese komponente, met inbegrip van parasitiese induktansie, passiewe komponentmodellering en ook seinintegriteitskwessies.

Die integrasie word eerstens meer idealisties oorweeg deur wiskundige substelsels te gebruik en dan later prakties te implementeer deur komplementêre metaaloksied-halfgeleiertegnologie (CMOS) te gebruik. Die integrasie behels gemengdesein- en radiofrekwensie(RF)-ontwerptegnieke – en finale integrasie behels verskeie gespesialiseerde analoë substelsels soos 'n klas F-kragversterker (KV), 'n laeruis-versterker (LRV), en LC-spanningbeheerde ossileerders (SBO's). Die navorsing oorweeg ook verskeie kwessies in verband met op-skyfie induktors en oorweeg ook 'n aktiewe induktorimplementering as 'n opsie vir die SBO. Met sodanige induktor is 'n beter kwaliteitsfaktor haalbaar. Hoewel enkele konvensionele substelsel-ontwerptegnieke aangewend word, word daar verskeie wysigings aangebring om 'n gegewe substelsel by die ontwerpvereistes vir hierdie tesis aan te pas. Die bydrae van die navorsing is hoofsaaklik die stroombaanmodifikasies wat gedoen is op substelselvlak om integrasie te vergemaklik. Vir veelvoudige-toegang kommunikasiestelsels waar 'n aantal onafhanklike

gebruikers dieselfde seinkanaal moet deel, kan die sender-ontvanger voorgestel in hierdie tesis meewerk om die datatempo en fouttempo te verbeter.

Die ontwerp is voltooi vir vervaardiging in ‘n standaard 0.35-µm CMOS-proses met minimale eksterne komponente. Met ‘n aktiewe skyfie-oppervlakte van ongeveer 5 mm^2, verbruik die gesimuleerde sender ongeveer 250 mW en die ontvanger verbruik ongeveer 200 mW.

Sleutelwoorde: komplementêre metaaloksied-halfgeleier (CMOS), spreispektrum (SS), komplekse spreisekwenssies (KSS), vertragingsluitlus (VSL), Costa se lus, spanningsbeheerde ossilleerder (SBO), menger, op-skyfie induktors, klas F-kragversterker (KV).

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The research work of this thesis would not be possible without the kind co-operation and support of many friends, students, and colleagues. I would like to acknowledge and extend my appreciation to all those that have contributed indirectly or directly to the research conducted in this thesis. The following names are worthy of a special mention:

- Prof. Monuko du Plessis for his technical guidance as the research supervisor,
- Prof. Louis Linde for his initiative towards the broader area of research, and serving as the research co-supervisor, and
- Prof. Wilhelm Leuschner for allowing me time (as my boss) to conduct this research.

I would also like to acknowledge the excellent resources (human and financial) provided by the Carl & Emily Fuchs Institute for Microelectronics (CEFIM), University of Pretoria. During the course of this thesis, I have also had the opportunity to serve on several IEEE committees (both at the level of Region 8 and the South Africa Section). Due to the time required for this thesis, I reduced the time that I normally spent as a volunteer, yet received immense support from some IEEE volunteers in our Section, some names that come to thought: Prof. Gerhard Hancke, Prof. Nico Beute, Prof. Tinus Pretorius, Dr Edward Chikuni, and Jacques van Wyk.

I would also like to extend a very special thanks to my RFIC microelectronics research group whose work also contributed to my own academic development; in particular I would like to thank Mladen Božanić, Calvin Coetzee, Simon Ross, Neil Naudé, John Meyer, and Tinu Elenjical.

I would also like to extend my gratitude to my parents (Pramod & Sudha Sinha) and friends for their kind support and understanding as this thesis was concluded. In particular, I would like to acknowledge my close friends, Jaco du Preez and Rina Mostert & colleagues, Jannes Venter, Johan Schoeman, Maryna Bekker, Marí Ferreira, Tilla Loubser, and Prof. Johan Hanekom.

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LIST OF ABBREVIATIONS

AC	Auto-correlation
AMS	austriamicrosystems
BER	Bit error rate
BERT	Bit error ratio test
BJT	Bipolar junction transistor
BPF	Band-pass filter
BPSK	Binary phase-shift keying
BTS	Base transceiver station
BUF	Buffer
CC	Cross-correlation
CDLL	Complex delay lock loop
CDMA	Code division multiple access
CEFIM	Carl and Emily Fuchs Institute for Microelectronics
CLK	Clock
CMOS	Complementary metal-oxide semiconductor
CMRR	Common-mode rejection ratio
CSS	Complex spreading sequences
DA	Differential amplifier
DDC-CRL	Decision directed Costas carrier recovery loop
DRC	Design rule check
DSSS	Direct sequence spread spectrum
FET	Field-effect transistor
FF	Flip-flop
FHSS	Frequency hopping spread spectrum
FM	Frequency modulation
FPGA	Field programmable graphics array
FU	Functional Unit
GCL	Generalized chirp-like
IF	Interface
IR	Infrared
LNA	Low-noise amplifier

LO	Local oscillator
LPF	Low pass filter
LPI	Low probability of intercept
LVS	Layout versus Schematic
MN	Matching network
MS	Mobile station
MTLL	Mean time to lose lock
MUI	Multi-user interference
NDA	Non-disclosure agreement
NF	Noise figure
NIC	Negative impedance converter
NRZ	Non-return-to-zero
P/S	Parallel-to-Serial
PA	Power amplifier
PCB	Printed circuit board
PCM	Pulse code modulation
PD	Phase detector
PN	Pseudonoise
PRBS	Pseudo random binary sequence
PSD	Power spectral density
QPSK	Quadrature phase-shift keying
RMS	Root-mean square
RUF	Root-of-unity filtered
S/P	Serial-to-parallel
SNR	Signal-to-noise ratio
SPICE	Simulation program with integrated circuit emphasis
VCO	Voltage controlled oscillator
VLSI	Very large-scale integration

CHAPTER 1: INTRODUCTION

1.1 Background to the research

Communication system engineers are often concerned with efficiency with which systems utilize signal energy and bandwidth. In most communication systems these are essential issues. However, in some cases, there exist situations in which it is necessary for the system to resist external interference, to operate at low spectral energy, to provide multiple access capability without external control, and to provide a secure channel inaccessible to outside listeners [1]. Thus, it is sometimes necessary to trade-off efficiency of a system for such enhanced features. Communication systems deploy spread spectrum techniques to achieve such features [2].

The theoretical aspects of using spread spectrum in a strong interference environment have been known for over four decades. It is only over the last decade that practical implementations became more feasible. Initially, spread spectrum techniques were developed for military purposes [3] and their implementations were exceedingly expensive. Technological advancements such as VLSI, and advanced signal processing techniques made it possible to develop cheaper spread spectrum equipment for general public use [4]. Applications of this technology include mobile phones, wireless data transmission and satellite communications [5].

Spread-spectrum systems adhere to two criteria [2]:
1. the bandwidth of the transmitted signal must be greater than the transmitted signal, and
2. transmitted bandwidth must be determined by some function that is independent of the message and is known to the receiver.

Bandwidth expansion in spread spectrum systems is achieved by using a function that is independent of the message. Spread spectrum techniques have other features that make it unique and useful. These features include [4]:

- anti-jam capability-particularly for narrow-band jamming,
- interference rejection,
- multiple-access capability,
- multi-path protection,

- covert operation or low probability of intercept (LPI),
- secure communications,
- improved spectral efficiency-in special circumstances, and
- ranging.

One of the methods of classifying spread spectrum techniques that will be used throughout this thesis is by modulation. Some of the modulation techniques employed in spread spectrum techniques include [3]:

- direct sequence spread spectrum (DSSS),
- frequency hopping spread spectrum (FHSS),
- time hopping,
- chirp, and
- hybrid methods.

Spread spectrum techniques can be used to transmit both analogue and digital data signals using an analogue signal. Essentially, a higher frequency PN sequence is used to spread an information signal over a wider bandwidth, thereby making jamming and interception of the signal more difficult as only small portions of the signal can be blocked out. Various spread spectrum techniques have been developed, as listed above; the two most popular types will be discussed in some more detail: FHSS and DSSS. In FHSS the information signal is transmitted over a series of frequencies seemingly randomly (hopping). The receiver hops between frequencies in synchronisation with the transmitter. This allows the transmitted signal to be recovered. DSSS, as used in this thesis and explained later, is a more recent development. A third, hybrid type of spread spectrum, which combines the advantages of FHSS and DSSS techniques while reducing their shortcomings - for instance, the need for power control in DSSS systems, or the probability that a FHSS system will transmit at a frequency that happens to have high interference - has also been developed. In this technique, each data bit in the message signal is spread individually using a PN sequence while the channel hops between frequencies [6].

Table 1 serves as a comparison between the two main types of spread spectrum.

DSSS	FHSS
Higher performance, data rate, and larger packets.	Lower cost, better for lower data rates, and more burst data.
Broadband continuous transmission.	Narrowband at any instant, discontinuous transmission.
More complex, more efficient PSK modulation.	Simple, less efficient FSK modulation.
Traditionally use linear power amplifiers, making it less power efficient.	Can use nonlinear power amplifiers, thus achieving higher power efficiency.
Quicker synchronization.	Requires guard band, longer sync time.
Requires less efficient linear amplifier.	Requires a more efficient nonlinear amplifier.
Near-far effect[1] is dominant, this can be reduced by employing power control in cellular systems.	Near-far effect has less influence as users are not always in the same frequency slot.
Avoids interference by spreading energy across band.	Avoids interfering source by hopping around it.

Table 1.

Comparison of DSSS techniques with FHSS techniques [6, 7].

The following excerpt [8] is an important basis for this thesis:

> "This invention relates to a multi-dimensional, DSSS communication system and method.
>
> In a DSSS system, the spectrum spreading is accomplished before transmission through the use of a spreading sequence that is independent of the data signal. The same spreading sequence is used in the receiver (operating in synchronism with the transmitter) to despread the received signal, so that the original data may be recovered.
>
> In some multiple-access communication systems, a number of independent users are required to share a common channel. It is known to use bipolar phase shift keying spread spectrum (BPSK-SS) or quadrature phase shift keying spread spectrum (QPSK-SS) modems in such systems. However, the data rate or bit error rate (BER) of these systems for a given bandwidth is not always satisfactory for many applications, for example multi-user applications and multimedia applications including voice, data and video data streams.

[1] Near-far effect: When more than one users are active on a system, the power transmitted by non-reference users is suppressed due to the correlation between the codes of the active users. The interference caused by a non-reference user close to the receiver may have more power than a distant reference user, thereby drowning out the signal from the reference user.

> Object of the invention: Accordingly, it is an object of the present invention to provide a multi-dimensional DSSS modem, a modulator and a demodulator for such a modem and associated methods with which the applicant believes the aforementioned disadvantages may at least be alleviated."

The importance of the spreading sequences to spread spectrum is difficult to overemphasize, for the type of sequences used, its length, and its chip rate set bounds on the capability of the system that can be changed only by changing the spreading sequences [9, 10]. In order for an orthogonal set of sequences to qualify for use in a spread spectrum system, it is desirable for the sequences to have good cross-correlation and auto-correlation characteristics. Ideally, the cross-correlation between two different sequences of the same family would be 0 or constant and the auto-correlation would exhibit a single peak value at 0 time lag.

Families of complex spreading sequences exist that exhibit both these qualities [11]. These sequences are in the form of a complex number, with real and imaginary parts, so only a single sequence is required per user in a two-dimensional multi-user QPSK-like modulation system as opposed to a pair of binary sequences in convolutional systems [12]. Figure 1.1 shows the auto and cross-correlation of a length 13 root-of-unity filtered (RUF) sequence.

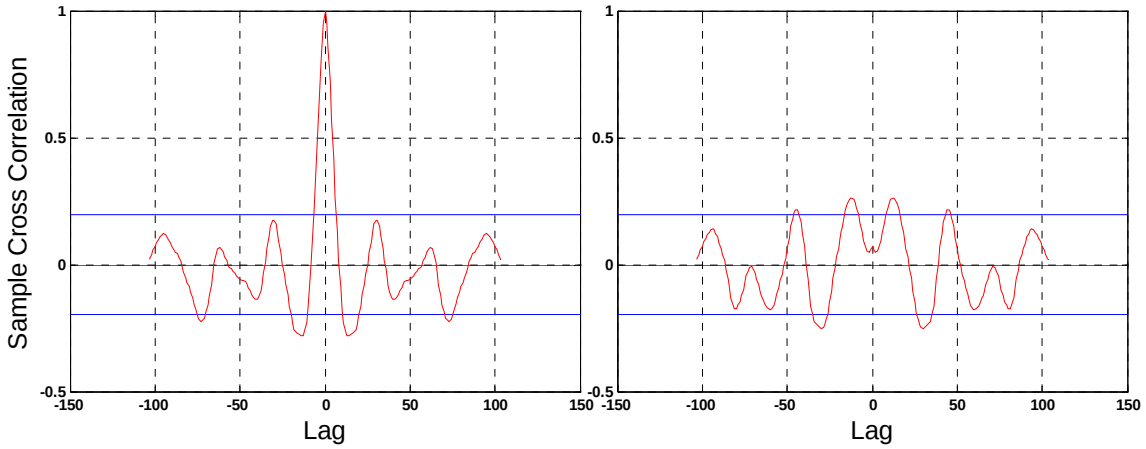


Figure 1.1.

Normalized auto-correlation and cross-correlation of a length 13 sequence. The horizontal lines indicate the 80% confidence intervals.

There is a strong market demand for cheap, but miniaturized, wireless systems. Such a system comprises of an RF transceiver that transfers antenna signals to bits and vice versa

and a digital sub-system for data processing. RF transceivers are typically realized in dedicated, expensive IC processes nowadays, whereas digital circuits are processed in the relatively cheap CMOS technology.

Parallel to the integration trend, nowadays there is the trend to integration of RF circuitry in CMOS technologies. When the technology is used without any special adaptations towards analogue design, the offering can be cheap. This is especially true if one wants to achieve the ultimate goal of full integration: the complete transceiver system on a single chip, both the analogue front-end and the digital demodulator implemented on the same die.

Due to limitations of CMOS performance in the RF range and analogue functions, bipolar CMOS (BiCMOS) technology is used most often for RF systems. BiCMOS combines the high speed and high driving capability of bipolar devices with the CMOS advantages of high density, low power and relatively low cost. BiCMOS technologies are commonly used, as bipolar transistors outperform CMOS transistors in many RF applications. This leads to smaller chip size and better design margins [13]. When comparing the relative sizes of BiCMOS, SiGe and CMOS radio design die areas, it can be seen that BiCMOS technology enables extremely small die sizes. BiCMOS also provides higher levels of integration and performance than similar CMOS solutions. The relative performances of CMOS, BiCMOS and bipolar technologies can be seen in Figure 1.2 [14].

1.2 Justification for research

It is clear from the literature that the theory regarding DSSS employing complex spreading sequences (CSS) is well developed, and several hardware and software implementations have been proposed.

The hardware implementations were either bulky [11] or required the use of a DSP, both of which are entirely digital. None of the implementations performed carrier recovery, which although treated as a trivial matter by the literature, still needs to be performed. A single chip solution does not yet exist that performs all functions required for a successful DSSS communication transceiver (implemented according to [8]). This will be the main contribution for this thesis, but the contribution is further appended by various RF design challenges: high-speed requirements make RF circuits extremely sensitive to the effects of

parasitics, including parasitic inductance, passive component modelling, as well as signal integrity issues.

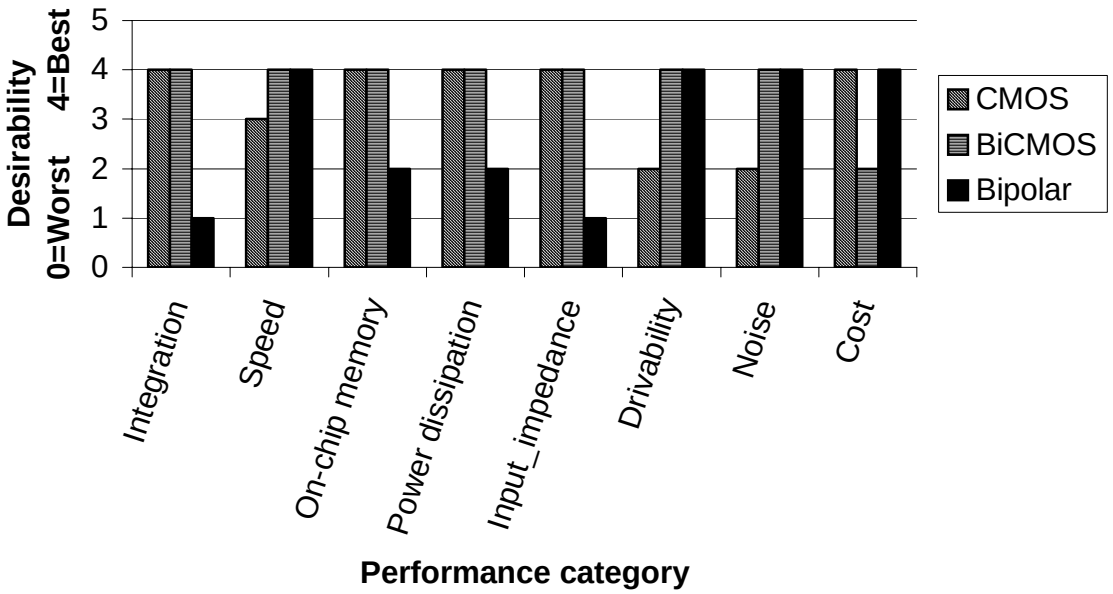


Figure 1.2.
Relative performance of CMOS, BiCMOS and bipolar technologies.

The design of a DSSS system introduces a set of trade-offs. Parameters such as power, BER, bandwidth, security and other related factors must be traded-off in order to find the optimal solution [7]. Under the DSSS scheme, each bit in the original signal is represented by multiple bits (chipping code) in the transmitted signal. The chipping code spreads the signal across a wider frequency band in direct proportion to the number of bits used [15]. The chipping code is a redundant bit pattern for each transmitted bit, thereby increasing the resistance of the signal to interference and corruption. The original data can still be recovered if a number of bits in the pattern are damaged during transmission. A longer chipping code supports more users and provides for greater security, but this is at the expense of increased bandwidth [16], as well as time to establish correlation at the receiver. This in turn decreases the efficiency with which the data is received, and should be compensated for. The PN sequence used in DSSS systems should have good cross correlation so as to support a multi-user environment, as well as good auto-correlation to allow for easy code synchronization. Various types of sequences, such as Kasami sequences and Gold sequences, are available for use in DSSS applications. However, trade-offs must be made once again when selecting the family of sequences. For instance, Gold codes provide a large sequence, whilst introducing relatively high noise levels.

Kasami sequences on the other hand introduce lower noise levels, but smaller family size. For this thesis, CSS is used (as discussed above Figure 1.1, and in Chapter 2). CMOS is further chosen from a perspective of cost (Figure 1.2), yet achieving adequate functionality for the research intended in this thesis.

The value system of the thesis will further encompass the following:

- optimize simulation time [17],
- facilitate verification,
- enable detailed analysis at the block and chip levels,
- manage and facilitate simulation with full parasitics,
- enable analysis (noise, IR, EM),
- include layout automation that can be used at appropriate points in the design, and
- enable several levels of passive modelling throughout the design process.

1.3 Methodology

The research process used in developing this thesis can be broken down to the following phases.

Phase 1: Literature studies to investigate system topologies developed elsewhere, and uniquely identify research niches (often either a system specification/topology and/or a specific circuit configuration). Challenges associated with recent device size miniaturization and associated simulation problems are included during such a study. Phase 1 was also supported by some project management, for instance development of work breakdown structures, and Gantt diagrams.

Phase 2: A system level analysis was proposed, and validated via system-level simulations (MATLAB was proposed for this purpose). The mathematical level analysis gave a good feeling of the feasibility, but was considered ideal as the circuit parasitics and stray elements cannot be modelled at this stage. An output of this phase was the system topology, system specifications, and system level simulations.

Phase 3: Upon accomplishing a system level design, the system was decomposed to gain an understanding at sub-system level, and sub-system specifications were developed. From the beginning, system integration was an important thought: hence, design was done to

include system interface specifications, too. These specifications are an output of this phase.

Phase 4: Circuit level designs were studied (to determine what exists elsewhere), and some unique solutions were proposed. Using suitable approximations, the circuits were first designed "by hand." Circuits were further tested by simulations: advanced CMOS circuit design software such as Tanner tools was deployed for this purpose. The outcome of this phase was several (sub-system) circuit schematics, and often circuit layouts (coined as part of a library). Such tools, when used with device models supplied by circuit manufacturers, could be effectively used in attaining worst case simulations.

Phase 5: The components of the library were integrated and a full-circuit layout was developed, i.e. a circuit level design and associated simulation was accomplished, and compared to the simulations output of Phase 2. A circuit netlist (including parasitic elements) was extracted from the layout, and also from the schematic, and this served as a further outcome of this phase.

Phase 6: The circuit netlist derived from layouts, and the circuit netlist derived from schematics were compared. During this phase, LVS (layout versus schematics) was performed and some more thorough, but automated, design evaluation: DRC (design rule check) was performed.

Phase 7: Via the Europractice programme, engaged by CEFIM, the IC was sent for fabrication. During this phase, the circuit models developed (in software) was used to construct some measurement printed circuit boards (PCBs). This was to enable speedy testing and measurement when the ICs are back from Europe. In parallel, the thesis was also partially completed.

Phase 8: The prototypes were received three months later, and measurements were performed. The thesis is further supported by the achieved measurement results.

Phase 9: The output of the research process was consolidated for an identified research journal, and further tested against overall international research endeavours in the field. In some cases, software will be written to archive the design process, to assist in future designs, one of the deliverables of the thesis. The thesis was fully completed thereafter.

Phases 4-6 are an important development part of this thesis, thus further discussed in Figure 1.3.

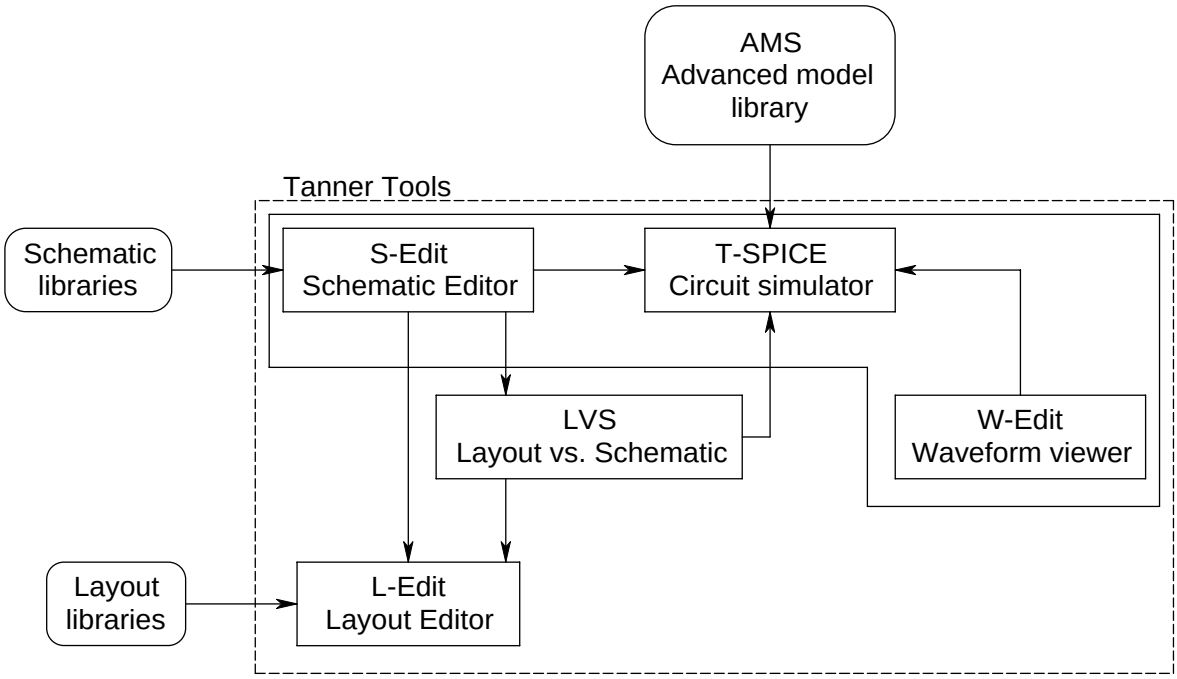


Figure 1.3.

Process followed during the design of the DSSS transceiver IC in terms circuit level design. The software tools that were used are shown at each node. The applications within the dashed frames are part of the Tanner tools.

The design carried out in this thesis involved the design of multiple stages, on a schematic and then layout basis [18]. Each sub-section was built up on a modular level, where each sub-section was simulated and verified, before being integrated. In layout a similar method of design was carried out from laying each transistor out in CMOS, however this was a far more intricate design process as factors such as parasitic capacitance had to be considered in each case. The layout was firstly verified using DRC. To complete all schematic, and layout requirements, the Tanner Tools Pro software package was utilised, as it includes all necessary software for schematic and layout design, as well as simulation. The tools included in the package that were utilised for this thesis are listed below.

S-Edit

Schematic capture was done using S-Edit, a software package included in the Tanner Tools Pro package to design schematics. The schematic contains all relevant information needed to create a netlist in various formats, including a compatible version for the use in SPICE

simulations. S-Edit exports the schematic design to a netlist using the 'SPICE OUTPUT' property of primitive devices[2].

T-SPICE

T-SPICE is a simulation engine based on Berkeley's SPICE3F5[3] simulation system. To be able to simulate a design, a netlist, as generated by S-Edit as well as the necessary model files are needed. Different types of simulations, (transient analysis, operating point determination, or frequency analysis) can be carried out, depending on the required simulation.

W-Edit

To interpret T-Spice output data, a waveform viewer named W-Edit was used. This software provided the graphical link between the simulation data and the user. W-Edit allows the user to perform various display options. W-Edit is also aimed mainly at the display of data from analogue simulation results, and was not very user-friendly in terms of displaying digital results. For this reason some of the results that were obtained from T-SPICE were exported to MATLAB which had better graph plotting capabilities, to be used for figures in this thesis.

L-Edit

L-Edit is the application within Tanner Tools used to develop the layout. At this level the transistors, capacitors and other devices are drawn in accordance with the design rules specified by the process from austriamicrosystems (AMS). The DRC module is included within L-Edit.

DRC

Due to the cost of IC manufacturing, certain rules such as spacing between tracks and minimum widths had to be carefully adhered to, in order for the manufactured IC to function properly, and according to the design process used. The DRC-engine has a database of all the rules as provided by AMS and cross-checks the layout according to these rules.

[2] A primitive device is a device which cannot be dissected to any lower level and its operation has to be defined. This includes resistors, capacitors transistors, diodes, etc.
[3] Developed at the University of Berkeley, http://www-cad.eecs.berkeley.edu

1.4 Outline of this thesis

The structure of this thesis is as follows:

- Chapter 1 (aligns with Phase 1 of the past sub-section) provides the background to the research, and provides motivation for the work. To allow for a full research investigation, a prototype is to be developed.
- Chapter 2 (Phase 2) further motivates the type of spreading sequence. A functional analysis for the prototype is proposed, and developed at a system-level. From the functional analysis, more clarity to the analogue and digital sub-systems is proposed.
- Chapter 3 (Phases 1, and 3-5) develops the analogue sub-systems at transistor level.
- Chapter 4 (Phases 1, and 3-5) develops the digital sub-systems at transistor level.
- Chapter 5 (Phases 1, and 6-8) serves to integrate the past two chapters, as per the system-level intentions of Chapter 2. The prototype is coined, in software, as an IC (a library), and an analogy is drawn to hardware. Considerations relating to device packaging are first investigated, and a qualification protocol is setup. A complete verification is done by characterizing the prototypes.
- Chapter 6 (Phases 8-9) serves to conclude the thesis by summarizing the contributions from the abovementioned process.

1.5 List of publications

Several publications have a result of works directly or indirectly relating to this thesis. A listing is provided below.

Journal publications

M. Božanić, S. Sinha, J. Schoeman, L.P. Linde, and M du Plessis, “CMOS Direct Sequence Spread Spectrum Transceiver Employing Complex Sequences,” submitted to the Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE), Oct. 2008.

M. Božanić and S. Sinha, "Software Aided Design of a CMOS Based Power Amplifier Deploying a Passive Inductor," Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 99, No. 1 (March 2008), pp 18-24.

S. Sinha and M. du Plessis, "PLL based frequency synthesizer implemented with an active inductor oscillator," Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 97, No. 3 (Sept. 2006), pp 237-242.

H.R. Swanepoel and S. Sinha, "Design of a frequency hopping spread spectrum transceiver for CDMA2000 systems", Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 97, No. 3 (Sept. 2006), pp 248-254.

O.S. Adekeye, S. Sinha and M. du Plessis, "Design and Implementation of a CMOS Automatic Control Gain Control (AGC) Amplifier," South African Journal of Science, Vol. 102, No. 11/12 (Oct./Nov. 2006), pp. 606-608.

Peer-reviewed international conference proceedings

T.S. Elenjical, S. Sinha, and L.P. Linde, "Analogue CMOS DSSS CDLL synchronisation scheme employing complex spreading sequences," Proceedings: IEEE Melecon 2008, 5-7 May, 2008, Corsica, France, pp. 380-386.

N. Naudé, L.P. Linde, and S. Sinha, "CMOS Based Decision Directed Costas Carrier Recovery Loop (DDC-CRL) for a DSSS Communication System," Proceedings: IEEE Africon 2007, Sept. 26-28, 2007, Windhoek, Namibia.

M. Božanić and S. Sinha, "Design methodology for a CMOS based power amplifier deploying a passive inductor," Proceedings: IEEE Africon 2007, Sept. 26-28, 2007, Windhoek, Namibia.

S.W. Ross, and S. Sinha, "A pipeline analogue to digital converter in 0.35 μm CMOS," Proceedings: IEEE Eurocon 2007, Sept. 9-12, 2007, Warsaw, Poland, pp. 1096-1100

N. Naudé, S. Sinha and M. Božanić, "Design of a CMOS DSSS Transceiver with Carrier Recovery Employing Complex Spreading Sequences," University of Pretoria Research Symposium, Sanlam Auditorium, 26 Oct. 2006.

N. Naudé, M. Božanić, and S. Sinha, "Analogue CMOS Direct Sequence Spread Spectrum Transceiver with Carrier Recovery Employing Complex Spreading Sequences," Proceedings of the IEEE MELECON 2006, May 16-19, 2006, Benalmádena (Málaga), Spain, pp. 1227-1231. [Selected finalist for the IEEE Student Paper Contest – IEEE Region 8]

CHAPTER 2: SYSTEM ANALYSIS AND DESIGN

This chapter motivates this thesis by presenting the broader research context. A design motivation is proposed, developed mathematically, and verified at systems-level. Developed design specifications serve as a qualification protocol to address the research questions posed in Chapter 1.

2.1 Direct sequence spread spectrum (DSSS)

DSSS, also known as direct sequence code division multiple access (DS-CDMA), is one of two approaches to spread spectrum modulation for digital signal transmission over the airwaves. The design of a DSSS system introduces a set of trade-offs. Parameters such as power, bit error rate (BER), bandwidth, security and other related factors must be traded-off in order to find an optimal solution [19]. Under the DSSS scheme, each bit in the original signal is represented by multiple bits (chipping code) in the transmitted signal. The chipping code spreads the signal across a wider frequency band in direct proportion to the number of bits used [15]. The chipping code is a redundant bit pattern for each transmitted bit, thereby increasing the resistance of the signal to interference and corruption. The original data can be recovered if a number of bits in the pattern are damaged during transmission. A longer chipping code supports more users and provides for greater security, but this is at the expense of increased bandwidth [16], as well as time to establish correlation at the receiver. This in turn decreases the efficiency with which the data is received, and should be compensated for. The PN sequence used in DSSS systems should have good cross-correlation so as to support a multi-user environment, as well as good autocorrelation to allow for easy code synchronization. Various types of sequences, such as Kasami sequences and Gold sequences, are available for use in DSSS applications. However, trade-offs must be made once again when selecting the family of sequences. For instance, Gold codes provide a large number of codes, whilst introducing relatively high noise levels. As a rule of thumb only approximately 10% of the family size can be used whereafter the multi-user interference (MUI) would have grown to such proportions so as to render the processing gain useless [9]. Kasami sequences on the other hand introduce lower noise levels, but smaller family size. For this thesis, CSS is chosen. While CSS was proposed in 1992 [20], its usage in DSSS systems is proposed in the patent [12] for DSSS communication systems. The use of the CSS allows for various data rates by choosing

different sequence lengths and transmission bandwidths. It also allows for a choice of modulation techniques and guarantees the processing gain of 20 dB. When CSS are used, a transmitter can operate in both balanced and unbalanced fashion by using one spreading sequence for every two-dimensions utilised.

The proposed CSS are generalized-chirp like (GCL) sequences. The *r*th sequence is defined [20] as

$$c(r,k) = \begin{cases} W_N^{\frac{k^2}{2}+ql} & ; N \text{ even} \\ W_N^{\frac{k(k+1)}{2}+qk} & ; N \text{ odd} \end{cases} \tag{2.1}$$

where W_N is defined as $W_N = e^{-j\frac{2\pi r}{N}}$, $j = \sqrt{-1}$, r is any integer relatively prime to N, $k = 0, 1, 2, \ldots, N\text{-}1$, and q is an integer. Sequences must be sampled for their use in DSSS transceiver systems. The sampling rate is chosen so that the bandwidth, as determined by the IEEE 802.11 standard is

$$BW = \frac{f_{sample}}{RF\_samples\_per\_chip} \tag{2.2}$$

where BW is the bandwidth. The length of the spreading sequence is chosen arbitrarily. With increased sequence length, the number of possible users in a multi user environment increases. Alternatively, the sequence families can be used in one transmitter to increase data rates by means of serial-to-parallel conversion.

The spectrum of a long unfiltered GCL sequence is perfectly flat, as shown in Figure 2.1; therefore, for the use of such sequences in a band limited communication system, the sequences must be filtered.

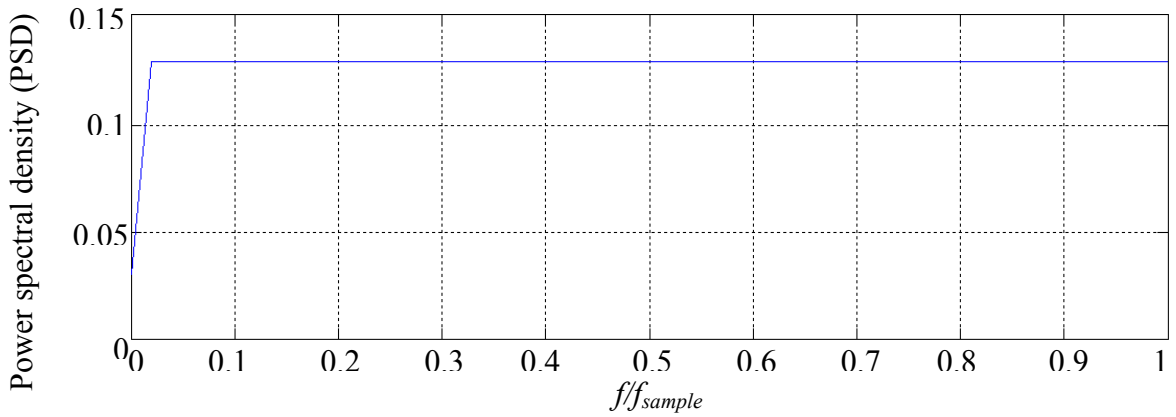


Figure 2.1.

Power spectral density (PSD) of length 49 complex sequence.

CSS exhibits two very important properties: good auto-correlation and good cross-correlation. These properties prove the orthogonality of CSS. Ideally, the cross-correlation between two sequences inside a family will be a constant, and the autocorrelation will exhibit the peak value at the zero-time lag. Filtered sequences do not have ideal properties, but the properties can be assumed within a confidence interval. The two correlation functions of length 13 sequences are shown in Figure 2.2 and Figure 2.3, respectively.

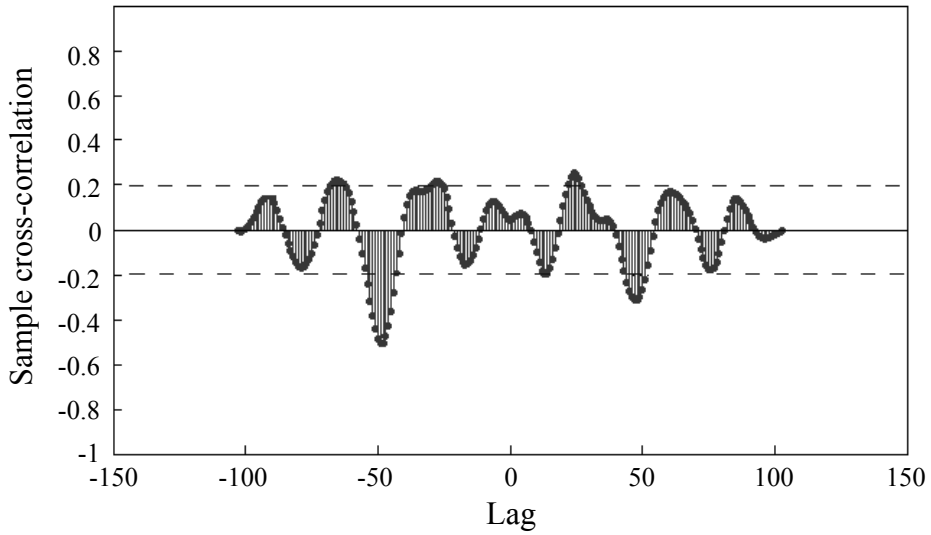


Figure 2.2.

Cross-correlation of two sequences of length 13. Lines $y = \pm 0.2$ present 80 % confidence intervals.

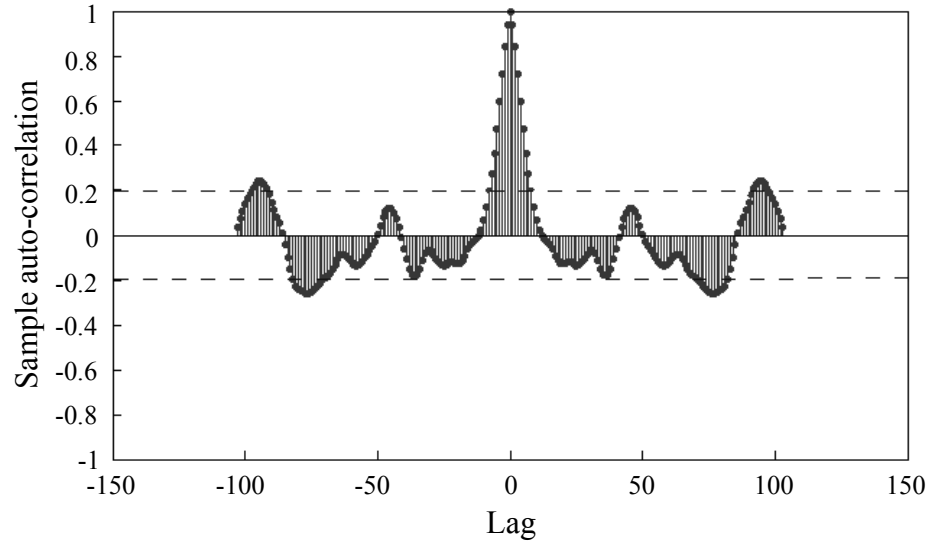


Figure 2.3.

Auto-correlation of the real part of the length 13 sequence. Lines $y = \pm 0.2$ present 80 % confidence intervals.

The exact sequences used in this thesis are protected by a non-disclosure agreement (NDA) between the author and the University of Pretoria, and will therefore not be detailed here.

2.2 System Analysis

The system analysis depends on the type of modulation scheme. Two techniques were considered, BPSK and Q^2PSK. Section 2.2.1 presents the BPSK based system analysis, which also serves to give a general system analysis, and then section 2.2.2 presents QPSK based system analysis. Furthermore, in Section 2.2.1 Gold codes of length 31 chips per data bit were chosen for the first analysis as they are easier to implement, and yield a CDMA system comparable with existing binary standards, which may also simultaneously provide some useful benchmark to compare with the CSS used in Section 2.2.2.

2.2.1 BPSK based system analysis

Figure 2.4 presents the functional analysis for a DSSS transceiver.

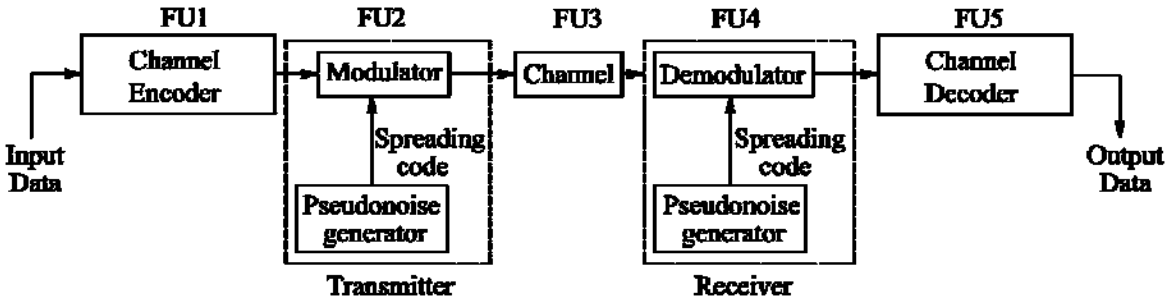
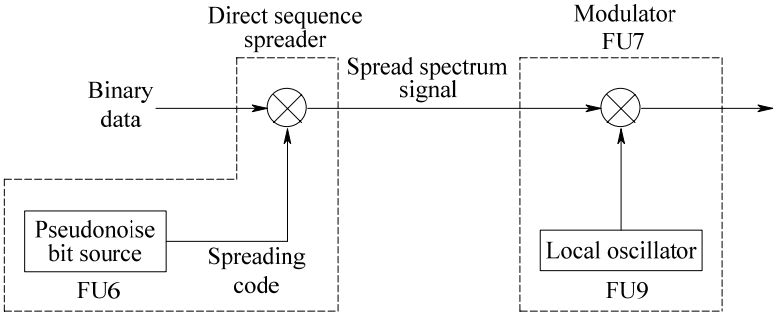


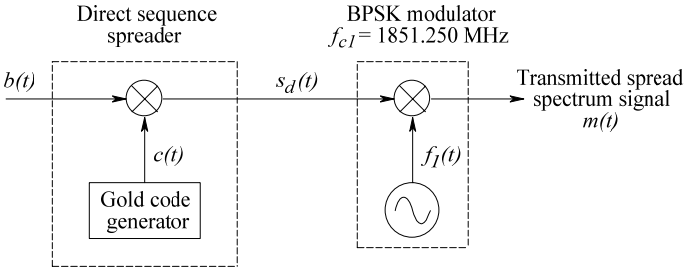
Figure 2.4

DSSS transceiver functional analysis. FU stands for functional unit.

Figure 2.5 and Figure 2.6 shows the transmitter and receiver functional analysis separately.



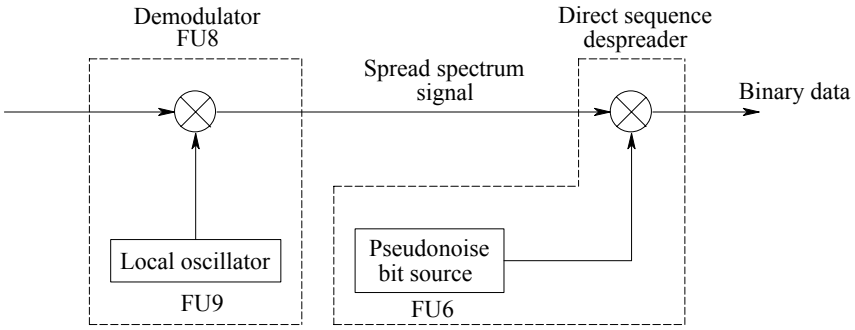
(a)



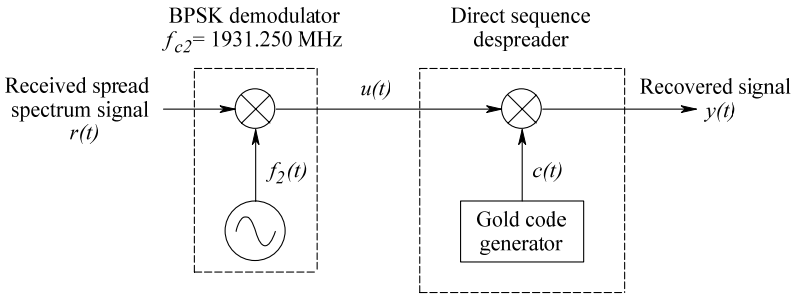
(b)

Figure 2.5.

Functional block diagram of the (a) generalized DSSS transmitter module, and (b) transmitter module employing BPSK modulation and a Gold sequence.



(a)



(b)

Figure 2.6.

Functional block diagram of the (a) generalized DSSS receiver module, and (b) receiver module employing BPSK modulation and a Gold sequence.

The system receives a digital signal as input. The channel encoder (FU1) then produces a signal with a relatively narrow bandwidth around some centre frequency. The data signal is then sent through the direct sequence (DS) spreader, which spreads the received signal using the user specific chipping code generated by the pseudonoise (PN) bit source (FU6). This serves to increase the bandwidth of the data signal, or in effect, spreads the spectrum. This signal is then sent to the transmitter (FU2), where it is subsequently modulated (FU7) with the HF output of the LO (FU9). BPSK/NRZ is used as a digital-to-analogue encoding scheme in the modulator in this subsystem. This is used to represent the phase shifted data in terms of 1's and -1's, rather than 1's and 0's.

The signal is then transmitted over the wireless channel (or air interface) (FU3) to the receiver (FU4). The received signal is then despread using the same scheme as the modulator in FU6. The channel decoder (FU5) recovers the original data signal. The signal is then despread by the DS despreader, using the same chipping code as used in the transmitter (FU2). This decreases the input signal bandwidth (or effectively despreads the spectrum of the input signal), to obtain the original encoded data signal.

The implementation discussed above assumes signal transmission between the mobile station (MS) and the base transceiver station (BTS). The demodulation of such a system requires the LO's at both the transmitter and the receiver to operate at the same frequency in order to convert the received signal to baseband.

The following paragraphs discuss the transmitter shown in Figure 2.5 (b).

The direct sequence (DS) spreader is used to spread the received binary signal, *b(t)*, with the user specific chipping code, *c(t)*, that is generated by the Gold code generator. The input signal bit rate was chosen so as to allow for transmission of good quality signals e.g. music. This spreading function serves to increase the bandwidth of the data signal, or effectively spreads the spectrum in direct proportion to the number of chips used. Spreading results in the signal in

$$s_d(t) = b(t)c(t) \tag{2.3}$$

The results of this signal spreading can be seen in Figure 2.7.

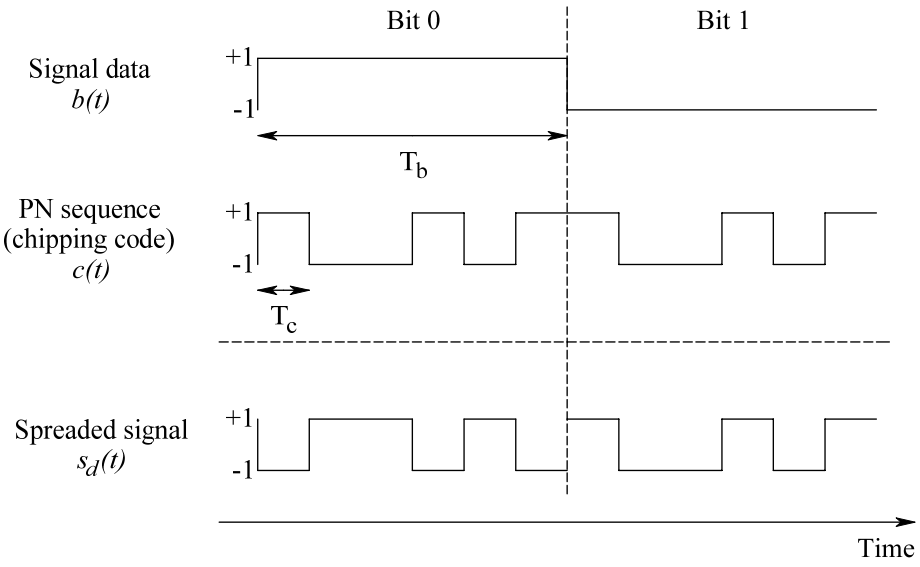


Figure 2.7.

Representation of binary data, *b(t)* and PN sequence, *c(t)* used in BPSK DSSS systems, as well as the resulting signal $s_d(t)$ when the data signal is spread.

A PN sequence of length $L = 31$ bits results in a transmitted signal rate of 31 Mcps when transmitting a high quality signal (for instance, a music signal at 1 Mbps). In the ideal case, an RF bandwidth 31 times greater than the original signal bandwidth is required for transmission of the spread spectrum signal. Thus, in this case a baseband bandwidth of 31 MHz is required for successful transmission of such a signal.

The required RF bandwidth is related to the data rates in the following way when using ideal Nyquist filtering (i.e. with roll-off, $\alpha = 0$):

$$B_T = 2f_{NYQ} = f_c = Lf_b \tag{2.4}$$

B_T is the bandwidth required for transmission (after modulation), L is the length of the chipping code, f_{NYQ} is the Nyquist frequency, f_c is the reciprocal of the chip period and f_b is the reciprocal of the data period.

Figure 2.8 serves as a graphical representation of the spreading of the signal bandwidth.

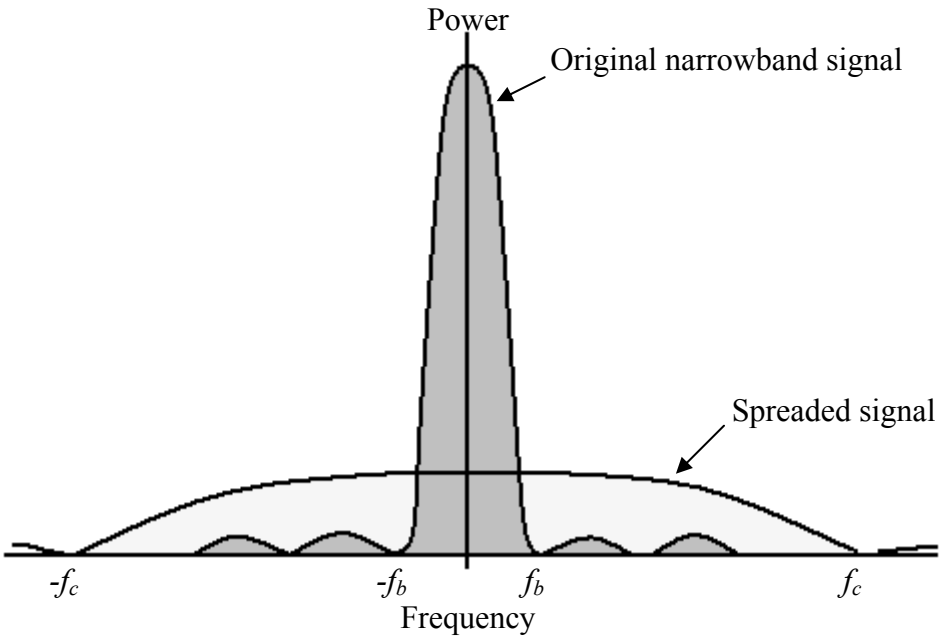


Figure 2.8.

Relative bandwidth of the original signal and the spread spectrum signal obtained by modulation with a chipping code.

The signal is subsequently modulated onto the carrier (operating) frequency. The carrier frequency of the transmitter module has been chosen to be 1851.250 MHz, to comply with CDMA2000 specifications [21]. BPSK has been used as the digital-to-analogue encoding scheme in the modulator in this subsystem as it is one of the more power efficient modulation schemes. BPSK modulation results in a signal of the form

$$m(t) = s_d(t) A \cos(2\pi f_{c1} t) \tag{2.5}$$

where A is the amplitude of carrier signal and f_{c1} is the transmitter carrier frequency.

At this point, external filtering of the signal may be done in order to reduce the transmitted bandwidth. For this function, Nyquist's criterion [15] should be considered.

The RF modulated spread spectrum signal, *m(t)*, is then transmitted over the air interface to the receiver. This channel (air interface) may add a narrow band interference signal, *i(t)*, to the transmitted signal that has been spread, as shown in Figure 2.9. The following signal results:

$$r(t) = m(t) + i(t) = s(t) A \cos(2\pi f_{c1} t) + i(t) \tag{2.6}$$

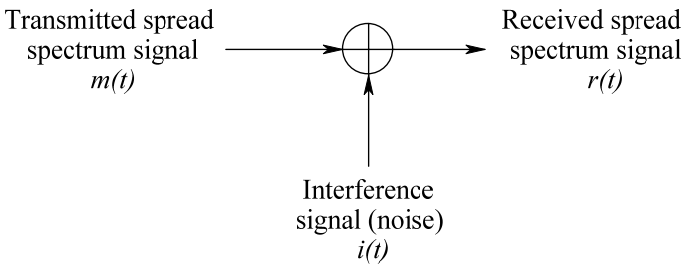


Figure 2.9.

Interference added by the transmission channel (air interface).

Despreading of the interference signal works in the same way as the original spreading of the data signal (commutative function), thus the interference signal is spread over a wider bandwidth. When the spread data signal is despread the original narrowband signal is obtained. Spreading of the received signal, therefore results in the original data signal and a wideband interference signal with low amplitude. Most of this interfering signal can then be filtered out, leaving the narrowband data signal. This interference term is however neglected in the present analysis in order to simplify the calculations.

The received signal is demodulated using the same modulation scheme as previously used to modulate the signal before transmission, as shown in Figure 2.6 (b).

In the case of the DSSS transceiver, the signal is received from the BTS. The BTS transmitter uses the same modulation scheme as the MS transmitter (i.e. BPSK), but at a frequency of 1.93125 GHz. Demodulation of the RF signal results in a signal that has components at both the sum and difference of the spread transmitted signal frequency, and the oscillator frequency (this is explained in more detail later). The high frequency signal components can be filtered out, leaving only signal components present at the spread signal frequency, $s_d(t)$.

The signal is then despread by the DS despreader which uses the same chipping code, $c(t)$, as that which was generated at the transmitter (assuming perfect code synchronisation).

The recovered signal is

$$y(t) = c(t)s_d(t) = b(t)c^2(t) \tag{2.7}$$

However

$$c(t) \cdot c(t) = 1 \tag{2.8}$$

This is true as *c(t)* takes on only two values, -1 and 1. The result is the original data signal being recovered at the system output.

$$y(t) = b(t) \tag{2.9}$$

2.2.2 QPSK based system analysis

In [22] four distinct two-dimensional (2D) modulation techniques were proposed for the DSSS system employing the CSS: QPSK, $\pi/4$-QPSK, 8-PSK and 7x1-PSK [22]. A higher processing gain is obtained when the QPSK transceiver uses SSB and is operated in balanced mode, data transmission rate cannot be increased by more than a factor of two. For these reasons, a basic QPSK design will normally employ DSB modulation. The signal constellation of the basic QPSK modulation scheme is given in Figure 2.10.

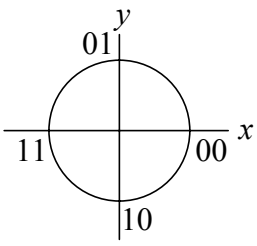


Figure 2.10.
QPSK constellation.

For this thesis, only the QPSK-based system is of importance [12], since the final Q^{2}PSK modulation scheme is derived from it (i.e., two 2D QPSK systems in parallel).

Balanced and unbalanced configurations of the Q^{2}PSK DSSS transmitter

Figure 2.11 shows a transmitter operating in the balanced configuration. With balanced transmission the same data stream is transmitted on all orthogonal bases (the inphase and quadrature components inclusive), so that whenever the signal of one or more components is lost during the transmission the original data can be recovered from other components. Thus, an inherent fourth order diversity gain is achieved with this particular configuration. If the incoming data sequence is $a(t)$, then the transmitted signal is [12]

$$\begin{aligned} u(t) &= a(t)C_r \cos\omega_c t + a(t)C_i \cos\omega_c t + a(t)C_r \sin\omega_c t + a(t)C_i \sin\omega_c t \\ &= a(t)\{\zeta_1(t) + \zeta_2(t) + \zeta_3(t) + \zeta_4(t)\} \end{aligned} \tag{2.10}$$

where C_r is the CSS real part, C_i is the CSS imaginary part, and $\{\zeta_i\}$, i =1, 2, 3, 4 constitutes the 4D orthogonal base. For this equation to be valid, $a(t)$ must have non-return

to zero (NRZ) levels of 1 and -1. This equation was expanded for further comparison with the unbalanced configuration.

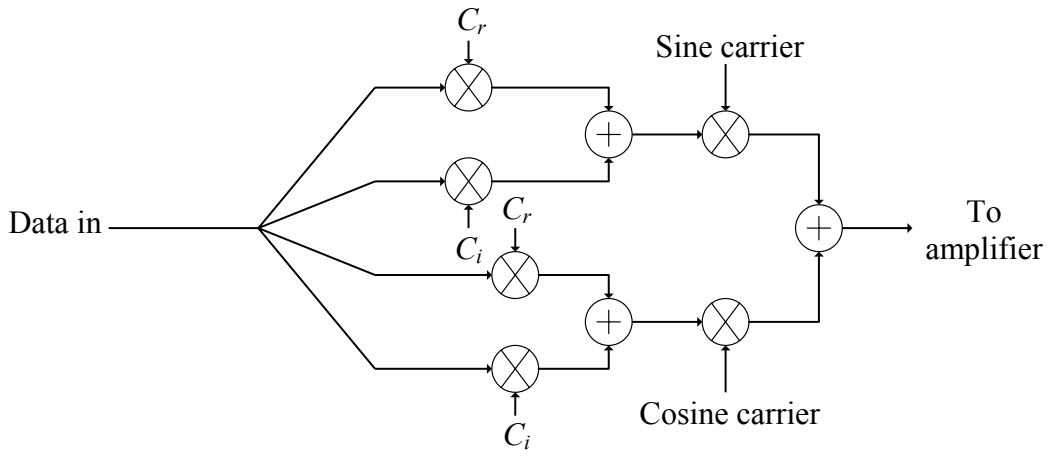


Figure 2.11.

Balanced Q^2PSK configuration of a DSSS transmitter.

Figure 2.12 shows a transmitter operating in an unbalanced configuration. The data signal is converted into four parallel data streams $a_1(t)$, $a_2(t)$, $a_3(t)$, and $a_4(t)$, and each signal is multiplied with different base-carrier combinations. The transmitted signal is now

$$\begin{aligned} u(t) &= a_1(t)C_r \cos\omega_c t + a_2(t)C_i \cos\omega_c t + a_3(t)C_r \sin\omega_c t + a_4(t)C_i \sin\omega_c t \\ &= a_1(t)\zeta_1(t) + a_2(t)\zeta_2(t) + a_3(t)\zeta_3(t) + a_4(t)\zeta_4(t) \end{aligned} \tag{2.11}$$

It can be seen from Equations (2.10) and (2.11) that the signals transmitted in the balanced and unbalanced configurations have the same form, and that by including and excluding the serial-to-parallel converter from the circuitry the transmitter (and receiver) can be made to operate in both modes.

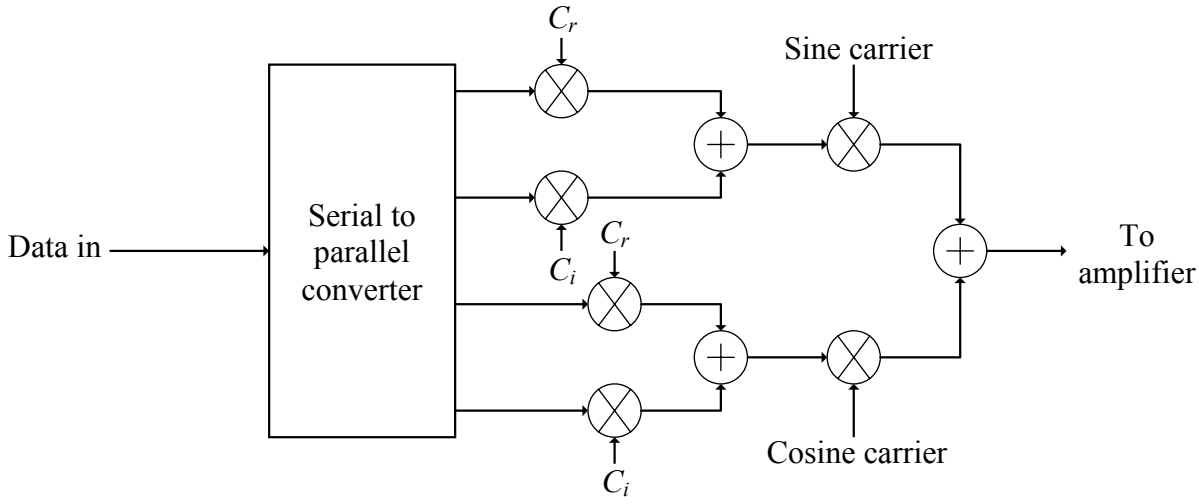


Figure 2.12.

Unbalanced Q^2PSK configuration of a DSSS transmitter.

Channel models

The DSSS transmitter operates over noisy and fading channels.

The noise in a channel can be modelled by Gaussian (normal) distribution. PDF of this distribution is given by

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}}, x \in \mathbb{R} \tag{2.12}$$

where μ is the mean and σ^2 is the variance. Noise has an additive effect on the transmitted signal.

Fading of the channel can be modelled by the Rayleigh and Rician models. The Rayleigh fading signal amplitude is described by the PDF [16]

$$f(\alpha) = \begin{cases} \frac{\alpha}{\sigma^2} e^{-\alpha^2/2\sigma^2}, \alpha \geq 0 \\ 0, \alpha < 0 \end{cases} \tag{2.13}$$

The Rician fading amplitude is given by the PDF [16]

$$f(\alpha) = \frac{\alpha}{\sigma^2} e^{-(\alpha^2+s^2)/2\sigma^2} I_0\left(\frac{s\alpha}{\sigma^2}\right), \alpha \geq 0 \tag{2.14}$$

where s^2 represents the power of the received nonfading component and $I_0(s\alpha/\sigma^2)$ is the modified Bessel function of order zero. Both the Rayleigh and Rician distributions have a multiplicative effect on the transmitted signal.

Topology trade-offs

The following is the list of trade-offs that govern the topology chosen.

- Various modulation schemes were proposed for a DSSS transceiver employing complex sequences.
- The transceiver can be operated in balanced and unbalanced modes. When the balanced mode is used, the maximum data rate that can be transmitted over the channel is determined purely by the available bandwidth, the CSS length and the roll-off factor of the Nyquist filter used for bandwidth limiting. When operated in this mode the system cannot be made faster than $BW/(1+\alpha)L$, where BW is the bandwidth, α is the roll-off factor of the Nyquist filter and L is the CSS length. However, if one of the signal components is lost in transmission, the data can still be recovered from the other signal components. When the unbalanced mode is

applied, the possible data rate is $BW/(1+\alpha)L$ times the number of the orthogonal bases used (four in the case of this thesis).

- Another trade-off exists between using single sideband (SSB) and double sideband (DSB) for modulation. SSB uses less bandwidth, yet obtains faster data transmission. However, for SSB modulation, a specific choice of the CSS must be made: sequences must be capable of annulling one sideband when real and imaginary parts are mixed with the sine and cosine carriers, and added together. A further drawback is that with SSB implementation, the transceiver cannot operate in unbalanced mode.
- There is a large number of CSS to choose from. It is possible to generate a number L of CSS in a family, where L is the CSS length (where L is a prime number). Auto-correlation and cross-correlation properties (together with information for signal recovery) improves with increase in the CSS length, but the data rate ($BW/(1+\alpha)L$) decreases.

Topology choices

The following choices from the previous subsection took precedence.

- The thesis is aimed for research purposes only. Therefore, only one CSS is used in conjunction with a sine carrier and a cosine carrier, giving effectively only four orthogonal bases (CSS real part and inphase carrier, CSS real part and quadrature carrier, CSS imaginary part and inphase carrier; and CSS imaginary part and quadrature carrier), yielding Q^2PSK (i.e., two 2D QPSK modulators in parallel, as described previously).
- Both balanced and unbalanced operation modes of the transceiver are desirable for implementation, the thesis includes a possibility to switch between the two modes of operation.
- Since the prototype device makes use of only one CSS in a family, shorter CSS are desired to obtain high data rate. Sequence of length L=13 from the Zadoff-Chu (GCL) CSS family is the most viable option [12].

In the rest of this section, the first concept design for this thesis is presented. Similar to an earlier section, a functional analysis is presented. For the purpose of the functional analysis, the transmitter (Figure 2.13) and receiver (Figure 2.14) will be considered separately.

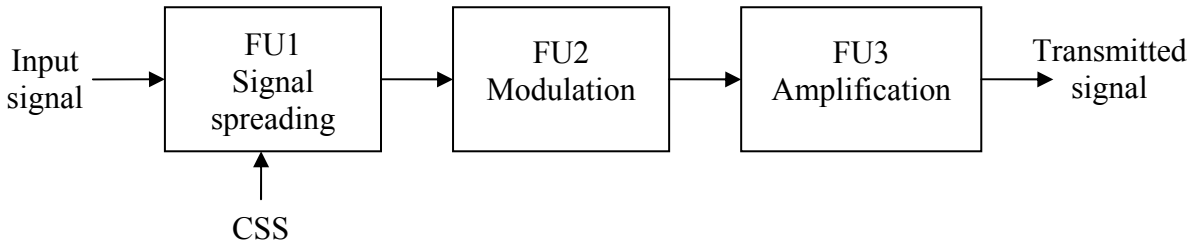


Figure 2.13.

Functional diagram of the proposed DSSS transmitter.

A binary signal is received as an input to the transmitter. Relevant complex calculations are performed in FU1. The signal is multiplied by a CSS available from the outside of the chip, which spreads it in the frequency domain. FU2 serves to modulate the output of FU1 to the required frequency band. In FU3 the output of FU2 is amplified to the power level required for the transmission.

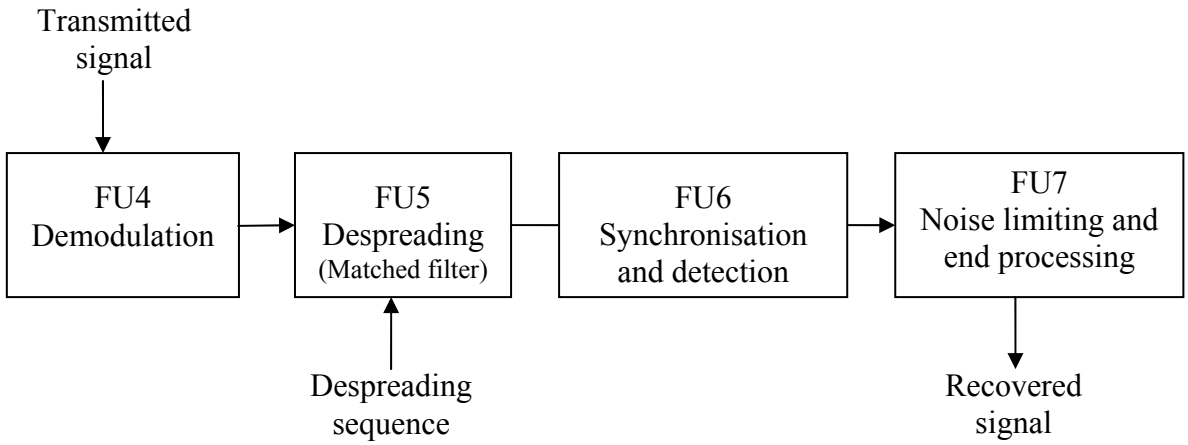


Figure 2.14.

Functional block diagram of the proposed DSSS receiver.

The transmitted signal corrupted by noise is amplified (by a low noise amplifier (LNA)) and quadrature demodulated by FU4 of the receiver. After demodulation and filtering (LPF), the signal is despread by a despreading sequence in FU5 (decorrelation matched filter). The despread signal of FU5 is sampled and level detected by FU6, thereby recovering the data as a baseband signal. Necessary signal shaping is performed in FU7. Here, the signal is filtered in order to limit the noise created in the process of demodulation. This subsystem also includes the end processing of the signal, such as the combining of the signal components (i.e., parallel-to-serial conversion) and wave shaping.

The next few paragraphs serve to analyze some of the above FUs in more detail.

In FU1, spreading of the binary data signal is performed. First, the signal is passed through a switching circuitry which determines whether the transmitter is operating in the balanced (Figure 2.11) or unbalanced (Figure 2.12) configuration. If the unbalanced mode is used the serial-to-parallel conversion is done to obtain four data streams. In the balanced mode the signal is simply fed to four lines. The four data streams are then mixed with the CSS real and imaginary parts. The CSS are available externally, either from a personal computer (PC) or from an external memory module. In simulation the root-of-unity filtered (RUF) CSS real and imaginary parts are treated as separate inputs (the so-called equivalent baseband form). Sequences are sampled at the rate as follows:

$$f_{sample} = BW \cdot samples\_per\_chip = 20\,\text{MHz} \cdot 8\,\text{samples/chip} = 160\,\text{Msamples/s} \quad (2.15)$$

The chosen spreading sequences of L=13 chips result in 8 × 13 = 104 samples for one sequence repetition.

For the block diagram of the implementation of this FU (assuming the unbalanced mode), refer to Figure 2.15.

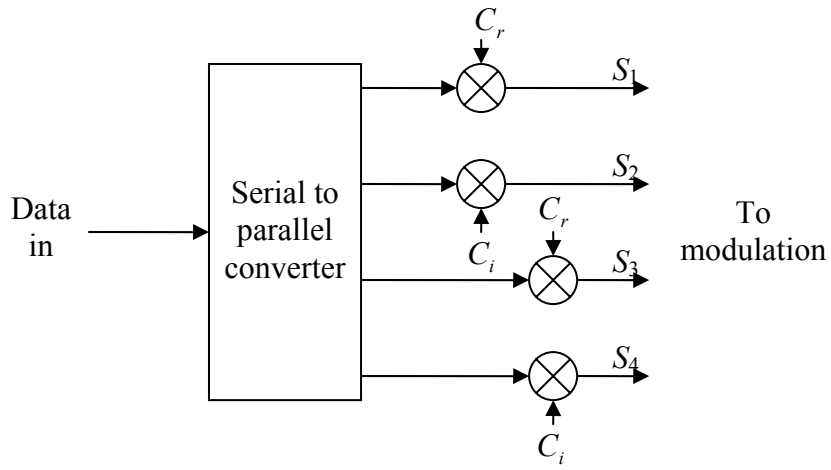


Figure 2.15.
Block diagram of FU1. C_r and C_i are the CSS RUFed real and imaginary parts and S_1 to S_4 are signal lines.

The mixers that multiply data streams S1 to S4 with the CSS real and imaginary parts, and the serial-to-parallel converter form the core of this subsystem from a microelectronics perspective.

Modulation is implemented by FU2. In this subsystem four signals are mixed with the sine and cosine carriers running at the frequency within the range of 2.4 GHz ISM band. The

four signal lines are then added and fed to the amplifier. This is shown in Figure 2.16. LO with phase shifters and mixers is used in the implementation of this subsystem.

FU3 serves as RF amplifier and transmitter of the signal. The core of this block is a power amplifier (detailed in chapter 3). This is the last bit of circuitry on the transmitter side of the transceiver IC.

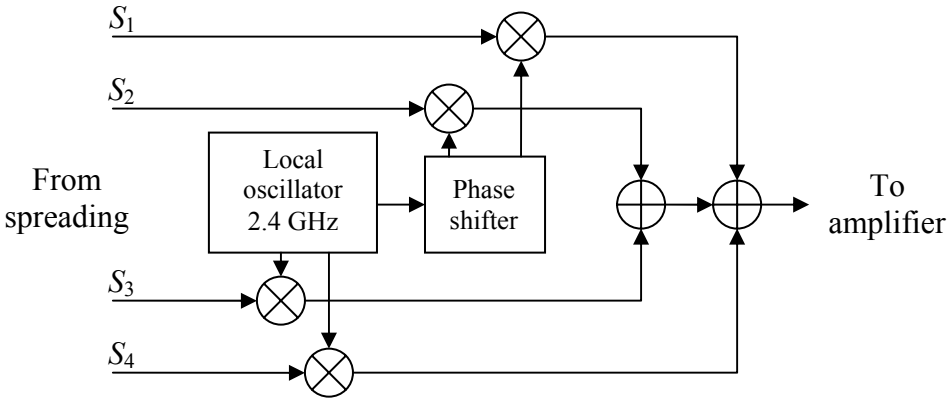


Figure 2.16.
Block diagram of FU2.

The functional block diagram of the receiver is shown in Figure 2.14. The signal is first amplified (by a LNA), and demodulated (FU4) from a noisy, fading channel at the carrier frequency (close to 2.4 GHz). This is on-chip circuitry on the receiver side of the transceiver IC.

This is followed by demodulation (FU4) and despreading (FU5). The order of despreading and demodulation assists from a perspective of implementation, since better isolation can be achieved (prevention of RF coupling). At the first concept design level the detected signal was first brought down to baseband by being split into two lines and mixed with the sine and cosine carriers at the required frequency. Signals are then filtered to eliminate the double frequency carrier components.

Each of the signals is then split again and as the CSS are pre-RUFed at the receiver (i.e., effectively interpolated and filtered on the unity circle, with roll-off factor α = 0, closely resembling a Nyquist filter), despreading is achieved in the receiver by merely decorrelating the RUF CSS sequences by a local pre-stored zero-interpolated replica of the relevant spreading sequence components, C'_r and C'_i, containing only the non-zero primary sequence samples.

Integration and dump circuitry as well as comparators are then used as the decision logic on each signal line (FU7). . In this way, four signals are created that resemble the four original parallel data streams, S_1 to S_4.

In the case of the balanced receiver configuration, all four data lines will ideally contain exactly the same signals as the input signal to the transmitter, while in the case of the unbalanced configuration the four data lines will have to be passed through a parallel-to-serial converter to obtain the original data signal.

Data and sampling rates of signals on the receiver side of the transceiver IC are identical to the data and sampling rates of the signals on the transmitter side. The core of the receiver consists of mixers, an oscillator with phase shifters, switching circuitry, integration circuitry, comparators, and a parallel-to-serial converter. The complete block diagram of the transceiver discussed so far is given in Figure 2.17 [12]. Input is marked with Data in and output with Data out. The unbalanced transceiver configuration is assumed. As discussed earlier, the primary sampled zero-interpolated CSS real (C'_r) and imaginary (C'_i) parts are input from outside the IC in the receiver.

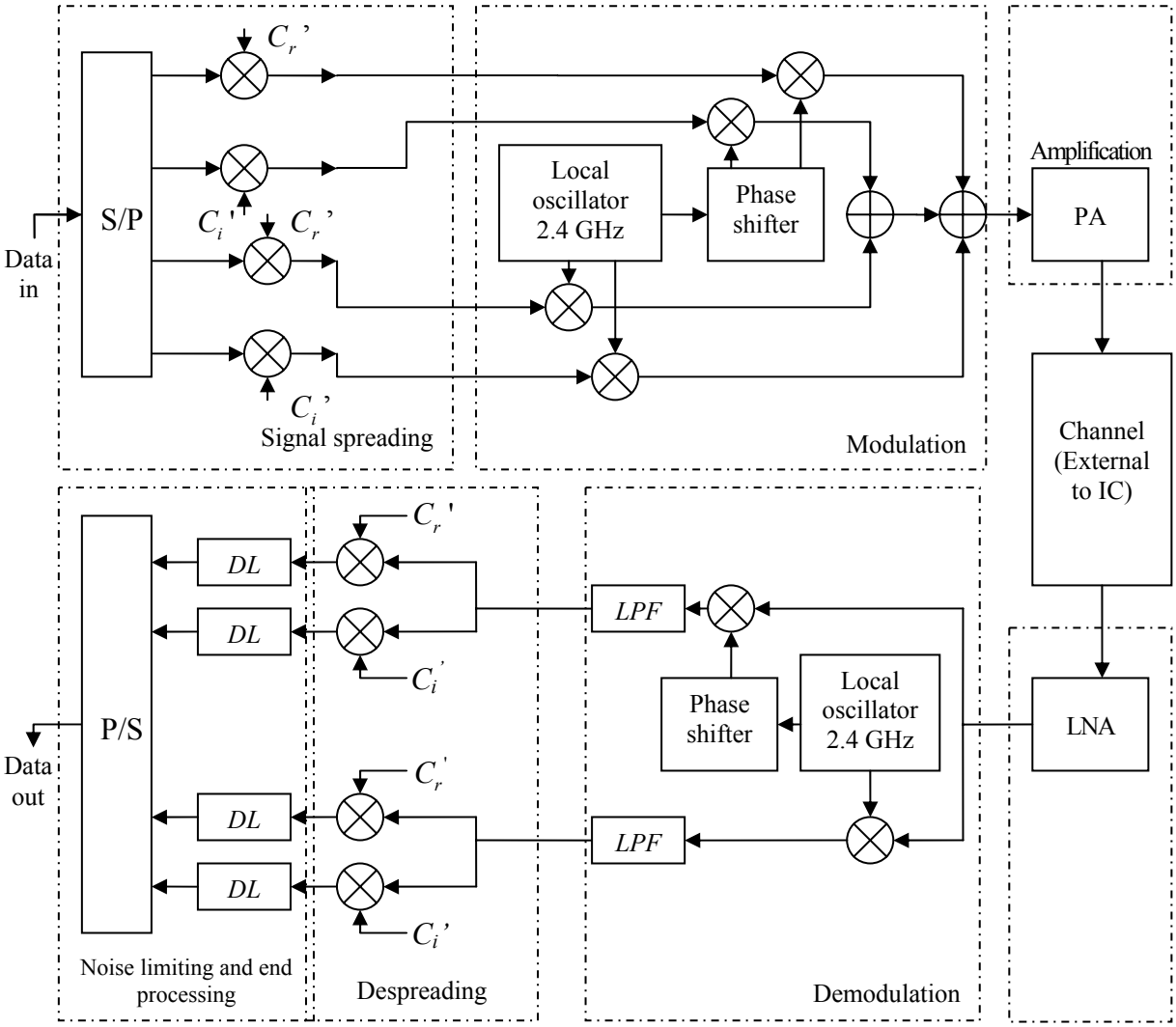


Figure 2.17.

Concept design of the transceiver. LPF stands for low-pass filter and DL for decision logic.

To simplify the discussion, thus far receiver synchronization remained a silent issue. The receiver synchronization scheme consists of three subsystems running in parallel, namely the acquisition circuitry, a decision directed Costas carrier recovery loop (DDC-CRL) and a complex delay lock loop (CDLL) [23]. The major advantages of this unique code locking scheme is that it eliminates the problem of arm imbalance, simplifies hardware, and improves tracking ability [23]. This is presented in Figure 2.18.

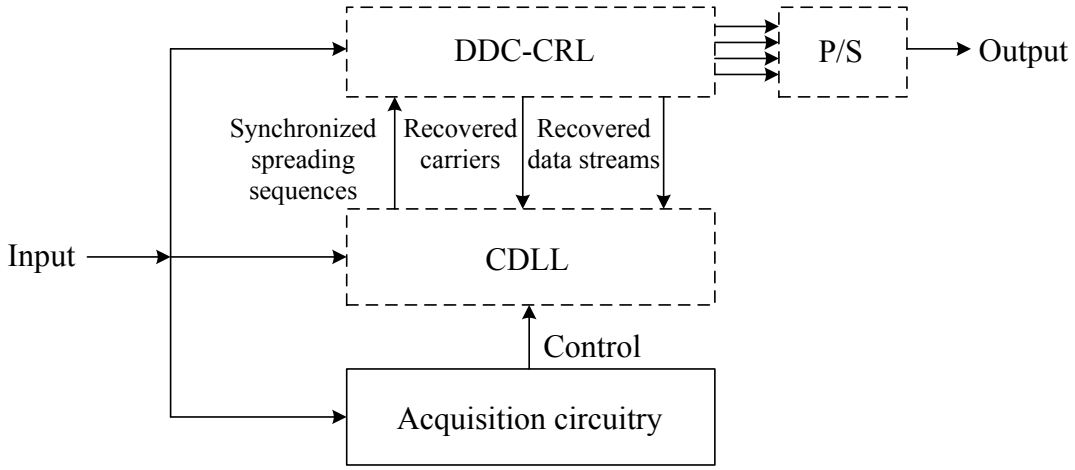


Figure 2.18.

Receiver with synchronization.

The four outputs of the DDC-CRL leading to the P/S converter are the recovered data streams. The CDLL has four inputs: the first input is the received four dimensional signal, the second input is a course clock reference control signal from the acquisition circuitry, and the third input is the recovered data stream that are outputs from the DDC-CRL. This recovered data stream serves to remove the data modulation on each of the branch signals [8], and the fourth input is the recovered carrier that is output from the DDC-CRL. The CDLL then processes these signals and outputs synchronized despreading sequences.

Figure 2.19 analyses the CDLL. FU1 serves to despread the incoming four dimensional signal. It is assumed that the incoming signal has already been band limited and amplified via a receiver front end. FU1.1 and FU1.2 serve to despread the inphase and quadrature components of the received signal, respectively. To ensure symmetry of operation, FU1.1 and FU1.2 should be matched units in terms of speed of operation and signal deterioration [8]. FU2 serves to demodulate the inphase and quadrature signals. It is assumed that the DDC-CRL has recovered the carrier signals ideally, i.e. proper demodulation and sequence matching occurs in the demodulation process. Since analogue mixing will have to be performed in FU1, mixers will be required in FU1.1 and FU1.2. FU3 serves to perform signal conditioning on the signals which includes filtering of the signal to remove unwanted signal components that may have been introduced by FU1. FU3.1 and FU3.2 are necessary functions in order to achieve the required signal conditioning. FU4 serves to modulate the incoming inphase and quadrature carriers with the recovered data that is output from the DDC-CRL. It is assumed that this recovered data is such that its characteristics are similar to the original parallel to serially converted data from the

transmitter. FU5 serves to combine the modulated inphase and quadrature components. FU6 serves to perform signal conditioning in the form of loop filtering. This is done to minimize the error signal in order to achieve minimum timing error between the incoming CSS and the locally generated despreading sequence [24]. After conditioning, FU6 outputs the recovered synchronized despreading sequence as well as a difference despreading sequence (IF6). These difference despreading sequences are equal to the difference between a late and an early replica of the recovered synchronized despreading sequence [8], and serves to increase the linear range of the S-curve[1] for improved code locking.

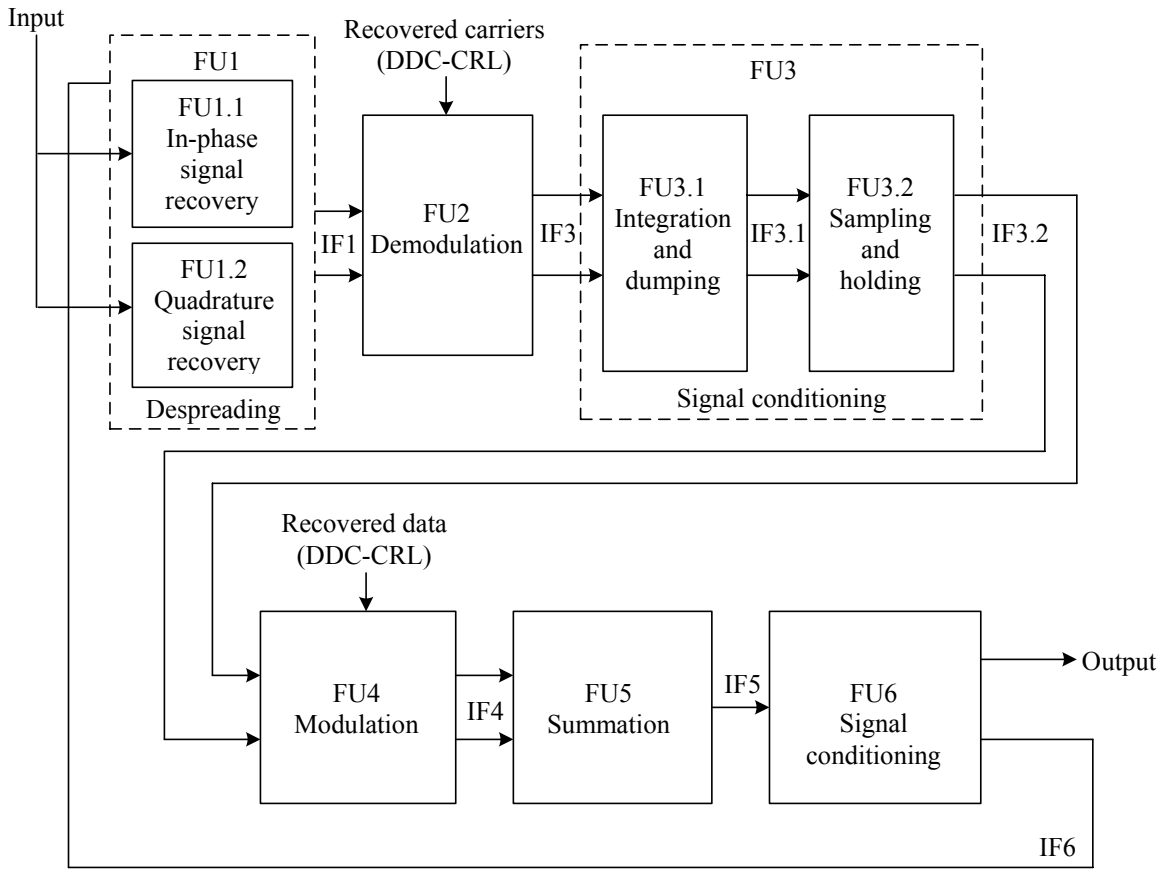


Figure 2.19.

Functional analysis of the CDLL.

The DDC-CRL and the CDLL operate as one integrated recovery loop. This combined structure recovers the quadrature carriers, synchronises the locally generated despreading sequences and recovers the different data streams [8]. Figure 2.20 depicts the DDC-CRL. The CDLL has been adapted from [27].

[1] The normalised CDLL error function, otherwise known as the S-curve [23]. Increasing the linear range of the S-curve results in an increased code locking range and therefore a decreased code timing error.

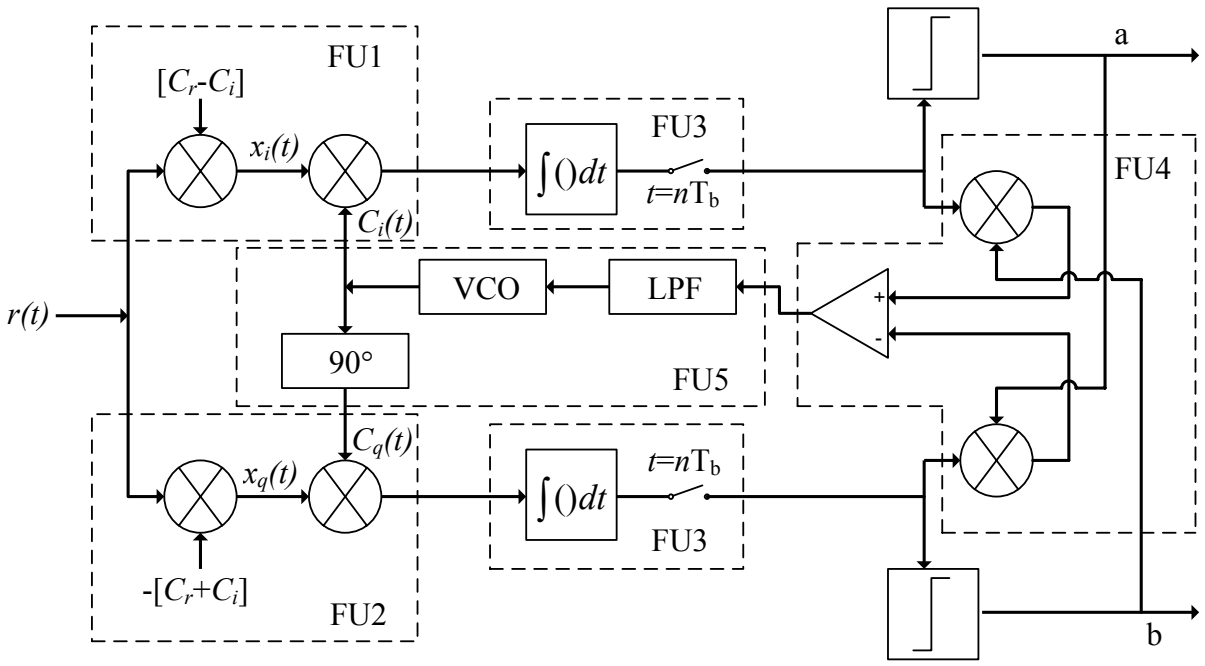


Figure 2.20.
Functional analysis of the DDC-CRL [73].

FU1 performs inphase signal recovery. Similarly, FU2 performs quadrature signal recovery. Both these functional units operate in the same way but use a different set or combination of spreading sequences. Spreading at the transmitter is performed by multiplying each bit with an appropriate spreading sequence, and despreading is performed in the same manner. Modulation at the transmitter is performed by multiplying the desired signal by a carrier at the desired frequency. Demodulation is performed in the same way, provided that the carrier frequency is at the same frequency as the received signal.

Analogue multiplication is performed using mixers. Mixers in CMOS can be implemented as current controlled current sources. Gilbert mixers [25] are most suited for the demodulation and despreading operations that need to be performed. Gilbert mixers have good linearity across their range of operation and a single design is suitable for both high and low frequency operation. Differential inputs and outputs allow Gilbert mixers to be cascaded with ease, and without any need for buffering between mixers.

Demodulation produces a term at twice the carrier frequency as well as at baseband. The double carrier frequency term must be removed since it can be seen as high frequency noise in the time domain. The high frequency terms complicate bit detection by being seen as noise spikes by the bit detector (a simple comparator), causing the bit detector to output

a series of pulses or even an incorrect value. The integrate and dump operation performed by FU3 removes the unwanted high frequency terms and also produces a distinct triangular wave that allows for easy bit detection without errors. Figure 2.21 demonstrates this operation.

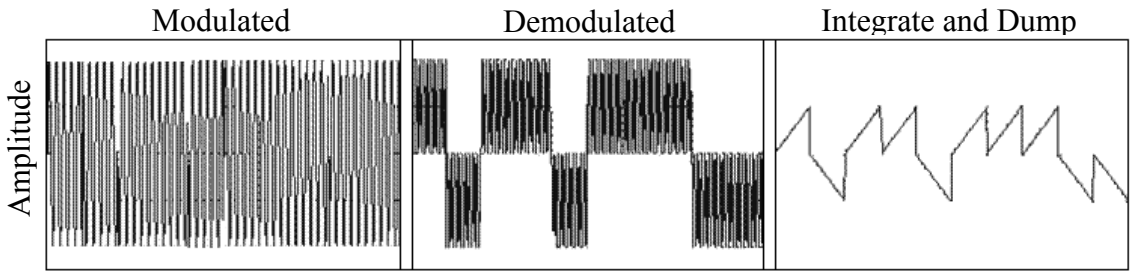


Figure 2.21.

Demodulation of a signal to illustrate the integrate and dump operation. The modulation scheme used is binary phase shift keying (BPSK).

Integration in CMOS can be performed using either inverting or non-inverting active integrators. Passive integrators offer no gain and were not considered. An integrate and dump operation is performed by rapidly discharging the capacitor used in the integrator at the end of every bit interval.

FU4 is the recovered signal comparison unit. The unit consists of a phase comparator which produces an error signal if a phase difference is detected between the two branches of the DDC-CRL. Multipliers generate an error signal based on phase difference between the two branches. Inputs to the multipliers are taken from before bit detection and after bit detection. The difference of the products generates a positive or negative error signal.

The magnitude of this error signal is proportional to the degree of phase or frequency error compared to the local reference. The sign of the error signal indicates whether the difference is positive or negative and is determined by the phase difference between branches. The phase detector can either be digital or analogue. A digital solution makes use of exclusive OR (XOR) gates and generates a square wave where the duty cycle is a function of the phase and frequency. Analogue mixers can again be used for the multiply operation required, but the digital nature of both of the input signals (from the comparators) allows for simpler multipliers to be used.

FU5 generates the carrier reference required to ensure that the carrier used to demodulate the input signal is at the same frequency as the carrier of the input. The error signal produced by the phase detector of FU4 is passed through a low pass filter to remove the AC component and pass the DC component. The filtered error signal is then passed onto a voltage controller oscillator (VCO). The VCO oscillates at a free running frequency that can increase or decrease based on the magnitude and sign of the filtered error signal.

VCOs can be implemented by changing the resonance frequency of a LC tank. Using a varactor (variable capacitor effect) to either replace the capacitor in the tank or to vary the load capacitance seen by the tank is a simple and effective technique to implement a VCO. The 90° phase shift can be implemented in one of three ways. The first is to use an all pass filter with an approximate 90° phase shift in the region of 2.4 GHz. The second is to use Havens technique [25]. The third technique is to design a VCO with quadrature outputs.

In summary, if the phase detector detects a change in phase or frequency an error signal is passed to the VCO, which will increase or decrease the frequency at which it is oscillating. In this way, a change in frequency at the input of the DDC-CRL propagates through both branches to the phase detector. The VCO then compensates for this change.

2.3 Developing the system specifications

2.3.1. System inputs

Figure 2.17 shows the overall inputs and outputs of the system. The inputs to the system consist of the data signal inputs and the sequence inputs. The primary input to the transmitter (FU1) is a binary data signal running at a bit rate proportional to the RF transmission bandwidth divided by the CSS length. The secondary input to the transmitter (FU1) is a CSS of the chosen length. In order to transmit data at a high rate the sequence length should be as small as possible, but in order to keep the quality of the transmission the sequence should not be shorter than a certain length. The sequence length of 11 is used as the lower boundary to satisfy both conditions. The CSS used are the families of the GCL sequences. These sequences are the intellectual property of the University of Pretoria [8].

The primary input to the receiver is the noise corrupted transmitted signal (FU4) running at the rate of 20 Mchips/s, which corresponds to the bandwidth of 20 MHz. Complex spreading sequences form the secondary input to the receiver at FU5.

2.3.2 System outputs

As shown in Figure 2.17, the receiver and transmitter have one output each. The transmitter output (FU3) is an amplified signal with the spread spectrum running at the chip rate specified above. The receiver output (FU7) is a recovered data signal of the same characteristics as those of the transmitter input.

2.3.3 Major subsystem specifications

The subsystems involved are shown in Figures 2.17, 2.19, and 2.20.

The system of Figure 2.17 uses spread Q^2PSK as the modulation scheme (i.e. FU2 and FU6, in Figures 2.13 and 2.16, respectively). As discussed previously, this scheme accommodates a data rate four times higher than in the case of the conventional BPSK and is sufficient to carry all the required information.

The following is the list of additional specifications (referring to Figure 2.17).

- Eight samples per chip are used as this is sufficient for sequence processing.
- The resulting sampling frequency is 160 Msamples/s. This figure is equal to the chip rate times the number of samples.
- The transmitter power is chosen as 17.5 dBm (FU3). This is a typical figure for DSSS transmitters.
- Receiver sensitivity of less than -91 dBm is chosen (FU4). This is also a typical figure.
- The chosen bit-error rate (BER) of the system is less than 10^{-3} (FU4). With this BER, simple error-correction techniques will be sufficient for the improvement of this figure to less than 10^{-6}.
- Integration and dump filtering is necessary for the quality filtering in FU7.

The specifications of the CDLL shown in Figure 2.19 are listed below.

- The received signal in FU1 must have maximum peak amplitude of magnitude 3.3 V as prescribed by the AMS process [15].
- The difference despreading sequences used by FU1.1 and FU1.2 are from the family of generalised chirp like (GCL) sequences.
- To ensure minimal interference between channels, the internal bandwidth of FU1.1 and FU1.2 is restricted to 20 MHz [26].
- The modulation scheme employed in FU2 and FU4 is Q^2PSK.

- FU3 eliminates higher-order and even harmonics from the despreaded demodulated signal.
- Analogue summation takes place in FU5.
- The recovered synchronized data provided by FU6 must have at most, a peak amplitude of 3.3 V as prescribed by the CMOS process.
- The recovered CSS which are output from FU6 should have the following two properties, a mean time to lose lock (MTLL) of at least 1 µs which is a general DLL specification, and a root mean square (rms) tracking jitter of at most 500 ps.
- The data must run at a chip rate of 5 Mchips/s since B_{spread} = 5 MHz [12].
- The sampling rate is determined by the specifications chosen above and by calculation f_{sample} is found to be 160 Msamples/s [11].
- The number of samples/chip is determined by the specifications chosen above and by calculation S is found to be 8 samples/chip which is sufficient for digital processing.
- The transmission bandwidth must be 10/12.5 MHz double side band (DSB) and 5/6.25 MHz single side band (SSB) [12].

The specifications of the DDC-CRL shown in Figure 2.20 are listed below. Specifications were chosen with reference to the IEEE 802.11 standard.

- The CSS used by FU1 and FU2 are from the family of generalised chirp like (GCL) sequences with selectable length.
- The band of operation of FU1 and FU2 should accommodate typical channel widths specified by the IEEE 802.11 standard. The IEEE 802.11 standard has numerous channels of width 5 MHz assigned within its bands of operation, thus a system based on this standard cannot assign more than 20 MHz of bandwidth to a channel. For this reason the internal CMOS operational bandwidth of the DDC-CRL is restricted to 20 MHz. Another benefit of this bandwidth selection is that it prevents the DDC-CRL from acting on adjacent channels.
- The carrier reference generated by FU5 must be able to vary across the range of the channel width to offer a large tracking range, thus has a limit of ± 10 MHz around the centre frequency of operation to prevent the reference frequency from drifting into adjacent bands.
- The centre frequency of operation of the system (FU1, FU2 and FU5) must be in the range of 2.4 GHz to 2.4835 GHz, which is one of the industrial, scientific and medical (ISM) bands specified by the IEEE 802.11 standard [27].

- The BER of the output at a bit rate of 1 Mbps should be no more than 10^{-3}. The BER can be improved by using error correcting codes [23]. However, such codes are considered to be outside the scope of this thesis.
- The maximum bit rate is dependent on the length of the CSS used and the modulation scheme employed, both of which are selectable. The maximum spreading channel width of 5 MHz also limits the bit rate.

2.4 System level simulation

2.4.1 BPSK based system modelling and simulation

SIMULINK was used to model the system to gain a better understanding of the operation of a DSSS transceiver. The total mathematical system diagram is shown in Figure 2.22. The diagram indicates the positioning of the transmitter and receiver in an ideal DSSS system.

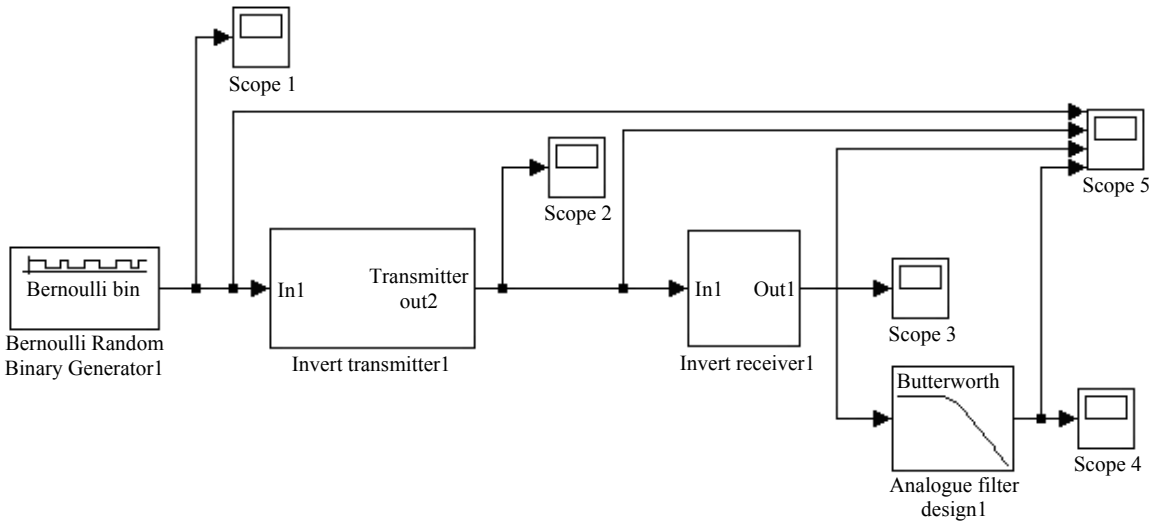


Figure 2.22.
System diagram indicating transmitter and receiver modules.

The system input is shown in Figure 2.23, and the system output is shown in Figure 2.24. By zooming into the Figures 2.23 and 2.24, as expected (Section 2.2.1), the output is a delayed version of the input (delayed by one chip).

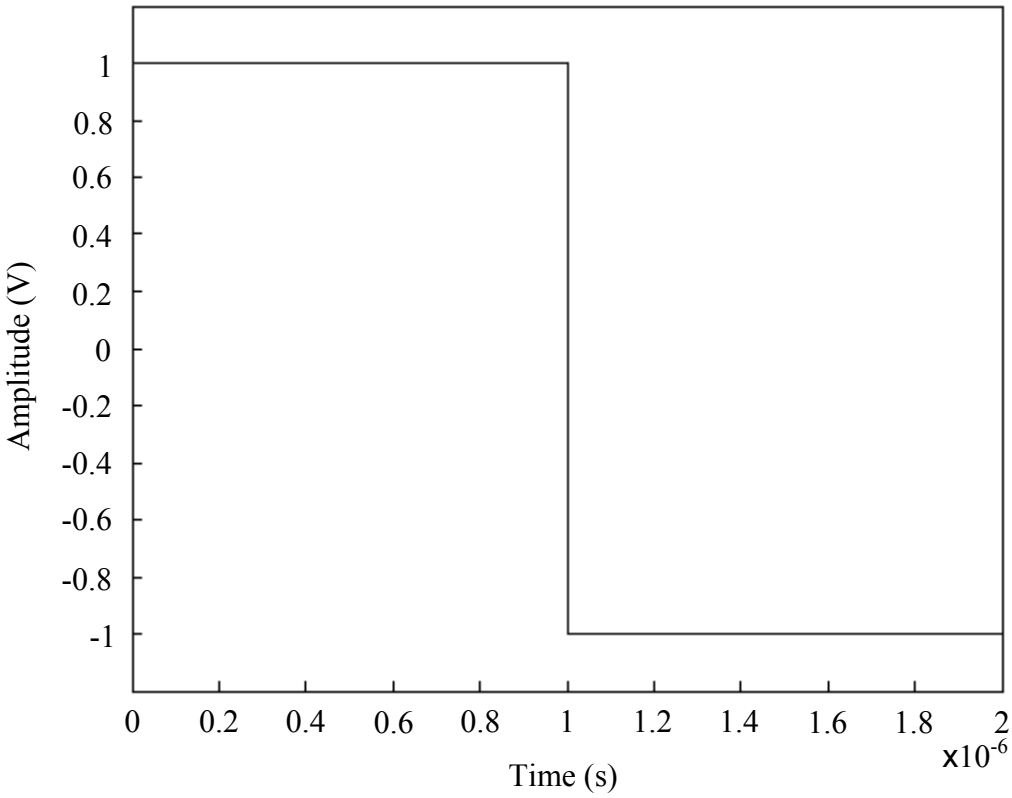


Figure 2.23.

Mathematical system input signal.

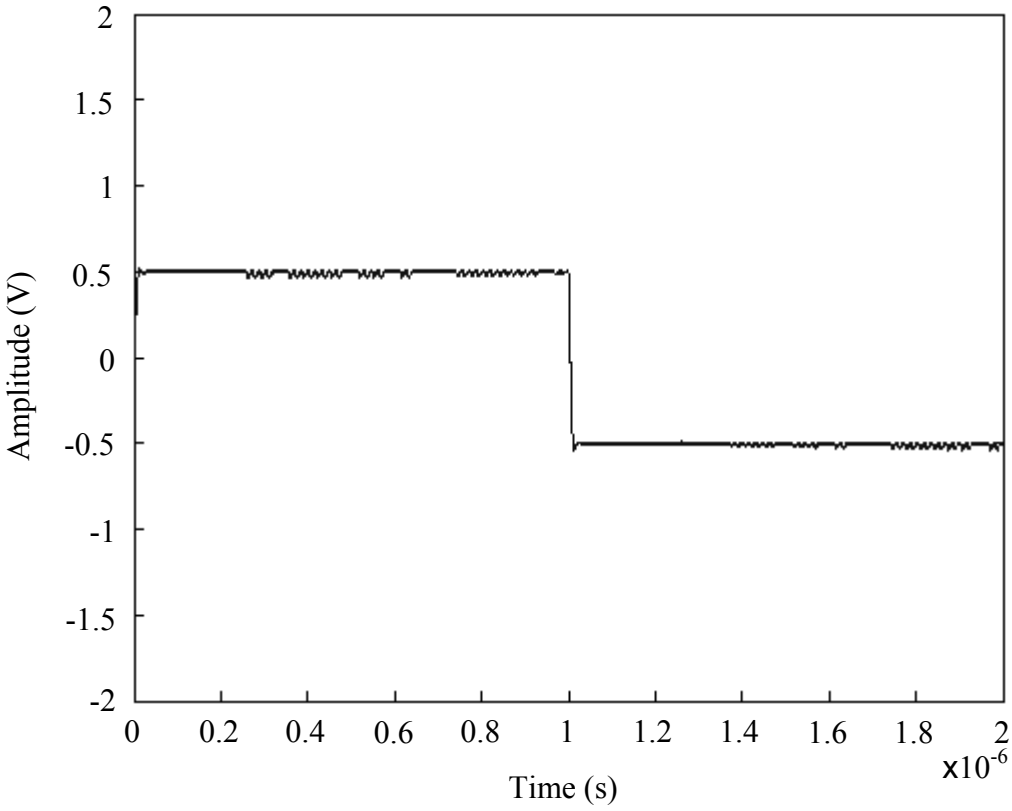


Figure 2.24.

Mathematical system output signal. A delay of 32 ns corresponds to one chip.

Figure 2.25 shows the mathematical transmitter module.

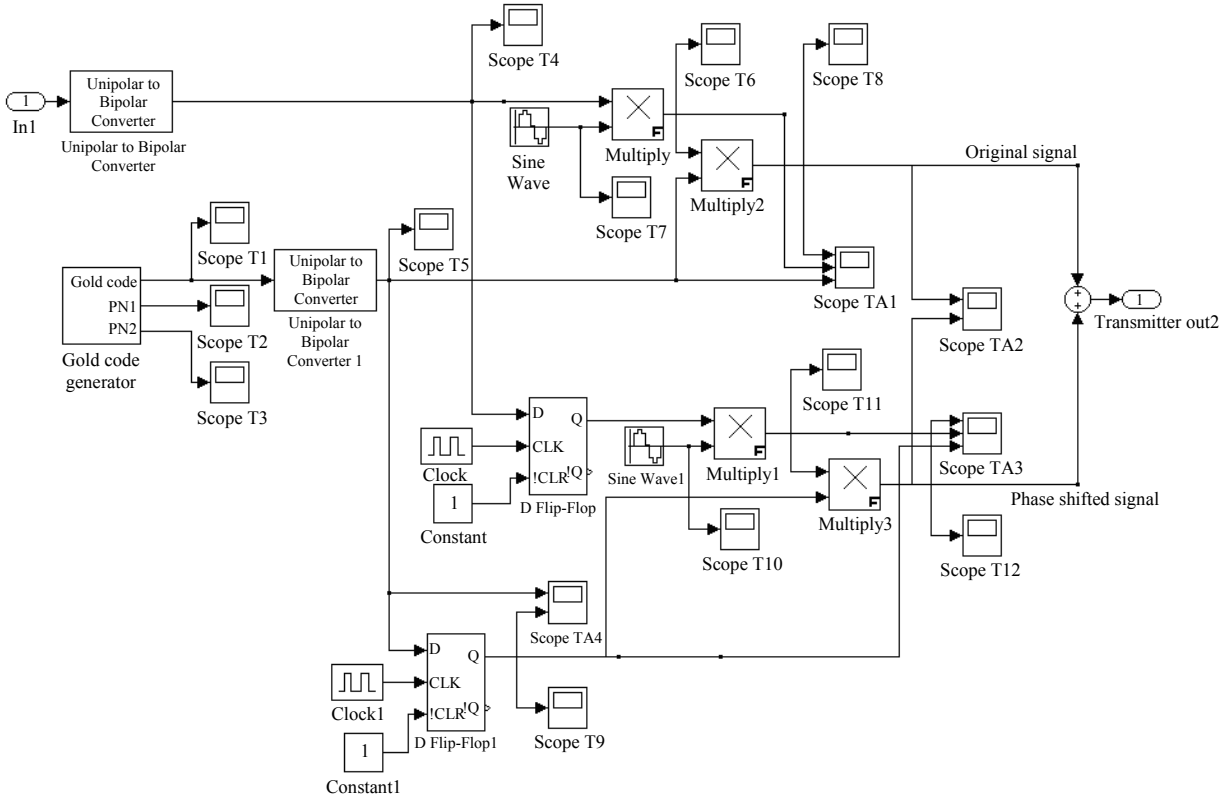


Figure 2.25.

Detailed system diagram for the transmitter.

The PN sequence outputs are shown in the Figures 2.26 and 2.27, respectively. These are then XOR'ed to produce a Gold sequence as shown in Figure 2.28.

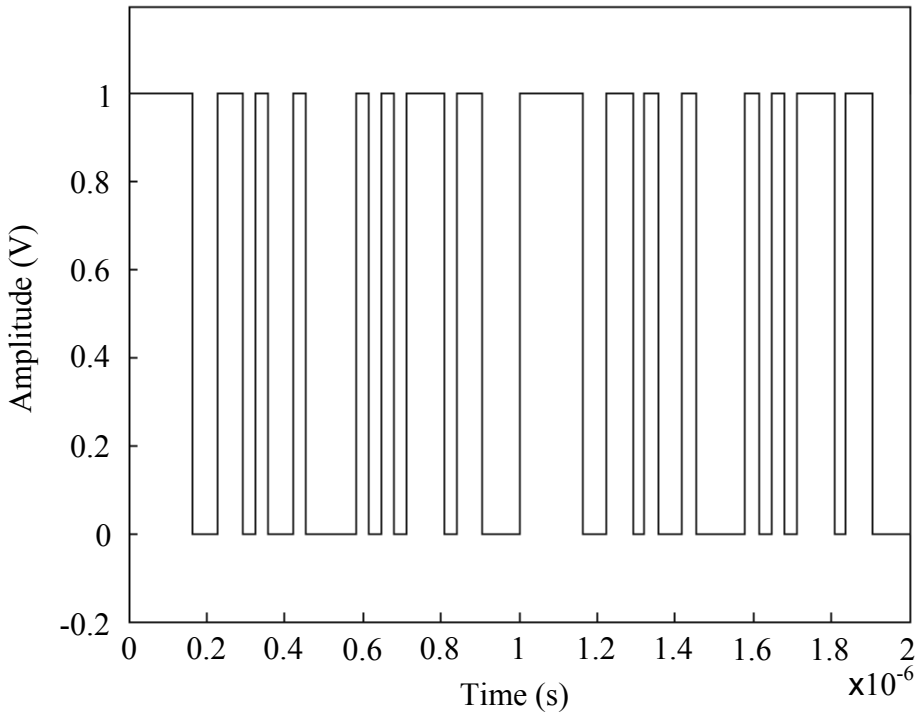


Figure 2.26.

PN sequence A output.

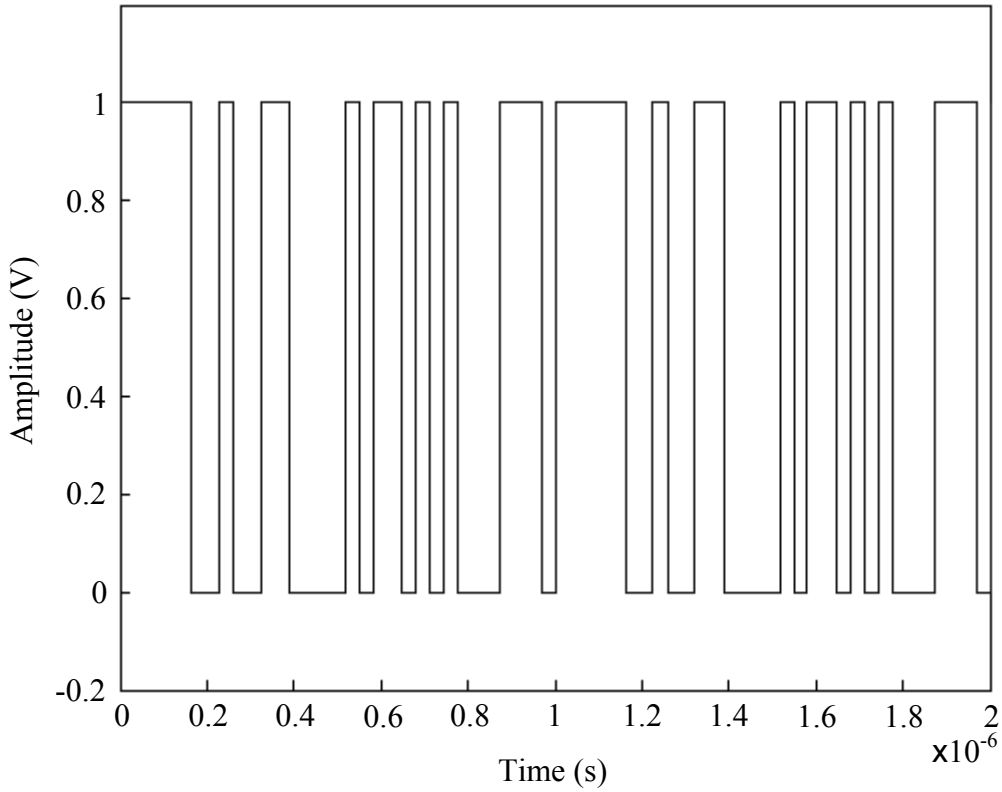


Figure 2.27.

PN sequence B output.

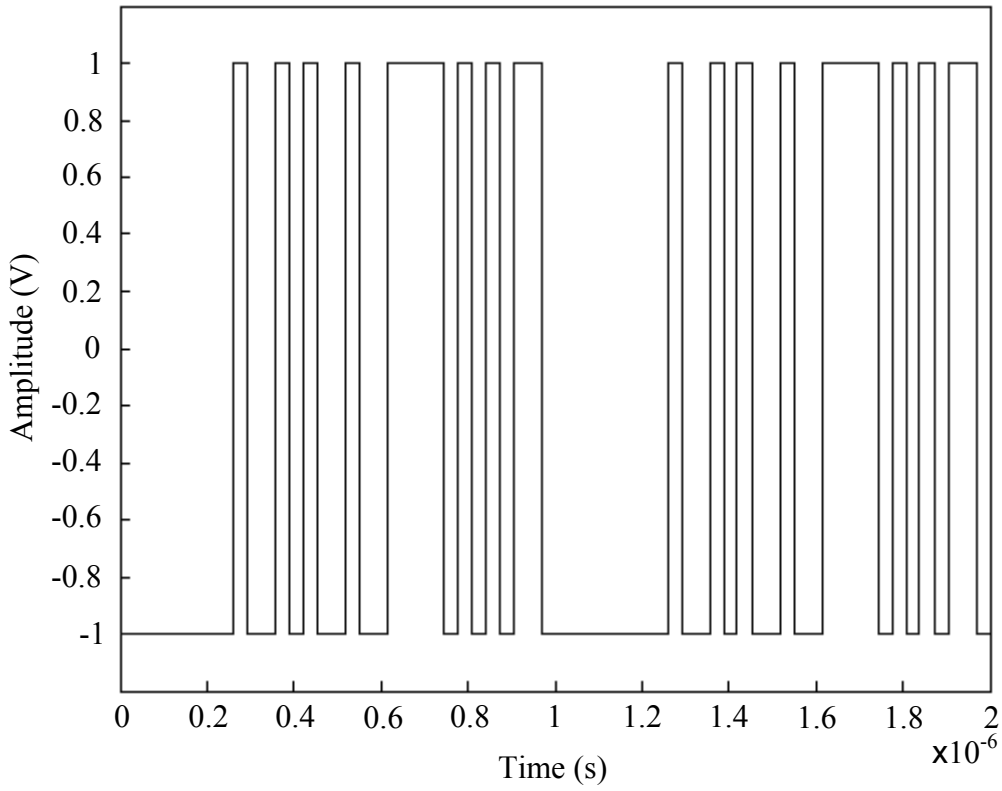


Figure 2.28.

XOR of PN sequence A output with PN sequence B output to form a Gold code.

This signal is then XOR'd (essentially multiplied) with the RF modulated data signal which is shown in Figure 2.29. The 180 phase shift at the bit change can be seen.

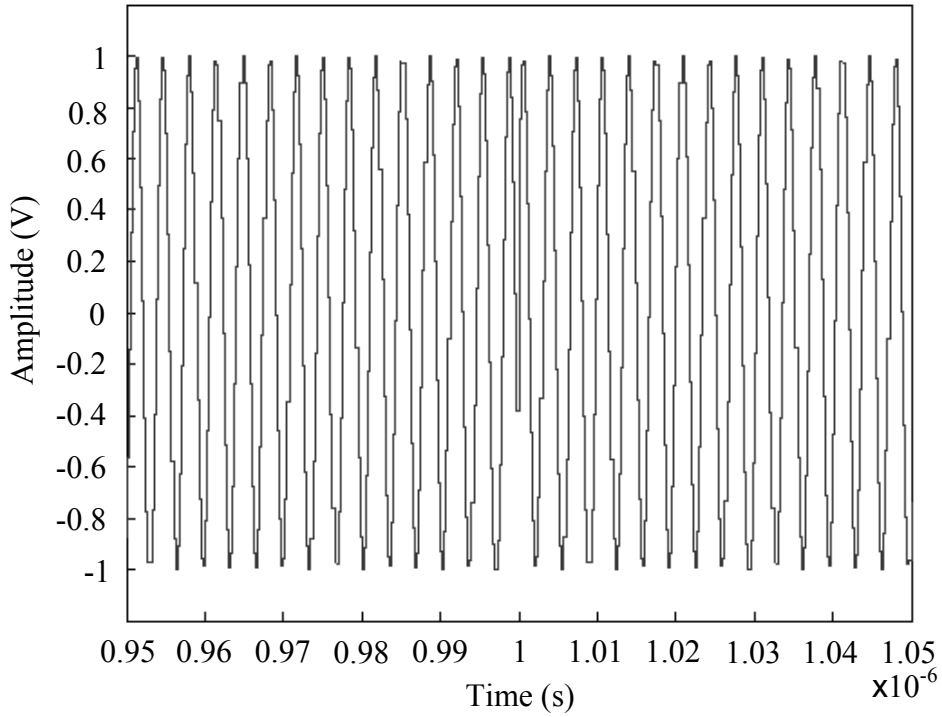


Figure 2.29.

Modulated data signal (1.85125 GHz).

The result of XORing the signal in Figure 2.28 with the Gold sequence can be seen in Figure 2.30.

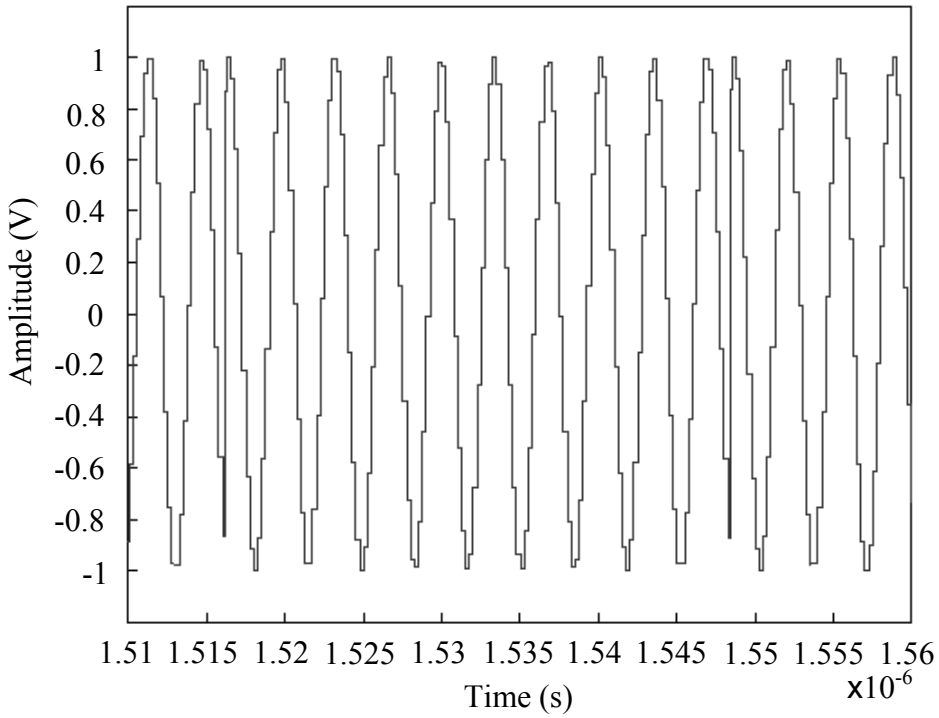


Figure 2.30.

Spreaded data signal.

Inphase and quadrature versions of both the LO and the Gold code are mathematically generated. These are then treated in a similar manner, in order to obtain inphase and quadrature components of this signal. The two similarly spreaded signals are then summed to produce a transmitter output signal at a single frequency. This signal is shown in Figure 2.31.

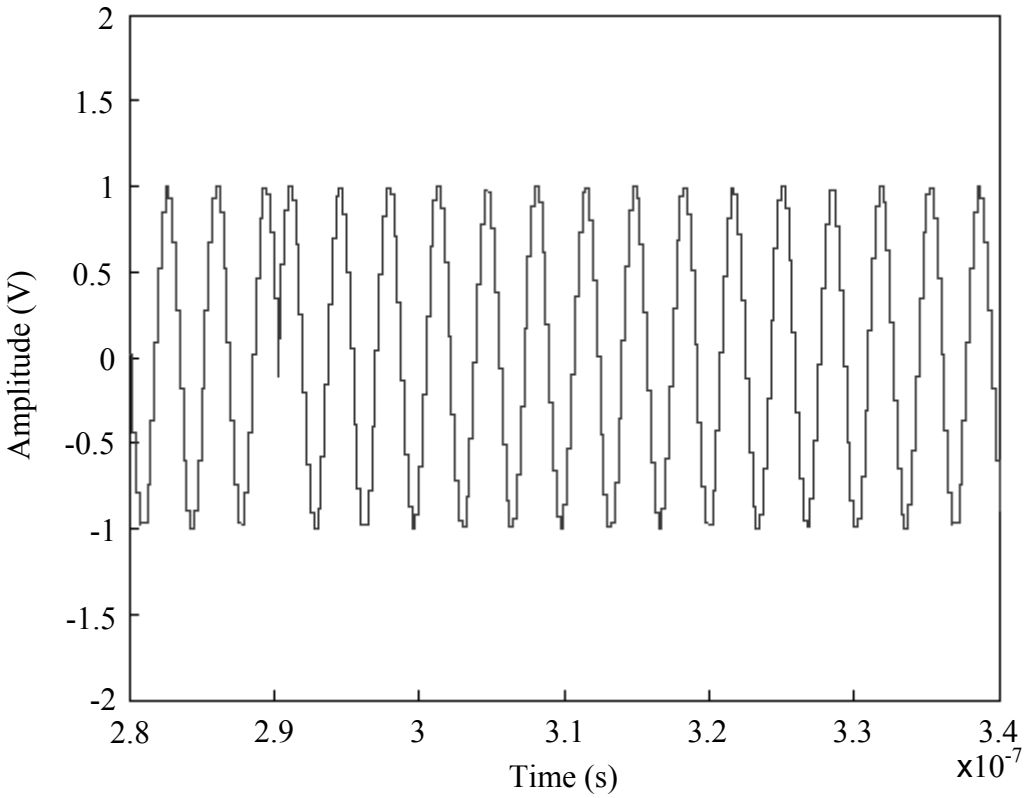


Figure 2.31.

A portion of the mathematical system transmission signal.

Figure 2.32 shows the mathematical model of the receiver module. The original signal is recovered after despreading and demodulation.

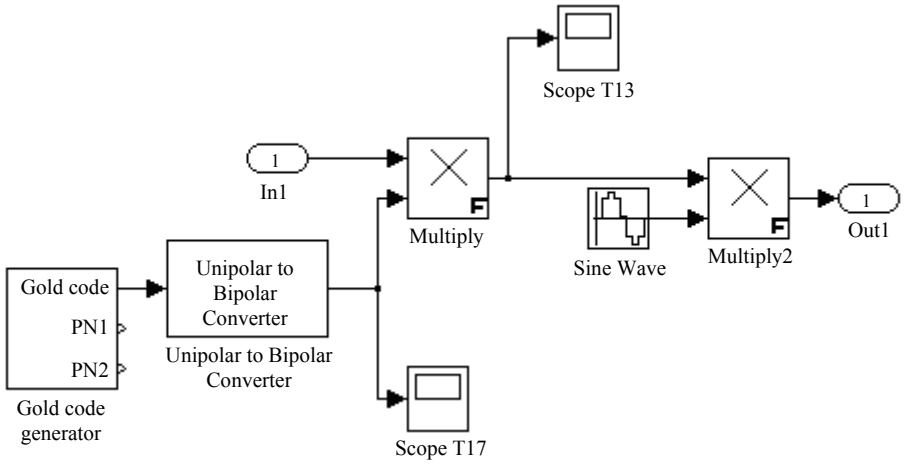


Figure 2.32.

Detailed system diagram for the receiver.

Figure 2.33 shows the signal that is generated when multiplying the Gold code with the received signal. This is also termed the despreaded signal.

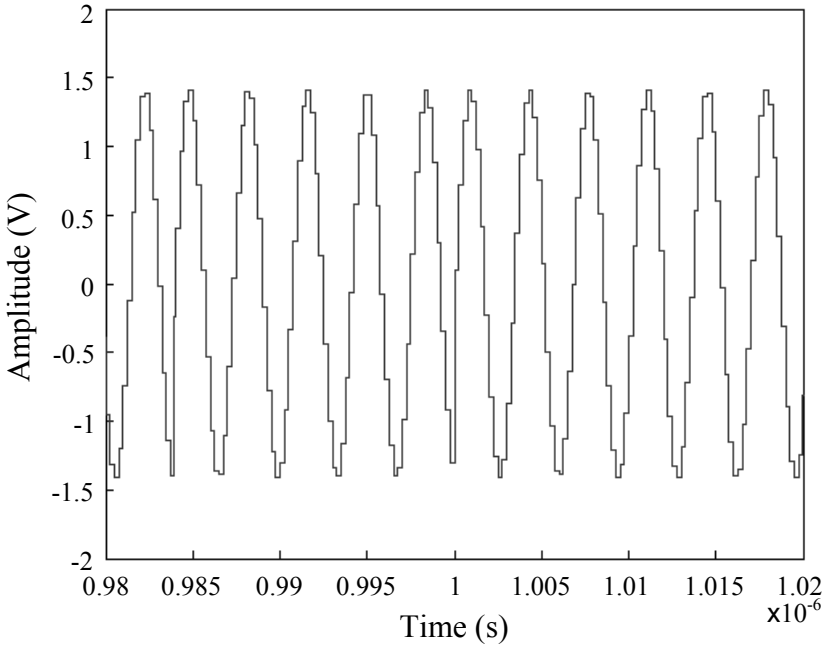


Figure 2.33.

Despreaded signal.

The despreaded signal of Figure 2.33 is then demodulated using the same carrier frequency as that which was used at the transmitter (for a test case, 1.85125 GHz is used). The resulting signal is shown in Figure 2.34. This signal should resemble the data signal, but has a high frequency component that must still be filtered out.

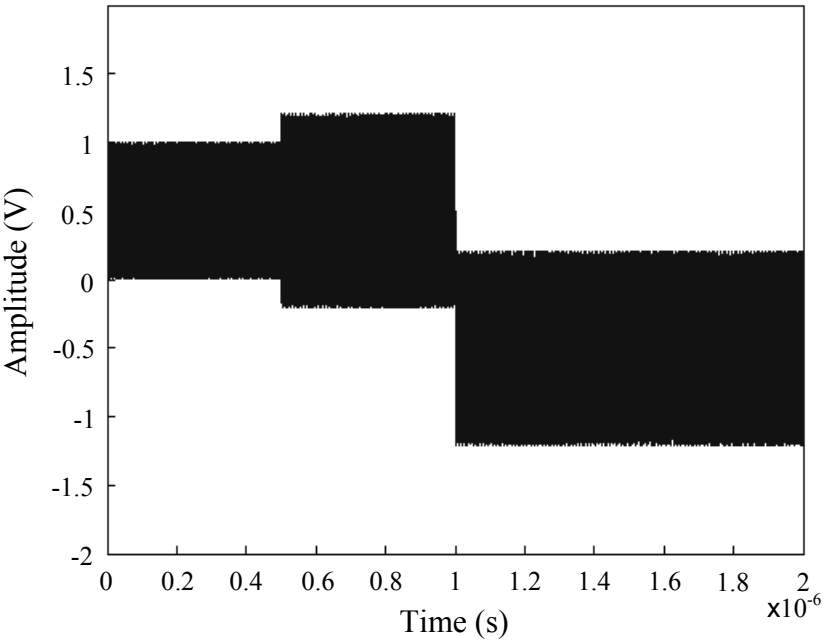


Figure 2.34.

Recovered, unfiltered signal.

This signal was then filtered using an ideal Butterworth filter. The filtered signal was shown previously in Figure 2.24, and thus it is clear that the recovered output signal resembles the original input signal (Figure 2.23).

2.4.2 Q^{2}PSK based system modelling and simulation

The operation of this system can be summarized by

$$u(t) = a(t)C_r \cos\omega_c t + a(t)C_i \cos\omega_c t + a(t)C_r \sin\omega_c t + a(t)C_i \sin\omega_c t \quad (2.17)$$

$$u(t) = a_1(t)C_r \cos\omega_c t + a_2(t)C_i \cos\omega_c t + a_3(t)C_r \sin\omega_c t + a_4(t)C_i \sin\omega_c t \quad (2.18)$$

These two equations are valid for the transmitter if it operates in balanced and unbalanced mode, respectively. $u(t)$ is the transmitted signal, $a(t)$ is the digital data with NRZ logic levels, and ω_c is the carrier frequency. These equations can be expanded to suit the receiver. The following slightly more complicated equations result and they show how each bit can be recovered from the transmitted signal:

$$a_1(t) = \begin{cases} 1,\ T_b < t < 2T_b \text{ iff } \left\{ \int_0^{T_b} \left[u(t)C_r \cos\omega_c t \otimes \Im^{-1}\prod\left(\frac{f}{BW}\right)\right] dt \right\}\Big|_{T_b} > 0 \\ -1, T_b < t < 2T_b, \text{ otherwise} \end{cases} \quad (2.19)$$

$$a_2(t) = \begin{cases} 1,\ T_b < t < 2T_b \text{ iff } \left\{ \int_0^{T_b} \left[u(t)C_i \cos\omega_c t \otimes \Im^{-1}\prod\left(\frac{f}{BW}\right)\right] dt \right\}\Big|_{T_b} > 0 \\ -1, T_b < t < 2T_b, \text{ otherwise} \end{cases} \quad (2.20)$$

$$a_2(t) = \begin{cases} 1,\ T_b < t < 2T_b \text{ iff } \left\{ \int_0^{T_b} \left[u(t)C_r \sin\omega_c t \otimes \Im^{-1}\prod\left(\frac{f}{BW}\right)\right] dt \right\}\Big|_{T_b} > 0 \\ -1, T_b < t < 2T_b, \text{ otherwise} \end{cases} \quad (2.21)$$

$$a_3(t) = \begin{cases} 1,\ T_b < t < 2T_b \text{ iff } \left\{ \int_0^{T_b} \left[u(t)C_i \sin\omega_c t \otimes \Im^{-1}\prod\left(\frac{f}{BW}\right)\right] dt \right\}\Big|_{T_b} > 0 \\ -1, T_b < t < 2T_b, \text{ otherwise} \end{cases} \quad (2.22)$$

where BW is transmission bandwidth. Equations (2.19) to (2.22) hold for the unbalanced configuration, while for the balanced configuration it is to be expected that $a(t) = a_1(t) = a_2(t) = a_3(t) = a_4(t)$.

The implementation of a DSSS transceiver system essentially scales down to implementing the following mathematical equations:

$$u(t) = a(t)C_r \cos\omega_c t + a(t)C_i \cos\omega_c t + a(t)C_r \sin\omega_c t + a(t)C_i \sin\omega_c t\,, \tag{2.23}$$

$$u(t) = a_1(t)C_r \cos\omega_c t + a_2(t)C_i \cos\omega_c t + a_3(t)C_r \sin\omega_c t + a_4(t)C_i \sin\omega_c t\,, \tag{2.24}$$

which are valid for the transmitter, and are slightly more complicated for the receiver, in a manner of the block diagram showed in Figure 2.18. This block diagram is modelled in Simulink. The developed model of the transmitter is shown in Figure 2.35, while the models of the noisy and fading channel [11] as well as the receiver are shown in Figure 2.36 and Figure 2.37, respectively.

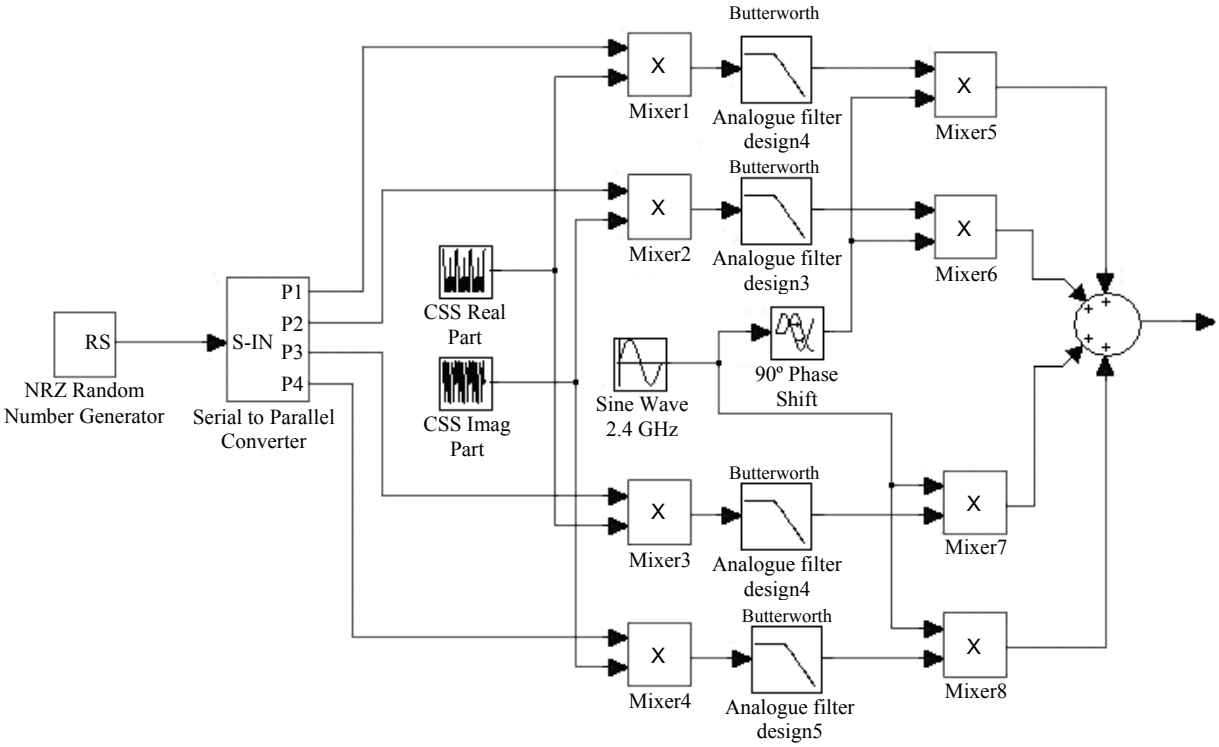


Figure 2.35.

Simulink model of the proposed transmitter.

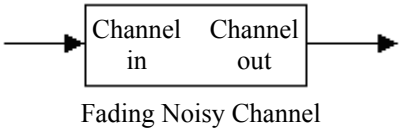


Figure 2.36.

Simulink model of a noisy fading channel.

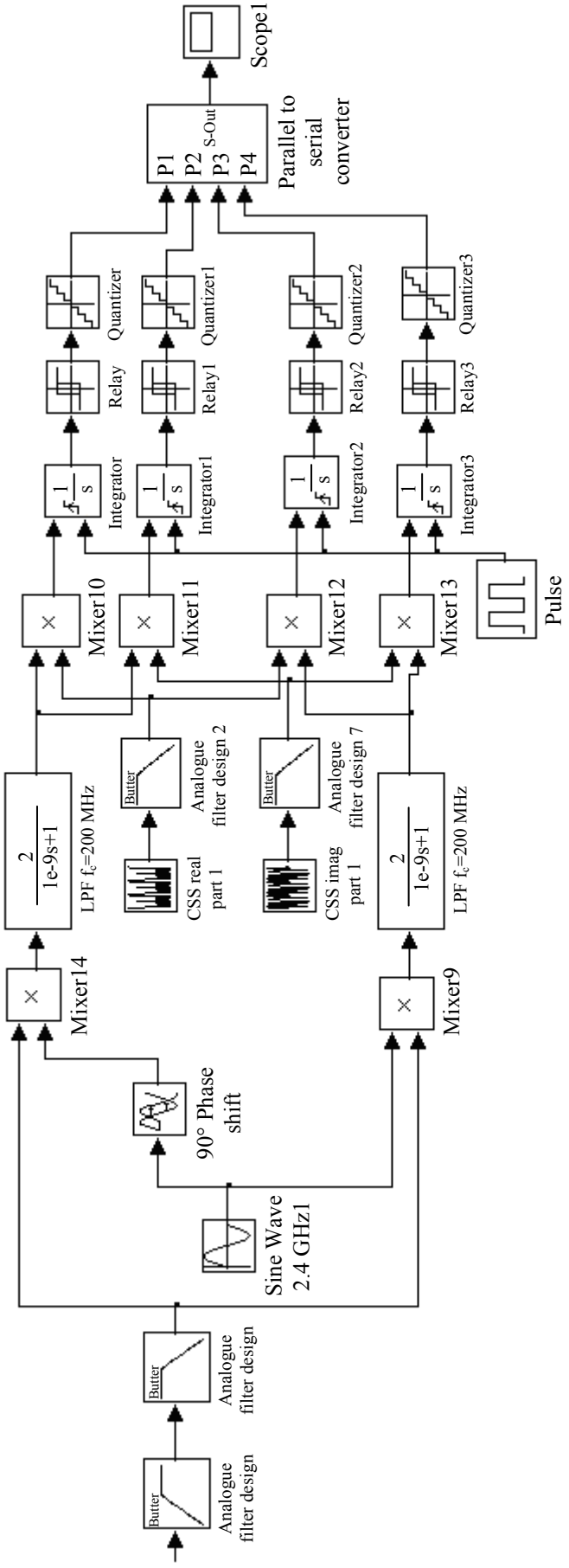


Figure 2.37.

Simulink model of the proposed receiver. CSS real & imaginary parts provided [8].

Simulation results

The shape of the signal after each stage of processing in the transmitter (Figure 2.35) and receiver (Figure 2.36), as well as the shape of the signal after the channel (Figure 2.37) are presented below. Table 2.1 shows specifications of the three signals used for simulation purposes. The simulation is run for 40 bit repetitions (6.5 µs).

Signal	**Parameter**	**Specification**
PRBS data source	Bit length	0.1625 µs
Spreading sequence	Length	13
Spreading sequence	Duration of one repetition	0.65 µs
Spreading sequence	Sampling rate	160 Msamples/s
Clock	Period	0.65 µs

Table 2.1.

Parameters of the test signals that were used to obtain Simulink results for the transceiver.

The results are organised in the following way: The CSS real and imaginary parts are shown in Figure 2.38 and Figure 2.39. The test PRBS data stream is shown in Figure 2.40. Time and, where applicable, frequency domain waveforms after propagation of the signal through the whole system are shown in Figure 2.40 through Figure 2.52, concluding with the final, recovered data signal. In the subsystems where signals are processed in four branches only the simulation of the top branch is given. No gain losses are assumed in simulation.

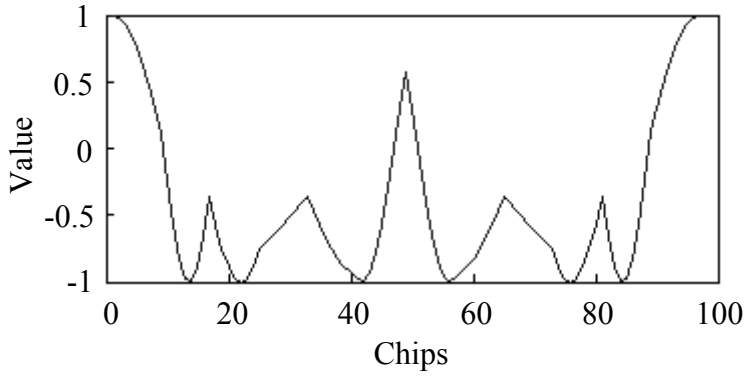


Figure 2.38.

Real part of the sequence of length 13 used in the system.

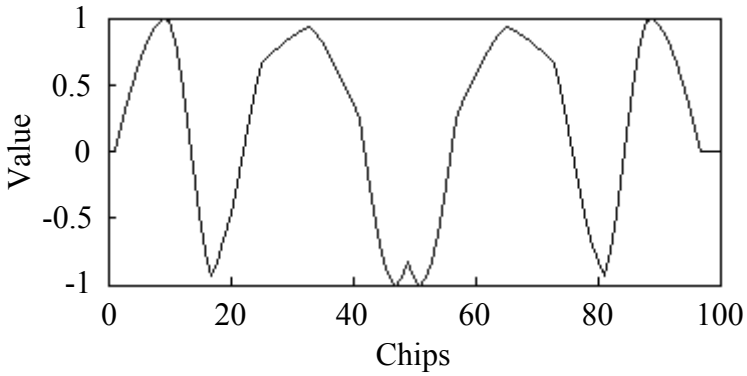


Figure 2.39.

Imaginary part of the sequence of length 13 used in the system.

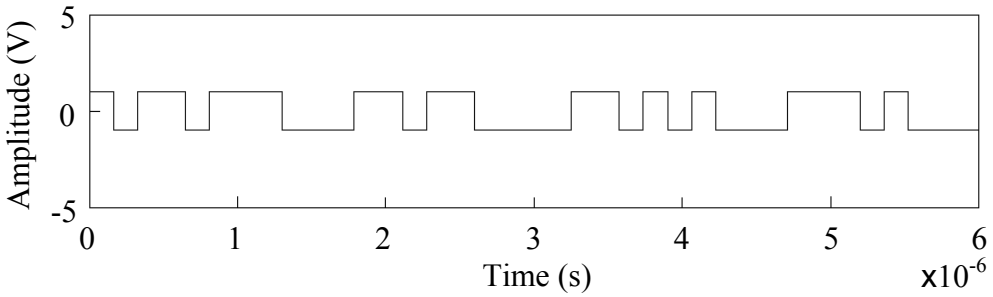


Figure 2.40.

Time-domain simulation trace of the PRBS data stream used at the input of the transmitter.

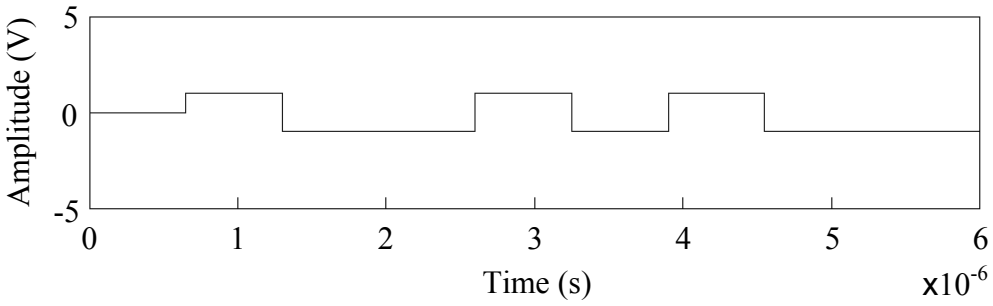


Figure 2.41.

Time-domain simulation trace of the data stream in the top branch of the transmitter after parallel-to-serial conversion.

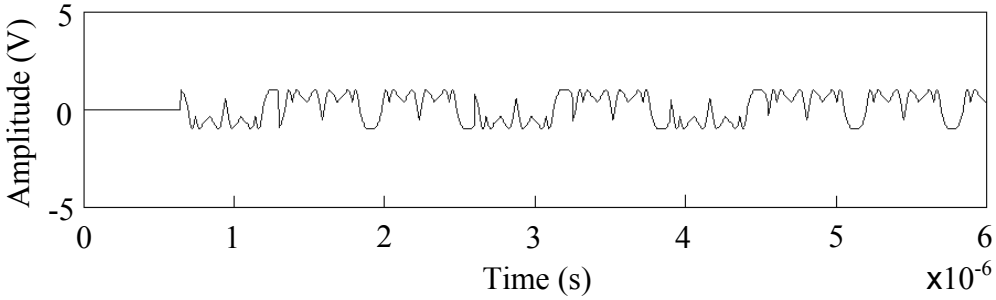


Figure 2.42.

Time-domain simulation trace of the data stream in the top branch of the transmitter after it has been spread with the real part of the CSS.

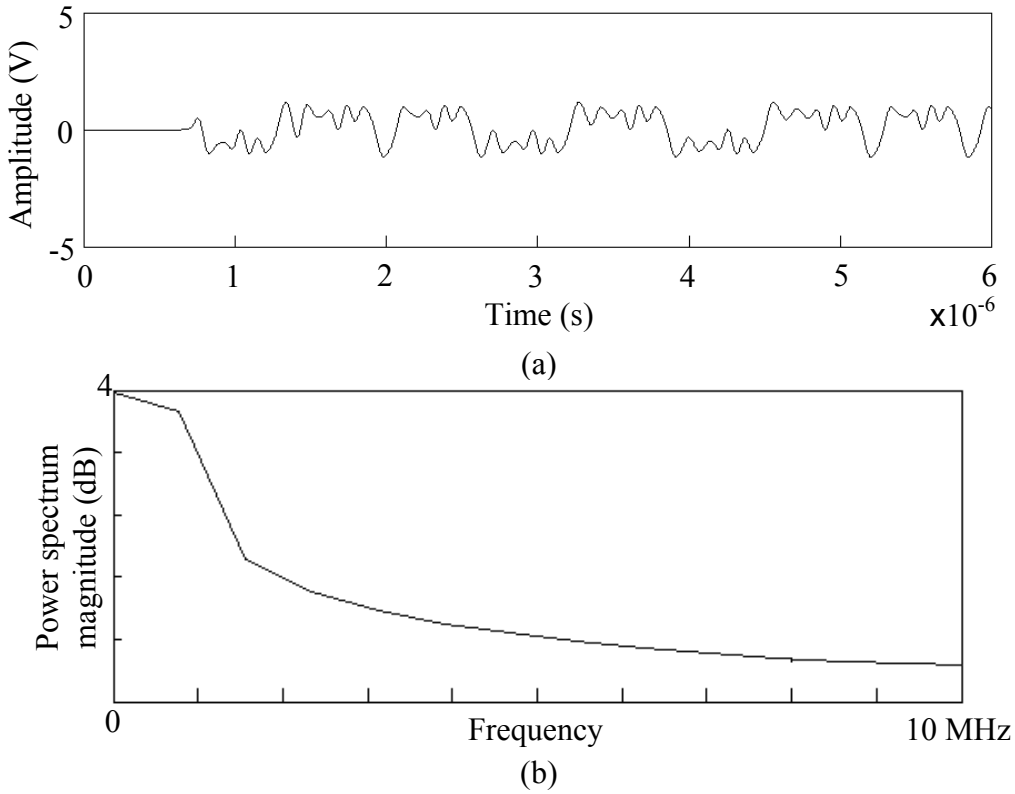


Figure 2.43.

(a) Time-domain and (b) frequency-domain simulation traces of the data stream in the top branch of the transmitter after it has been filtered.

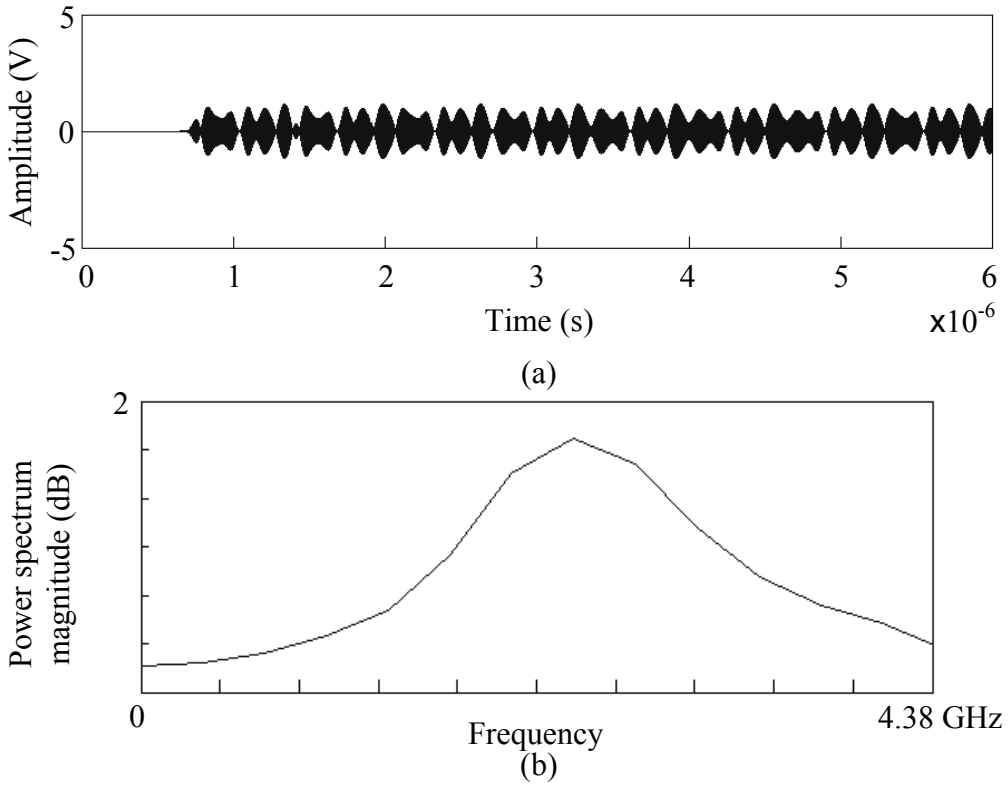


Figure 2.44.

(a) Time-domain and (b) Frequency domain simulation traces of the signal in the top branch of the transmitter after it has been modulated onto a 2.4 GHz carrier.

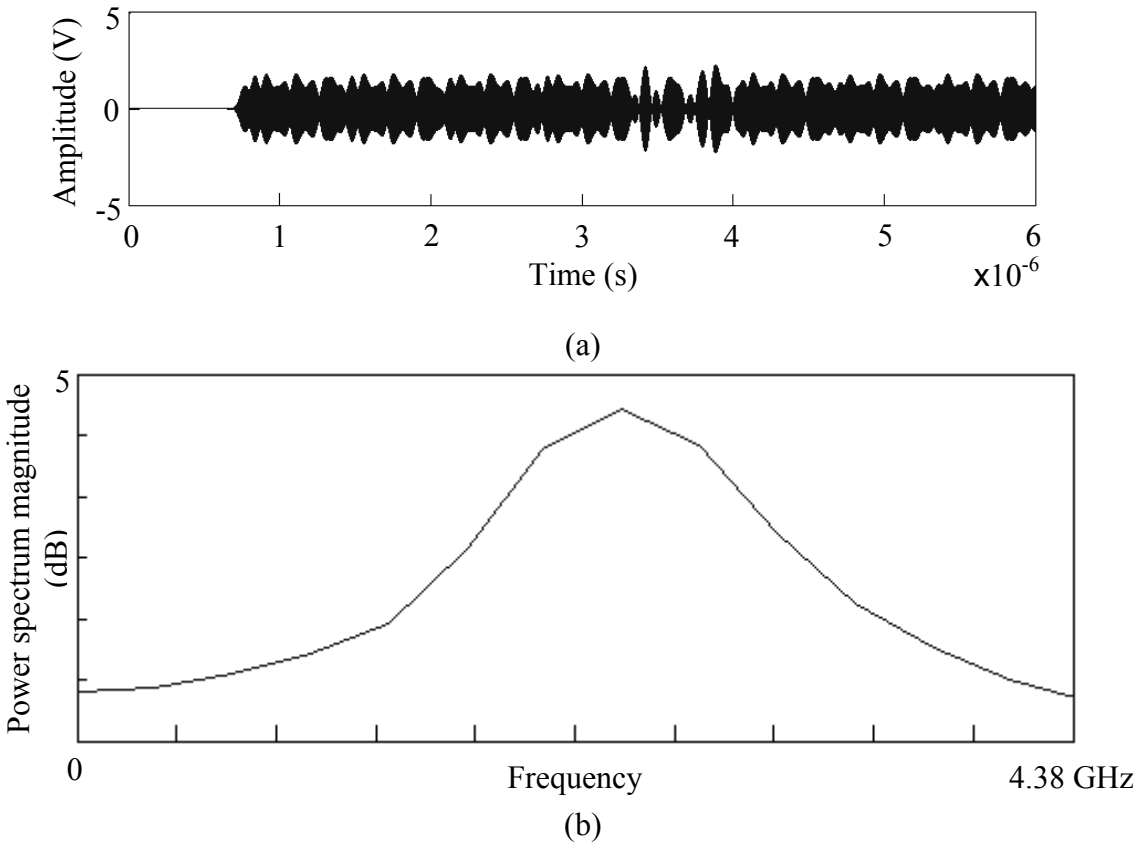


Figure 2.45.

Transmitted signal in (a) time domain and (b) frequency domain.

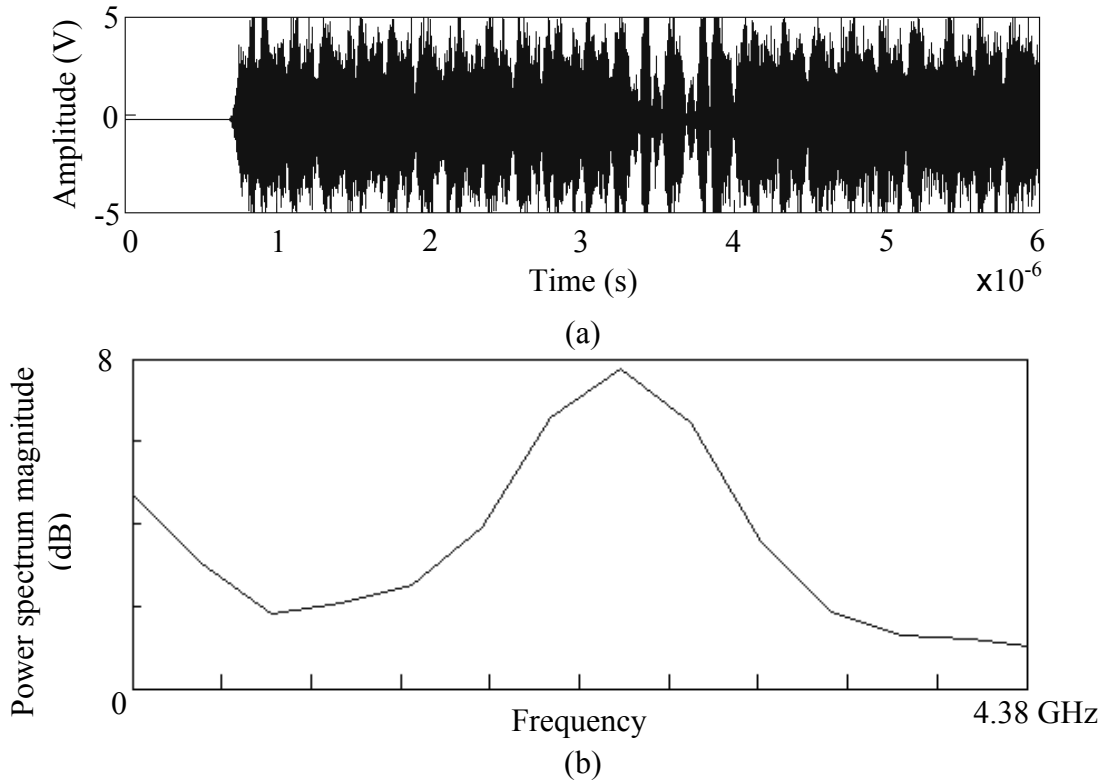


Figure 2.46.

(a) Time-domain and (b) frequency domain simulation traces of the signal after it has been passed through the noisy and fading channel (using MATLAB).

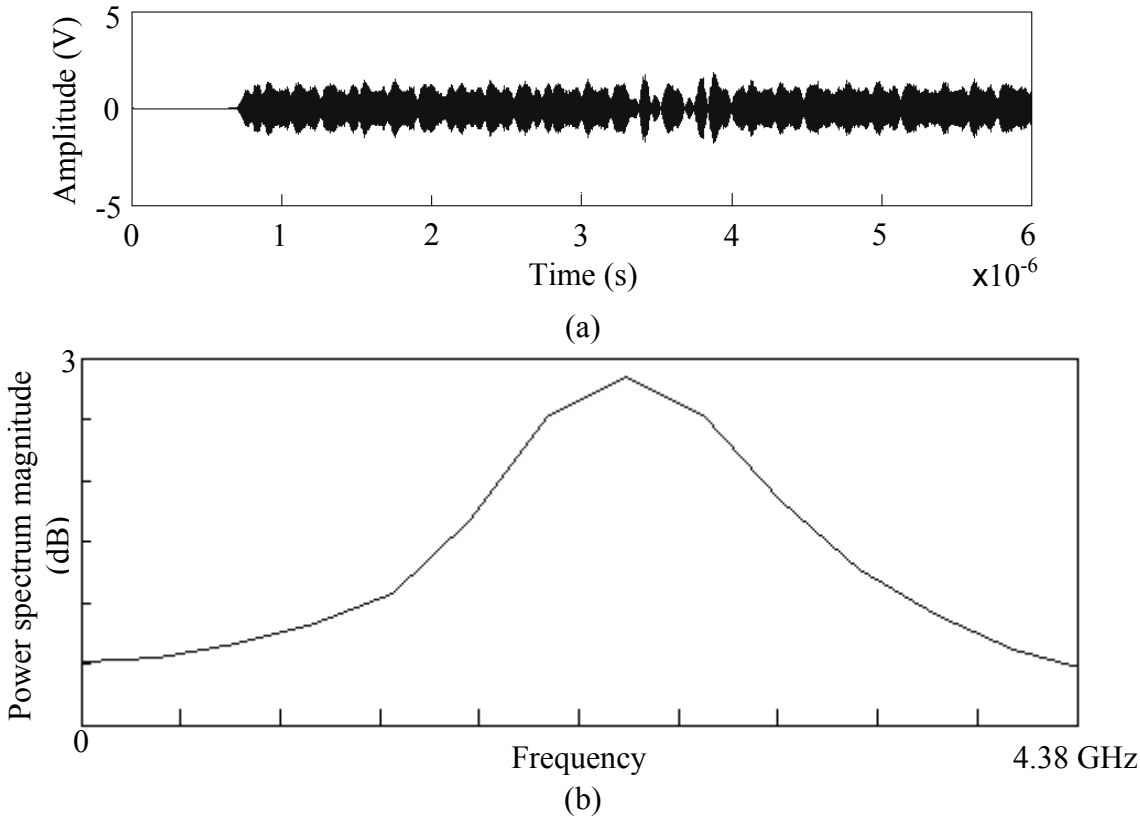


Figure 2.47.

(a) Time-domain and (b) frequency-domain simulation traces of the signal after it has been received.

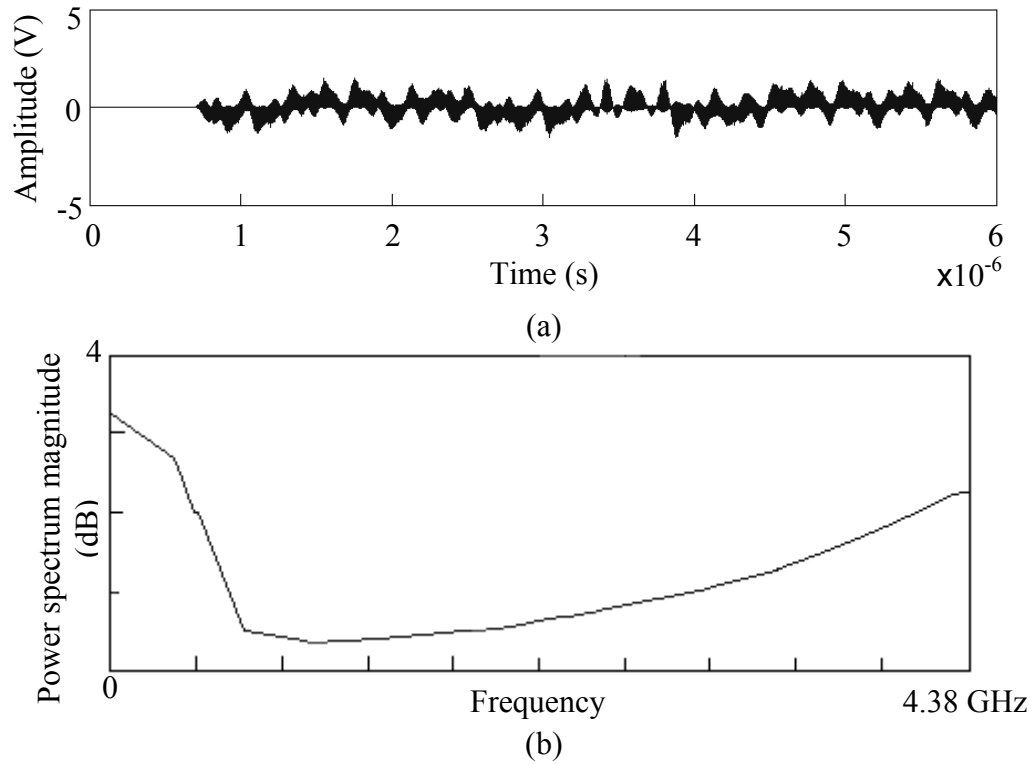
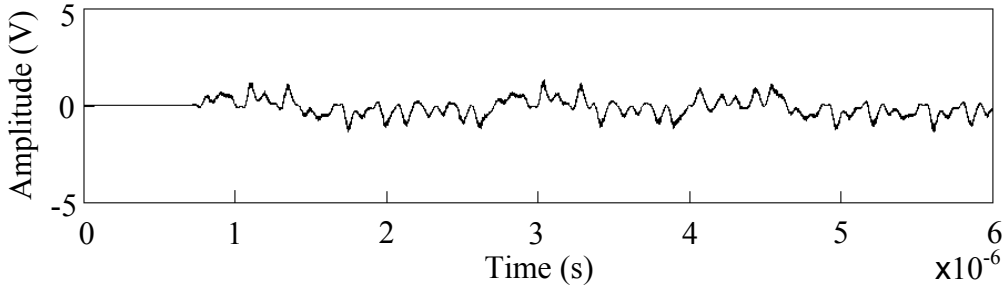
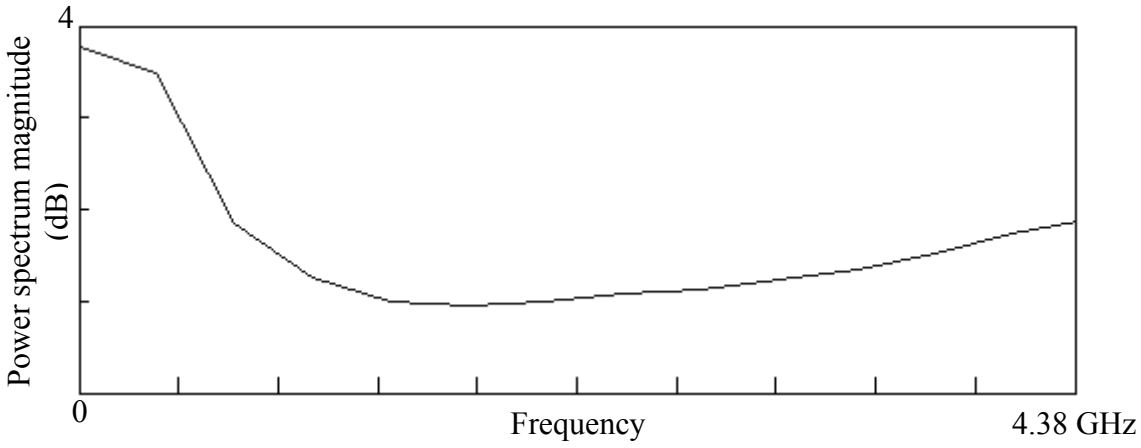


Figure 2.48.

(a) Time-domain and (b) frequency-domain simulation traces of the signal in the top branch of the receiver after demodulation.



(a)



(b)

Figure 2.49.

(a) Time-domain and (b) frequency domain simulation trace of the signal at the top branch of the receiver after despreading.

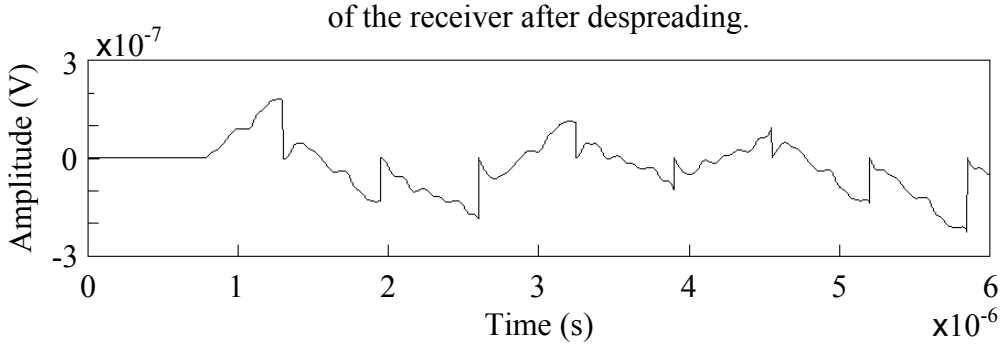


Figure 2.50.

Time-domain simulation trace of the signal in the top branch of the receiver after it has been processed by the integrate and dump subsystem.

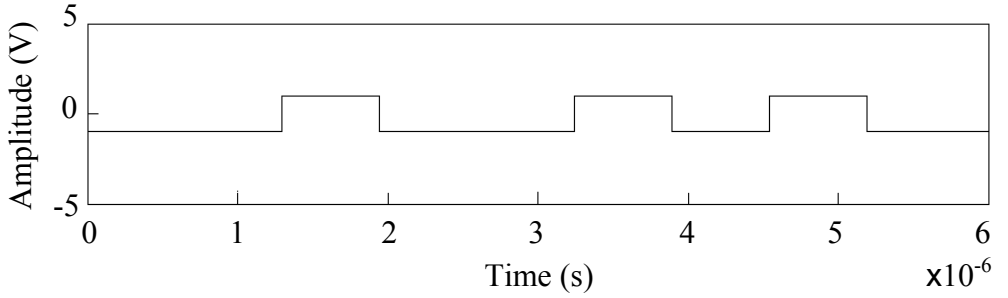


Figure 2.51.

Time-domain simulation trace of the signal after it has been passed through limiting and sampling.

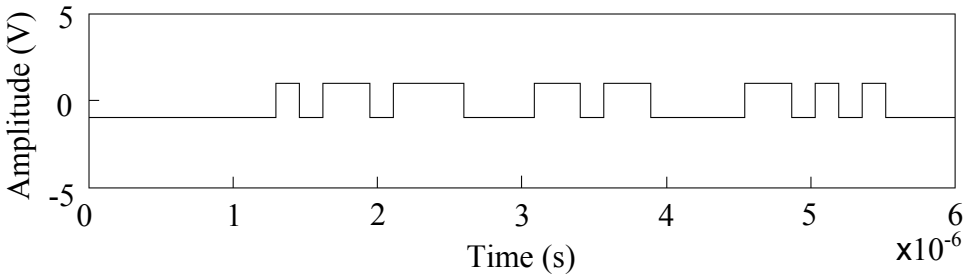


Figure 2.52.

Time-domain simulation trace of the final recovered signal.

CHAPTER 3: ANALOGUE SUB-SYSTEMS DESIGN

In the previous chapter, a systems level design was achieved for the transceiver proposed in this thesis. The aim of this chapter is to isolate, yet take inter-stage loading into account, and implement the various identified sub-systems using CMOS technology.

3.1 CMOS process parameters

The CMOS process used for this thesis is the AMS 0.35 µm process [28]. The C35B4C3 process allows for a minimum gate length of 0.35 µm, and has four metal layers and two layers of poly. A cross section of the wafer, shown in Figure 3.1 highlights the available layers and illustrates the layout of the transistor and capacitor modules. The process allows for n-channel MOSFETs (NMOS), p-channel MOSFETs (PMOS), resistors, capacitors, diodes and Zener diodes. Although the process does allow for BiCMOS fabrication[1] it is more expensive to produce, for this reason this thesis is limited to MOSFET implementation.

The most important parameters for design, as used in this thesis, are listed in tables 3.1 – 3.3. These and other process dependant details are protected by a non-disclosure agreement between the author and the University of Pretoria. For this reason the process parameters are not discussed in detail.

[1] BiCMOS refers to integrated circuits that include both MOSFETs and bipolar junction transistors (BJTs) in the same silicon substrate.

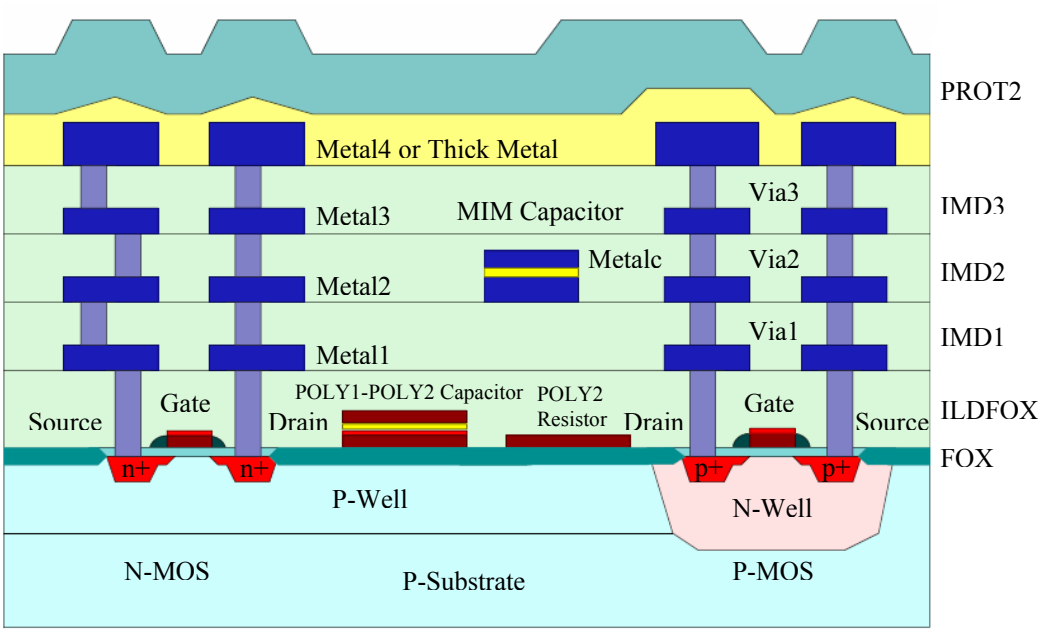


Figure 3.1.

A cross-sectional view of the AMS C35B4C3 process [28].

MOS Transistor	Max V_{GS} [V]	Max V_{DS} [V]	Max V_{GB} [V]	Max V_{DB} [V]	Max V_{SB} [V]
3.3 V NMOS / PMOS	3.6 (5) V	3.6 (5) V	3.6 (5) V	3.6 (5) V	3.6 (5) V

Table 3.1.

Operating ranges for the NMOS and PMOS transistors. The values in brackets denote the absolute maximum ratings [28].

NMOS				PMOS			
Parameter	Min	Typ	Max	Parameter	Min	Typ	Max
Long-channel (0.35) VTH [V]	0.36	0.46	0.56	Long-channel (0.35) VTH [V]	-0.48	-0.58	-0.68
Short-channel (10*0.35) VTH [V]	0.4	0.5	0.6	Short-channel (10*0.35)VTH [V]	-0.55	-0.65	-0.75
Effective channel length 0.35 µm	0.49	0.59	0.69	Effective channel length 0.35 µm	0.42	0.5	0.58
Effective channel width 0.35 µm	0.30	0.38	0.46	Effective channel width 0.35 µm	0.2	0.35	0.5
Body factor (γ) [V1/2]	0.48	0.58	0.68	Body factor (γ) [V1/2]	-0.32	-0.4	-0.48
Gain factor (KPn) [µA/V2]	150	170	190	Gain factor (KPp) [µA/V2]	48	58	68
Saturation current ID,sat [µA/µm]	450	540	630	Saturation current ID,sat [µA/µm]	-180	-240	-300
Effective mobility µo [cm2/Vs]	-	370	-	Effective mobility µo [cm2/Vs]	-	126	-

Table 3.2.

Summary of transistor parameters used in this thesis [28].

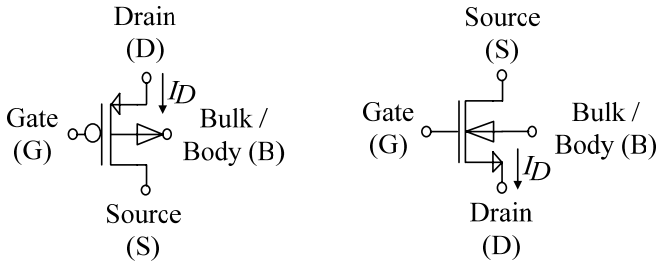
Resistance Parameters				Capacitance Parameters			
Parameter	Min	Typ	Max	Parameter	Min	Typ	Max
N-well sheet resistance [kΩ/□]	0.9	1.0	1.1	MOS varactor (CVAR) [fF/ µm^2]	2.40	3.01	3.61
N-well temp. coeff. (α) [10^{-3}/K]	-	6.2	-	Poly-1 – Poly-2 Capacitor			
Poly-1 sheet resistance [Ω/□]	-	8	11	CPoly area capacitance [fF/ µm^2]	0.78	0.86	0.96
Poly-1 temp. coeff. (α) [10^{-3}/K]	-	0.9	-	Cpoly perim capacitance [fF/ µm]	0.083	0.086	0.089
Poly-2 sheet resistance [Ω/□]	40	50	60	CPoly linearity [ppm/V]	-	85	-
Poly-2 temp. coeff. (α) [10^{-3}/K]	-	0.8	-				
RPOLYH sheet resistance [kΩ/□]	1.0	1.2	1.4				
RPOLYH temp. coeff.(α) [10^{-3}/K]	-	-0.4	-				

Table 3.3.

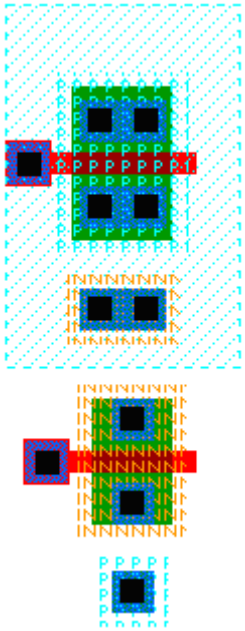
Summary of AMS parameters required for design of passive elements [28].

3.2 MOSFET summary

Since MOSFETs form the basis of this thesis, a short summary is provided in this section. The MOSFET is a four terminal device, as shown in Figure 3.2, including gate, drain, source and bulk terminals.



(a)



(b)

Figure 3.2.

(a) Symbols used to represent the PMOS (left) and NMOS (right) transistors.

(b) Layout of transistors: PMOS (top), and NMOS (below).

The MOSFET can be biased to work in one of two regions of operation, namely the triode or saturation region (including the sub-threshold region). These regions can be seen in the *I-V* characteristic of a MOSFET (Figure 3.3), where the gate-source voltage, v_{GS} is held constant at various values while the drain current, I_D, is measured for a sweep of the drain-source voltage v_{DS} (the PMOS operation is the same with symbols inverted i.e. v_{SG} for a PMOS is equivalent to v_{GS} for an NMOS).

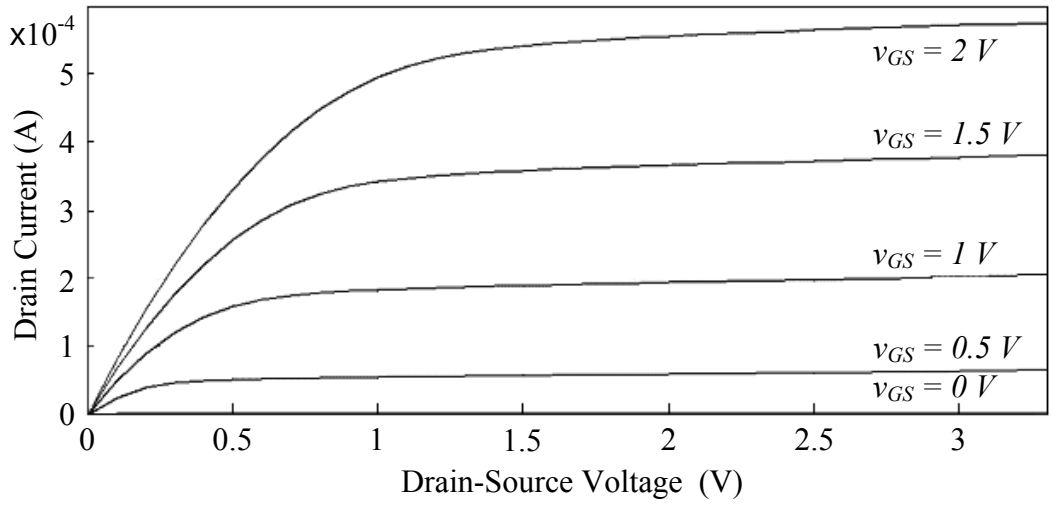


Figure 3.3.

A plot of the drain current, I_D, against a sweep of the drain-source voltage, v_{DS}, for increasing values of gate-source voltage, v_{GS}.

Operation in the triode region

This section describes equations used to relate i_D, v_{GS}, and v_{DS} [29]. There exists a capacitance between the gate and the inversion layers due to the oxide between the two layers.

This oxide capacitance per unit area can be calculated using

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.1}$$

where ε_{ox} represents the SiO_2 dielectric constant and t_{ox} is the thickness of the oxide layer.

The exact value of this capacitance, C_{ox}, can be calculated as

$$C_{ox} = C'_{ox} \cdot A = C'_{ox} \cdot WL \tag{3.2}$$

The transconductance parameter KP is defined for an NMOS device as

$$KP_n = \mu_n \cdot C'_{ox}, \tag{3.3}$$

and for a PMOS device

$$KP_p = \mu_p \cdot C'_{ox} \tag{3.4}$$

Thus for an NMOS device operating in the triode region the current flowing into the drain of the device can be shown to be

$$I_D = KP_n \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right] = \mu_n \cdot C'_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3.5}$$

where V_{THN} is the threshold voltage for an NMOS transistor. Note that equation (3.5) is only valid for $V_{GS} \geq V_{THN}$ and $V_{DS} \leq V_{GS} - V_{THN}$. The equation for a PMOS transistor is identical if each parameter is replaced with the PMOS equivalent parameter.

Operation in the saturation region

When $V_{DS} \geq V_{GS} - V_{THN}$ the NMOS moves into the saturation region, as the channel formed under the gate oxide starts to "pinch off" and further increase in current is not possible. The value of V_{DS} at which this occurs (when the inequality is equal) is defined as $V_{DS,sat}$. Ignoring the effects of channel length modulation (included in Equation 3.7) and assuming V_{GS} remains constant, any increase in V_{DS} beyond this level does not cause an increase in the drain current. The drain current for an NMOS operating in the saturation region is given by

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{THN}\right)^2 \tag{3.6}$$

for $V_{GS} \geq V_{THN}$ and $V_{DS} \geq V_{GS} - V_{THN}$. This equation is generally referred to as the "square-law" equation for MOSFETs.

The assumption that once the channel becomes "pinched off" at the drain end, further increases in V_{DS} have no effect on the channels shape is an ideal one. In practice, increasing V_{DS} beyond its saturation point moves the "pinched off" region closer to the source, and in effect, the channel length is reduced. This is referred to as channel-length modulation. Equation (3.6) can be altered to include the effect of channel length modulation as

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{THN}\right)^2 \left[1 + \lambda \left(V_{DS} - V_{DS,sat}\right)\right] \tag{3.7}$$

This equation makes another assumption, and that is that the effective mobility of the majority carrier (μ_n in this case) remains uniform. This assumption is valid for transistors with longer channel lengths, however in short channel MOSFETs the change in mobility can no longer be ignored.

Short-channel MOSFETs

In short-channel MOSFETs the main difference in operation occurs because the carriers drifting between the channel and drain of the MOSFET saturate in an effect called carrier velocity saturation, or v_{sat}. This results in a reduction in the hole or electron mobility which increases the channels effective sheet resistance.

While the velocity at low field values is governed by Ohm's law (also implying $v \propto E$), the velocity at high field values approaches a constant called the scattering-limited velocity [29; 57], v_{scl}. A first order analytical approximation to this curve is [57]

$$v_d = \frac{\mu_n E}{1 + \frac{E}{E_{critical}}}, \tag{3.8}$$

where the critical field, $E_{critical}$ is approximately 1.5 MV/m and $\mu_n = 0.07$ m^2/V-s.

As $E_{critical} \to \infty$, $v_d \to v_{scl} = \mu_n E_{critical}$. At the critical field value, the carrier velocity is a factor of 2 less than the low-field relationship would predict. It is further shown [57] that, in the active region,

$$V_{DS(act)} \to (V_{GS} - V_{THN}), \tag{3.9}$$

for $E_{critical} \to \infty$.

The drain current in the active region with velocity saturation is given by [57]

$$\lim_{E_{critical} \to \infty} I_D = \mu_n C_{ox} W (V_{GS} - V_{THN}) E_{critical} = C_{ox} W (V_{GS} - V_{THN}) v_{scl} \tag{3.10}$$

The implication of this is that for short channel MOSFETs, the current I_D is linearly related to the overdrive voltage, $V_{GS} - V_{THN}$.

3.3 Bias network design

By creating a basic list that can be used as a premise for design, the process of creating subsequent modules is somewhat simplified, in that it has a basis on which it can build. Building these parameters was based on the square-law equation for transistors and since the specification for the thesis is low-voltage, the transistors were designed to be operated in the saturation region with minimum excess gate-source voltage (also known as overdrive voltage, V_{OD}). Since the transistor was not pushed too far into the saturation region, channel length modulation was ignored for the basic design, unless otherwise mentioned.

NMOS design parameters

The design is based on a width to length ratio (aspect ratio) of 5/1, this was chosen so that if the *W/L* ratio needed changing later in the design there was room for this. The length was designed to be a minimum to ensure greater achievable speeds (as the same aspect ratio will be used for some other sub-systems later on). Thus for the 0.35 µm process the following ratio was used for the basic NMOS transistor

$$\left(\frac{W}{L}\right)_n = \frac{5}{1} = \frac{1.75\mu m}{0.35\mu m} \tag{3.11}$$

To begin to calculate the required variables for the square law equation each of the required parameters needed to be evaluated. The dielectric constant of SiO_2 is given by

$$\varepsilon_{ox} = \varepsilon_r \varepsilon_0 = 3.97\varepsilon_0 = 35.1511\, pF/m \tag{3.12}$$

where ε_r is the relative dielectric constant for SiO_2 and ε_0 the vacuum dielectric constant.

The thickness of the SiO_2 was obtained from the AMS process parameters and thus the oxide capacitance can be calculated as

$$\begin{aligned} t_{ox} &= 7.575\ nm \\ \therefore C'_{ox} &= \frac{\varepsilon_{ox}}{t_{ox}} = 4.64\ \frac{fF}{(\mu m)^2} \end{aligned} \tag{3.13}$$

The electron mobility coefficient is also defined in the AMS process parameters model as $\mu_n = 370\ cm^2/V \cdot s$. Using this along with the oxide capacitance in (3.13) the transconductance gain parameter KP_n can be calculated as

$$\begin{aligned} KP_n &= \mu_n C'_{ox} = \left(47.58\times10^{-3}\right)\left(370\times10^{-5}\right) \\ &= 176.05\ \mu A/V^2 \end{aligned} \tag{3.14}$$

which corresponds to the typical mean value as given in the process parameters. Using $V_{THN} = 0.4979\ V$ as defined in modn.md[2] and in the process parameters, along with the values calculated above and the required voltages, basic transistor biasing can be done by looking at the *I-V* transfer characteristic for a sweep of v_{GS}. The circuit setup is shown in Figure 3.4, and the *I-V* characteristic is shown in Figure 3.5.

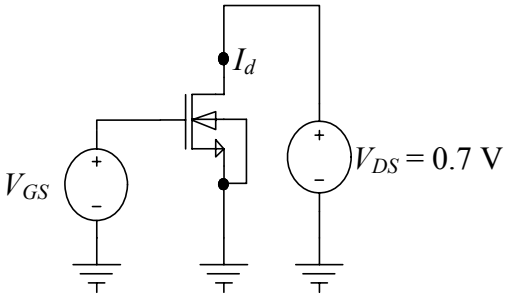


Figure 3.4.

Setup used to obtain the *I-V* characteristic for the NMOS transistor, with v_{DS} held constant at 0.7 V.

[2] modn.md is the model file used by T-Spice to simulate the AMS transistor.

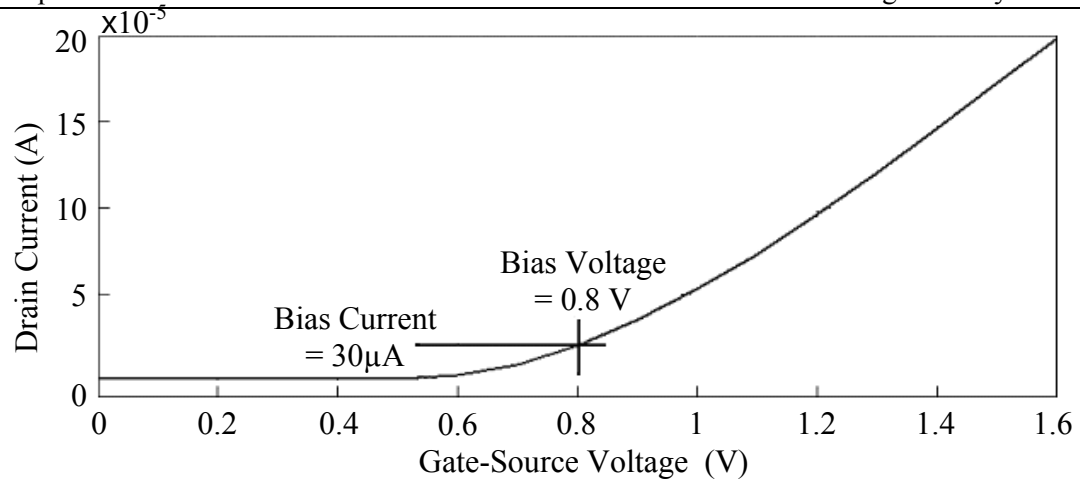


Figure 3.5.

Drain current for a sweep of the gate-source voltage with the drain-source voltage held constant at 0.7 V.

It was decided to use a biasing drain current of I_D = 30 µA to keep the transistors in the saturation region while consuming a minimum amount of power (since the power consumption is related to the current by $P = VI$). Thus the V_{GS} required to obtain I_D = 30 µA can be calculated as

$$V_{GS} = \sqrt{\frac{2I_D}{KP_n}\left(\frac{L}{W}\right)_n} + V_{THN} \cong 0.8\ V \tag{3.15}$$

and, $V_{DS,sat} = V_{GS} - V_{THN} = 261.08\ mV = V_{OD}$.

PMOS design parameters

Similar results hold for the PMOS transistor if the width of the transistor is adjusted therefore only the major differences are discussed here. Since the mobility of holes is lower than that of electrons, the width of the PMOS is usually adjusted to account for this and keep operation of the two devices similar. The width and length of the PMOS can be calculated using the adjustment factor given by,

$$\frac{\mu_n}{\mu_p} = \frac{370\,cm^2/V\cdot s}{126\,cm^2/V\cdot s} = 2.94 \cong 3 \tag{3.16}$$

Thus the width of the PMOS should be related to that of the NMOS by,

$$\left(\frac{W}{L}\right)_p = 3\left(\frac{W}{L}\right)_n$$

$$\therefore W_p = 3W_n \tag{3.17}$$

So the *W/L* ratio of the PMOS is given by,

$$\left(\frac{W}{L}\right)_p = \frac{15}{1} = \frac{5.25\mu m}{0.35\mu m} \tag{3.18}$$

The only other parameter that differs for the PMOS transistor is the threshold voltage, V_{THP}. A summary of both the NMOS and PMOS parameters used in the design process for biasing networks in this thesis is shown in table 3.4.

Parameter	NMOS	PMOS	Additional
Bias Current, I_D	30 µA	30 µA	From Figure 3.5
W/L	5/1	15/1	$\mu_n/\mu_p \approx 3$
Actual	1.75 µm/ 0.35 µm	5.6 µm/ 0.35 µm	L = 0.35 µm
V_{TH}	0.4979 V	0.6842 V	Typical Mean
KP	176 µA/V^2	58 µA/V^2	
$C_{ox} = \varepsilon_{ox}/t_{ox}$	4.64 mF/m^2	4.64 mF/m^2	t_{ox} = 7.575 nm
$\lvert V_{GS}\rvert$	0.8 V	0.92 V	From Figure 3.5
$\lvert V_{DS,sat}\rvert$	261 mV	260 mV	$V_{DS,sat} = V_{GS} - V_{THN}$

Table 3.4.

Summary of transistor parameters used for the biasing network.

The bias network is important part of the system for this thesis, since for components to function as designed their biasing voltages must remain stable and must start up to the correct value [30, 31]. The design starts with designs for current mirrors and then moves onto the beta-multiplier and finally a full biasing networks.

Current mirror

The most basic form of a current mirror is shown in Figure 3.6. In this circuit the resistor, *R*, is used to generate a reference current which is 'mirrored' through the second NMOS – M2. As will be shown the amount of current the mirror is able to sink is dependant on the width ratios of M1 and M2. The connection of the gates to the drain of M1 is referred to as a "diode" connection, since the transistor will always operate in the saturation region.

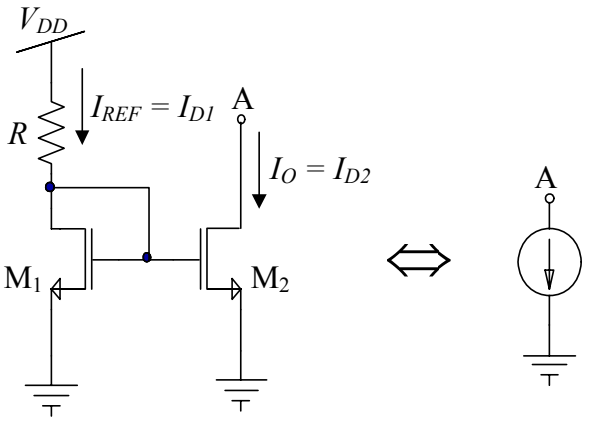


Figure 3.6.

Basic circuit schematic of a simple current mirror, and its equivalent representation.

From Equation (3.6) the following can be derived

$$I_{REF} = \frac{KP_n}{2} \cdot \frac{W_1}{L_1} \cdot \left(V_{GS1} - V_{THN}\right)^2$$
$$I_O = \frac{KP_n}{2} \cdot \frac{W_2}{L_2} \cdot \left(V_{GS2} - V_{THN}\right)^2 \qquad (3.19)$$
$$\frac{I_{REF}}{I_O} = \frac{\frac{W_1}{L_1} \cdot \left(V_{GS1} - V_{THN}\right)^2}{\frac{W_2}{L_2} \cdot \left(V_{GS2} - V_{THN}\right)^2}$$

Since the gates of M1 and M2 are connected and both of their sources go to ground, $V_{GS2} = V_{GS1}$, and therefore I_O is related to I_{REF} by (letting $L_1 = L_2$)

$$I_O = \frac{W_2}{W_1} I_{REF} \qquad (3.20)$$

This current source offers a good method of sinking current if supply voltage, V_{DD}, is constant and the resistor remains at a constant temperature. In general, however, the voltage supply will not always be constant and the value of the resistor depends on various factors, like process variations and changes in temperature. Therefore a reliable supply independent current reference is required.

Beta-multiplier circuit

If the resistor is placed on the source side of the current mirror instead of the drain side, it becomes isolated from the influence of the power supply. Also adding a PMOS mirror forces the same current through each channel, making the voltage reference far less dependant on the value of the resistor, and thus less dependant on variations in

temperature. Figure 3.7 shows the schematic of the beta multiplier circuit, including a start-up circuit to ensure the system starts up with the correct levels (imbalance in the mirror could turn one of the current mirrors off and the other on sending the references to either V_{DD} or ground).

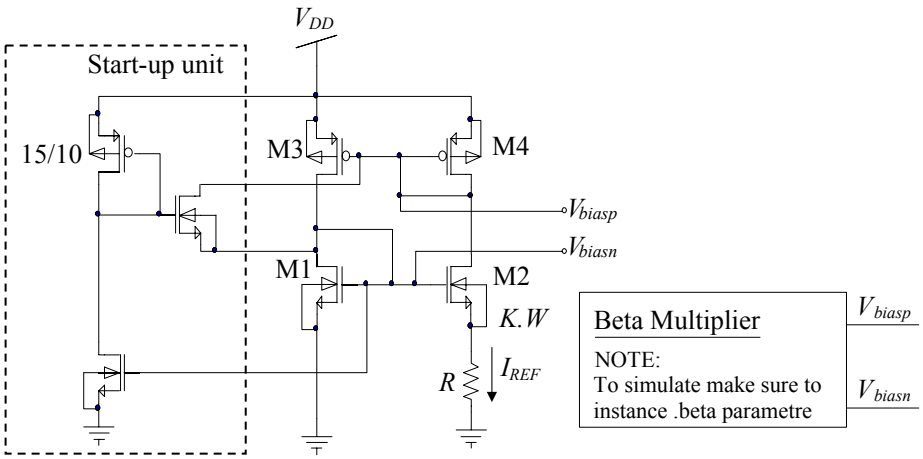


Figure 3.7.

Circuit schematic for a beta-multiplier including the start-up circuitry and the symbol used for instancing the circuit. All unlabelled NMOS and PMOS transistors have aspect ratios of 5/1 and 15/1, respectively. $V_{biasp} = V_{bp}$ & $V_{biasn} = V_{bn}$.

Since the current flowing through the resistor is forced to I_{REF} by the PMOS current mirror the gate-source voltage of M1 can be written as

$$V_{GS1} = V_{GS2} + I_{REF} \cdot R \tag{3.21}$$

For this to be valid V_{GS1} must be greater than V_{GS2}, and to ensure this a larger value of β is required[3], since

$$V_{GS} = \sqrt{\frac{2I_D}{\beta}} + V_{THN} \tag{3.22}$$

The length of the transistors is already a minimum and the transconductance parameter is constant, the relation of $\beta_2 = K\beta_1$ must therefore be satisfied by letting $W_2 = KW_1$. From this, the reference current through M2 can be expressed as,

$$I_{REF} = \frac{2}{R^2 KP_n \cdot \frac{W_1}{L_1}}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \tag{3.23}$$

If K = 4 & I = 30 µA, and Equation 3.23 solved using the design parameters from Table 3.4, R can be found to be 4.35 kΩ.

[3] β is often used to represent the multiplicand of $KP \cdot W/L$ hence the name 'Beta-multiplier'.

Full biasing network

Using cascode[4] current mirror loads (e.g. the folded cascode and telescopic amplifiers) can increase the amplification of a differential gain circuit. To use a differential output, as required by other sub-systems of this thesis, each level of the cascode needs to be precisely biased to ensure all transistors operate in the saturation region.

The design is basically an extension of the beta-multiplier circuit, where the reference voltage of the NMOS transistor is first used to drive a PMOS cascode current mirror, and then used in an NMOS cascode current source.

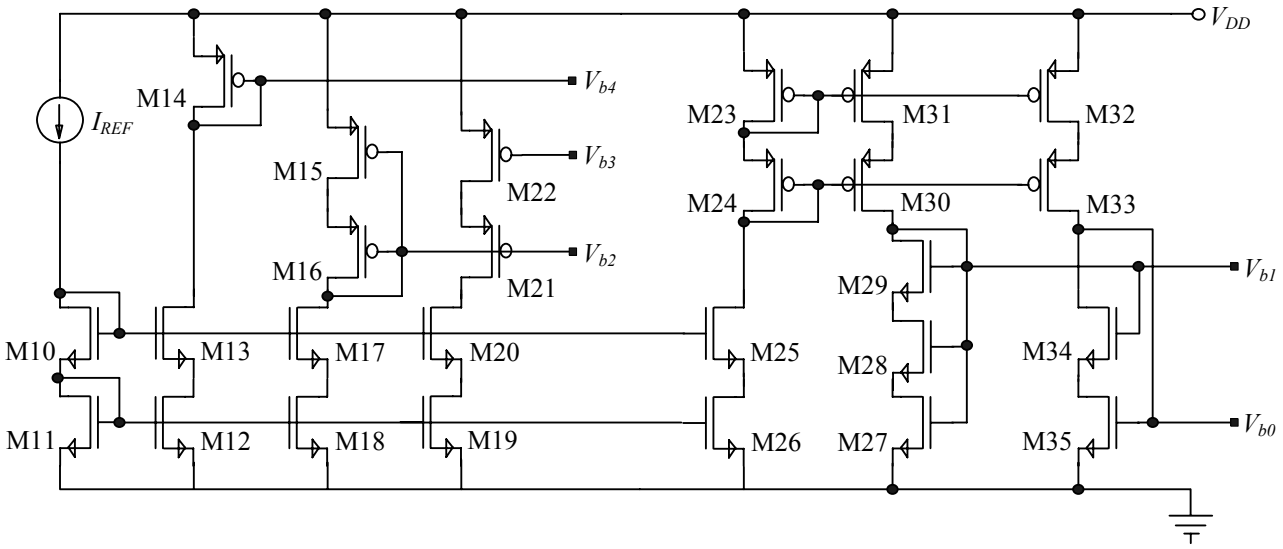


Figure 3.8.
Circuit schematic of the bias network used in this thesis. All unlabelled NMOS and PMOS transistors have aspect ratios of 5/1 and 15/1, respectively.

The basic concept of its operation is based on using various stages of current mirrors to keep "mirroring" the I_{REF} from the beta-multiplier. Since I_{REF} is mirrored through the PMOS and NMOS cascode current mirror structures and since they are diode connected, their gate voltages can be used to mirror the same current in other structures which therefore do not need to be diode connected to operate in the saturation region. This fact is important, because since the transistors can run off the voltages generated by the bias network, the output of an amplifier using this bias scheme can be taken differentially [30].

[4] The term 'cascode' originated in the days of using vacuum tubes. It is an acronym for "cascaded triodes".

Operating temperature range of reference voltages

Figure 3.9 shows the plotted results of a temperature sweep simulation of the beta-multiplier circuit of Figure 3.7.

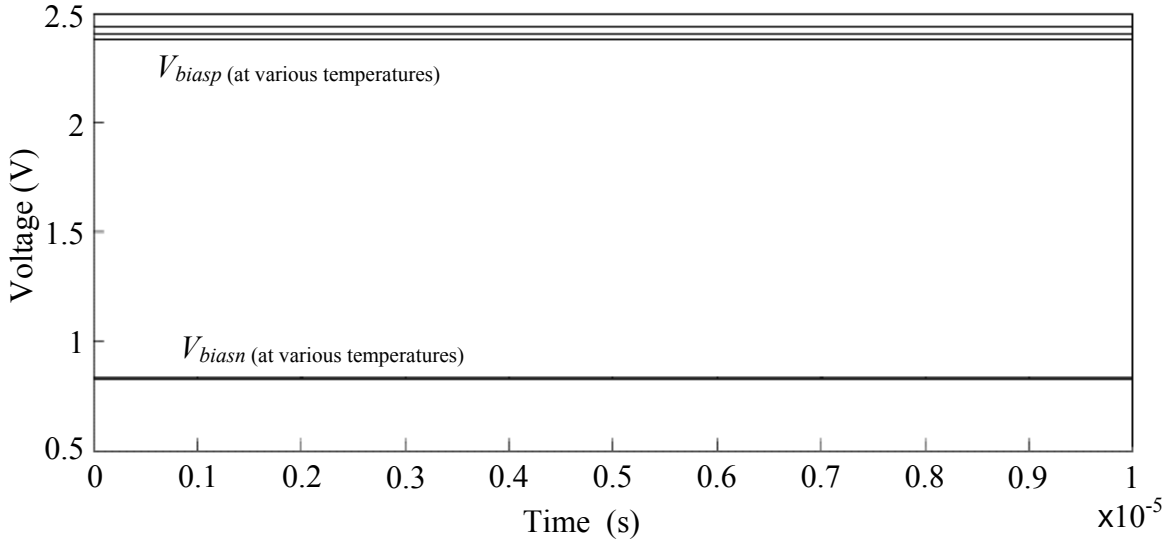


Figure 3.9.

Temperature sweep transient simulation for the beta-multiplier.

Table 3.5 summarizes the results for various temperatures.

Parameter	***-10 °C***	***25 °C***	***70°C***
V_{biasn}	***0.828 V***	***0.8261 V***	***0.8244 V***
V_{biasp}	***2.377 V***	***2.402 V***	***2.438 V***

Table 3.5.

Bias values measured for the commercial range.

Figure 3.10 displays the variation in bias current with temperature.

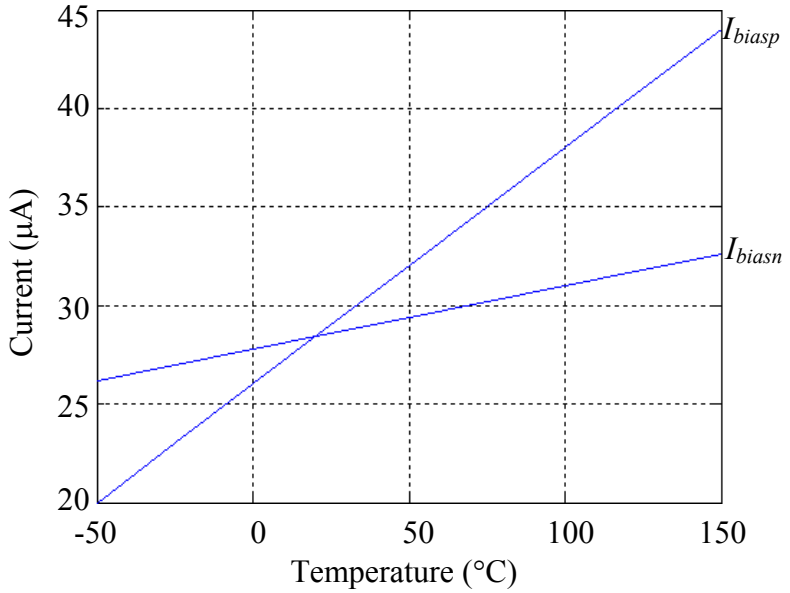


Figure 3.10.

Temperature sweep performed on the Beta-Multiplier to display the bias currents.

Table 3.6 records the various bias voltages obtained from Fig. 3.8.

Parameter	*-10 °C*	*25 °C*	*70°C*
V_{b4}	*2.212 V*	*2.221 V*	*2.23 V*
V_{b3}	*1.852 V*	*1.862 V*	*1.872 V*
V_{b2}	*1.382 V*	*1.344 V*	*1.308 V*
V_{b1}	*0.9423 V*	*0.9339 V*	*0.9263 V*
V_{b0}	*0.881 V*	*0.883 V*	*0.884 V*

Table 3.6.

Values obtained from simulation of the bias circuit for selected temperatures in the commercial temperature range.

Since the voltage references constitute the foundation for the entire system, their ability to remain constant is crucial to reliable operation in varying conditions. As expected, the threshold voltage, V_{TH}, decreases for the NMOS transistor and increases for the PMOS transistor with increasing temperature.

3.4 Amplifier design

For large amplification and improved bandwidth qualities the differential CMOS amplifier with active loads are the most effective amplifier topologies.

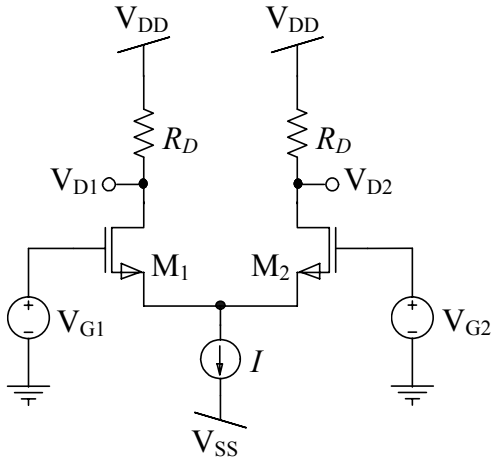


Figure 3.11.

Basic MOS differential-pair configuration.

In the design of fully differential operational amplifiers, several different topologies exist that build on the basic differential amplifier topology (which is shown in Figure 3.11). The advantages and disadvantages of various topologies are described in table 3.7 [32].

	Gain	Speed	Output Swing	Noise	Power Consumption
Telescopic	Medium	Highest	Low	Low	Low
Folded- Cascode	Medium	High	Medium	Medium	Medium
Multistage	Highest	Low	Highest	Low	Medium
Gain-Boosted	High	Medium	Medium	Medium	High

Table 3.7.

Amplifier topologies and their properties [32].

The design of complex amplifier circuits requires complex biasing circuitry and analysis of the transistors used and their DC operating points.

The output of an amplifier can be defined, generically, in terms of its common-mode and differential-mode gain as

$$v_O = A_d v_{ID} + A_{cm} v_{IC} \tag{3.24}$$

where A_d represents the differential-mode voltage gain and A_{cm} represents the common-mode voltage gain, [31]. The differential-mode input voltage, v_{ID}, and the common-mode input voltage, v_{IC} are defined in terms of the differential input pair $v_{I1(G1)}$ and $v_{I2(G2)}$ as stated below.

$$v_{ID} = v_{I1} - v_{I2} \tag{3.25}$$

$$v_{IC} = \frac{v_{I1} + v_{I2}}{2} \tag{3.26}$$

The common-mode rejection ratio (CMRR) is then defined by

$$CMRR_{dB} = 20\log\left(\frac{A_d}{A_{cm}}\right) \tag{3.27}$$

In designing an amplifier for high-speed, low-power applications, the telescopic and folded cascode structures are two of the most commonly used topologies [33-35]. The challenge in designing the amplifier lies in managing trade-offs between the various topologies, including required speed, gain, power usage and die size. From the basic topologies that exist in literature, minor variations can be made to improve the operation of the amplifier to meet the specifications and requirements that are dictated by its intended application.

Amplifiers are generally used with feedback to improve stability, increase bandwidth and to control amplification [31]. The general structure of a feedback amplifier is shown in Figure 3.12.

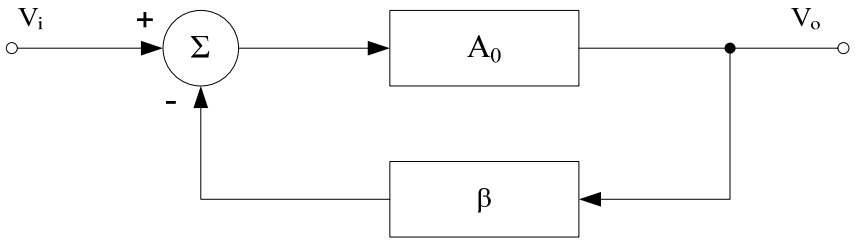


Figure 3.12.
General structure of a feedback amplifier in a signal flow diagram.

The feedback of the amplifier is defined by the feedback factor β. The open loop gain of the amplifier, A_o, is the gain of the amplifier when there is no feedback structure in place ($\beta = 0$). The closed loop gain of the amplifier can be shown to be

$$A_f \equiv \frac{v_O}{v_I} = \frac{A_o}{1 + A_o\beta} \tag{3.28}$$

The quantity $A_o\beta$ is called the loop gain and for the feedback to be negative (required for the amplifier to be stable), this quantity must be positive. If the open loop gain A_o is large then the loop gain $A_o\beta$ will also be large ($A_o\beta \gg 1$) and thus the amplification can be approximated as

$$A_f \cong \frac{1}{\beta} \tag{3.29}$$

which implies that the gain of the feedback amplifier is almost entirely determined by the feedback network.

Basic differential amplifier

The operation of a differential pair can be described, with reference to Figure 3.11. Assuming that v_{G1} - v_{G2} varies from -∞ to +∞. If v_{G1} is much more negative than v_{G2} then M1 turns off and M2 turns on. Then the current through M2 is equal to the current drawn by the biasing current source. As v_{G1} is brought gradually closer to v_{G2} M1 starts to turn on and starts to draw some of the current from the biasing source and thus starts to lower v_{D1}. The same happens in the opposite direction. Thus, because the current through each side of the amplifier varies between 0 and I_{MAX}, the output voltage varies between 0 and $I_{MAX} \cdot R$.

The implication of this is that the amount of gain that the amplifier can produce is proportional to the load resistance and the bias current it uses. Since increasing the bias current of the amplifier will increase its power consumption, the gain is improved by increasing the load resistance.

Using a PMOS current source load instead of a resistive load can provide a much larger load using a smaller area in the silicon. This was implemented as shown in Figure 3.13 (a).

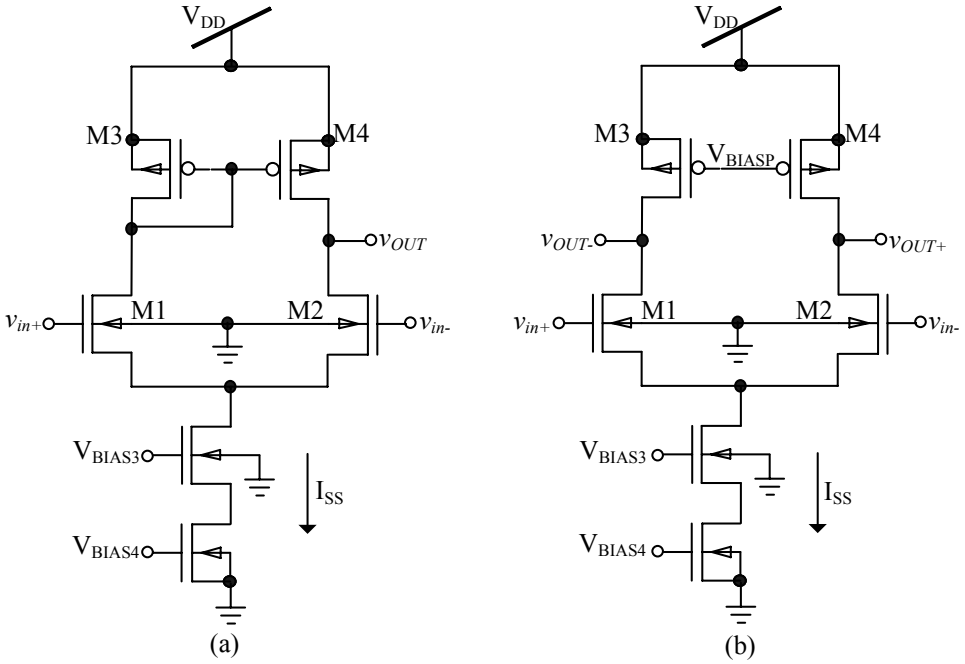


Figure 3.13.

(a) Circuit schematic of the single-ended differential amplifier.

(b) Circuit schematic of a fully differential amplifier.

All unlabelled NMOS and PMOS transistors have aspect ratios of 5/1 and 15/1, respectively. The complete biasing circuitry has not been shown, since these circuits were not eventually used.

Although this circuit offers mild open loop gain, when used with a feedback network the open loop gain is not high enough to warrant its implementation. The open-loop gain of this amplifier (Fig. 3.13 (a)) is given by

$$A_v = -g_{mN}\left(r_{ON} \parallel r_{OP}\right) \tag{3.30}$$

In Figure 3.13 (b) the circuit was changed to allow for a differential output. This was achieved by removing the diode connection on the PMOS current mirror, and instead, connecting the gates to the PMOS current mirror in the beta-multiplier circuit (see Figure 3.7). Figure 3.14 shows the voltage transfer characteristics for both of these circuits.

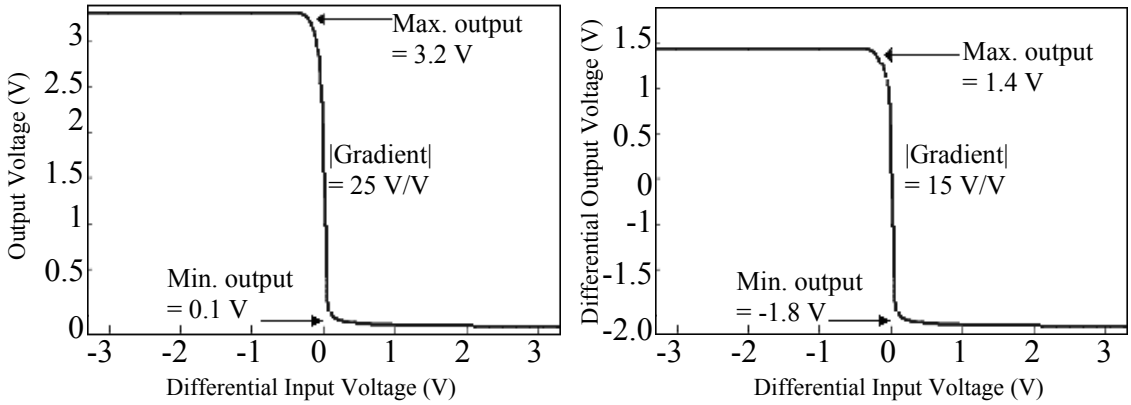


Figure 3.14.

Voltage transfer characteristics for both the single-ended and the fully differential amplifiers.

The above amplifier showed a gain of less than 40 dB, which is not adequate for all sub-systems of this thesis, hence a higher gain amplifier was also designed (as below).

Telescopic amplifier

The telescopic amplifier is a form of cascode amplifier. It employs both a PMOS cascode current source load, and an NMOS current source load, to create a gain using NMOS differential pair. As discussed in table 3.7, this amplifier topology is able to produce high gain but a relatively limited signal swing. The gain of this amplifier is given by

$$A_v = \frac{v_{out}}{v_{in}} = g_{mN}\left[\left(g_{mN}r_{ON}^2\right)\|\left(g_{mP}r_{OP}^2\right)\right] \tag{3.31}$$

where g_{mN} is the small signal gain of the NMOS transistor, g_{mP} is the small signal gain of the PMOS transistor, r_{ON} is the small signal resistance of the NMOS transistor and r_{OP} is the small signal resistance of the PMOS transistor. For a transistor with I_D = 30 µA, and a $v_{DS,sat} = v_{SD,sat}$ = 260 mV, then the small signal gain of the PMOS and NMOS transistors is given by

$$g_m = \frac{W}{L}\cdot KP\cdot V_{DS,sat}$$

$$\therefore g_{mN} = \left(\frac{5}{1}\right)(176)(0.26) = 228.8\mu A/V \tag{3.32}$$

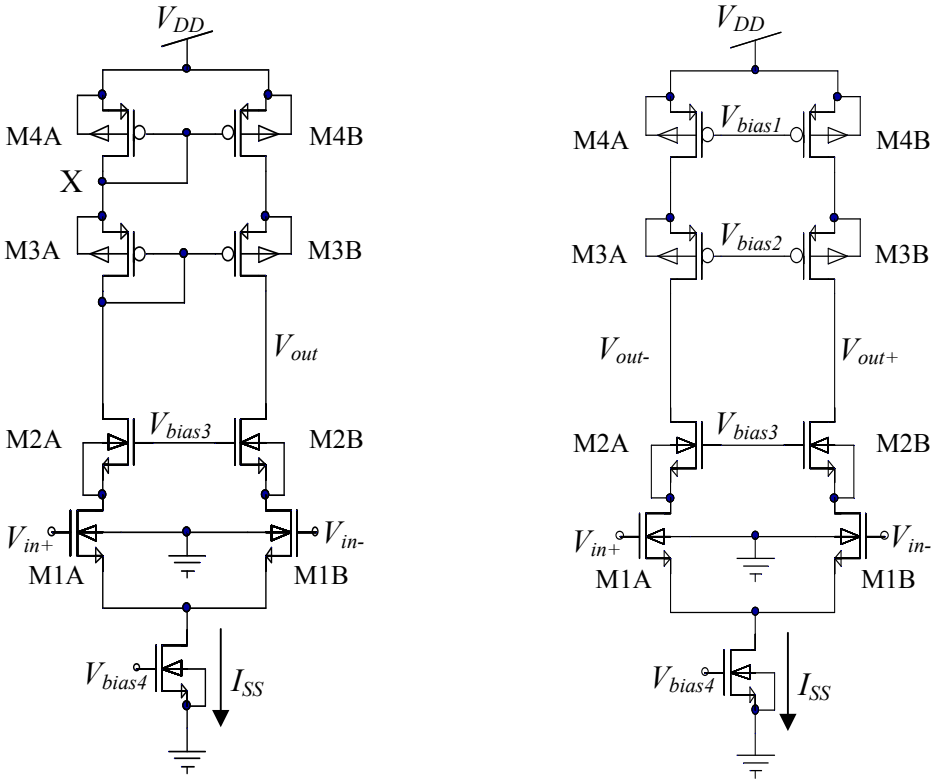
$$\therefore g_{mP} = \left(\frac{15}{1}\right)(58)(0.26) = 226.2\mu A/V \tag{3.33}$$

The values of r_O can be calculated using the channel length modulation factor, λ, being 0.03 V^{-1} for NMOS and 0.08 V^{-1} for PMOS, as specified by CMOS process parameters. So r_O can be calculated as

$$r_O = \frac{1}{\lambda I_D} \tag{3.34}$$

which gives $r_{Op} = 416.67\ k\Omega$ and $r_{On} = 1.11\ M\Omega$, thus using (3.32) the ideal open loop gain of the circuit is approximately 70 dB.

Figure 3.15 shows the schematics of the telescopic amplifier implemented in single-ended and in differential topologies. At node X in the single-ended topology, the circuit suffers from a mirror pole[5] which causes stability issues. This is not of concern in this thesis as the single-ended topology was not implemented. The advantages of the telescopic amplifier include, a very high gain for a one-stage amplifier, and high-speed (large GBW), however it suffers from limited output swing voltage and does not operate very well in unity gain configurations.



(a) (b)

Figure 3.15.

(a) Single-ended differential telescopic amplifier

(b) Fully differential telescopic amplifier.

Simulations of this circuit (Figure 3.16) show a much higher gain than that obtained for the simple differential amplifier, but not quite at the ideal level. This deviation from the ideal

[5] Poles and zeros are used to analyse the stability of a circuit

can be attributed to the non-ideal current source and the fact that the CMOS process utilised borders on being a short-channel process which (as mentioned in Section 3.1) has a different *I-V* relationship to long-channel processes.

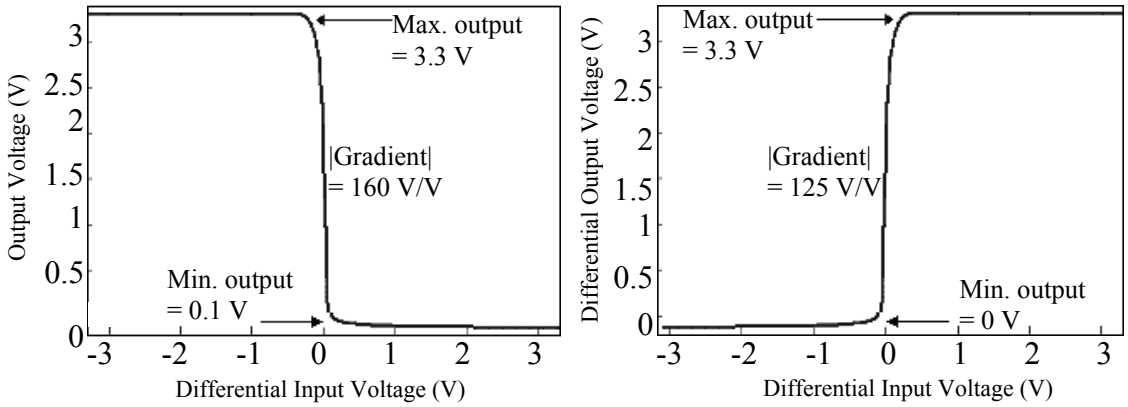


Figure 3.16.

Voltage transfer characteristics for the single ended (left) and the fully differential (right) telescopic amplifiers.

This design can be significantly improved by using a second stage to increase the output swing of the amplifier.

Two-stage telescopic amplifier

The design of this amplifier builds on a telescopic first stage [32]: This paper presented a highly customisable, high-gain differential CMOS amplifier with a large unity gain bandwidth. The design was adjusted for the requirements for this thesis but the 2nd stage topology (shown in Figure 3.17) was utilised. Since the second stage of the amplifier is just a common-source configuration the gain of this amplifier can be calculated as

$$|A_v| = A_{v1}A_{v2} = g_{mN}\left(r_{ON} \parallel r_{OP}\right) \cdot g_{mN}\left[\left(g_{mN}r_{ON}^2\right) \parallel \left(g_{mP}r_{OP}^2\right)\right] \tag{3.35}$$

which can be approximated as

$$|A_v| = {g_{mN}}^2\left(r_{ON} \parallel r_{OP}\right)^2 \tag{3.36}$$

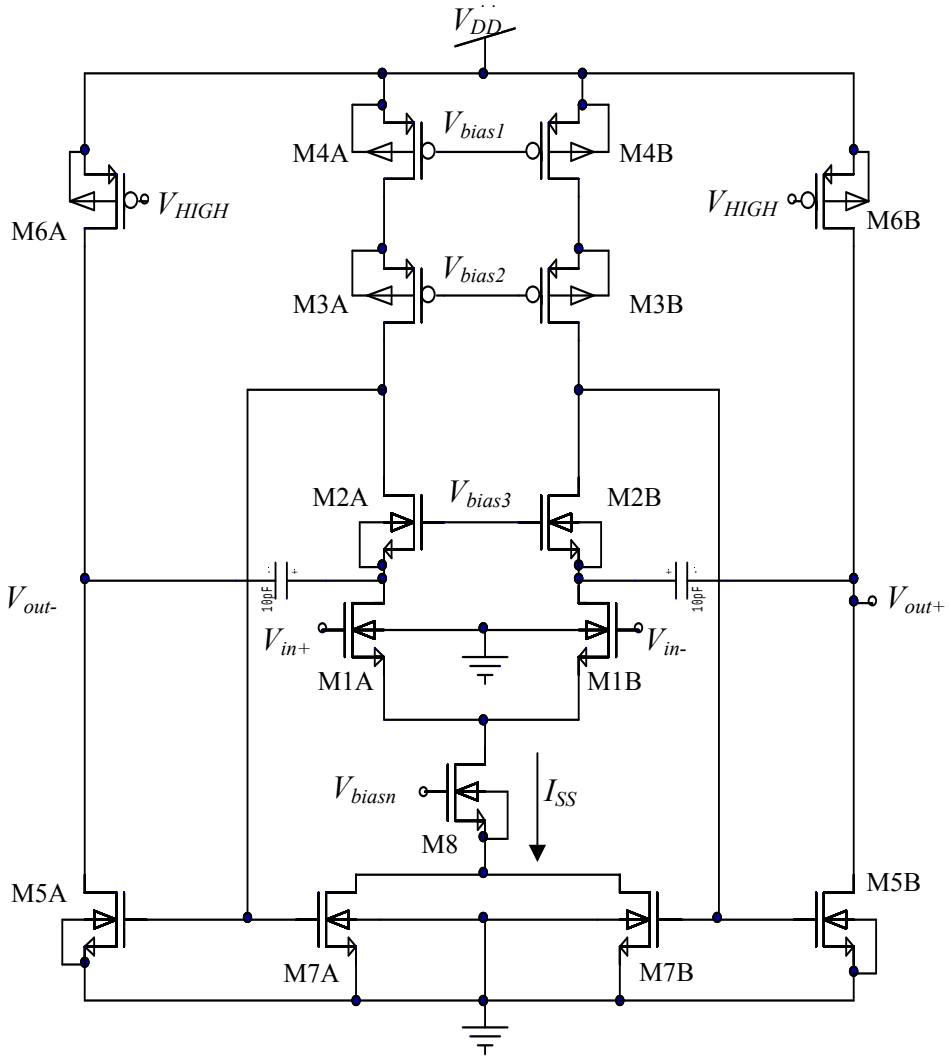


Figure 3.17.

Circuit schematic of the two-stage telescopic amplifier [68].

Since offset, which is a source of non-linearity, can be increased between the two stages, two offset reduction techniques are employed in this circuit. The first method is the introduction of coupling capacitors between the stages, and the second through the use of internal feedback. In Figure 3.17 it can be seen that the output of the first amplifier stage is directed back into the NMOS pair M7A and M7B. Both of these transistors operate in the triode region for tuning of the tail-current.

Feedback analysis

From (3.28) the closed loop gain of an amplifier is given by

$$A_f \equiv \frac{v_O}{v_i} = \frac{A_o}{1 + A_o \beta} \tag{3.37}$$

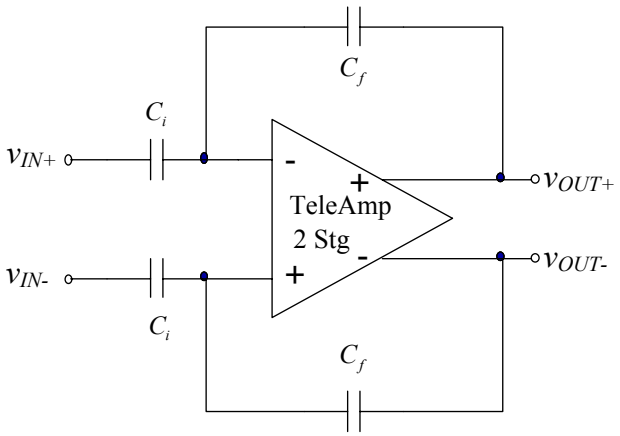


Figure 3.18.

Feedback configuration used with the two stage telescopic amplifier.

The feedback of this system utilises capacitive feedback. For the feedback configuration shown in Figure 3.18, the closed loop gain can be written as [31]

$$A_f = \frac{C_i}{C_f}\frac{A_v}{\beta^{-1} + A_v} \tag{3.38}$$

where C_i is the input capacitance, C_f is the feedback capacitance and β is the feedback factor given by

$$\beta = \frac{C_f}{C_i + C_f} \tag{3.39}$$

Since $A_v\beta \gg 1$ the gain of the feedback structure can be approximated as

$$A_f = \frac{C_i}{C_f}\left(1 - \frac{1}{\beta A_v}\right) \tag{3.40}$$

The factor $1/\beta A_v$ is referred to as the settling accuracy (ε_s) of the amplifier. Solving this for C_f to yield a closed loop gain of 2, with the open loop gain being 1000 V/V and choosing C_i = 1 pF yields C_f = 0.5 pF.

The layout of the telescopic amplifier is shown in Figure 3.19.

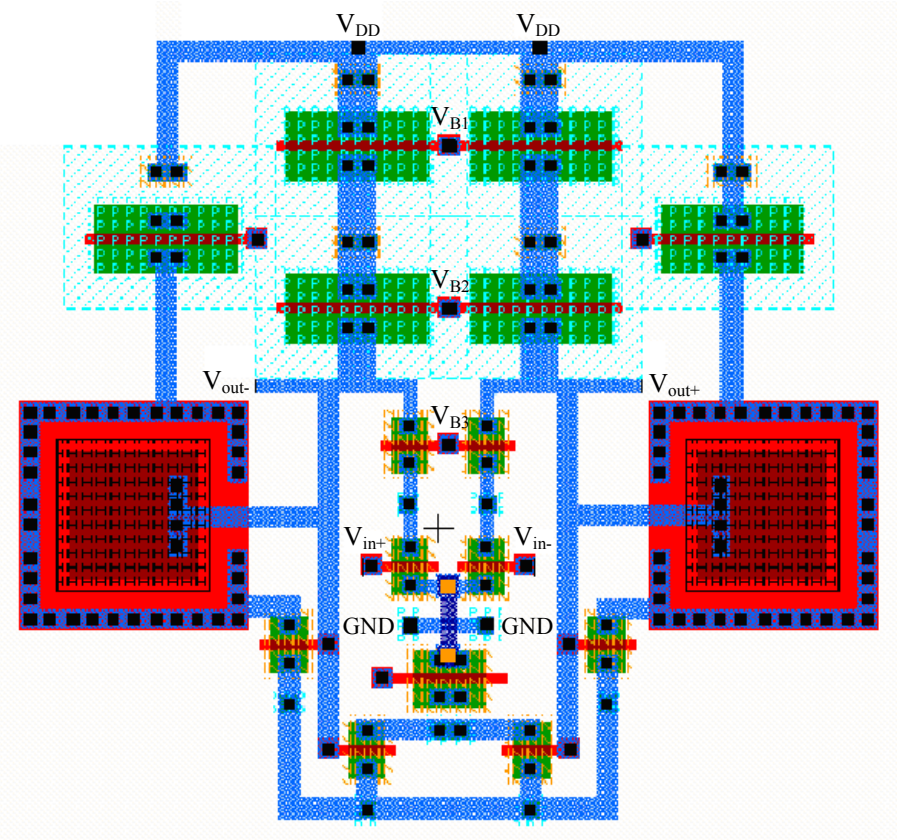


Figure 3.19.

Circuit layout for the two stage telescopic amplifier.

Simulation results

Figure 3.20 shows that the amplifier has a very steep transfer curve. To calculate the gain of the circuit the gradient of the transfer curve in its linear region was calculated using the equation for a straight line. Hence the gain is calculated as

$$Gain = |Gradient| = \frac{v_{OUT,f} - v_{OUT,i}}{v_{IN,f} - v_{IN,i}} = \frac{2.96}{1.786 \times 10^{-3}} = 1657.3 \text{ V/V} \qquad (3.41)$$

which is equivalent to 64.39 dB.

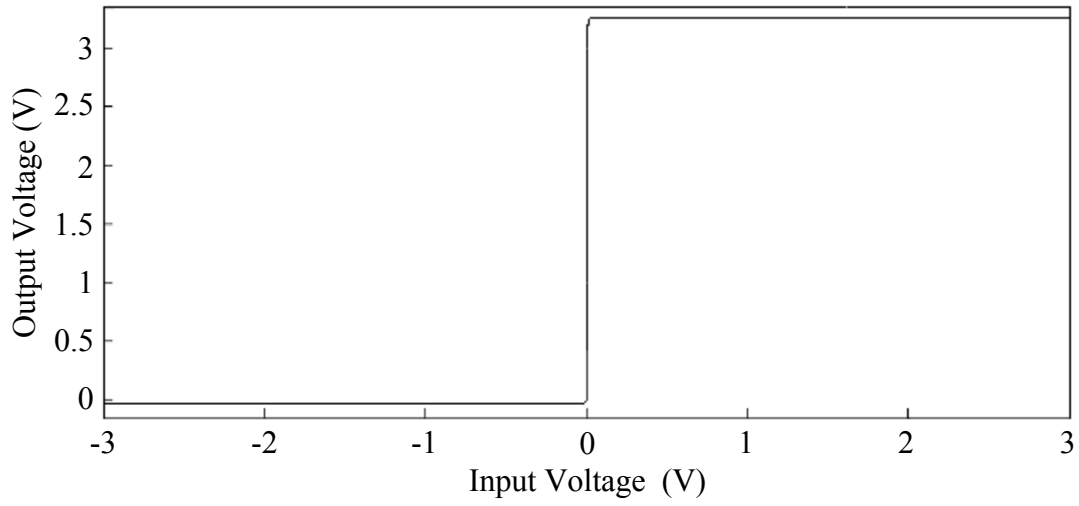


Figure 3.20.

DC transfer characteristic of the two-stage telescopic amplifier.

The AC analysis demonstrates (in Figure 3.21) a 3 dB cut-off frequency of 30 MHz and a unity gain bandwidth of just over 1 GHz.

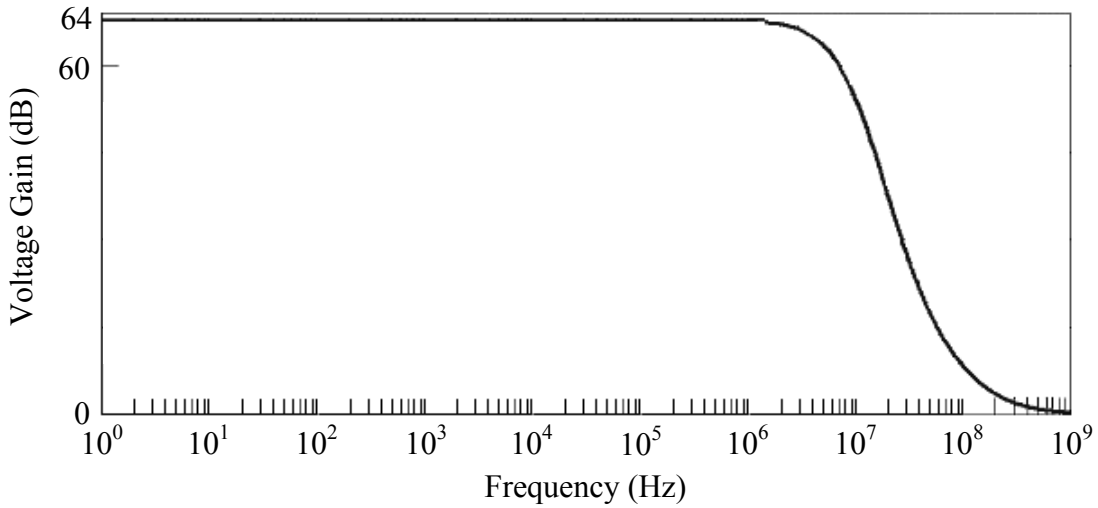


Figure 3.21.

AC sweep performed on the telescopic amplifier implemented.

3.5 Mixer design

This section briefly covers the different types of mixer topologies available; namely the FET and BJT mixer topologies suitable for microelectronic integration. Description and the typical layout of an image rejection mixer that can remove unwanted mixing images are also shown in this section. The section then briefly covers the noise types generally found in mixing systems and the causes of these noise signals.

The latter part of the section details the simulation results for the mixer implemented for this thesis.

FET Mixers

FETs can be used as mixers in both their active and their passive modes. Active mixers using FETs are transconductance mixers that use the local oscillator (LO) to vary the transconductance of the transistor. The advantage of using this method of mixing is that the system can have conversion gain as opposed to loss[6] and that active systems generally have lower noise figures than that of passive designs. Figure 3.22 shows the typical topology for a mixer of this type.

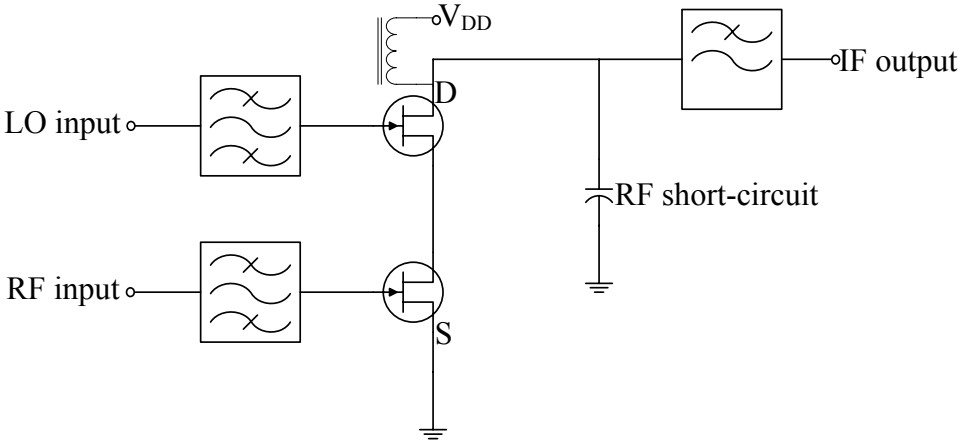


Figure 3.22.

General topology for an active dual FET mixer topology.

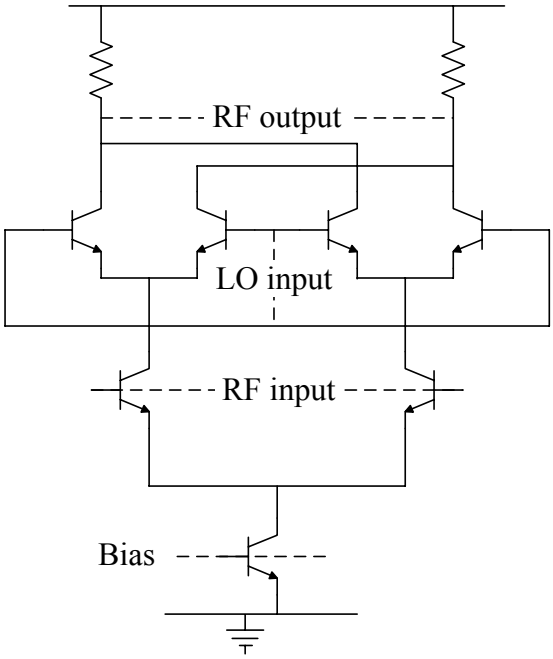
In Figure 3.22 the RF signal is applied to the bottom transistor, which is matched using standard amplifier design techniques, with the IF frequency applied to the top device. The reason for the RF choke on the output of the system is so that the value of the transistor V_{DS} does not move significantly from its DC bias point when the LO is applied. One advantage of this method of mixing is that the IF and RF signals are inherently isolated from each other. A disadvantage of this mixing type is that the system will have lower linearity than the passive design methods.

BJT mixers (Barry Gilbert Mixers)

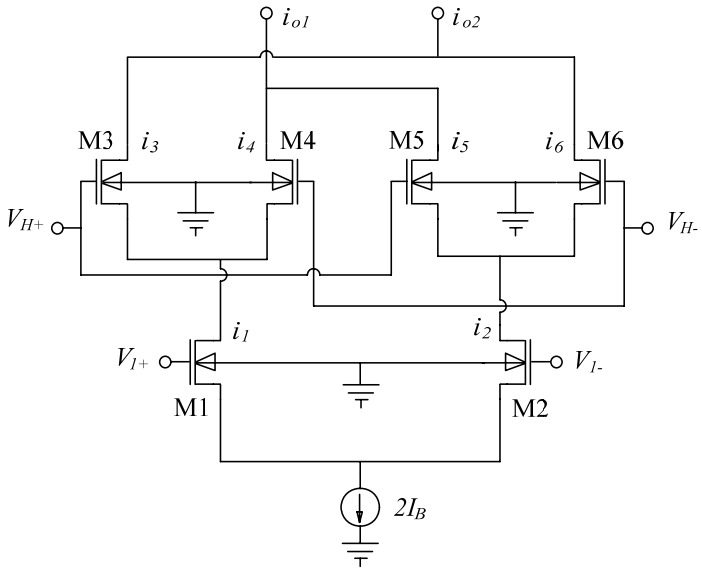
Discrete bipolar mixers are low cost, low power mixers. There are a wide range of commercially available Si bipolar integrated transceivers, each containing a mixer implementation. When transistors are fabricated close to each other on an IC, such as that proposed in this thesis, they tend to behave similar to one another, meaning that they are well matched. This matching allows the design of a Gilbert Cell mixer, as shown in Figure 3.23 (a) [36].

[6] Conversion loss is the ratio of the wanted signal level to the input signal, expressed in dB

The mixer shown in Figure 3.23 (a) is essentially a multiplication device that multiplies the RF signal by ±1 at the LO frequency. In order for this to occur the transistor devices have to be matched with one another; this requires that the system is active and therefore impractical in a discrete implementation. Unfortunately BJT mixers tend to have lower linearity than other mixer types. However, the Gilbert cell can be implemented by using MOSFET devices in order to increase the linearity of the system; such a configuration is shown by Figure 3.23 (b).



(a)



(b)

Figure 3.23.

(a) Double balanced Gilbert cell topology

(b) Gilbert cell topology in MOSFET.

Image rejection mixers

An image rejection mixer is two balanced mixers of any type, driven in quadrature by a RF signal. The RF signal is shifted in phase by 90º and mixed with an in-phase LO signal. This creates four quadrature signals that when shifted again by 90º and added, reinforces the wanted signal and cancel out the unwanted images. Figure 3.24 shows the typical block diagram for an image rejection mixer.

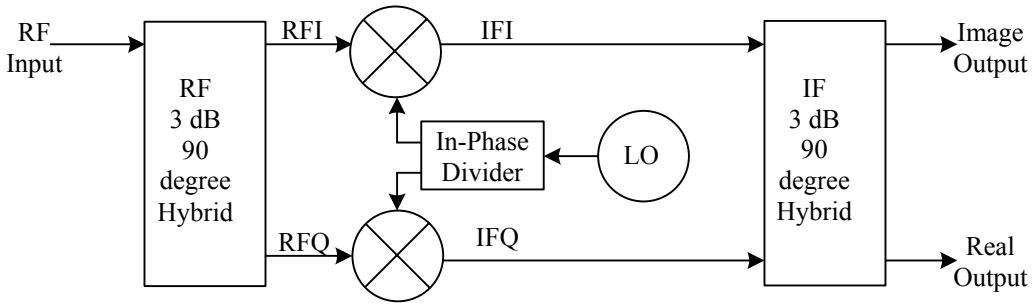


Figure 3.24.

Typical layout of image rejection mixing system

Noise in mixers

Thermal noise

Thermal noise is caused by random thermal motion of electrons in a conducting media. While moving through a conducting media, the large numbers of free electrons that constitute the current collide with ions that vibrate about their normal position in a lattice. The consequence of these random collisions is that the electric current is likewise random.

Thermal noise is directly proportional to the absolute temperature *T,* since the source of this kind of noise is due to the thermal motion of electrons. The probability density function of thermal noise is Gaussian distributed, while the power spectral density is a constant [37]. Since the power spectral density is a constant, thermal noise is a white noise and independent of frequency.

Shot noise

The flow of current is not continuous. It consists of discrete charges equal to the electron charge q (= $1.602.10^{-19}$ C). Shot noise occurs when there is a current flowing across a potential barrier. Fluctuations in the average current are due to random hopping of a charge across this barrier. In semiconductor devices, shot noise manifests itself through the

random diffusion of electrons or the random recombination of electrons with holes. Shot noise is characterized by a Gaussian probability function.

Flicker noise

Also known as, 1/*f* noise, the origin of this kind of noise is not clearly understood. It is observed that flicker noise is most prominent in devices that are sensitive to surface phenomena. This suggests that the source of flicker noise is kinds of defects and impurities that randomly trap and release charge. This charge-trapping phenomenon realises in such a way that it gives rise to a 1/*f* spectrum. The fact that the operating frequency of the mixers that are designed for this thesis is very high means that flicker noise will not be the dominant noise mechanism due to its 1/*f* spectrum.

Mixer implementation

The following list indicates particular characteristics that a mixer must adhere to in order to provide a reliable down or up conversion process within the transceiver of this thesis.

- The mixer must provide good linearity ensuring that the input RF signal is not distorted.
- Noise contributions to the final signal must be kept to a minimum; in order to preserve the signal to noise ratio of the input RF signal
- The local oscillator to intermediate frequency feed through should be minimised; in order to minimise interference generated within the IF band.

The simplest solution to the characteristics of the mixer described earlier is the use of a double balanced Gilbert cell in order to perform the down conversion process. The operation of the mixer can be determined using translinear analysis in Figure 3.23.

This analysis (repeated here, from [71]) disregards second order effects, which means that all AC currents are dependent on the gate source voltage

$$i = k_n' \frac{W}{L}(V_{GS} - V_t)v_{gs} = g_m v_{gs} \tag{3.42}$$

It can be seen that the mixer is biased with constant current source equal to $2I_B$. Drain (and source) currents of transistors M1 and M2 are respectively

$$i_1 = I_B + i_l \tag{3.43}$$

and

$$i_2 = I_B - i_l, \tag{3.44}$$

where i_l is small signal AC current due to the voltage $v_{l+,}$ and $-i_l$ is the AC current due to voltage v_{l-}.

Following the similar analysis procedure the currents through transistors M3, M4, M5 and M6 can be determined as

$$i_3 = \frac{I_B}{2} + \frac{i_l}{2} + i_h \tag{3.45}$$

$$i_4 = \frac{I_B}{2} + \frac{i_l}{2} - i_h \tag{3.46}$$

$$i_5 = \frac{I_B}{2} - \frac{i_l}{2} + i_h \tag{3.47}$$

$$i_6 = \frac{I_B}{2} - \frac{i_l}{2} - i_h \tag{3.48}$$

respectively, where i_h is the current due to the high frequency voltage v_h and $-i_h$ is the current due to voltage v_{h-}. Finally, currents i_{O1} and i_{O2} are $i_3 + i_6$ and $i_4 + i_5$, or equivalently

$$i_{O1} = \left(\frac{I_B}{2} + \frac{i_l}{2} + i_h\right) + \left(\frac{I_B}{2} - \frac{i_l}{2} - i_h\right) = I_B \tag{3.49}$$

$$i_{O2} = \left(\frac{I_B}{2} + \frac{i_l}{2} - i_h\right) + \left(\frac{I_B}{2} - \frac{i_l}{2} + i_h\right) = I_B \tag{3.50}$$

According to this analysis output of the mixer is a DC current of value I_B in both outputs, which makes the device useless.

However, if the second order effects are not disregarded the currents through each of the top four transistors will have additional currents equal to $\frac{1}{2}k'\frac{W}{L}v_{gs}{}^2$ [31], all four flowing from drain to source because they depend on the square of the voltage. This is contrary to the currents due to the first order effects, which alternate the direction. New i_3, i_4, i_5 and i_6 are now

$$i_3 = \frac{I_B}{2} + \frac{i_l}{2} + i_h + i_{so3}, \tag{3.51}$$

$$i_4 = \frac{I_B}{2} + \frac{i_l}{2} - i_h + i_{so4}, \tag{3.52}$$

$$i_5 = \frac{I_B}{2} - \frac{i_l}{2} + i_h + i_{so5} \tag{3.53}$$

$$i_6 = \frac{I_B}{2} - \frac{i_l}{2} - i_h + i_{so6} \tag{3.54}$$

The second order effects in transistors M1 and M2 are not of importance (the currents will cancel) and are therefore excluded in the analysis.

Output currents will thus be

$$i_{O1} = \left(\frac{I_B}{2} + \frac{i_l}{2} + i_h + i_{so3}\right) + \left(\frac{I_B}{2} - \frac{i_l}{2} - i_h + i_{so6}\right) = I_B + i_{so3} + i_{so6} \tag{3.55}$$

$$i_{O2} = \left(\frac{I_B}{2} + \frac{i_l}{2} - i_h + i_{so4}\right) + \left(\frac{I_B}{2} - \frac{i_l}{2} + i_h + i_{so5}\right) = I_B + i_{so4} + i_{so5} \tag{3.56}$$

Further

$$i_{so3} \propto v_{gs3}{}^2, \tag{3.57}$$

$$i_{so4} \propto v_{gs4}{}^2, \tag{3.58}$$

$$i_{so5} \propto v_{gs5}{}^2 \tag{3.59}$$

$$i_{so6} \propto v_{gs6}{}^2 \tag{3.60}$$

But

$$v_{gs3} = v_{h+} - v_{s3,4}, \tag{3.61}$$

$$v_{gs4} = v_{h-} - v_{s3,4}, \tag{3.62}$$

$$v_{gs5} = v_{h+} - v_{s5,6}, \tag{3.63}$$

$$v_{gs6} = v_{h-} - v_{s5,6}, \tag{3.64}$$

$$v_{h+} = v_h, \tag{3.65}$$

$$v_{h-} = -v_h, \tag{3.66}$$

$$v_{s3,4} \propto v_{l+} = v_l \tag{3.67}$$

$$v_{s5,6} \propto v_{l-} = -v_l \tag{3.68}$$

If the constant of proportionality in Equations (3.67) and (3.68) is 1 (which can be done by setting the proper *W*/*L* ratio for M1 and M2), this analysis results in

$$i_{so3} \propto v_h{}^2 + v_l{}^2 - 2v_h v_l \tag{3.69}$$

$$i_{so4} \propto v_h{}^2 + v_l{}^2 + 2v_h v_l \tag{3.70}$$

$$i_{so5} \propto v_h{}^2 + v_l{}^2 + 2v_h v_l \tag{3.71}$$

$$i_{so6} \propto v_h{}^2 + v_l{}^2 - 2v_h v_l \tag{3.72}$$

Then,

$$i_{o1} = i_{so3} + i_{so6} \propto 2v_h^{\,2} + 2v_l^{\,2} - 4v_h v_l \tag{3.73}$$

$$i_{o2} = i_{so4} + i_{so5} \propto 2v_h^{\,2} + 2v_l^{\,2} + 4v_h v_l \tag{3.74}$$

If the two outputs of the mixer are taken differentially the final output current will be

$$i_O = i_{o2} - i_{o1} = 8v_h v_l \quad \text{(mixing is thus evident)} \tag{3.75}$$

In order to determine meaningful results from a mixer design a set amount of benchmarks must be determined in order to qualify the design [38]. For this thesis, the implementation is shown in Figure 3.25.

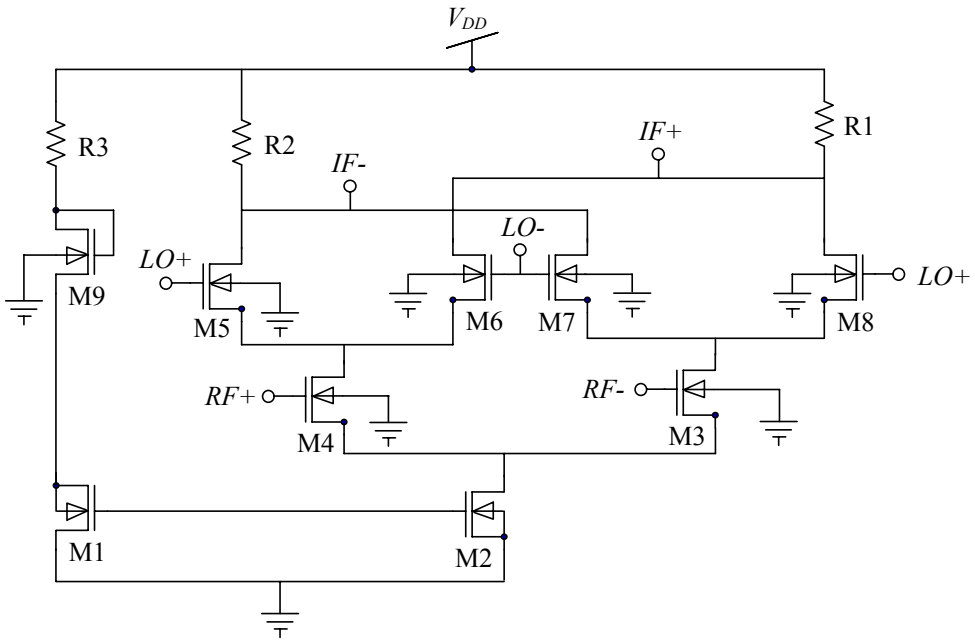


Figure 3.25.

Circuit configuration for a double balanced Gilbert mixer [71].

The forward voltage conversion gain of a mixer is calculated by [31]

$$K_c = \frac{v_{OUT,IF}}{v_{RF}} = \frac{2g_{M4}R}{\pi} \tag{3.76}$$

The voltage conversion gain is a measure of the ratio of root mean square (RMS) output voltage of the mixer to the input RF voltage to the mixer. It is advantageous to have a high forward conversion gain, but this usually comes with the trade off of increased noise power at the output of the mixer.

Linearity is the second benchmark that must be determined. The linearity is a measure of distortion that the mixer creates due to the conversion process. When the branch currents

of the two RF commutation transistors (M1 and M2) are analysed an expression can be determined for the distortion of the input RF signal given by

$$I_{RF+} = \frac{K_n}{2}\left(\frac{W}{L}\right)(V_{GS1} - V_t)^2 \qquad I_{RF-} = \frac{K_n}{2}\left(\frac{W}{L}\right)(V_{GS2} - V_t)^2 \tag{3.77}$$

$$V_{RF} = V_{GS1} - V_{GS2} \tag{3.78}$$

$$V_{RF} = \sqrt{\frac{I_{ss}}{K_n^{'}}} \cdot \left(\sqrt{1 + \frac{\Delta I_{RF}}{I_{ss}/2}} - \sqrt{1 - \frac{\Delta I_{RF}}{I_{ss}/2}}\right) \tag{3.79}$$

$$\Delta I_{RF} = \frac{I_{ss}}{2} \cdot \sqrt{\frac{K_n^{'} V_{RF}^2}{I_{ss}}} \cdot \left(1 - \frac{K_n^{'} V_{RF}^2}{4 I_{ss}}\right) \tag{3.80}$$

where ΔI_{RF} measures the distortion introduced by the mixer and $K_n^{'}$ is the gain parameter of the transistor. I_{SS} is the drain current of transistor M2. The distortion can be determined analytically through the use of the Taylor expansion of the harmonics introduced to the system, given by

$$\begin{aligned} \Delta I_{RF} &= a_1 V_{RF} + a_2 V_{RF}^2 + a_3 V_{RF}^3 + \ldots \\ a_1 &= \sqrt{\frac{K_n^{'} I_{ss}}{4}} \\ a_2 &= 0 \\ a_3 &= -\frac{K_n^{'}}{16}\sqrt{\frac{K_n^{'}}{I_{ss}}} \end{aligned} \tag{3.81}$$

The noise figure of Gilbert's double balanced mixer can be determined by Equation (3.82) [38].

$$NF_{Gilbert} = \frac{\pi^2}{4}\left(1 + \frac{2\gamma}{g_{M4\_RF} \cdot R_s} + \frac{2}{g_{M4\_RF} \cdot R_s \cdot R_3}\right) \tag{3.82}$$

where γ – factor dependent on device gate length (assumed as 3)

where R_s is the source resistance (assumed as 50 Ω)

where R_3 is the load resistance (500 Ω)

Table 3.8 presents the obtained values for the Gilbert cell mixer.

Component	**Value**
L_1-L_9	0.35 µm
W_5-W_8	50 µm
W_4-W_3	100 µm
W_1-W_2 and W_9	5 µm
R_3	500 Ω

Table 3.8.

Component values for the Gilbert cell.

The layout of this circuit is shown in Figure 3.26.

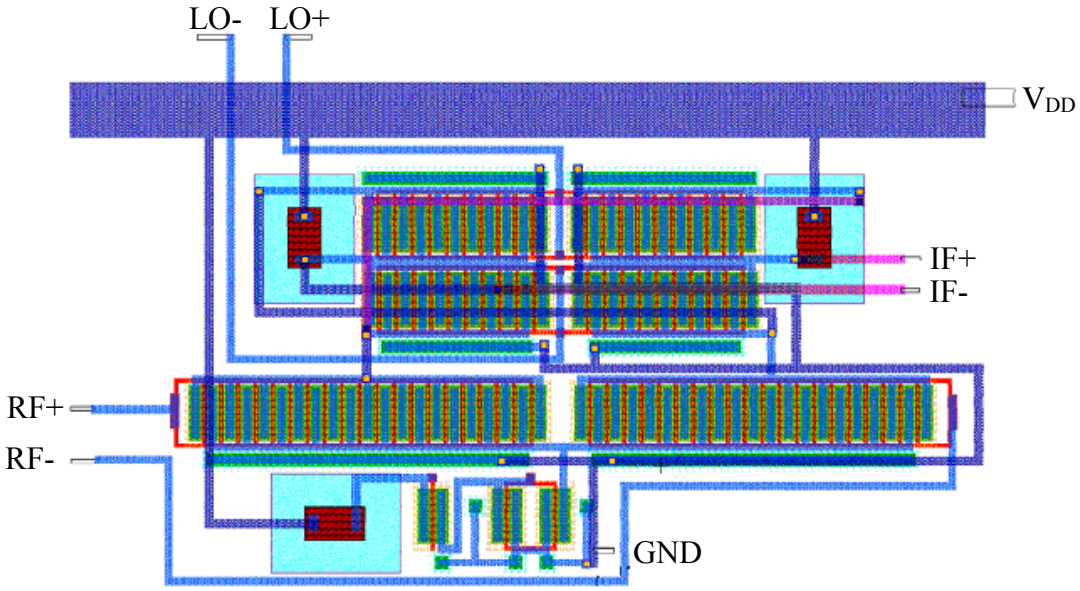


Figure 3.26.

Circuit layout for the mixer.

Simulation results

Figure 3.27 shows successful test simulation results of this circuit (Figure 3.25) with high frequency and lower frequency sinusoidal waves as inputs.

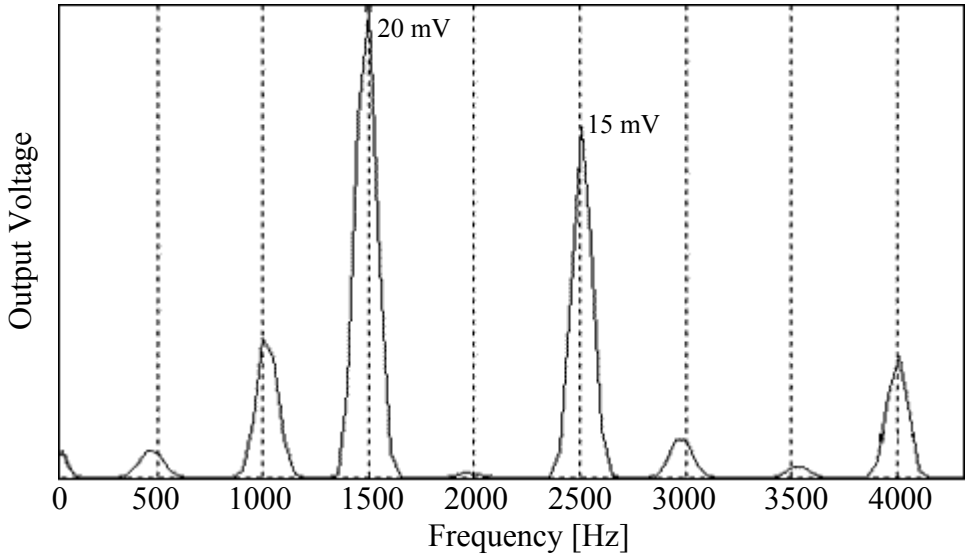


Figure 3.27.

Mixer tested with two signals, one at 0.5 GHz, and other at 2 GHz.

Intercept point is defined in Fig. 3.28. The input power is plotted along the horizontal axis, and output power is plotted along the vertical axis. Two lines are plotted: one relating IF

output power to RF input power, and another relating intermodulation output power to RF input power.

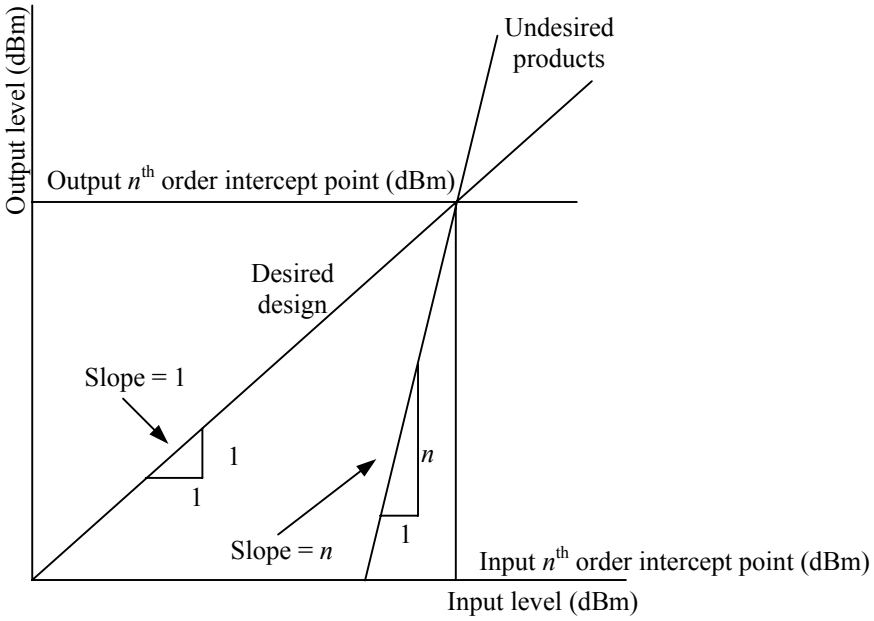


Figure 3.28.

Definition of Intercept Point.

The point at which these lines intersect gives the input and output intercept points for the mixer at a particular set of input frequencies for a given LO power level and temperature. For the mixer designed for this thesis, the intercept point is obtained as in Fig. 3.29.

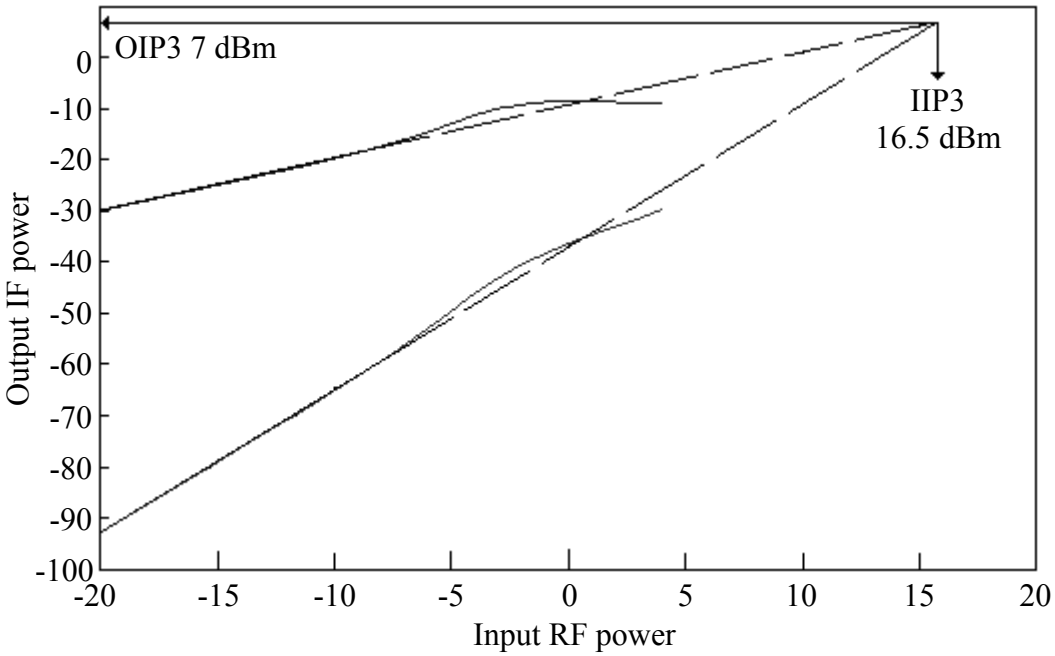


Figure 3.29.

Plot of first and third harmonic outputs of the mixer.

The third intercept point (IIP3) is given by (for long channel devices) [38]:

$$IIP3 = 4\sqrt{\frac{2}{3}}\left(V_{gs} - V_t\right) = 2.8 \tag{3.83}$$

3.6 LNA design

Within any modern RF IC design, the use of a low noise amplifier (LNA) has become pivotal in determining the success of a system's operation. The objective of the LNA is to amplify the incoming signal without the addition of any unnecessary noise produced by the circuit.

Another objective of the LNA is to provide input matching to the characteristic impedance of the RF input signal. This has the consequence that the LNA absorbs the input power of the RF input signal so that it can be amplified.

An LNA is an important sub-system of the receiver, as the overall noise figure (NF) of the RF front end is scaled by the LNA gain. All the subsequent noise figures subsequent to the LNA are scaled by the LNA gain demonstrated by Friis' formula:

$$NF_{receiver} = \left(\frac{1}{G_{LNA}}\right)(NF_{subsequent\_stages} - 1) + NF_{LNA} \tag{3.84}$$

The operation of an LNA entails some of the aspects listed below.

- To transform the characteristic input impedance, while retaining stability during operation.
- Amplifying the input signal to level that is of use to the rest of the system.
- To finally transform the output signal of the amplifier in order to attain maximum power transfer without the addition of unnecessary noise.

Figure 3.30 shows the different operations performed by the LNA.

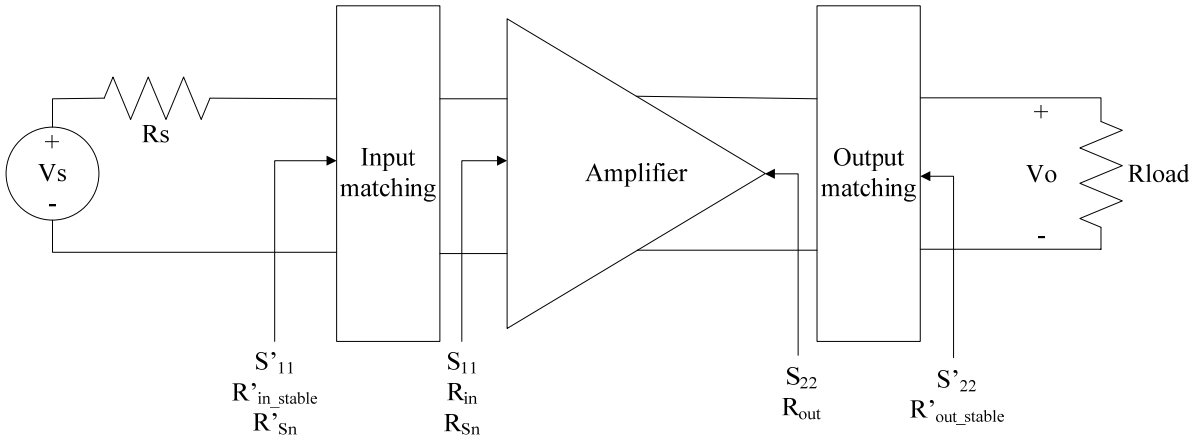


Figure 3.30.

Different stages of an LNA operation.

With reference to Figure 3.30 the scattering parameters (S-parameters) are indicated upon the figure, where S_{11} is the input reflection coefficient and S_{22} is the output reflection coefficient. The simultaneous use of a power-constrained noise and input matching technique was applied to the differential cascode configuration [39]. The cascode LNA (Fig. 3.31) uses an inductive degeneration topology in order to provide a real part matching to the input RF source. Coupled with the inductive degeneration topology an L matching network is used in order to match for S_{11}.

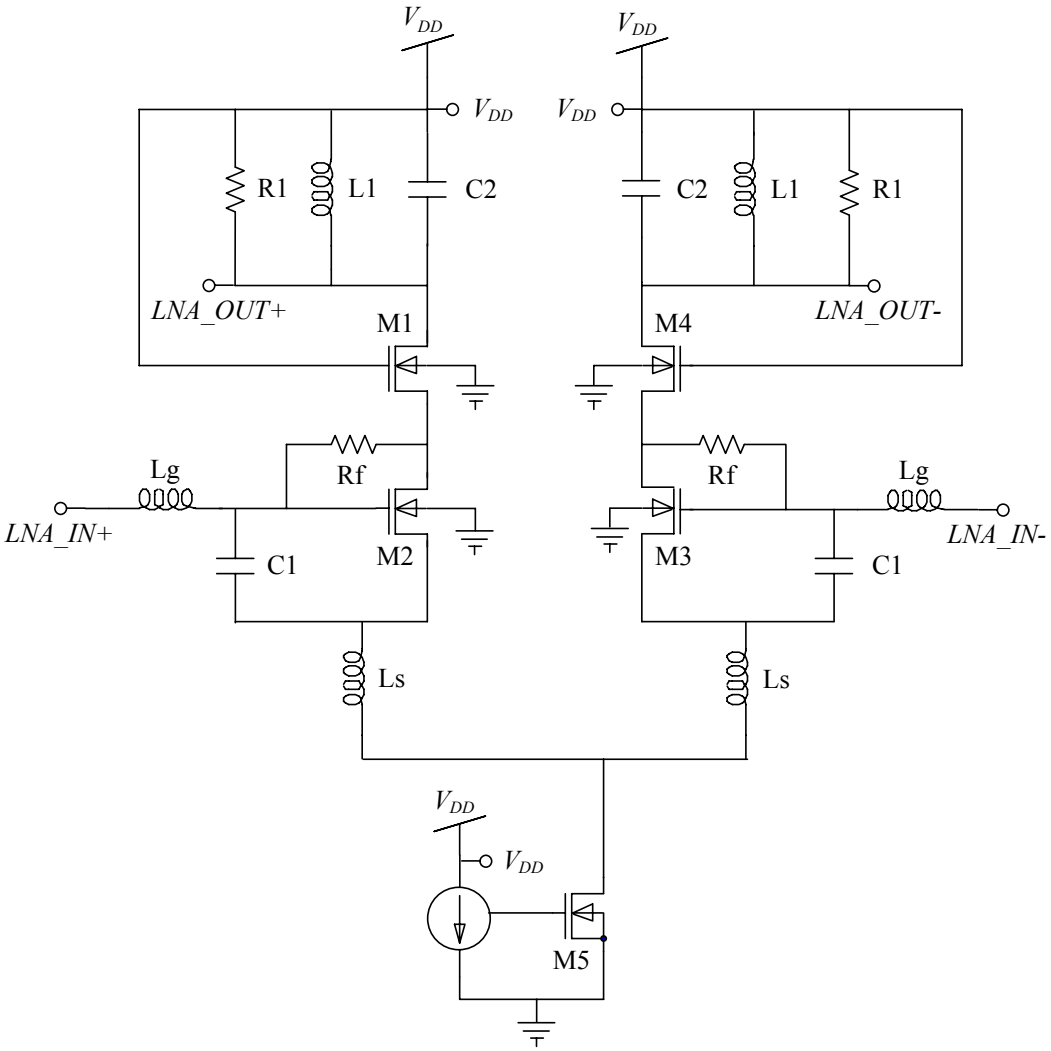


Figure 3.31.

Cascode differential LNA circuit – basic topology adapted from [40].

It can be shown that for one branch of the LNA (M1 and M2) that the noise figure is given by

$$NF = 1 + \frac{2}{3g_{M3}R_s} \tag{3.85}$$

where g_{m3} is the transconductance of MOSFET M3 and R_S the equivalent noise resistance of the source. In order to provide input matching both the real and imaginary part of the characteristic input impedance must be matched to the input impedance of the amplifier. It can be shown that from the small signal model of the M1 and M2 branch that the input impedance of the LNA is represented by

$$
\begin{aligned}
Z_{in} &= j\omega(L_g + L_s) + \frac{1}{j\omega C} + g_{M3}\frac{L_2}{C} \\
\text{Choosing } &\frac{1}{\omega C} = \omega(L_g + L_s) \\
\Re\{Z_{in}\} &= g_{M3}\frac{L_s}{C} \\
\Im\{Z_{in}\} &= j\omega(L_s + L_g) + \frac{1}{j\omega C}
\end{aligned}
\tag{3.86}
$$

where C = C_{gs} + $C_{1,}$ it is worth noting that the addition of C_1 to the transistor lowers the overall unity gain frequency of the transistor [41].

By matching the components to real and imaginary condition of Z_{in} the noise figure can be simplified to [40]

$$NF = 1 + \frac{2}{3}\frac{1}{1 + \frac{L_g}{L_s}} \tag{3.87}$$

The transistor M1 is set to a specific transconductance value through the use of the current source M5 and correct biasing of V_{GS}. The transconductance can be determined by

$$g_{M3} = \sqrt{I_{M5}k_n'\left(\frac{W_3}{L_3}\right)} \tag{3.88}$$

By setting W_3 = 200 µm and L_3 = 0.35 µm and using k_n' is 170 µA/V, equation (3.88) can be simplified to:

$$g_{M3} = \sqrt{I_{M5}}\,0.3116 \tag{3.89}$$

The voltage gain of the LNA [40] is given by

$$A_v = \frac{L_1}{L_s(1 - \omega_c^2 L_1 C_2)} \tag{3.90}$$

Using the above-mentioned relations the LNA was designed for an f_c of 2.4 GHz. The final values obtained for the LNA is tabulated in table 3.9.

Parameter	Value
L_1-L_4	0.35 µm
W_1-W_4	200 µm
Number of gate fingers	40
L_s	2 nH
L_g	6.2 nH
C_1	500 fF
C_2	1.2115 pF
L1 (Inductor)	8 nH

Table 3.9.

Transistor parameters and component values required for the LNA.

The layout of this circuit is shown in Figure 3.32.

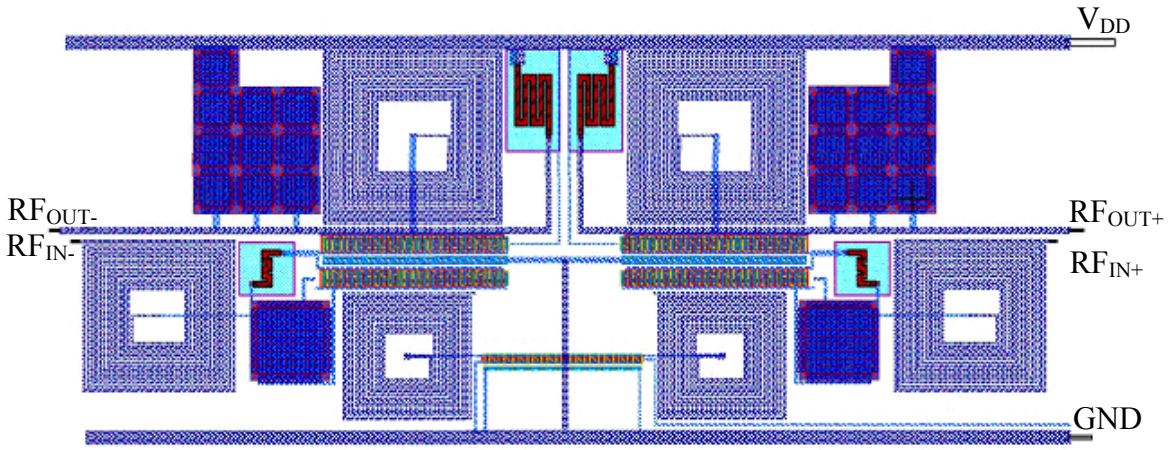


Figure 3.32.

Circuit layout for the LNA.

The noise figure predicted by equation (3.87) is about 1.2 dB. For the differential topology, the figure will be twice this value, thus about 2.4 dB.

Simulation results

The S_{11} parameter can be determined by

$$Z_{in} = \frac{V_{in}}{I_{in}}$$
$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \qquad (3.91)$$

The simulated parameters are shown in Figures 3.33-3.35.

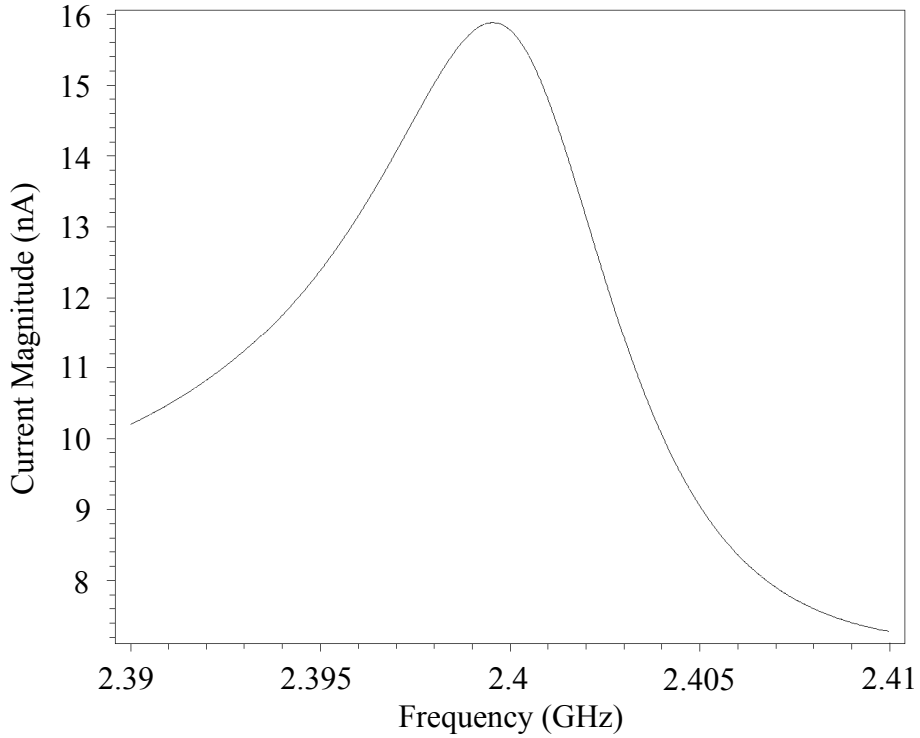


Figure 3.33.

Input current of the LNA.

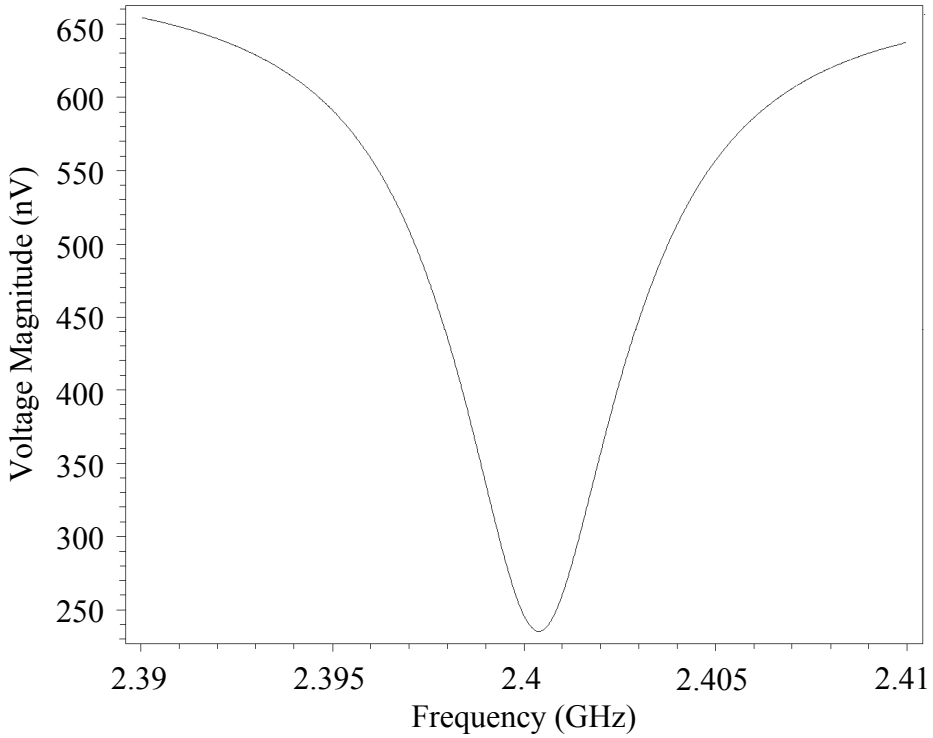


Figure 3.34.

Input voltage to the LNA as a function of input frequency.

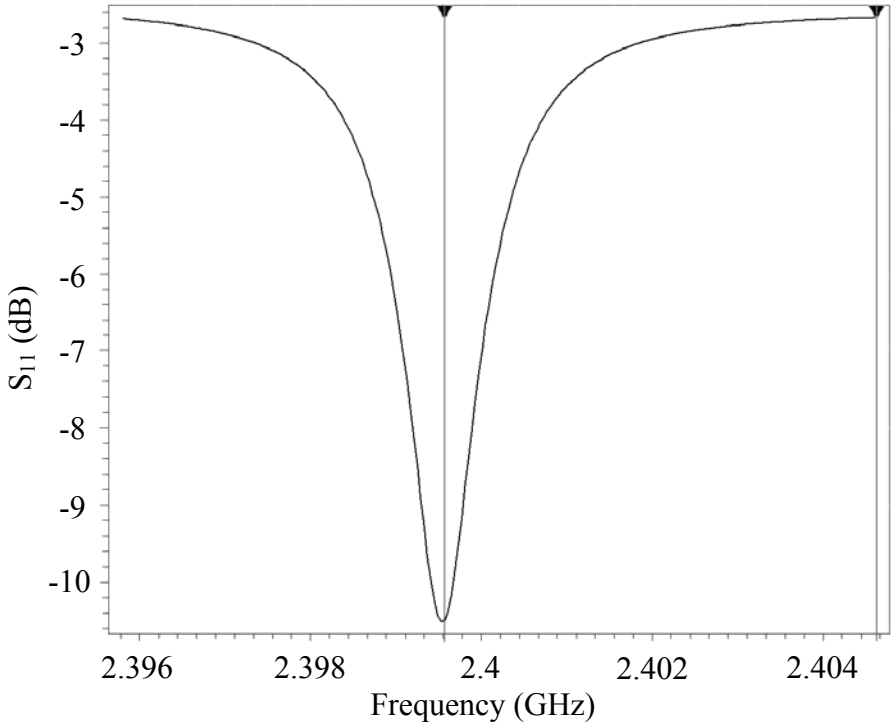


Figure 3.35.

S_{11} input parameter of the LNA.

The input port reflection coefficient was found to be -10.5 dB at 2.3988 GHz. The gain of the LNA is measured:

$$Gain_{dB} = 20\log_{10}\left(\frac{v_{out}}{v_{in}}\right) \tag{3.92}$$

Figure 3.36 plots this gain.

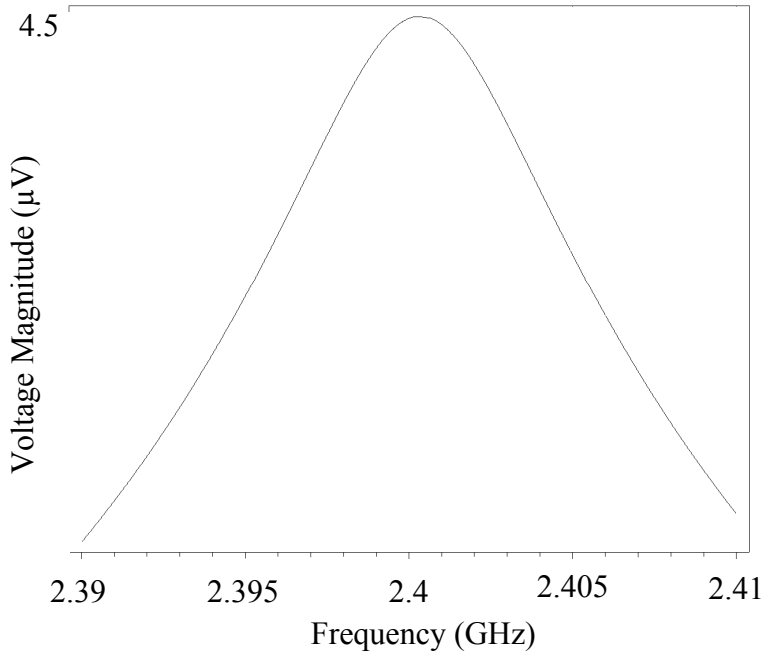


Figure 3.36.

Measurements of the LNA gain (for a 250 nV input).

From Figure 3.36, it can be seen that the LNA has a peak voltage gain of about 25 dB at 2.4006 GHz. Figure 3.37 plots the LNA input referred noise.

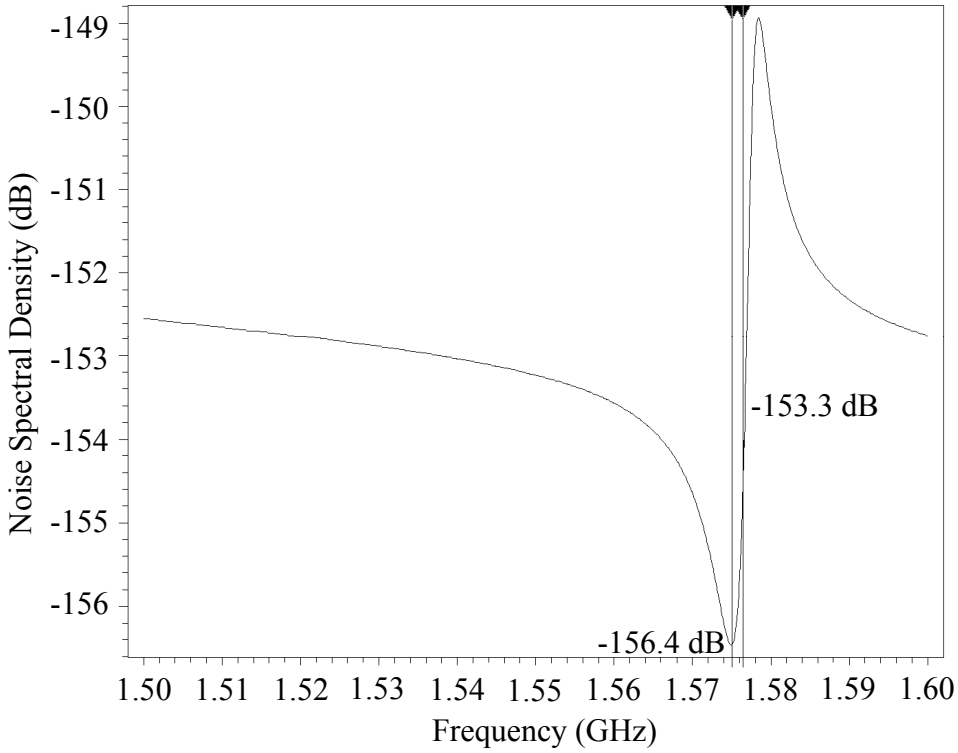


Figure 3.37.

Simulation to determine the LNA input referred noise.

Noise figure is the noise factor, expressed in dB.

It can be seen from Figure 3.37 that the LNA has noise figure of 3.1 dB (-153.3 dB-(-156.4 dB)) in the bandwidth of interest.

3.7 Active Inductor design

This section discusses the design of active inductors used in the filtering and oscillation sub-systems of this thesis. The active inductors designed are somewhat limited due to their larger power consumption [42; 63].

Active inductors are available in many forms depending on the usage for which the design is intended. The two configurations used in the system of this thesis are the push-pull gyrator-C and the push-push intrinsic-C model [43]. The inductance of the devices shown in Figure 3.38 is realized by the combination of the two transistors in such a way that the two active devices realise the high frequency characteristics of a normal inductor. The

inductor system is unfortunately extremely dependant on the intrinsic capacitances of the transistor models.

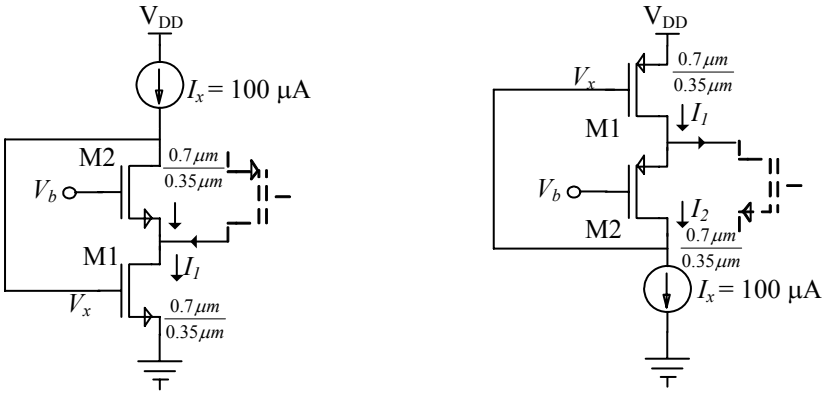


Figure 3.38.

Basic layout for two possible configurations resulting in active inductance [56].

Various kinds of active inductors have been proposed for on-chip design [42, 43]. A common feature of these active inductors is that all active inductors feature a form of shunt feedback to emulate inductive impedance. A small signal model is shown in Figure 3.39.

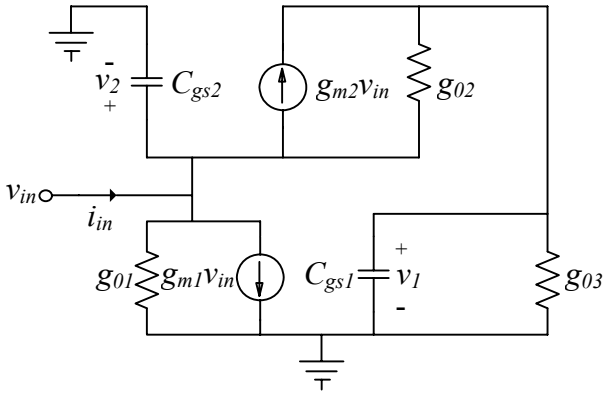


Figure 3.39.

Small signal model for the active inductor system.

The small-signal current can be derived as shown in equation (3.93):

$$i_{in} = \left[\left(g_{o1} + g_{m2} \right) + sC_{gs2} + \frac{g_{m1}\left(g_{m2} + g_{o2} \right)}{sC_{gs1} + g_{o2} + g_i} \right] v_{in} \tag{3.93}$$

where g_m and g_o are the transconductance and output conductance of the corresponding transistors, g_i is the output conductance of current source, and C_{gs} is the gate source capacitance.

The inductive effect of the circuits can be understood as follows. Since the circuits use shunt feedback at the input node, the impedance seen at low frequencies is relatively small.

When the frequency increases the gate-source capacitance will cause a drop in the feedback loop gain, thus, input impedance will increase with frequency, simulating the effect of an inductive element.

By analogy, the following expressions can be derived from equation (3.93):

$$C_p = C_{gs2} \tag{3.94}$$

$$R_p = \frac{1}{g_{o1}} \| \frac{1}{g_{m2}} \approx \frac{1}{g_{m2}} = \frac{1}{\sqrt{2K_n'(\frac{W_2}{L_2})I_2}} \tag{3.95}$$

$$R_s = \frac{g_{o2} + g_{o3}}{g_{m1} g_{m2}} \tag{3.96}$$

$$L_{eff} = \frac{C_{gs1} + C_{gd1} + C_{gd2}}{g_{m1} g_{m2}} \approx \frac{C_{gs1}}{g_{m1} g_{m2}} \tag{3.97}$$

By analysis of the above small-signal model and the Equations (3.94-3.97), the RLC model of Figure 3.40 can be derived.

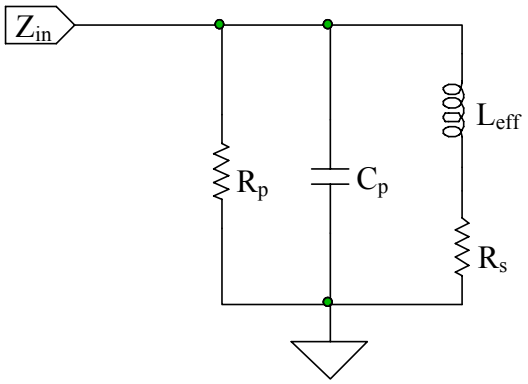


Figure 3.40.

Equivalent circuit derived from the small-signal model.

The self-resonant frequency of the active-inductor is:

$$\omega_t^2 = \frac{g_{m1} g_{m2}}{C_{gs1} C_{gs2}} = \omega_{t1} \omega_{t2} \tag{3.98}$$

where ω_{t1} and ω_{t2} are the unity current gain frequencies of M1 and M2 respectively. The Q value is approximately:

$$Q = \frac{R_p}{\omega_t L_p} = \sqrt{\frac{\omega_{t1}}{\omega_{t2}}} \tag{3.99}$$

For $\omega > \omega_t$: the circuit will become capacitive, so a higher ω_t is preferred. From equation (3.98), smaller values of L_1, L_2 and larger biasing currents (I_1 and I_2) will increase ω_t. While from equations (3.95) and (3.99), increasing I_2 means that the equivalent parallel

resistance, R_p and Q will be reduced. To increase ω_t without degrading the Q-factor of the active inductor, a folded DC coupling structure as shown in the dashed part of Fig. 3.38 can be used [43]. The biasing current from the other stages (for example, the input transconductance stage) is reused by M_1 while I_2 is kept the same, thus a higher ω_t and Q factor can be obtained. Since the current is reused by other stages, the power consumption is also well contained.

In order to reduce the noise seen in the system due to the resistive effects of the inductive current and increase the Q factor of the overall system a negative impedance converter (NIC) is required. The design of this device is simple; a negative g_m configuration is used to cancel out the resistor R_p of the active inductor.

The layout of the negative g_m configuration is shown in Figure 3.41.

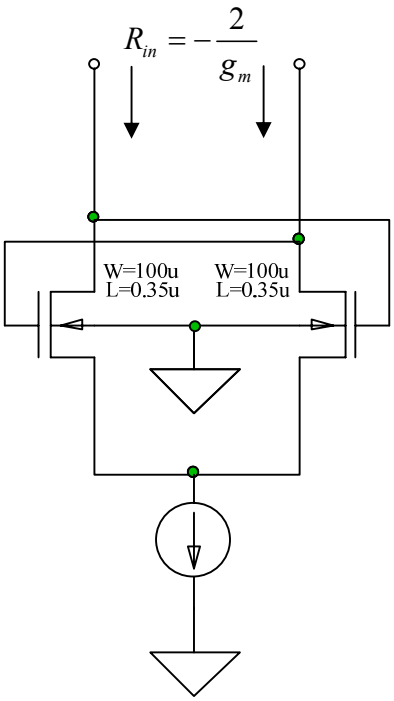


Figure 3.41.

Negative g_m transistor circuit.

The resistance created by the above circuit is given by the following equation:

$$R_{in} = -\frac{2}{g_m} \tag{3.100}$$

This resistive effect of the two matched transistors of the negative impedance circuit is used to cancel out the resistance represented by resistor R_p of Figure 3.41. Figure 3.42 shows the equivalent RLC model of the NIC. The relatively small capacitance added to the circuit will have negligible effects if a discrete capacitor is used to force a device to a required resonance, their effects must however be considered in designs where the intrinsic resonance frequency is used to create an oscillation tank.

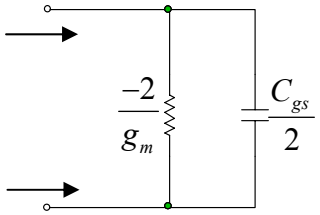


Figure 3.42.

RLC model of a NIC.

Thus,

$$R_p = \left| \frac{2}{g_m} \right|. \tag{3.101}$$

Active inductor oscillator and control

Conventional LC oscillators depend on a combination of inductors and capacitors to realize a resonance tank, necessary for generating the poles required for oscillation. This sub-system does the same but without the use of on-chip inductors. An active inductor topology was implemented in a negative g_m configuration, where active devices and capacitances were used to create an inductive effect. In summary, a NMOS and a PMOS device as well as two current sources were used, to produce a grounded inductor [44]. The inductance can be varied by varying the device transconductances.

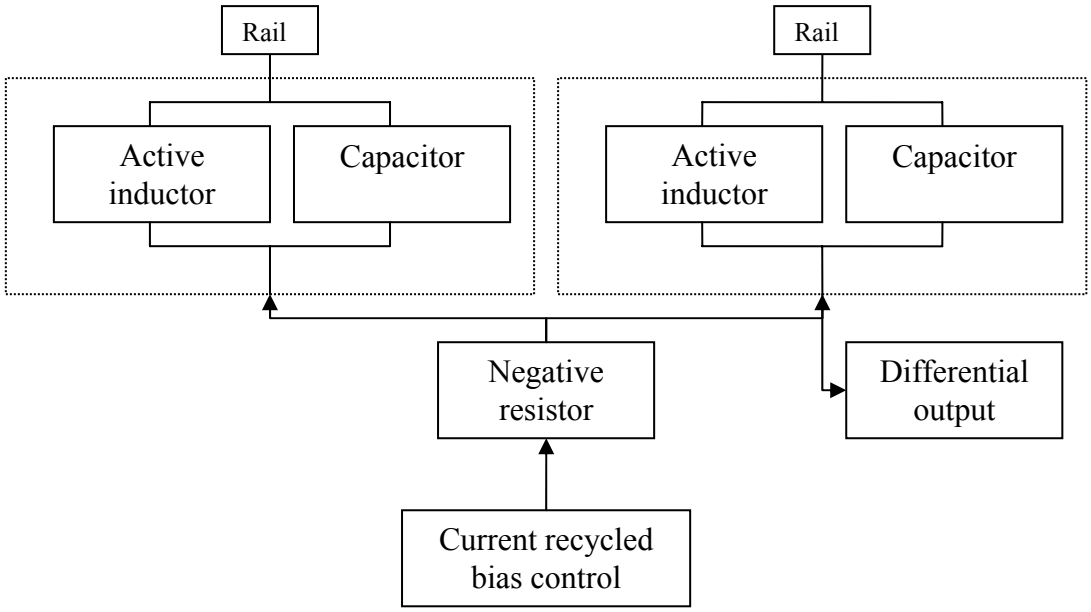
The frequency of oscillation is determined by the effective parallel capacitance and inductance in parallel

$$f_{out} = \frac{1}{2\pi\sqrt{LC}} \tag{3.102}$$

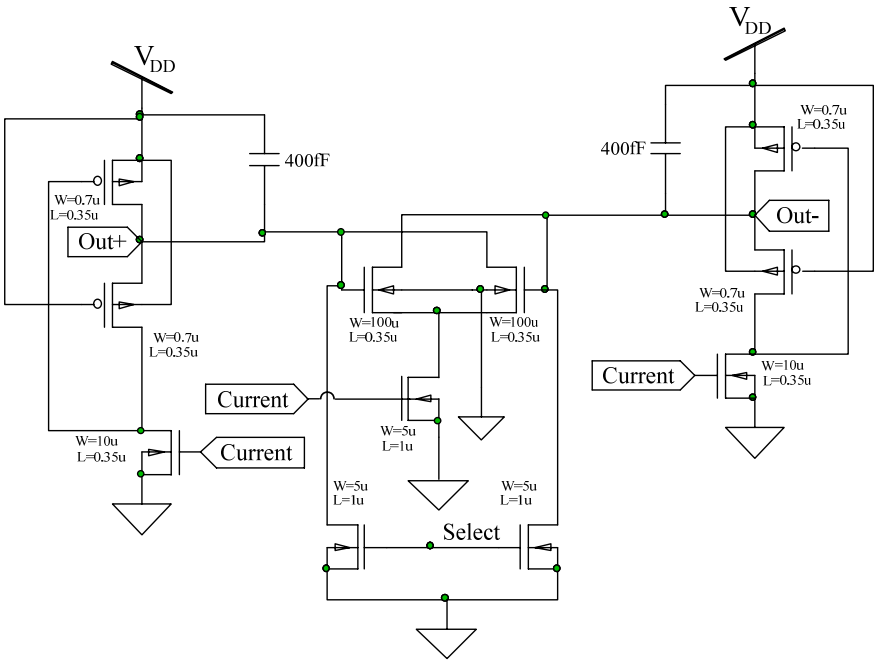
where L and C refers to the total parallel inductive and capacitive components, respectively. The resistive component was cancelled by the NIC, resulting in oscillations at the frequency specified in Equation (3.102).

A capacitor was connected to the active inductor inputs, where the value of the capacitor was chosen to be much larger than the intrinsic device capacitances. This forces the

capacitance value to be a nearly fixed value as opposed to a variable that is dependant on the aspect ratio of the transistor. The capacitor also served to reduce the phase noise content of the VCO output, as well as restrict the sensitivity of the active device to process variations in the transistor components. The VCO is shown in Figure 3.43.



(a)



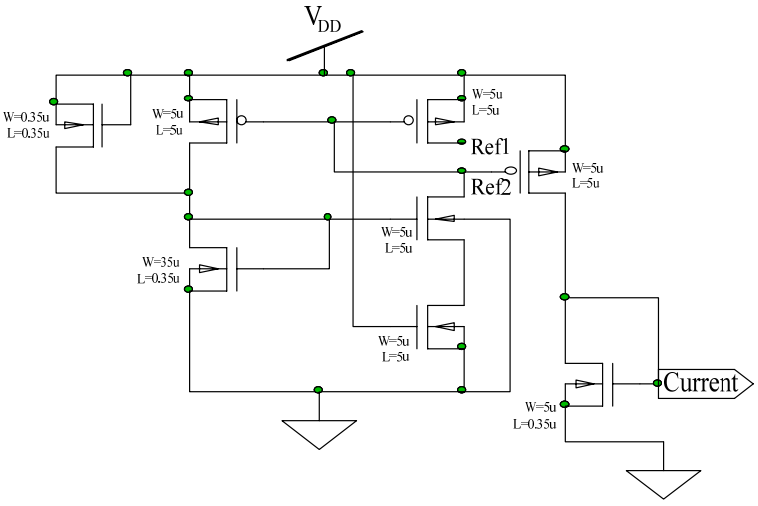
(b)

Figure 3.43 [56].

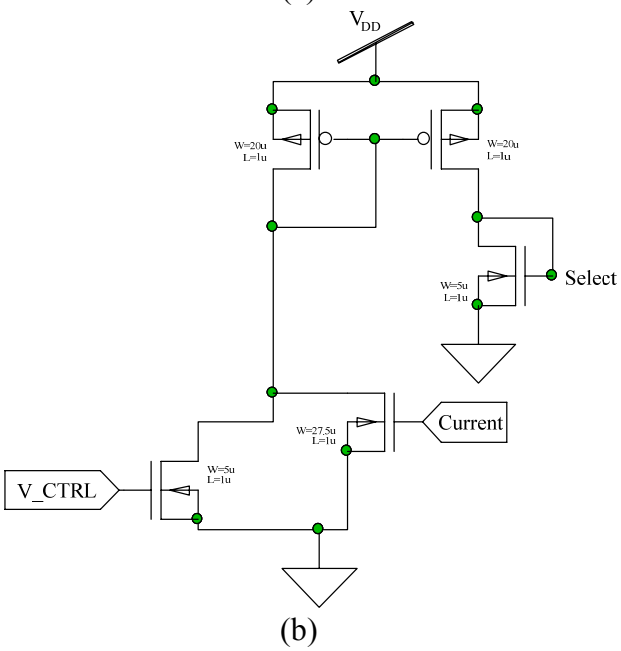
(a) Active inductor oscillator block diagram.

(b) Active inductor oscillator schematic. The current is generated as per Fig. 3.44 (a).

The frequency of oscillation was controlled by varying the resonant inductance. By biasing a transistor with an input control voltage (Fig. 3.44), the output of the current source (Fig. 3.38) could be adjusted (select input). This adjusted value was used as a reference in the biasing of the active transistor (transistors drawn in dashed lines in Fig. 3.38). By doing so the device Q-point can be shifted, allowing the adjustment of the inductive value and thus the frequency of oscillation. Figure 3.44 shows the schematic of the controlling circuit for the active inductor circuit shown in Figure 3.43. The resonant frequency of the inductor circuit is controlled by adjusting the biasing of each transistor separately to one another (current recycling) [44].



(a)



(b)

Figure 3.44.

(a) Current source (similar to the current terminal, Ref1 & Ref2 go to other points in the circuit – this has not been shown for clarity).

(b) Control circuit to adjust the frequency of oscillation for the active inductor.

The layout of the oscillator is shown in Figure 3.45.

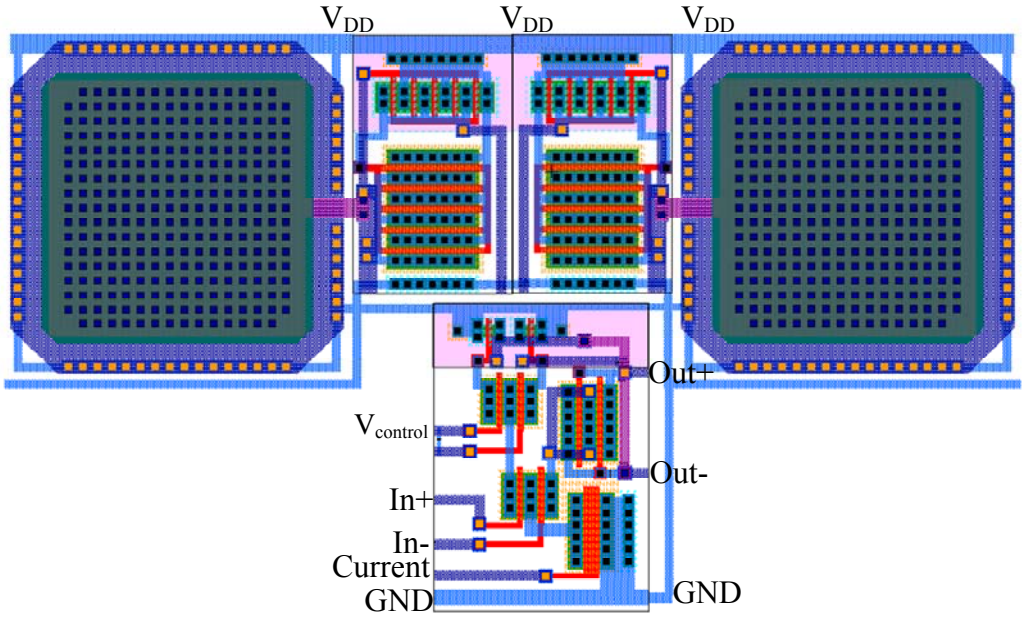


Figure 3.45.

Circuit layout for the active inductor oscillator. The output of the oscillator feeds into a mixer (also shown in this layout).

Simulation results

The frequency/voltage gain of the VCO is an important parameter, and can be depicted in form of the VCO output frequency as a function of input voltage range as shown in Figure 3.46. The output frequency of the VCO is dependant on the input current to the biasing section of the negative g_m resistor configuration.

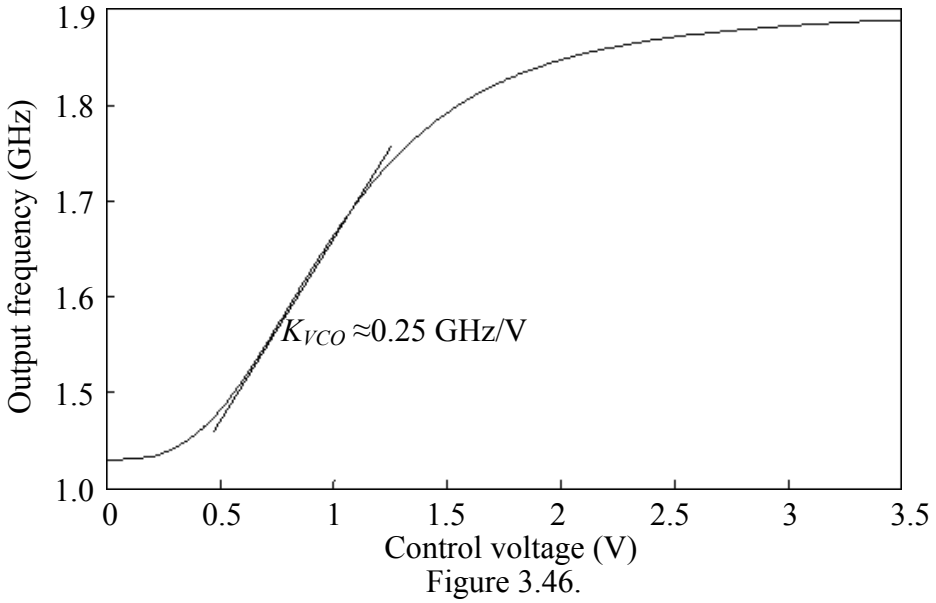


Figure 3.46.

Plot of the output frequency against the input voltage.

In Figures 3.47 and 3.48: A transient analysis is done at two different frequencies, relevant plotting is also done in the frequency domain, respectively.

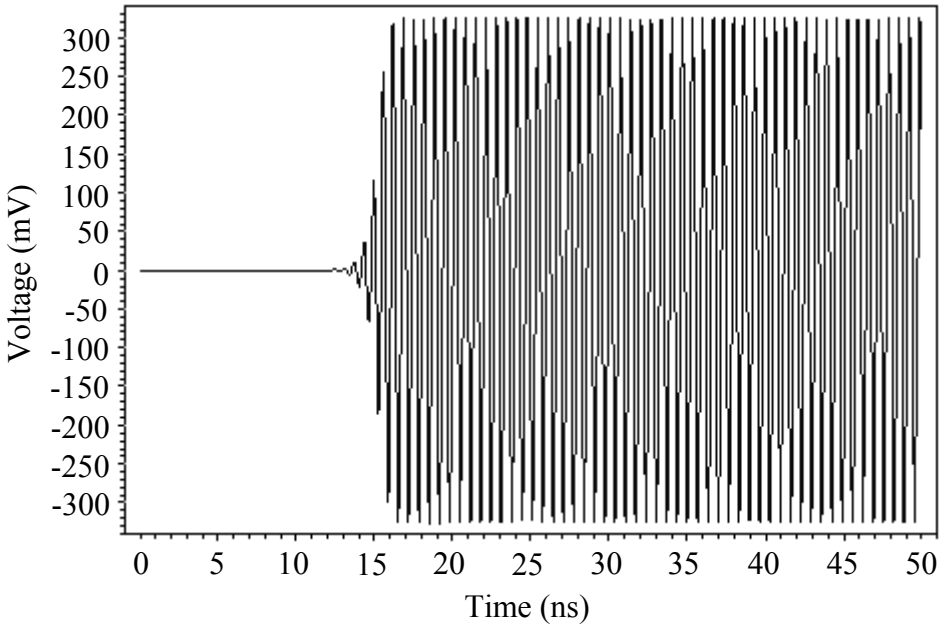


Figure 3.47.

Transient analysis to show the output signal for the 1.5 GHz active inductor oscillator.

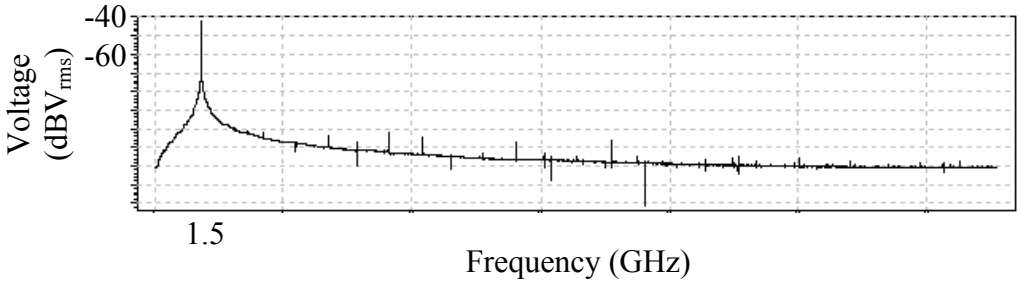


Figure 3.48.

Frequency domain analysis to show the output of the 1.5 GHz active inductor VCO.

Figure 3.47 shows the oscillator output qualifies as a sinusoidal signal. Higher frequency components cause the system output to have a slight distortion, but the first signal component is distinguished to serve as the main signal component influencing mixing (Figure 2.17).

3.8 Integrate and dump

The integrate and dump operation serves to transform the sequence representation of the bits into a ramp like signal that can be processed more easily. The integration process also removes any high frequency terms that remains after mixing and determines the bandwidth of the DDC-CRL.

Two integrate and dump circuits were considered [73], each operating on the principle that at the end of each bit period, the reactive element (a capacitor) is rapidly discharged. The two integrators considered were an active inverting integrator and a non-inverting or Deboo integrator [45]. Both make use of an op-amp as the active element. The most important aspect of the output signal of the integrator is that the signal magnitude is equal for both positive and negative inputs, this is referred to as having a balanced output. The design of the op-amp is documented in Appendix A, and a negative supply voltage is used – as discussed in the next section. The bulk connections are connected to this negative reference.

The inverting integrator has the advantage of having a lower component count and will occupy a smaller area on the silicon substrate. The output of the inverting integrator is inverted and is prone to having a DC offset. The offset is caused by the input offset voltage of the op-amp used. Realizing a balanced output with correct polarity and a stable DC offset requires excessive conditioning circuitry when compared to the non-inverting integrator.

The non-inverting integrator, or Deboo integrator, produces a non-inverted output with no DC offset. Only the input offset voltage of the op-amp must be compensated for to ensure that the output is balanced.

Figure 3.52 shows the schematic of a Deboo integrator, and Figure 3.53 shows the schematic of an inverting integrator. The transfer function of the Deboo integrator is

$$H(s) = \frac{1}{sRC} \tag{3.103}$$

and that of the inverting integrator is

$$H(s) = -\frac{1}{sRC} \tag{3.104}$$

The magnitude of RC, determines the aggressiveness of the integrator [31]. RC is chosen such that the output of the integrator is approximately a linear ramp.

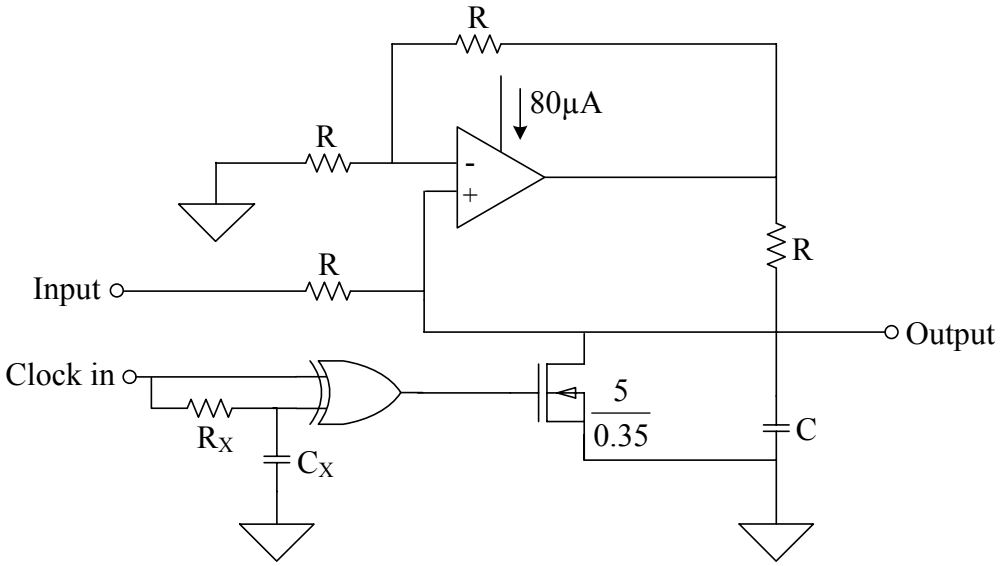


Figure 3.52.

Non-inverting or Deboo integrate and dump (C = 3.5 pF, C_X = 1 pF, R = R_x = 10 kΩ).

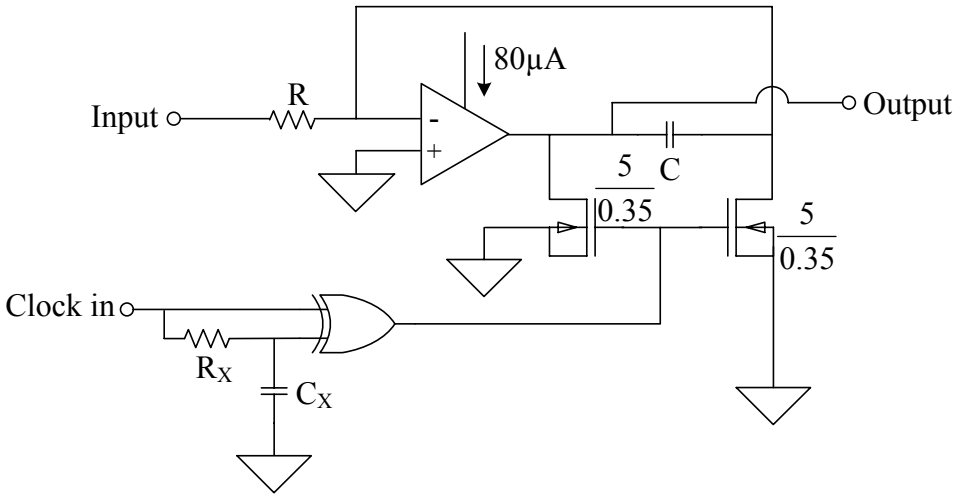


Figure 3.53.

Inverting integrate and dump (C_x = 1 pF, R_x = R = 10 kΩ, C = 3.5 pF).

Both integrators use a pulse to reset the capacitors. The pulse is generated by means of a clock signal and an exclusive OR (XOR) gate. The clock signal is XORed with a delayed version of the clock. The XOR gate outputs 3.3 V when there is a difference between its two inputs. This amounts to a pulse with duration given by

$$\tau_{delay} = R_x C_x \tag{3.105}$$

Integrator design

The pulse turns on the transistors connecting the capacitor terminals to ground, pulling the output of the integrator to ground and creating a low resistance path to ground through which the capacitor discharges.

The maximum specified bit rate for the DDC-CRL is 1 Mbps, or 1 bit every 1 µs. The discharging of the capacitor in the integrator should ideally instantaneous, but the transistors only offer a low resistive path and not a true short. To ensure that the capacitor fully discharges, the pulse must have a duration equal to the time it takes the capacitor to discharge from its maximum possible value after one integration period.

To ensure that the capacitor performing integration is always discharged at the end of each reset period without introducing excessive 'dead time' at the output, pulse length was chosen to be 10 ns, or 100th a bit period. From equation (3.105), R_x = 10 kΩ and C_x = 1 pF.

The data in the received signal occupies a maximum double sided bandwidth of 20 MHz, the demodulated signal occupies half this bandwidth, or 10 MHz. The highest frequency difference term present in the demodulated signal is assumed to not exceed 10 MHz. To acquire a linear ramp output from the integrator, integration should be linear over the signal bandwidth. This can be achieved by setting the integrators bandwidth to be 50% larger than the demodulated signal. C can the be determined from (R is fixed to 10 kΩ)

$$C = \frac{1}{1.5 f_b R} \tag{3.106}$$

which yields C = 3.5 pF.

In testing, the non-inverting or Deboo integrator was chosen above the inverting integrator. Lower total component count and a non-inverted output with 0 V DC offset made the Deboo integrator the preferred choice.

The layout of the integrate and dump circuit is shown in Figure 3.54.

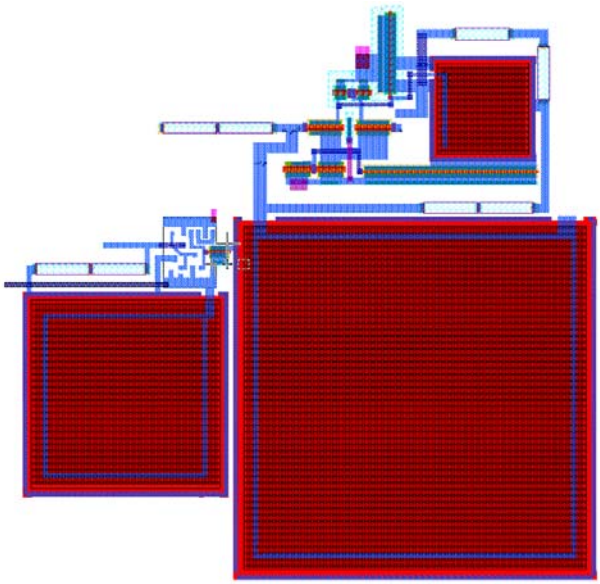


Figure 3.54.

Layout for the integrate and dump sub-system.

Simulation results

Figure 3.55 shows the simulated output of the integrate and dump circuit: the parameters under study are the linearity of the ramp produced by the integration operation as well as the reset time after each integration period.

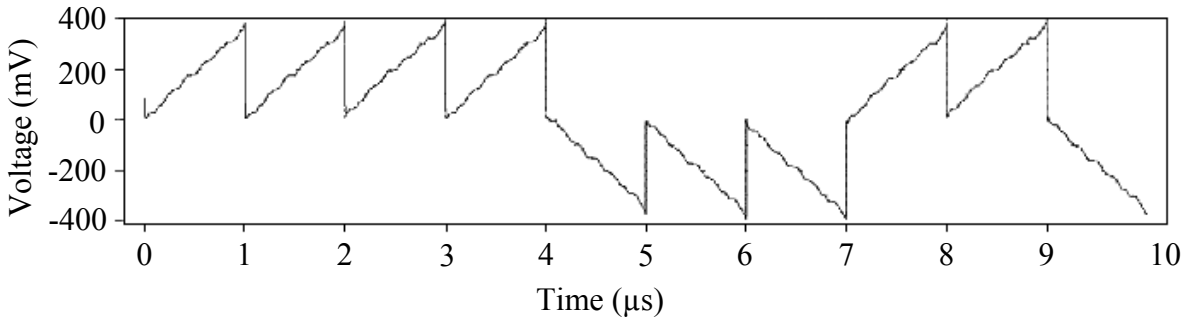


Figure 3.55.

Simulation results to validate the operation of the integrate and dump sub-system.

The reset time is within 10 ns. Certain imperfections in the ramp signal are noted, however does not affect parameters of interest to the DDC-CRL.

3.9 Comparator

Two comparator topologies were initially considered, a simple two stage comparator and a more complex comparator with hysterisis. Earlier attempts to design a comparator with hysterisis proved difficult and yielded unsatisfactory results.

Hysterisis was considered as a technique to reduce the effects of noise on the comparator output. Simulations of the integrate and dump output suggested that hysterisis would be detrimental to the system. In the case of frequency mismatch between the received signal and the local carrier reference, difference terms are produced during demodulation, hysterisis suppresses high frequency difference terms. Suppression of high frequency difference terms decreases the change in the error produced by the phase detector for a given frequency error. This decrease is not desirable.

The comparator topology implemented is shown in Figure 3.56. The design is based on a two stage comparator design [46]. The comparator topology shown in Figure 3.56 is similar to that of an operational amplifier, with some minor changes.

The comparator consists of two-stages: a differential input stage and a current sink inverter drive stage. The differential input stage is used to precisely control the point at which the comparator trips positive or negative. The inverter serves to swing the comparator positive or negative in the presence of a large capacitive load. The output stage converts the output to a form compatible with CMOS digital logic levels.

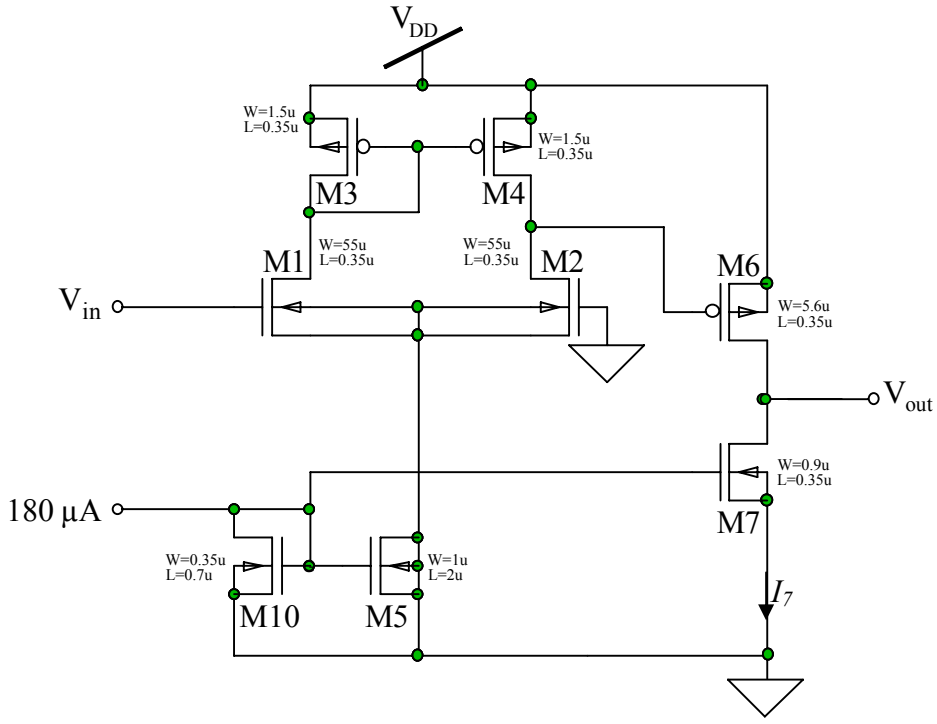


Figure 3.56.

Circuit of a two-stage comparator.

C_L is the load capacitance seen with respect to the output terminal.

Figure 3.56 has a clear resemblance to the amplifier in Figure 3.11. The most obvious differences are that there is no compensating capacitor and that the body of the two input transistors is connected to the source and not V_{SS}. By connecting the body of the transistors to the source terminal, the body effect can be exploited to make the transistor more sensitive to changes on its gate. The body effect is where the body of the transistor behaves like a second gate.

The comparator design procedure is similar to that of the telescopic amplifier. The primary specifications of the comparator are its slew rate (SR) and trip point, the input voltage at which the comparator switches its output. Comparator design starts by defining the slew rate for a specific load. This specification is used to determine the value of I_7 given by

$$I_7 = C_L\left(SR\right) \tag{3.107}$$

$(W/L)_6$ and $(W/L)_7$ are determined from the maximum desired output swing. $(W/L)_6$ and $(W/L)_7$ are determined by

$$V_{DS(sat)} = \sqrt{\frac{2I}{k`\left(\frac{W}{L}\right)}} \tag{3.108}$$

The second stage gain is calculated using

$$A_{v2} = \frac{-g_{m6}}{g_{o6} + g_{o7}} = \frac{-g_{m6}}{I_6\left(\lambda_6 + \lambda_7\right)} \tag{3.109}$$

For the comparator to have balanced operation around the reference specified at the gate of M2, the following relationship must be satisfied.

$$\frac{\left(W/L\right)_6}{\left(W/L\right)_4} = 2\frac{\left(W/L\right)_7}{\left(W/L\right)_5} \tag{3.110}$$

$(W/L)_1$ and $(W/L)_2$ are designed for a user specified gain. The open loop gain of the comparator is typically several thousand V/V, and the first stage gain must be designed to compensate for the low voltage gain in the second stage. The first stage gain is specified by

$$A_{v1} = \frac{-g_{m1}}{g_{o2} + g_{o4}} = \frac{-2g_{m1}}{I_5\left(\lambda_2 + \lambda_4\right)} \tag{3.111}$$

It is assumed that the M1, M2 transistor pair are matched as well as the M3, M4 pair. $(W/L)_5$ can be determined from the relation

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_7\left(\frac{I_5}{I_7}\right) \tag{3.112}$$

Once all ratios are calculated, $(W/L)_3$ and $(W/L)_6$ are adjusted for proper balanced operation.

Comparator design and analysis

The comparator was designed for a slew rate of 1000 V/µs for a 10 pF load capacitance and an open loop gain of 2000 V/V. Linearity and stability do not form part of the specification because they have little affect of the comparators performance.

From equations (3.108) and (3.109), $(W/L)_6$ and $(W/L)_7$ can be determined for an output swing of 2 V. Initial ratios for $(W/L)_6$ and $(W/L)_7$ are 1 and 0.5 respectively. Using these ratios a second stage gain of –10 V/V is calculated.

To meet the specification of 2000 V/V, the first stage gain is set to -200 V/V. This yields a (W/L) ratio for transistors M1 and M2 of 143 using (3.111).

The remainder transistor ratios are determined using Equations (3.110) and (3.112).

The layout of the comparator is shown in Figure 3.57.

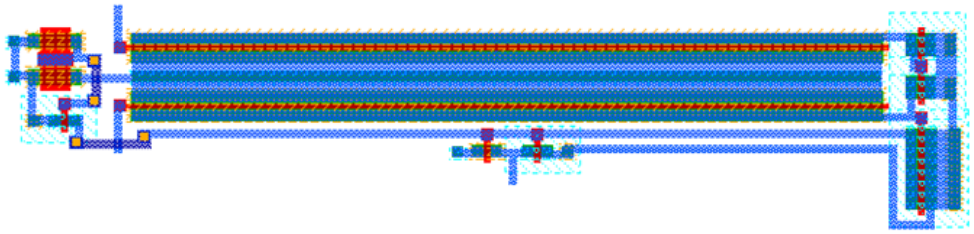


Figure 3.57.
Layout of the comparator.

Simulation results

Figure 3.58 shows a simulation of the comparator.

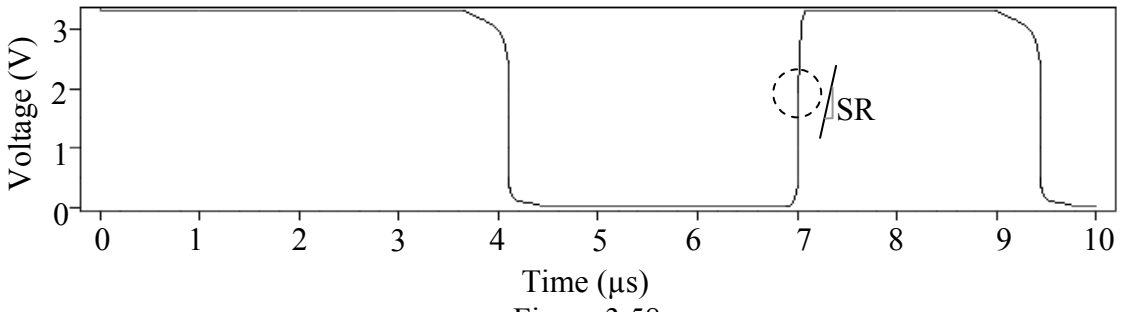


Figure 3.58.
Output waveforms of the CMOS comparator. The positive slew rate (SR) can be determined by analyzing the slope

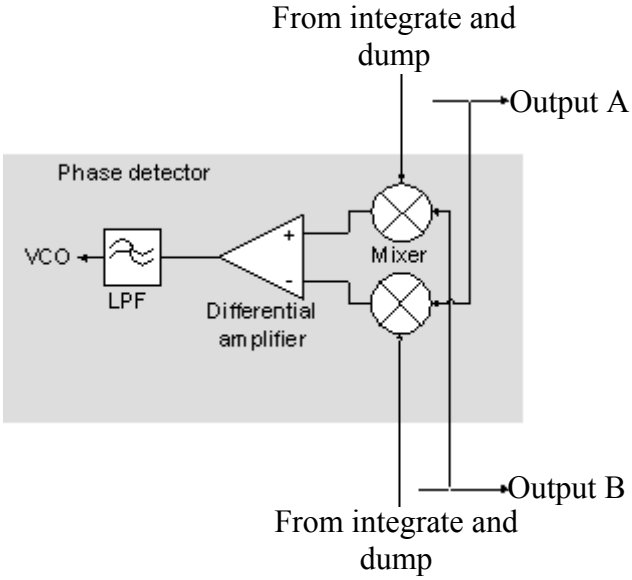
The CMOS comparator initially shows a delayed response to a bit change, but the delay decreases substantially as the system powers up. The initial delay is attributed to the combined effects of system startup and the non-ideal nature of the ramp waveform from the integrate and dump circuit. Delay is not apparent after 5 µs, suggesting that the system has stabilized after power up and comparator operation is acceptable.

3.10 Phase detector

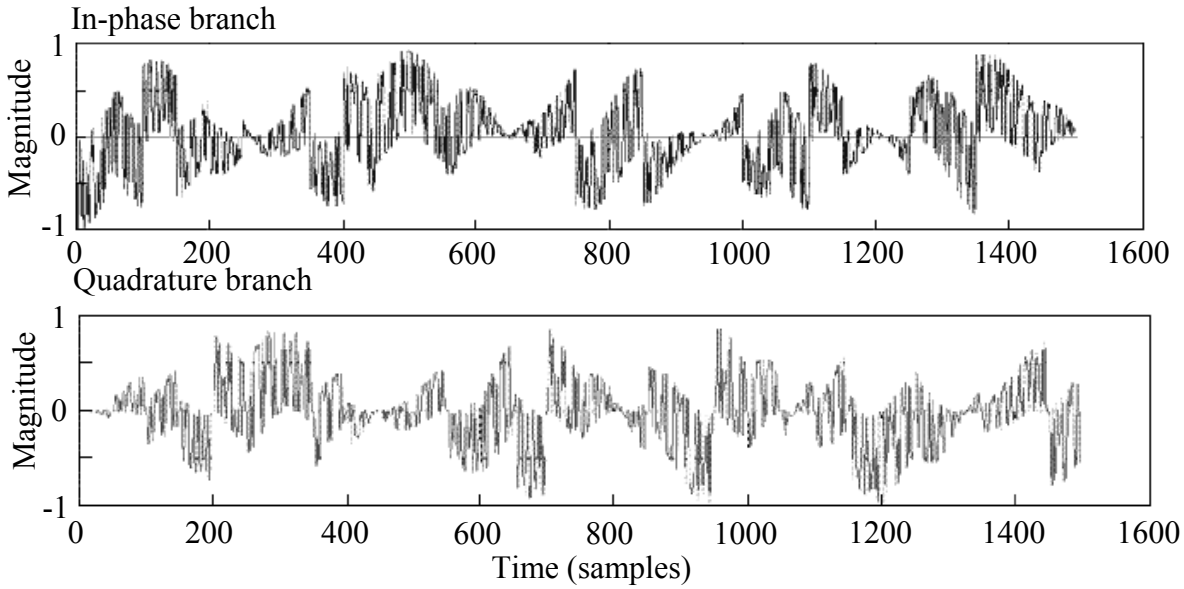
The phase detector compares the in-phase and quadrature branches and determines the magnitude and sign of the frequency difference between the received signal and the reference carrier in the receiver. The premise behind the operation of the phase detector is that increased mismatch between the in-phase and quadrature branches increases the magnitude of the error signal generated by the phase detector.

After demodulation, the difference term present on the in-phase and quadrature branch is of the same frequency but with a 90° phase difference. The effect of this term on the demodulated signal is shown in Figure 3.59 (b).

As the difference term increases or decreases, its net effect on the recovered data stream also increases or decreases. As the difference term approaches 0 Hz, the phase detectors output will stabilize around some DC value. If the phase difference between the two branches is not equal to 90°, the phase detector output will vary slowly around the DC output for a specific error. This slow variation is used to adjust the phase of the local carrier reference to match that of the received signal.



(a)



(b)

Figure 3.59 [73].

(a) A block diagram showing the position of the phase detector in the DDC-CRL.

(b) 90° phase difference between the in-phase and quadrature branches of the DDC-CRL. The variations in the magnitude are due to the sum and difference terms composed, and also due to the imperfections in the integrator.

Two phase detectors were initially considered (Chapter 2). Both were rejected in favour of a hybrid design. All phase detector designs consist of 3 stages (Figure 3.59 (a)): a multiplying stage that multiplies the integrated signal from one branch (Figure 2.20) with the comparator output of the opposite branch (Figure 2.20), a subtraction stage that calculates the difference between the outputs of the multiplying stage, and a low pass filter, which extracts the DC component from the calculated difference.

The alternatives considered only differ in the way that multiplication is performed. The first alternative used the most direct approach to multiplication, using analogue mixers to perform the multiplication. The excess amount of bias circuitry required to condition the inputs led to the rejection of the design.

A digital approach to phase detection using XOR gates to perform multiplication [45]. This method of multiplication was rejected because the input from the integrator is analogue in nature.

The design used to implement the phase detector is a hybrid of the two design

alternatives. Analogue multipliers are used to perform the multiplication, but the digital nature of the comparator output allows for the multipliers to be significantly simpler than analogue mixers.

Multiplier

Multiplication requires an analogue signal to be multiplied by a digital signal, a task that is easily performed if the digital signal is used to control a switch through which the analogue signal must pass. This is the concept used to design a hybrid phase detector that mimics the output of a phase detector based on analogue mixers. Figure 3.60 illustrates this concept.

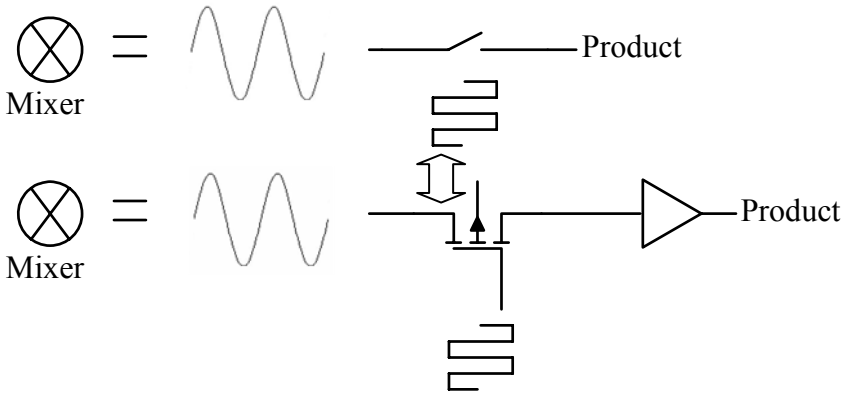


Figure 3.60.

Hybrid phase detector multiplier (as utilized in Fig. 3.59 (a)) concept.

The conceptual circuit in Figure 3.60 can be extended to provide an inverted output when a 'low' bit is present on the switch, effectively providing multiplication by –1. The multiplier shown in Figure 3.61 demonstrates this, and is the topology used in the DDC-CRL's phase detector. The amplifier used as the multiplier has each of the input terminals connected to a pair of NMOS switches. The switch pair controlling multiplication by +1 is controlled by the digital input, while the pair controlling multiplication by –1 is controlled by the inverse of the digital input.

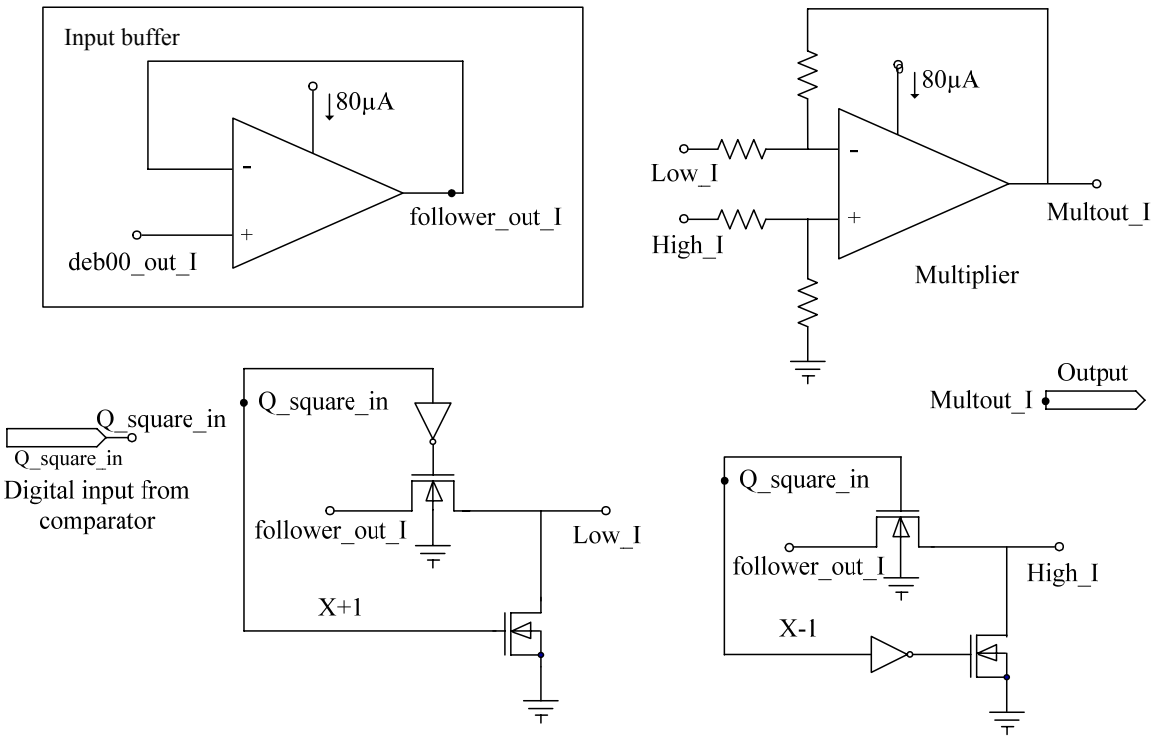


Figure 3.61.

Topology for multiplying a bi-polar digital signal with an analogue signal.

A digital high (at node `Q_square_in`) routes the analogue signal to the non-inverting terminal of the op-amp and grounds the inverting terminal, resulting in the analogue input simply passing through unchanged. Similarly, a digital low configures the multiplier to invert the input signal. This results in the output resembling the multiplication of an analogue signal with a bipolar digital signal.

The values of the resistors in the resistive network of the op-amp are 10 kΩ, providing a balance output for either configuration. The (W/L) ratios of the NMOS switches are 10. A large width increases switching speed, whereas a small length minimizes the on resistance, r_{ds}, of the transistor.

Difference amplifier

The phase detector's error signal is obtained by taking the difference of the multiplier outputs. The difference is determined by an op-amp in a difference amplifier configuration. A standard differential amplifier is not suitable because the output of a differential amplifier has an undesired DC offset. The output of a difference amplifier is given by [45]

$$v_O = \frac{R_2}{R_1}(v_2 - v_1) \tag{3.113}$$

where v_2 and v_1 are the inputs of the difference amplifier. The main advantages of the difference amplifier over a differential amplifier are the ability to weight the inputs and the use of feedback ensures a precise and stable output.

Figure 3.62 shows the difference amplifier used in the DDC-CRL. R_1 and R_2 are set to 10 kΩ.

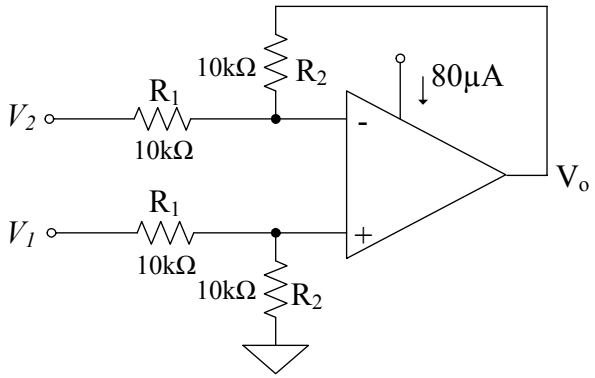


Figure 3.62.

Difference amplifier of the DDC-CRL's phase detector.

Low-pass filter

The LPF used in the DDC-CRL is a first order passive low pass filter as shown in Figure 3.63.

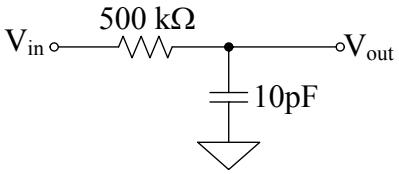


Figure 3.63.

First order passive low pass filter.

The cut off frequency of the LPF is given by

$$f_c = \frac{1}{2\pi RC} \tag{3.114}$$

where R and C are the values of the resistor and capacitor in Figure 3.63. The chosen cut off frequency is 30 kHz, which yields: R = 500 kΩ and C = 10 pF.

The large values of R and C can be implemented in CMOS, but are instead implemented externally. The value of f_c can be used as a tuning parameter to adjust the step response time of the DDC-CRL. Larger values command a faster response but with higher susceptibility to low frequency noise within the DDC-CRL. A first order passive filter is

considered suitable for rejecting the AC component of the phase detector output because higher order filters only offer greater attenuation at higher frequencies, when the primary concern is low frequency components within the pass band of the filter. The first order step response is also preferred, as an aggressive second or third order step response is characterized by a degree of overshoot, despite lower settling time. Overshoot will drive the VCO to a higher frequency than desired, introducing further error in to the system and causing the VCO output to first 'bounce' around the desired operating frequency before stabilizing. The CMOS layout of the phase detector is shown in Figure 3.64.

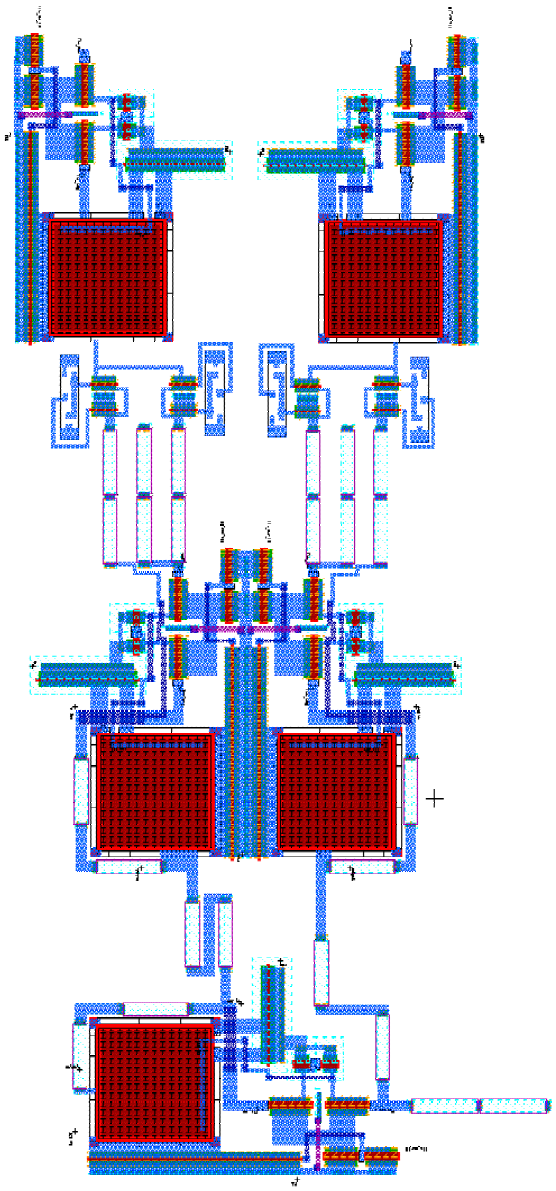


Figure 3.64.

CMOS layout of phase detector. The following sub-systems are included: multipliers, buffers, digital switching and difference amplifier.

Simulation results

The primary parameter of concern is the linearity of the error signal, i.e. the amount of distortion prior to the introduction of a frequency error into the system. This is considered critical to the operation of the system, as it directly affects the performance of the VCO generating the reference carrier.

Figure 3.65 shows the output of both phase detector multipliers (on the top axis), with the filtered and unfiltered error signals shown on the bottom axis.

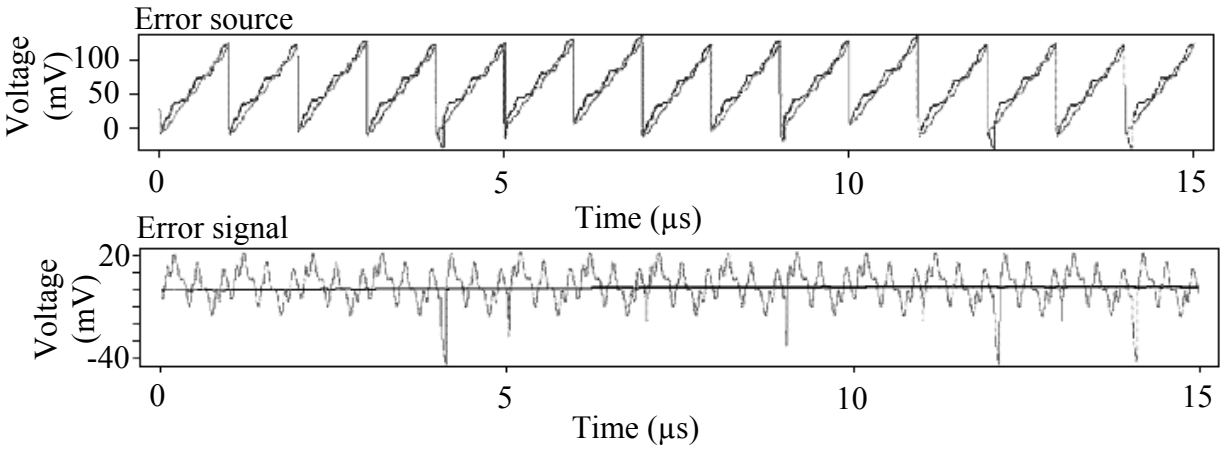


Figure 3.65.

Waveforms within the phase detector for 0 phase and frequency error when a length 13 sequence is used.

Figure 3.66 shows the phase detector output for a sequence with a length that tends to infinity for the ideal low pass filter (time constant tending to 0 s) in the phase detector. The output from both multipliers is shown on the lower set of axis, with the error signal shown on the upper axis.

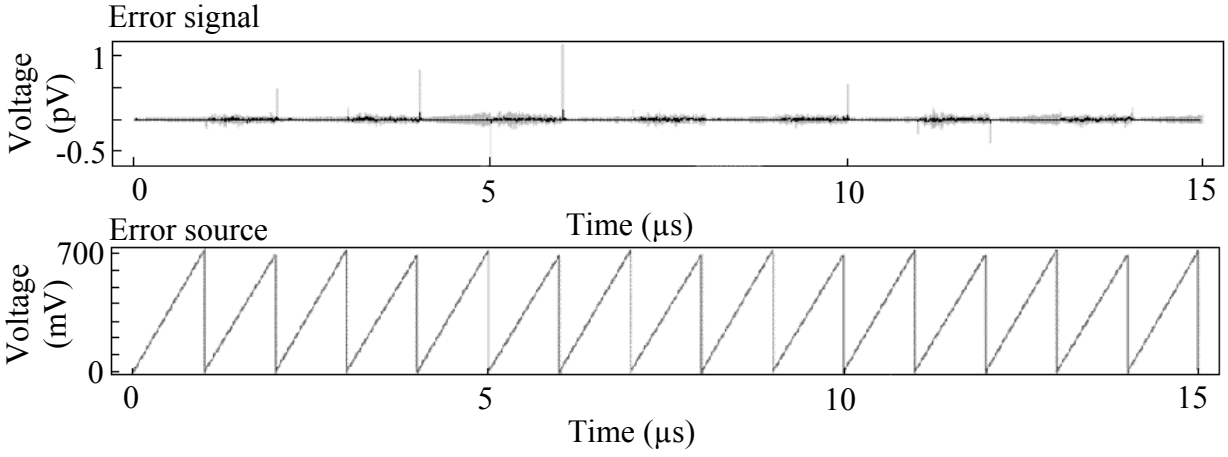


Figure 3.66.

Shown are phase detector wave forms if the sequence length tends to infinity.

The output of the phase detector multipliers is an approximate saw tooth wave for both the in-phase and quadrature branches. The error signal derived from the two saw tooth waveforms reflects the differences in the two ramps. The magnitude of the filtered error signal is approximately –2 mV. The output of the phase detector for a sequence of infinite length and ideal LPF is approximately 0 V.

The varying gradient present on the ramps generated by the integrate and dump circuit has a significant effect on the phase detectors output signal. The deviations from the desired gradient manifest as low frequency distortion on the error signal. The net effect of the distortion on the system results in phase jitter, as the VCO can not distinguish between the DC error signal and the distortion, causing the VCO output to deviate slowly about the desired frequency.

Figure 3.66 shows that if the sequence is made very long and the low pass filter ideal, the ramps generated by the integrate and dump circuit approach those generated for an infinitely long sequence. The error signal derived from these ramps is more refined, with significantly less distortion.

Figure 3.67 shows the results of a frequency error.

3.11 Summing circuit

The summing circuit is used at 2.4 GHz frequency. It adds the modulated spread signals before transmission. It can be implemented by forcing the drain currents from the amplifier in the common-source configuration into a node and by using a resistor to convert the sum current into voltage.

If a transistor is switched on, the total drain current will be [47]

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2 \ , \tag{3.115}$$

which for small signals simplifies to

$$i_D = I_D + k'_n \frac{W}{L} (V_{GS} - V_t) v_{gs} \tag{3.116}$$

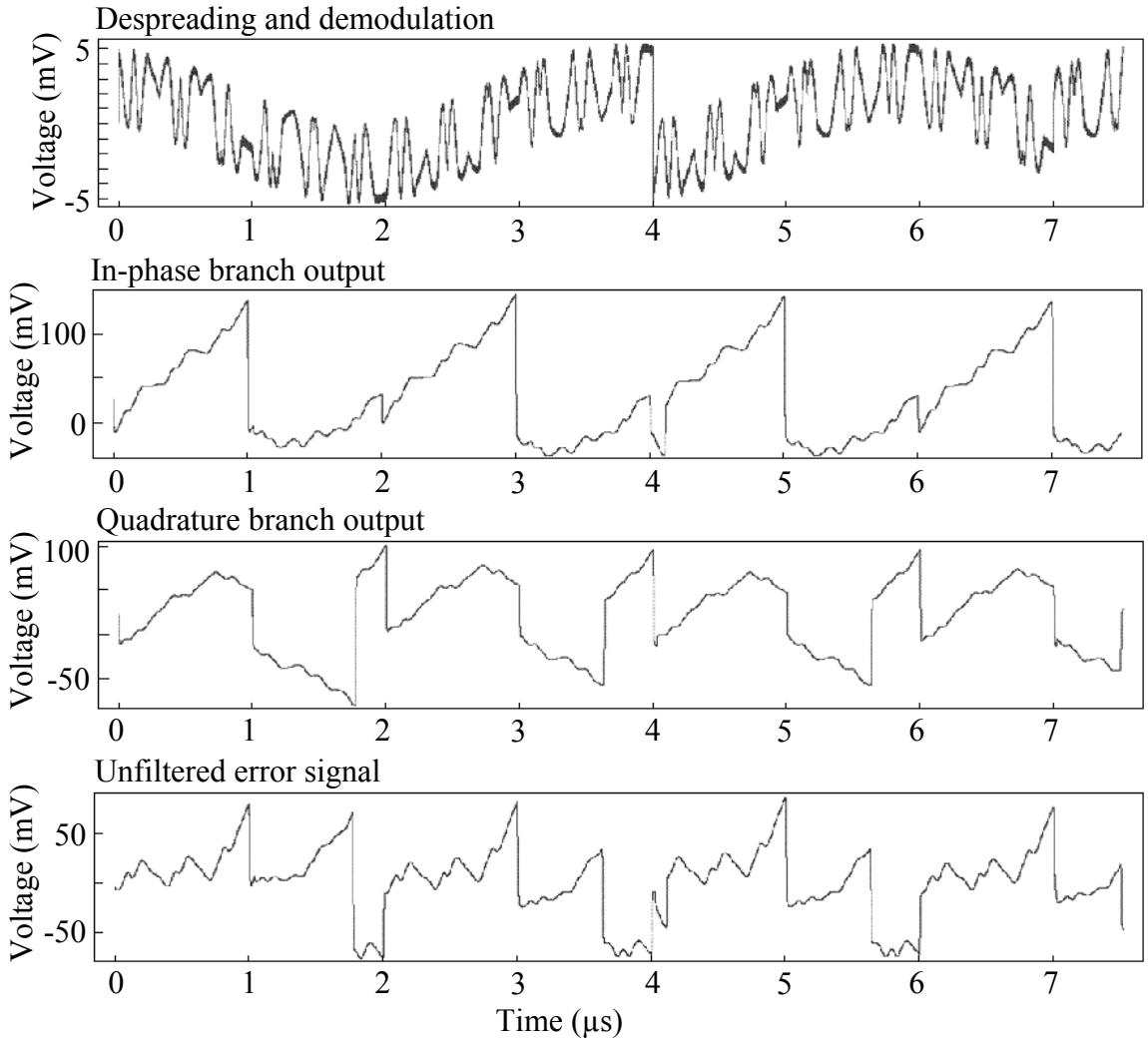


Figure 3.67.

Effect of a 250 kHz positive frequency difference on various waveforms of the DDC-CRL.

AC current, for $v_{gs} << 2(V_{GS} - V_t)$, is given by

$$i_d = k'_n \frac{W}{L}(V_{GS} - V_t)v_{gs} \tag{3.117}$$

For a specific biasing the V_{GS} is also constant, and i_d is essentially

$$i_d = g_m v_{gs}, \tag{3.118}$$

where $g_m = k'_n \frac{W}{L}(V_{GS} - V_t)$.

Forcing four currents into a node will result in the addition of AC v_{gs} (if identical biasing and transistors are assumed), i.e.

$$i_{d1} + i_{d2} + i_{d3} + i_{d4} = g_m(v_{gs1} + v_{gs2} + v_{gs3} + v_{gs4}) \tag{3.119}$$

The circuit used in the system is shown in Figure 3.68.

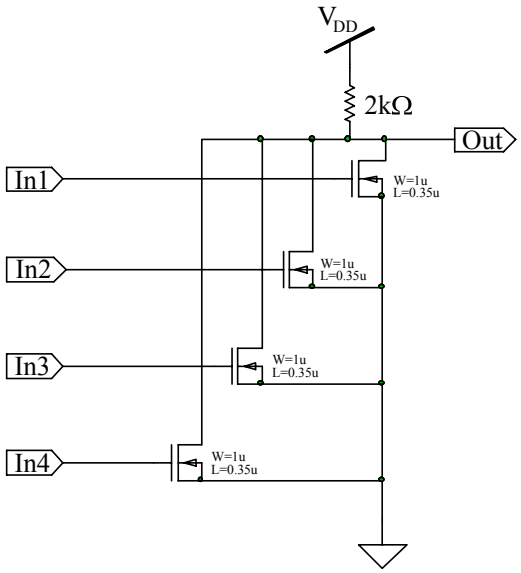


Figure 3.68.

Summing circuit.

The chosen component values (W/L=3 and R = 2 kΩ) result in the calculated AC voltage gain of about 1. The CMOS layout of the summing amplifier is shown in Figure 3.69.

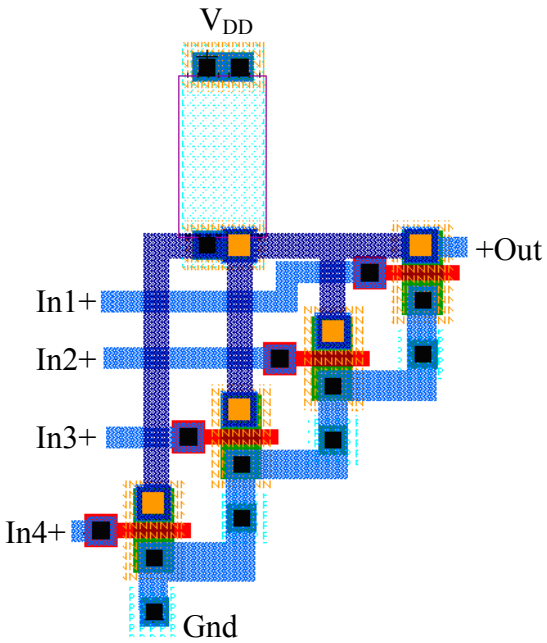


Figure 3.69.

Layout of the summing amplifier.

3.12 High-frequency buffer

Equations and parameters described in these sections present very good approximations for the low frequency operation of a transistor-based circuit. With the increased frequency of

operation, unfortunately, some approximations can no longer be used. A high-frequency model is proposed in Figure 3.70.

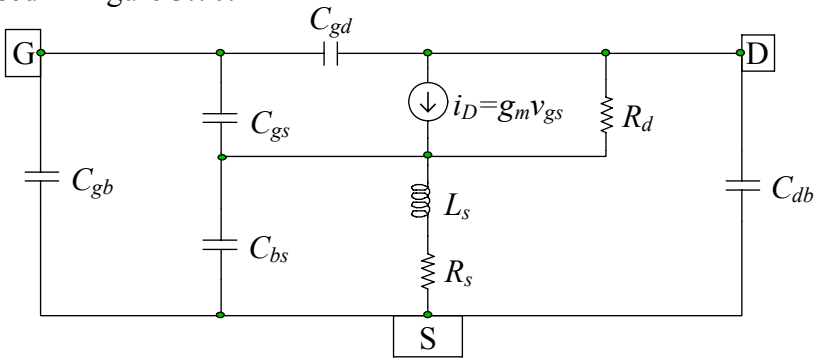


Figure 3.70.

High frequency small signal of an NMOS transistor.

The most commonly used approximation in designing transistor circuits is that the input resistance of a MOS transistor at the gate is infinite. At the low frequency operation this is true, but at high frequencies the effect of the gate-source capacitance (C_{gs}) and other parasitic capacitances becomes profound. The two-port admittance (y) parameters are applicable when analysing for the input resistance as this appears in shunt [47]. This was somewhat simplified, as shown in Figure 3.70 [48]. A few different equations for the input resistance are given in this source. One very complex equation is presented here, based only on the following approximations (X is the reactance and Z is the impedance of a passive component, and R_L is the load resistor not shown):

$$R_L \parallel X_{db} \approx R_L \tag{3.120}$$

$$R_d \gg R_s \tag{3.121}$$

$$R_d \gg R_L \tag{3.122}$$

$$X_{bs} \parallel Z_s \approx Z_s \tag{3.123}$$

$$g_m \gg 1 / R_d \tag{3.124}$$

If the quality factor of the inductor is

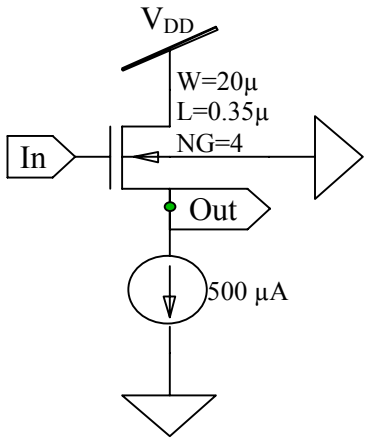
$$Q \approx 3 \tag{3.125}$$

then

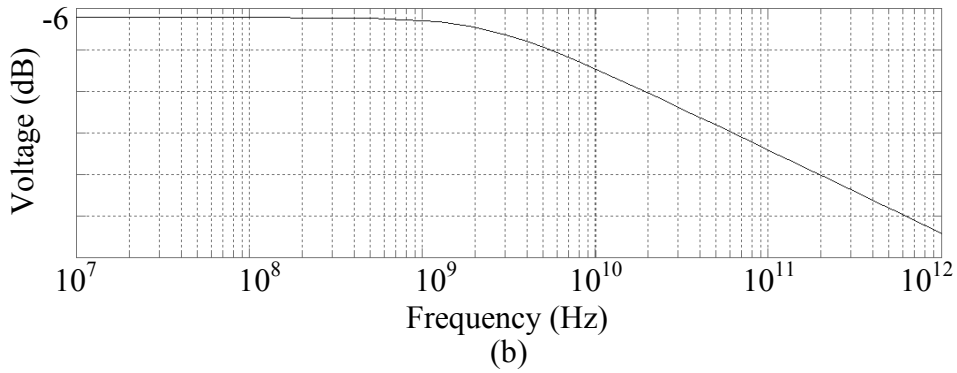
$$\mathrm{Re}(Z_{in}) = \frac{\frac{L_s}{C_{gs}} g_m \left(1+\frac{C_{gd}}{C_{gs}} g_m R_L \left(1-\omega^2 L_s (C_{gd}+C_{gb})\right)\right) + \left(1+\frac{C_{gd}}{C_{gs}} g_m R_L \left(1+\frac{C_{gd}}{C_{gs}}\left(2+g_m (R_L+R_s)\right)\right)\right)}{\left(1+\frac{C_{gd}}{C_{gs}} g_m R_L + \frac{C_{gd}+C_{gb}}{C_{gs}}(1+g_m R_s) - \omega^2 L_s (C_{gd}+C_{gb})^2\right)^2 + \left(\omega C_{gd}\left(\left(r_s+\frac{L_s}{C_{gs}} g_m\right)\left(1+\frac{C_{gb}}{C_{gd}}\right) + R_L (1-\omega^2 L_s C_{gb}) + \frac{L_s}{C_{gd} R_d}\right)\right)^2} \tag{3.126}$$

This is a very close, but tedious approximation of the input resistance of a transistor. In high frequency CMOS applications the infinite gate resistance of a transistor is replaced by the finite gate-to-source capacitance. This implies that when connecting stages the output impedance of the preceding stage must be small in order not to loose gain.

The problem of connecting stages can partially be solved by means of a high frequency buffer. This buffer must have a high bandwidth, the high level stability and lower output impedance than the preceding stage that the buffer is connected to. The source follower to be used for this application must be driven by a large current source (1 mA range). The transistor's *W*/*L* ratio must also be high, of any value from 50 to 600. The circuit diagram is shown in Figure 3.71.



(a)



(b)

Figure 3.71.

(a) High frequency buffer.

(b) Frequency sweep on the High frequency buffer.

3.13 Filter design

Whenever an LPF is required, simple RC LPF configuration of Figure 3.72 is used. This configuration has the transfer function

$$f = \frac{1}{2\pi RC} \tag{3.127}$$

This formula can be used to determine component values R and C for any cut-off frequency f specified.

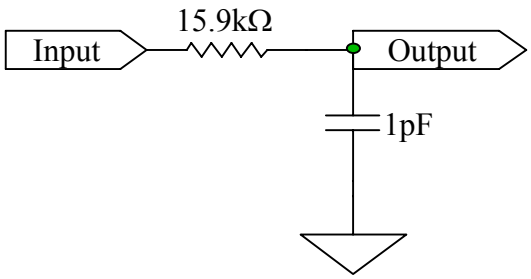


Figure 3.72.
Circuit diagram of the LPF.

3.14 Sequence processing circuit

Sequence processing circuit is an analogue circuit which is used to prepare spreading sequences for usage in the system. The same circuit is used both in the transmitter and receiver part of the system, and is connected to it via an analogue switch. Ideally, the real or imaginary part of the spreading sequence has values between -1 and 1, therefore for further processing, it has to be offset to a DC value. A simple transistor-based one-to-two voltage divider is used here. The real or imaginary part of the sequence is then used with or without inverting. For inversion, a common source inverter with enhancement load is used.

The inverter has the gain given as [47]

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \tag{3.128}$$

(disregarding the Early effect). Lengths of approximately 1 µm and widths of 1.5 µm were used to establish the gain of approximately one. The complete design is shown in Figure 3.73.

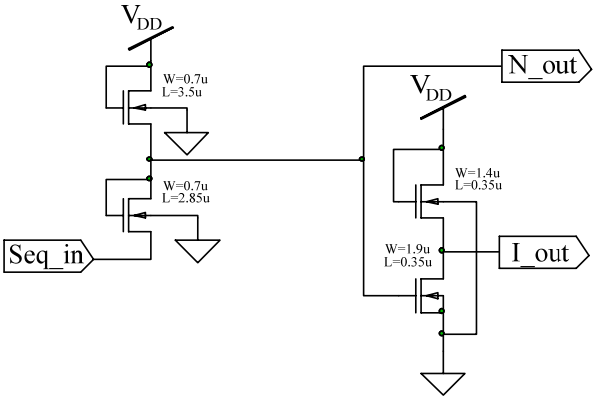


Figure 3.73.

Sequence processing circuit.

3.15 Power amplifier

In the system for this thesis, and for most communication applications, in general, only fundamental output power is considered to be allowed to reach the output load, filtering out harmonic components, thus leading to the following definition for drain efficiency η,

$$\eta = \frac{P_{out,f}}{P_{dc}} = \frac{P_{out,f}}{P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf}} \tag{3.129}$$

In this expression, P_{diss} and $P_{out,nf}$ take into account the output network characteristics. If the latter is an ideal lowpass filter, then $P_{out,nf} = 0$ for $n > 1$, while P_{diss} already accounts for the power reflected by the filter towards the device. From (3.129), maximum drain efficiency is obtained if

$$P_{diss} + \sum_{n=2}^{\infty} P_{out,nf} = 0, \tag{3.130}$$

that is, if $P_{diss} = 0$ and $\sum_{n=2}^{\infty} P_{out,nf} = 0$. Maximum drain efficiency can therefore be obtained if the fundamental output power $P_{out,f}$ is maximized, or the sum of P_{diss} and $P_{out,nf}$ $(n > 1)$ is minimized.

Class F power amplifiers can provide the highest power added efficiency while still linear enough [48]. The basic principles of operation of the Class F amplifier as illustrated in Figure 3.74 [49] are as follows.

- Fundamental-frequency drain voltage and current are shifted in phase by 180˚ from each other.
- The voltage waveform adds odd harmonics to build its shape towards a square wave.
- The current waveform adds even harmonics to build its shape towards a half sine wave.
- No power is generated at the harmonics because there is either no voltage or no current present at a given harmonic.
- At microwave frequencies, the number of harmonics is usually relatively small.
- The RF-power device acts as a saturating current source. Only when all harmonics are properly terminated can it act as a true switch.

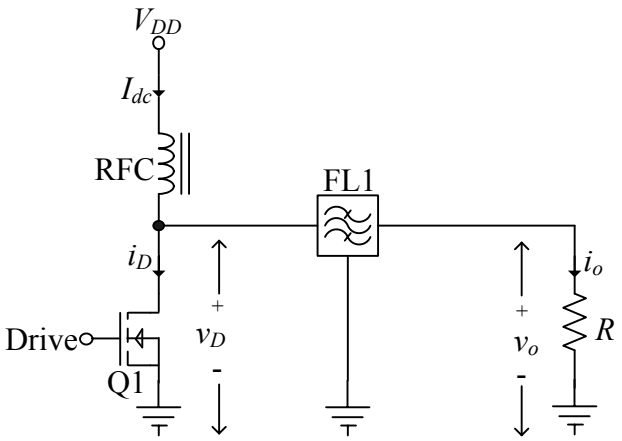


Figure 3.74.

Simplified circuit diagram for a class F amplifier [49].

The gain coefficient can be defined as the ratio between the fundamental-frequency component and the minimum value (excluding DC), assumed by the voltage waveform. It is shown that for a maximum gain coefficient, the ratio between fundamental and third harmonic drain voltage components (ε_3) must be -7.5 < ε_3 <-4.5 [51]. The DC power consumption is unaffected by third harmonic flattening, but output power drain efficiency is increased by the gain coefficient. The choice of ε_3 automatically determines the optimum third harmonic loading. It can also be noted that the power dissipation can be more than halved if a bias point close to pinch-off is selected allowing a major reduction in P_{diss}. Figure 3.75 shows that the maximum efficiency of an ideal power amplifier increases from 50 % of a class A up to 100 % for infinite harmonic traps. The power amplifier design was adapted from [72].

The input and output matching networks can be provided using passive element matching networks such as a L-network, a T-network and a Π-network. The discrete elements for the matching network can also be used as coupling capacitors and inductor chokes. A differential amplifier will act as the pre-amplifier and the biasing network [45]. Since this topic has been discussed earlier in this thesis, it will not be repeated. For the current source, a negative voltage (dc) source was required. The negative voltage source is a ring oscillator with a negative biased diode rectifier, a filter and a voltage regulator.

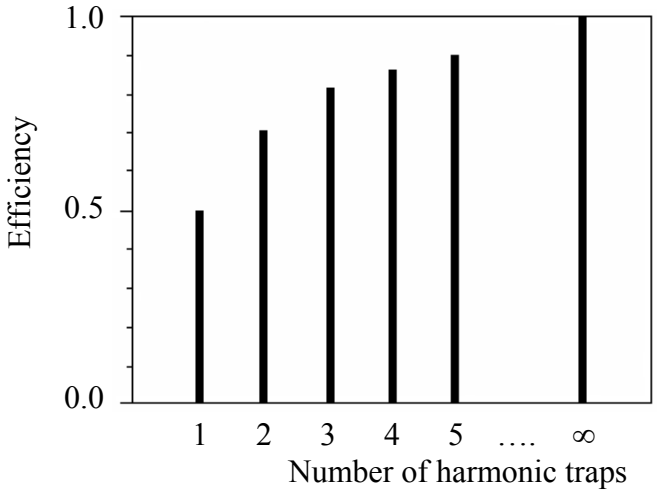


Figure 3.75.

Efficiency improvement in an ideal power amplifier as the number of harmonic traps is increased [49].

Figure 3.76 shows the schematic layout of the class F amplifier, where L_1 and L_2 are the choke inductance and C_1 and C_2 are the dc-blocking capacitors. L_1 and L_2 are seen as DC short circuits and RF open circuits, while C_1 and C_2 has the opposite behaviour. A RF NMOS transistor was used with a length of 0.35 µm and a width of 150 µm.

The filters for the odd harmonics were implemented with bandreject filters connected in series with the output of the amplifier. The impedance of an inductor in parallel with a capacitor can be calculated with

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \textbf{(3.131)}$$

were the total impedance is very high at the frequency, f and otherwise almost zero. The filters for the even harmonics were implemented with bandpass filters connected in parallel to ground. The impedance of an inductor in series with a capacitor can also be calculated with equation (3.131), but then the impedance is almost zero at the frequency, f and very high at the other frequencies.

A class F amplifier with up to the sixth harmonic was implemented for this thesis. The efficiency gained by adding more harmonics was not found worth the output-network complexity needed for higher harmonics. The third and fifth harmonics were filtered out with the circuits in Figure 3.77 (a) connected in series with the output, while the second, fourth and sixth harmonics were filtered out with the circuits in Figure 3.77 (b) connected in shunt.

The inductors of the filters at the first and second harmonics were chosen to by 1 nH to minimize the size on the IC, while the inductors of the filters at the third, forth and fifth harmonics were chosen to be 0.5 nH. The values of the capacitors were calculated from equation (3.131) and are tabulated in table 3.10.

Harmonic, n	*Frequency*	*Capacitor*	*Inductor*
2	4.28 GHZ	1.38 pF	1 nH
3	6.42 GHZ	0.615 pF	1 nH
4	8.56 GHz	0.691 pF	0.5 nH
5	10.70 GHZ	0.442 pF	0.5 nH
6	12.84 GHz	0.307 pF	0.5 nH

Table 3.10.

Values calculated for the capacitors and inductors of the LC filters for the different harmonic frequencies.

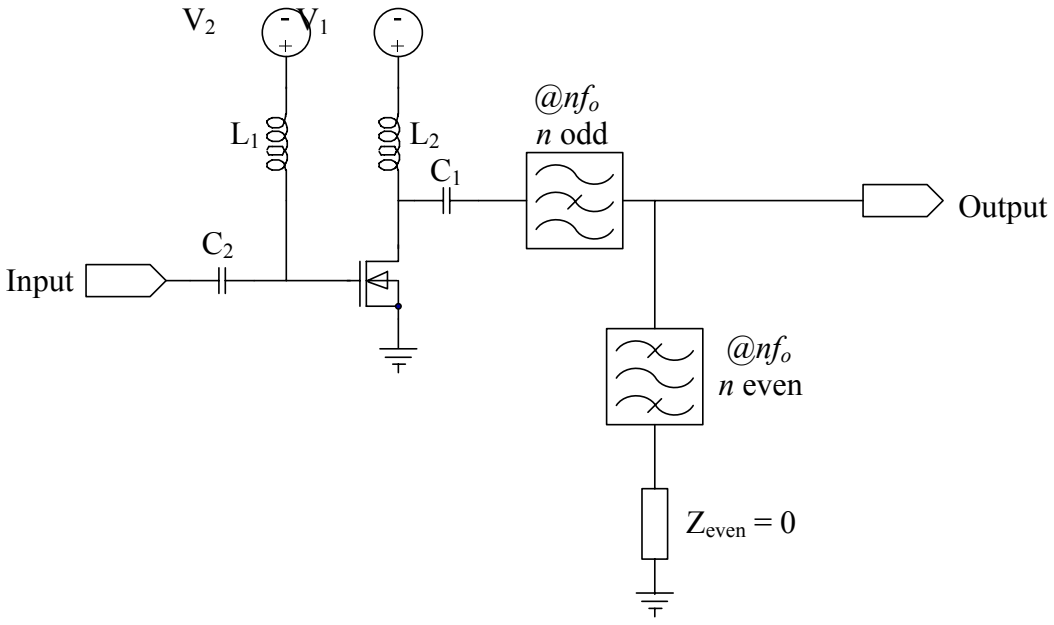
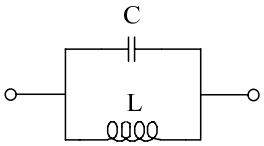
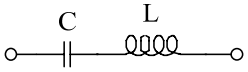


Figure 3.76.

Basic schematic of the class F amplifier.



(a)



(b)

Figure 3.77.

(a) Bandreject filter, and (b) Bandpass filter (bottom) used in the class F amplifier.

The next step towards designing the class F amplifier was to select a suitable bias point for operation. A class F amplifier can be biased as a class A, AB, B and C amplifier. Class A, AB, B and C amplifiers differ merely by their respective conduction angles.

Thus a device can be made to operate under any of these modes by adjusting the gate bias. In order to determine the bias point a DC bias point simulation was performed. Figure 3.78 shows the plot of the DC transfer characteristics for the transistor. For this thesis, the maximum drain-source voltage applicable is 3.3 V.

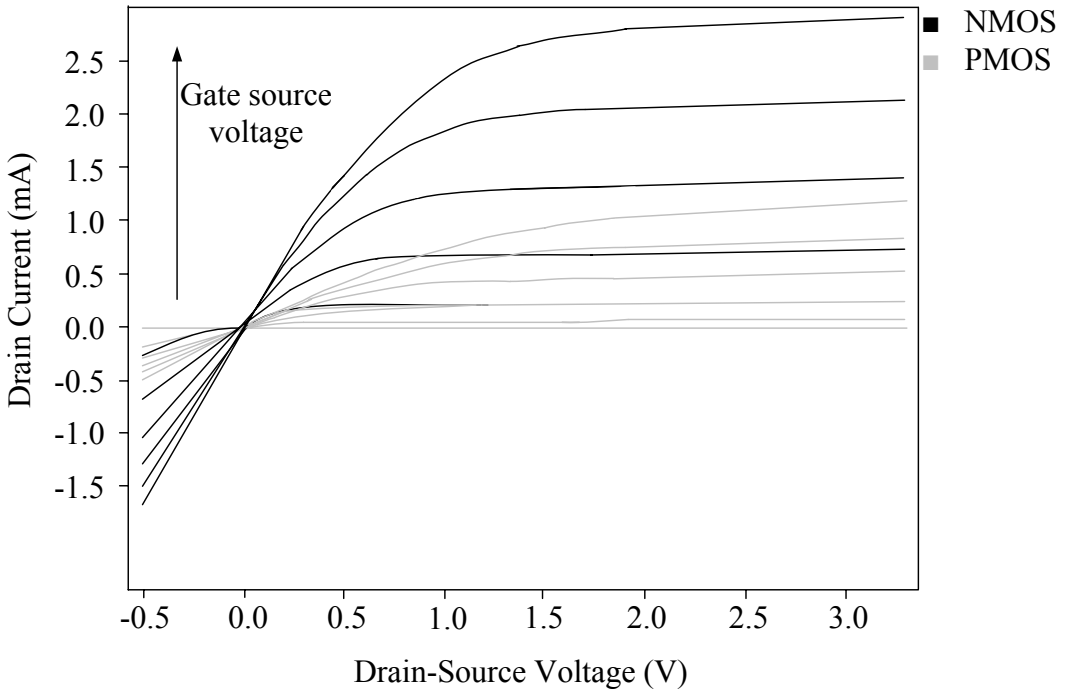


Figure 3.78.

Plot of the DC transfer characteristics for the transistor [28] as the gate source voltage is linearly increased.

Usually the Class F transistor is biased in Class B mode as it gives a better efficiency than biased as Class A or Class B due to the generation of large harmonics. However that would result in a poor linearity [50]. Hence a Class AB bias point was chosen for this thesis.

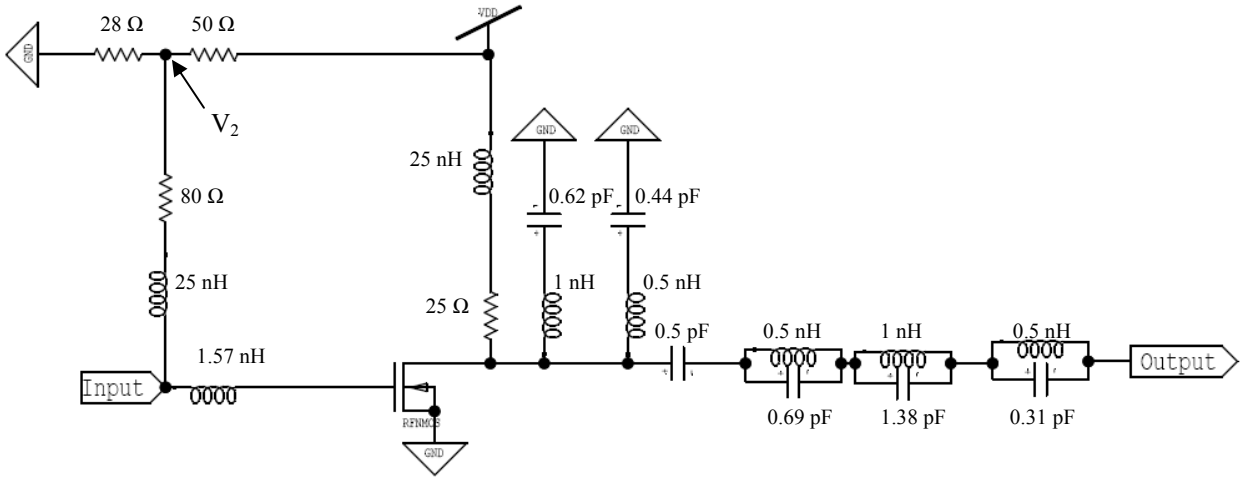


Figure 3.79.

Designed Class F amplifier [V_2 = 1.5 V & V_{DD} = 3.3 V]. Inductor design as in [62].

Difference amplifier

Figure 3.11 (a) shows the schematic of the differential amplifier. This will give the maximum gain, because the difference between v_{IN+} and v_{IN-} will be maximised. A highpass filter produces a frequency dependent leading phase shift of 90˚ at the filters corner frequency. To get a phase shift of 180˚, two highpass filters are placed in series with each other. Figure 3.80 shows the schematic of the highpass filter used for the 90˚ phase shift.

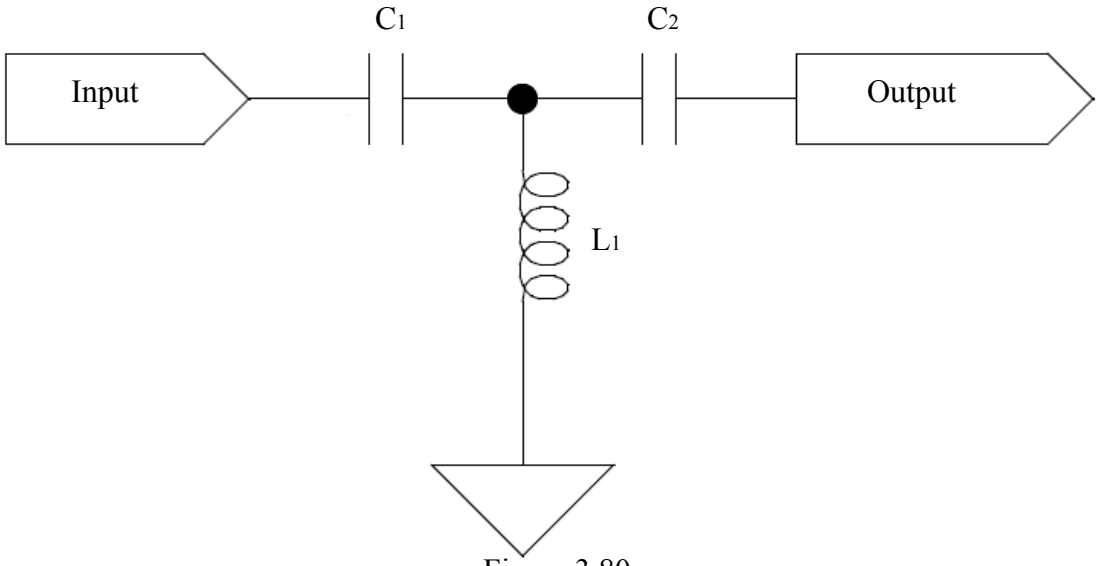


Figure 3.80.

Highpass filter used to create a 90˚ phase shift.

If R_S is the source resistance and R_L the load resistance that connects the two differential outputs to each other, then the characteristic impedance of each filter should be equal to the geometric mean of those source and termination resistances. If $C_1 = C_2$:

$$\sqrt{\frac{L_1}{C_1}} = \sqrt{R_S R_L} \Rightarrow \frac{L_1}{C_1} = R_S R_L \qquad \textbf{(3.132)}$$

The other equation needed to complete the design derives from choosing the corner frequencies of the filters equal to the centre frequency of operation:

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \qquad \textbf{(3.133)}$$

Substituting equation (3.132) into equation (3.133) and solving:

$$C_1 = \frac{1}{\omega_0 \sqrt{R_S R_L}} \qquad \textbf{(3.134)}$$

and

$$L_1 = \frac{\sqrt{R_S R_L}}{\omega_0} \qquad \textbf{(3.135)}$$

R_L is derived from the S-parameters of the 0.35 µm CMOS transistor [28]. The S-parameters are explained in detail in the section detailing the design of the input matching network. From the S-parameters R_L = 38.46 Ω, while R_S equals the 50 Ω resistance. Substituting R_S and R_L into equation (3.134) and (3.135), C_1 = 1.7 pF and L_1 = 3.26 nH. For the 180˚ phase shift, two highpass filters were added in series. A simple current mirror of 4 mA was designed for this differential amplifier [47]. The negative DC voltage is designed as per the next section.

Negative DC voltage

The negative supply was generated with an oscillator, a rectifier, a filter and a voltage regulator.

Design of the ring oscillator

Ring oscillators derive from digital-like building blocks. Compared to tuned oscillators, they have inferior phase noise performance, but their relatively large tuning range and simplicity are strong enough attributes to make them attractive [52]. The ring oscillator

consist of *n* inverters in a ring, where *n* is odd. Figure 3.81 shows the schematic of a CMOS inverter.

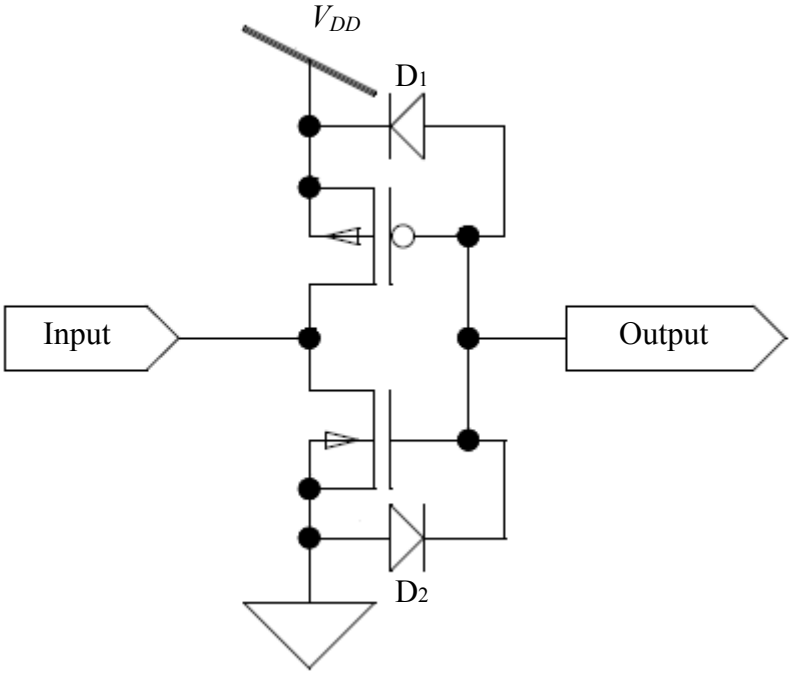


Figure 3.81.

Schematic of a typical inverter.

The inverter can be regarded as an inverting-type threshold detector. D_1 and D_2 are protective diodes. They protect the transistor against possible electrostatic discharge. The inverter inverts an input of 0 V to V_{DD} and an input of V_{DD} down to 0 V. The diodes were replaced with NMOS transistors with length of 0.35 µm and width of 50 µm, where the base of the transistor is connected to its drain and the gate is grounded (Fig. 3.94).

Figure 3.82 shows the schematic of the ring oscillator. I_1, I_2 and I_3 are the inverters shown in Figure 3.81. The ring oscillator consists of an odd number of inverters added in a ring. In its simplest analysis it is assumed that each inverter can be characterized by a propagation delay T_{pd}. No stable DC point exists, and a logic level propagates around the loop, experiencing one net inversion each traversal [52].

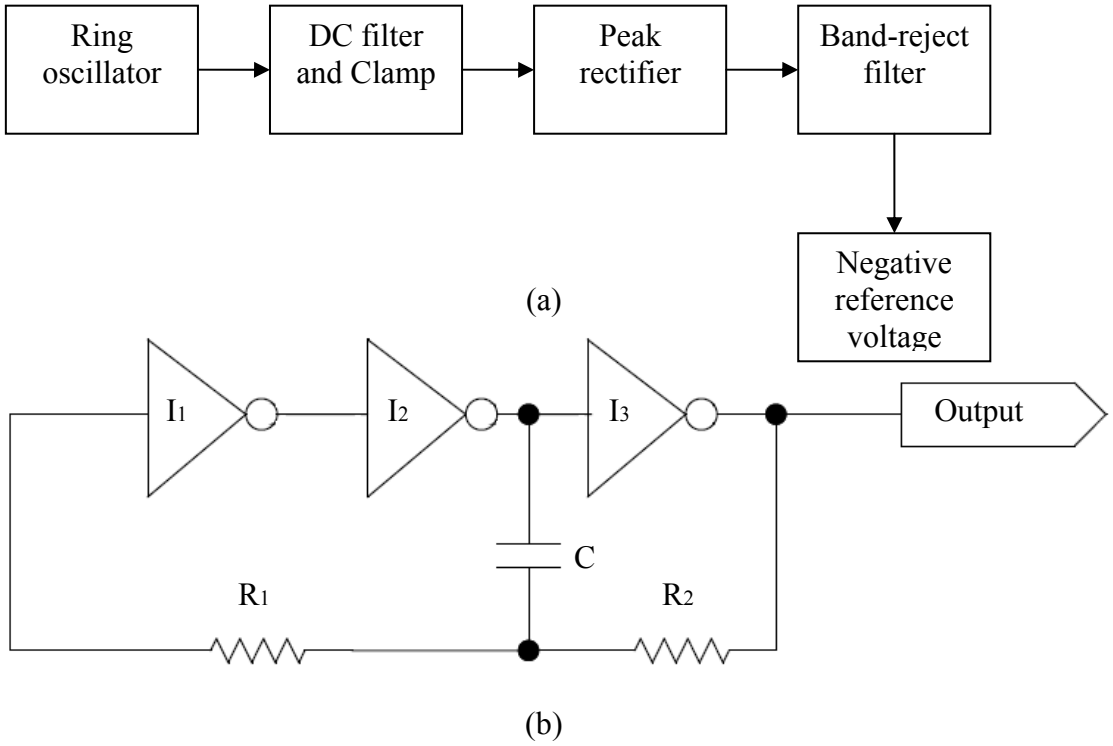


Figure 3.82.

(a) Context of the ring oscillator in generating the negative reference voltage.

(b) Schematic of the ring oscillator.

The oscillation period is therefore simply

$$f_{osc} = \frac{1}{2nT_{pd}} \tag{3.136}$$

where n is the number of inverters and f_{osc} the frequency of the oscillator. To control the oscillator, the propagation delay needs to be adjusted. The best way to adjust the propagation delay is by changing the load [45]

$$nf_{osc} = \frac{1}{R_2 C \ln\left(\frac{V_{DD}+V_T}{V_T} \times \frac{2V_{DD}-V_T}{V_{DD}-V_T}\right)} \tag{3.137}$$

where V_{DD} is the positive DC supply voltage and V_T the threshold voltage of the transistor. It is observed that if the loop was applied directly into I_1, the input protection diodes of the inverter would clamp the voltage of the loop and alter the timing significantly. This is avoided by using a decoupling resistor $R_1 >> R_2$. R_1 is chosen to be 100 Ω and R_2 is chosen as 10 Ω. The oscillator was chosen to oscillate at 1.4 GHz (large enough), as that will give a good negative voltage after the regulator. That will also keep the capacitor value

reasonably low. By substituting the values into equation (3.137), C can be calculated to give $C = 1$ pF.

Design of the rectifier circuit

Figure 3.83 shows the schematic of the rectifier circuit. The circuit is composed of two sections in cascade. That is a clamp formed by C_1, D_1 and R, and a peak rectifier formed by D_2 and C_2. C_1 of the clamp circuit also acts as the DC-blocking capacitor. A clamped circuit results when the output is taken across the diode, rather than across the capacitor. Due to the polarity in which the diode is connected, the capacitor will charge to a voltage V_P equal to the most positive peak of the input signal. A load resistance R is connected across the diode. That forces a net DC current through resistor, R. Since at this time the diode is off, this current comes from the capacitor, thus causing the capacitor to discharge and the output voltage to fall. The output voltage falls exponentially with the time constant RC.

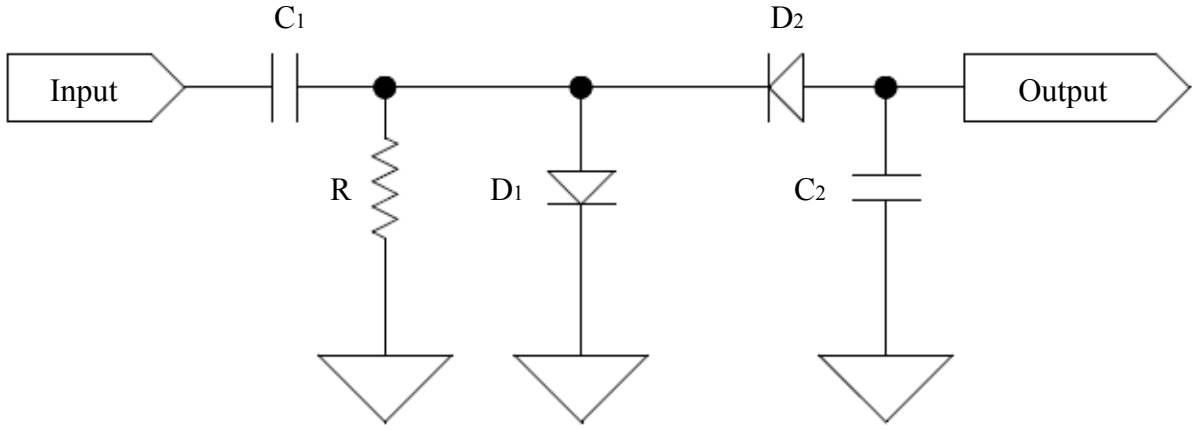


Figure 3.83.
Schematic of a rectifier. The diodes were implemented as shown in Fig. 3.91.

Note that the input voltage, excited by a sinusoid of amplitude $V_P \approx 300$ mV is clamped downwards, giving a positive peak of 0 V, while the negative peak reaches $-2V_P$.

A reversed diode peak rectifier converts the input sinusoid to a negative unipolar output. A filter is added to reduce the variations in the magnitude of the rectifier output. The filter rectifier can be discussed: let the input voltage v_{in} be a sinusoidal waveform with a peak voltage V_{peak} and assume the diode to be ideal. As v_{in} goes negative, the reverse-biased diode conducts and the capacitor is charged in order for the output voltage, $v_{out} = V_{PEAK}$. This situation continues until v_{in} reaches the negative peak value of V_{PEAK}. As v_{in} increases,

the diode cuts off and the voltage remains constant at $-V_{PEAK}$. Thus the circuit provides a DC voltage output equal to the negative peak of the input sine wave.

C_1 is chosen to be equal to C_2. With minor fine tuning on the circuit, the best results are given with R = 2 kΩ and $C_1 = C_2$ = 1 pF. Figure 3.84 shows the output of the negative DC voltage designed. A band-reject filter was added in series with the negative supply to filter out any of the oscillator's signal that leaked through.

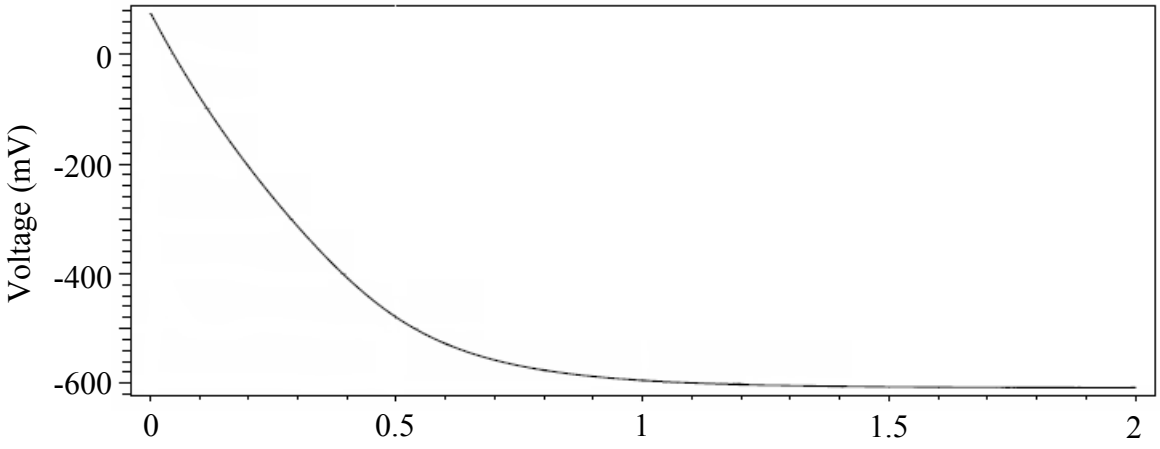


Figure 3.84.

Output from the negative supply.

Design of the input matching network

The input matching network matches the 50 Ω output impedance of the system, to the input impedance of the differential amplifier. Figure 3.85 shows the graph of the S_{11}-parameters at different frequencies for the 150 µm NMOS transistor. Interpolation was used to determine relevant parameters at 2.4 GHz.

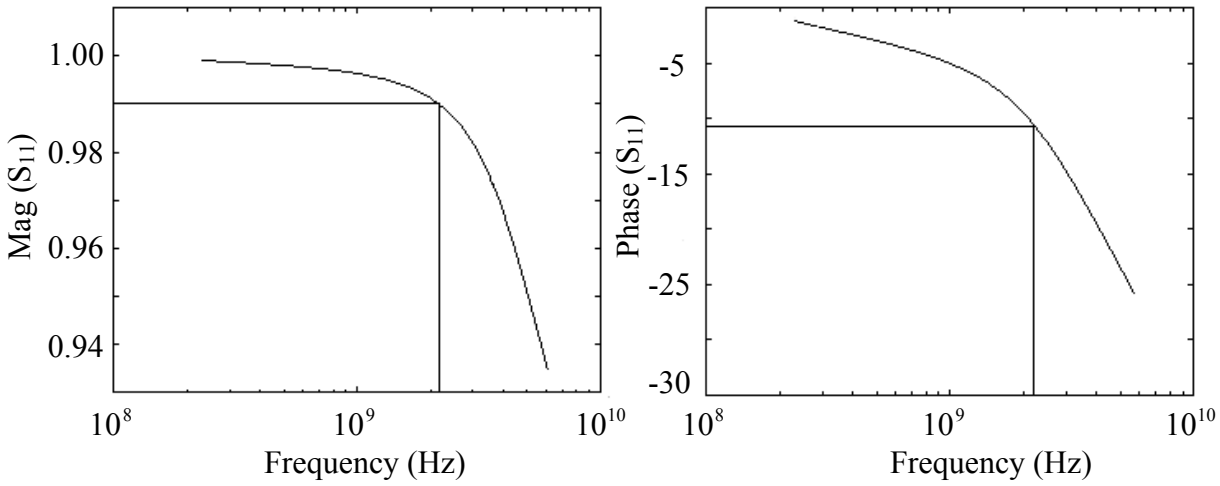


Figure 3.85.

S_{11} parameter for the 150 µm NMOS transistor [28].

Figure 3.86 shows the S_{22} parameters of the same transistor. Interpolation was used to determine relevant parameters at 2.4 GHz.

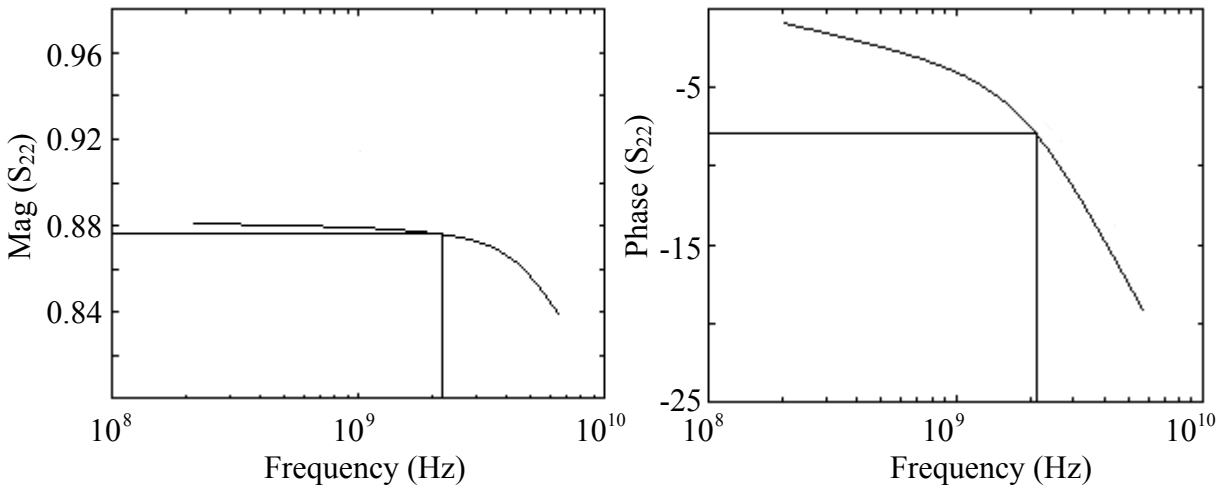


Figure 3.86.

S_{22}-parameter for the 150 µm NMOS transistor [28].

The *S_{21}*- and *S_{12}*-parameters of the NMOS transistor and all the S-parameters of the PMOS transistor were calculated in a similar way to the above. Table 3.11 shows the S-parameters of the NMOS and the PMOS transistors used at 2.4 GHz.

Transistor	**S_{11}**	**S_{22}**	**S_{12}**	**S_{21}**
NMOS (Mag)	0.99	0.875	0.03	1.695
NMOS (Phase)	-11˚	-8˚	81.5˚	167.5˚
PMOS (Mag)	0.6	0.59	0.81	0.76
PMOS (Phase)	-55˚	-53˚	-37˚	-3˚

Table 3.11.

S-parameters for the NMOS and PMOS transistors used at 2.4 GHz.

The differential amplifier (shown as part of Fig. 3.91) used a 150 µm NMOS transistor in parallel with an 18 µm PMOS transistor. For two transistors connected in parallel, the overall Y-parameter can be calculated by adding the individual Y-parameters [53].

The following equations are used to convert the S-parameters to the Y-parameters [53].

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{\Delta_6} \quad \textbf{(3.138)}$$

$$Y_{12} = \frac{-2S_{12}}{\Delta_6} \quad \textbf{(3.139)}$$

$$Y_{21} = \frac{-2S_{21}}{\Delta_6} \quad \textbf{(3.140)}$$

$$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{\Delta_6} \quad \textbf{(3.141)}$$

where

$$\Delta_6 = (1+S_{11})(1+S_{22})-S_{12}S_{21} \quad \textbf{(3.142)}$$

With these equations the Y-parameters of the two transistors were calculated and is tabulated in Table 3.12. Table 3.13 also shows the sum of the two transistor's Y-parameters.

Transistor	**Y_{11}**	**Y_{22}**	**Y_{12}**	**Y_{21}**
NMOS (Mag)	0.08	0.40	0.02	0.912
NMOS (Phase)	87.67˚	40.75˚	-90˚	-4.06˚
PMOS (Mag)	1.10	1.09	1.13	1.06
PMOS (Phase)	37.55˚	36.05˚	-178.06˚	-144.06˚
Total (Mag)	1.15	1.49	1.13	0.69
Total (Phase)	40.71˚	37.32˚	-177.25˚	-85.71˚

Table 3.12.

Y-parameters for the NMOS and PMOS transistors, together with the sum of the two transistors.

	S_{11}	**S_{22}**	**S_{12}**	**S_{21}**
Magnitude	0.26	0.25	0.52	0.32
Phase	-77.06˚	-113.49˚	-33.33˚	58.21˚

Table 3.13.

S-parameters for two transistors in parallel.

It is further given that

$$\Gamma_S = S_{11}^* \tag{3.143}$$

$$\Gamma_L = S_{22}^* \tag{3.144}$$

The input matching network is designed to match the output impedance of the transmitter to the input impedance of the differential amplifier (as shown in Figure 3.91). With the use of the computer program SMITH V1.91[7] and the new S-parameters calculated, the input impedance of the differential amplifier was calculated to be $(5 - j15)$ Ω. For an input matching network it is necessary to match the 50 Ω resistor to the input admittance. The input matching network was designed using the SMITH V1.91. It was necessary to have at least one series capacitor to be used as the DC-blocking capacitor.

The input admittance was calculated to be $(0.02 + j0.06)$ S, which means that the differential amplifier can be simulated with a resistor of 5 Ω and an inductor with an inductance of

$$L = \frac{I_M}{2\pi f} \tag{3.145}$$

where I_M equals the imaginary value of the input admittance and f the frequency of the circuit. The inductor was determined to be 3 pH. A frequency sweep simulation was done

[7] A mathematical modelling tool from the University of Berne.

on the circuit, to include 2.4 GHz. Figure 3.87 shows the schematic of the input matching network.

R_1 and v_s (200 μV_{peak}) serve to model the transmitter. R_2 and L_2 are the input admittances of the transistor as calculated earlier. C_1 and L_1 represents the input matching network. Figure 3.88 shows the result of the frequency domain simulation.

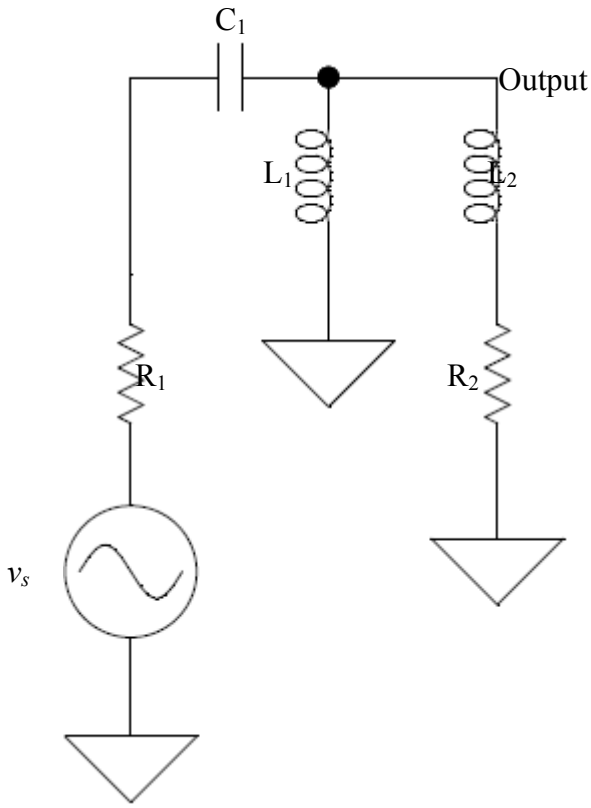


Figure 3.87.

Input matching network.

From Figure 3.88, it is clear to see that the input matching network has a voltage peak at 2.4 GHz.

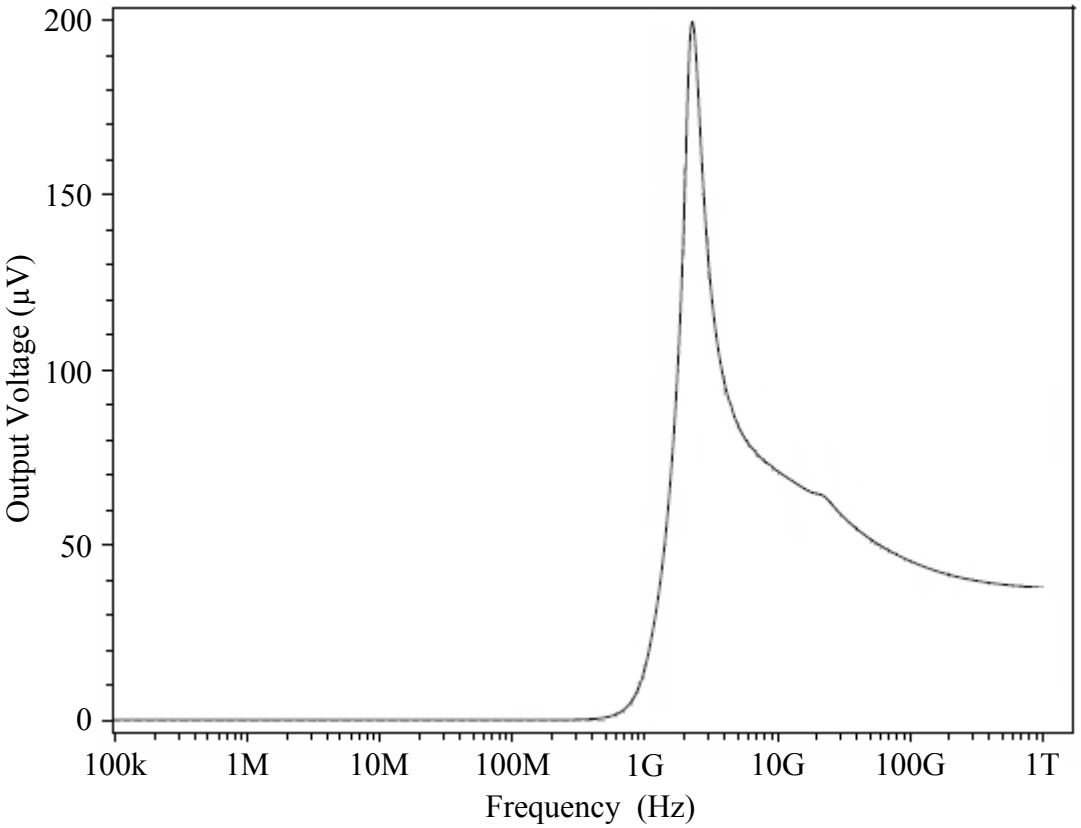


Figure 3.88.

Frequency sweep of the input matching network.

Design of the amplifier matching network

The amplifier matching network matches the output impedance of the differential amplifier to the input impedance of the class F amplifier. It was also implemented using passive elements as it needs to act as a DC-coupling capacitor, an inductor choke as well as the matching network. Figure 3.11 (a) shows that the differential amplifier is horizontally symmetric. This means that the output impedance of the differential amplifier can be calculated with the S-parameters in table 3.13. The amplifier matching network (shown in Figure 3.89) was also done using the SMITH V1.91 and the different S-parameters. It was necessary to have at least one series capacitor to be used as the DC-blocking capacitor and one parallel inductor to be used as an inductor choke. Just like the input matching network, the transistors were simulated using inductors, capacitors and resistor and a frequency sweep was done to confirm functionality. The amplifier matching network was adjusted to give the ideal peak. Figure 3.90 shows the result of the frequency sweep analysis done on the amplifier matching network circuitry. The frequency sweep shows a clear voltage peak at 2.4 GHz.

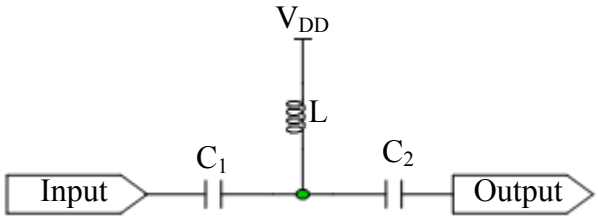


Figure 3.89.

Modified amplifier matching network. The final circuit is shown as part of Fig. 3.91.

Design of the output matching network

The output matching network was used to match the output impedance of the class F amplifier to the 50 Ω antenna. The output matching network included a DC-blocking capacitor and an inductor choke. The output matching network was designed in a similar way as the previous matching networks, using the NMOS S-parameters in table 3.11. Next the transistor was replaced with an equivalent capacitor and resistor pair, and a frequency sweep analysis was done on the circuit. The circuit was fine tuned until it gave the desired voltage peaked at the 2.4 GHz.

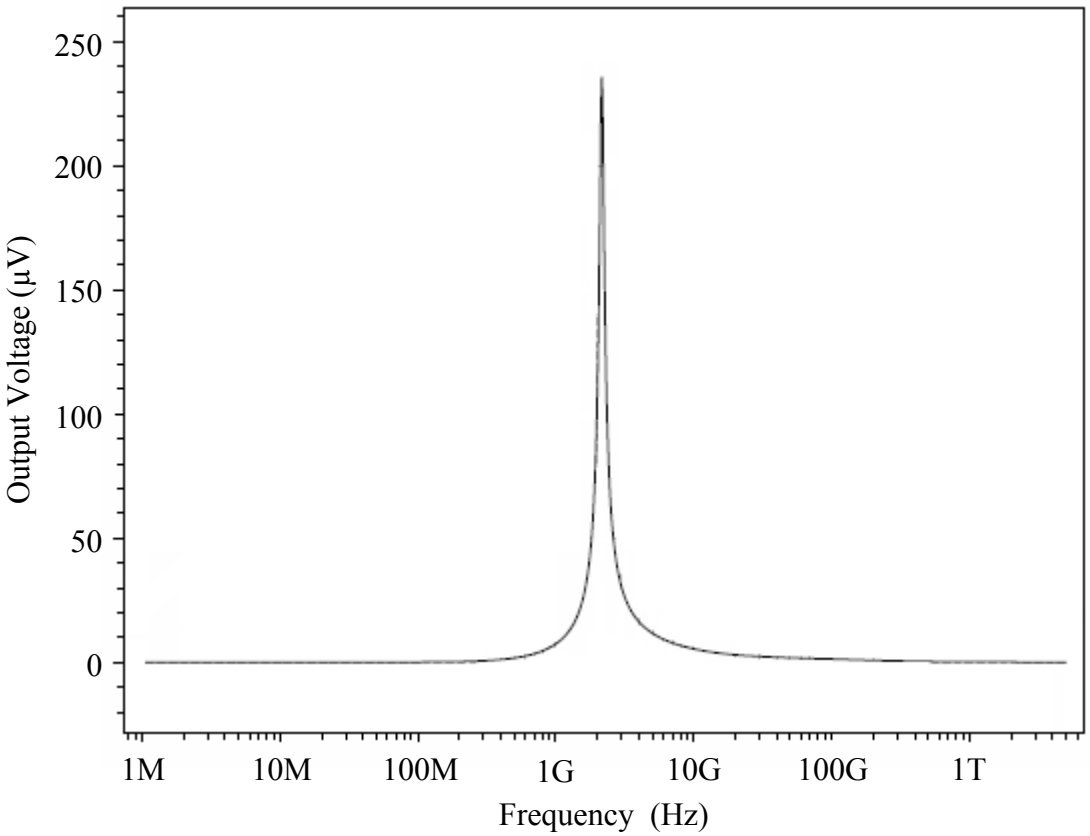


Figure 3.90.

Frequency sweep analysis of the amplifier matching network. An input signal of 250 µV was used for this simulation.

Complete implementation of the power amplifier

The various design blocks of the complete power amplifier were discussed in the previous sub-sections. The various design blocks were integrated, to also include the matching networks. Figure 3.91 shows the complete power amplifier. The values for the different components are tabulated in table 3.14.

The input (centred at about 2.4 GHz), v_s consists of 13 sine waves, each with amplitude of 10 mV spaced 50 MHz from each other. V_1 is the DC supply that controls the variable gain. V_2 and V_3 are used to bias the class F amplifier.

R1	140 Ω	C10	10 pF
R2	500 Ω	C11	12.92 pF
R3	80 Ω	C12	1 pF
R4	2 kΩ	C13	1 nF
R5	100Ω	C14	1 nF
R6	1000 Ω	L1	6.6 nH
R7	200 Ω	L2	7.32 nH
R8	50 Ω	L3	1 nH
R9	0 Ω	L4	25 nH
C1	2.91 pF	L5	1.57 nH
C2	0.44 pF	L6	25 nH
C3	1.43 pF	L7	1 nH
C4	0.50 pF	L8	0.5 nH
C5	0.62 pF	L9	0.5 nH
C6	0.44 pF	L10	1 nH
C7	0.69 pF	L11	0.5 nH
C8	1.38 pF	L12	8.4 nH
C9	0.31 pF		

Table 3.14.

Components used for the total system.

The layout of the power amplifier is shown in Figure 3.92.

Simulation results

Simulation results yielded a gain of (using a 50 Ω load impedance):

$$Gain = 10\log\left(\frac{V_o I_o}{V_i I_i}\right) \tag{3.146}$$

$$Gain = 10\log\left(\frac{(333.07mV)(194.36\mu A)}{(10mV)(8.61\mu A)}\right) \approx 28\,\text{dB} \tag{3.147}$$

The power added efficiency (PAE) was calculated with [48]

$$PAE = \frac{P_o}{P_{S1} + P_{S2} + P_i} \tag{3.148}$$

where P_o is the output power, P_{S1} is the power delivered by the source V2, is the power delivered by the source V3 and P_i is the input power. Parameters provided in table 3.15.

P_o	64.46 µW
P_i	1.90 µW
P_{S1}	5.01 µW
P_{S2}	72.94 µW

Table 3.15.

Calculated power at different stages of the amplifier.

The PAE was computed to be about 81 % (for five harmonic traps). Table 3.16 shows the variation in PAE for less harmonic traps.

ACPR is the ratio of power in the adjacent channel to the power in the main channel. ACPR values are widely used in the design of power amplifiers to serve as a measure of linearity [31]. As shown in Figure 3.93, the ACPR was computed to be -55 dB.

Total harmonic distortion (THD) is an important amplifier performance figure, a good figure for the THD for this thesis was chosen to be less than 1 % [47].

THD was calculated using:

$$THD = \frac{\sum_{n=2}^{\infty} V_{fn}}{V_{f0}} \tag{3.149}$$

where V_{fn} is the RMS voltage at the harmonics frequencies and V_{fo} is the RMS voltage at the fundamental frequency. Figure 3.94 shows the RMS value of the output voltage.

THD was computed to be about 0.6 %.

The *Q*-factor is an important measure for a power amplifier. Figure 3.95 shows a frequency sweep at the output to determine the Q-factor:

$$Q = \frac{f_O}{BW} \tag{3.150}$$

The *Q*-factor was calculated to be about 4. The low Q-value is attributed to the large number of passive on-chip inductors.

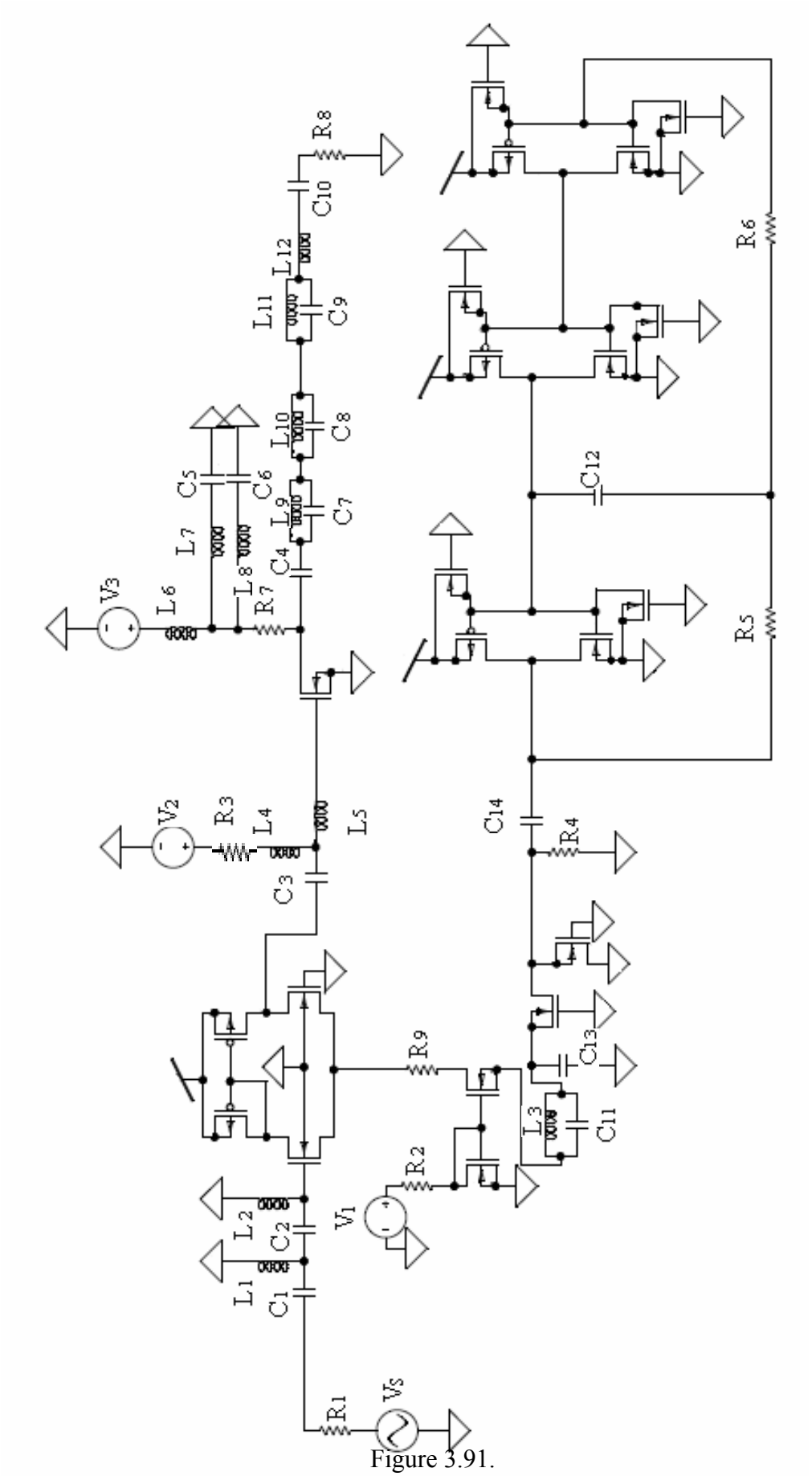


Figure 3.91.

Complete Class F power amplifier [72].

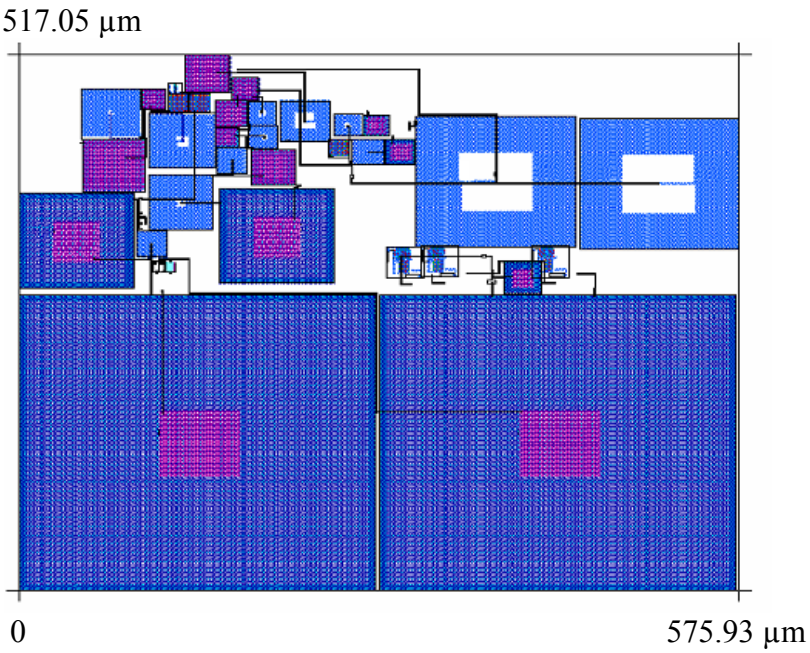


Figure 3.92.

Circuit layout for the power amplifier.

Harmonic traps	PAE
5	80.73%
4	80.27%
3	77.52 %
2	71.06 %
1	67.99 %
0	62.35 %

Table 3.16.

Effect of harmonic traps on PAE.

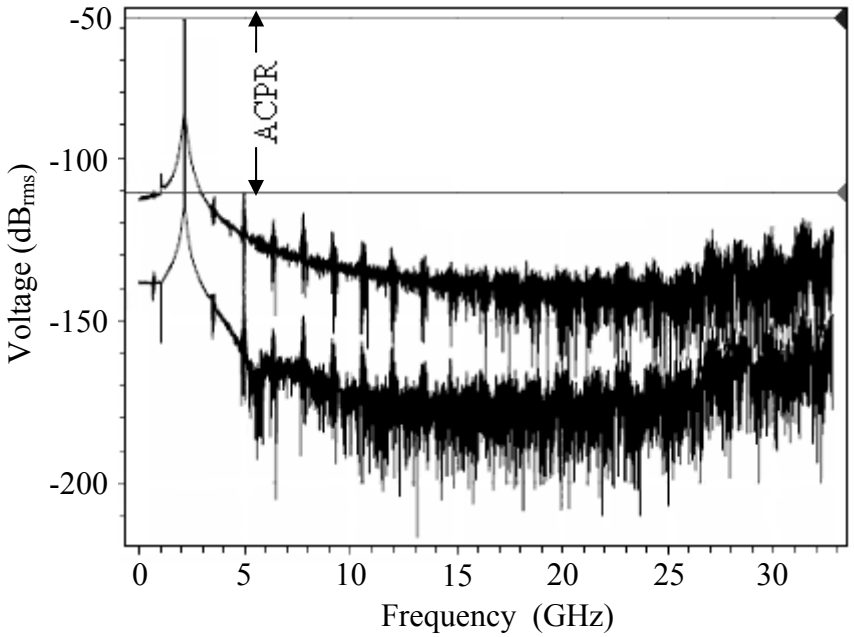


Figure 3.93.

FFT of the output voltage (top) and the input voltage (bottom).

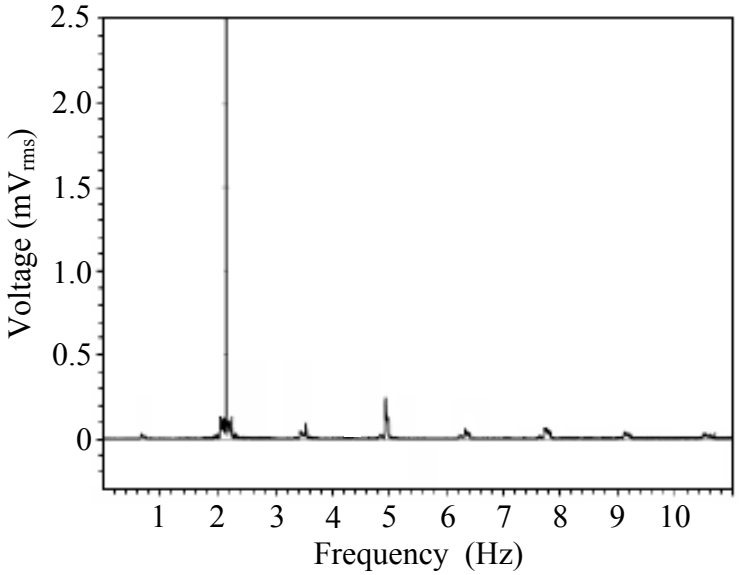


Figure 3.94.

RMS value of the output voltage.

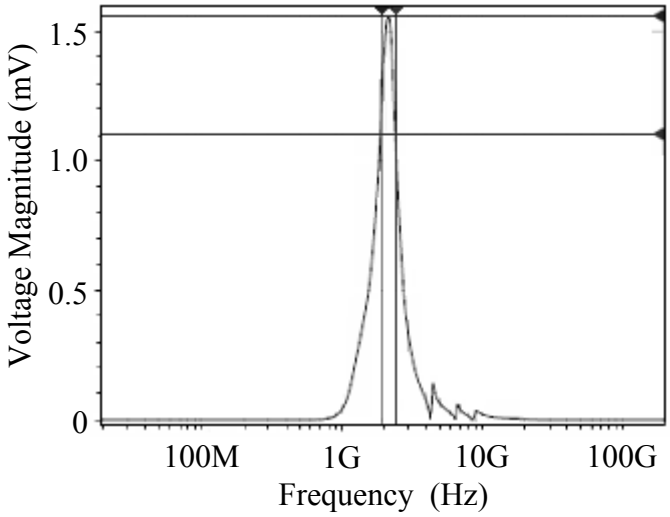


Figure 3.95.

Frequency sweep of the complete power amplifier. This figure aims to show the frequency range only – and used to determine the *Q* factor.

CHAPTER 4: DIGITAL AND MIXED SUB-SYSTEMS DESIGN

This chapter details the basic elements utilised for digital and mixed-circuit design. Since these circuits are quite common, the analysis done here is from an overview perspective only. Most textbooks on CMOS digital design cover these circuits in detail [54-55]. Furthermore, not all digital cells were designed by first principles, as AMS also provides such cells, as part of a digital library. With the exception of the digital buffer (last sub-section of this chapter), the sub-sections below represent cases where the AMS digital cells were not directly used.

4.1 Digital sub-systems

4.1.1 Bidirectional transmission gate

The switches in this thesis have been implemented as bidirectional transmission gates as shown in Figure 4.1 [55].

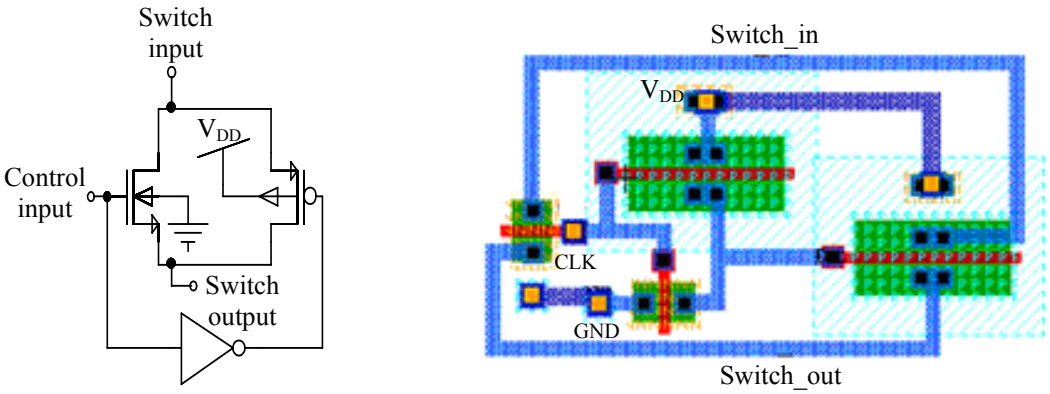


Figure 4.1.

Circuit schematic (left) for the bidirectional gate and (right) the layout of the circuit.

The advantage of using bidirectional gates instead of implementing the NMOS or PMOS as a stand alone switch is that the on resistance of the device is drastically reduced. This is given by

$$R_{on,eq} = R_{on,n} \parallel R_{on,p} \tag{4.1}$$

which is solved to yield,

$$R_{on,eq}^{-1} = \left[\mu_n C_{ox} \left(\frac{W}{L} \right)_n (V_{DD} - V_{THN}) - \left[\mu_n C_{ox} \left(\frac{W}{L} \right)_n - \mu_p C_{ox} \left(\frac{W}{L} \right)_p \right] V_{in} - \mu_p C_{ox} \left(\frac{W}{L} \right)_p |V_{THP}| \right] \tag{4.2}$$

If $\mu_n C_{ox} (W/L)_n$ is set equal to $\mu_p C_{ox} (W/L)_p$ and this factor is represented as β then equation (4.2) simplifies to

$$R_{on,eq}^{-1} = \beta \left[(V_{DD} - V_{THN}) - |V_{THP}| \right] \tag{4.3}$$

indicating that the on resistance of the switch is independent of the input voltage level. A simulation to verify the operation of this switch was generated in which the switch operated as a "chopper" on the input signal. It was found that the switch operated very well until about 500 MHz when its performance began to decline. This simulation is shown in Figure 4.2.

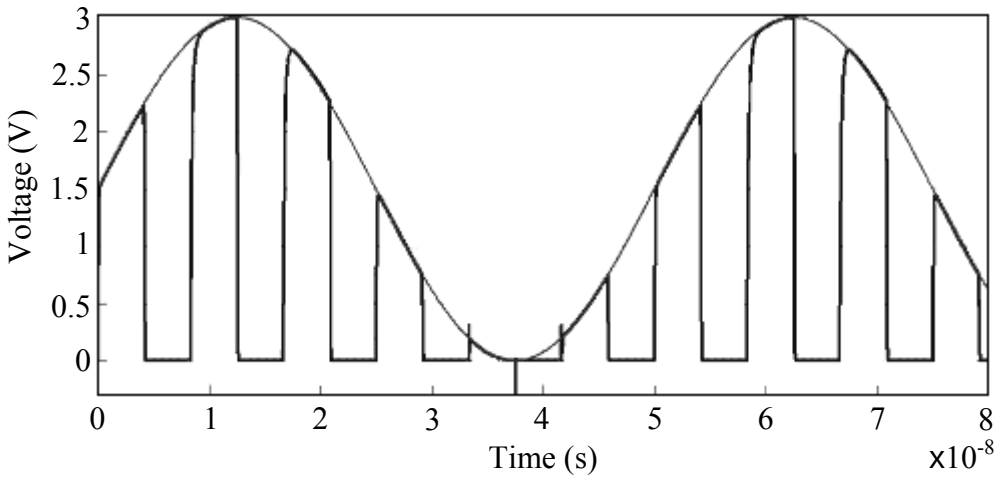


Figure 4.2.

Simulation of the switch implemented in a chopper configuration with a sinusoidal input and the chopped output shown in bold.

4.1.2 Logic gate - inverter

The CMOS logic inverter utilised uses two MOSFETs, one NMOS device and one PMOS device. The circuit schematic is shown in Figure 4.3 along with the layout.

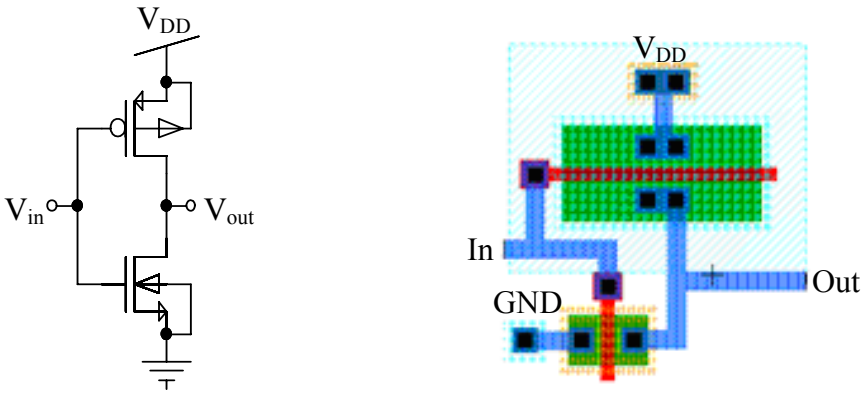


Figure 4.3.

Circuit schematic (left) and layout (right) for the CMOS logic inverter.

The circuit operates (in the extreme cases) as follows, when the input is high, the NMOS turns on and the PMOS turns off, thus pulling the output to ground. When the input is low, the NMOS turns off and the PMOS turns on pulling the input to V_{DD}.

To give the inverter symmetric transfer characteristics the widths must be set to

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \tag{4.4}$$

which was already done for the basic NMOS and PMOS transistors used for design in this thesis (see chapter 3). Using this fact, the maximum permissible input for the output to go high is given by V_{IL} can be calculated using ($V_{THP} \approx$ -0.5 V)

$$V_{IL} = \frac{3V_{DD} + 2V_{THP}}{8} \tag{4.5}$$

and the minimum permissible input for the output to go low, given by V_{IH} which can be calculated using

$$V_{IH} = \frac{5V_{DD} + 2V_{THN}}{8} \tag{4.6}$$

The transfer characteristic for the inverter is shown in Figure 4.4.

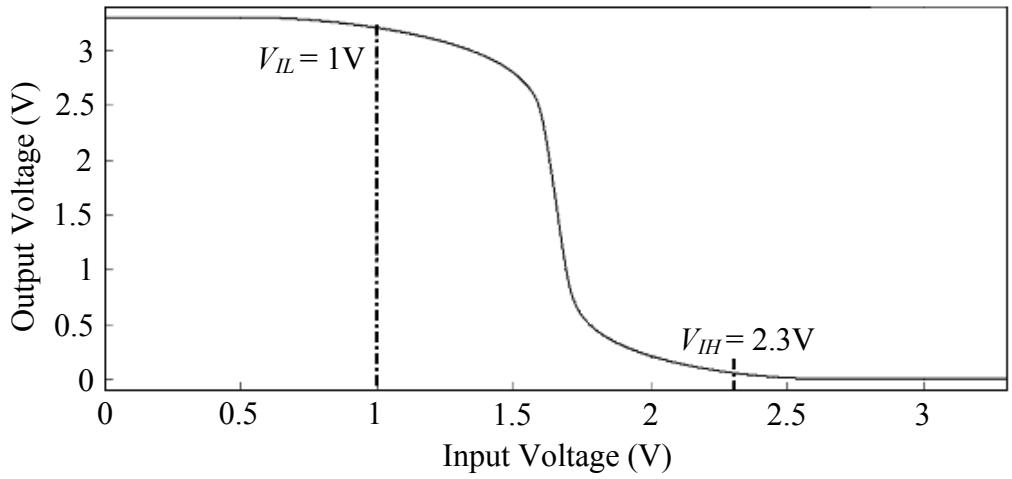


Figure 4.4.

Transfer characteristic for the logic inverter.

4.1.3 Logic gate – NAND

In the digital implementation of this circuit, 2-input NAND, 3-input NAND and 2-input AND gates were required. The switching point of the device can be determined using the fact that the two NMOS transistors in parallel are equivalent to one NMOS with $W_{n,eq} = 2W_n$ and the two PMOS devices in series are equivalent to one PMOS device with $L_{p,eq} = 2L_p$. Using these equivalences, the transconductance ratio of the two devices in the NAND gate be written as $\beta_n/4\beta_p$. Then the switching point of the NAND gate can be shown to be [55]

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{4\beta_p}} \cdot V_{THN} + \left(V_{DD} - |V_{THP}|\right)}{1 + \sqrt{\frac{\beta_n}{4\beta_p}}} \tag{4.7}$$

4.1.4 Logic gate – NOR

The NOR gate implemented for this thesis was a 2-input NOR gate, the schematic of which is shown in Figure 4.5, along with its layout. In a similar method of analysis to that of the NAND gate the transconductance ratio of a 2-input NOR logic gate can be calculated as $\sqrt{4\beta_n/\beta_p}$ and thus the switching point equation is given by

$$V_{SP} = \frac{\sqrt{\frac{4\beta_n}{\beta_p}} \cdot V_{THN} + \left(V_{DD} - |V_{THP}|\right)}{1 + \sqrt{\frac{4\beta_n}{\beta_p}}} \tag{4.8}$$

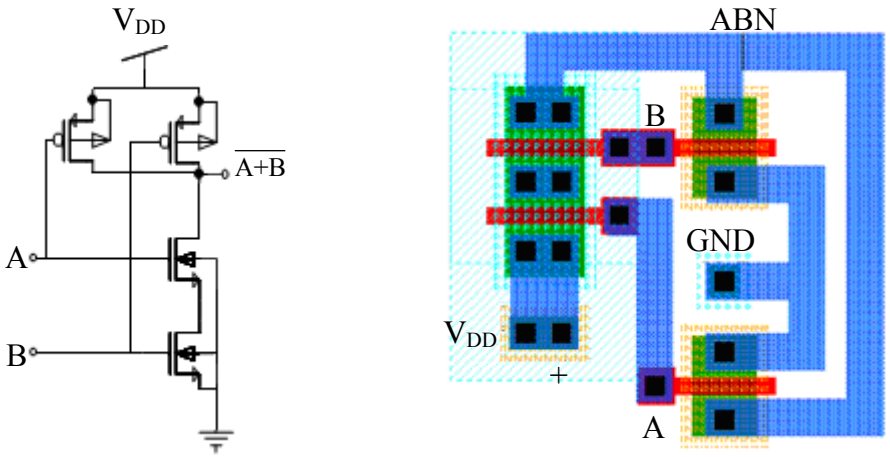


Figure 4.5.

Circuit schematic (left) and layout (right) of the logic NOR gate. All NMOS and PMOS have an aspect ratio of 5/1.

4.1.5 D-Type flip-flop (FF)

The D-FF implemented in this thesis was designed to trigger on the positive clock edge. The logic circuit for the D-FF [54] explains the functional operation of the D-FF, however to implement it using the logic gates proposed leads to many redundant circuit elements and inefficient operation of the device. A simpler implementation was used in this thesis which employs just switches and inverters to achieve the same functionality. The implemented circuit is shown in Figure 4.6 where all the switches implemented represent the transmission gate of the earlier section.

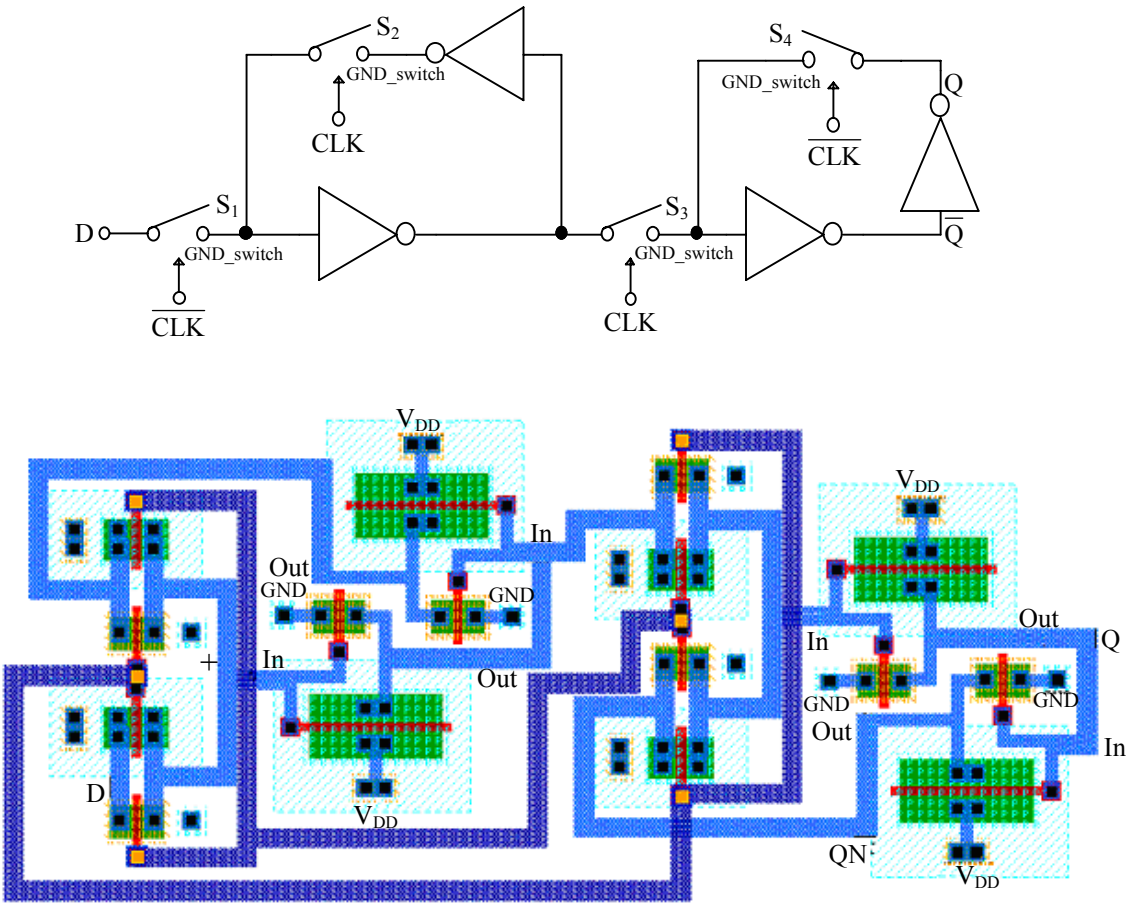


Figure 4.6.

Circuit schematic (above) of the edge triggered D-FF and (below) the layout of the circuit.

When the clock signal is low, switches S1 and S4 are on, allowing the "D" input to flow through the inverter. When the clock signal changes, S1 and S4 turn off while S2 and S3 turn on, and the inverse value of the "D" input from the previous state is passed through switch S3 and inverted again to give output "Q", which also flows through an inverter to yield its inverse. When the clock returns to low, the value of Q and its inverse circulates in the now closed loop, holding their values constant until the clock goes high again.

Implementing the circuit as described above not only increases the speed and efficiency of the D-FF, but also uses far less die area than its logic gate counterpart.

4.1.6 Counter

A synchronous 4-bit binary counter was implemented in this thesis. The choice of this counter was based on the design of a parallel-to-serial converter (section 4.1.7) which

implements two such counters [54]. The circuit schematic of the counter implemented is shown in Figure 4.7.

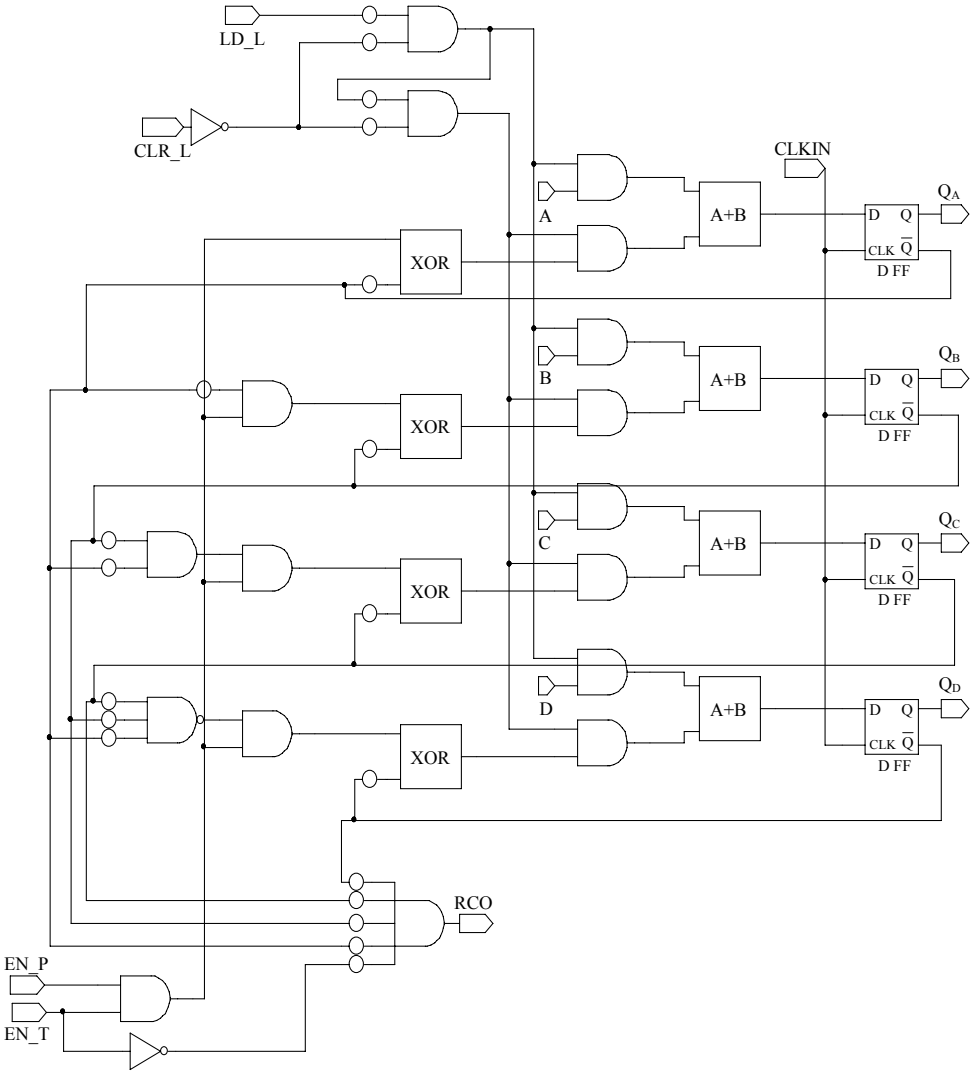


Figure 4.7.

Counter logic diagram [54].

Each input to the D-FFs shown is driven by a 2-input multiplexer (the two AND gates whose output provides the input to the OR gate). The multiplexer is controlled by the active-low clear signal and its output is cleared if the clear signal goes low. If the active-low "load" input goes low then the top AND gate in the multiplexer passes the four input signals through to the output. If both the "load" and the "clear" inputs are high (not activated) then the bottom AND gate of each multiplexer passes the output of the XNOR gate to the counter output. The actual counting performed by the device is done by the XNOR gates. The "ripple carry over" output signal indicates carry and is at logic 1 when all the output count bits are logic 1.

4.1.7 Parallel-to-serial (P/S) converter

The P/S converter combines data from many parallel streams into one serial stream [54]. It is used at the back-end of the receiver running in unbalanced mode. The circuit schematic for this register is shown in Figure 4.8. The operation is far simpler than that of the counter. The multiplexer at the input to the D-FF operates in basically the same manner as the counter, when the load signal goes low, the parallel input signals are loaded to the D-FF. When the load signal is low the clock shifts the loaded values, essentially creating the serial output.

Figure 4.10 shows simulation results (from the layout – shown in Figure 4.9) to indicate the position of each bit in the serial data stream. As can be seen from the figure, the output signal B7_L indicates the start of a new 8-bit serial word. Each bit was tested individually to show its position in the serial word, this is shown in the figure, with reference to the clock signal.

4.1.8 Serial-to-parallel (S/P) converter

S/P converter distributes data into different data lines. The number of data lines determines the reduction in data speed. It is used at the front end of the transmitter which runs in an unbalanced mode. To ensure the success of conversion, a digital clock is used. For this thesis, a 4-bit S/P conversion was deployed using one 2-bit counter, one 4-bit serial-in parallel-out shift register and one 4-bit register [54].

4.1.9 Clock recovery

Clock recovery is the only synchronisation scheme used in the system. It is used on the front-end of the transmitter to recover the clock from the data stream so that it can be used for the S/P conversion. The clock recovery circuit is shown in Figure 4.12. It is based on two sub-systems [56]:

- edge detection, where edges are detected whenever the data makes 0-to-1 or 1-to-0 transition, and
- a counter, that runs in the free mode by means of an external clock, and resets whenever an edge is detected in the data stream. The counter is driven by an external clock that is required to run approximately eight times faster than the recovered clock.

The circuit was simulated for a data bit period of 1 µs as shown in Figure 4.13.

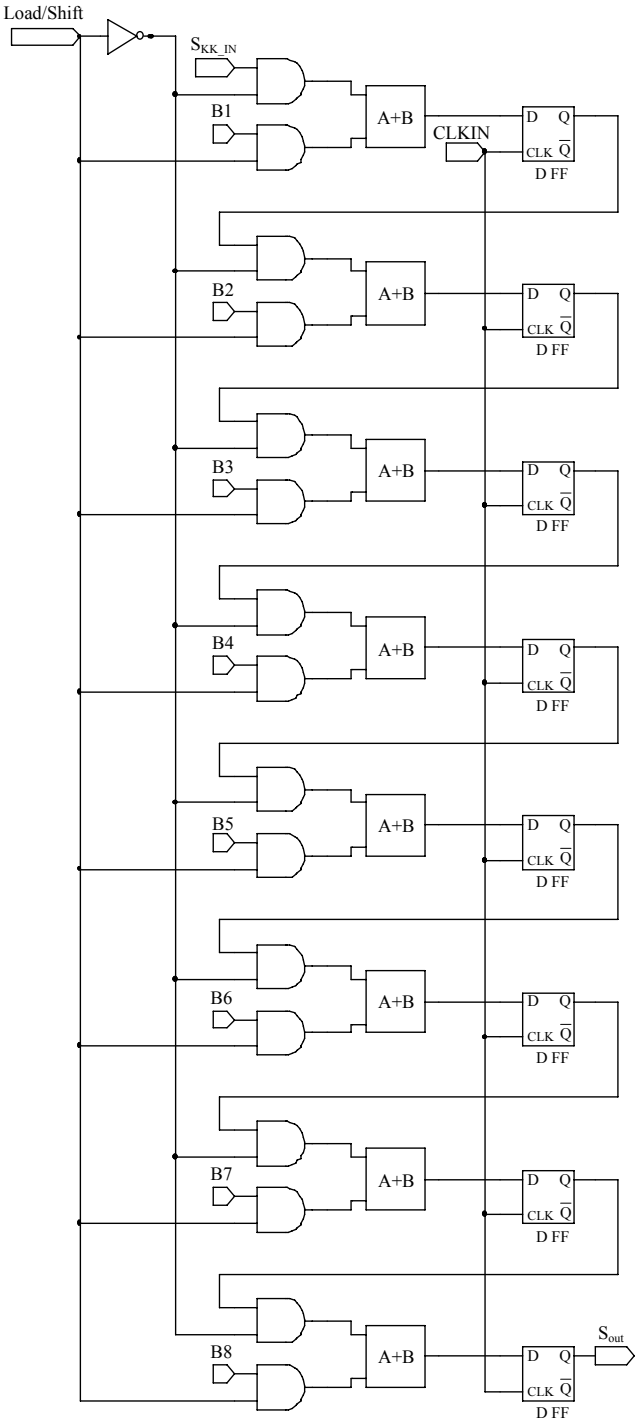


Figure 4.8.

P/S converter [54].

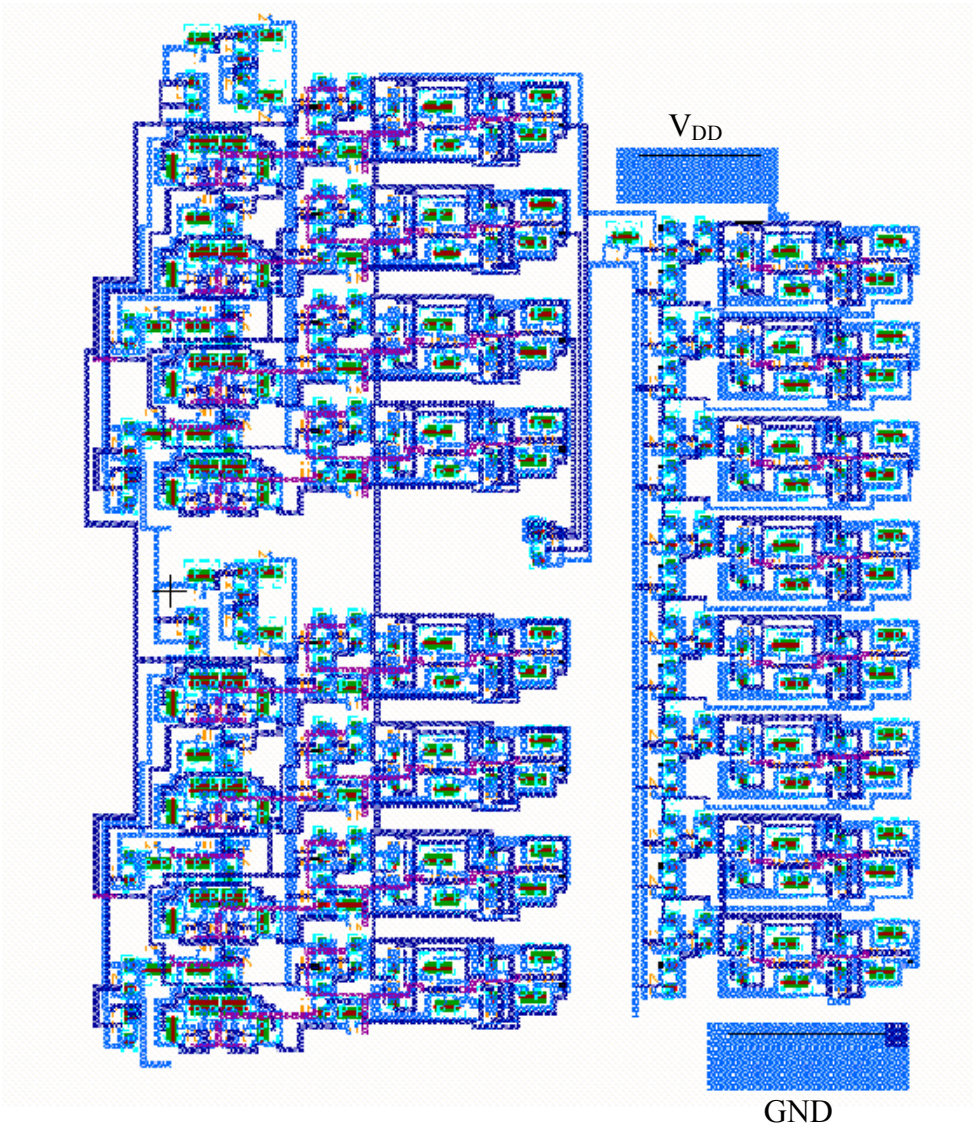


Figure 4.9.

Layout of the P/S Converter.

4.1.10 Error correction

This block is a piece of digital circuitry used to correct errors in the receiver if it is running in the balanced mode. If a bit in one of the four branches is received in error, the circuit will ignore it based on the data in other three branches. If two bits in two branches are received in error, the circuit will assume that 0 is received. If more than two branches are in error, the error will not be detected. The truth table for such a circuit is shown in table 4.1.

The function of the circuit can be derived to be

$$O = X.Y.Z + W.Y.Z + W.X.Z + W.X.Y \tag{4.9}$$

$$O = \mathbf{(}\{[(X.Y.Z)'.(W.Y.Z)']' + [(W.X.Z)'.(W.X.Y)']'\}'\mathbf{)}' \tag{4.10}$$

The implemented circuit is shown in Figure 4.14.

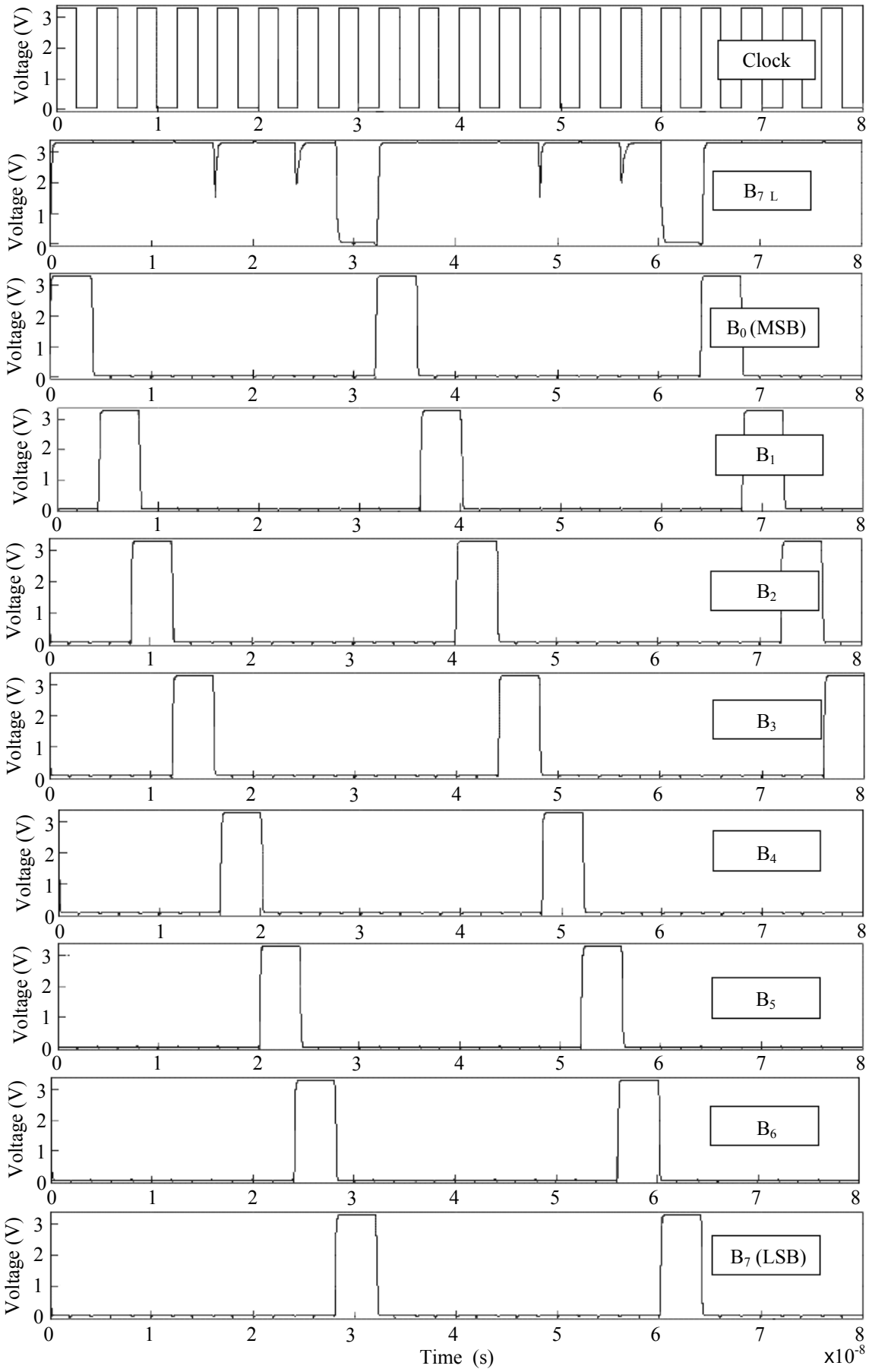


Figure 4.10.

Serial output for each of the bits that were tested for the P/S converter.

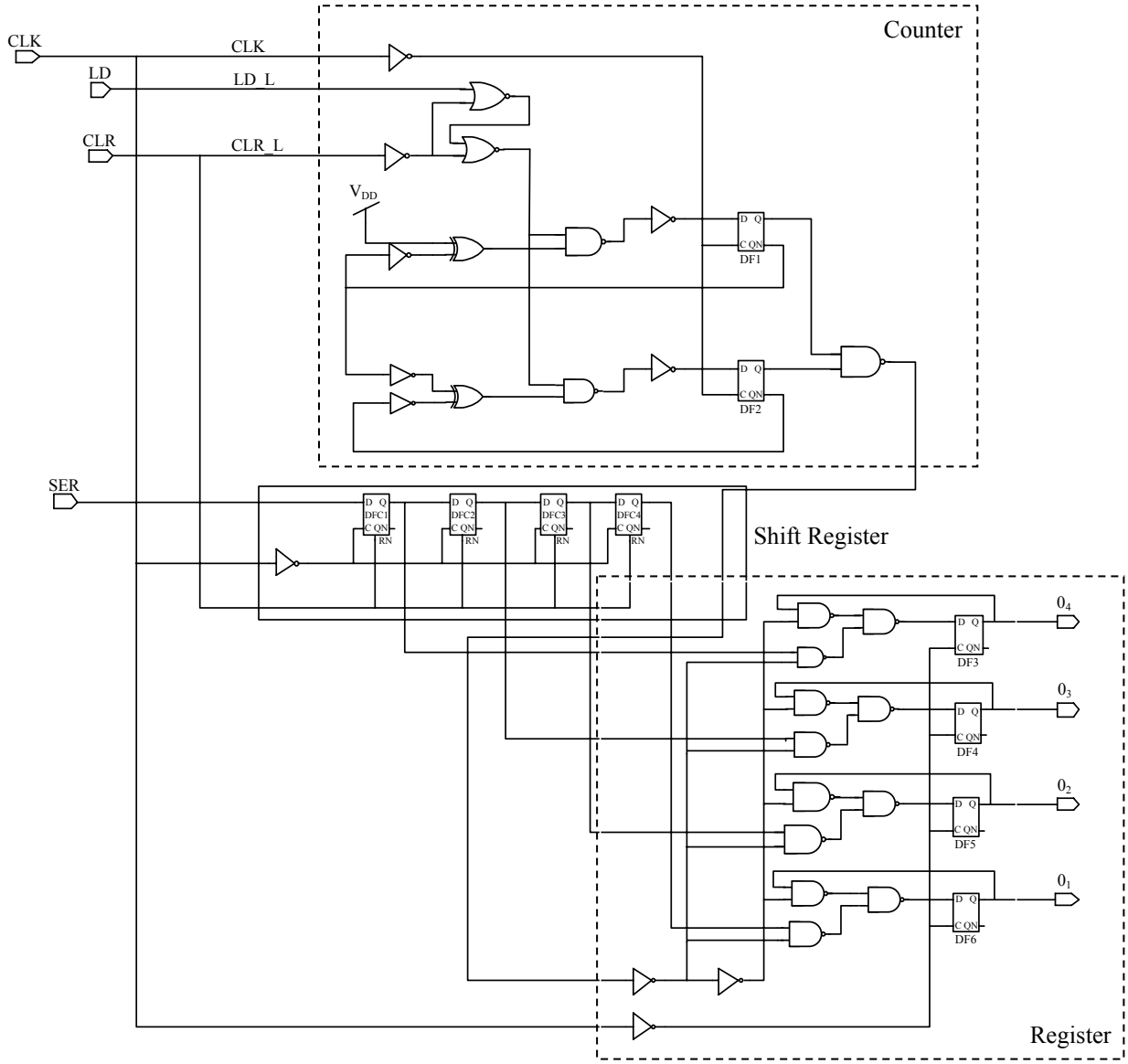


Figure 4.11.

S/P converter [54].

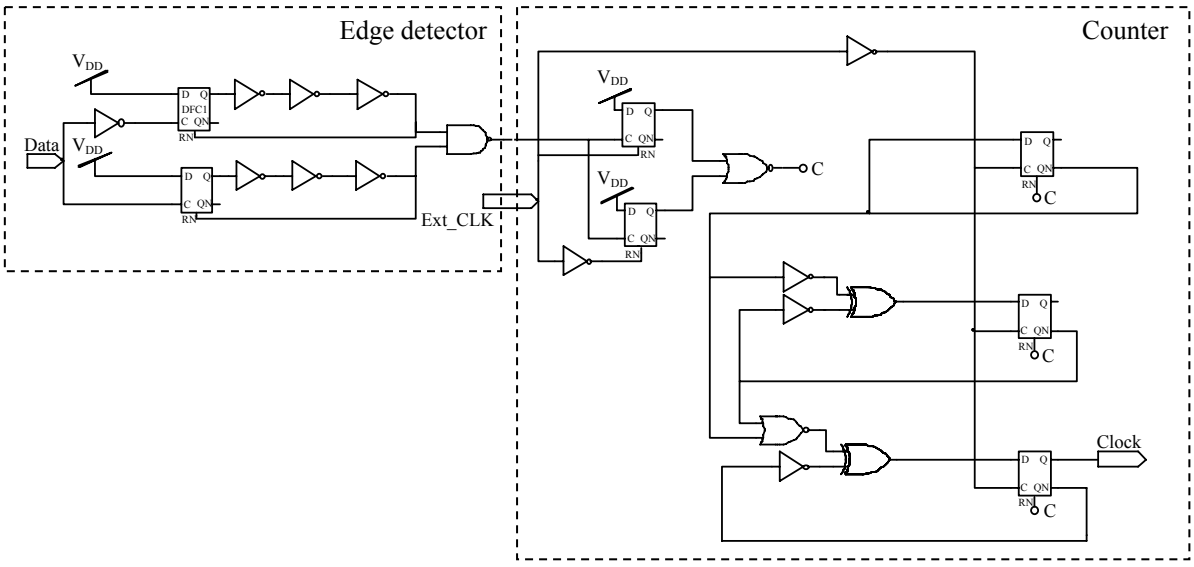


Figure 4.12.

Clock recovery circuit.

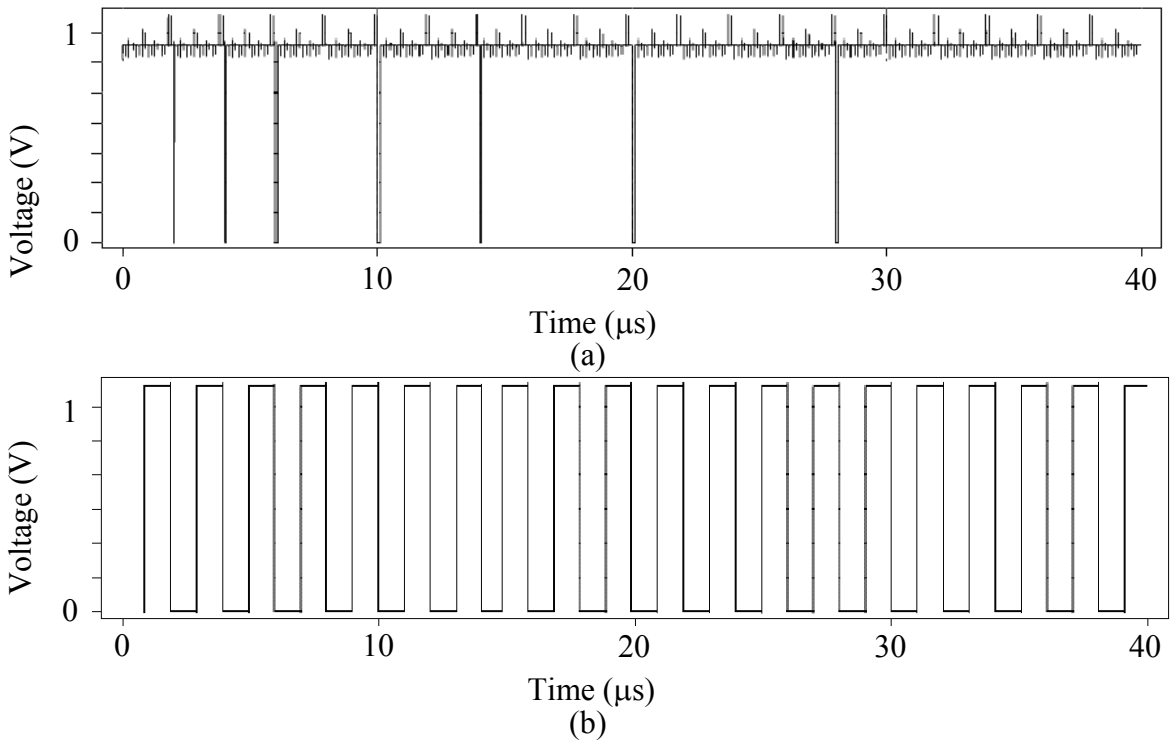


Figure 4.13.

Clock recovery circuit operation (a) shows detected edges, and (b) shows the recovered clock.

Branch 1 (W)	Branch 2 (X)	Branch 3 (Y)	Branch 4 (Z)	Common stream (O)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 4.1.

Truth table for the error correcting circuit.

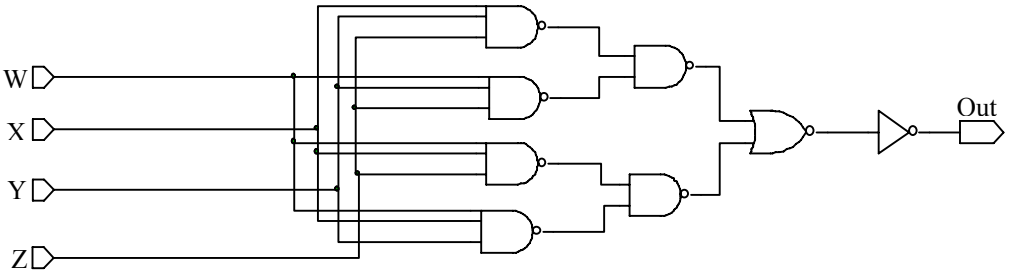


Figure 4.14.

Error correction circuit.

4.2 Mixed circuit sub-systems

4.2.1 Sequence mixer

The sequence mixer is not actually a mixer [71], but a decision circuitry that selects either a positive or a negative version of the real or imaginary part of the CSS. It is based on an analogue CMOS switch. Since the outputs of this block are differential and can be modulated later in the process, a mixing function is established. Depending on whether the data bit is 0 or 1, the CMOS switch is either ON or OFF. The switches work in pairs, so that if one is OFF, the other one is ON. In this way, either an inverted or non-inverted version of the sequence is passed through. The smallest length and width of the transistor of 0.35 µm and 0.7 µm respectively has been chosen for this thesis. The schematic of the sequence mixer is shown in Figure 4.15.

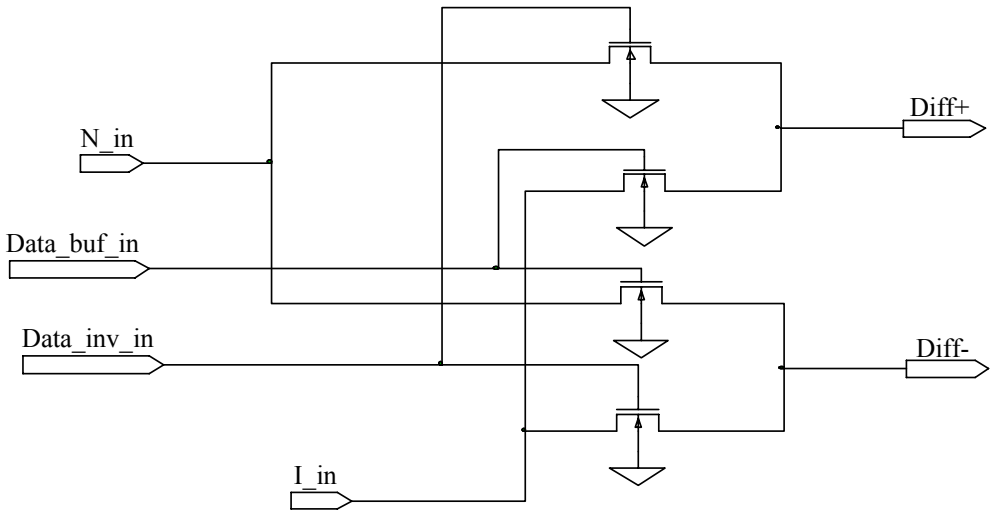


Figure 4.15.

Sequence mixer circuit.

4.2.2 Digital buffer

Buffering is needed when a signal does not exactly have the voltage level of 0 V for bit 0 and 3.3 V for bit 1. Analogue voltages close to these, when passed through a buffer, give exact digital voltages. The non-inverting buffer is a standard CMOS block available in the Tanner digital library. Its symbol is shown in Figure 4.16.

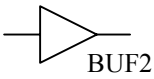


Figure 4.16.

Symbol of the buffer, as part of the AMS digital library.

CHAPTER 5: SYSTEM INTEGRATION

In Chapter 2, the overall system analysis has been accomplished. Chapters 3 and 4, separately, conceptualize the analogue and digital sub-systems. This chapter serves to integrate the analogue and digital sub-systems to verify whether the system specifications proposed in Chapter 2 are met.

5.1 Simulation results for the integrated system

Integration is achieved as shown in Figure 2.17. In summary:

Transmitter

Inputs:

- digital data signal, f_a,
- CSS (real and imaginary parts),
- external clock signal (running at 8 f_a), and a
- digital HIGH or LOW determining whether the transmitter operates in balanced or unbalanced configuration.

Output: 50 Ω antenna (to be connected to the PA output).

The external clock signal is a required input signal for digital sub-systems and is denoted as `CLK_IN` or `CLKIN` in Chapter 4.

Receiver

Inputs:

- CSS (real and imaginary parts),
- 50 Ω antenna (connected to the LNA input),
- synchronization clock signal (same rate as data rate), and a
- digital HIGH or LOW determining whether the receiver operates in balanced or unbalanced configuration.

Output: Received data signal.

Figure 5.1 presents the test setup for simulating the DSSS transceiver.

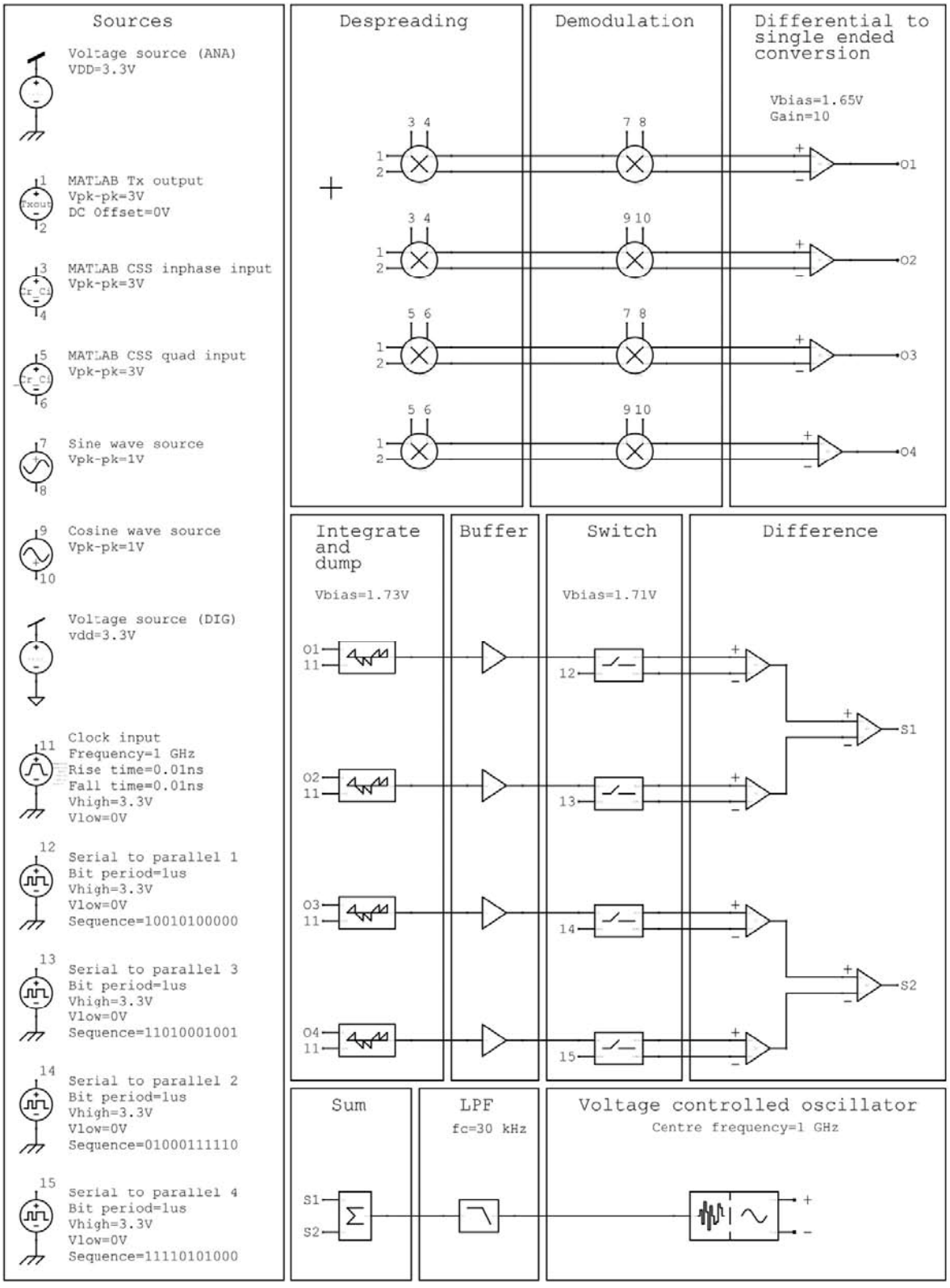


Figure 5.1.

Test signals used in simulating (exported from S-Edit) the DSSS transceiver.

Figure 5.2 captures an overview, and Figures 5.3 – 5.5 depicts the sequences used for the receiver.

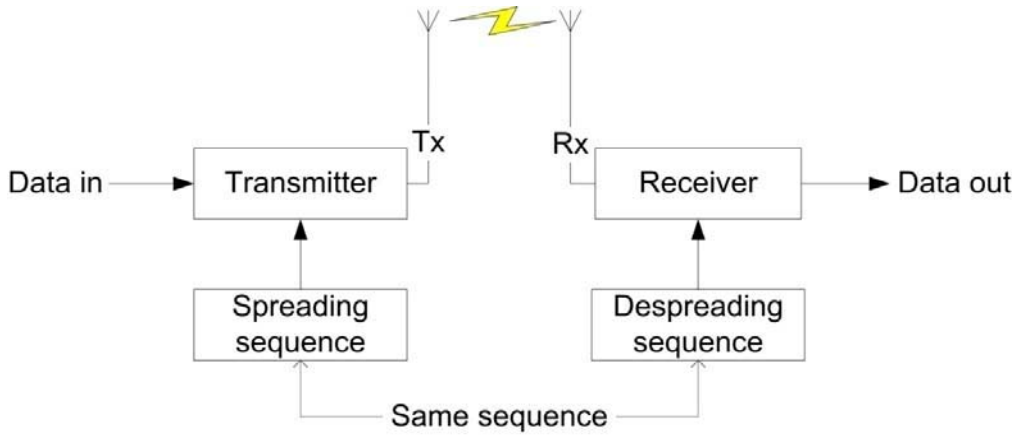


Figure 5.2.

Overview of transceiver setup.

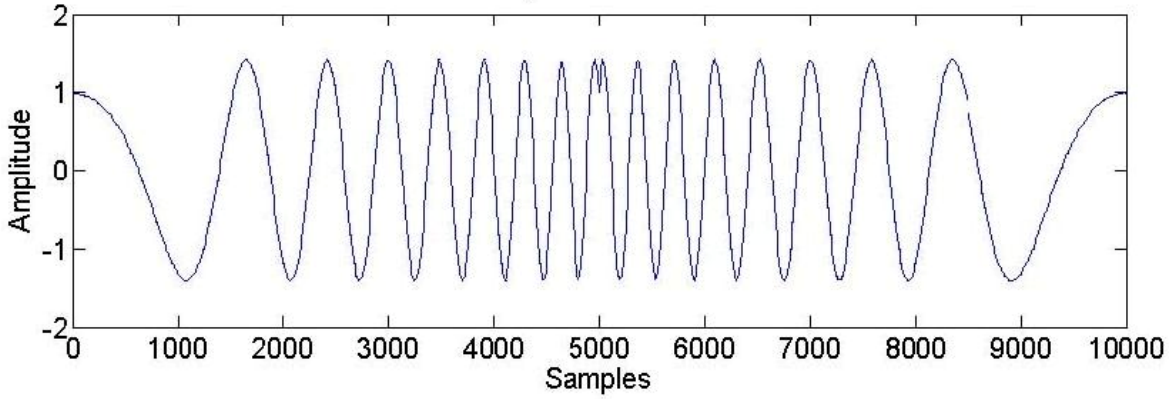


Figure 5.3.

In-phase CSS (L=64)

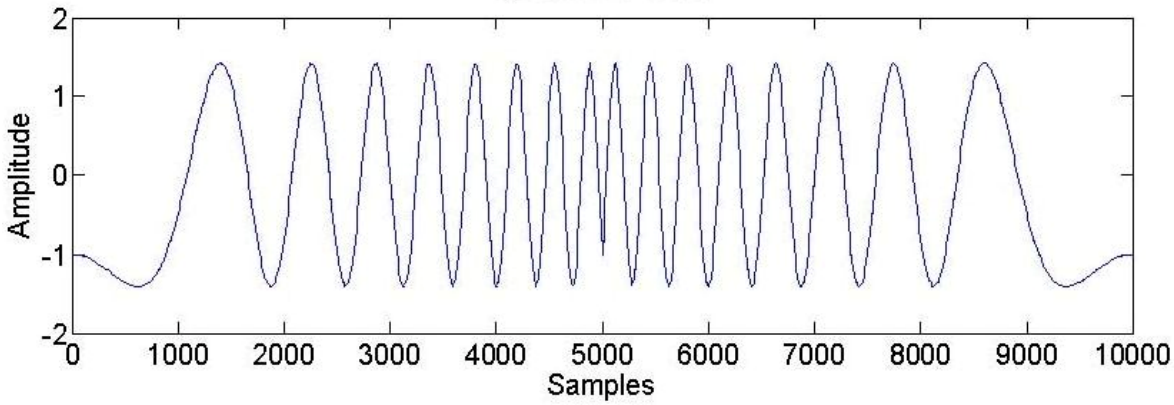


Figure 5.4.

The quadrature CSS (L=64)

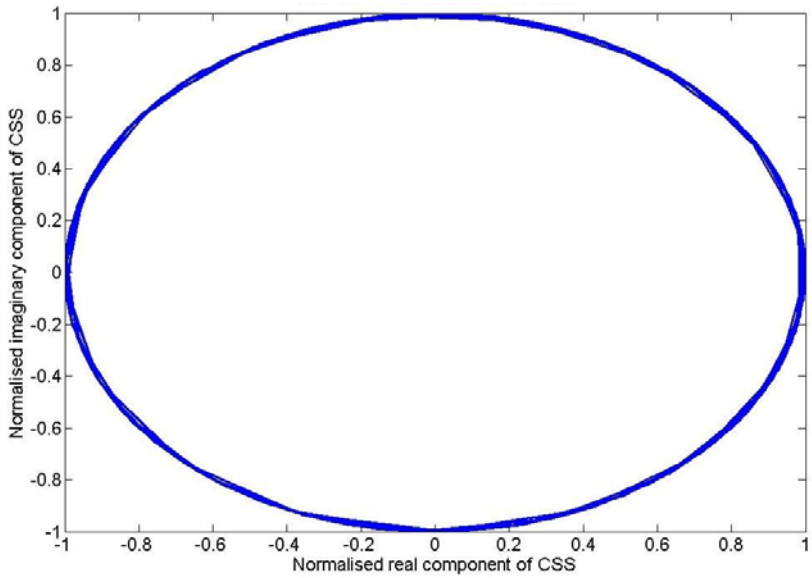


Figure 5.5.

The real versus imaginary part of the CSS (L=64).

The output of the transmitter is shown in Figures 5.6 and 5.7.

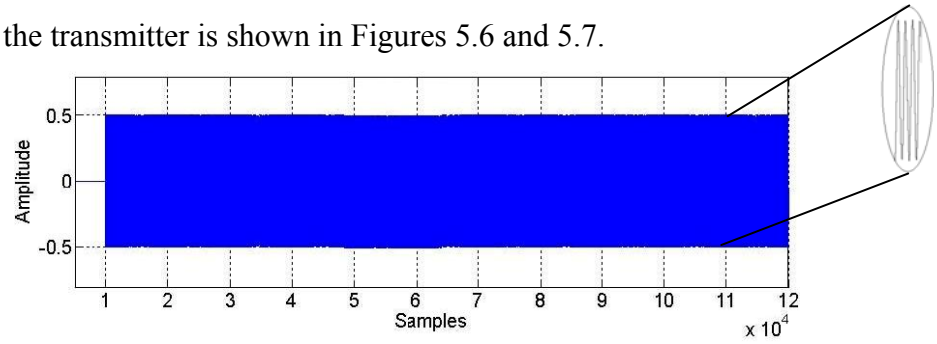


Figure 5.6.

The time domain output of the transmitter.

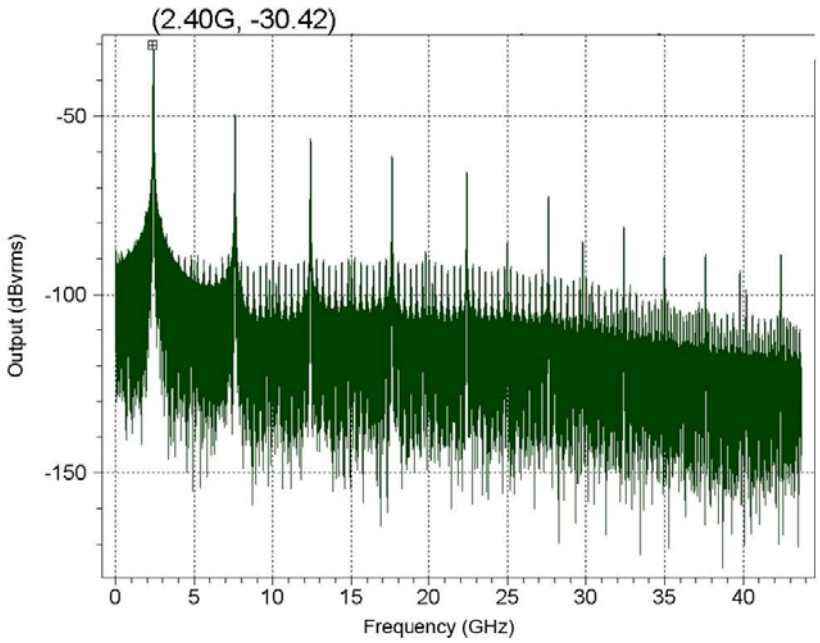


Figure 5.7.

The frequency domain spectrum of the transmitter.

As the receiver is a more complex system (Figure 2.18), step-by-step results are provided. The result of the top-branch is provided here. The output of despreading and demodulation is presented in Figures 5.8 and 5.9, respectively.

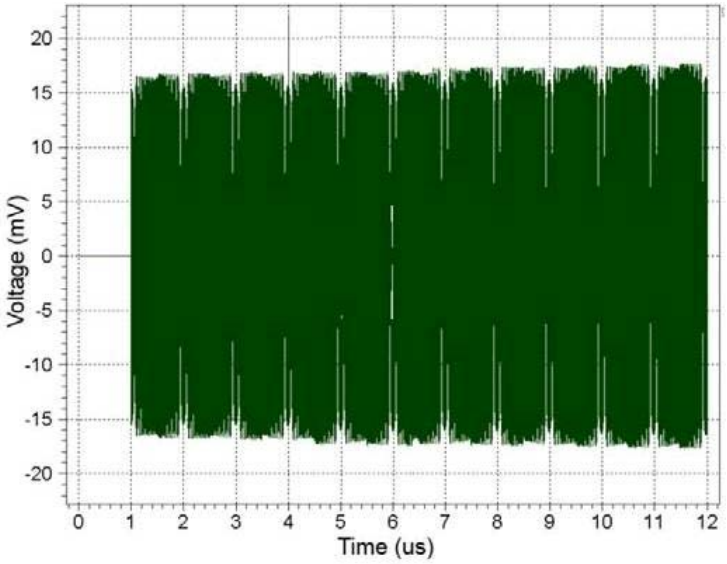


Figure 5.8.

Despread output (in-phase branch).

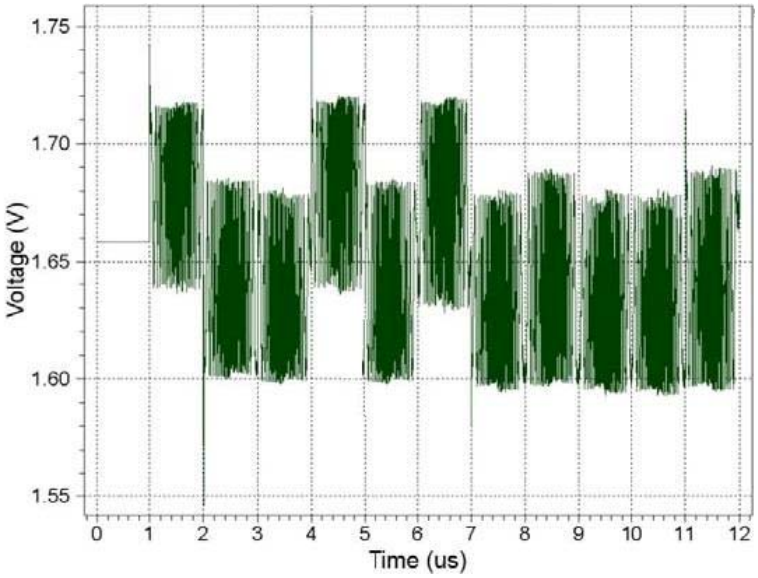


Figure 5.9.

Demodulated output (in-phase branch)

Due to the inherent bandwidth of the CMOS mixers, the double frequency terms are partially suppressed. An unexpected attribute of the CMOS demodulated output was the inconsistent bit voltage levels. This inconsistency is most likely to have been caused by the nonlinear characteristics such as inter-modulation products of the demodulating mixer components.

Figure 5.10 presents the integrate and dump circuit. As expected, a bipolar ramp output is achieved.

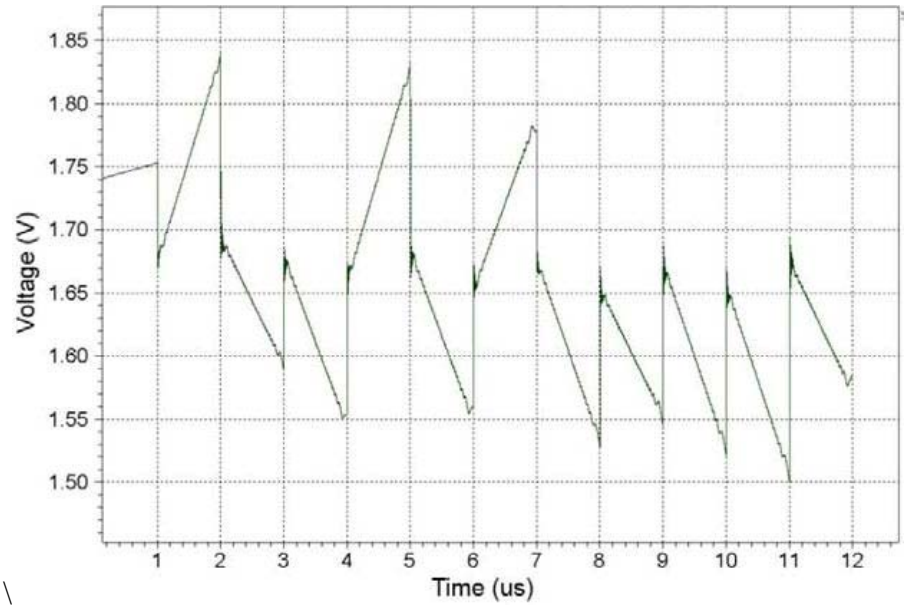


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Figure 5.10.

The output of the integrate and dump circuit.

5.2 Qualification test protocol

The main specifications of the thesis (as presented in Chapter 2) are firstly verified by SPICE simulations. Selected sub-systems were also submitted for prototyping, the results are included later in the chapter.

Some specifications are defined by inputs to the system. The length and sampling rate of the CSS have been chosen arbitrarily, for these simulations it has been assumed that the chip rate of the sequence can be fixed externally to 20 Mchips/s. The sampling rate of 160 MSamples/s can be determined from the time-domain simulation of the CSS. The signal data rate is also a specified input. The modulation technique is evident from the conceptual design performed in Chapter 2. The assumed bandwidth, carrier frequency, transmitter power, receiver sensitivity, BER and power dissipation are important specifications that are verified in the next few sub-sections. These parameters have been verified mathematically in Chapter 2: in this chapter, the simulations are extended to further include process and component tolerances.

5.2.1 Carrier frequency of the transmitted signal

A data rate of 4 Mbits/s and a sequence sampling rate of 104 MSamples/s were used for this simulation. Figure 5.11 shows the FFT simulation of the transmitted signal within the range of 0 to 10 GHz. The highest magnitude lies between 2 and 3 GHz. Figure 5.12 shows a zoomed-in version of the same FFT graph: it is clear that the centre frequency is at about 2.4 GHz.

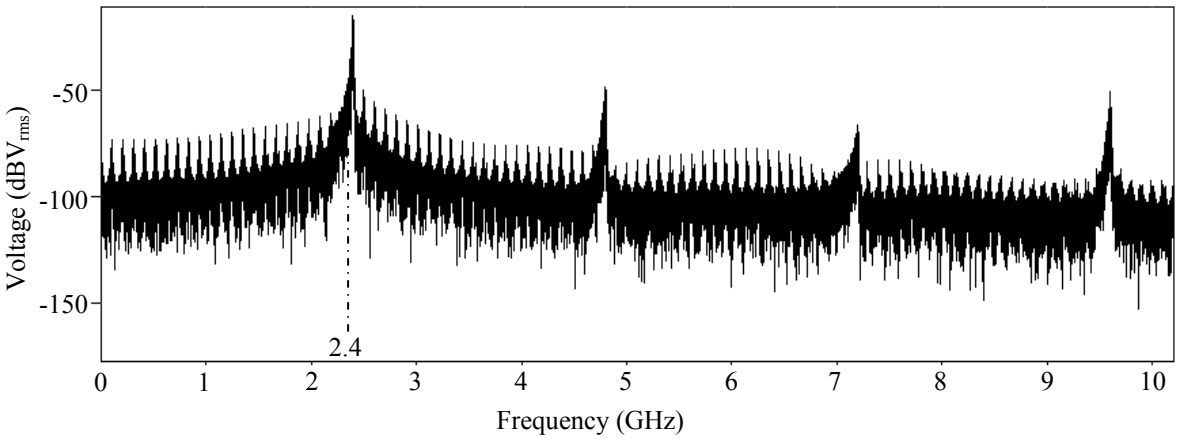


Figure 5.11.

FFT of the transmitted signal.

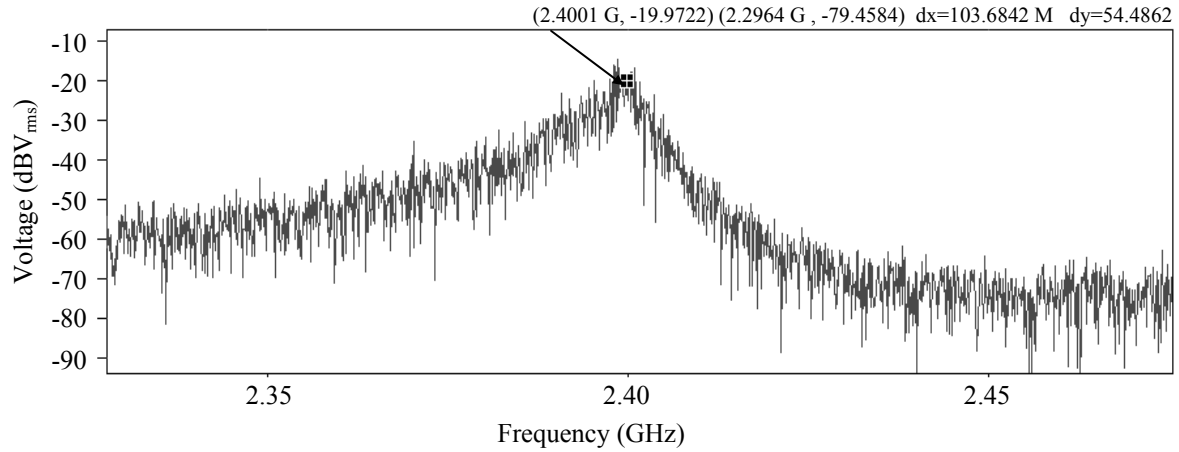


Figure 5.12.

Zoomed-in view of Figure 5.11 to show the carrier frequency.

5.2.2 Transmission bandwidth

A data rate of 6.12 Mbits/s and sequence sampling rate of 160 MSamples/s were used, as the sampling rate directly influences the bandwidth. Figure 5.13 shows a simulation of the

bandwidth. A zoomed-in version is shown in Figure 5.14, it can be seen that the bandwidth is much smaller than 20 MHz.

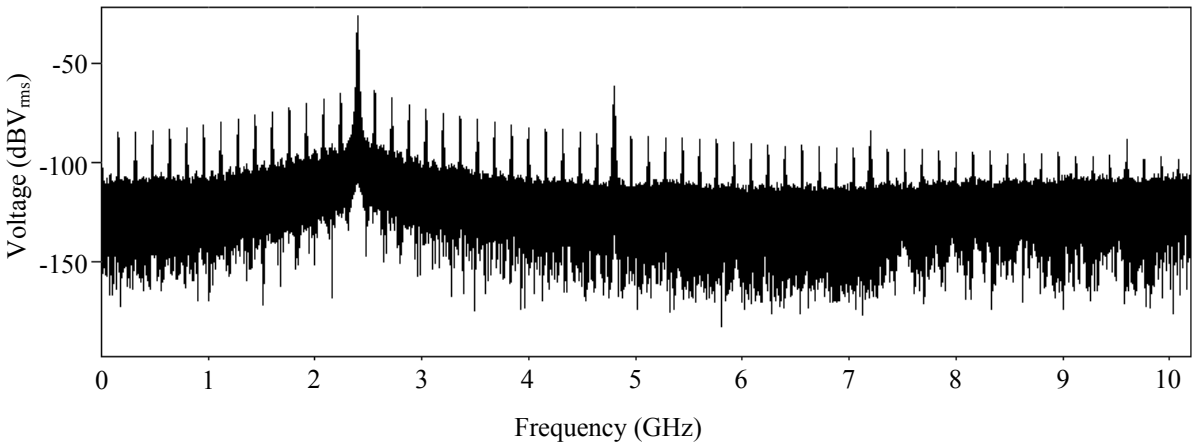


Figure 5.13.

FFT of the transmitted signal used to verify the bandwidth specification. A simulation profile is created with a PRBS data stream and the specified CSS as an input.

The bandwidth is measured between the two -3 dB points observed in Fig. 5.14.

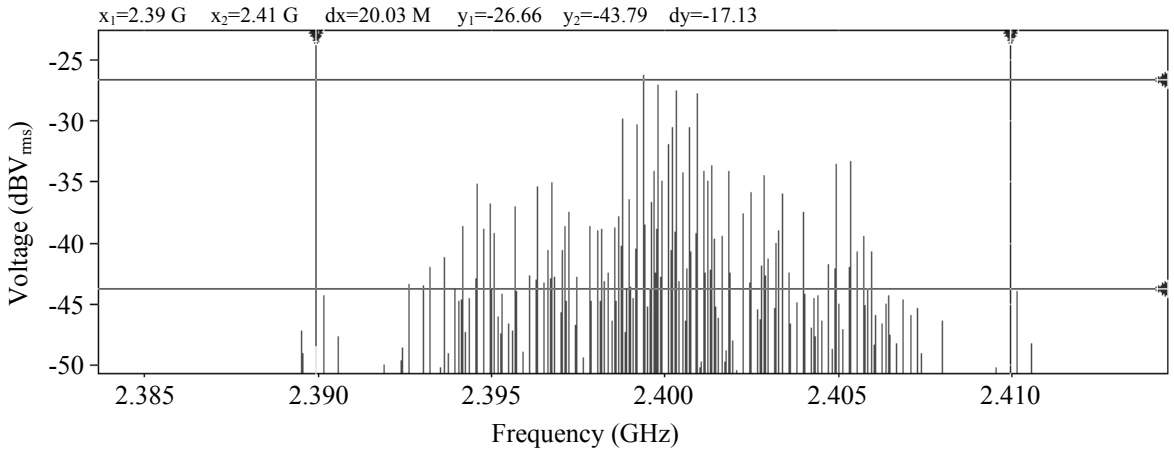


Figure 5.14.

Zoomed-in view of Figure 5.13 to show the transmission bandwidth.

As discussed in Chapter 2, the bandwidth is specified as 20 MHz, as the maximum allowed bandwidth in the 2.5 GHz ISM band is 22 MHz.

5.2.3 Transmitter power

A data rate of 4 Mbits/s and sequence sampling rate of 104 MSamples/s was used again. Figure 5.15 shows the time-domain waveform of the transmitted signal. From the simulation, the peak voltage was approximately 1 V. For a short-time period, the signal can

be approximated by a sinusoidal waveform, justifying the usage of the equation, $V_{RMS} = \frac{V_{PEAK}}{\sqrt{2}}$, to determine the RMS voltage. The maximum transmitted power is estimated to be 2 mW () over the 50 Ω load, or equivalently to be 3 dBm.

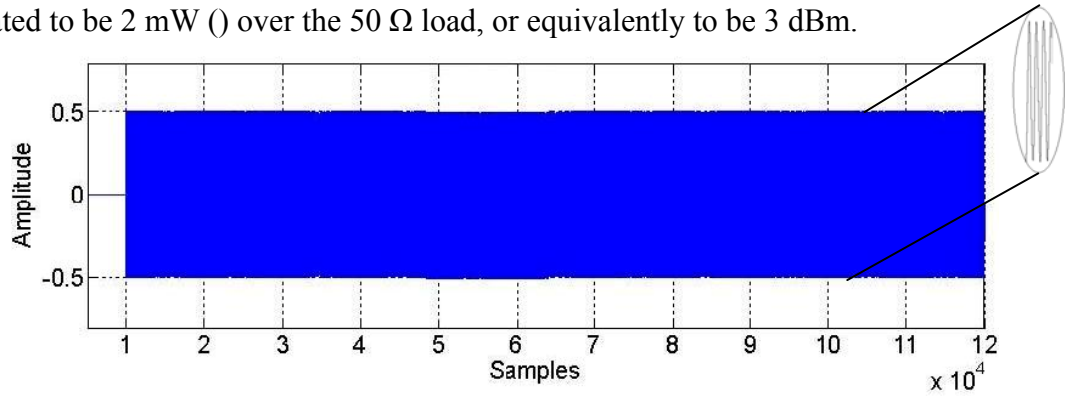


Figure 5.15.

Time-domain simulation of the transmitted signal.

5.2.4 Receiver sensitivity

A receiver's sensitivity is a measure of its ability to discern low level signals. Sensitivity in a receiver is normally taken as the minimum input signal required to produce a specified output signal having a specified signal-to-noise ratio (SNR) and is defined as the minimum signal-to-noise ratio times the mean noise power. Figure 5.16 shows the input signal (to the receiver) with a power of approximately -91 dBm. Figure 5.17 and Figure 5.18 shows the signal after integrate and dump and after comparison, respectively. The integrate and dump waveforms are weak but ramping evidently follows the direction towards the end of bit period.

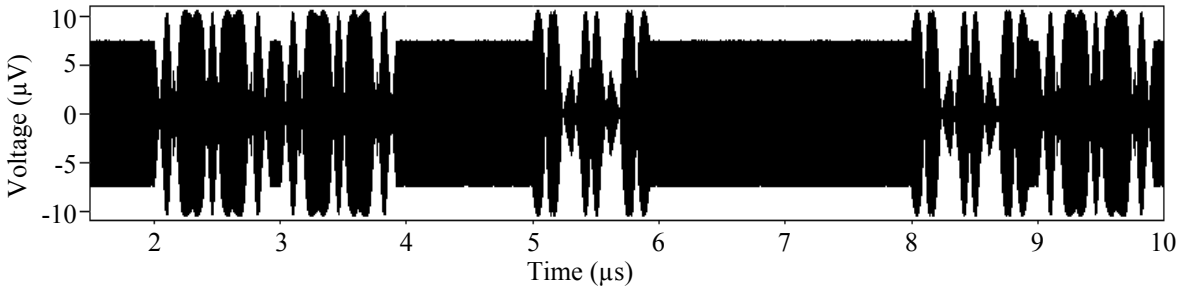


Figure 5.16.

A typical signal of approximate power of -91 dBm.

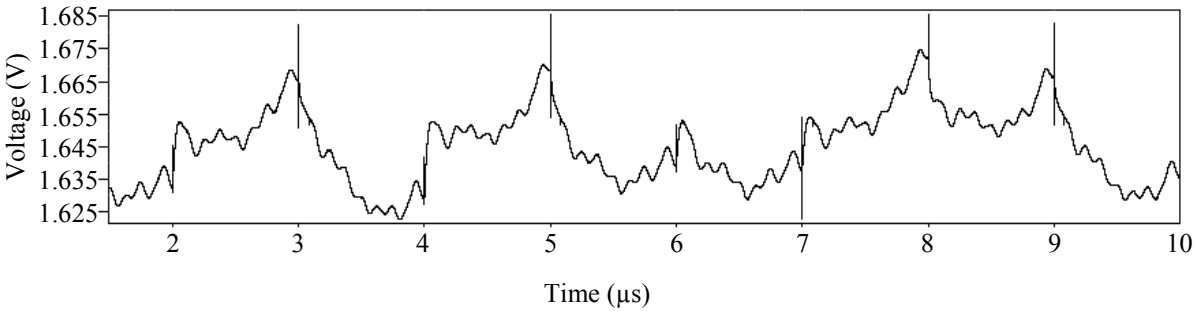


Figure 5.17.

Received signal as processed by the integrate and dump sub-system.

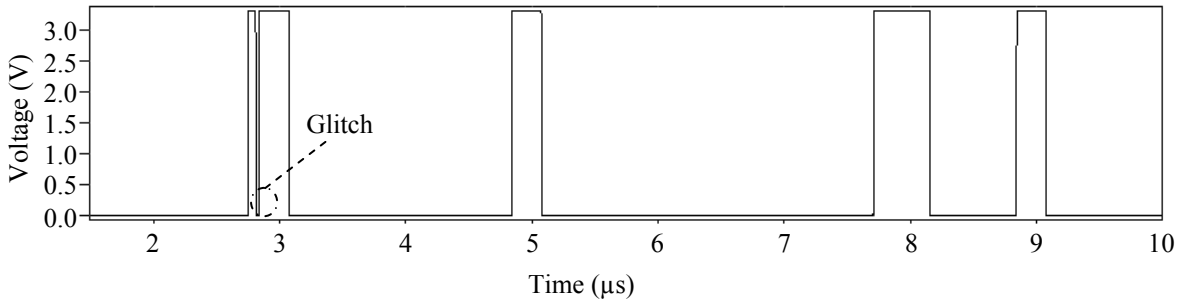


Figure 5.18.

Comparison performed on the integrated signal.

5.2.5 Bit error rate test (BERT)

Bit Error Rate Test is a testing method for digital communication circuits that uses predetermined stress patterns comprising of a sequence of logical ones and zeros. An eye diagram is used to measure the BER. The eye diagram, which is normally displayed on an oscilloscope, is simulated using MATLAB. The eye diagram is generated by repetitively sampling a digital data signal from a receiver and applying this to the vertical input, while the horizontal sweep is triggered by the data rate.

Several system performance measures can be derived by analyzing an eye diagram [37]. If the signals are too long, too short, poorly synchronized with the system clock, too high, too low, too noisy too slow to change, or have too much undershoot or overshoot, this can be observed from the eye diagram. An open eye pattern corresponds to minimal signal distortion. Distortion of the signal waveform due to inter-symbol interference and noise appears as closure of the eye pattern. In summary the following features of the eye-diagram define

1. Eye opening (height, peak to peak): measure of the additive noise in the signal

2. Eye overshoot/undershoot: measure of the peak distortion
3. Eye width: measure of timing synchronization & jitter effects

Figure 5.19 shows the modified eye diagram for the system if no noise or fading is present. Figure 5.20 shows the modified eye diagram if only fading with variance 0.25 and sampling time of 80 ns is specified. Figure 5.21 shows the modified eye diagram if the noise of variance 1 is added and sampled at a default value of 20 ps. Figure 5.22 shows the modified eye diagram of the system when the errors start appearing in the first 100 bits. The variance of noise is experimentally determined to be 25, as fading is kept constant at a variance 0.25 and sampling time of 80 ns. This estimates the BER as 10^{-2} for these parameters in the top branch (Figure 2.17) of the receiver (if there is no error detected in the other three branches of the receiver, the total BER is 1/250). This process could be carried out in a more refined manner if more time and memory was available, however, the technique can be used to determine the BER for any noise and constant fading parameters.

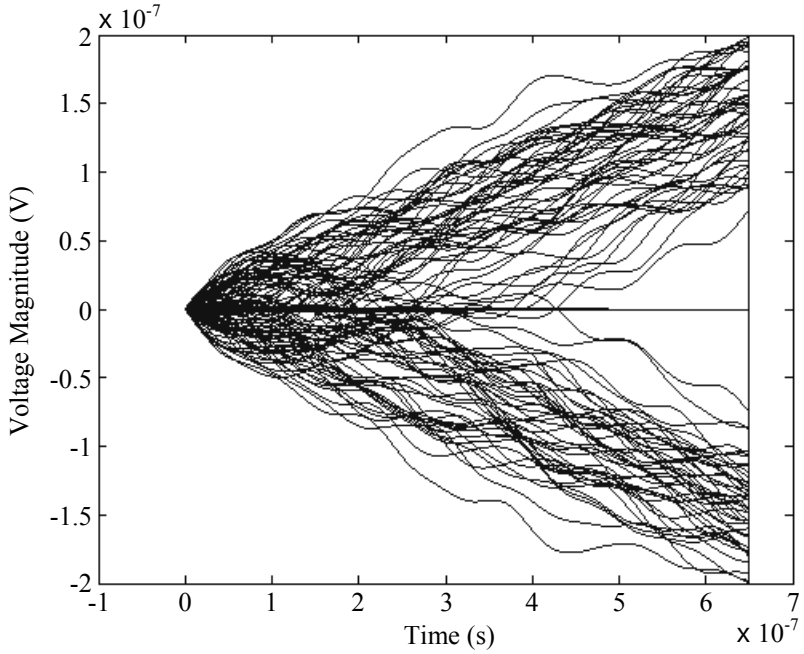


Figure 5.19.

Modified eye diagram of the signal after it is processed by the integrate and dump sub-system if no fading or noise is present in the channel.

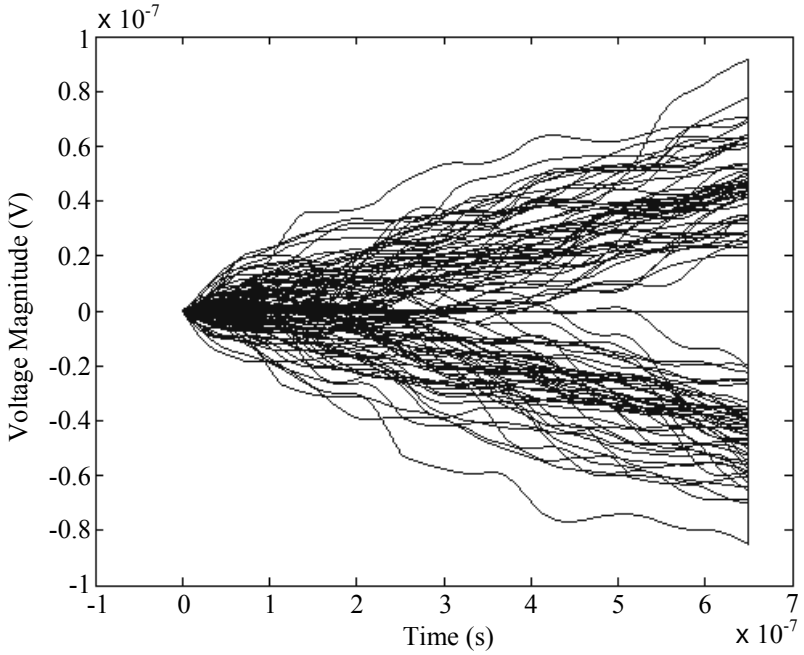


Figure 5.20.

Modified eye diagram of the signal after it is processed by the integrate and dump sub-system if only fading with variance of 0.25 and sampling period of 80 ns is present in the channel.

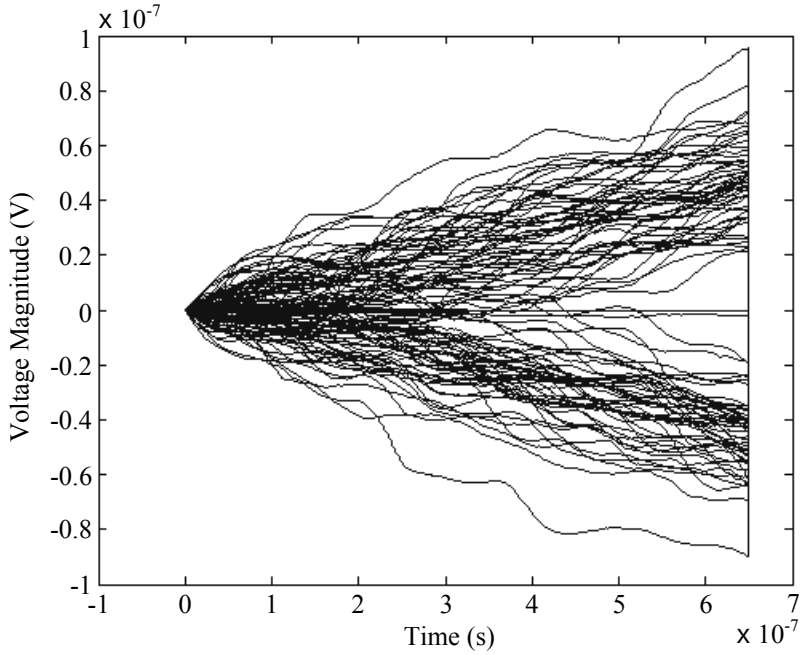


Figure 5.21.

Modified eye diagram of the signal after it is processed by the integrate and dump sub-system if fading with variance 0.25 and sampling time of 80 ns. Noise with a variance of 1 and sampling time of 20 ps are present in the channel.

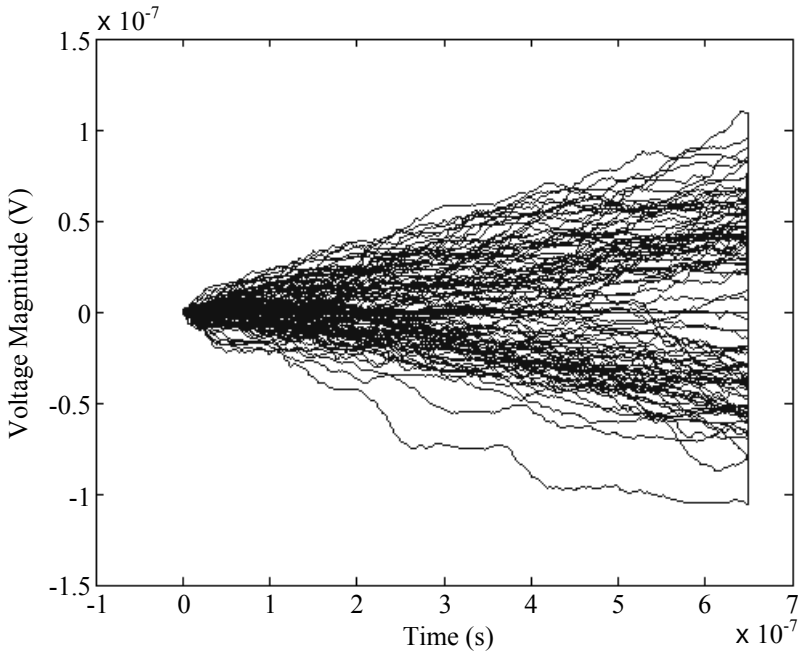


Figure 5.22.

Modified eye diagram of the signal after it is processed by the integrate and dump sub-system if the channel has the properties that just start to influence the performance of the receiver.

5.2.6 CDLL BER

The CDLL is integrated as shown in Figure 2.19. This section summarizes the test procedure used to simulate the BER of the CDLL. For the first part, simulation was setup to determine the BER of the CDLL in the locked state with jitter.

The spreading sequence used was of length 64 CSS and the bit rate was 1 Mbps. The carrier frequency was set to have a mean frequency of 1 GHz and a standard deviation of 5 kHz. The graph generated is half an eye diagram, with the top half representing positive ramps and the lower half negative ramps. Positive ramps represent logic highs and negative ramps represent logic lows. Traces crossing the centre line about 0 result in error bits. The proximity of a ramp to the centre line is an indication of the deviation from the ideal. The bold line around the centre line is caused by MATLAB interpolating between the first and last sample of each bit.

Figure 5.28 shows that no apparent bits are in error. This shows that the CDLL has met the specified BER of 10^{-3} for the simulation period in a mathematical environment. The result

is considered satisfactory, but several factors must be taken into consideration when extrapolating these results to the CMOS CDLL.

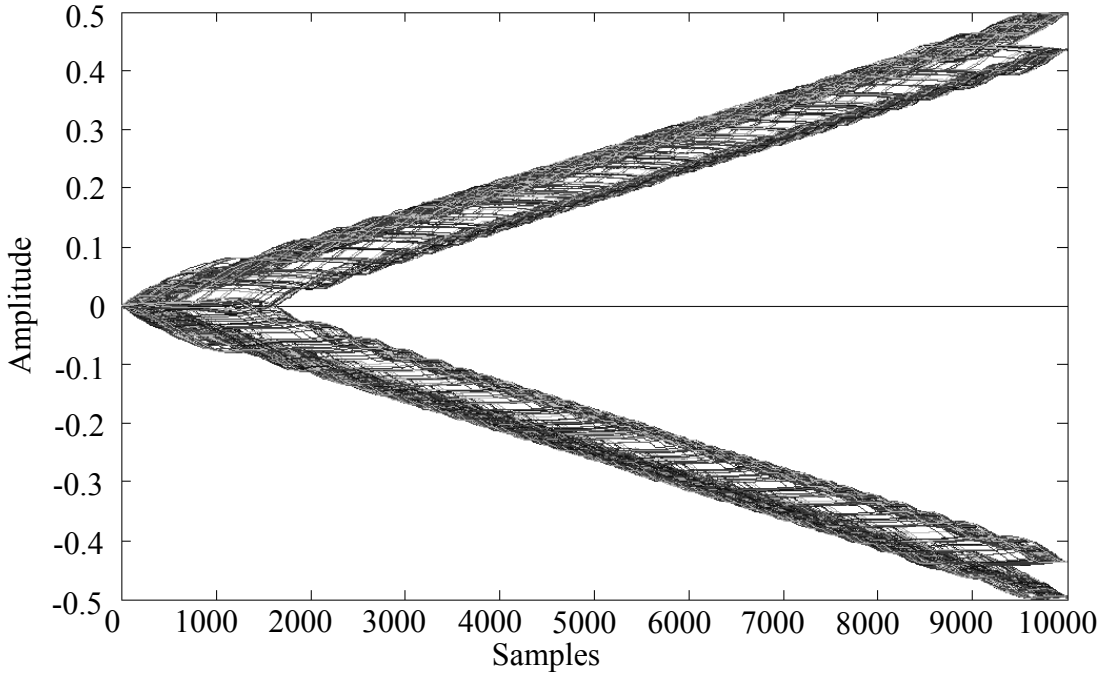


Figure 5.23.
Eye diagram of the recovered data with a noiseless channel.

Figure 5.24 shows the performance of the CDLL operating with a noisy channel, the data is still recovered with no apparent bits in error, this proves the immunity of a DSSS system employing CSS to interference and noise in the channel. It is evident from Figure 5.25 that if the CDLL looses lock, the BER will increase and the bits cannot be recovered since accurate despreading cannot occur. The eye diagram of the CMOS CDLL will tend to show a narrower eye since the integrator of the CDLL is not ideal, which results in a decrease in the ramps ideal gradient, with a tendency to have negative gradients during the early stages of the integration period.

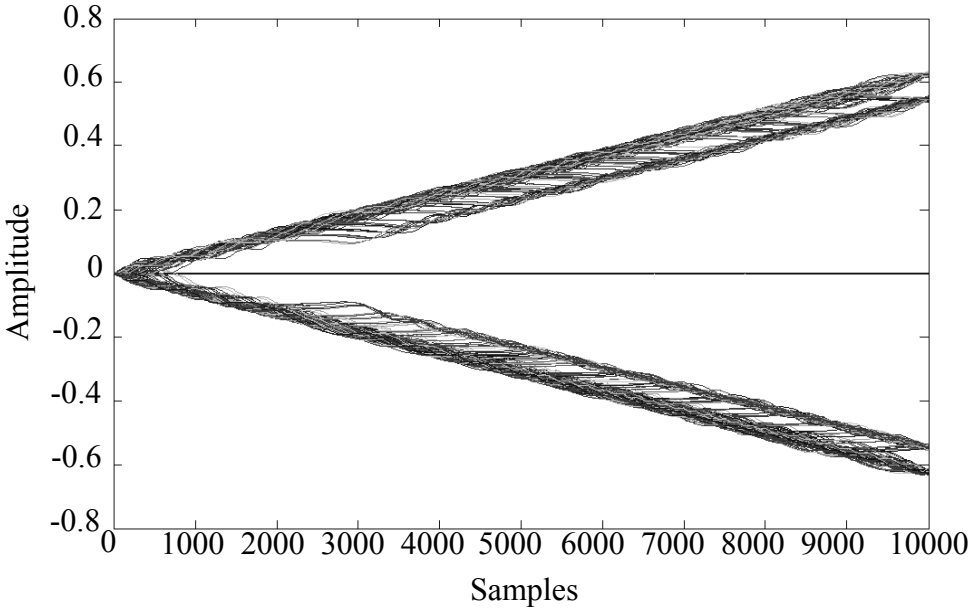


Figure 5.24.

Eye diagram of the recovered data with a noisy channel.

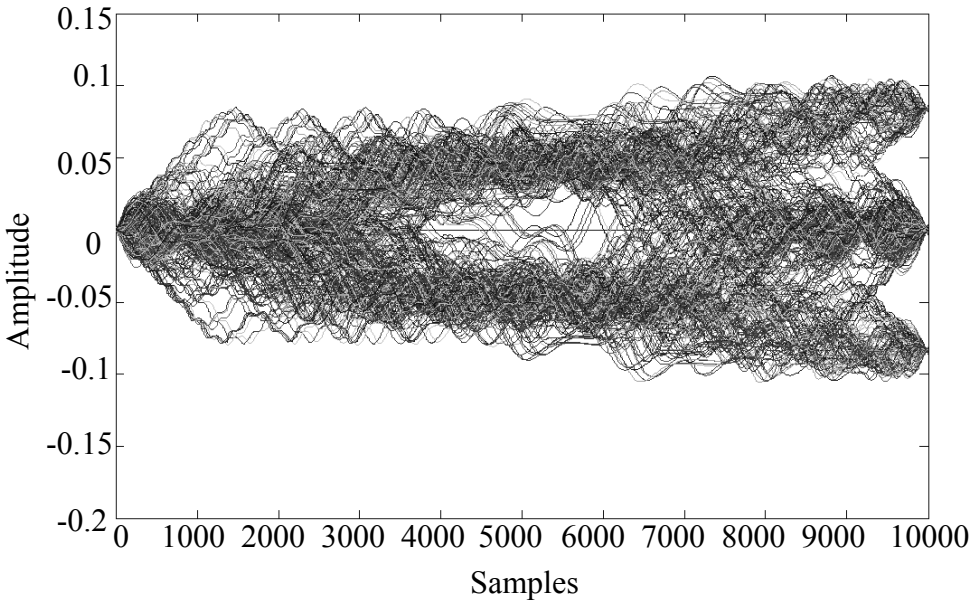


Figure 5.25.

Eye diagram of the recovered data when the CDLL has lost lock [27].

5.2.7 Power dissipation

Figure 5.26 shows the waveform of the total current drawn from the positive power supply and therefore delivered to the rest of the circuit if the IC is actively operating in transmit mode. It is seen that the maximum current is approximately 77 mA, or the power dissipation is about 254 mW.

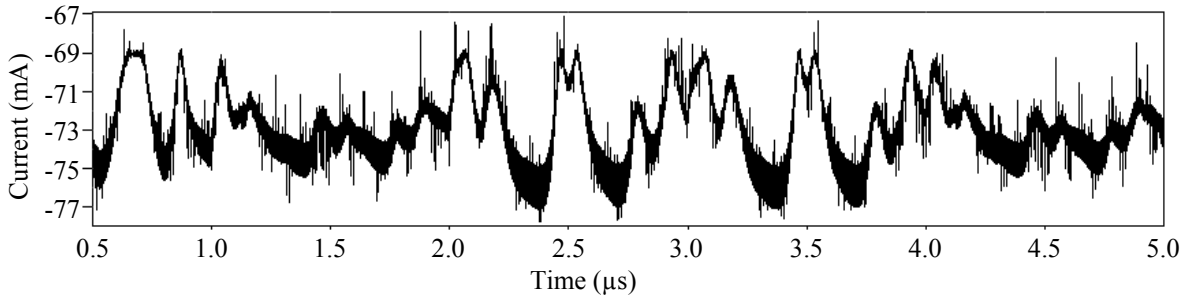


Figure 5.26.

Waveform of the current drawn by the transmitter for a duration of 4.5 µs [71; 72].

Figure 5.27 shows the waveform of the total current drawn from the positive power supply if the IC is operating as a receiver. It is seen that the maximum current drawn is approximately 70 mA, or the power dissipation is about 210 mW.

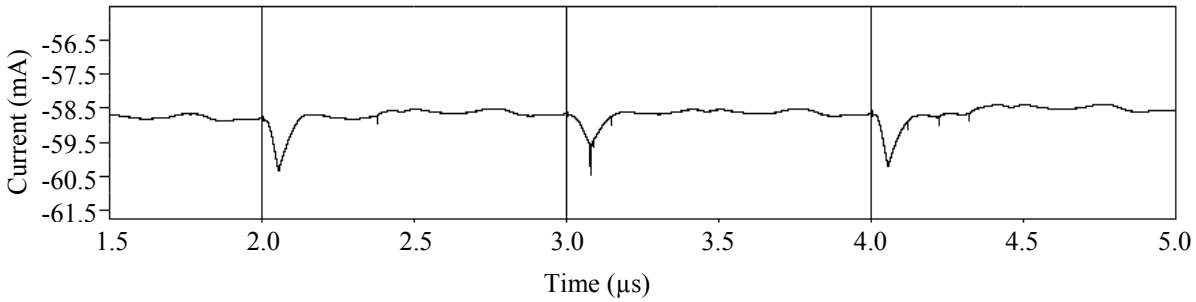


Figure 5.27.

Waveform of the current drawn by the receiver for a duration of 3.5 µs [71; 72].

5.3 Prototyping of design

5.3.1 Design submission to Europractice

The University of Pretoria interfaces with foundries, such as AMS via Europractice. It was the intention of this thesis to submit selected sub-systems for prototyping. To enable effective probing, a large number of test pads are proposed, and individual sub-systems are kept independent of each other (i.e. separate grounds, separate supply rails, etc). The independence also assists in a case where a faulty sub-system does not affect another working sub-system. A design rule check (DRC) and layout versus schematic (LVS) was completed prior to design submission. Due to the large nature of the design of this thesis and research cost/timeline, only selected sub-systems were integrated.

5.3.2 Packaging & test printed circuit board (PCB)

Packaging serves:

- as a bridge between components and the external world,
- as a physical scale translator between component features and the surrounding environment,
- as a product differentiator to keep pace with device requirement in increased performance (functionality/complexity) and reduced cost,
- to offer protection (environmental management of device),
- for providing connectivity and routing (electrical, optical, and material),
- to provide mechanical stress control,
- for thermal management, and
- for testability and burn-in.

Both packaged and naked chips were ordered. A ceramic package was chosen as it can withstand high temperatures and can be hermetically sealed. From a prototyping perspective, the ceramic packages offered by Europractice are also cheaper than plastic packages. A 68-pin ceramic leadless chip carrier (CLCC) was considered sufficient for this design. Such ceramic leadless chip carriers do not have metallic external leads. Additional features of CLCCs include their compact size, their light weight, and their ability to adapt to multiple functions. A typical example is shown in Fig. 5.28.

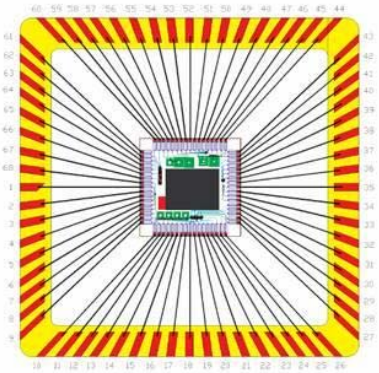
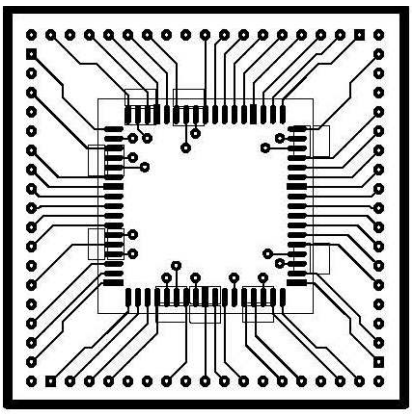


Figure 5.28.
Example bonding diagram for the CLCC-68.

A test-circuit was designed to enable an effective probing of the CLCC-68. This is shown in Figure 5.29.



(a)

Figure 5.29.

Typical PCB that was designed for probing for measurements.

5.3.3 High-frequency equipment and test-bench

A typical measurement setup is shown in Figure 5.30.

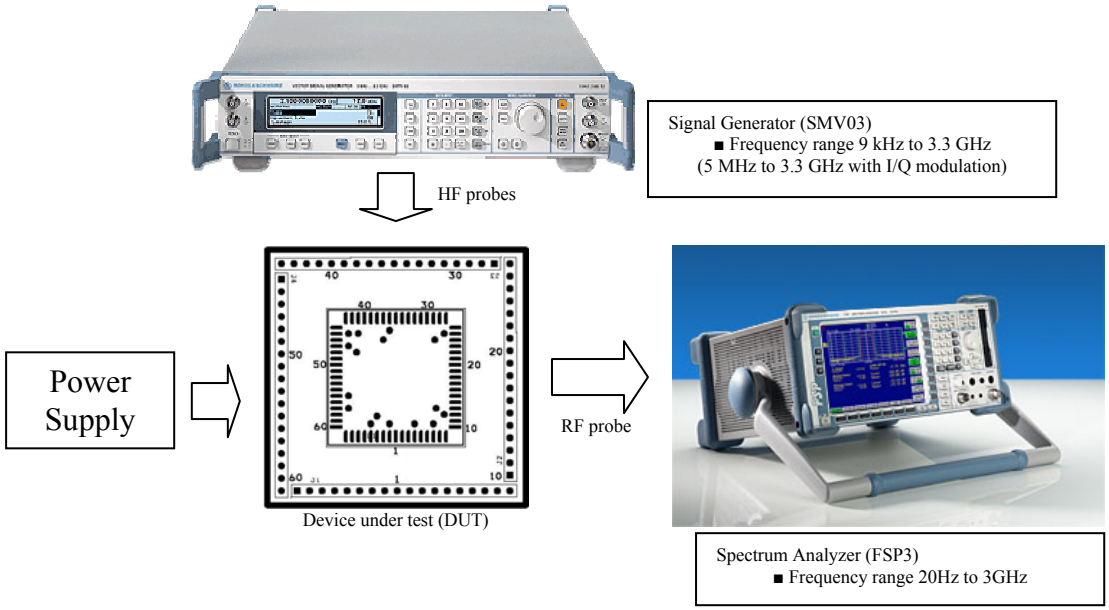


Figure 5.30.

Typical laboratory bench setup (not drawn to scale) for measurements. In case where a VCO is tested, the signal generator[1] is not utilized. The signal generator is further utilized to emulate a received signal (for test purposes) for the LNA, the PA, & the receiver.

The following user manual specifications are important and repeated here. The following specifications should not be exceeded:

• Maximum safe DC input voltage (without 10:1 divider (Fig. 5.31)): ±50 V

• Maximum safe DC input voltage through a 10:1 divider: ±200 V

[1] http://www.rohdeschwarz.com

• Maximum safe RF voltage (without 10:1 divider): 1.5 V peak

• Maximum safe RF voltage through a 10:1 divider: 15 V peak

To minimize the potential for damage, measurements were first taken with the 10:1 divider. The 10:1 divider was only removed when the following conditions are met:

• RF and DC levels were known to be within the above tolerances.

• Higher sensitivity is required than is possible with the 10:1 divider.

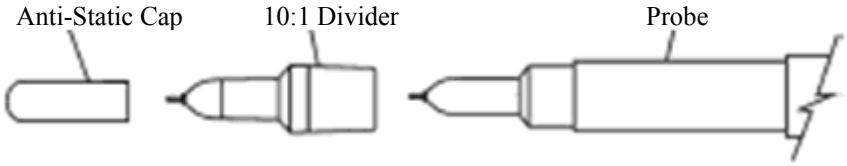


Figure 5.31.

A RF probe including a 10:1 Divider [58].

Electrostatic discharge (ESD) is a serious problem [58]; the following steps were observed:

• The tip of the probe is never touched as the probe microcircuit is susceptible to damage by static discharge.

• A ground strap was worn to eliminate ESD on the body.

• An anti-static bench mat is used to eliminate ESD on the work surface. Caution was observed to use a workbench that was not covered by carpet.

• It was also ensured that ESD is not introduced to the DUT while the probe is being used as the static charge could damage the DUT as well as the probe.

5.4 Practical measurements

Fig. 5.32 shows the output of the VCO.

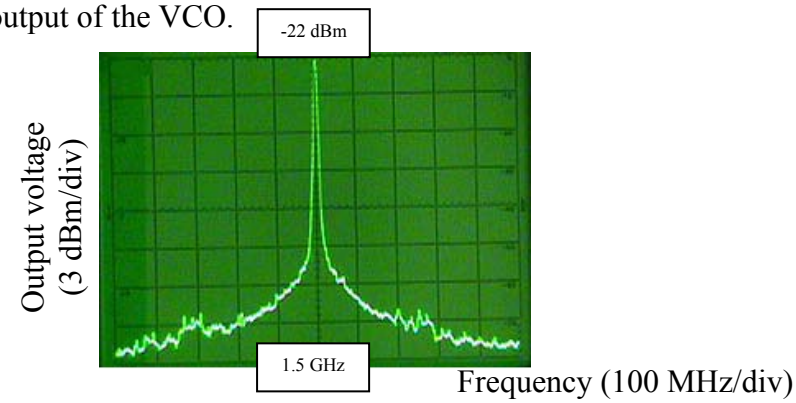


Figure 5.32.

A frequency sweep around 1.5 GHz (the test oscillator).

By changing the dc voltage to the VCO, the frequency/voltage gain, K_{VCO} was obtained (Fig. 5.33). K_{VCO} compares well to a value of about 0.25 GHz/V obtained in simulation. The phase noise of the VCO is shown in Fig. 5.34.

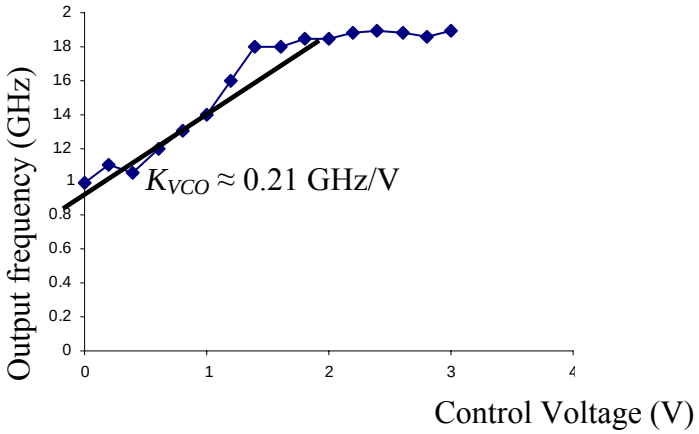


Figure 5.33.

Plot of the output frequency against the input voltage.

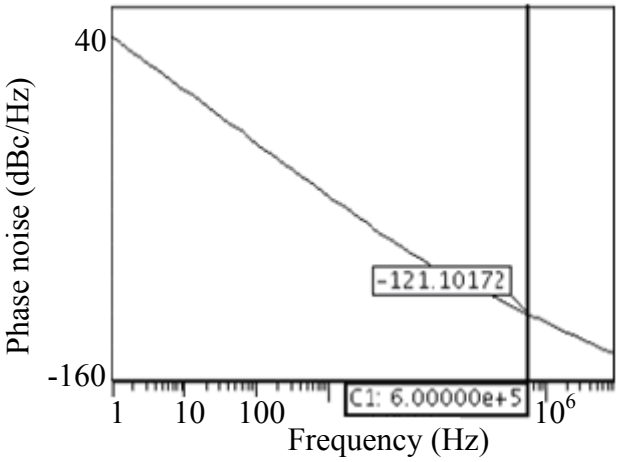


Figure 5.34.

VCO phase noise of -121 dBc/Hz at an offset of 1 MHz.

Analogous to the simulation of Fig. 3.23, a measurement is performed to determine the intercept points of the mixer – this is shown in Fig. 5.35.

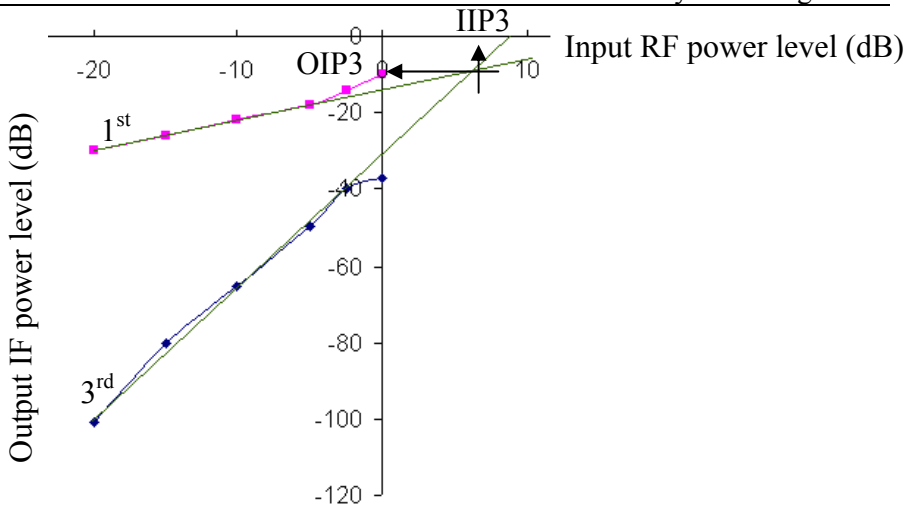


Figure 5.35.

Plot of first and third harmonic outputs of the mixer.

An OIP3 of -10 dBm & IIP3 of 7 dBm is obtained.

Since a hardware system to generate CSS was outside the scope of this thesis, a PN sequence and a GOLD sequence was used to test the multiplier and the summation performed (top branch of the transmitter). The VCO designed for the thesis also served as the local oscillator (see Fig. 2.17). The results are shown in Figures 5.36-5.37. The results are similar to the results of Chapter 2, except that the amplitudes were generally reduced (since frequency is the parameter of interest for these specific sub-systems, the reduced amplitudes did not pose a major problem). Only selected results (as per measurement points on the transmitter branch) are repeated in this section.

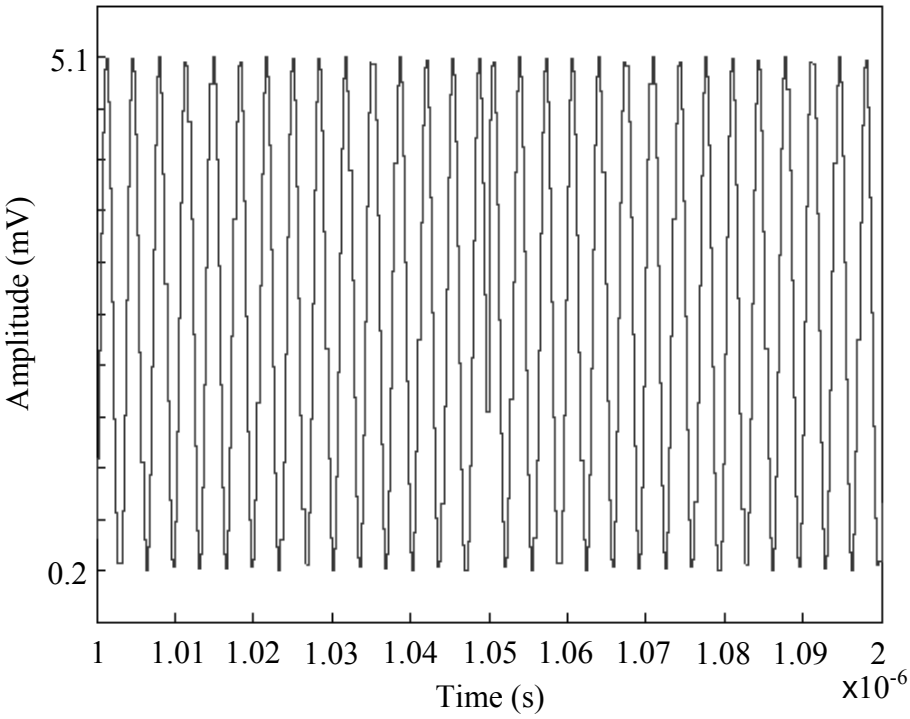


Figure 5.36.

Modulated data signal.

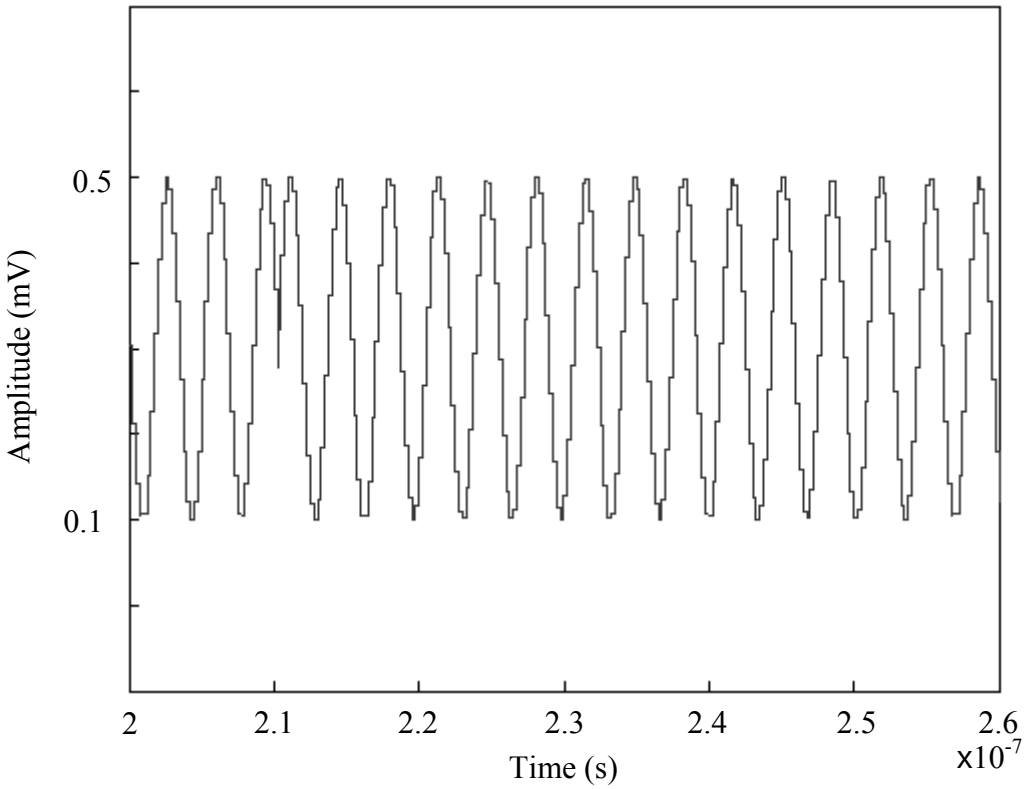


Figure 5.37.

A portion of the signal, after the summation sub-system.

Using the same sequences as for the transmitter, measurements were performed to test the despreading sub-system (Fig. 2.17). The result is shown in Fig. 5.38.

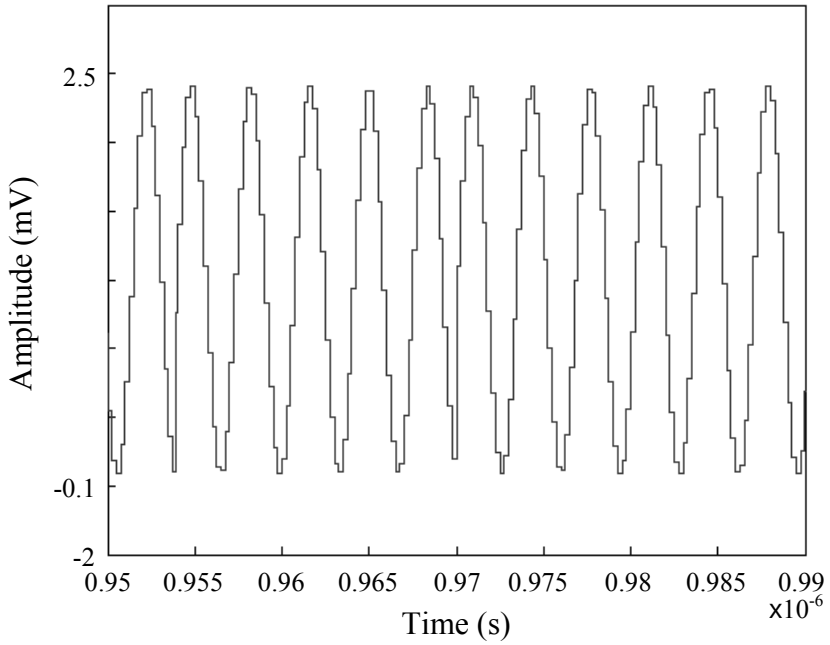


Figure 5.38.

Despread signal.

The despread signal of Fig. 5.38 is then demodulated using the same carrier frequency as that which was used at the transmitter. The resulting signal is shown in Fig. 5.39. This

signal resembles the data signal, but has a high frequency component that can be filtered out.

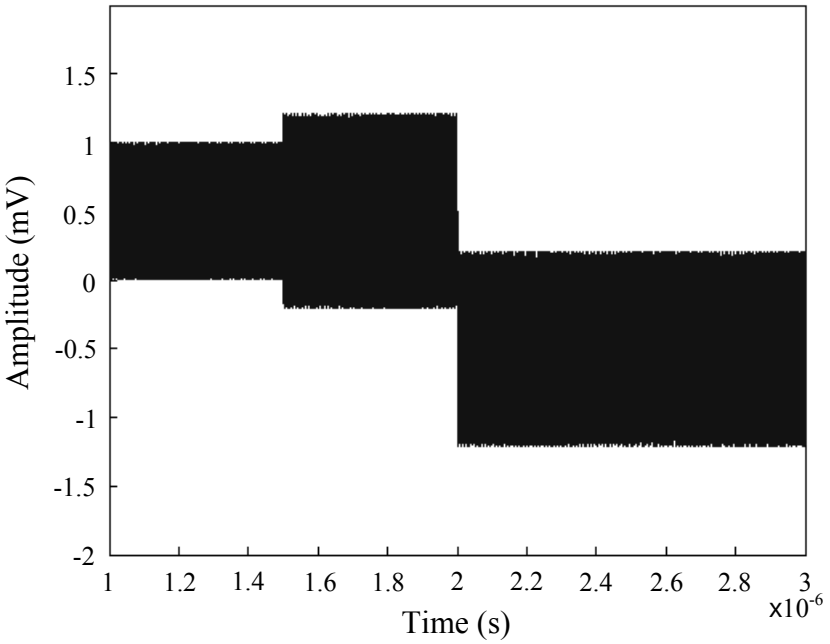


Figure 5.39.

Recovered, unfiltered signal.

The reduced amplitudes are expected and can be attributed to gain variations in CMOS sub-systems but also due to impedance matching differences (probe & scope).

CHAPTER 6: CONCLUSION

This chapter summarizes the research contributions of this thesis as well as provides some ideas for future research.

6.1 Technical summary and contribution

DSSS systems are SS systems where spreading is achieved by direct modulation of a data modulated carrier by a wideband spreading signal or code. The spreading signal is chosen to facilitate demodulation at the intended receiver and to make demodulation as difficult as possible for an unintended receiver [59]. The information signal *d(t)* is spread by the complex spreading sequence *c(t)* and then modulated on a carrier resulting in the final spread output [11]:

$$s(t) = d(t) \times c(t) \times \cos(2\pi f_{RF} t) \tag{6.1}$$

In code division multiple access (CDMA), the capacity is dependent on the amount of multi-user interference (MUI) that is present. During the despreading process in the receiver, both auto-correlation (AC) and cross-correlation (CC) functions are performed. The CC value is not necessarily zero, and therefore the spreading sequences of other users generate noise in the process of signal detection. CSS have optimal AC and CC values, and therefore result in minimum MUI [11]. The CSS used for this thesis are band limited and are constant envelope spreading sequences; this allows optimum power usage and longer battery life.

QPSK is used as the modulation scheme. The main reason for transmitting simultaneously on two carriers which are in quadrature is to conserve spectrum [59]. Spectrum is conserved since for the same total power the same bit error rate (BER) can be achieved using only half the power.

Several DSSS transceivers exist, however, patent [8] is a relatively recent filing, and to date the patent has been developed using a field programmable gate array (FPGA) and supporting discrete components only. A custom-chip design for such a transceiver is a complex art, and this thesis is a first attempt, to the knowledge of the filers of the patent [8], towards an on-chip implementation. To enable effective design, the relationship of a sub-system to the integrated system was conceptualized and tested mathematically using

SIMULINK/MATLAB. Some of the sub-systems had to be developed by first principles & others were designed by referral to extensive research [1-58] conducted elsewhere – the following sub-sections highlights some of the achievements [66; 69-70].

Biasing network design

The voltage references constitute the foundation of many of the sub-systems, thus their ability to remain constant is crucial to reliable operation in varying conditions. As expected, the threshold voltage, ΔV_{TH}, decreases for the NMOS transistor and increases for the PMOS transistor with increasing temperature. As seen in Figures 3.9 and 3.10, the bias circuit implemented shows limited deviation in reference voltages and currents from their values at room temperature.

Amplifier design

A telescopic amplifier was designed to achieve a unity gain bandwidth of just over 1 GHz and gain of about 65 dB. The choice of the amplifier was attributed to improved speed, better noise performance and low power consumption.

Mixer

A mixer with a conversion gain of about 10 dB and NF of about 15 dB was designed. The OIP3 and IIP3 were 7 dBm and 16.5 dBm respectively, proving sufficient for the system of this thesis.

LNA

The LNA used a source degenerated topology with which a minimum NF can be obtained. The core amplifier was realized using a differential topology. This topology has the advantage of rejecting common-mode noise components in a signal. The differential amplifier was realized by a transconductance amplifier, which drives a transresistance amplifier connected in a cascode topology. Due to the fact that the cascode topology was used, the high frequency response of the amplifier was enhanced.

Active inductor design & VCO

The current recycling method of the VCO design allows the system to be functional as a linearly adjustable oscillator. With an active inductor, the quality factor (and resulting VCO phase noise) can be improved. Inductor Q-factors as high as 50 (relatively higher than passive spiral inductor counterparts) can be obtained.

Comparator

A conventional two-stage comparator was designed. A modification (connecting the body of the transistors to the source) allowed the transistors to be more sensitive to changes at the gate inputs. For a load capacitor of 10 pF, a slew rate of 1000 V/μs was achieved.

Phase detector

The phase detector is an important part of the DDC-CRL. Figure 6.1 shows the phase detector output in the ideal case of an instantaneous response to a frequency error. Dashed lines indicate the phase detector output in the absence of phase inversion.

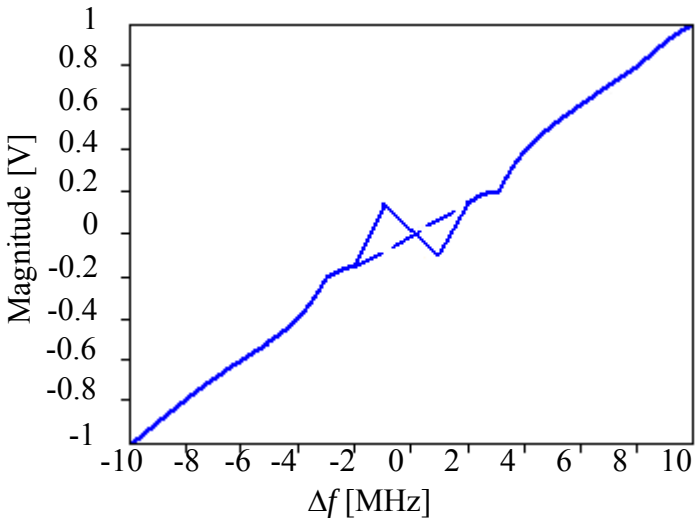


Figure 6.1.
Instantaneous response of phase detector with the effects of phase inversion shown in dashed lines.

Figure 6.2 is the simulated phase detector output of the DDC-CRL as a function of frequency deviation, dashed lines indicate the output in the absence of phase inversion.

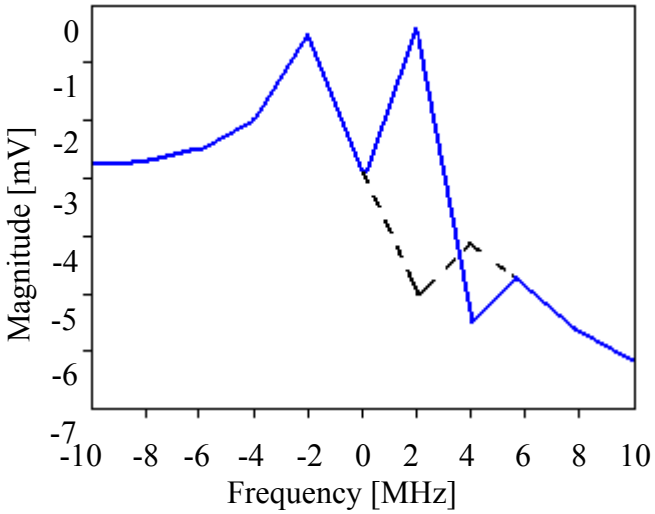


Figure 6.2.
Actual response of the DDC-CRL phase detector to a frequency error. Dashed lines indicate response without phase inversion.

Fig. 6.1 shows the phase detector output as a function of frequency deviation from ideal if the error signal is determined within one bit period. The change in polarity at 1 MHz is the phase detector's response to phase inversion. The dashed line indicates the output for no inversion. Phase inversion occurs when the difference term after demodulation causes the bit stream to invert, this inversion occurs in both branches. This causes the output of the phase detector to have correct magnitude, but incorrect polarity. Phase inversion in effect reverses the roles performed by each branch. Phase inversion is reduced by encoding the data using Manchester encoding, which has a DC average of approximately 0 V. The specification for the operating range of the DDC-CRL does not account for phase inversion, which will cause the loop to momentarily loose lock. Phase inversion can be forced to occur, as in Fig. 6.1 by allowing the difference term to be synchronized with the zero crossings of the bit stream, but also occurs for random bit streams as in Fig. 6.2.

The output characteristic of Fig. 6.1 is most desirable (without phase inversion) but is not achievable because the LPF settling time is several microseconds. The phase detector responds more readily to negative changes in frequency.

Similarly, Fig. 6.2 shows the simulated output of the phase detector once the DDC-CRL has stabilized to a step change in frequency. The simulation was conducted once the output of the LPF had settled to approximately DC after 8 μs. The dashed line represents the output if no phase inversion is present. In both cases, the phase detector is able to produce an error signal of correct polarity to drive the VCO's operating frequency towards the received signals frequency over a range of ±10 MHz, meeting the tracking range requirements of the DDC-CRL. The control voltage range is less than 300 mV.

The simulation of Figure 6.2 was performed with only frequency and not phase differences. The dashed line in Fig. 6.1 is plotted by inverting the output at 1 MHz difference. The dashed line in Fig. 6.2 is plotted using simulation results obtained by using a new random bit sequence in the model transmitter.

The larger apparent tracking range is caused by the non-linear relationship between the resonate frequency of the VCO's LC tank and the capacitive load used to control the resonate frequency. The relationship is approximately linear in the region of interest (2.39 GHz to 2.41 GHz), as this is the region in which the varactor behaves linearly to the control voltage. Outside this region, the varactor value saturates regardless of increased magnitude of the control voltage. This saturation level is used to limit the range of the VCO, but is too high to limit the VCO to within the desired range. Use of a smaller varactor with narrower tuning range is not possible, as the device model used is not valid for varactors smaller than the one currently in use.

Power Amplifier

A class F PA has been designed to achieve a gain of 25 dB (the gain was reduced to above 10 dB for this thesis). With the class F design, a PAE of about 80 % and a low THD was achieved. The class F amplifier design also required a negative voltage rail, this was designed using a ring oscillator, rectifier, filter and a voltage regulator.

Digital sub-systems

Several digital sub-systems were designed from first principles (albeit that they are conventional circuits). Some design simplification was done, for instance the D-Type FF was implemented using switches and inverters. Similarly, clock recovery was implemented

with edge detection and a counter (it was assumed that an external clock is available for the counter).

6.2 Future research work

While this thesis has laid a foundation for further integration of the DSSS modem, several iterations can be done to improve the overall design:

1. generation or storage of CSS on-chip (particularly longer sequences),
2. investigate the usage of alternative (different geometries) spiral inductors to achieve an enhanced Q-factor for the PA,
3. each sub-system could be independently and further optimised,
4. reduce the number of mixers to reduce the power dissipation,
5. conduct Monte-Carlo analysis for a deeper understanding of process variations, and impact thereof on the overall system, and
6. consideration of a different floor-plan and an electromagnetic analysis, for instance, laying out oscillators that are out-of-phase next to each other to achieve better common mode rejection.

REFERENCES

[1] Russe, S.F., 2001. Wireless Network Security for Users, *Proceedings: International Conference on Information Technology: Coding and Computing*, Las Vegas, 2-4 April, p. 172.

[2] Ito, A. and Habuchi, H., 2000. *IEEE Proceedings: Sixth International Symposium on Spread Spectrum Techniques and Applications,* 6-8 September, Parsippany.

[3] Brodsky, W., 1987. Digital communications and spread spectrum systems. *IEEE Communications Magazine,* Vol. 25, No. 9, pp. 62-63.

[4] Jung, P., Baier, P.W., and Steil, A., 1993. Advantages of CDMA and spread spectrum techniques over FDMA and TDMA in cellular mobile radio applications. *IEEE Transactions on Vehicular Technology*, Vol. 42, No. 3, pp. 357-364.

[5] Kohno, R., Meidan, R., and Milstein, L.B., 1995. Spread spectrum access methods for wireless communications. *IEEE Communications Magazine,* Vol. 33, No.1, pp. 58-67.

[6] Glas, J.P.F., and Skolnik, S.E., 1994. Fourier transform based DS/FH spread spectrum receiver. *IEEE Proceedings: International Conference on Computer Design: VLSI in Computers and Processors*, 10-12 Oct., Cambridge, pp. 420-423.

[7] Tranter, W.H., Rappaport, T.S., Woerner, B.D., and Reed, J.H., 1999. Wireless Personal Communications Emerging Technologies for Enhanced Communications, Norwell: Kluwer Academic Publishers.

[8] Linde, L.P., and Marx, F.E., 2004. Multi-dimensional spread spectrum modem. *USA complete patent no. 6,744,807 B1*. Date of Patent: 2004-06-01.

[9] Fan, P.Z., and Darnell, M., 1996. Sequence Design for Communications Applications, Research Studies Press (RSP), London: Wiley & Sons.

[10] Peng, D. and Fan, P.Z., 2001. Sequence Design and Applications for CDMA Systems, Chengdu: Southwest Jiaotong University Press.

[11] Marx, F.E., 2005. Masters dissertation: DSSS communication link employing complex spreading sequences. Faculty of Engineering, Built Environment & Information Technology, University of Pretoria, South Africa.

[12] Marx, F.E. and Linde, L.P., 1996. Theoretical analysis and practical implementation of a balanced DSSS transmitter and receiver employing complex spreading sequences. *IEEE Proceedings: Africon 1996,* Vol. 1, 24-27 Sept., Stellenbosch, pp. 402-407.

[13] Meng, T.H. McFarland, B., Su, D., and Thomson, J. 2003. Design and implementation of an all-CMOS 802.11a wireless LAN chipset. *IEEE Communications Magazine.* Vol. 41, No. 8, pp. 160-168.

[14] Razavi, B., 1999. CMOS technology characterization for analog and RF design. *IEEE Journal of Solid-State Circuits*, Vol. 33, No.3, pp. 268-276.

[15] Stallings, W., 2001. Spread Spectrum. In: W. Stallings, *Wireless Communications and Networks*. Upper Saddle River: Prentice Hall, 2002, pp 167-196.

[16] Proakis, J.G and M. Salehi, 2002. *Communication systems engineering*. 2nd ed. Upper Saddle River: Prentice-Hall, pp 729-734.

[17] Kevenaar, T.A.M. and ter Maten, E.J.W., 1999. RF IC simulation: state-of-the-art and future trends. *IEEE Proceedings: International Conference on Simulation of Semiconductor Processes and Devices, 1999.* 6-8 Sept., Kyoto, pp. 7-10.

[18] Boyce, D.E. and Baker, R.J., 1997. A complete layout system for the PC. *Proceedings: 40th Midwest Symposium on Circuits and Systems*, 3-6 Aug., Sacramento, pp. 1091-1094.

[19] Schweber, B., 1996. Choices and confusion spread wider as spread spectrum goes mainstream, EDN, 10 Oct., New York, 79-87.

[20] Popović, B.M., 1992. "Generalized chirp-like polyphase sequences with optimum correlation properties," *IEEE Transactions on Information Theory*, Vol. 38, No. 4, pp. 1406-1409.

[21] Telecommunications Industry Association, 2001. *TIA/EIA-98-D (Revision of TIA/EIA-98-C) Recommended minimum performance standards for CDMA2000 spread spectrum mobile stations*, pp 3-5.

[22] Marx, F.E. and Linde, L.P., 1995. DSP implementation of a generic DSSS transmitter employing complex or binary spreading sequences. *IEEE Proceedings: Conference on Communications and Signal Processing*, 16 Nov., Pretoria, pp. 75-80.

[23] Marx, F.E. and Linde, L.P., 1998. A combined coherent carrier recovery and decision-directed delay-lock-loop scheme for DS/SSMA communication systems employing complex spreading sequences. *Transactions of the SAIEE - Special Issue: CDMA Technology - Changing the face of wireless access*, Vol. 89, No. 3, pp. 131-139.

[24] Marx, F.E. and Linde, L.P., 1999. A four dimensional modem employing complex spreading sequences. *IEEE Proceedings: Africon 1999.* 28 Sept.-01 Oct., Cape Town, pp. 221-226.

[25] Ramiah, H.; and Zulkifli, T.Z.A. 2004. Design of Tunable CMOS Up-Conversion Mixer for RF Integrated Circuit. *IEEE Proceedings: Tencon 2004*. Vol. 4, 21-24 Nov., Chiang Mai, pp. 352 - 355.

[26] Lahti, M., [19 May 2005]. IEEE 802.11 Wireless LAN [online]. Available from http://www.tml.tkk.fi/Opinnot/Tik-110.551/2000/papers/IEEE_802/wlan.html [Accessed: March 2007].

[27] T.S. Elenjical, 2007. Final year project (EPR400) report: Design of a CMOS based complex delay-lock loop (CDLL) synchronization scheme. Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa. (Study Leader: Saurabh Sinha & Prof. L.P. Linde).

[28] Austriamicrosystems, 1999. 0.35 µm CMOS process parameters (9933016), pp. 1-55.

[29] B Razavi, 1998. *RF microelectronics*, Upper Saddle River: Prentice Hall, p. 248, pp. 88-149.

[30] Baker, R, 2005. *CMOS Circuit Design, Layout and Simulation.* 2nd Ed. London: Wiley-IEEE Press.

[31] Razavi B., 2001. *Design of CMOS Analog Integrated Circuits*. Boston : McGraw-Hill.

[32] Bian, C., Liu, Z., Wang Z., and Zhang, C. 2005. Full custom design of a two-stage fully differential CMOS amplifier with high unity-gain bandwidth and large dynamic range at output. *IEEE Proceedings: Midwest Symposium on circuits and systems.* 7-10 Aug., Cincinnati, Vol.2, pp. 984-987.

[33] Banerjee, S., Chatterjee, A., 2005. A 160 MS/s 8-bit Pipeline-based ADC. *Proceedings: International conference on VLSI design* (VLSID '05), 3-7 Jan., Kolkata, [No page numbers].

[34] Bae, H-H., Cho,Y-J., Lee M-J., Kim, M-J., Lee S-H., and Kim, Y-L. 2004. An 8b 220 MS/s 0.25 /spl mu/m CMOS pipeline ADC with on-chip RC-filter based voltage references. *IEEE Proceedings: Advanced System Integrated Circuits*. 4-5 Aug., Fukuoka, pp. 90 – 93.

[35] Peach, C.T.; Ravi, A.; Bishop, R.; Soumyanath, K.; and Allstot, D.J. 2005. A 9-b 400 Msample/s pipelined ADC in 90nm CMOS. *Proceedings: European Solid State Circuits Conference*, 12-16 Sept., Grenoble.

[36] Bilotti, A., 1968. Applications of a Monolithic Analog Multiplier, *IEEE Journal of Solid-State Circuits*, Vol. 3, No. 4, pp. 373-380.

[37] Proakis, J.G. and Salehi, M., 2004. *Fundamentals of Communication Systems.* Upper Saddle River: Prentice Hall.

[38] Dabrowski, J. and Bayon, J.G., 2004. Mixed Loopback BiST for RF Digital Transceivers**.** *IEEE Proceedings: International Symposium on Defect and Fault Tolerance in VLSI Systems***,** 11-13 Oct., pp. 295-302.

[39] Nguyen, T.K., et. al. 2004. CMOS low-noise amplifier design optimisation techniques*. IEEE Transactions on Microwave Theory and Techniques,* Vol. 52, No. 5, pp. 1433 – 1442.

[40] Bosco, H.L., 2002, *VLSI for wireless communication.* 1st ed., Upper Saddle River: Prentice Hall.

[41] Jaeger, R.C., Blalock, T. N, 2003. *Microelectronic Circuit Design*. International ed., pp 128-129, 325-326, 374-375, 1027-1028, Hightstown: McGraw-Hill.

[42] Wu, Y., Ismail, M., and Olsson H., 2000. A Novel CMOS fully differential inductorless RF bandpass filter, *IEEE Proceedings: International Symposium on Circuits and Systems*. 28-31 May, Geneva.

[43] Tang, C., Lu, W., Van, L., Feng, W. and Liu, S., 2001, *A 2.4 GHz CMOS Down-Conversion Doubly Balanced Mixer with Low Supply Voltage,* Taipei, Taiwan, National Taiwan University.

[44] Lin, T.Y.K. and Payne, A.J., 2000. Design of a Low-Voltage, Low-Power, Wide-Tuning Integrated Oscillator. *IEEE Proceedings: International Symposium on Circuits and Systems (ISCAS),* May 28-31, Geneva.

[45] Franco, S., 2002. *Design with Operational Amplifiers and Analog Integrated Circuits.* 3rd ed. New York: McGraw-Hill.

[46] Allen, E.A. and Holberg, D.R., 1987. *CMOS Analogue circuit design.* 1st ed. New York: Holt, Rinehart and Winston, pp. 310-365.

[47] Stenman, A.K. and Sundtström, L., 1999. Extended analysis of input impedance control of an NMOS-transistor with and inductive series feedback. *IEEE Proceedings: International Conference on Electronics, Circuits and Systems*, Sept. 5-8, Paphos.

[48] Venkataramani, M., 2004. *Efficiency improvement of WCDMA base station transmitter using class F power amplifiers* (Master thesis). Virginia: Polytechmic Institute and State University.

[49] Raab, F.H., 2001. Maximum efficiency and output of class-F power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, Vol. 49, No. 6, pp. 1162-1166.

[50] Colantonio, P., Giannini F., Leuzzi G., and Limiti, E., 1999. On the class-F power amplifier design. *International Journal of RF and Microwave Computer-Aided Engineering*, Vol. 9, No. 2, pp. 129-149.

[51] Colantonio, P, Giannini, P., Limiti, E., and Leuzzi, G., 1999. High Efficiency Low Voltage Power Amplifier Design by Second Harmonic Manipulation. *International Journal of RF and Microwave Computer-Aided Engineering*, Vol. 9, No. 4, 1999, pp. 33-46.

[52] Lee, T.H., 2004. *The design of CMOS radio-frequency integrated circuits*. 2nd ed. Cambridge: University of Cambridge.

[53] Gonzalez, G., 1997. *Microwave transistor amplifiers: Analysis and design*. 2nd ed. Upper Saddle River: Prentice-Hall.

[54] Wakerly J.F., 2001, *Digital Design - Principles & Practices*, 3rd edition, Upper Saddle River: Prentice Hall.

[55] Sedra, A.S., and Smith, K.C., 1998. *Microelectronic Circuits.* 4th ed. New York: Oxford University Press.

[56] J.G.D. Meyer, 2005. Tunable CMOS RF active mixer with adjustable lowpass filter IC. Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa (Study Leader: Johan Schoeman).

[57] Gray, P.R., Meyer, R.G., Hurst, P.J., and Lewis, S.H., 2001. *Analysis and Design of Analog Integrated Circuits*. 4th ed. London: Wiley & Sons.

[58] Agilent Technologies, 2000. *Agilent Technologies 85024A (High Frequency Probe)*. Agilent part number 85024-90001, USA.

[59] Ziemer, R.E. and Peterson, L.P., 1985. *Digital communications and spread spectrum systems*. New York: McMillan publishing company, pp. 327-347, pp. 419-480.

[60] Elenjical, T.S., Sinha, S, Linde, L.P., 2008. "Analogue CMOS DSSS CDLL synchronisation scheme employing complex spreading sequences," Accepted for inclusion in *IEEE Proceedings: MELECON 2008*, 5-7 May, Ajaccio.

[61] Toumazou, C., Moschytz, G., and Gilbert, B., 2002. Trade-offs in analogue circuit design: The designers companion. Dordrecht: Kluwer Academic Publishers. pp. 207-227, 517-585, 787-821.

[62] M. Božanić and S. Sinha, "Software Aided Design of a CMOS Based Power Amplifier Deploying a Passive Inductor," accepted for publication: Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 99, No. 1 (March 2008).

[63] S. Sinha and M. du Plessis, "PLL based frequency synthesizer implemented with an active inductor oscillator," Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 97, No. 3 (Sept. 2006), pp 237-242.

[64] H.R. Swanepoel and S. Sinha, "Design of a frequency hopping spread spectrum transceiver for CDMA2000 systems", Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 97, No. 3 (Sept. 2006), pp 248-254.

[65] O.S. Adekeye, S. Sinha and M. du Plessis, "Design and Implementation of a CMOS Automatic Control Gain Control (AGC) Amplifier," South African Journal of Science, Vol. 102, No. 11/12 (Oct./Nov. 2006), pp. 606-608.

[66] N. Naudé, L.P. Linde, and S. Sinha, "CMOS Based Decision Directed Costas Carrier Recovery Loop (DDC-CRL) for a DSSS Communication System," Proceedings: IEEE Africon 2007, Sept. 26-28, 2007, Windhoek, Namibia.

[67] M. Božanić and S. Sinha, "Design methodology for a CMOS based power amplifier deploying a passive inductor," Proceedings: IEEE Africon 2007, Sept. 26-28, 2007, Windhoek, Namibia.

[68] S.W. Ross, and S. Sinha, "A pipeline analogue to digital converter in 0.35 μm CMOS," Proceedings: IEEE Eurocon 2007, Sept. 9-12, 2007, Warsaw, Poland, pp. 1096-1100

[69] N. Naudé, S. Sinha and M. Božanić, "Design of a CMOS DSSS Transceiver with Carrier Recovery Employing Complex Spreading Sequences," University of Pretoria Research Symposium, Sanlam Auditorium, 26 Oct. 2006.

[70] N. Naudé, M. Božanić, and S. Sinha, "Analogue CMOS Direct Sequence Spread Spectrum Transceiver with Carrier Recovery Employing Complex Spreading Sequences," Proceedings of the IEEE MELECON 2006, May 16-19, 2006, Benalmádena (Málaga), Spain, pp. 1227-1231.

[71] M. Božanić, 2005. Design of CMOS Balanced DSSS transmitter and receiver employing complex sequences. Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa (Study Leader: Saurabh Sinha & Prof. L.P. Linde).

[72] L.R. Badenhorst, 2005. Highly efficient RF CMOS power amplifier IC for WCDMA systems. Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa (Study Leader: Johan Schoeman & Prof. L.P. Linde).

[73] N. Naudé, 2005. Design of a decision directed Costas carrier recovery loop (DDC-CRL) synchronization scheme for a DSSS communication system. Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa (Study Leader: Saurabh Sinha & Prof. L.P. Linde).

APPENDIX A: OPERATIONAL AMPLIFIER DESIGN

Operational amplifiers (op amps) are an integral part of any analogue and mixed signal system [14]. Op amps are used to realise numerous mathematical functions in this thesis, including differential to single ended conversion, differencing, integrate and dumping, buffering and summing. Implementation of a high performance op amp requires the use of passive components such as capacitors in order to control the closed loop stability [46]. This appendix deals with the analysis and design of the operational amplifier.

Before op amp architectures were examined, performance parameters of op amps were studied so that comparisons could be made between the various op amp topologies (Figure A.1). Performance parameters of op amps include gain, output swing, speed, power dissipation, input offset voltages, and noise.

Gain

The open loop gain of the op amp determines the precision of the feedback system employing the op amp [14]. In order to suppress nonlinearities, it is necessary that the op amp has a high open loop gain.

Output swing

The output swing of an op amp is defined as the maximum swing in voltage amplitude that can be passed without clipping. Since the input to the various op amp sub-systems has a wide range of signal amplitudes, it is imperative that the operational amplifier has a large swing. According to [14], achieving a large op amp swing is a principal challenge in today's op amp design.

Speed

The speed or slew rate of an op amp is defined as the op amps response to a step function. An ideal op amp has the property of reacting to a step response without any delay; however, practical op amps introduce delays in the response. With large input steps, the output of the op amp displays a linear ramp with a constant slope. Under this condition,

the op amp is said to be 'slewed' and the slope of the ramp is termed an op amps 'slew rate' [14]. Since the incoming signal can be described as a high frequency signal in nature, it is imperative that the op amp has a high slew rate.

Power dissipation

Although power dissipation is one of the main performance parameters of op amps, for the purpose of this thesis, power dissipation was a secondary concern; instead, focus was kept on high performance rather than imposing restrictions on power dissipation. From Table A4.2, the power dissipation is still reasonable.

Noise

The input noise and offset of op amps determine the minimum signal level that can be processed with reasonable quality [14]. Noise can be minimised by enlarging transistor sizes, however increasing transistor sizes will result in larger delays in the circuit. There is a trade off between output swing and noise, larger output swings result in higher noise content. For the purpose of this thesis, a compromised solution was reached so as to minimize the noise content while still maintaining as large a swing as possible.

Figure of merit

The choice of operational amplifier topology is strongly dependant on the desired performance and circuit application. Design of an operational amplifier therefore poses numerous trade-offs between parameters which eventually require a multi-dimensional compromise in overall implementation [60]. In order to make the optimal choice for the op amp topology, and based on the op amp parameters discussed above, a FOM was derived for the purpose of an op amp for this thesis. Qualitatively:

$$FOM = 2F_{gain} + 2F_{OutputSwing} + F_{speed} + \frac{1}{F_{PowerDissipation}} + \frac{1}{F_{noise}} \qquad \text{(A.1)}$$

where F_{gain}, $F_{OutputSwing}$, F_{speed}, $F_{PowerDissipation}$ and F_{noise} are the figure of gain, the output swing, the speed, the power dissipation, and the noise figure, respectively. The weighting has been added as per the requirements for this thesis.

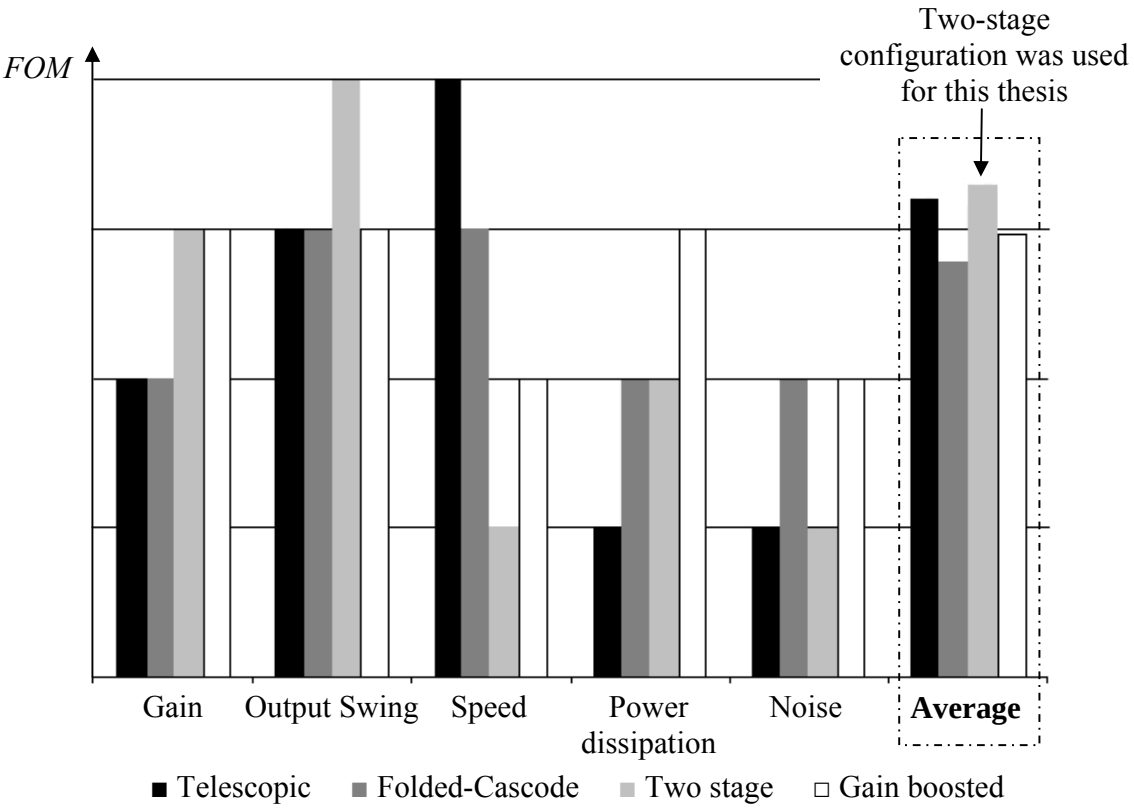


Figure A.1.

Operational amplifier topology comparison [14; 61].

The two stage operational amplifier design

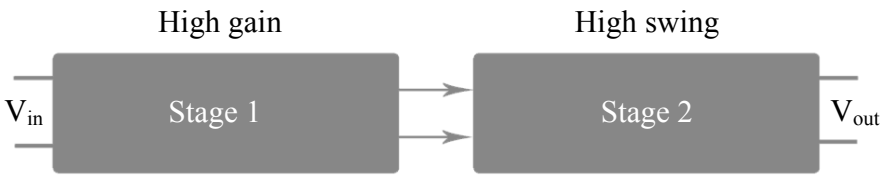


Figure A.2.

Illustration of the two stage op amp.

Figure A.3 shows the schematic of the two stage op amp used for this thesis. The design approach has been adopted from [46] and summarized in the next few paragraphs.

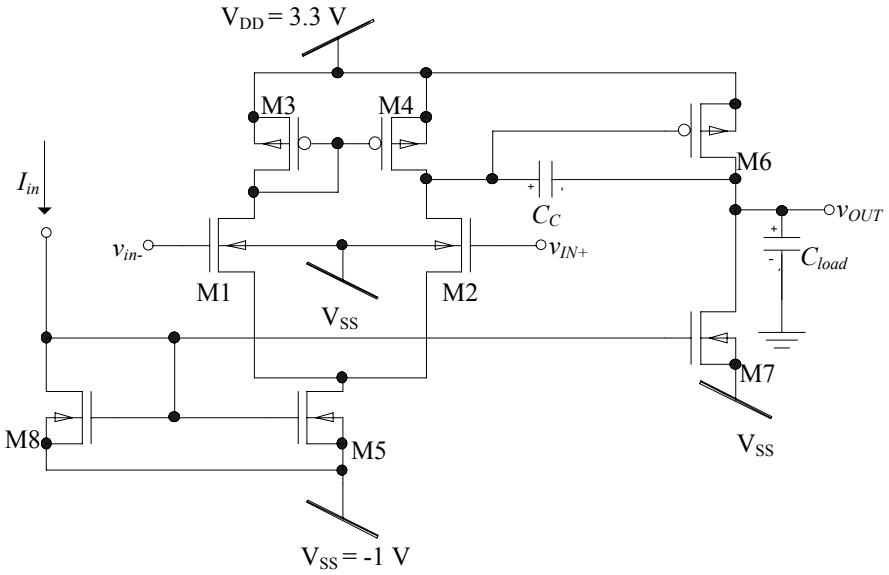


Figure A.3.

Schematic of the two stage op amp.

The op amp of Figure A.3 is a two stage unbuffered op amp. The first stage is a differential input stage with moderate gain followed by a high gain common source amplifier. The gain of the first stage is given by

$$A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \tag{A.1}$$

and the gain of the second stage is given by

$$A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6 + \lambda_7)} \tag{A.2}$$

where g_m is the transconductance of the transistor and λ is a MOS parameter that can be approximated from information provided by AMS [28]. g_m is given by

$$g_m = \sqrt{\frac{W}{L} k' I_{DS}} \tag{A.3}$$

I_{DS} is the current through the transistor and $k`$ is the transconductance parameter. $k`$ is provided by AMS and is considered a constant.

The total open loop gain of the op amp is given by

$$A_{TOTAL} = A_{v1} \times A_{v2} \tag{A.4}$$

The slew rate of the op amp is given by

$$SR = \frac{I_5}{C_C} \tag{A.5}$$

The gain bandwidth product (GBWP) of the op amp is

$$GBWP = \frac{g_{m1}}{C_C} \tag{A.6}$$

where C_c is the compensating capacitor used to stabilize the op amp.

For this design, g_{m6} is chosen such that [46]

$$g_{m6} = 2.2 g_{m2} \frac{C_{Load}}{C_C} \tag{A.7}$$

The op amp was designed to have a high slew rate and a high gain bandwidth product. High open loop gain was of secondary concern, having an op amp that could perform low gain operations on signals over a large bandwidth was more desirable than a very limited range of operation with high gain. The two primary specifications of the op amp were a GBWP of 200 MHz and a slew rate of 100 V/µs for a 10 pF load. The maximum dc input common mode voltage is chosen to be 2 V.

The specification fixes the minimum value of I_5 to 22 µA. To ensure that the design meets specifications, I_5 is set to 80 µA. The value of the compensating capacitor is set to be 5 times smaller than C_{load} to ensure a phase margin of at least 60° (see Figure A.4), this yields a C_C of 2 pF for a load capacitance of 10 pF. From (A.3), g_{m1} = 276 µA/V^2. Assuming $g_{m1} = g_{m2}$, transistor aspect ratios for the first stage can be determined using (A.1). g_{m6} can be determined from (A.7).

Table A.1 provides a summary of the calculated transistor aspect ratios.

Before implementing the op amp in any other circuits, it was simulated to determine certain specifications: for this thesis, the most important characteristics of the op amp are its GBWP, open loop gain and linearity. The results are summarized in Table A.2.

Transistor	(W/L) Ratio	Transistor	(W/L) Ratio
M1	6	M5	4.6
M2	6	M6	40
M3	2	M7	91
M4	2	M8	4.6

Table A.1.

Summary of transistor aspect ratios for the two stage op amp.

Op amp characteristic	Simulated value
Open loop gain	50 dB
GBWP (unity gain configuration)	1 GHz
Linear range (open loop)	10 mV
Output offset voltage	-3 mV
Power dissipation	4.6 mW
Input white noise	6 nV / $(Hz)^{½}$
Phase Margin	60º

Table A.2.

Summary of primary op amp characteristics.

The maximum output swing of the op amp must be limited to 0.3 V when the op amp is employed with feedback networks that control gain. If this value is exceeded, the transistors in the second (output) stage will break down, eventually damaging the transistors. AMS specifies that the maximum voltage that may be applied over a transistor is 3.6 V. For an output of 0 V, both transistors have a source-drain voltage of approximately 3.3 V.

Figure A.4 shows the op amp frequency response. A phase margin of 60º is achieved.

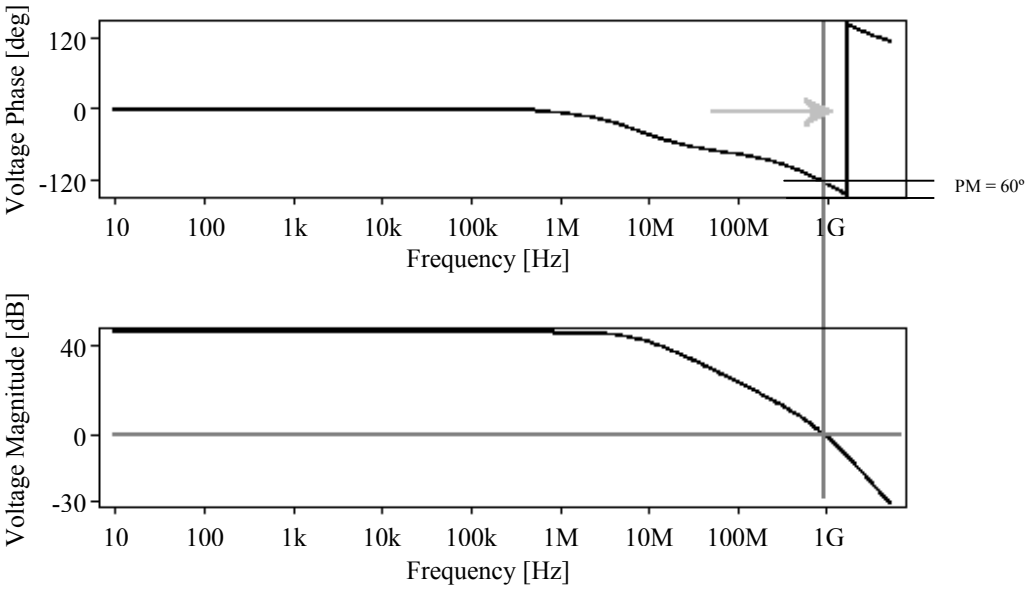
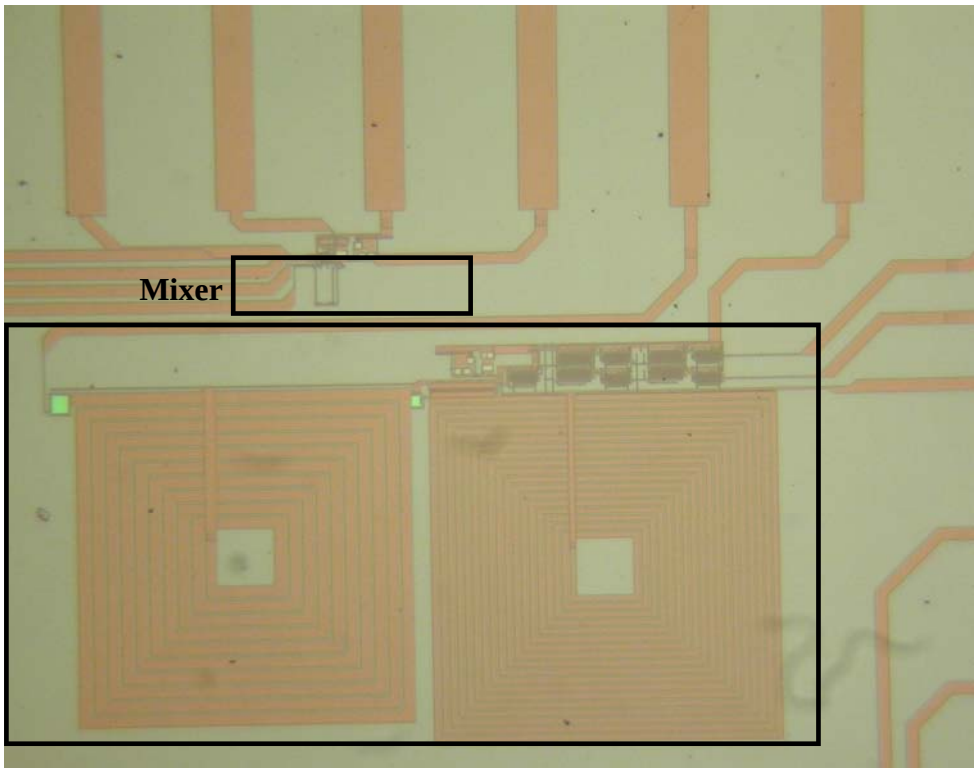


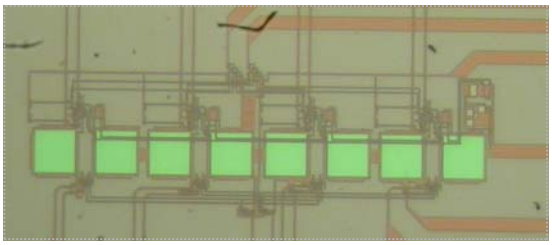
Figure A.4.

Open-loop frequency response.

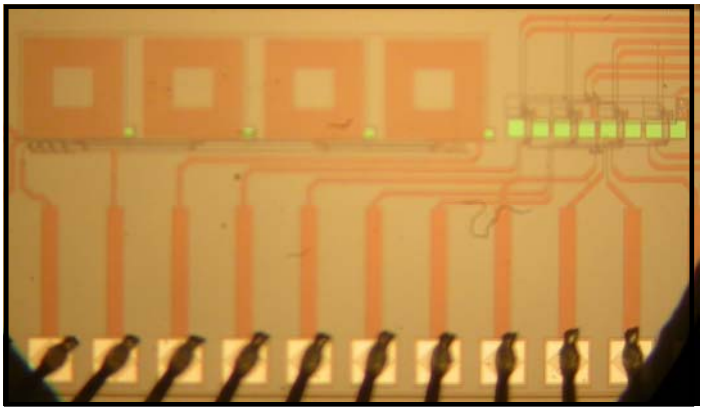
APPENDIX B: CHIP PHOTOGRAPHS



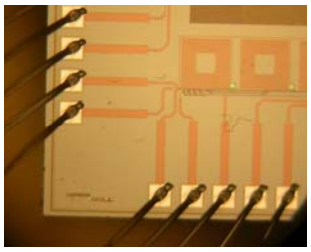
Power Amplifier



Receiver Structure



Voltage Controlled Oscillator



Pads