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APPENDIX A: OPERATIONAL AMPLIFIER DESIGN

Operational amplifiers (op amps) are an integral part of any analogue and mixed signal system [14]. Op amps are used to realise numerous mathematical functions in this thesis, including differential to single ended conversion, differencing, integrate and dumping, buffering and summing. Implementation of a high performance op amp requires the use of passive components such as capacitors in order to control the closed loop stability [46]. This appendix deals with the analysis and design of the operational amplifier.

Before op amp architectures were examined, performance parameters of op amps were studied so that comparisons could be made between the various op amp topologies (Figure A.1). Performance parameters of op amps include gain, output swing, speed, power dissipation, input offset voltages, and noise.

Gain

The open loop gain of the op amp determines the precision of the feedback system employing the op amp [14]. In order to suppress nonlinearities, it is necessary that the op amp has a high open loop gain.

Output swing

The output swing of an op amp is defined as the maximum swing in voltage amplitude that can be passed without clipping. Since the input to the various op amp sub-systems has a wide range of signal amplitudes, it is imperative that the operational amplifier has a large swing. According to [14], achieving a large op amp swing is a principal challenge in today's op amp design.

Speed

The speed or slew rate of an op amp is defined as the op amps response to a step function. An ideal op amp has the property of reacting to a step response without any delay; however, practical op amps introduce delays in the response. With large input steps, the output of the op amp displays a linear ramp with a constant slope. Under this condition,

the op amp is said to be 'slewed' and the slope of the ramp is termed an op amps 'slew rate' [14]. Since the incoming signal can be described as a high frequency signal in nature, it is imperative that the op amp has a high slew rate.

Power dissipation

Although power dissipation is one of the main performance parameters of op amps, for the purpose of this thesis, power dissipation was a secondary concern; instead, focus was kept on high performance rather than imposing restrictions on power dissipation. From Table A4.2, the power dissipation is still reasonable.

Noise

The input noise and offset of op amps determine the minimum signal level that can be processed with reasonable quality [14]. Noise can be minimised by enlarging transistor sizes, however increasing transistor sizes will result in larger delays in the circuit. There is a trade off between output swing and noise, larger output swings result in higher noise content. For the purpose of this thesis, a compromised solution was reached so as to minimize the noise content while still maintaining as large a swing as possible.

Figure of merit

The choice of operational amplifier topology is strongly dependant on the desired performance and circuit application. Design of an operational amplifier therefore poses numerous trade-offs between parameters which eventually require a multi-dimensional compromise in overall implementation [60]. In order to make the optimal choice for the op amp topology, and based on the op amp parameters discussed above, a FOM was derived for the purpose of an op amp for this thesis. Qualitatively:

$$FOM = 2F_{gain} + 2F_{OutputSwing} + F_{speed} + \frac{1}{F_{PowerDissipation}} + \frac{1}{F_{noise}} \qquad \text{(A.1)}$$

where F_{gain}, $F_{OutputSwing}$, F_{speed}, $F_{PowerDissipation}$ and F_{noise} are the figure of gain, the output swing, the speed, the power dissipation, and the noise figure, respectively. The weighting has been added as per the requirements for this thesis.

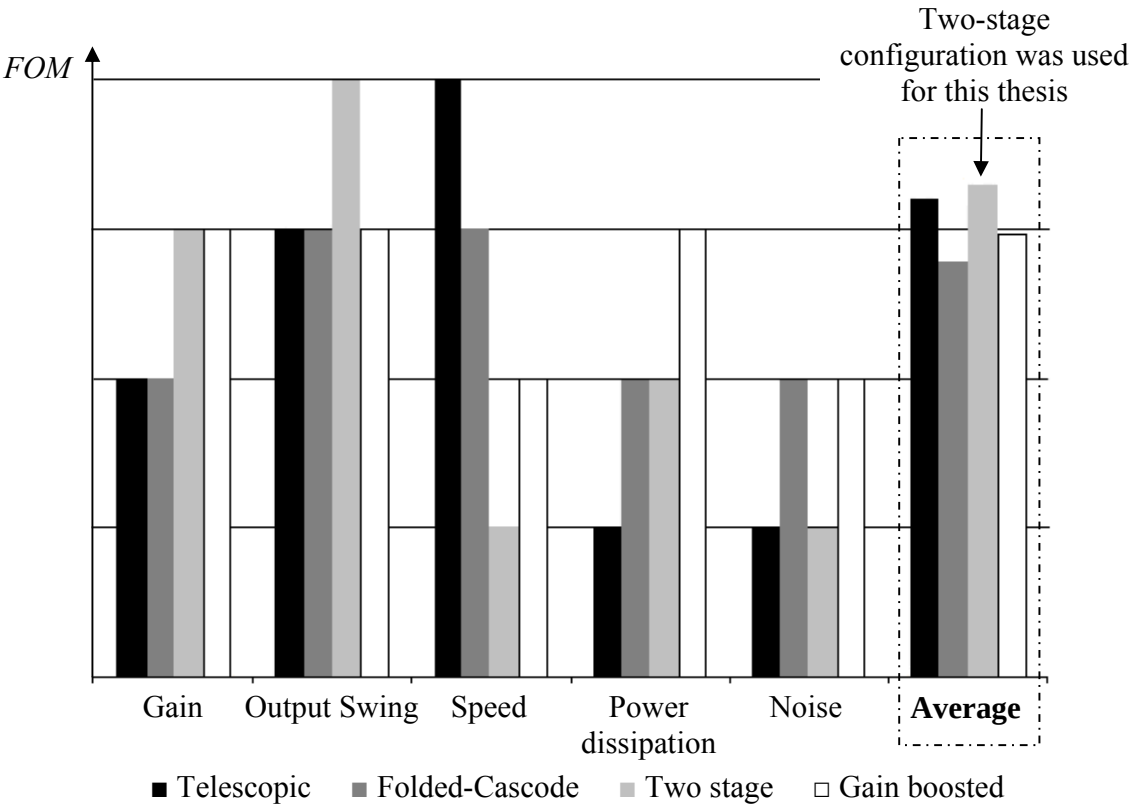


Figure A.1.

Operational amplifier topology comparison [14; 61].

The two stage operational amplifier design

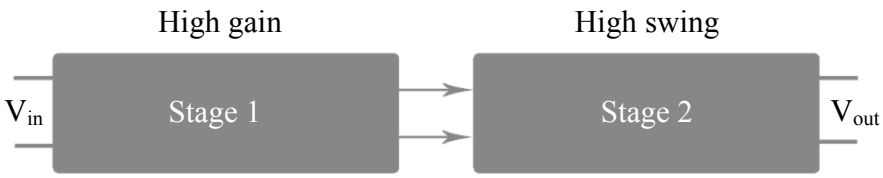


Figure A.2.

Illustration of the two stage op amp.

Figure A.3 shows the schematic of the two stage op amp used for this thesis. The design approach has been adopted from [46] and summarized in the next few paragraphs.

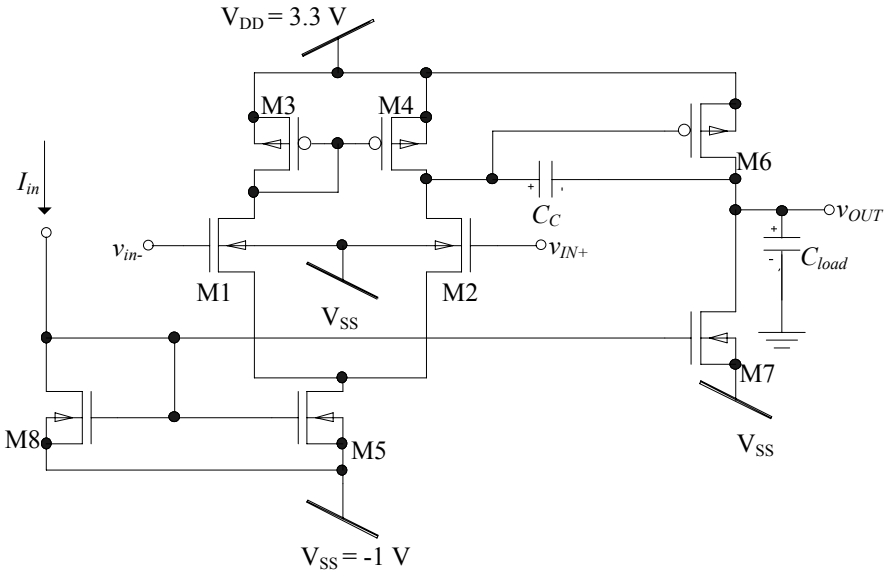


Figure A.3.

Schematic of the two stage op amp.

The op amp of Figure A.3 is a two stage unbuffered op amp. The first stage is a differential input stage with moderate gain followed by a high gain common source amplifier. The gain of the first stage is given by

$$A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \tag{A.1}$$

and the gain of the second stage is given by

$$A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6 + \lambda_7)} \tag{A.2}$$

where g_m is the transconductance of the transistor and λ is a MOS parameter that can be approximated from information provided by AMS [28]. g_m is given by

$$g_m = \sqrt{\frac{W}{L} k' I_{DS}} \tag{A.3}$$

I_{DS} is the current through the transistor and $k`$ is the transconductance parameter. $k`$ is provided by AMS and is considered a constant.

The total open loop gain of the op amp is given by

$$A_{TOTAL} = A_{v1} \times A_{v2} \tag{A.4}$$

The slew rate of the op amp is given by

$$SR = \frac{I_5}{C_C} \tag{A.5}$$

The gain bandwidth product (GBWP) of the op amp is

$$GBWP = \frac{g_{m1}}{C_C} \tag{A.6}$$

where C_c is the compensating capacitor used to stabilize the op amp.

For this design, g_{m6} is chosen such that [46]

$$g_{m6} = 2.2 g_{m2} \frac{C_{Load}}{C_C} \tag{A.7}$$

The op amp was designed to have a high slew rate and a high gain bandwidth product. High open loop gain was of secondary concern, having an op amp that could perform low gain operations on signals over a large bandwidth was more desirable than a very limited range of operation with high gain. The two primary specifications of the op amp were a GBWP of 200 MHz and a slew rate of 100 V/µs for a 10 pF load. The maximum dc input common mode voltage is chosen to be 2 V.

The specification fixes the minimum value of I_5 to 22 µA. To ensure that the design meets specifications, I_5 is set to 80 µA. The value of the compensating capacitor is set to be 5 times smaller than C_{load} to ensure a phase margin of at least 60° (see Figure A.4), this yields a C_C of 2 pF for a load capacitance of 10 pF. From (A.3), g_{m1} = 276 µA/V^2. Assuming $g_{m1} = g_{m2}$, transistor aspect ratios for the first stage can be determined using (A.1). g_{m6} can be determined from (A.7).

Table A.1 provides a summary of the calculated transistor aspect ratios.

Before implementing the op amp in any other circuits, it was simulated to determine certain specifications: for this thesis, the most important characteristics of the op amp are its GBWP, open loop gain and linearity. The results are summarized in Table A.2.

Transistor	(W/L) Ratio	Transistor	(W/L) Ratio
M1	6	M5	4.6
M2	6	M6	40
M3	2	M7	91
M4	2	M8	4.6

Table A.1.

Summary of transistor aspect ratios for the two stage op amp.

Op amp characteristic	Simulated value
Open loop gain	50 dB
GBWP (unity gain configuration)	1 GHz
Linear range (open loop)	10 mV
Output offset voltage	-3 mV
Power dissipation	4.6 mW
Input white noise	6 nV / $(Hz)^{½}$
Phase Margin	60º

Table A.2.

Summary of primary op amp characteristics.

The maximum output swing of the op amp must be limited to 0.3 V when the op amp is employed with feedback networks that control gain. If this value is exceeded, the transistors in the second (output) stage will break down, eventually damaging the transistors. AMS specifies that the maximum voltage that may be applied over a transistor is 3.6 V. For an output of 0 V, both transistors have a source-drain voltage of approximately 3.3 V.

Figure A.4 shows the op amp frequency response. A phase margin of 60º is achieved.

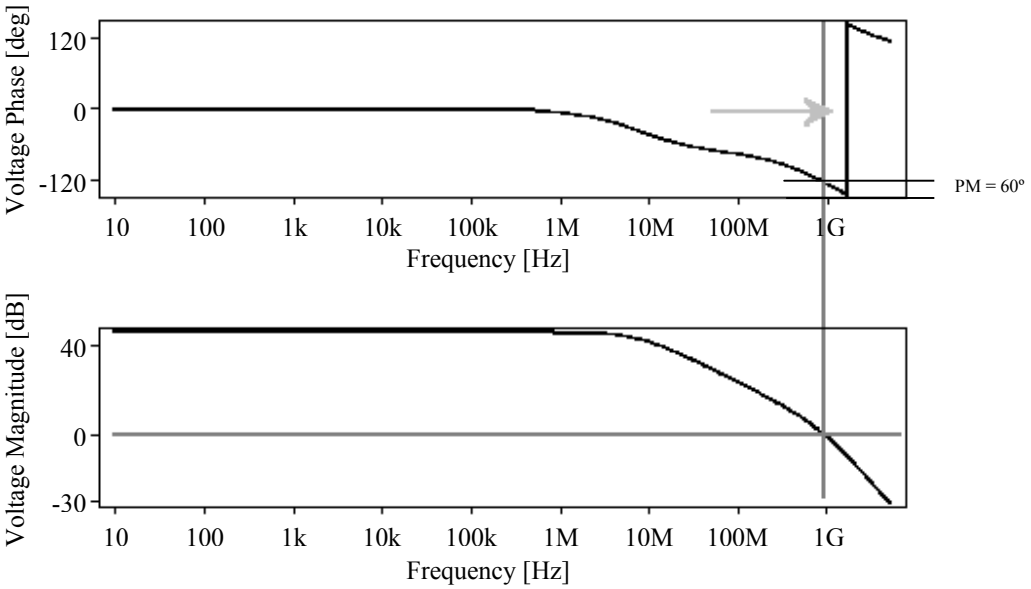
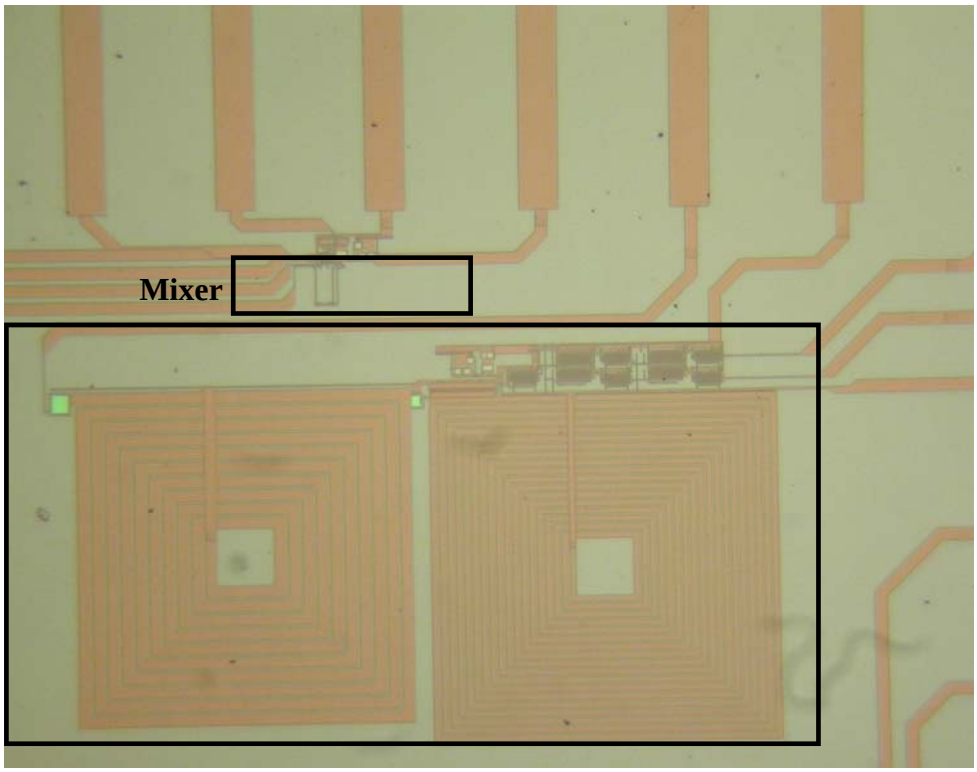


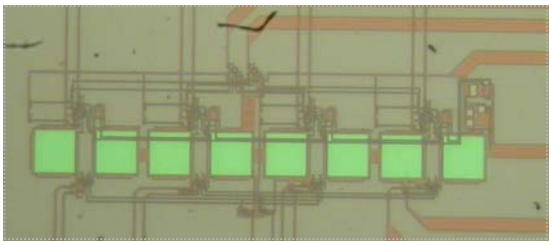
Figure A.4.

Open-loop frequency response.

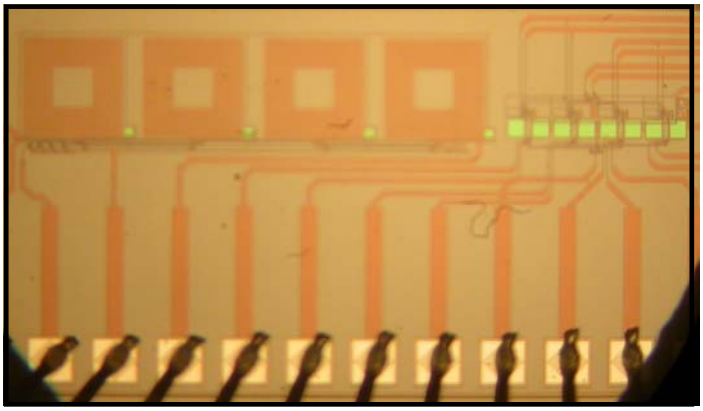
APPENDIX B: CHIP PHOTOGRAPHS



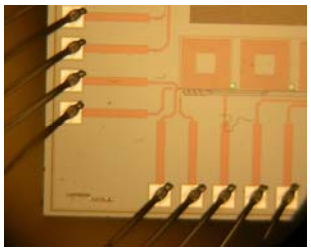
Power Amplifier



Receiver Structure



Voltage Controlled Oscillator



Pads