CHAPTER 5: SYSTEM INTEGRATION

In Chapter 2, the overall system analysis has been accomplished. Chapters 3 and 4, separately, conceptualize the analogue and digital sub-systems. This chapter serves to integrate the analogue and digital sub-systems to verify whether the system specifications proposed in Chapter 2 are met.

5.1 Simulation results for the integrated system

Integration is achieved as shown in Figure 2.17. In summary:

Transmitter

Inputs:

- digital data signal, f_a,
- CSS (real and imaginary parts),
- external clock signal (running at 8 f_a), and a
- digital HIGH or LOW determining whether the transmitter operates in balanced or unbalanced configuration.

Output: 50 Ω antenna (to be connected to the PA output).

The external clock signal is a required input signal for digital sub-systems and is denoted as `CLK_IN` or `CLKIN` in Chapter 4.

Receiver

Inputs:

- CSS (real and imaginary parts),
- 50 Ω antenna (connected to the LNA input),
- synchronization clock signal (same rate as data rate), and a
- digital HIGH or LOW determining whether the receiver operates in balanced or unbalanced configuration.

Output: Received data signal.

Figure 5.1 presents the test setup for simulating the DSSS transceiver.

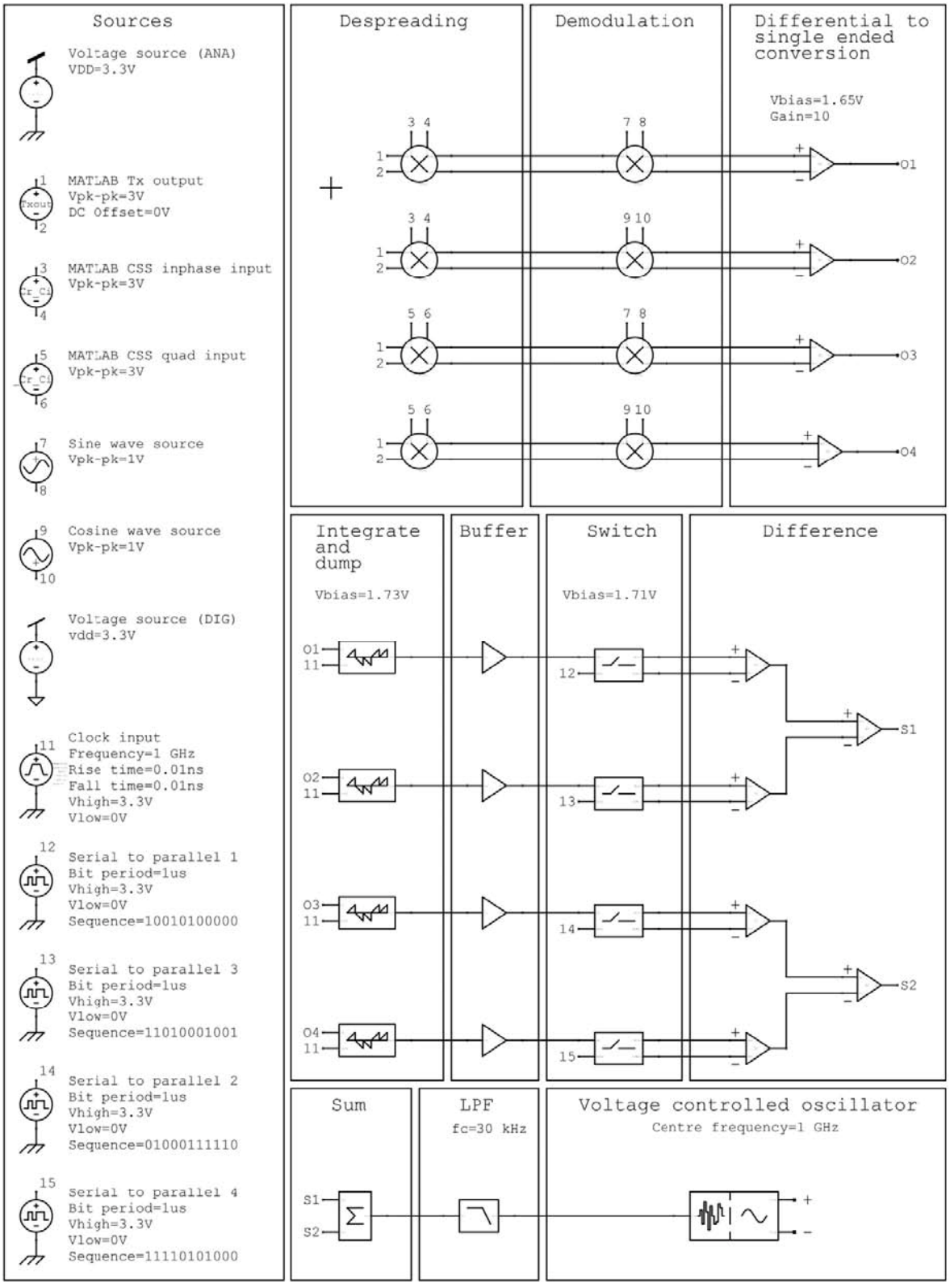


Figure 5.1.

Test signals used in simulating (exported from S-Edit) the DSSS transceiver.

Figure 5.2 captures an overview, and Figures 5.3 – 5.5 depicts the sequences used for the receiver.

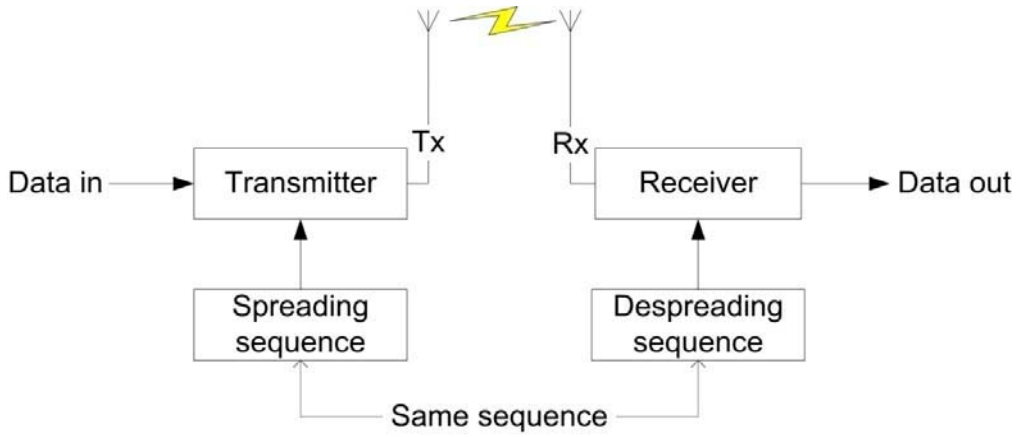


Figure 5.2.

Overview of transceiver setup.

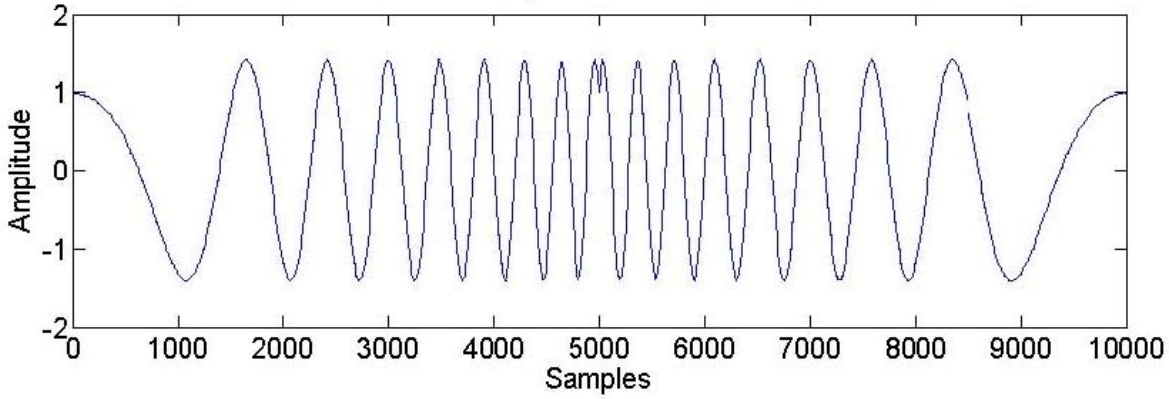


Figure 5.3.

In-phase CSS (L=64)

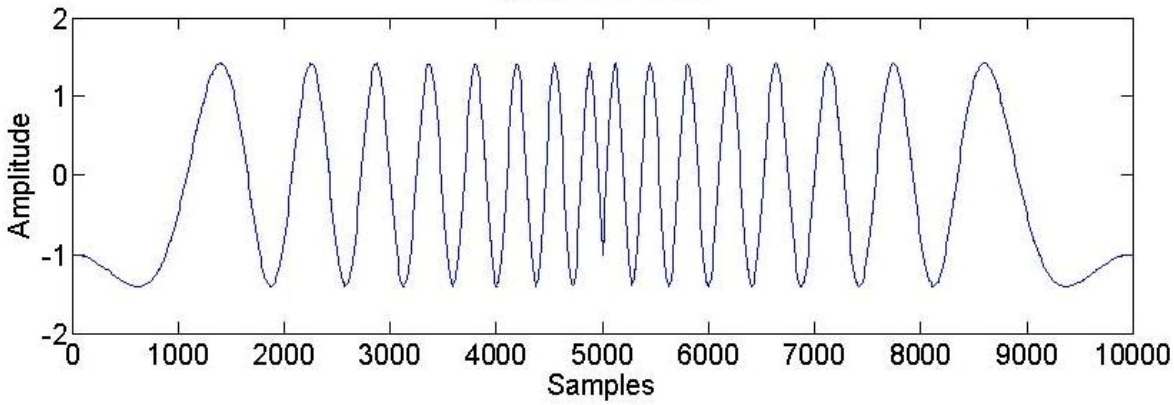


Figure 5.4.

The quadrature CSS (L=64)

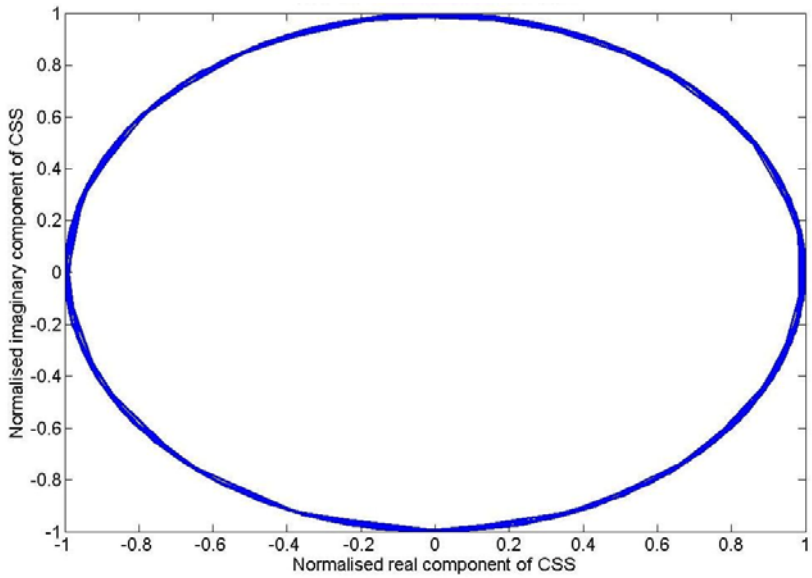


Figure 5.5.

The real versus imaginary part of the CSS (L=64).

The output of the transmitter is shown in Figures 5.6 and 5.7.

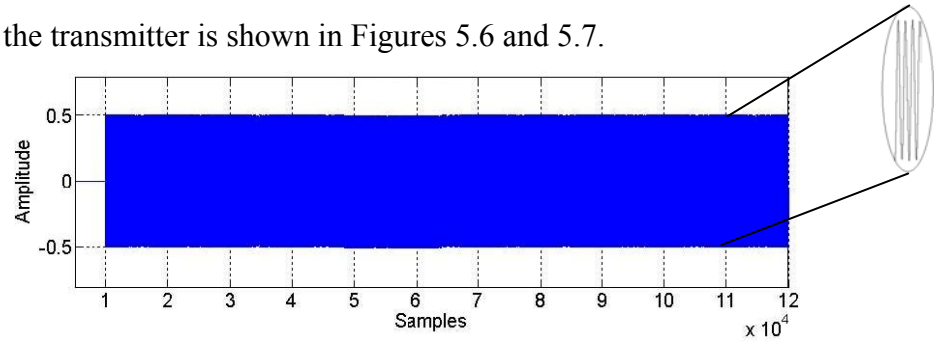


Figure 5.6.

The time domain output of the transmitter.

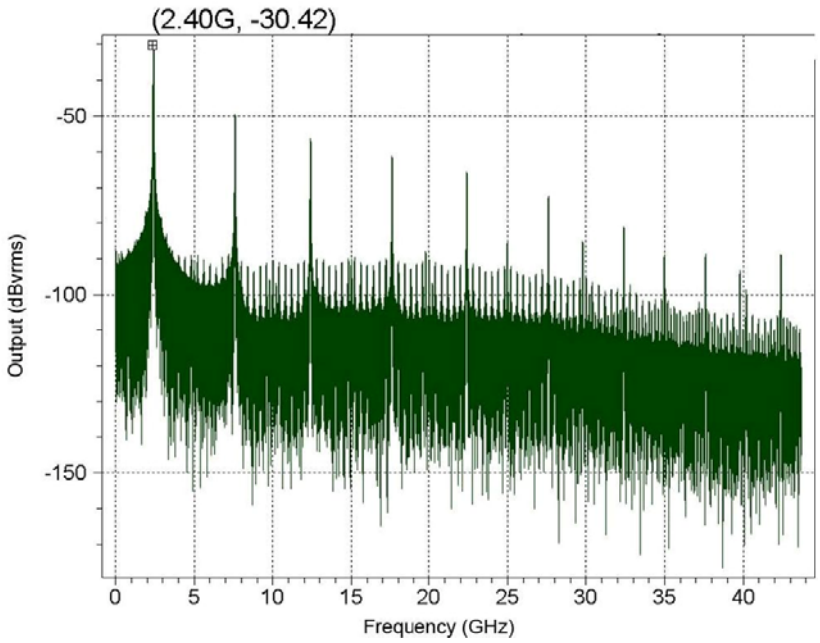


Figure 5.7.

The frequency domain spectrum of the transmitter.

As the receiver is a more complex system (Figure 2.18), step-by-step results are provided. The result of the top-branch is provided here. The output of despreading and demodulation is presented in Figures 5.8 and 5.9, respectively.

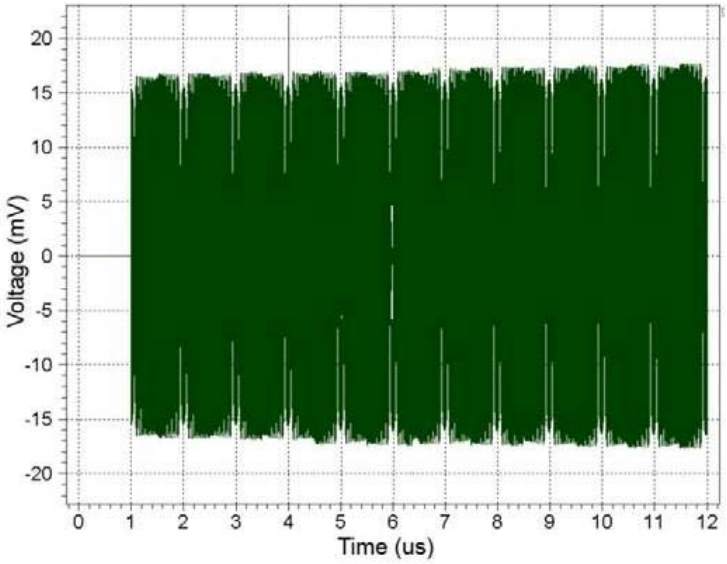


Figure 5.8.

Despread output (in-phase branch).

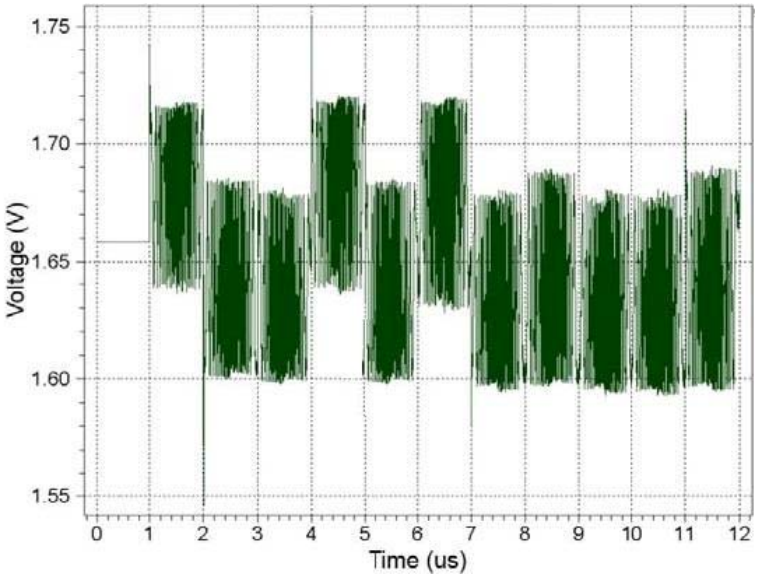
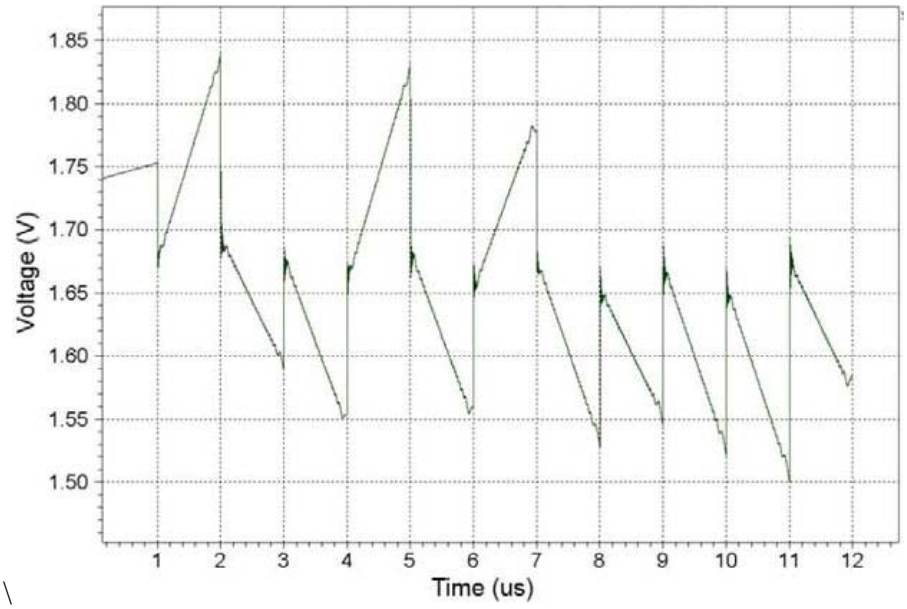


Figure 5.9.

Demodulated output (in-phase branch)

Due to the inherent bandwidth of the CMOS mixers, the double frequency terms are partially suppressed. An unexpected attribute of the CMOS demodulated output was the inconsistent bit voltage levels. This inconsistency is most likely to have been caused by the nonlinear characteristics such as inter-modulation products of the demodulating mixer components.

Figure 5.10 presents the integrate and dump circuit. As expected, a bipolar ramp output is achieved.



\

Figure 5.10.

The output of the integrate and dump circuit.

5.2 Qualification test protocol

The main specifications of the thesis (as presented in Chapter 2) are firstly verified by SPICE simulations. Selected sub-systems were also submitted for prototyping, the results are included later in the chapter.

Some specifications are defined by inputs to the system. The length and sampling rate of the CSS have been chosen arbitrarily, for these simulations it has been assumed that the chip rate of the sequence can be fixed externally to 20 Mchips/s. The sampling rate of 160 MSamples/s can be determined from the time-domain simulation of the CSS. The signal data rate is also a specified input. The modulation technique is evident from the conceptual design performed in Chapter 2. The assumed bandwidth, carrier frequency, transmitter power, receiver sensitivity, BER and power dissipation are important specifications that are verified in the next few sub-sections. These parameters have been verified mathematically in Chapter 2: in this chapter, the simulations are extended to further include process and component tolerances.

5.2.1 Carrier frequency of the transmitted signal

A data rate of 4 Mbits/s and a sequence sampling rate of 104 MSamples/s were used for this simulation. Figure 5.11 shows the FFT simulation of the transmitted signal within the range of 0 to 10 GHz. The highest magnitude lies between 2 and 3 GHz. Figure 5.12 shows a zoomed-in version of the same FFT graph: it is clear that the centre frequency is at about 2.4 GHz.

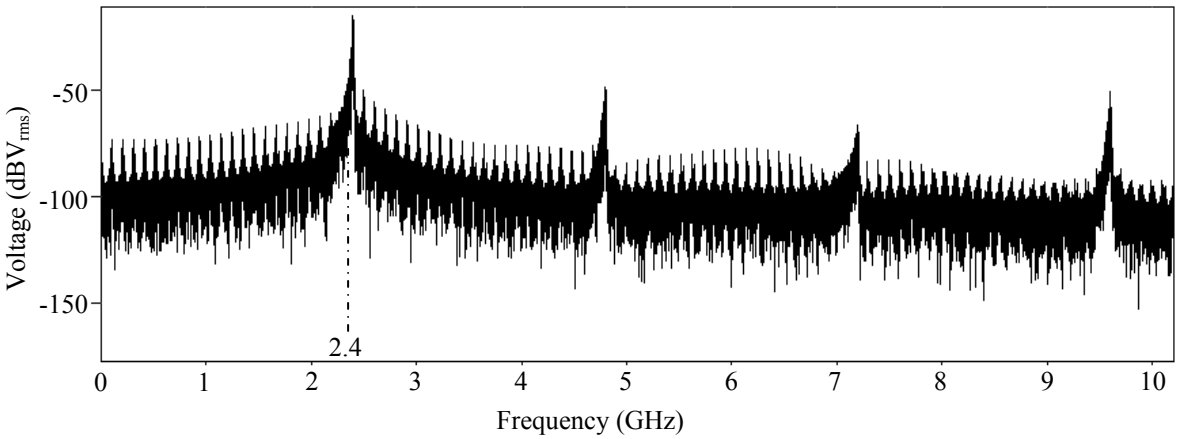


Figure 5.11.

FFT of the transmitted signal.

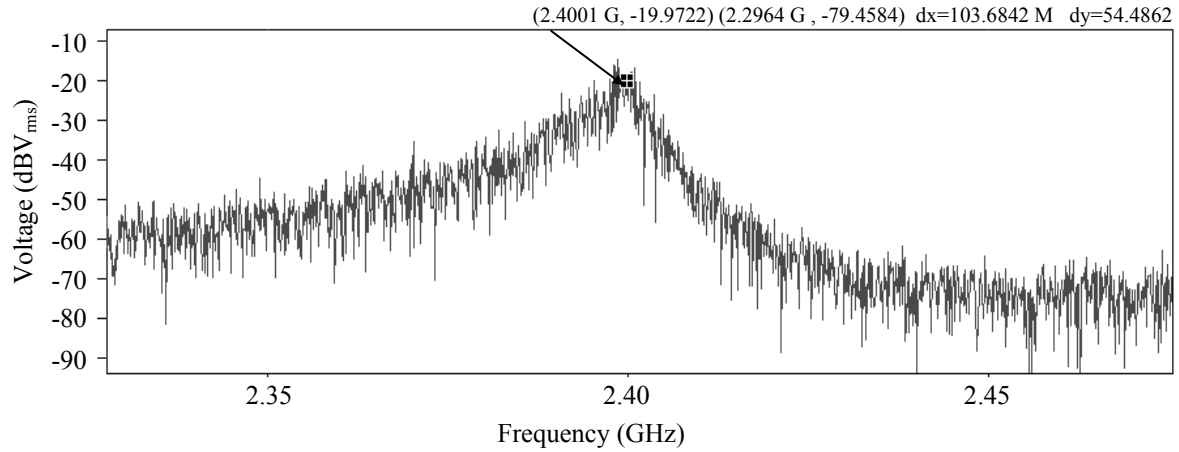


Figure 5.12.

Zoomed-in view of Figure 5.11 to show the carrier frequency.

5.2.2 Transmission bandwidth

A data rate of 6.12 Mbits/s and sequence sampling rate of 160 MSamples/s were used, as the sampling rate directly influences the bandwidth. Figure 5.13 shows a simulation of the

bandwidth. A zoomed-in version is shown in Figure 5.14, it can be seen that the bandwidth is much smaller than 20 MHz.

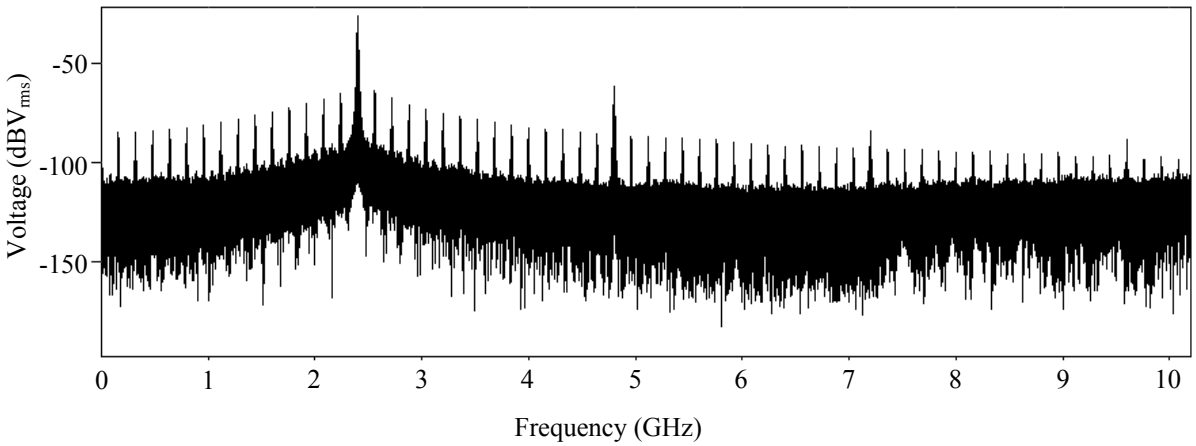


Figure 5.13.

FFT of the transmitted signal used to verify the bandwidth specification. A simulation profile is created with a PRBS data stream and the specified CSS as an input.

The bandwidth is measured between the two -3 dB points observed in Fig. 5.14.

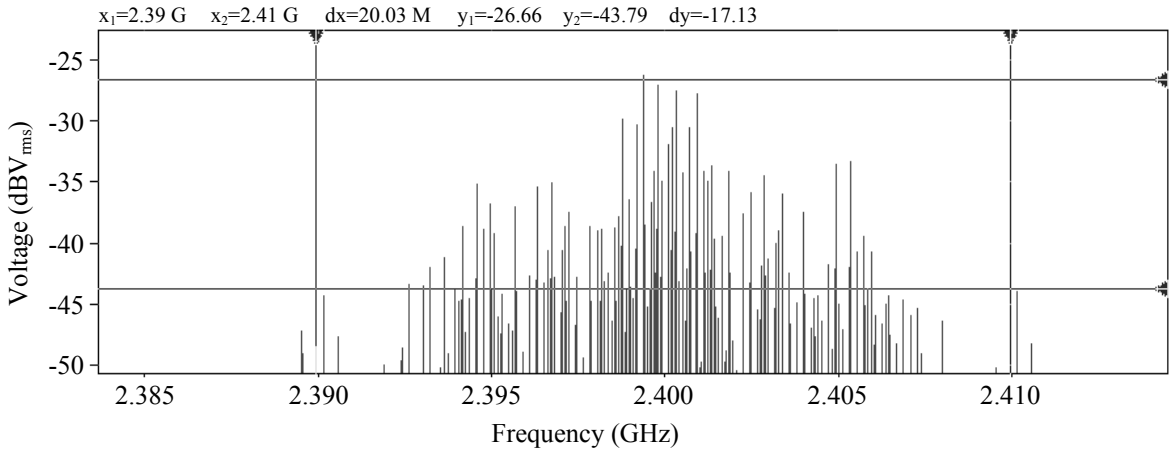


Figure 5.14.

Zoomed-in view of Figure 5.13 to show the transmission bandwidth.

As discussed in Chapter 2, the bandwidth is specified as 20 MHz, as the maximum allowed bandwidth in the 2.5 GHz ISM band is 22 MHz.

5.2.3 Transmitter power

A data rate of 4 Mbits/s and sequence sampling rate of 104 MSamples/s was used again. Figure 5.15 shows the time-domain waveform of the transmitted signal. From the simulation, the peak voltage was approximately 1 V. For a short-time period, the signal can

be approximated by a sinusoidal waveform, justifying the usage of the equation, $V_{RMS} = \frac{V_{PEAK}}{\sqrt{2}}$, to determine the RMS voltage. The maximum transmitted power is estimated to be 2 mW () over the 50 Ω load, or equivalently to be 3 dBm.

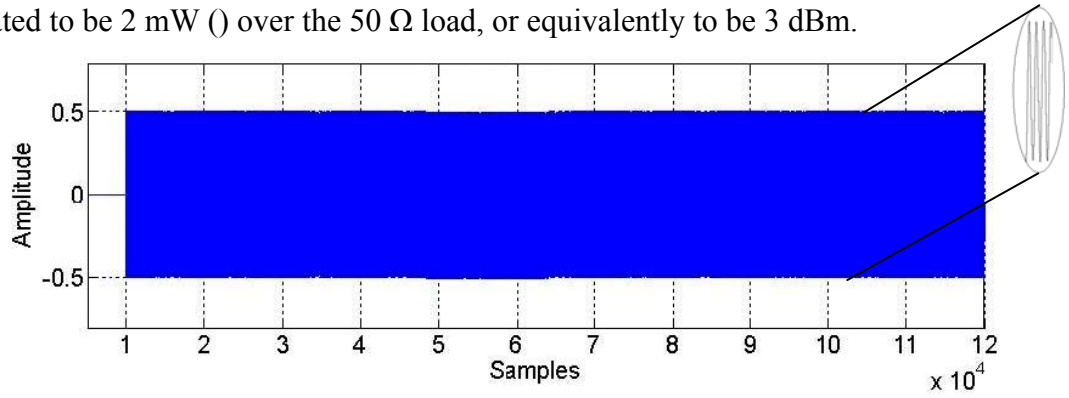


Figure 5.15.

Time-domain simulation of the transmitted signal.

5.2.4 Receiver sensitivity

A receiver's sensitivity is a measure of its ability to discern low level signals. Sensitivity in a receiver is normally taken as the minimum input signal required to produce a specified output signal having a specified signal-to-noise ratio (SNR) and is defined as the minimum signal-to-noise ratio times the mean noise power. Figure 5.16 shows the input signal (to the receiver) with a power of approximately -91 dBm. Figure 5.17 and Figure 5.18 shows the signal after integrate and dump and after comparison, respectively. The integrate and dump waveforms are weak but ramping evidently follows the direction towards the end of bit period.

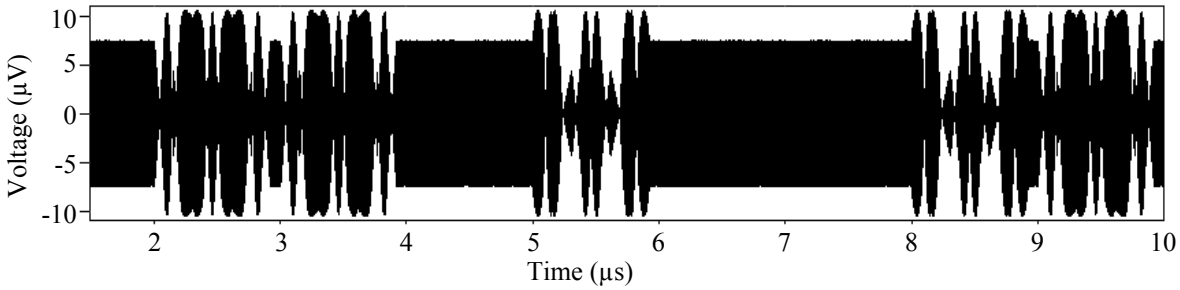


Figure 5.16.

A typical signal of approximate power of -91 dBm.

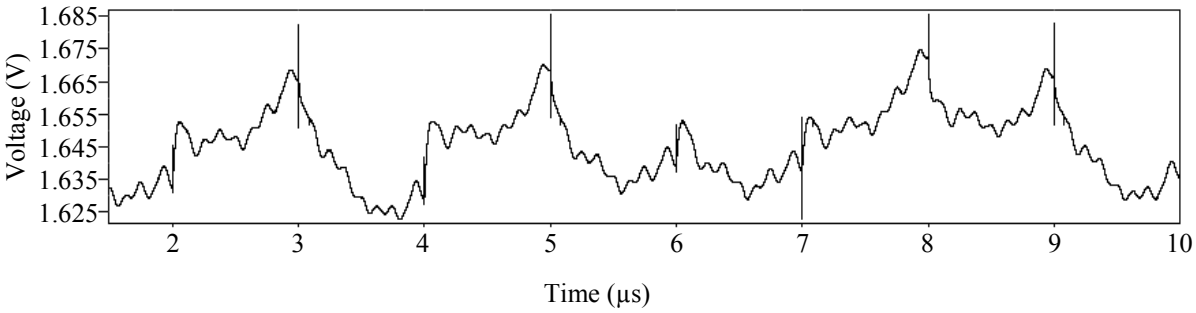


Figure 5.17.

Received signal as processed by the integrate and dump sub-system.

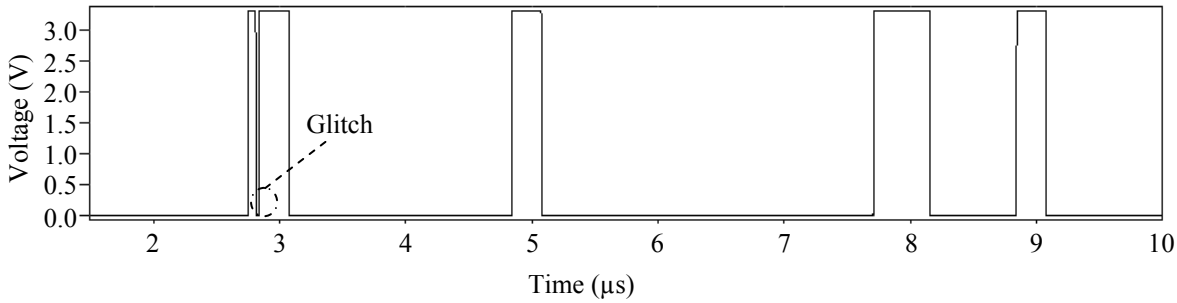


Figure 5.18.

Comparison performed on the integrated signal.

5.2.5 Bit error rate test (BERT)

Bit Error Rate Test is a testing method for digital communication circuits that uses predetermined stress patterns comprising of a sequence of logical ones and zeros. An eye diagram is used to measure the BER. The eye diagram, which is normally displayed on an oscilloscope, is simulated using MATLAB. The eye diagram is generated by repetitively sampling a digital data signal from a receiver and applying this to the vertical input, while the horizontal sweep is triggered by the data rate.

Several system performance measures can be derived by analyzing an eye diagram [37]. If the signals are too long, too short, poorly synchronized with the system clock, too high, too low, too noisy too slow to change, or have too much undershoot or overshoot, this can be observed from the eye diagram. An open eye pattern corresponds to minimal signal distortion. Distortion of the signal waveform due to inter-symbol interference and noise appears as closure of the eye pattern. In summary the following features of the eye-diagram define

1. Eye opening (height, peak to peak): measure of the additive noise in the signal

2. Eye overshoot/undershoot: measure of the peak distortion
3. Eye width: measure of timing synchronization & jitter effects

Figure 5.19 shows the modified eye diagram for the system if no noise or fading is present. Figure 5.20 shows the modified eye diagram if only fading with variance 0.25 and sampling time of 80 ns is specified. Figure 5.21 shows the modified eye diagram if the noise of variance 1 is added and sampled at a default value of 20 ps. Figure 5.22 shows the modified eye diagram of the system when the errors start appearing in the first 100 bits. The variance of noise is experimentally determined to be 25, as fading is kept constant at a variance 0.25 and sampling time of 80 ns. This estimates the BER as 10^{-2} for these parameters in the top branch (Figure 2.17) of the receiver (if there is no error detected in the other three branches of the receiver, the total BER is 1/250). This process could be carried out in a more refined manner if more time and memory was available, however, the technique can be used to determine the BER for any noise and constant fading parameters.

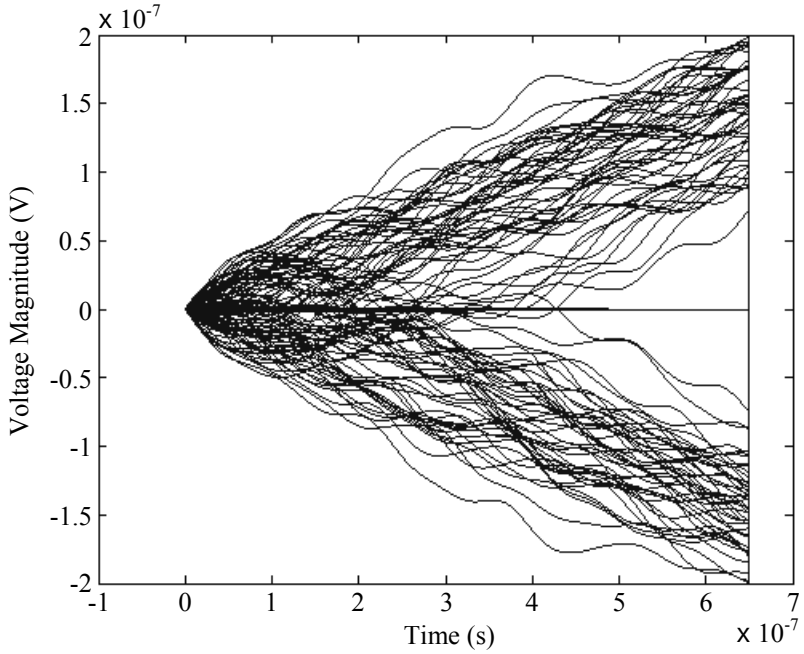


Figure 5.19.

Modified eye diagram of the signal after it is processed by the integrate and dump sub-system if no fading or noise is present in the channel.

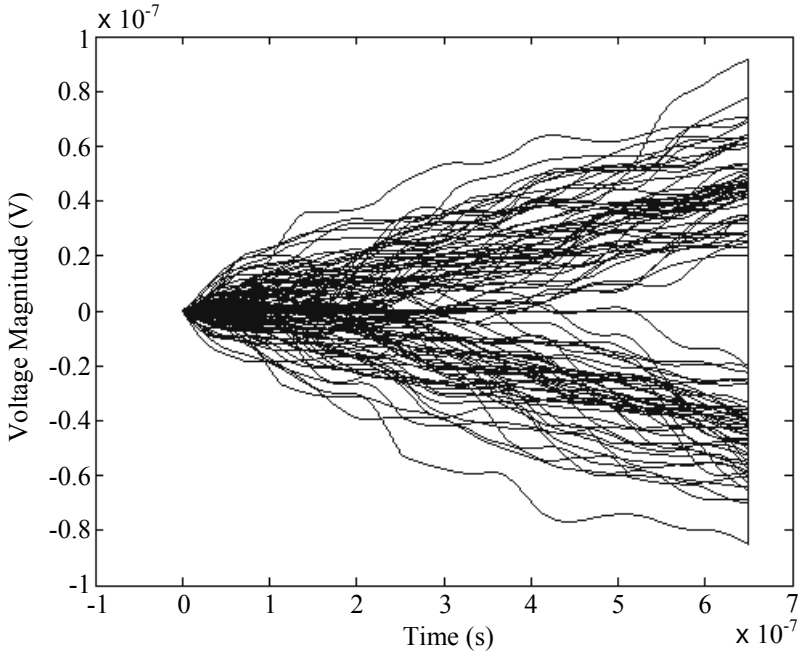


Figure 5.20.

Modified eye diagram of the signal after it is processed by the integrate and dump sub-system if only fading with variance of 0.25 and sampling period of 80 ns is present in the channel.

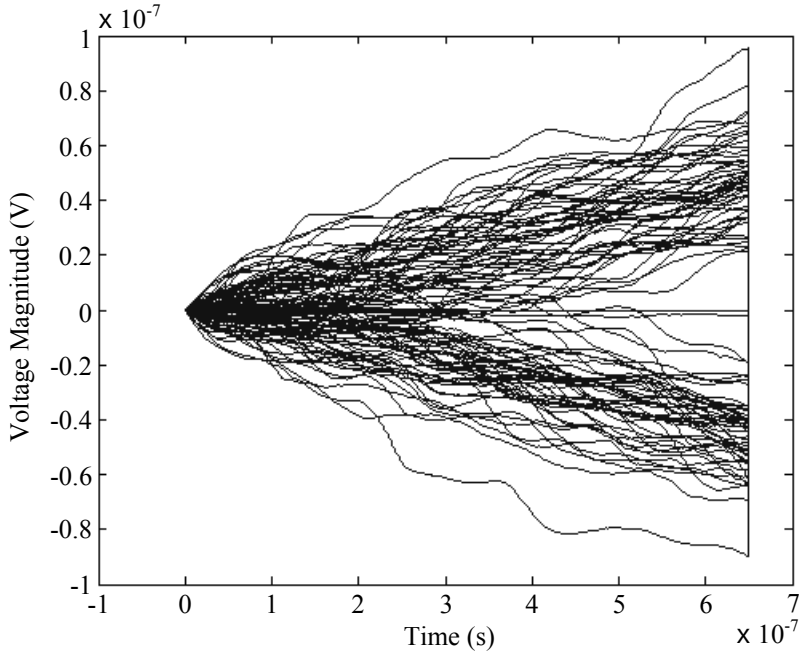


Figure 5.21.

Modified eye diagram of the signal after it is processed by the integrate and dump sub-system if fading with variance 0.25 and sampling time of 80 ns. Noise with a variance of 1 and sampling time of 20 ps are present in the channel.

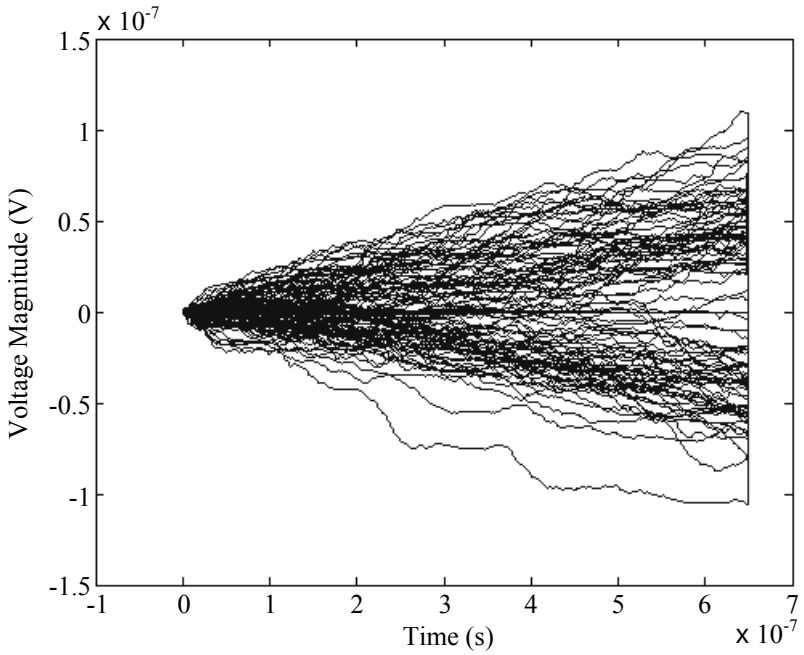


Figure 5.22.

Modified eye diagram of the signal after it is processed by the integrate and dump sub-system if the channel has the properties that just start to influence the performance of the receiver.

5.2.6 CDLL BER

The CDLL is integrated as shown in Figure 2.19. This section summarizes the test procedure used to simulate the BER of the CDLL. For the first part, simulation was setup to determine the BER of the CDLL in the locked state with jitter.

The spreading sequence used was of length 64 CSS and the bit rate was 1 Mbps. The carrier frequency was set to have a mean frequency of 1 GHz and a standard deviation of 5 kHz. The graph generated is half an eye diagram, with the top half representing positive ramps and the lower half negative ramps. Positive ramps represent logic highs and negative ramps represent logic lows. Traces crossing the centre line about 0 result in error bits. The proximity of a ramp to the centre line is an indication of the deviation from the ideal. The bold line around the centre line is caused by MATLAB interpolating between the first and last sample of each bit.

Figure 5.28 shows that no apparent bits are in error. This shows that the CDLL has met the specified BER of 10^{-3} for the simulation period in a mathematical environment. The result

is considered satisfactory, but several factors must be taken into consideration when extrapolating these results to the CMOS CDLL.

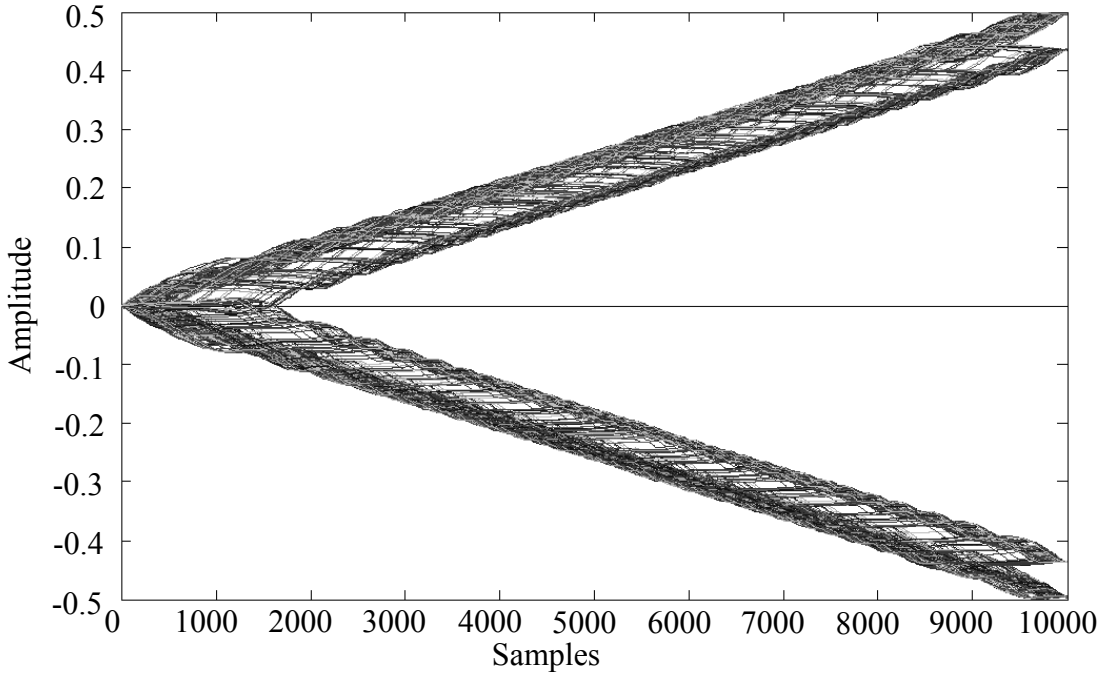


Figure 5.23.
Eye diagram of the recovered data with a noiseless channel.

Figure 5.24 shows the performance of the CDLL operating with a noisy channel, the data is still recovered with no apparent bits in error, this proves the immunity of a DSSS system employing CSS to interference and noise in the channel. It is evident from Figure 5.25 that if the CDLL looses lock, the BER will increase and the bits cannot be recovered since accurate despreading cannot occur. The eye diagram of the CMOS CDLL will tend to show a narrower eye since the integrator of the CDLL is not ideal, which results in a decrease in the ramps ideal gradient, with a tendency to have negative gradients during the early stages of the integration period.

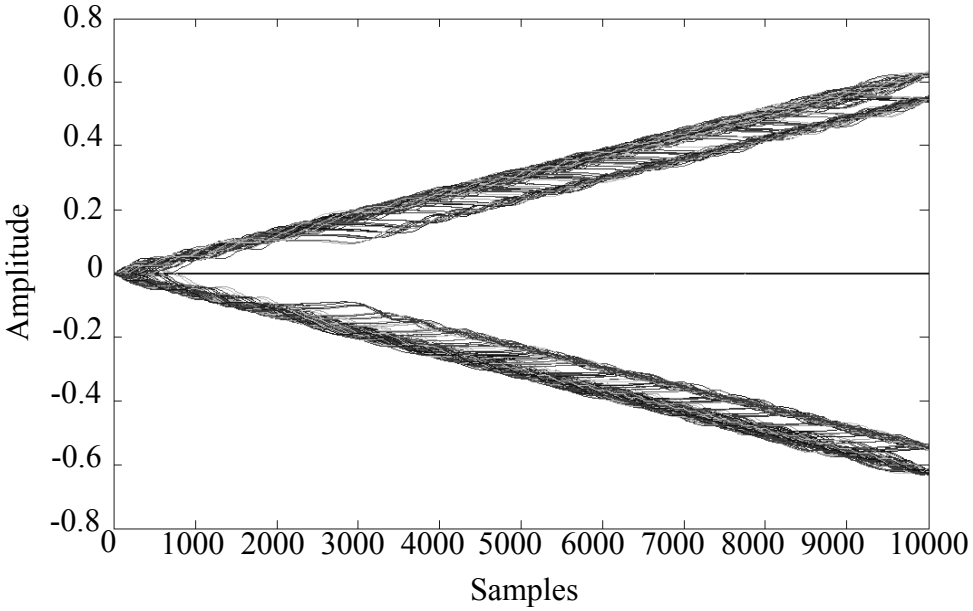


Figure 5.24.

Eye diagram of the recovered data with a noisy channel.

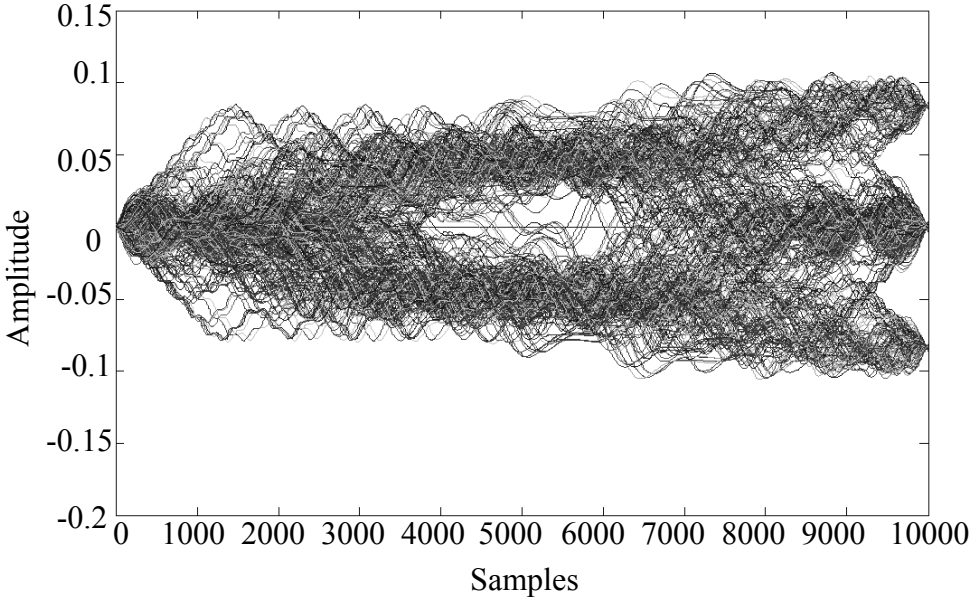


Figure 5.25.

Eye diagram of the recovered data when the CDLL has lost lock [27].

5.2.7 Power dissipation

Figure 5.26 shows the waveform of the total current drawn from the positive power supply and therefore delivered to the rest of the circuit if the IC is actively operating in transmit mode. It is seen that the maximum current is approximately 77 mA, or the power dissipation is about 254 mW.

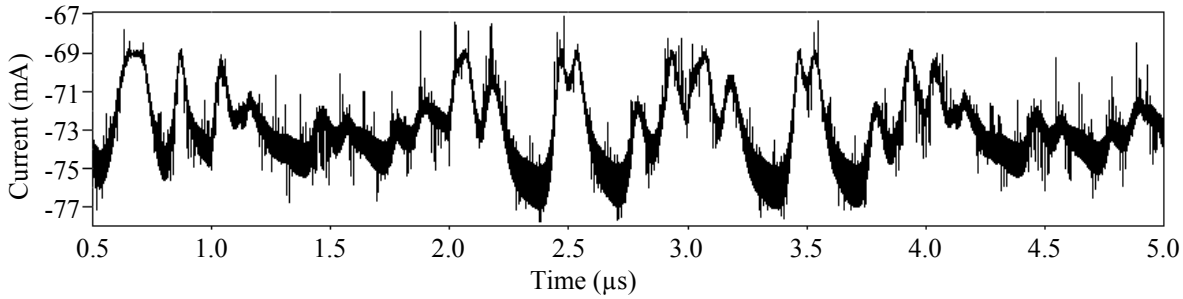


Figure 5.26.

Waveform of the current drawn by the transmitter for a duration of 4.5 µs [71; 72].

Figure 5.27 shows the waveform of the total current drawn from the positive power supply if the IC is operating as a receiver. It is seen that the maximum current drawn is approximately 70 mA, or the power dissipation is about 210 mW.

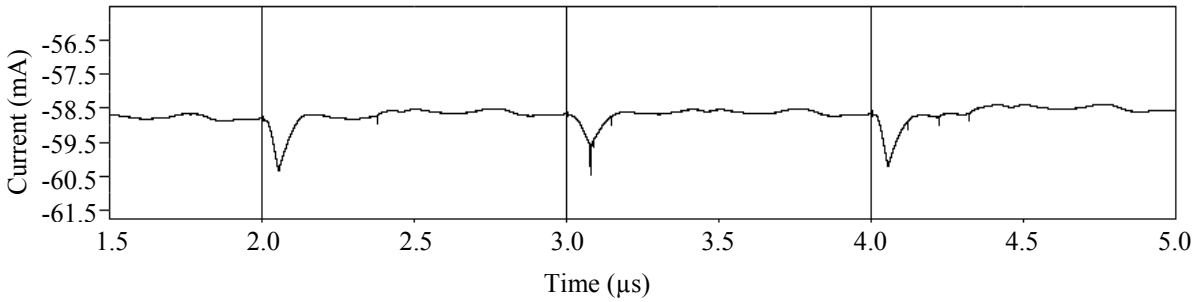


Figure 5.27.

Waveform of the current drawn by the receiver for a duration of 3.5 µs [71; 72].

5.3 Prototyping of design

5.3.1 Design submission to Europractice

The University of Pretoria interfaces with foundries, such as AMS via Europractice. It was the intention of this thesis to submit selected sub-systems for prototyping. To enable effective probing, a large number of test pads are proposed, and individual sub-systems are kept independent of each other (i.e. separate grounds, separate supply rails, etc). The independence also assists in a case where a faulty sub-system does not affect another working sub-system. A design rule check (DRC) and layout versus schematic (LVS) was completed prior to design submission. Due to the large nature of the design of this thesis and research cost/timeline, only selected sub-systems were integrated.

5.3.2 Packaging & test printed circuit board (PCB)

Packaging serves:

- as a bridge between components and the external world,
- as a physical scale translator between component features and the surrounding environment,
- as a product differentiator to keep pace with device requirement in increased performance (functionality/complexity) and reduced cost,
- to offer protection (environmental management of device),
- for providing connectivity and routing (electrical, optical, and material),
- to provide mechanical stress control,
- for thermal management, and
- for testability and burn-in.

Both packaged and naked chips were ordered. A ceramic package was chosen as it can withstand high temperatures and can be hermetically sealed. From a prototyping perspective, the ceramic packages offered by Europractice are also cheaper than plastic packages. A 68-pin ceramic leadless chip carrier (CLCC) was considered sufficient for this design. Such ceramic leadless chip carriers do not have metallic external leads. Additional features of CLCCs include their compact size, their light weight, and their ability to adapt to multiple functions. A typical example is shown in Fig. 5.28.

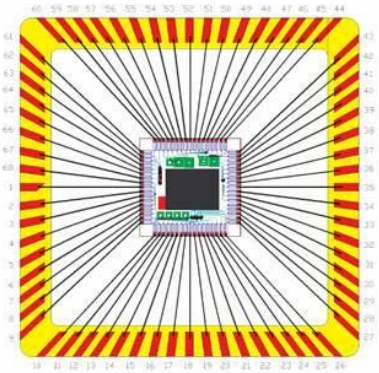
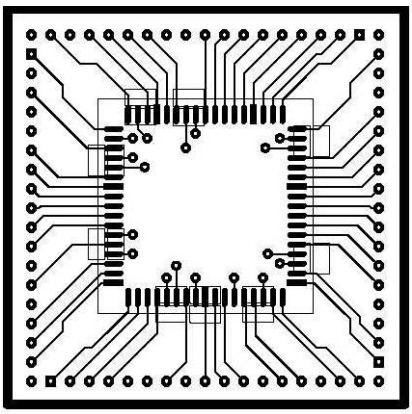


Figure 5.28.
Example bonding diagram for the CLCC-68.

A test-circuit was designed to enable an effective probing of the CLCC-68. This is shown in Figure 5.29.



(a)

Figure 5.29.

Typical PCB that was designed for probing for measurements.

5.3.3 High-frequency equipment and test-bench

A typical measurement setup is shown in Figure 5.30.

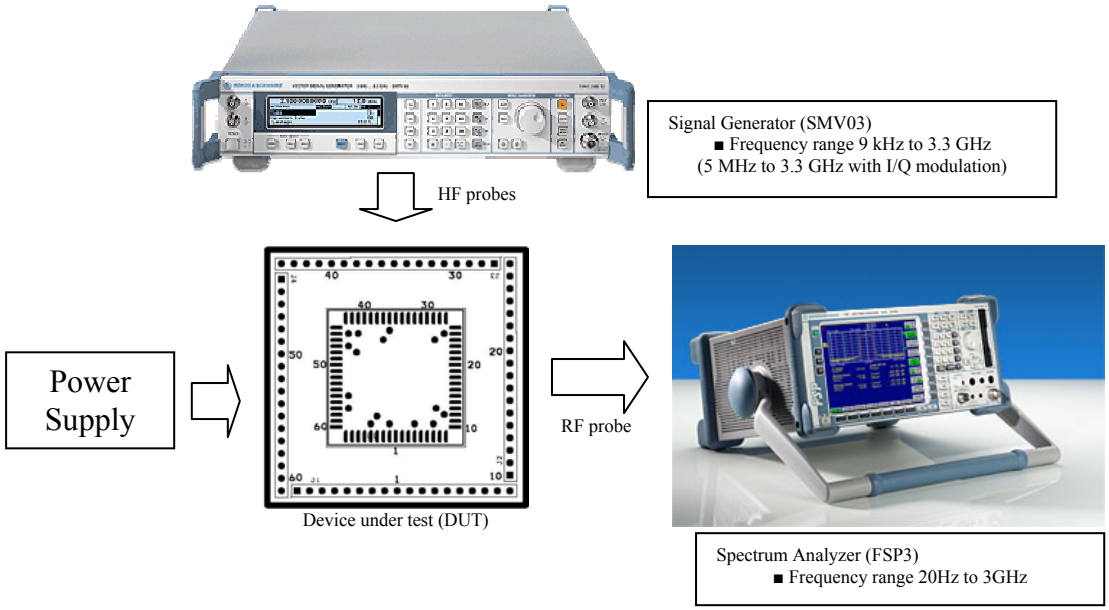


Figure 5.30.

Typical laboratory bench setup (not drawn to scale) for measurements. In case where a VCO is tested, the signal generator[1] is not utilized. The signal generator is further utilized to emulate a received signal (for test purposes) for the LNA, the PA, & the receiver.

The following user manual specifications are important and repeated here. The following specifications should not be exceeded:

• Maximum safe DC input voltage (without 10:1 divider (Fig. 5.31)): ±50 V

• Maximum safe DC input voltage through a 10:1 divider: ±200 V

[1] http://www.rohdeschwarz.com

• Maximum safe RF voltage (without 10:1 divider): 1.5 V peak

• Maximum safe RF voltage through a 10:1 divider: 15 V peak

To minimize the potential for damage, measurements were first taken with the 10:1 divider. The 10:1 divider was only removed when the following conditions are met:

• RF and DC levels were known to be within the above tolerances.

• Higher sensitivity is required than is possible with the 10:1 divider.

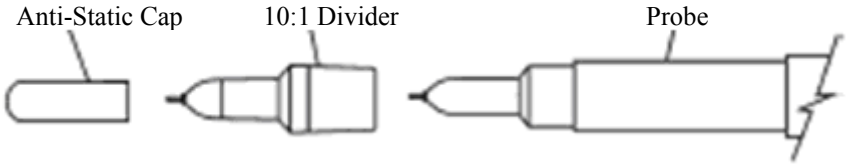


Figure 5.31.

A RF probe including a 10:1 Divider [58].

Electrostatic discharge (ESD) is a serious problem [58]; the following steps were observed:

• The tip of the probe is never touched as the probe microcircuit is susceptible to damage by static discharge.

• A ground strap was worn to eliminate ESD on the body.

• An anti-static bench mat is used to eliminate ESD on the work surface. Caution was observed to use a workbench that was not covered by carpet.

• It was also ensured that ESD is not introduced to the DUT while the probe is being used as the static charge could damage the DUT as well as the probe.

5.4 Practical measurements

Fig. 5.32 shows the output of the VCO.

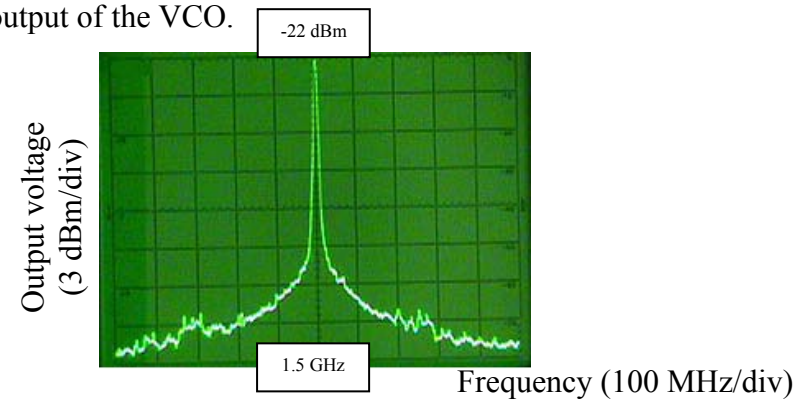


Figure 5.32.

A frequency sweep around 1.5 GHz (the test oscillator).

By changing the dc voltage to the VCO, the frequency/voltage gain, K_{VCO} was obtained (Fig. 5.33). K_{VCO} compares well to a value of about 0.25 GHz/V obtained in simulation. The phase noise of the VCO is shown in Fig. 5.34.

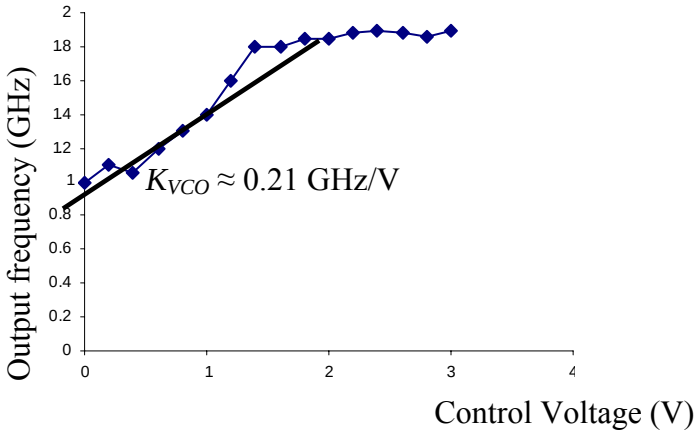


Figure 5.33.

Plot of the output frequency against the input voltage.

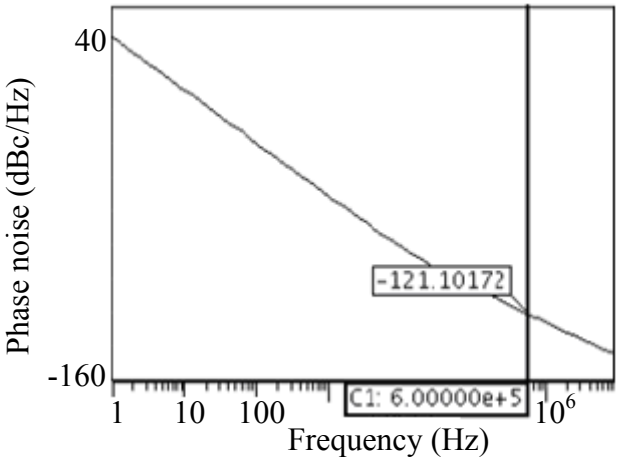


Figure 5.34.

VCO phase noise of -121 dBc/Hz at an offset of 1 MHz.

Analogous to the simulation of Fig. 3.23, a measurement is performed to determine the intercept points of the mixer – this is shown in Fig. 5.35.

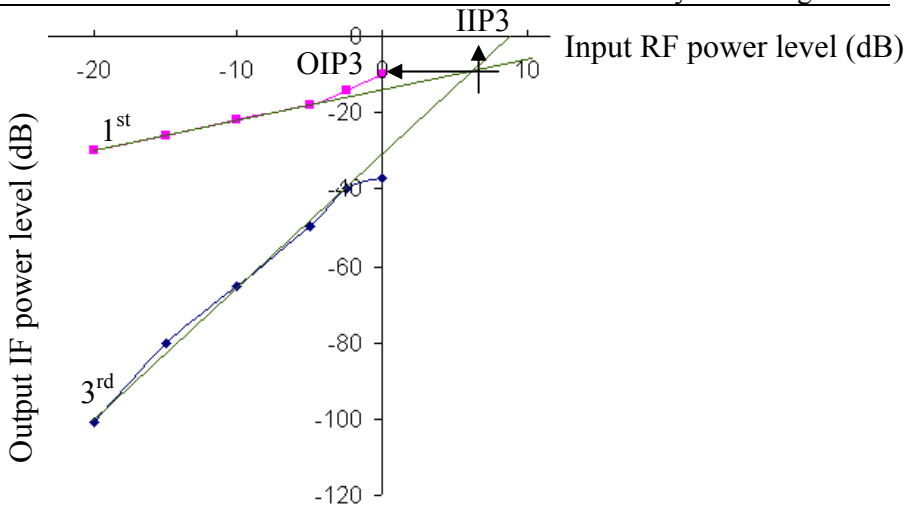


Figure 5.35.

Plot of first and third harmonic outputs of the mixer.

An OIP3 of -10 dBm & IIP3 of 7 dBm is obtained.

Since a hardware system to generate CSS was outside the scope of this thesis, a PN sequence and a GOLD sequence was used to test the multiplier and the summation performed (top branch of the transmitter). The VCO designed for the thesis also served as the local oscillator (see Fig. 2.17). The results are shown in Figures 5.36-5.37. The results are similar to the results of Chapter 2, except that the amplitudes were generally reduced (since frequency is the parameter of interest for these specific sub-systems, the reduced amplitudes did not pose a major problem). Only selected results (as per measurement points on the transmitter branch) are repeated in this section.

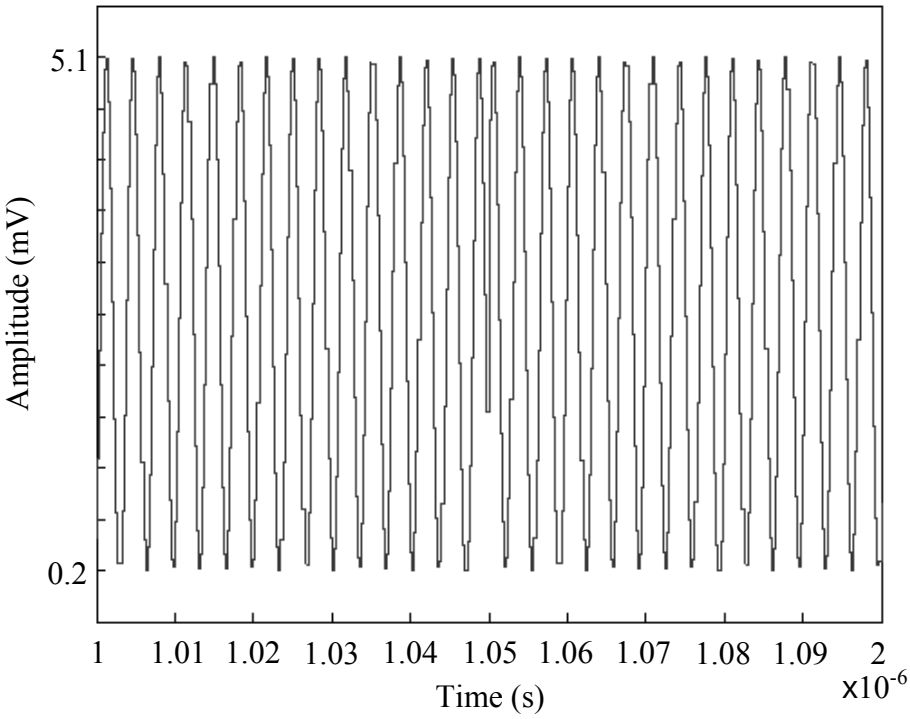


Figure 5.36.

Modulated data signal.

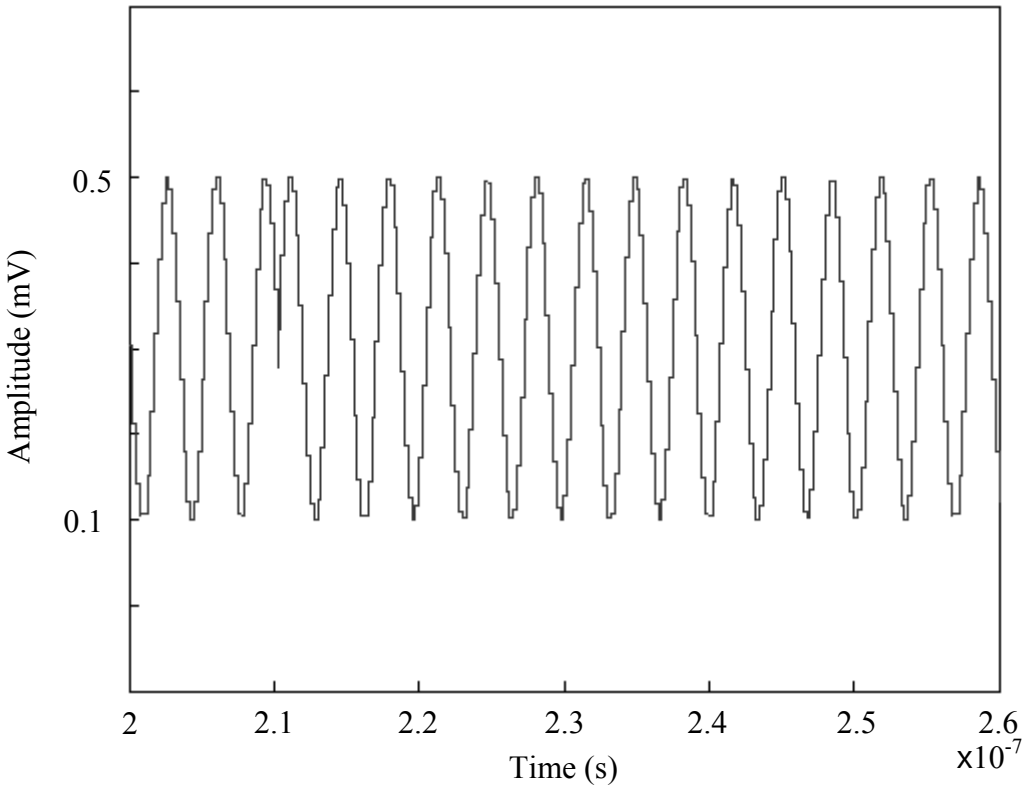


Figure 5.37.

A portion of the signal, after the summation sub-system.

Using the same sequences as for the transmitter, measurements were performed to test the despreading sub-system (Fig. 2.17). The result is shown in Fig. 5.38.

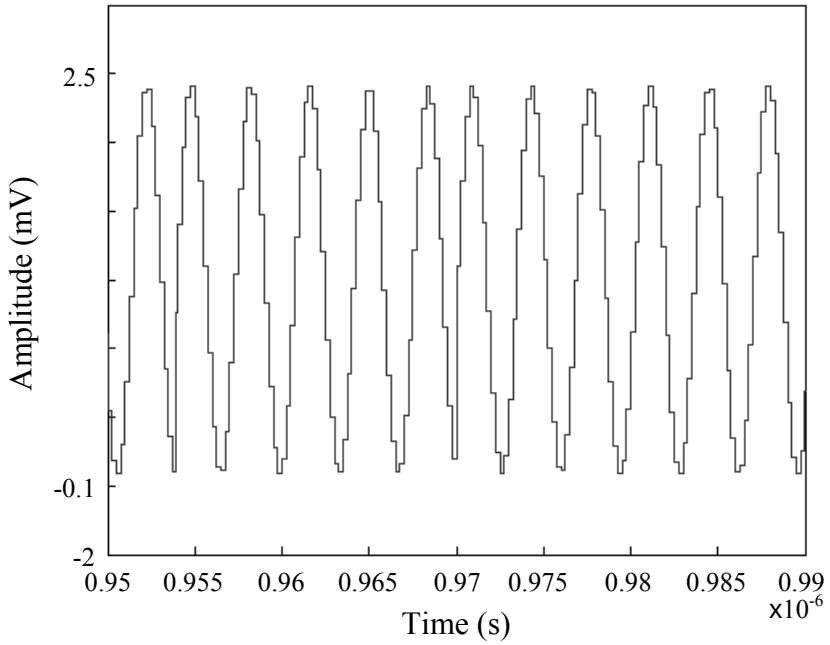


Figure 5.38.

Despread signal.

The despread signal of Fig. 5.38 is then demodulated using the same carrier frequency as that which was used at the transmitter. The resulting signal is shown in Fig. 5.39. This

signal resembles the data signal, but has a high frequency component that can be filtered out.

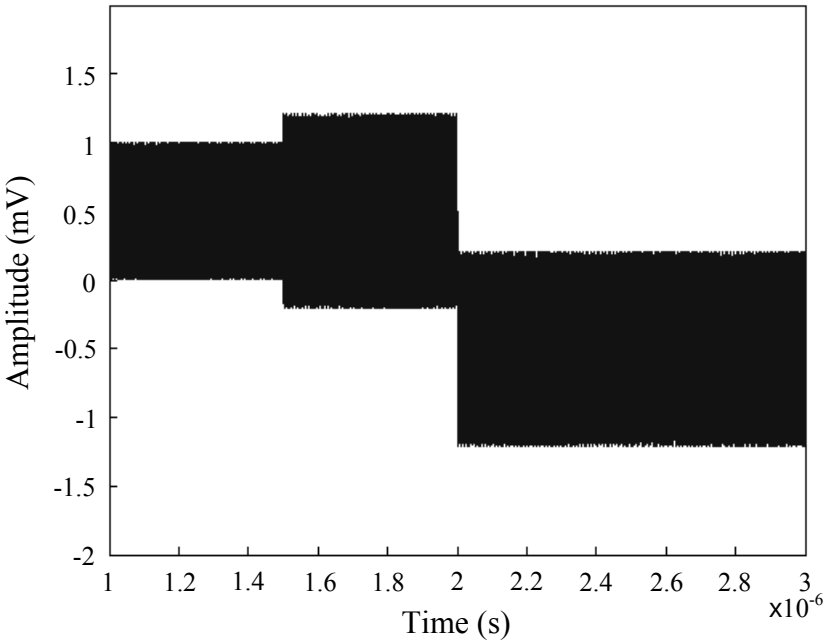


Figure 5.39.

Recovered, unfiltered signal.

The reduced amplitudes are expected and can be attributed to gain variations in CMOS sub-systems but also due to impedance matching differences (probe & scope).

CHAPTER 6: CONCLUSION

This chapter summarizes the research contributions of this thesis as well as provides some ideas for future research.

6.1 Technical summary and contribution

DSSS systems are SS systems where spreading is achieved by direct modulation of a data modulated carrier by a wideband spreading signal or code. The spreading signal is chosen to facilitate demodulation at the intended receiver and to make demodulation as difficult as possible for an unintended receiver [59]. The information signal *d(t)* is spread by the complex spreading sequence *c(t)* and then modulated on a carrier resulting in the final spread output [11]:

$$s(t) = d(t) \times c(t) \times \cos(2\pi f_{RF} t) \tag{6.1}$$

In code division multiple access (CDMA), the capacity is dependent on the amount of multi-user interference (MUI) that is present. During the despreading process in the receiver, both auto-correlation (AC) and cross-correlation (CC) functions are performed. The CC value is not necessarily zero, and therefore the spreading sequences of other users generate noise in the process of signal detection. CSS have optimal AC and CC values, and therefore result in minimum MUI [11]. The CSS used for this thesis are band limited and are constant envelope spreading sequences; this allows optimum power usage and longer battery life.

QPSK is used as the modulation scheme. The main reason for transmitting simultaneously on two carriers which are in quadrature is to conserve spectrum [59]. Spectrum is conserved since for the same total power the same bit error rate (BER) can be achieved using only half the power.

Several DSSS transceivers exist, however, patent [8] is a relatively recent filing, and to date the patent has been developed using a field programmable gate array (FPGA) and supporting discrete components only. A custom-chip design for such a transceiver is a complex art, and this thesis is a first attempt, to the knowledge of the filers of the patent [8], towards an on-chip implementation. To enable effective design, the relationship of a sub-system to the integrated system was conceptualized and tested mathematically using

SIMULINK/MATLAB. Some of the sub-systems had to be developed by first principles & others were designed by referral to extensive research [1-58] conducted elsewhere – the following sub-sections highlights some of the achievements [66; 69-70].

Biasing network design

The voltage references constitute the foundation of many of the sub-systems, thus their ability to remain constant is crucial to reliable operation in varying conditions. As expected, the threshold voltage, ΔV_{TH}, decreases for the NMOS transistor and increases for the PMOS transistor with increasing temperature. As seen in Figures 3.9 and 3.10, the bias circuit implemented shows limited deviation in reference voltages and currents from their values at room temperature.

Amplifier design

A telescopic amplifier was designed to achieve a unity gain bandwidth of just over 1 GHz and gain of about 65 dB. The choice of the amplifier was attributed to improved speed, better noise performance and low power consumption.

Mixer

A mixer with a conversion gain of about 10 dB and NF of about 15 dB was designed. The OIP3 and IIP3 were 7 dBm and 16.5 dBm respectively, proving sufficient for the system of this thesis.

LNA

The LNA used a source degenerated topology with which a minimum NF can be obtained. The core amplifier was realized using a differential topology. This topology has the advantage of rejecting common-mode noise components in a signal. The differential amplifier was realized by a transconductance amplifier, which drives a transresistance amplifier connected in a cascode topology. Due to the fact that the cascode topology was used, the high frequency response of the amplifier was enhanced.

Active inductor design & VCO

The current recycling method of the VCO design allows the system to be functional as a linearly adjustable oscillator. With an active inductor, the quality factor (and resulting VCO phase noise) can be improved. Inductor Q-factors as high as 50 (relatively higher than passive spiral inductor counterparts) can be obtained.

Comparator

A conventional two-stage comparator was designed. A modification (connecting the body of the transistors to the source) allowed the transistors to be more sensitive to changes at the gate inputs. For a load capacitor of 10 pF, a slew rate of 1000 V/μs was achieved.

Phase detector

The phase detector is an important part of the DDC-CRL. Figure 6.1 shows the phase detector output in the ideal case of an instantaneous response to a frequency error. Dashed lines indicate the phase detector output in the absence of phase inversion.

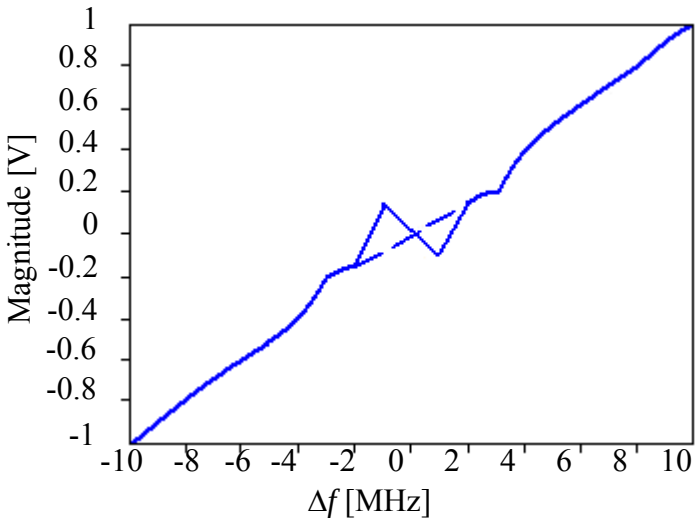


Figure 6.1.
Instantaneous response of phase detector with the effects of phase inversion shown in dashed lines.

Figure 6.2 is the simulated phase detector output of the DDC-CRL as a function of frequency deviation, dashed lines indicate the output in the absence of phase inversion.

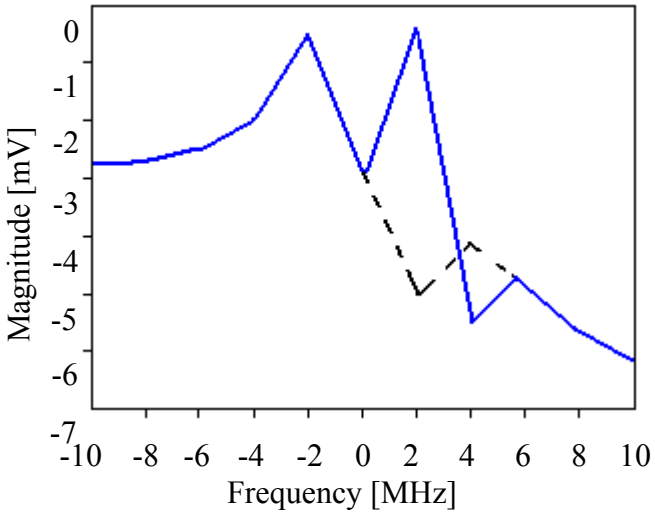


Figure 6.2.
Actual response of the DDC-CRL phase detector to a frequency error. Dashed lines indicate response without phase inversion.

Fig. 6.1 shows the phase detector output as a function of frequency deviation from ideal if the error signal is determined within one bit period. The change in polarity at 1 MHz is the phase detector's response to phase inversion. The dashed line indicates the output for no inversion. Phase inversion occurs when the difference term after demodulation causes the bit stream to invert, this inversion occurs in both branches. This causes the output of the phase detector to have correct magnitude, but incorrect polarity. Phase inversion in effect reverses the roles performed by each branch. Phase inversion is reduced by encoding the data using Manchester encoding, which has a DC average of approximately 0 V. The specification for the operating range of the DDC-CRL does not account for phase inversion, which will cause the loop to momentarily loose lock. Phase inversion can be forced to occur, as in Fig. 6.1 by allowing the difference term to be synchronized with the zero crossings of the bit stream, but also occurs for random bit streams as in Fig. 6.2.

The output characteristic of Fig. 6.1 is most desirable (without phase inversion) but is not achievable because the LPF settling time is several microseconds. The phase detector responds more readily to negative changes in frequency.

Similarly, Fig. 6.2 shows the simulated output of the phase detector once the DDC-CRL has stabilized to a step change in frequency. The simulation was conducted once the output of the LPF had settled to approximately DC after 8 μs. The dashed line represents the output if no phase inversion is present. In both cases, the phase detector is able to produce an error signal of correct polarity to drive the VCO's operating frequency towards the received signals frequency over a range of ±10 MHz, meeting the tracking range requirements of the DDC-CRL. The control voltage range is less than 300 mV.

The simulation of Figure 6.2 was performed with only frequency and not phase differences. The dashed line in Fig. 6.1 is plotted by inverting the output at 1 MHz difference. The dashed line in Fig. 6.2 is plotted using simulation results obtained by using a new random bit sequence in the model transmitter.

The larger apparent tracking range is caused by the non-linear relationship between the resonate frequency of the VCO's LC tank and the capacitive load used to control the resonate frequency. The relationship is approximately linear in the region of interest (2.39 GHz to 2.41 GHz), as this is the region in which the varactor behaves linearly to the control voltage. Outside this region, the varactor value saturates regardless of increased magnitude of the control voltage. This saturation level is used to limit the range of the VCO, but is too high to limit the VCO to within the desired range. Use of a smaller varactor with narrower tuning range is not possible, as the device model used is not valid for varactors smaller than the one currently in use.

Power Amplifier

A class F PA has been designed to achieve a gain of 25 dB (the gain was reduced to above 10 dB for this thesis). With the class F design, a PAE of about 80 % and a low THD was achieved. The class F amplifier design also required a negative voltage rail, this was designed using a ring oscillator, rectifier, filter and a voltage regulator.

Digital sub-systems

Several digital sub-systems were designed from first principles (albeit that they are conventional circuits). Some design simplification was done, for instance the D-Type FF was implemented using switches and inverters. Similarly, clock recovery was implemented

with edge detection and a counter (it was assumed that an external clock is available for the counter).

6.2 Future research work

While this thesis has laid a foundation for further integration of the DSSS modem, several iterations can be done to improve the overall design:

1. generation or storage of CSS on-chip (particularly longer sequences),
2. investigate the usage of alternative (different geometries) spiral inductors to achieve an enhanced Q-factor for the PA,
3. each sub-system could be independently and further optimised,
4. reduce the number of mixers to reduce the power dissipation,
5. conduct Monte-Carlo analysis for a deeper understanding of process variations, and impact thereof on the overall system, and
6. consideration of a different floor-plan and an electromagnetic analysis, for instance, laying out oscillators that are out-of-phase next to each other to achieve better common mode rejection.