CHAPTER 3: ANALOGUE SUB-SYSTEMS DESIGN

In the previous chapter, a systems level design was achieved for the transceiver proposed in this thesis. The aim of this chapter is to isolate, yet take inter-stage loading into account, and implement the various identified sub-systems using CMOS technology.

3.1 CMOS process parameters

The CMOS process used for this thesis is the AMS 0.35 µm process [28]. The C35B4C3 process allows for a minimum gate length of 0.35 µm, and has four metal layers and two layers of poly. A cross section of the wafer, shown in Figure 3.1 highlights the available layers and illustrates the layout of the transistor and capacitor modules. The process allows for n-channel MOSFETs (NMOS), p-channel MOSFETs (PMOS), resistors, capacitors, diodes and Zener diodes. Although the process does allow for BiCMOS fabrication[1] it is more expensive to produce, for this reason this thesis is limited to MOSFET implementation.

The most important parameters for design, as used in this thesis, are listed in tables 3.1 – 3.3. These and other process dependant details are protected by a non-disclosure agreement between the author and the University of Pretoria. For this reason the process parameters are not discussed in detail.

[1] BiCMOS refers to integrated circuits that include both MOSFETs and bipolar junction transistors (BJTs) in the same silicon substrate.

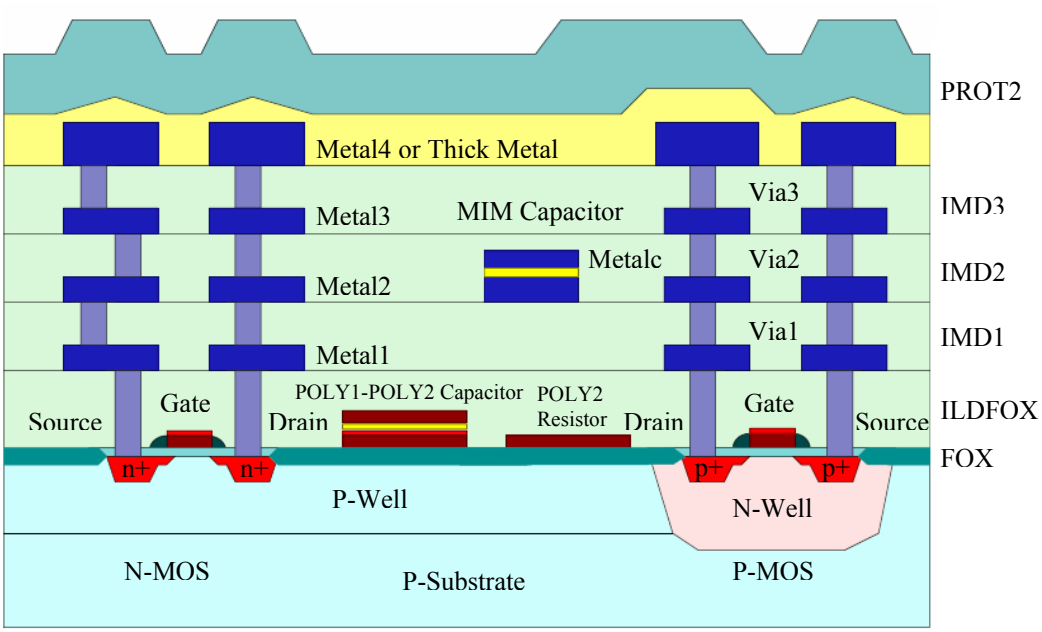


Figure 3.1.

A cross-sectional view of the AMS C35B4C3 process [28].

MOS Transistor	Max V_{GS} [V]	Max V_{DS} [V]	Max V_{GB} [V]	Max V_{DB} [V]	Max V_{SB} [V]
3.3 V NMOS / PMOS	3.6 (5) V	3.6 (5) V	3.6 (5) V	3.6 (5) V	3.6 (5) V

Table 3.1.

Operating ranges for the NMOS and PMOS transistors. The values in brackets denote the absolute maximum ratings [28].

NMOS				PMOS			
Parameter	Min	Typ	Max	Parameter	Min	Typ	Max
Long-channel (0.35) VTH [V]	0.36	0.46	0.56	Long-channel (0.35) VTH [V]	-0.48	-0.58	-0.68
Short-channel (10*0.35) VTH [V]	0.4	0.5	0.6	Short-channel (10*0.35)VTH [V]	-0.55	-0.65	-0.75
Effective channel length 0.35 µm	0.49	0.59	0.69	Effective channel length 0.35 µm	0.42	0.5	0.58
Effective channel width 0.35 µm	0.30	0.38	0.46	Effective channel width 0.35 µm	0.2	0.35	0.5
Body factor (γ) [V1/2]	0.48	0.58	0.68	Body factor (γ) [V1/2]	-0.32	-0.4	-0.48
Gain factor (KPn) [µA/V2]	150	170	190	Gain factor (KPp) [µA/V2]	48	58	68
Saturation current ID,sat [µA/µm]	450	540	630	Saturation current ID,sat [µA/µm]	-180	-240	-300
Effective mobility µo [cm2/Vs]	-	370	-	Effective mobility µo [cm2/Vs]	-	126	-

Table 3.2.

Summary of transistor parameters used in this thesis [28].

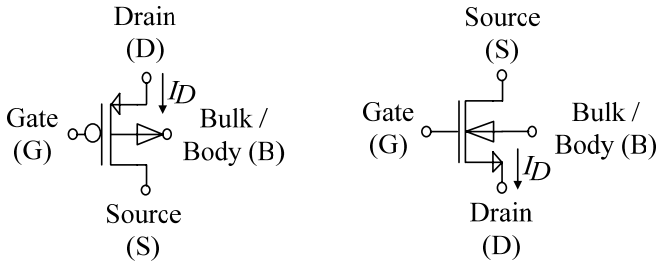
Resistance Parameters				Capacitance Parameters			
Parameter	Min	Typ	Max	Parameter	Min	Typ	Max
N-well sheet resistance [kΩ/□]	0.9	1.0	1.1	MOS varactor (CVAR) [fF/ µm^2]	2.40	3.01	3.61
N-well temp. coeff. (α) [10^{-3}/K]	-	6.2	-	Poly-1 – Poly-2 Capacitor			
Poly-1 sheet resistance [Ω/□]	-	8	11	CPoly area capacitance [fF/ µm^2]	0.78	0.86	0.96
Poly-1 temp. coeff. (α) [10^{-3}/K]	-	0.9	-	Cpoly perim capacitance [fF/ µm]	0.083	0.086	0.089
Poly-2 sheet resistance [Ω/□]	40	50	60	CPoly linearity [ppm/V]	-	85	-
Poly-2 temp. coeff. (α) [10^{-3}/K]	-	0.8	-				
RPOLYH sheet resistance [kΩ/□]	1.0	1.2	1.4				
RPOLYH temp. coeff.(α) [10^{-3}/K]	-	-0.4	-				

Table 3.3.

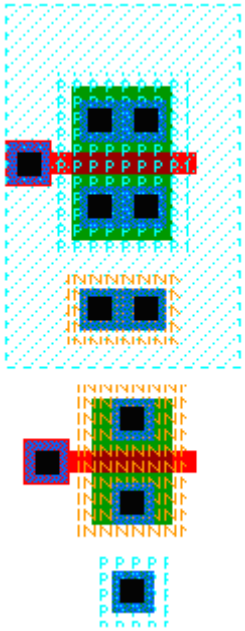
Summary of AMS parameters required for design of passive elements [28].

3.2 MOSFET summary

Since MOSFETs form the basis of this thesis, a short summary is provided in this section. The MOSFET is a four terminal device, as shown in Figure 3.2, including gate, drain, source and bulk terminals.



(a)



(b)

Figure 3.2.

(a) Symbols used to represent the PMOS (left) and NMOS (right) transistors.

(b) Layout of transistors: PMOS (top), and NMOS (below).

The MOSFET can be biased to work in one of two regions of operation, namely the triode or saturation region (including the sub-threshold region). These regions can be seen in the *I-V* characteristic of a MOSFET (Figure 3.3), where the gate-source voltage, v_{GS} is held constant at various values while the drain current, I_D, is measured for a sweep of the drain-source voltage v_{DS} (the PMOS operation is the same with symbols inverted i.e. v_{SG} for a PMOS is equivalent to v_{GS} for an NMOS).

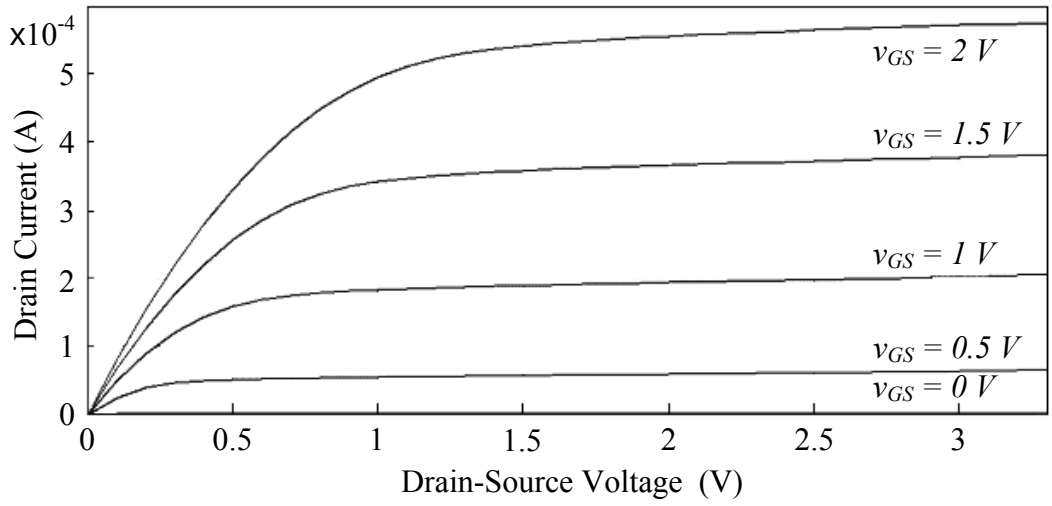


Figure 3.3.

A plot of the drain current, I_D, against a sweep of the drain-source voltage, v_{DS}, for increasing values of gate-source voltage, v_{GS}.

Operation in the triode region

This section describes equations used to relate i_D, v_{GS}, and v_{DS} [29]. There exists a capacitance between the gate and the inversion layers due to the oxide between the two layers.

This oxide capacitance per unit area can be calculated using

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.1}$$

where ε_{ox} represents the SiO_2 dielectric constant and t_{ox} is the thickness of the oxide layer.

The exact value of this capacitance, C_{ox}, can be calculated as

$$C_{ox} = C'_{ox} \cdot A = C'_{ox} \cdot WL \tag{3.2}$$

The transconductance parameter KP is defined for an NMOS device as

$$KP_n = \mu_n \cdot C'_{ox}, \tag{3.3}$$

and for a PMOS device

$$KP_p = \mu_p \cdot C'_{ox} \tag{3.4}$$

Thus for an NMOS device operating in the triode region the current flowing into the drain of the device can be shown to be

$$I_D = KP_n \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right] = \mu_n \cdot C'_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3.5}$$

where V_{THN} is the threshold voltage for an NMOS transistor. Note that equation (3.5) is only valid for $V_{GS} \geq V_{THN}$ and $V_{DS} \leq V_{GS} - V_{THN}$. The equation for a PMOS transistor is identical if each parameter is replaced with the PMOS equivalent parameter.

Operation in the saturation region

When $V_{DS} \geq V_{GS} - V_{THN}$ the NMOS moves into the saturation region, as the channel formed under the gate oxide starts to "pinch off" and further increase in current is not possible. The value of V_{DS} at which this occurs (when the inequality is equal) is defined as $V_{DS,sat}$. Ignoring the effects of channel length modulation (included in Equation 3.7) and assuming V_{GS} remains constant, any increase in V_{DS} beyond this level does not cause an increase in the drain current. The drain current for an NMOS operating in the saturation region is given by

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{THN}\right)^2 \tag{3.6}$$

for $V_{GS} \geq V_{THN}$ and $V_{DS} \geq V_{GS} - V_{THN}$. This equation is generally referred to as the "square-law" equation for MOSFETs.

The assumption that once the channel becomes "pinched off" at the drain end, further increases in V_{DS} have no effect on the channels shape is an ideal one. In practice, increasing V_{DS} beyond its saturation point moves the "pinched off" region closer to the source, and in effect, the channel length is reduced. This is referred to as channel-length modulation. Equation (3.6) can be altered to include the effect of channel length modulation as

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{THN}\right)^2 \left[1 + \lambda \left(V_{DS} - V_{DS,sat}\right)\right] \tag{3.7}$$

This equation makes another assumption, and that is that the effective mobility of the majority carrier (μ_n in this case) remains uniform. This assumption is valid for transistors with longer channel lengths, however in short channel MOSFETs the change in mobility can no longer be ignored.

Short-channel MOSFETs

In short-channel MOSFETs the main difference in operation occurs because the carriers drifting between the channel and drain of the MOSFET saturate in an effect called carrier velocity saturation, or v_{sat}. This results in a reduction in the hole or electron mobility which increases the channels effective sheet resistance.

While the velocity at low field values is governed by Ohm's law (also implying $v \propto E$), the velocity at high field values approaches a constant called the scattering-limited velocity [29; 57], v_{scl}. A first order analytical approximation to this curve is [57]

$$v_d = \frac{\mu_n E}{1 + \frac{E}{E_{critical}}}, \tag{3.8}$$

where the critical field, $E_{critical}$ is approximately 1.5 MV/m and $\mu_n = 0.07$ m^2/V-s.

As $E_{critical} \to \infty$, $v_d \to v_{scl} = \mu_n E_{critical}$. At the critical field value, the carrier velocity is a factor of 2 less than the low-field relationship would predict. It is further shown [57] that, in the active region,

$$V_{DS(act)} \to (V_{GS} - V_{THN}), \tag{3.9}$$

for $E_{critical} \to \infty$.

The drain current in the active region with velocity saturation is given by [57]

$$\lim_{E_{critical} \to \infty} I_D = \mu_n C_{ox} W (V_{GS} - V_{THN}) E_{critical} = C_{ox} W (V_{GS} - V_{THN}) v_{scl} \tag{3.10}$$

The implication of this is that for short channel MOSFETs, the current I_D is linearly related to the overdrive voltage, $V_{GS} - V_{THN}$.

3.3 Bias network design

By creating a basic list that can be used as a premise for design, the process of creating subsequent modules is somewhat simplified, in that it has a basis on which it can build. Building these parameters was based on the square-law equation for transistors and since the specification for the thesis is low-voltage, the transistors were designed to be operated in the saturation region with minimum excess gate-source voltage (also known as overdrive voltage, V_{OD}). Since the transistor was not pushed too far into the saturation region, channel length modulation was ignored for the basic design, unless otherwise mentioned.

NMOS design parameters

The design is based on a width to length ratio (aspect ratio) of 5/1, this was chosen so that if the *W/L* ratio needed changing later in the design there was room for this. The length was designed to be a minimum to ensure greater achievable speeds (as the same aspect ratio will be used for some other sub-systems later on). Thus for the 0.35 µm process the following ratio was used for the basic NMOS transistor

$$\left(\frac{W}{L}\right)_n = \frac{5}{1} = \frac{1.75\mu m}{0.35\mu m} \tag{3.11}$$

To begin to calculate the required variables for the square law equation each of the required parameters needed to be evaluated. The dielectric constant of SiO_2 is given by

$$\varepsilon_{ox} = \varepsilon_r \varepsilon_0 = 3.97\varepsilon_0 = 35.1511\, pF/m \tag{3.12}$$

where ε_r is the relative dielectric constant for SiO_2 and ε_0 the vacuum dielectric constant.

The thickness of the SiO_2 was obtained from the AMS process parameters and thus the oxide capacitance can be calculated as

$$\begin{aligned} t_{ox} &= 7.575\ nm \\ \therefore C'_{ox} &= \frac{\varepsilon_{ox}}{t_{ox}} = 4.64\ \frac{fF}{(\mu m)^2} \end{aligned} \tag{3.13}$$

The electron mobility coefficient is also defined in the AMS process parameters model as $\mu_n = 370\ cm^2/V \cdot s$. Using this along with the oxide capacitance in (3.13) the transconductance gain parameter KP_n can be calculated as

$$\begin{aligned} KP_n &= \mu_n C'_{ox} = \left(47.58\times10^{-3}\right)\left(370\times10^{-5}\right) \\ &= 176.05\ \mu A/V^2 \end{aligned} \tag{3.14}$$

which corresponds to the typical mean value as given in the process parameters. Using $V_{THN} = 0.4979\ V$ as defined in modn.md[2] and in the process parameters, along with the values calculated above and the required voltages, basic transistor biasing can be done by looking at the *I-V* transfer characteristic for a sweep of v_{GS}. The circuit setup is shown in Figure 3.4, and the *I-V* characteristic is shown in Figure 3.5.

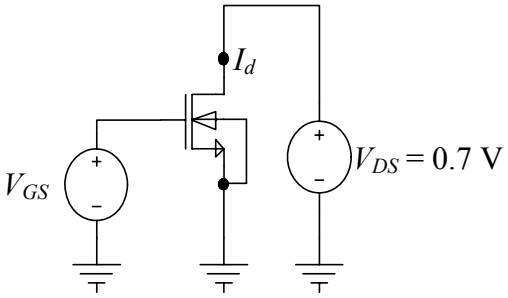


Figure 3.4.

Setup used to obtain the *I-V* characteristic for the NMOS transistor, with v_{DS} held constant at 0.7 V.

[2] modn.md is the model file used by T-Spice to simulate the AMS transistor.

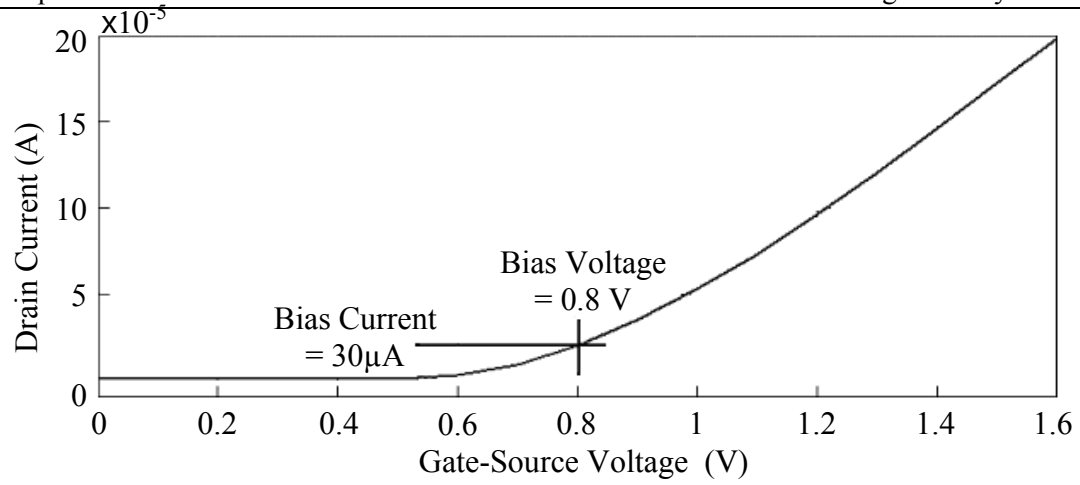


Figure 3.5.

Drain current for a sweep of the gate-source voltage with the drain-source voltage held constant at 0.7 V.

It was decided to use a biasing drain current of I_D = 30 µA to keep the transistors in the saturation region while consuming a minimum amount of power (since the power consumption is related to the current by $P = VI$). Thus the V_{GS} required to obtain I_D = 30 µA can be calculated as

$$V_{GS} = \sqrt{\frac{2I_D}{KP_n}\left(\frac{L}{W}\right)_n} + V_{THN} \cong 0.8\ V \tag{3.15}$$

and, $V_{DS,sat} = V_{GS} - V_{THN} = 261.08\ mV = V_{OD}$.

PMOS design parameters

Similar results hold for the PMOS transistor if the width of the transistor is adjusted therefore only the major differences are discussed here. Since the mobility of holes is lower than that of electrons, the width of the PMOS is usually adjusted to account for this and keep operation of the two devices similar. The width and length of the PMOS can be calculated using the adjustment factor given by,

$$\frac{\mu_n}{\mu_p} = \frac{370\,cm^2/V\cdot s}{126\,cm^2/V\cdot s} = 2.94 \cong 3 \tag{3.16}$$

Thus the width of the PMOS should be related to that of the NMOS by,

$$\left(\frac{W}{L}\right)_p = 3\left(\frac{W}{L}\right)_n$$

$$\therefore W_p = 3W_n \tag{3.17}$$

So the *W/L* ratio of the PMOS is given by,

$$\left(\frac{W}{L}\right)_p = \frac{15}{1} = \frac{5.25\mu m}{0.35\mu m} \tag{3.18}$$

The only other parameter that differs for the PMOS transistor is the threshold voltage, V_{THP}. A summary of both the NMOS and PMOS parameters used in the design process for biasing networks in this thesis is shown in table 3.4.

Parameter	NMOS	PMOS	Additional
Bias Current, I_D	30 µA	30 µA	From Figure 3.5
W/L	5/1	15/1	$\mu_n/\mu_p \approx 3$
Actual	1.75 µm/ 0.35 µm	5.6 µm/ 0.35 µm	L = 0.35 µm
V_{TH}	0.4979 V	0.6842 V	Typical Mean
KP	176 µA/V^2	58 µA/V^2	
$C_{ox} = \varepsilon_{ox}/t_{ox}$	4.64 mF/m^2	4.64 mF/m^2	t_{ox} = 7.575 nm
$\lvert V_{GS}\rvert$	0.8 V	0.92 V	From Figure 3.5
$\lvert V_{DS,sat}\rvert$	261 mV	260 mV	$V_{DS,sat} = V_{GS} - V_{THN}$

Table 3.4.

Summary of transistor parameters used for the biasing network.

The bias network is important part of the system for this thesis, since for components to function as designed their biasing voltages must remain stable and must start up to the correct value [30, 31]. The design starts with designs for current mirrors and then moves onto the beta-multiplier and finally a full biasing networks.

Current mirror

The most basic form of a current mirror is shown in Figure 3.6. In this circuit the resistor, *R*, is used to generate a reference current which is 'mirrored' through the second NMOS – M2. As will be shown the amount of current the mirror is able to sink is dependant on the width ratios of M1 and M2. The connection of the gates to the drain of M1 is referred to as a "diode" connection, since the transistor will always operate in the saturation region.

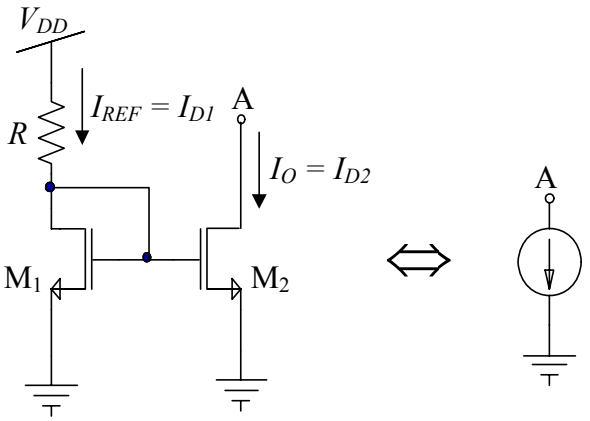


Figure 3.6.

Basic circuit schematic of a simple current mirror, and its equivalent representation.

From Equation (3.6) the following can be derived

$$I_{REF} = \frac{KP_n}{2} \cdot \frac{W_1}{L_1} \cdot \left(V_{GS1} - V_{THN}\right)^2$$
$$I_O = \frac{KP_n}{2} \cdot \frac{W_2}{L_2} \cdot \left(V_{GS2} - V_{THN}\right)^2 \qquad (3.19)$$
$$\frac{I_{REF}}{I_O} = \frac{\frac{W_1}{L_1} \cdot \left(V_{GS1} - V_{THN}\right)^2}{\frac{W_2}{L_2} \cdot \left(V_{GS2} - V_{THN}\right)^2}$$

Since the gates of M1 and M2 are connected and both of their sources go to ground, $V_{GS2} = V_{GS1}$, and therefore I_O is related to I_{REF} by (letting $L_1 = L_2$)

$$I_O = \frac{W_2}{W_1} I_{REF} \qquad (3.20)$$

This current source offers a good method of sinking current if supply voltage, V_{DD}, is constant and the resistor remains at a constant temperature. In general, however, the voltage supply will not always be constant and the value of the resistor depends on various factors, like process variations and changes in temperature. Therefore a reliable supply independent current reference is required.

Beta-multiplier circuit

If the resistor is placed on the source side of the current mirror instead of the drain side, it becomes isolated from the influence of the power supply. Also adding a PMOS mirror forces the same current through each channel, making the voltage reference far less dependant on the value of the resistor, and thus less dependant on variations in

temperature. Figure 3.7 shows the schematic of the beta multiplier circuit, including a start-up circuit to ensure the system starts up with the correct levels (imbalance in the mirror could turn one of the current mirrors off and the other on sending the references to either V_{DD} or ground).

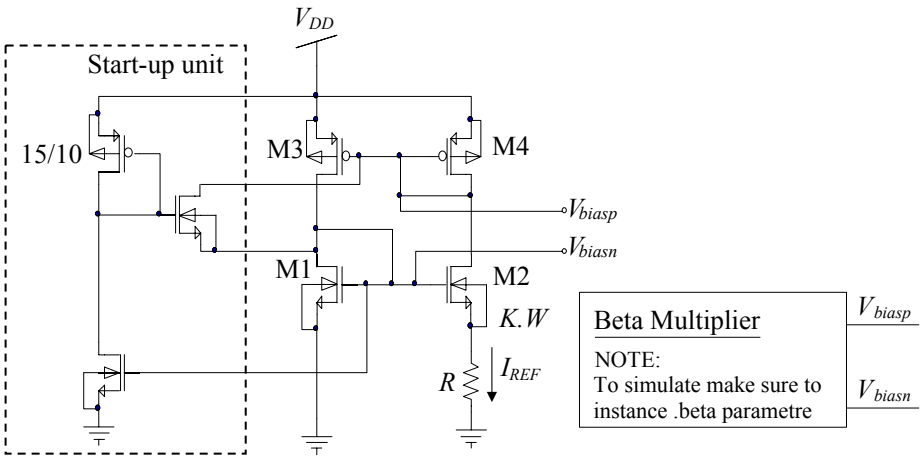


Figure 3.7.

Circuit schematic for a beta-multiplier including the start-up circuitry and the symbol used for instancing the circuit. All unlabelled NMOS and PMOS transistors have aspect ratios of 5/1 and 15/1, respectively. $V_{biasp} = V_{bp}$ & $V_{biasn} = V_{bn}$.

Since the current flowing through the resistor is forced to I_{REF} by the PMOS current mirror the gate-source voltage of M1 can be written as

$$V_{GS1} = V_{GS2} + I_{REF} \cdot R \tag{3.21}$$

For this to be valid V_{GS1} must be greater than V_{GS2}, and to ensure this a larger value of β is required[3], since

$$V_{GS} = \sqrt{\frac{2I_D}{\beta}} + V_{THN} \tag{3.22}$$

The length of the transistors is already a minimum and the transconductance parameter is constant, the relation of $\beta_2 = K\beta_1$ must therefore be satisfied by letting $W_2 = KW_1$. From this, the reference current through M2 can be expressed as,

$$I_{REF} = \frac{2}{R^2 KP_n \cdot \frac{W_1}{L_1}}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \tag{3.23}$$

If K = 4 & I = 30 µA, and Equation 3.23 solved using the design parameters from Table 3.4, R can be found to be 4.35 kΩ.

[3] β is often used to represent the multiplicand of $KP \cdot W/L$ hence the name 'Beta-multiplier'.

Full biasing network

Using cascode[4] current mirror loads (e.g. the folded cascode and telescopic amplifiers) can increase the amplification of a differential gain circuit. To use a differential output, as required by other sub-systems of this thesis, each level of the cascode needs to be precisely biased to ensure all transistors operate in the saturation region.

The design is basically an extension of the beta-multiplier circuit, where the reference voltage of the NMOS transistor is first used to drive a PMOS cascode current mirror, and then used in an NMOS cascode current source.

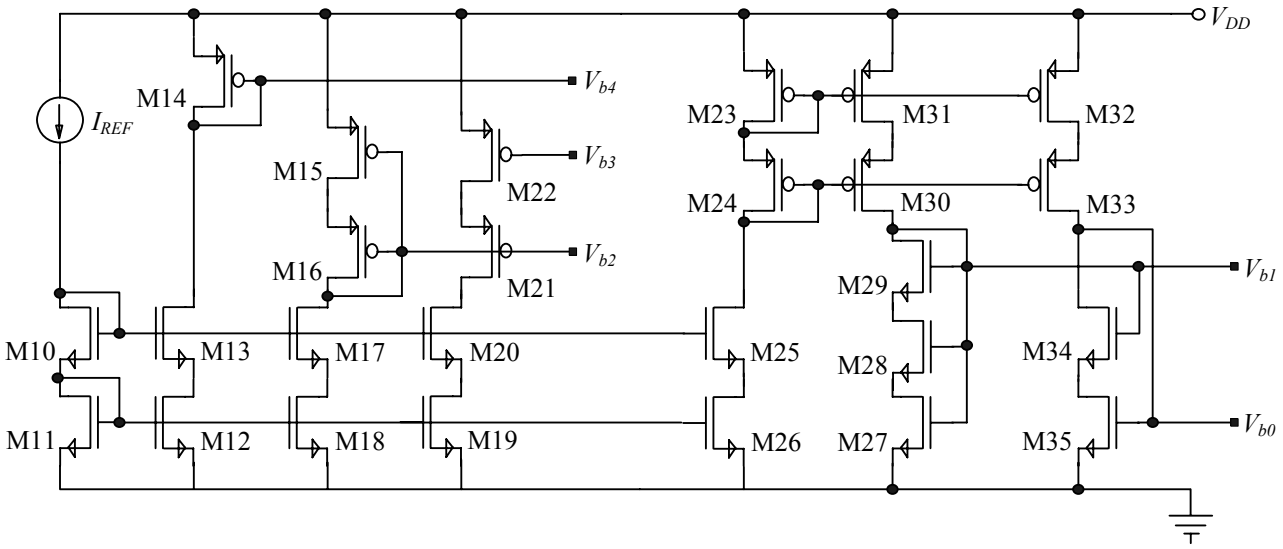


Figure 3.8.
Circuit schematic of the bias network used in this thesis. All unlabelled NMOS and PMOS transistors have aspect ratios of 5/1 and 15/1, respectively.

The basic concept of its operation is based on using various stages of current mirrors to keep "mirroring" the I_{REF} from the beta-multiplier. Since I_{REF} is mirrored through the PMOS and NMOS cascode current mirror structures and since they are diode connected, their gate voltages can be used to mirror the same current in other structures which therefore do not need to be diode connected to operate in the saturation region. This fact is important, because since the transistors can run off the voltages generated by the bias network, the output of an amplifier using this bias scheme can be taken differentially [30].

[4] The term 'cascode' originated in the days of using vacuum tubes. It is an acronym for "cascaded triodes".

Operating temperature range of reference voltages

Figure 3.9 shows the plotted results of a temperature sweep simulation of the beta-multiplier circuit of Figure 3.7.

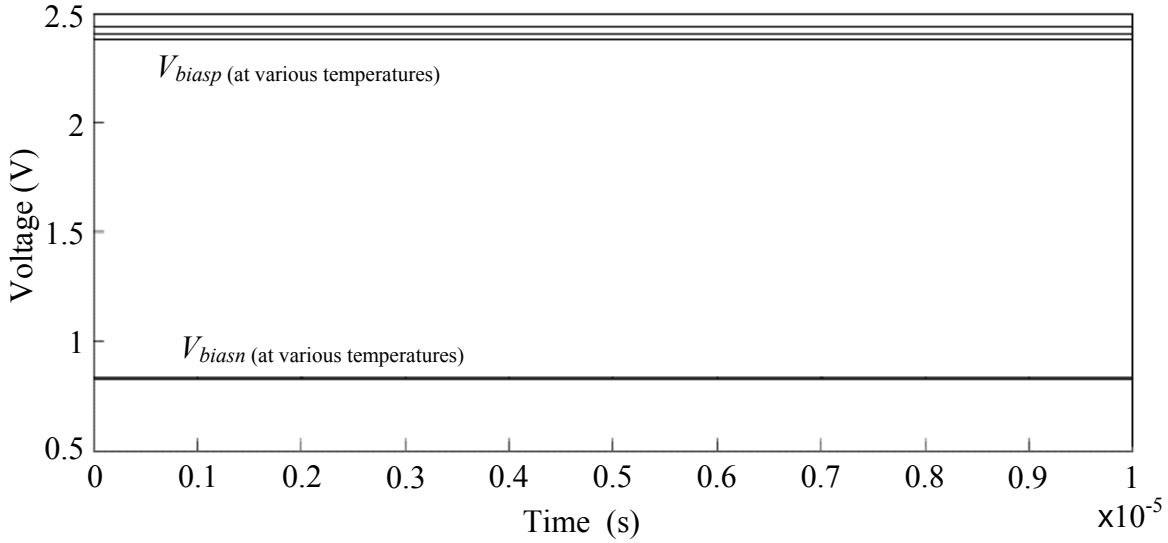


Figure 3.9.

Temperature sweep transient simulation for the beta-multiplier.

Table 3.5 summarizes the results for various temperatures.

Parameter	***-10 °C***	***25 °C***	***70°C***
V_{biasn}	***0.828 V***	***0.8261 V***	***0.8244 V***
V_{biasp}	***2.377 V***	***2.402 V***	***2.438 V***

Table 3.5.

Bias values measured for the commercial range.

Figure 3.10 displays the variation in bias current with temperature.

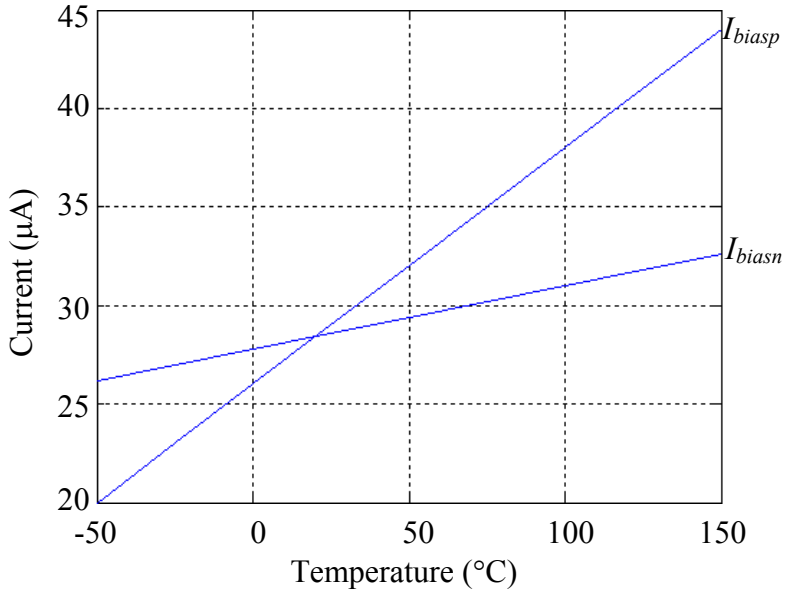


Figure 3.10.

Temperature sweep performed on the Beta-Multiplier to display the bias currents.

Table 3.6 records the various bias voltages obtained from Fig. 3.8.

Parameter	*-10 °C*	*25 °C*	*70°C*
V_{b4}	*2.212 V*	*2.221 V*	*2.23 V*
V_{b3}	*1.852 V*	*1.862 V*	*1.872 V*
V_{b2}	*1.382 V*	*1.344 V*	*1.308 V*
V_{b1}	*0.9423 V*	*0.9339 V*	*0.9263 V*
V_{b0}	*0.881 V*	*0.883 V*	*0.884 V*

Table 3.6.

Values obtained from simulation of the bias circuit for selected temperatures in the commercial temperature range.

Since the voltage references constitute the foundation for the entire system, their ability to remain constant is crucial to reliable operation in varying conditions. As expected, the threshold voltage, V_{TH}, decreases for the NMOS transistor and increases for the PMOS transistor with increasing temperature.

3.4 Amplifier design

For large amplification and improved bandwidth qualities the differential CMOS amplifier with active loads are the most effective amplifier topologies.

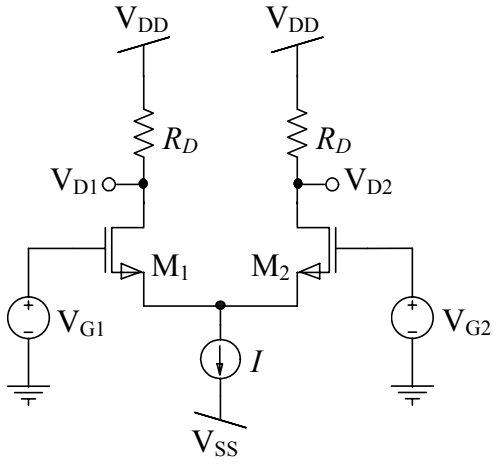


Figure 3.11.

Basic MOS differential-pair configuration.

In the design of fully differential operational amplifiers, several different topologies exist that build on the basic differential amplifier topology (which is shown in Figure 3.11). The advantages and disadvantages of various topologies are described in table 3.7 [32].

	Gain	Speed	Output Swing	Noise	Power Consumption
Telescopic	Medium	Highest	Low	Low	Low
Folded- Cascode	Medium	High	Medium	Medium	Medium
Multistage	Highest	Low	Highest	Low	Medium
Gain-Boosted	High	Medium	Medium	Medium	High

Table 3.7.

Amplifier topologies and their properties [32].

The design of complex amplifier circuits requires complex biasing circuitry and analysis of the transistors used and their DC operating points.

The output of an amplifier can be defined, generically, in terms of its common-mode and differential-mode gain as

$$v_O = A_d v_{ID} + A_{cm} v_{IC} \tag{3.24}$$

where A_d represents the differential-mode voltage gain and A_{cm} represents the common-mode voltage gain, [31]. The differential-mode input voltage, v_{ID}, and the common-mode input voltage, v_{IC} are defined in terms of the differential input pair $v_{I1(G1)}$ and $v_{I2(G2)}$ as stated below.

$$v_{ID} = v_{I1} - v_{I2} \tag{3.25}$$

$$v_{IC} = \frac{v_{I1} + v_{I2}}{2} \tag{3.26}$$

The common-mode rejection ratio (CMRR) is then defined by

$$CMRR_{dB} = 20\log\left(\frac{A_d}{A_{cm}}\right) \tag{3.27}$$

In designing an amplifier for high-speed, low-power applications, the telescopic and folded cascode structures are two of the most commonly used topologies [33-35]. The challenge in designing the amplifier lies in managing trade-offs between the various topologies, including required speed, gain, power usage and die size. From the basic topologies that exist in literature, minor variations can be made to improve the operation of the amplifier to meet the specifications and requirements that are dictated by its intended application.

Amplifiers are generally used with feedback to improve stability, increase bandwidth and to control amplification [31]. The general structure of a feedback amplifier is shown in Figure 3.12.

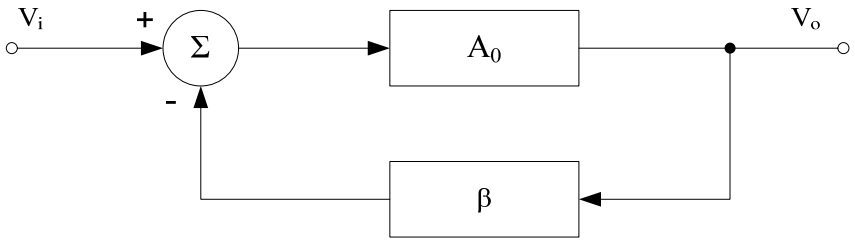


Figure 3.12.
General structure of a feedback amplifier in a signal flow diagram.

The feedback of the amplifier is defined by the feedback factor β. The open loop gain of the amplifier, A_o, is the gain of the amplifier when there is no feedback structure in place ($\beta = 0$). The closed loop gain of the amplifier can be shown to be

$$A_f \equiv \frac{v_O}{v_I} = \frac{A_o}{1 + A_o\beta} \tag{3.28}$$

The quantity $A_o\beta$ is called the loop gain and for the feedback to be negative (required for the amplifier to be stable), this quantity must be positive. If the open loop gain A_o is large then the loop gain $A_o\beta$ will also be large ($A_o\beta \gg 1$) and thus the amplification can be approximated as

$$A_f \cong \frac{1}{\beta} \tag{3.29}$$

which implies that the gain of the feedback amplifier is almost entirely determined by the feedback network.

Basic differential amplifier

The operation of a differential pair can be described, with reference to Figure 3.11. Assuming that v_{G1} - v_{G2} varies from -∞ to +∞. If v_{G1} is much more negative than v_{G2} then M1 turns off and M2 turns on. Then the current through M2 is equal to the current drawn by the biasing current source. As v_{G1} is brought gradually closer to v_{G2} M1 starts to turn on and starts to draw some of the current from the biasing source and thus starts to lower v_{D1}. The same happens in the opposite direction. Thus, because the current through each side of the amplifier varies between 0 and I_{MAX}, the output voltage varies between 0 and $I_{MAX} \cdot R$.

The implication of this is that the amount of gain that the amplifier can produce is proportional to the load resistance and the bias current it uses. Since increasing the bias current of the amplifier will increase its power consumption, the gain is improved by increasing the load resistance.

Using a PMOS current source load instead of a resistive load can provide a much larger load using a smaller area in the silicon. This was implemented as shown in Figure 3.13 (a).

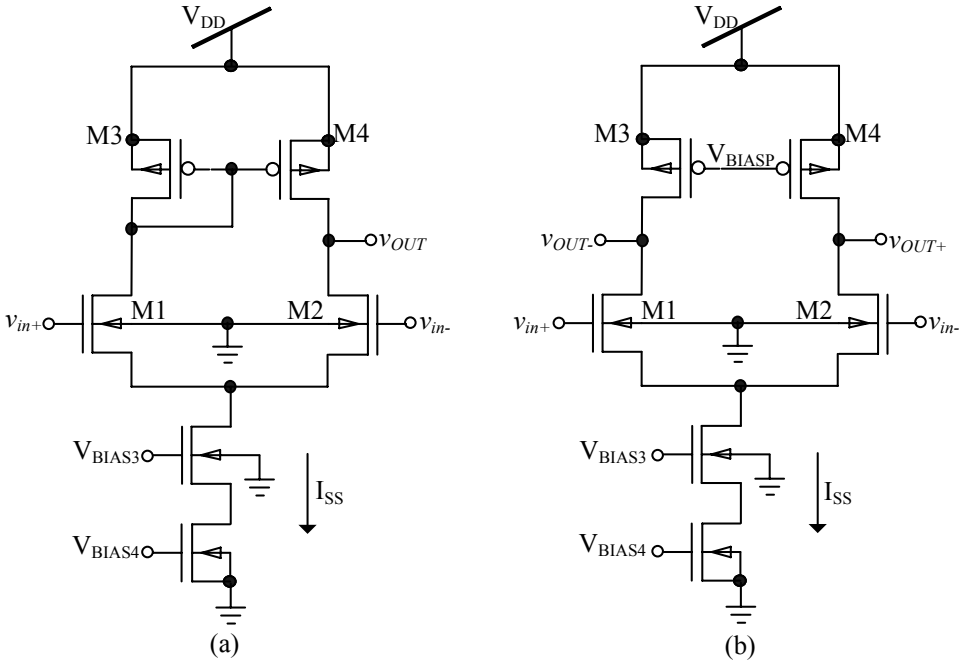


Figure 3.13.

(a) Circuit schematic of the single-ended differential amplifier.

(b) Circuit schematic of a fully differential amplifier.

All unlabelled NMOS and PMOS transistors have aspect ratios of 5/1 and 15/1, respectively. The complete biasing circuitry has not been shown, since these circuits were not eventually used.

Although this circuit offers mild open loop gain, when used with a feedback network the open loop gain is not high enough to warrant its implementation. The open-loop gain of this amplifier (Fig. 3.13 (a)) is given by

$$A_v = -g_{mN}\left(r_{ON} \parallel r_{OP}\right) \tag{3.30}$$

In Figure 3.13 (b) the circuit was changed to allow for a differential output. This was achieved by removing the diode connection on the PMOS current mirror, and instead, connecting the gates to the PMOS current mirror in the beta-multiplier circuit (see Figure 3.7). Figure 3.14 shows the voltage transfer characteristics for both of these circuits.

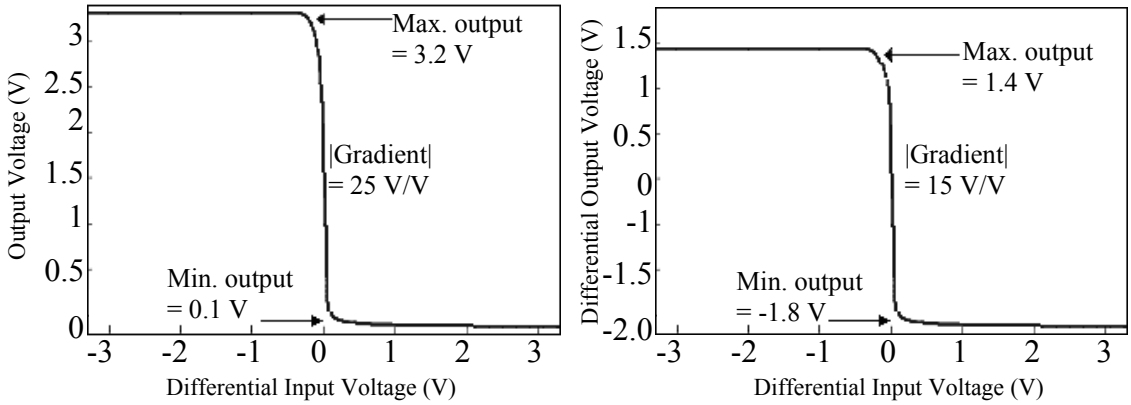


Figure 3.14.

Voltage transfer characteristics for both the single-ended and the fully differential amplifiers.

The above amplifier showed a gain of less than 40 dB, which is not adequate for all sub-systems of this thesis, hence a higher gain amplifier was also designed (as below).

Telescopic amplifier

The telescopic amplifier is a form of cascode amplifier. It employs both a PMOS cascode current source load, and an NMOS current source load, to create a gain using NMOS differential pair. As discussed in table 3.7, this amplifier topology is able to produce high gain but a relatively limited signal swing. The gain of this amplifier is given by

$$A_v = \frac{v_{out}}{v_{in}} = g_{mN}\left[\left(g_{mN}r_{ON}^2\right)\|\left(g_{mP}r_{OP}^2\right)\right] \tag{3.31}$$

where g_{mN} is the small signal gain of the NMOS transistor, g_{mP} is the small signal gain of the PMOS transistor, r_{ON} is the small signal resistance of the NMOS transistor and r_{OP} is the small signal resistance of the PMOS transistor. For a transistor with I_D = 30 µA, and a $v_{DS,sat} = v_{SD,sat}$ = 260 mV, then the small signal gain of the PMOS and NMOS transistors is given by

$$g_m = \frac{W}{L}\cdot KP\cdot V_{DS,sat}$$

$$\therefore g_{mN} = \left(\frac{5}{1}\right)(176)(0.26) = 228.8\mu A/V \tag{3.32}$$

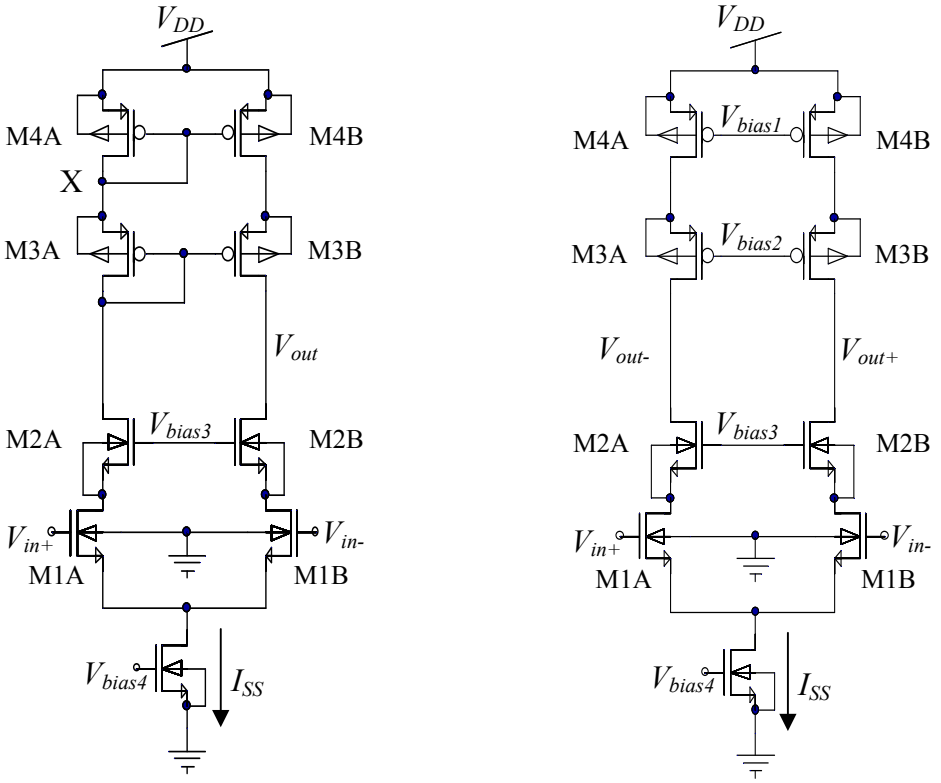
$$\therefore g_{mP} = \left(\frac{15}{1}\right)(58)(0.26) = 226.2\mu A/V \tag{3.33}$$

The values of r_O can be calculated using the channel length modulation factor, λ, being 0.03 V^{-1} for NMOS and 0.08 V^{-1} for PMOS, as specified by CMOS process parameters. So r_O can be calculated as

$$r_O = \frac{1}{\lambda I_D} \tag{3.34}$$

which gives $r_{Op} = 416.67\ k\Omega$ and $r_{On} = 1.11\ M\Omega$, thus using (3.32) the ideal open loop gain of the circuit is approximately 70 dB.

Figure 3.15 shows the schematics of the telescopic amplifier implemented in single-ended and in differential topologies. At node X in the single-ended topology, the circuit suffers from a mirror pole[5] which causes stability issues. This is not of concern in this thesis as the single-ended topology was not implemented. The advantages of the telescopic amplifier include, a very high gain for a one-stage amplifier, and high-speed (large GBW), however it suffers from limited output swing voltage and does not operate very well in unity gain configurations.



(a) (b)

Figure 3.15.

(a) Single-ended differential telescopic amplifier

(b) Fully differential telescopic amplifier.

Simulations of this circuit (Figure 3.16) show a much higher gain than that obtained for the simple differential amplifier, but not quite at the ideal level. This deviation from the ideal

[5] Poles and zeros are used to analyse the stability of a circuit

can be attributed to the non-ideal current source and the fact that the CMOS process utilised borders on being a short-channel process which (as mentioned in Section 3.1) has a different *I-V* relationship to long-channel processes.

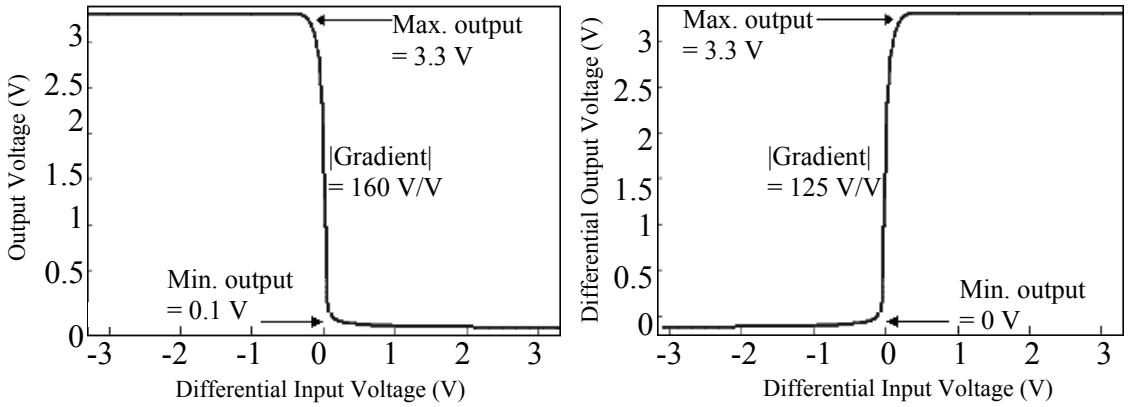


Figure 3.16.

Voltage transfer characteristics for the single ended (left) and the fully differential (right) telescopic amplifiers.

This design can be significantly improved by using a second stage to increase the output swing of the amplifier.

Two-stage telescopic amplifier

The design of this amplifier builds on a telescopic first stage [32]: This paper presented a highly customisable, high-gain differential CMOS amplifier with a large unity gain bandwidth. The design was adjusted for the requirements for this thesis but the 2nd stage topology (shown in Figure 3.17) was utilised. Since the second stage of the amplifier is just a common-source configuration the gain of this amplifier can be calculated as

$$|A_v| = A_{v1}A_{v2} = g_{mN}\left(r_{ON} \parallel r_{OP}\right) \cdot g_{mN}\left[\left(g_{mN}r_{ON}^2\right) \parallel \left(g_{mP}r_{OP}^2\right)\right] \tag{3.35}$$

which can be approximated as

$$|A_v| = {g_{mN}}^2\left(r_{ON} \parallel r_{OP}\right)^2 \tag{3.36}$$

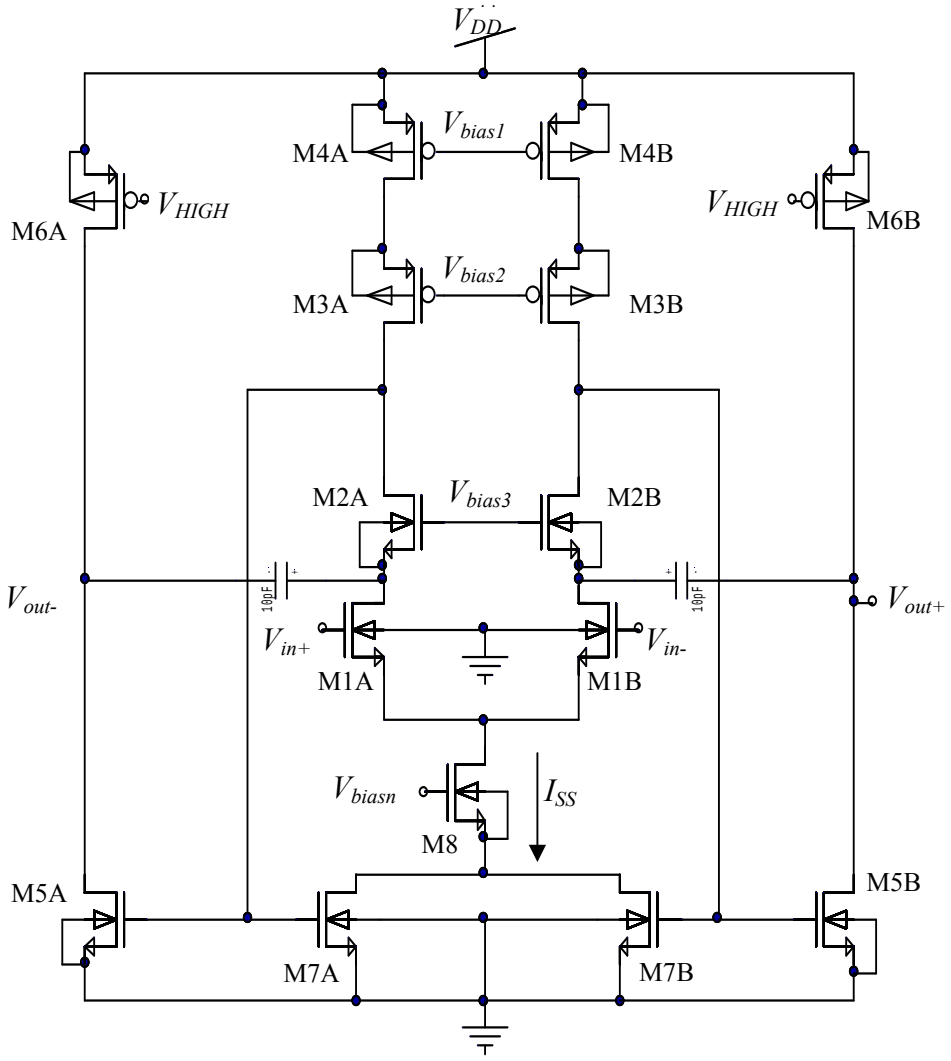


Figure 3.17.

Circuit schematic of the two-stage telescopic amplifier [68].

Since offset, which is a source of non-linearity, can be increased between the two stages, two offset reduction techniques are employed in this circuit. The first method is the introduction of coupling capacitors between the stages, and the second through the use of internal feedback. In Figure 3.17 it can be seen that the output of the first amplifier stage is directed back into the NMOS pair M7A and M7B. Both of these transistors operate in the triode region for tuning of the tail-current.

Feedback analysis

From (3.28) the closed loop gain of an amplifier is given by

$$A_f \equiv \frac{v_O}{v_i} = \frac{A_o}{1 + A_o \beta} \tag{3.37}$$

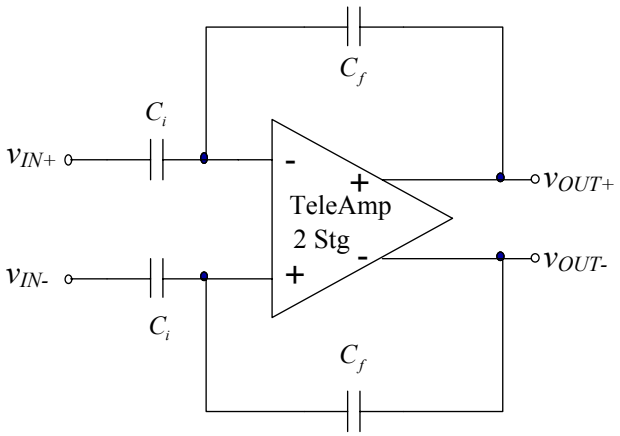


Figure 3.18.

Feedback configuration used with the two stage telescopic amplifier.

The feedback of this system utilises capacitive feedback. For the feedback configuration shown in Figure 3.18, the closed loop gain can be written as [31]

$$A_f = \frac{C_i}{C_f}\frac{A_v}{\beta^{-1} + A_v} \tag{3.38}$$

where C_i is the input capacitance, C_f is the feedback capacitance and β is the feedback factor given by

$$\beta = \frac{C_f}{C_i + C_f} \tag{3.39}$$

Since $A_v\beta \gg 1$ the gain of the feedback structure can be approximated as

$$A_f = \frac{C_i}{C_f}\left(1 - \frac{1}{\beta A_v}\right) \tag{3.40}$$

The factor $1/\beta A_v$ is referred to as the settling accuracy (ε_s) of the amplifier. Solving this for C_f to yield a closed loop gain of 2, with the open loop gain being 1000 V/V and choosing C_i = 1 pF yields C_f = 0.5 pF.

The layout of the telescopic amplifier is shown in Figure 3.19.

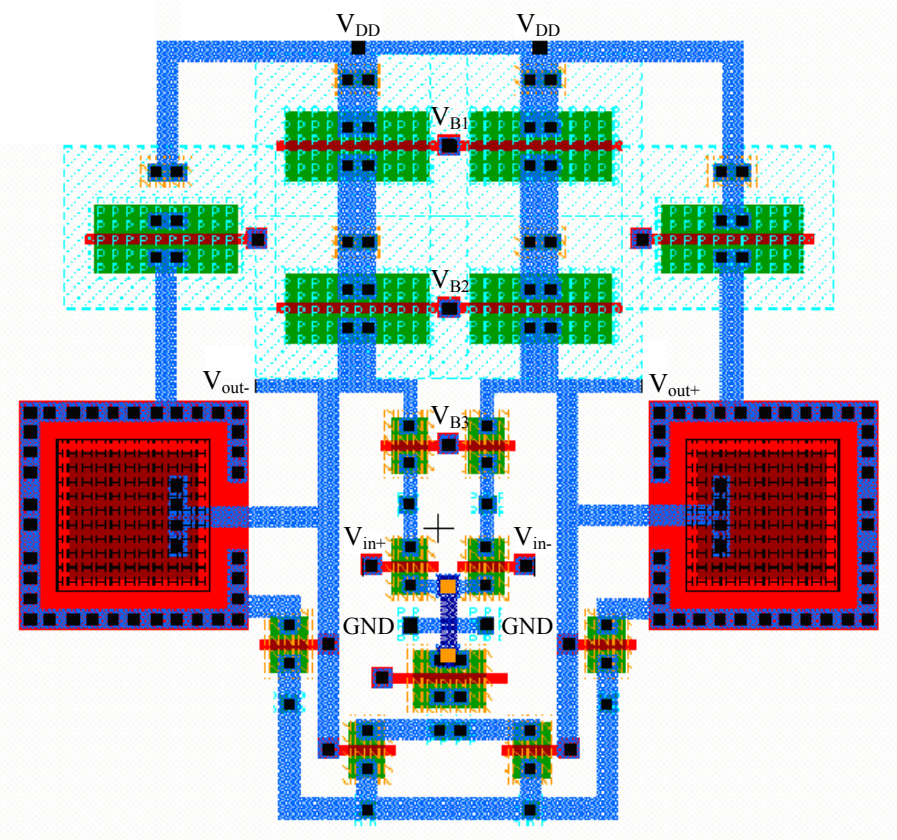


Figure 3.19.

Circuit layout for the two stage telescopic amplifier.

Simulation results

Figure 3.20 shows that the amplifier has a very steep transfer curve. To calculate the gain of the circuit the gradient of the transfer curve in its linear region was calculated using the equation for a straight line. Hence the gain is calculated as

$$Gain = |Gradient| = \frac{v_{OUT,f} - v_{OUT,i}}{v_{IN,f} - v_{IN,i}} = \frac{2.96}{1.786 \times 10^{-3}} = 1657.3 \text{ V/V} \qquad (3.41)$$

which is equivalent to 64.39 dB.

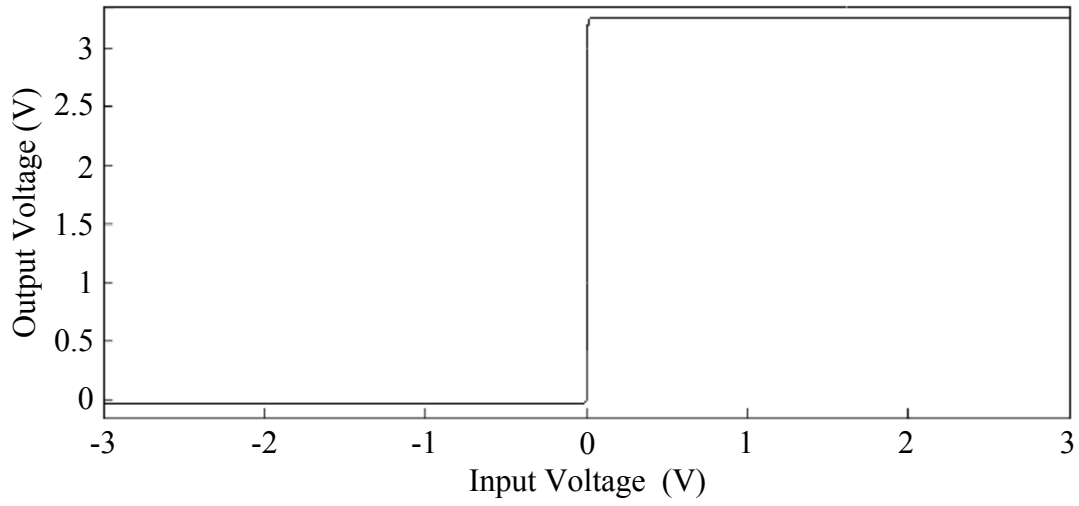


Figure 3.20.

DC transfer characteristic of the two-stage telescopic amplifier.

The AC analysis demonstrates (in Figure 3.21) a 3 dB cut-off frequency of 30 MHz and a unity gain bandwidth of just over 1 GHz.

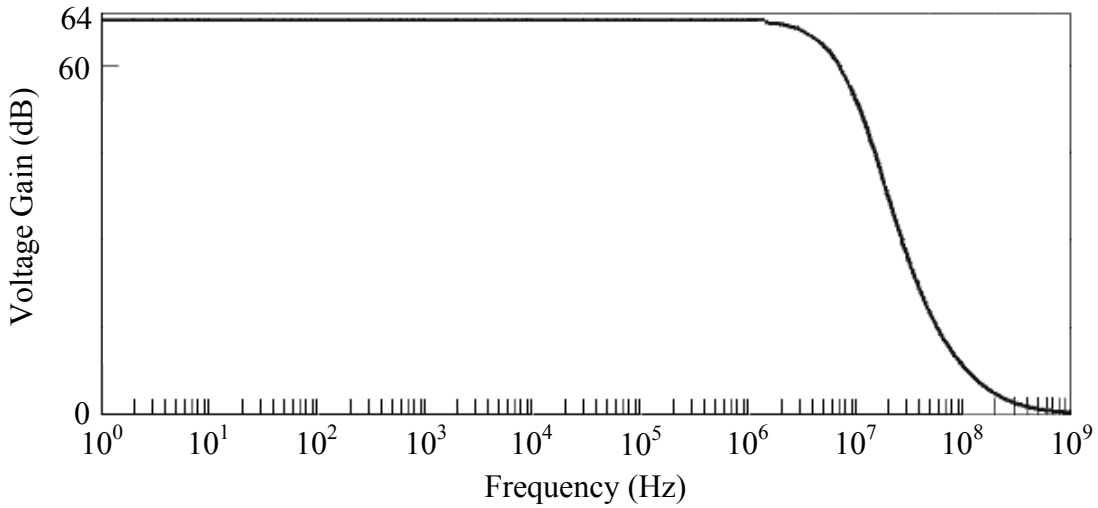


Figure 3.21.

AC sweep performed on the telescopic amplifier implemented.

3.5 Mixer design

This section briefly covers the different types of mixer topologies available; namely the FET and BJT mixer topologies suitable for microelectronic integration. Description and the typical layout of an image rejection mixer that can remove unwanted mixing images are also shown in this section. The section then briefly covers the noise types generally found in mixing systems and the causes of these noise signals.

The latter part of the section details the simulation results for the mixer implemented for this thesis.

FET Mixers

FETs can be used as mixers in both their active and their passive modes. Active mixers using FETs are transconductance mixers that use the local oscillator (LO) to vary the transconductance of the transistor. The advantage of using this method of mixing is that the system can have conversion gain as opposed to loss[6] and that active systems generally have lower noise figures than that of passive designs. Figure 3.22 shows the typical topology for a mixer of this type.

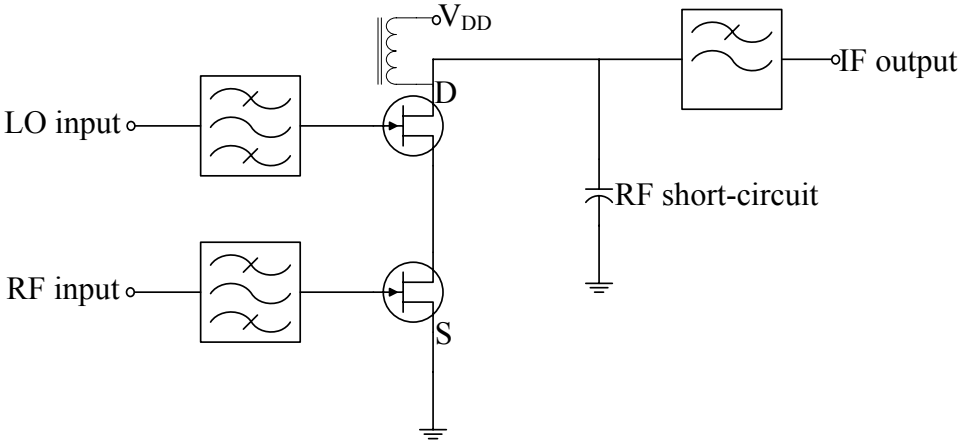


Figure 3.22.

General topology for an active dual FET mixer topology.

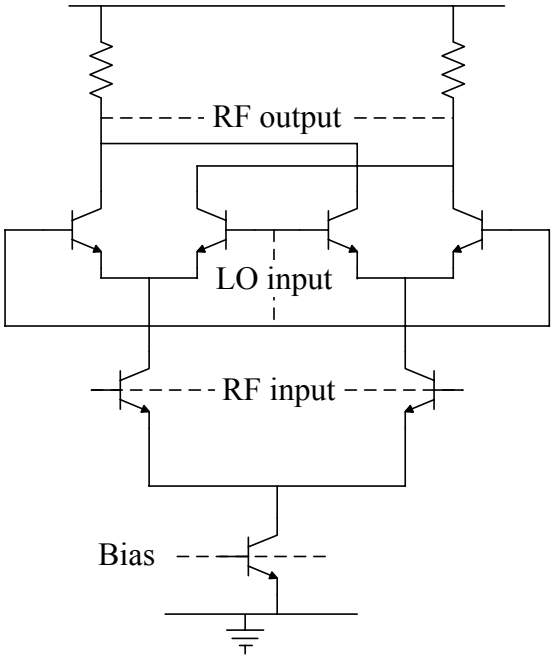
In Figure 3.22 the RF signal is applied to the bottom transistor, which is matched using standard amplifier design techniques, with the IF frequency applied to the top device. The reason for the RF choke on the output of the system is so that the value of the transistor V_{DS} does not move significantly from its DC bias point when the LO is applied. One advantage of this method of mixing is that the IF and RF signals are inherently isolated from each other. A disadvantage of this mixing type is that the system will have lower linearity than the passive design methods.

BJT mixers (Barry Gilbert Mixers)

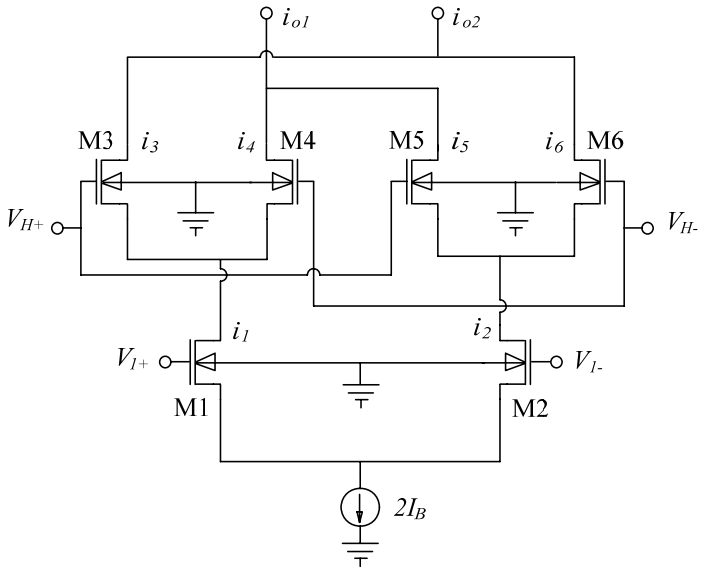
Discrete bipolar mixers are low cost, low power mixers. There are a wide range of commercially available Si bipolar integrated transceivers, each containing a mixer implementation. When transistors are fabricated close to each other on an IC, such as that proposed in this thesis, they tend to behave similar to one another, meaning that they are well matched. This matching allows the design of a Gilbert Cell mixer, as shown in Figure 3.23 (a) [36].

[6] Conversion loss is the ratio of the wanted signal level to the input signal, expressed in dB

The mixer shown in Figure 3.23 (a) is essentially a multiplication device that multiplies the RF signal by ±1 at the LO frequency. In order for this to occur the transistor devices have to be matched with one another; this requires that the system is active and therefore impractical in a discrete implementation. Unfortunately BJT mixers tend to have lower linearity than other mixer types. However, the Gilbert cell can be implemented by using MOSFET devices in order to increase the linearity of the system; such a configuration is shown by Figure 3.23 (b).



(a)



(b)

Figure 3.23.

(a) Double balanced Gilbert cell topology

(b) Gilbert cell topology in MOSFET.

Image rejection mixers

An image rejection mixer is two balanced mixers of any type, driven in quadrature by a RF signal. The RF signal is shifted in phase by 90º and mixed with an in-phase LO signal. This creates four quadrature signals that when shifted again by 90º and added, reinforces the wanted signal and cancel out the unwanted images. Figure 3.24 shows the typical block diagram for an image rejection mixer.

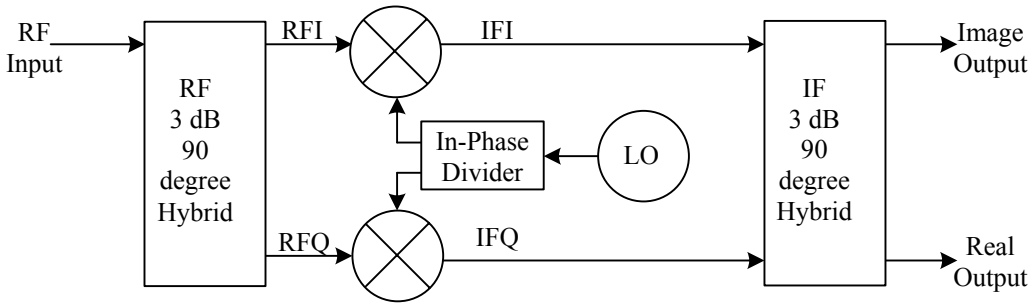


Figure 3.24.

Typical layout of image rejection mixing system

Noise in mixers

Thermal noise

Thermal noise is caused by random thermal motion of electrons in a conducting media. While moving through a conducting media, the large numbers of free electrons that constitute the current collide with ions that vibrate about their normal position in a lattice. The consequence of these random collisions is that the electric current is likewise random.

Thermal noise is directly proportional to the absolute temperature *T,* since the source of this kind of noise is due to the thermal motion of electrons. The probability density function of thermal noise is Gaussian distributed, while the power spectral density is a constant [37]. Since the power spectral density is a constant, thermal noise is a white noise and independent of frequency.

Shot noise

The flow of current is not continuous. It consists of discrete charges equal to the electron charge q (= $1.602.10^{-19}$ C). Shot noise occurs when there is a current flowing across a potential barrier. Fluctuations in the average current are due to random hopping of a charge across this barrier. In semiconductor devices, shot noise manifests itself through the

random diffusion of electrons or the random recombination of electrons with holes. Shot noise is characterized by a Gaussian probability function.

Flicker noise

Also known as, 1/*f* noise, the origin of this kind of noise is not clearly understood. It is observed that flicker noise is most prominent in devices that are sensitive to surface phenomena. This suggests that the source of flicker noise is kinds of defects and impurities that randomly trap and release charge. This charge-trapping phenomenon realises in such a way that it gives rise to a 1/*f* spectrum. The fact that the operating frequency of the mixers that are designed for this thesis is very high means that flicker noise will not be the dominant noise mechanism due to its 1/*f* spectrum.

Mixer implementation

The following list indicates particular characteristics that a mixer must adhere to in order to provide a reliable down or up conversion process within the transceiver of this thesis.

- The mixer must provide good linearity ensuring that the input RF signal is not distorted.
- Noise contributions to the final signal must be kept to a minimum; in order to preserve the signal to noise ratio of the input RF signal
- The local oscillator to intermediate frequency feed through should be minimised; in order to minimise interference generated within the IF band.

The simplest solution to the characteristics of the mixer described earlier is the use of a double balanced Gilbert cell in order to perform the down conversion process. The operation of the mixer can be determined using translinear analysis in Figure 3.23.

This analysis (repeated here, from [71]) disregards second order effects, which means that all AC currents are dependent on the gate source voltage

$$i = k_n' \frac{W}{L}(V_{GS} - V_t)v_{gs} = g_m v_{gs} \tag{3.42}$$

It can be seen that the mixer is biased with constant current source equal to $2I_B$. Drain (and source) currents of transistors M1 and M2 are respectively

$$i_1 = I_B + i_l \tag{3.43}$$

and

$$i_2 = I_B - i_l, \tag{3.44}$$

where i_l is small signal AC current due to the voltage $v_{l+,}$ and $-i_l$ is the AC current due to voltage v_{l-}.

Following the similar analysis procedure the currents through transistors M3, M4, M5 and M6 can be determined as

$$i_3 = \frac{I_B}{2} + \frac{i_l}{2} + i_h \tag{3.45}$$

$$i_4 = \frac{I_B}{2} + \frac{i_l}{2} - i_h \tag{3.46}$$

$$i_5 = \frac{I_B}{2} - \frac{i_l}{2} + i_h \tag{3.47}$$

$$i_6 = \frac{I_B}{2} - \frac{i_l}{2} - i_h \tag{3.48}$$

respectively, where i_h is the current due to the high frequency voltage v_h and $-i_h$ is the current due to voltage v_{h-}. Finally, currents i_{O1} and i_{O2} are $i_3 + i_6$ and $i_4 + i_5$, or equivalently

$$i_{O1} = \left(\frac{I_B}{2} + \frac{i_l}{2} + i_h\right) + \left(\frac{I_B}{2} - \frac{i_l}{2} - i_h\right) = I_B \tag{3.49}$$

$$i_{O2} = \left(\frac{I_B}{2} + \frac{i_l}{2} - i_h\right) + \left(\frac{I_B}{2} - \frac{i_l}{2} + i_h\right) = I_B \tag{3.50}$$

According to this analysis output of the mixer is a DC current of value I_B in both outputs, which makes the device useless.

However, if the second order effects are not disregarded the currents through each of the top four transistors will have additional currents equal to $\frac{1}{2}k'\frac{W}{L}v_{gs}{}^2$ [31], all four flowing from drain to source because they depend on the square of the voltage. This is contrary to the currents due to the first order effects, which alternate the direction. New i_3, i_4, i_5 and i_6 are now

$$i_3 = \frac{I_B}{2} + \frac{i_l}{2} + i_h + i_{so3}, \tag{3.51}$$

$$i_4 = \frac{I_B}{2} + \frac{i_l}{2} - i_h + i_{so4}, \tag{3.52}$$

$$i_5 = \frac{I_B}{2} - \frac{i_l}{2} + i_h + i_{so5} \tag{3.53}$$

$$i_6 = \frac{I_B}{2} - \frac{i_l}{2} - i_h + i_{so6} \tag{3.54}$$

The second order effects in transistors M1 and M2 are not of importance (the currents will cancel) and are therefore excluded in the analysis.

Output currents will thus be

$$i_{O1} = \left(\frac{I_B}{2} + \frac{i_l}{2} + i_h + i_{so3}\right) + \left(\frac{I_B}{2} - \frac{i_l}{2} - i_h + i_{so6}\right) = I_B + i_{so3} + i_{so6} \tag{3.55}$$

$$i_{O2} = \left(\frac{I_B}{2} + \frac{i_l}{2} - i_h + i_{so4}\right) + \left(\frac{I_B}{2} - \frac{i_l}{2} + i_h + i_{so5}\right) = I_B + i_{so4} + i_{so5} \tag{3.56}$$

Further

$$i_{so3} \propto v_{gs3}{}^2, \tag{3.57}$$

$$i_{so4} \propto v_{gs4}{}^2, \tag{3.58}$$

$$i_{so5} \propto v_{gs5}{}^2 \tag{3.59}$$

$$i_{so6} \propto v_{gs6}{}^2 \tag{3.60}$$

But

$$v_{gs3} = v_{h+} - v_{s3,4}, \tag{3.61}$$

$$v_{gs4} = v_{h-} - v_{s3,4}, \tag{3.62}$$

$$v_{gs5} = v_{h+} - v_{s5,6}, \tag{3.63}$$

$$v_{gs6} = v_{h-} - v_{s5,6}, \tag{3.64}$$

$$v_{h+} = v_h, \tag{3.65}$$

$$v_{h-} = -v_h, \tag{3.66}$$

$$v_{s3,4} \propto v_{l+} = v_l \tag{3.67}$$

$$v_{s5,6} \propto v_{l-} = -v_l \tag{3.68}$$

If the constant of proportionality in Equations (3.67) and (3.68) is 1 (which can be done by setting the proper *W*/*L* ratio for M1 and M2), this analysis results in

$$i_{so3} \propto v_h{}^2 + v_l{}^2 - 2v_h v_l \tag{3.69}$$

$$i_{so4} \propto v_h{}^2 + v_l{}^2 + 2v_h v_l \tag{3.70}$$

$$i_{so5} \propto v_h{}^2 + v_l{}^2 + 2v_h v_l \tag{3.71}$$

$$i_{so6} \propto v_h{}^2 + v_l{}^2 - 2v_h v_l \tag{3.72}$$

Then,

$$i_{o1} = i_{so3} + i_{so6} \propto 2v_h^{\,2} + 2v_l^{\,2} - 4v_h v_l \tag{3.73}$$

$$i_{o2} = i_{so4} + i_{so5} \propto 2v_h^{\,2} + 2v_l^{\,2} + 4v_h v_l \tag{3.74}$$

If the two outputs of the mixer are taken differentially the final output current will be

$$i_O = i_{o2} - i_{o1} = 8v_h v_l \quad \text{(mixing is thus evident)} \tag{3.75}$$

In order to determine meaningful results from a mixer design a set amount of benchmarks must be determined in order to qualify the design [38]. For this thesis, the implementation is shown in Figure 3.25.

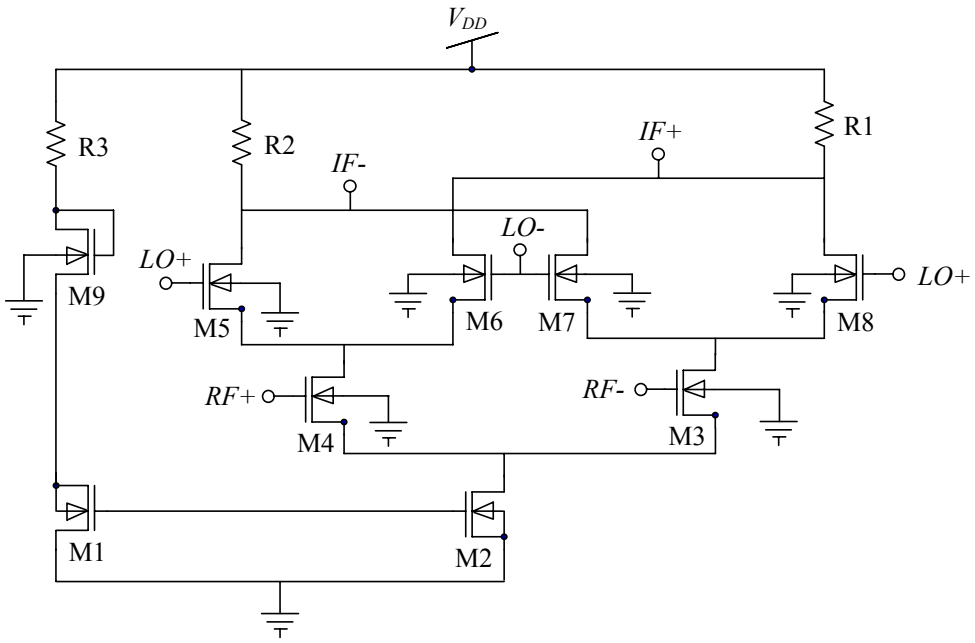


Figure 3.25.

Circuit configuration for a double balanced Gilbert mixer [71].

The forward voltage conversion gain of a mixer is calculated by [31]

$$K_c = \frac{v_{OUT,IF}}{v_{RF}} = \frac{2g_{M4}R}{\pi} \tag{3.76}$$

The voltage conversion gain is a measure of the ratio of root mean square (RMS) output voltage of the mixer to the input RF voltage to the mixer. It is advantageous to have a high forward conversion gain, but this usually comes with the trade off of increased noise power at the output of the mixer.

Linearity is the second benchmark that must be determined. The linearity is a measure of distortion that the mixer creates due to the conversion process. When the branch currents

of the two RF commutation transistors (M1 and M2) are analysed an expression can be determined for the distortion of the input RF signal given by

$$I_{RF+} = \frac{K_n}{2}\left(\frac{W}{L}\right)(V_{GS1} - V_t)^2 \qquad I_{RF-} = \frac{K_n}{2}\left(\frac{W}{L}\right)(V_{GS2} - V_t)^2 \tag{3.77}$$

$$V_{RF} = V_{GS1} - V_{GS2} \tag{3.78}$$

$$V_{RF} = \sqrt{\frac{I_{ss}}{K_n^{'}}} \cdot \left(\sqrt{1 + \frac{\Delta I_{RF}}{I_{ss}/2}} - \sqrt{1 - \frac{\Delta I_{RF}}{I_{ss}/2}}\right) \tag{3.79}$$

$$\Delta I_{RF} = \frac{I_{ss}}{2} \cdot \sqrt{\frac{K_n^{'} V_{RF}^2}{I_{ss}}} \cdot \left(1 - \frac{K_n^{'} V_{RF}^2}{4 I_{ss}}\right) \tag{3.80}$$

where ΔI_{RF} measures the distortion introduced by the mixer and $K_n^{'}$ is the gain parameter of the transistor. I_{SS} is the drain current of transistor M2. The distortion can be determined analytically through the use of the Taylor expansion of the harmonics introduced to the system, given by

$$\begin{aligned} \Delta I_{RF} &= a_1 V_{RF} + a_2 V_{RF}^2 + a_3 V_{RF}^3 + \ldots \\ a_1 &= \sqrt{\frac{K_n^{'} I_{ss}}{4}} \\ a_2 &= 0 \\ a_3 &= -\frac{K_n^{'}}{16}\sqrt{\frac{K_n^{'}}{I_{ss}}} \end{aligned} \tag{3.81}$$

The noise figure of Gilbert's double balanced mixer can be determined by Equation (3.82) [38].

$$NF_{Gilbert} = \frac{\pi^2}{4}\left(1 + \frac{2\gamma}{g_{M4\_RF} \cdot R_s} + \frac{2}{g_{M4\_RF} \cdot R_s \cdot R_3}\right) \tag{3.82}$$

where γ – factor dependent on device gate length (assumed as 3)

where R_s is the source resistance (assumed as 50 Ω)

where R_3 is the load resistance (500 Ω)

Table 3.8 presents the obtained values for the Gilbert cell mixer.

Component	**Value**
L_1-L_9	0.35 µm
W_5-W_8	50 µm
W_4-W_3	100 µm
W_1-W_2 and W_9	5 µm
R_3	500 Ω

Table 3.8.

Component values for the Gilbert cell.

The layout of this circuit is shown in Figure 3.26.

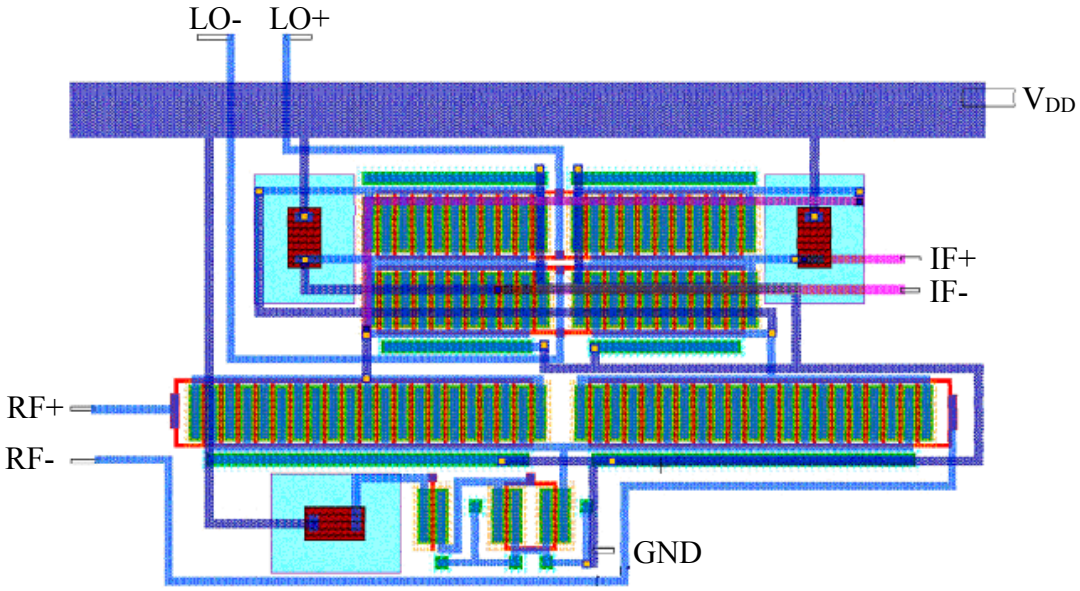


Figure 3.26.

Circuit layout for the mixer.

Simulation results

Figure 3.27 shows successful test simulation results of this circuit (Figure 3.25) with high frequency and lower frequency sinusoidal waves as inputs.

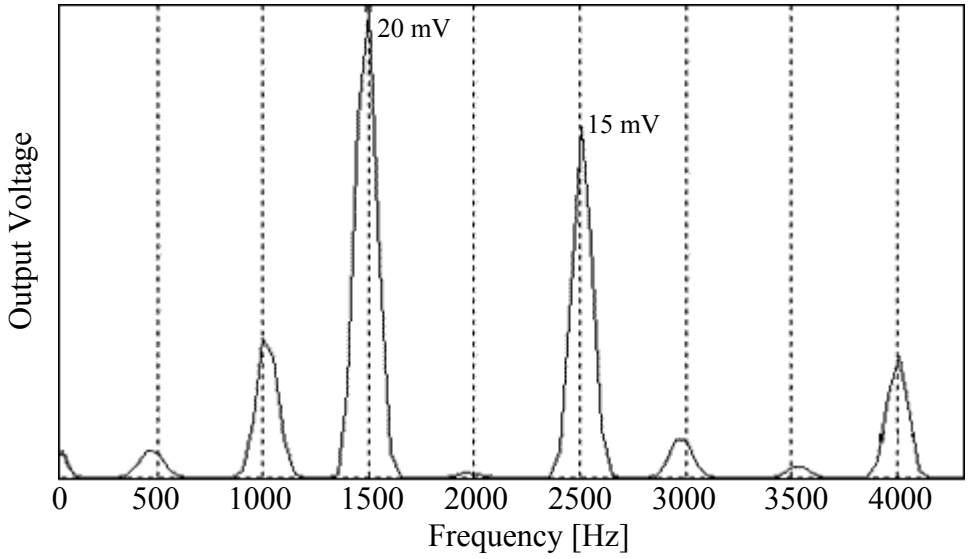


Figure 3.27.

Mixer tested with two signals, one at 0.5 GHz, and other at 2 GHz.

Intercept point is defined in Fig. 3.28. The input power is plotted along the horizontal axis, and output power is plotted along the vertical axis. Two lines are plotted: one relating IF

output power to RF input power, and another relating intermodulation output power to RF input power.

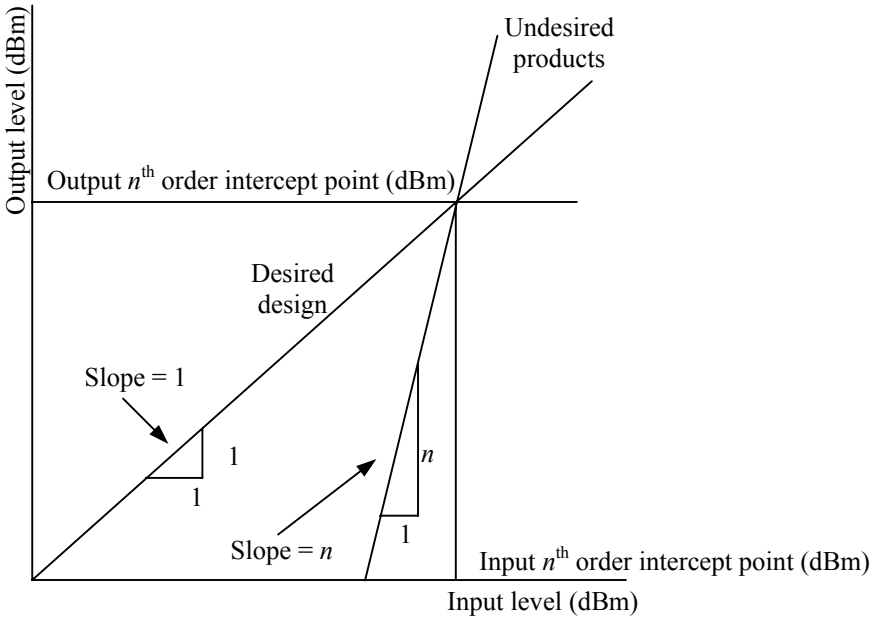


Figure 3.28.

Definition of Intercept Point.

The point at which these lines intersect gives the input and output intercept points for the mixer at a particular set of input frequencies for a given LO power level and temperature. For the mixer designed for this thesis, the intercept point is obtained as in Fig. 3.29.

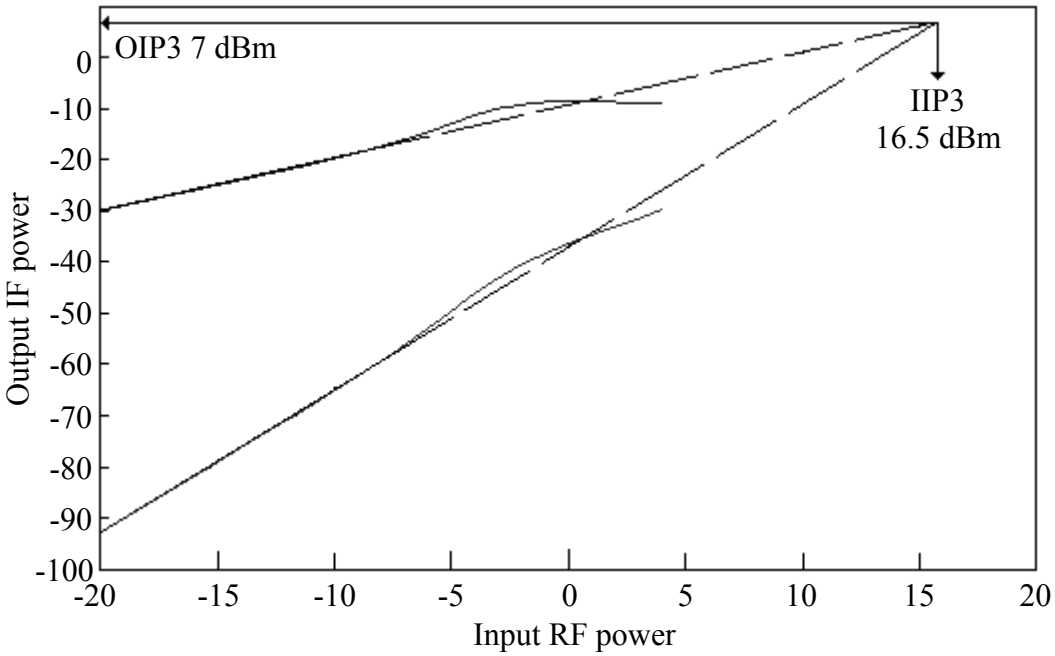


Figure 3.29.

Plot of first and third harmonic outputs of the mixer.

The third intercept point (IIP3) is given by (for long channel devices) [38]:

$$IIP3 = 4\sqrt{\frac{2}{3}}\left(V_{gs} - V_t\right) = 2.8 \tag{3.83}$$

3.6 LNA design

Within any modern RF IC design, the use of a low noise amplifier (LNA) has become pivotal in determining the success of a system's operation. The objective of the LNA is to amplify the incoming signal without the addition of any unnecessary noise produced by the circuit.

Another objective of the LNA is to provide input matching to the characteristic impedance of the RF input signal. This has the consequence that the LNA absorbs the input power of the RF input signal so that it can be amplified.

An LNA is an important sub-system of the receiver, as the overall noise figure (NF) of the RF front end is scaled by the LNA gain. All the subsequent noise figures subsequent to the LNA are scaled by the LNA gain demonstrated by Friis' formula:

$$NF_{receiver} = \left(\frac{1}{G_{LNA}}\right)(NF_{subsequent\_stages} - 1) + NF_{LNA} \tag{3.84}$$

The operation of an LNA entails some of the aspects listed below.

- To transform the characteristic input impedance, while retaining stability during operation.
- Amplifying the input signal to level that is of use to the rest of the system.
- To finally transform the output signal of the amplifier in order to attain maximum power transfer without the addition of unnecessary noise.

Figure 3.30 shows the different operations performed by the LNA.

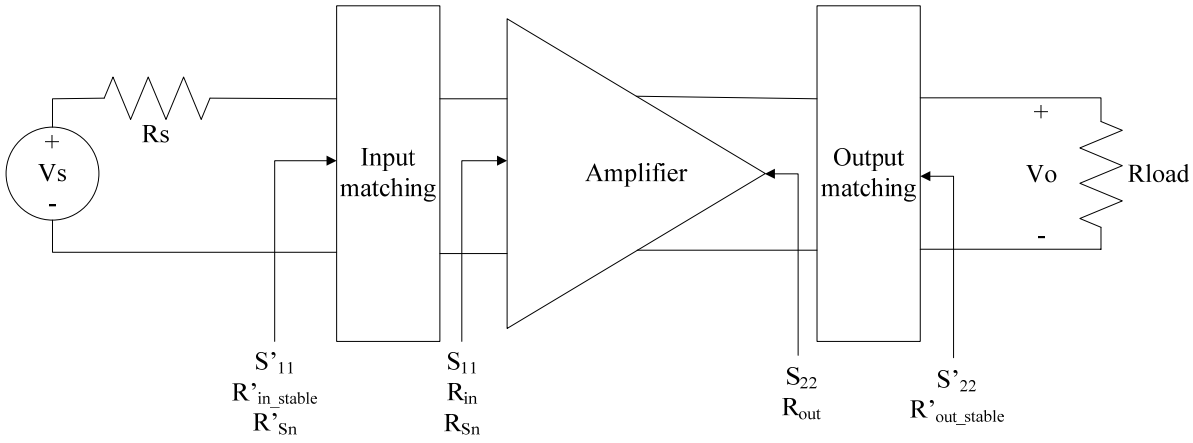


Figure 3.30.

Different stages of an LNA operation.

With reference to Figure 3.30 the scattering parameters (S-parameters) are indicated upon the figure, where S_{11} is the input reflection coefficient and S_{22} is the output reflection coefficient. The simultaneous use of a power-constrained noise and input matching technique was applied to the differential cascode configuration [39]. The cascode LNA (Fig. 3.31) uses an inductive degeneration topology in order to provide a real part matching to the input RF source. Coupled with the inductive degeneration topology an L matching network is used in order to match for S_{11}.

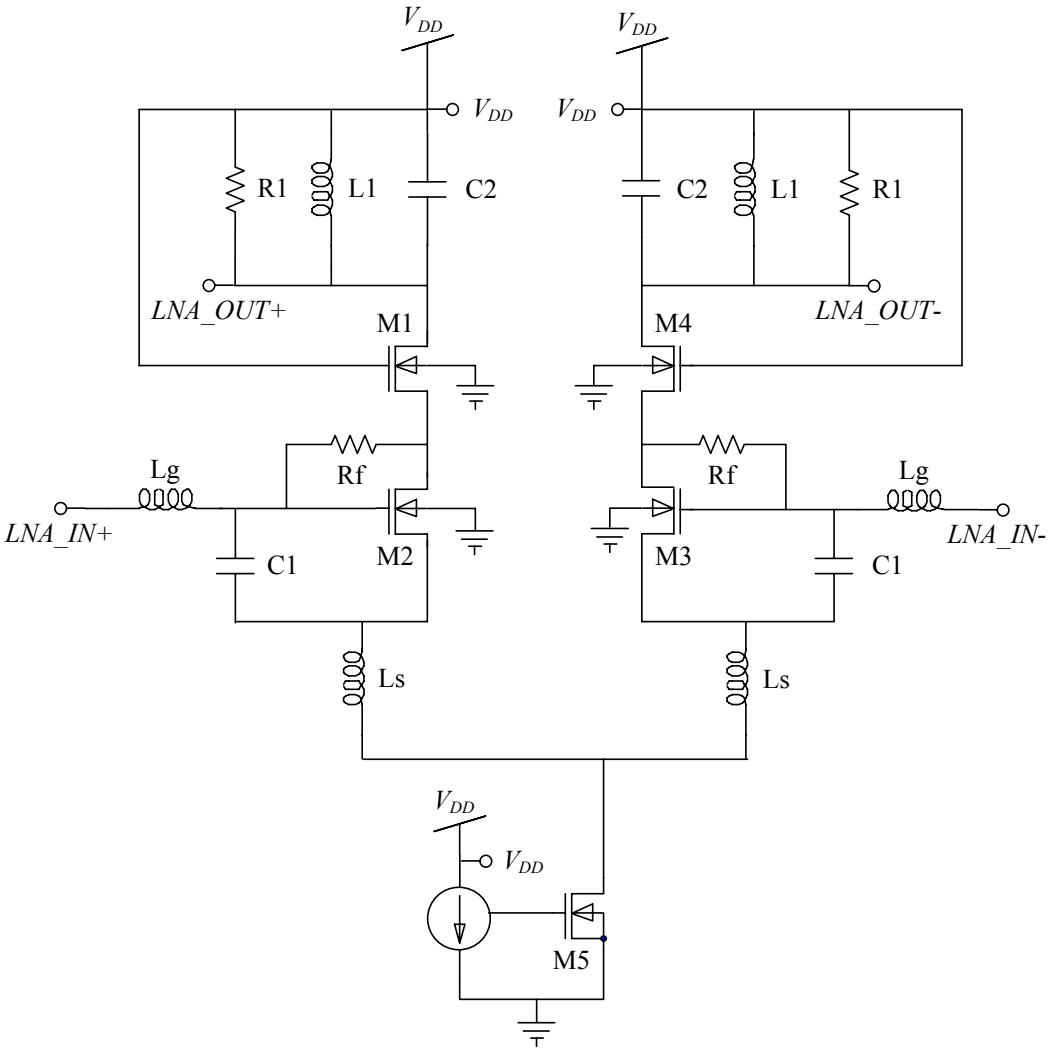


Figure 3.31.

Cascode differential LNA circuit – basic topology adapted from [40].

It can be shown that for one branch of the LNA (M1 and M2) that the noise figure is given by

$$NF = 1 + \frac{2}{3g_{M3}R_s} \tag{3.85}$$

where g_{m3} is the transconductance of MOSFET M3 and R_S the equivalent noise resistance of the source. In order to provide input matching both the real and imaginary part of the characteristic input impedance must be matched to the input impedance of the amplifier. It can be shown that from the small signal model of the M1 and M2 branch that the input impedance of the LNA is represented by

$$
\begin{aligned}
Z_{in} &= j\omega(L_g + L_s) + \frac{1}{j\omega C} + g_{M3}\frac{L_2}{C} \\
\text{Choosing } &\frac{1}{\omega C} = \omega(L_g + L_s) \\
\Re\{Z_{in}\} &= g_{M3}\frac{L_s}{C} \\
\Im\{Z_{in}\} &= j\omega(L_s + L_g) + \frac{1}{j\omega C}
\end{aligned}
\tag{3.86}
$$

where C = C_{gs} + $C_{1,}$ it is worth noting that the addition of C_1 to the transistor lowers the overall unity gain frequency of the transistor [41].

By matching the components to real and imaginary condition of Z_{in} the noise figure can be simplified to [40]

$$NF = 1 + \frac{2}{3}\frac{1}{1 + \frac{L_g}{L_s}} \tag{3.87}$$

The transistor M1 is set to a specific transconductance value through the use of the current source M5 and correct biasing of V_{GS}. The transconductance can be determined by

$$g_{M3} = \sqrt{I_{M5}k_n'\left(\frac{W_3}{L_3}\right)} \tag{3.88}$$

By setting W_3 = 200 µm and L_3 = 0.35 µm and using k_n' is 170 µA/V, equation (3.88) can be simplified to:

$$g_{M3} = \sqrt{I_{M5}}\,0.3116 \tag{3.89}$$

The voltage gain of the LNA [40] is given by

$$A_v = \frac{L_1}{L_s(1 - \omega_c^2 L_1 C_2)} \tag{3.90}$$

Using the above-mentioned relations the LNA was designed for an f_c of 2.4 GHz. The final values obtained for the LNA is tabulated in table 3.9.

Parameter	Value
L_1-L_4	0.35 µm
W_1-W_4	200 µm
Number of gate fingers	40
L_s	2 nH
L_g	6.2 nH
C_1	500 fF
C_2	1.2115 pF
L1 (Inductor)	8 nH

Table 3.9.

Transistor parameters and component values required for the LNA.

The layout of this circuit is shown in Figure 3.32.

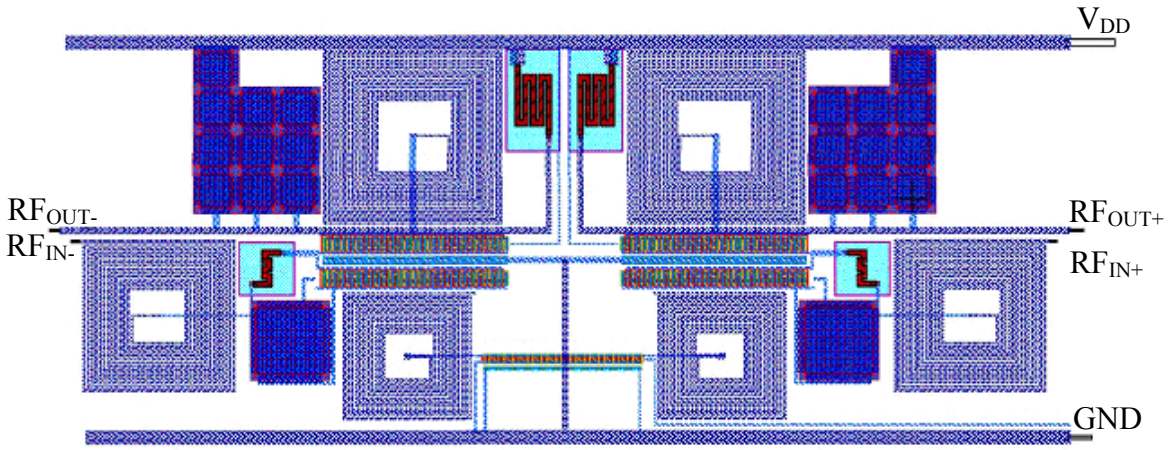


Figure 3.32.

Circuit layout for the LNA.

The noise figure predicted by equation (3.87) is about 1.2 dB. For the differential topology, the figure will be twice this value, thus about 2.4 dB.

Simulation results

The S_{11} parameter can be determined by

$$Z_{in} = \frac{V_{in}}{I_{in}}$$
$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \qquad (3.91)$$

The simulated parameters are shown in Figures 3.33-3.35.

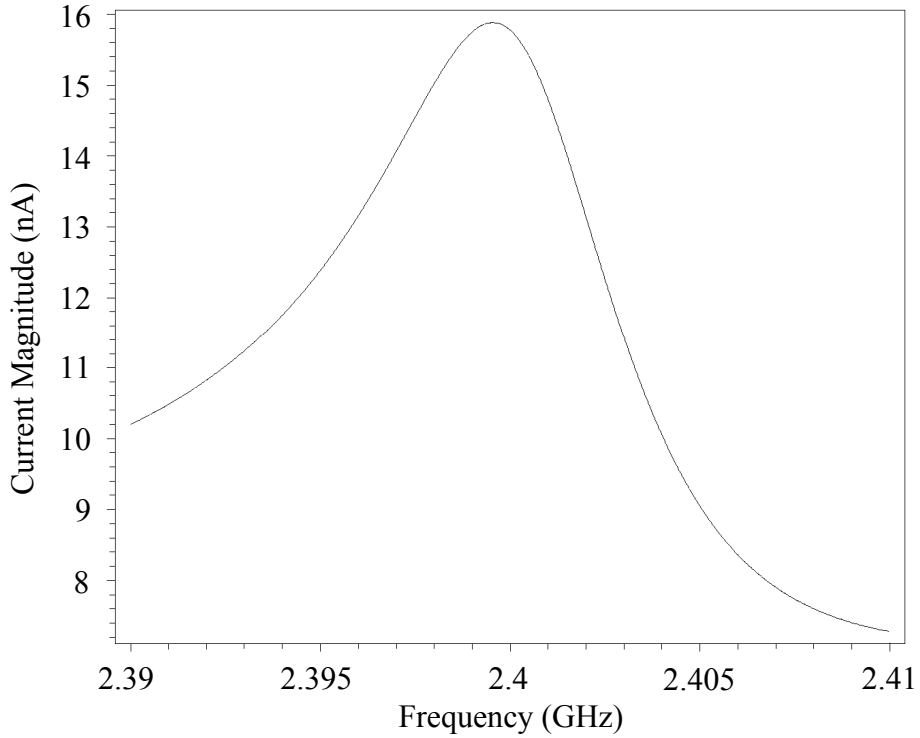


Figure 3.33.

Input current of the LNA.

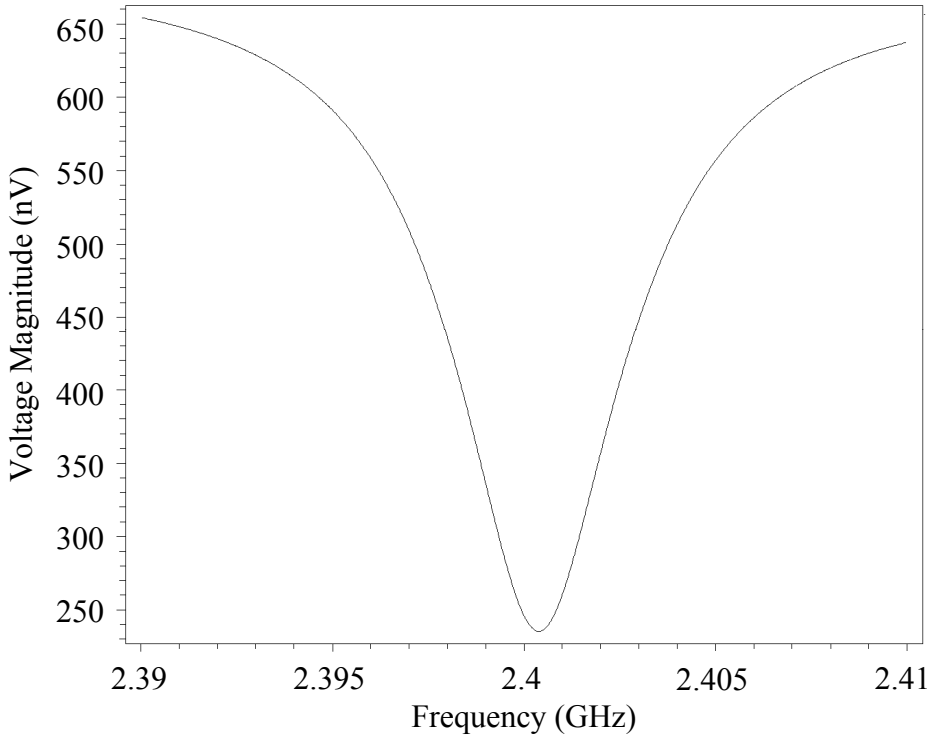


Figure 3.34.

Input voltage to the LNA as a function of input frequency.

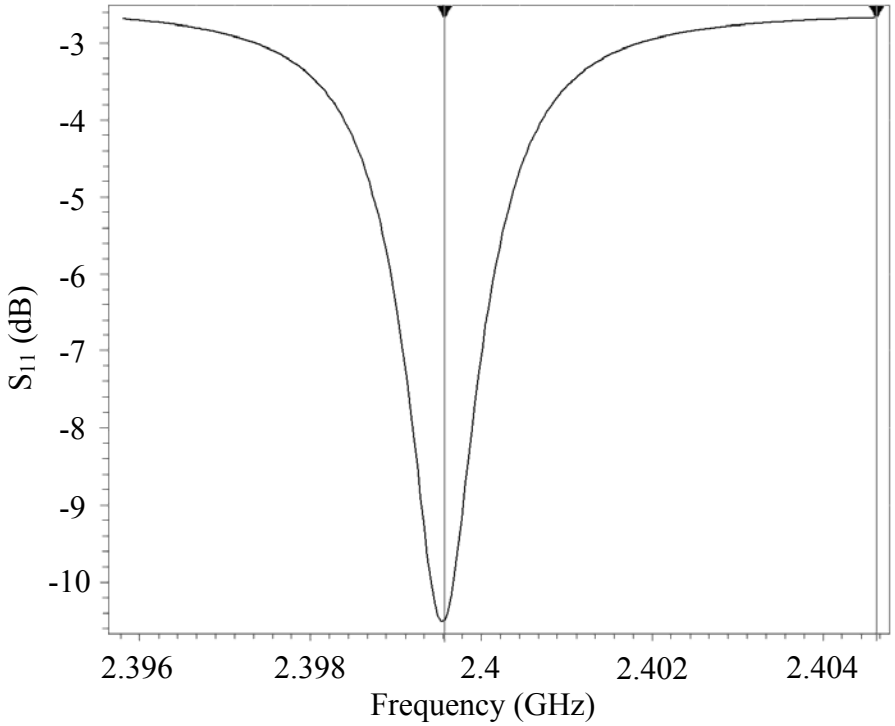


Figure 3.35.

S_{11} input parameter of the LNA.

The input port reflection coefficient was found to be -10.5 dB at 2.3988 GHz. The gain of the LNA is measured:

$$Gain_{dB} = 20\log_{10}\left(\frac{v_{out}}{v_{in}}\right) \tag{3.92}$$

Figure 3.36 plots this gain.

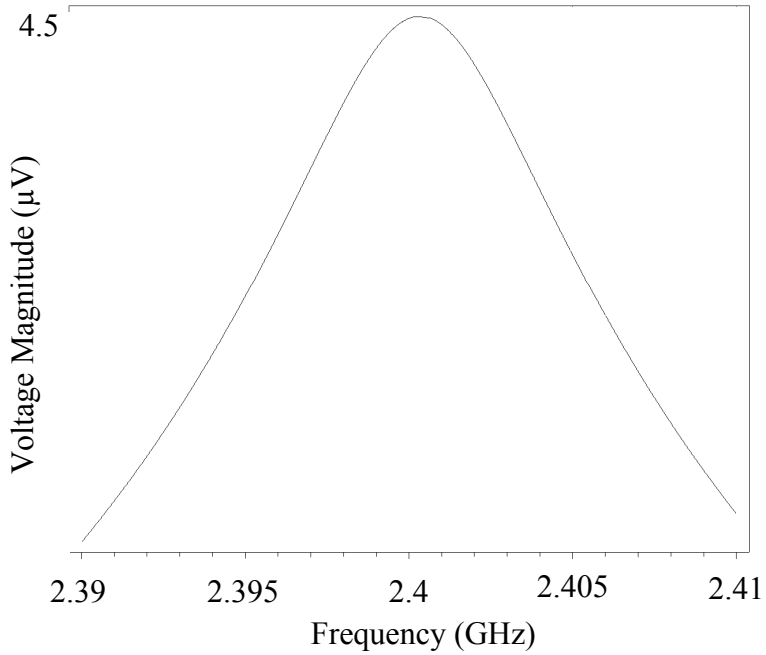


Figure 3.36.

Measurements of the LNA gain (for a 250 nV input).

From Figure 3.36, it can be seen that the LNA has a peak voltage gain of about 25 dB at 2.4006 GHz. Figure 3.37 plots the LNA input referred noise.

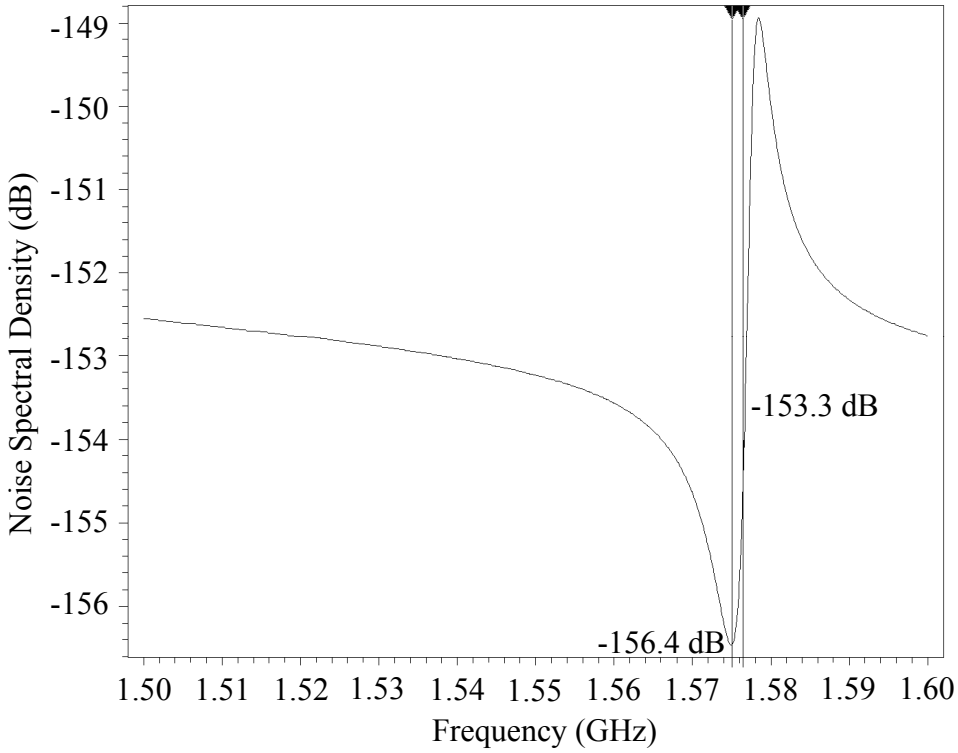


Figure 3.37.

Simulation to determine the LNA input referred noise.

Noise figure is the noise factor, expressed in dB.

It can be seen from Figure 3.37 that the LNA has noise figure of 3.1 dB (-153.3 dB-(-156.4 dB)) in the bandwidth of interest.

3.7 Active Inductor design

This section discusses the design of active inductors used in the filtering and oscillation sub-systems of this thesis. The active inductors designed are somewhat limited due to their larger power consumption [42; 63].

Active inductors are available in many forms depending on the usage for which the design is intended. The two configurations used in the system of this thesis are the push-pull gyrator-C and the push-push intrinsic-C model [43]. The inductance of the devices shown in Figure 3.38 is realized by the combination of the two transistors in such a way that the two active devices realise the high frequency characteristics of a normal inductor. The

inductor system is unfortunately extremely dependant on the intrinsic capacitances of the transistor models.

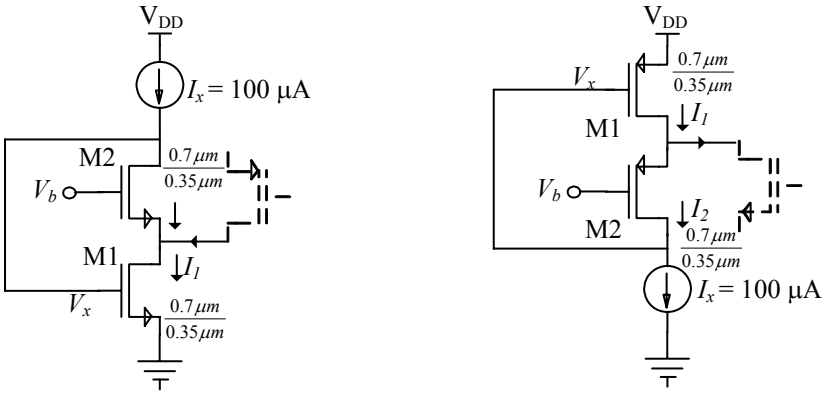


Figure 3.38.

Basic layout for two possible configurations resulting in active inductance [56].

Various kinds of active inductors have been proposed for on-chip design [42, 43]. A common feature of these active inductors is that all active inductors feature a form of shunt feedback to emulate inductive impedance. A small signal model is shown in Figure 3.39.

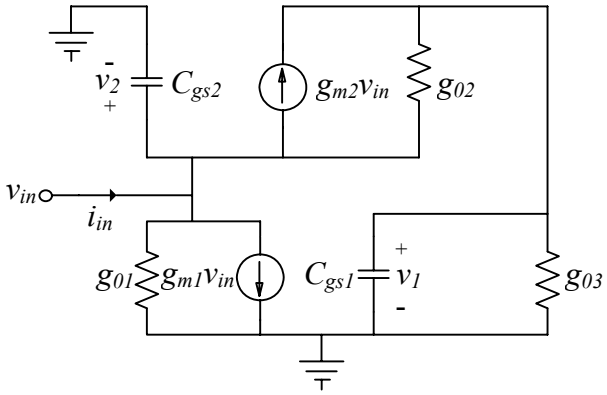


Figure 3.39.

Small signal model for the active inductor system.

The small-signal current can be derived as shown in equation (3.93):

$$i_{in} = \left[\left(g_{o1} + g_{m2} \right) + sC_{gs2} + \frac{g_{m1}\left(g_{m2} + g_{o2} \right)}{sC_{gs1} + g_{o2} + g_i} \right] v_{in} \tag{3.93}$$

where g_m and g_o are the transconductance and output conductance of the corresponding transistors, g_i is the output conductance of current source, and C_{gs} is the gate source capacitance.

The inductive effect of the circuits can be understood as follows. Since the circuits use shunt feedback at the input node, the impedance seen at low frequencies is relatively small.

When the frequency increases the gate-source capacitance will cause a drop in the feedback loop gain, thus, input impedance will increase with frequency, simulating the effect of an inductive element.

By analogy, the following expressions can be derived from equation (3.93):

$$C_p = C_{gs2} \tag{3.94}$$

$$R_p = \frac{1}{g_{o1}} \| \frac{1}{g_{m2}} \approx \frac{1}{g_{m2}} = \frac{1}{\sqrt{2K_n'(\frac{W_2}{L_2})I_2}} \tag{3.95}$$

$$R_s = \frac{g_{o2} + g_{o3}}{g_{m1} g_{m2}} \tag{3.96}$$

$$L_{eff} = \frac{C_{gs1} + C_{gd1} + C_{gd2}}{g_{m1} g_{m2}} \approx \frac{C_{gs1}}{g_{m1} g_{m2}} \tag{3.97}$$

By analysis of the above small-signal model and the Equations (3.94-3.97), the RLC model of Figure 3.40 can be derived.

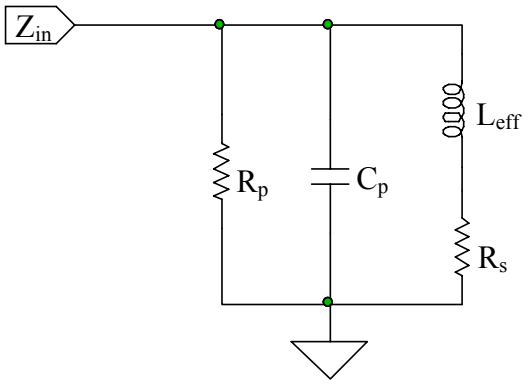


Figure 3.40.

Equivalent circuit derived from the small-signal model.

The self-resonant frequency of the active-inductor is:

$$\omega_t^2 = \frac{g_{m1} g_{m2}}{C_{gs1} C_{gs2}} = \omega_{t1} \omega_{t2} \tag{3.98}$$

where ω_{t1} and ω_{t2} are the unity current gain frequencies of M1 and M2 respectively. The Q value is approximately:

$$Q = \frac{R_p}{\omega_t L_p} = \sqrt{\frac{\omega_{t1}}{\omega_{t2}}} \tag{3.99}$$

For $\omega > \omega_t$: the circuit will become capacitive, so a higher ω_t is preferred. From equation (3.98), smaller values of L_1, L_2 and larger biasing currents (I_1 and I_2) will increase ω_t. While from equations (3.95) and (3.99), increasing I_2 means that the equivalent parallel

resistance, R_p and Q will be reduced. To increase ω_t without degrading the Q-factor of the active inductor, a folded DC coupling structure as shown in the dashed part of Fig. 3.38 can be used [43]. The biasing current from the other stages (for example, the input transconductance stage) is reused by M_1 while I_2 is kept the same, thus a higher ω_t and Q factor can be obtained. Since the current is reused by other stages, the power consumption is also well contained.

In order to reduce the noise seen in the system due to the resistive effects of the inductive current and increase the Q factor of the overall system a negative impedance converter (NIC) is required. The design of this device is simple; a negative g_m configuration is used to cancel out the resistor R_p of the active inductor.

The layout of the negative g_m configuration is shown in Figure 3.41.

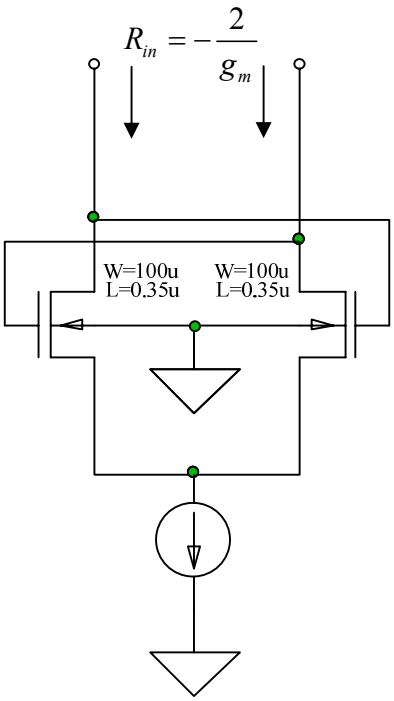


Figure 3.41.

Negative g_m transistor circuit.

The resistance created by the above circuit is given by the following equation:

$$R_{in} = -\frac{2}{g_m} \tag{3.100}$$

This resistive effect of the two matched transistors of the negative impedance circuit is used to cancel out the resistance represented by resistor R_p of Figure 3.41. Figure 3.42 shows the equivalent RLC model of the NIC. The relatively small capacitance added to the circuit will have negligible effects if a discrete capacitor is used to force a device to a required resonance, their effects must however be considered in designs where the intrinsic resonance frequency is used to create an oscillation tank.

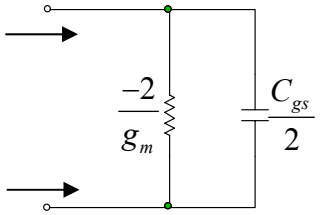


Figure 3.42.

RLC model of a NIC.

Thus,

$$R_p = \left| \frac{2}{g_m} \right|. \tag{3.101}$$

Active inductor oscillator and control

Conventional LC oscillators depend on a combination of inductors and capacitors to realize a resonance tank, necessary for generating the poles required for oscillation. This sub-system does the same but without the use of on-chip inductors. An active inductor topology was implemented in a negative g_m configuration, where active devices and capacitances were used to create an inductive effect. In summary, a NMOS and a PMOS device as well as two current sources were used, to produce a grounded inductor [44]. The inductance can be varied by varying the device transconductances.

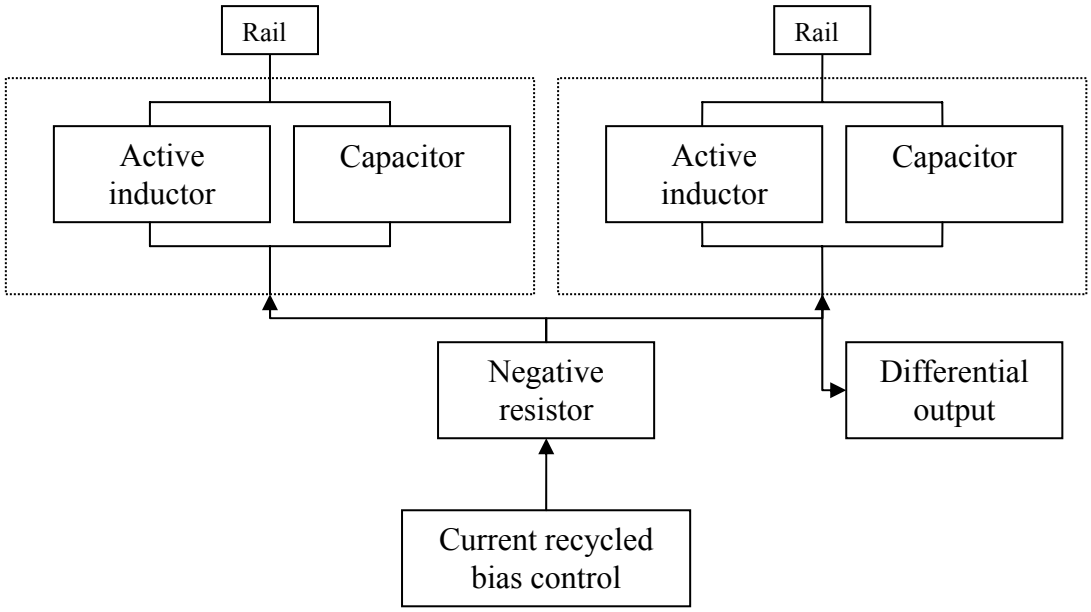
The frequency of oscillation is determined by the effective parallel capacitance and inductance in parallel

$$f_{out} = \frac{1}{2\pi\sqrt{LC}} \tag{3.102}$$

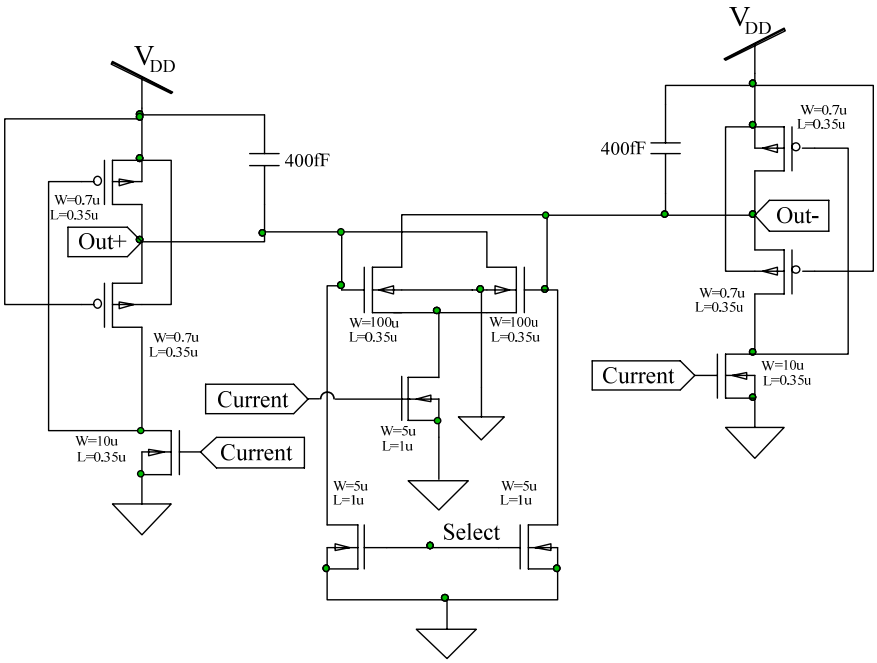
where L and C refers to the total parallel inductive and capacitive components, respectively. The resistive component was cancelled by the NIC, resulting in oscillations at the frequency specified in Equation (3.102).

A capacitor was connected to the active inductor inputs, where the value of the capacitor was chosen to be much larger than the intrinsic device capacitances. This forces the

capacitance value to be a nearly fixed value as opposed to a variable that is dependant on the aspect ratio of the transistor. The capacitor also served to reduce the phase noise content of the VCO output, as well as restrict the sensitivity of the active device to process variations in the transistor components. The VCO is shown in Figure 3.43.



(a)



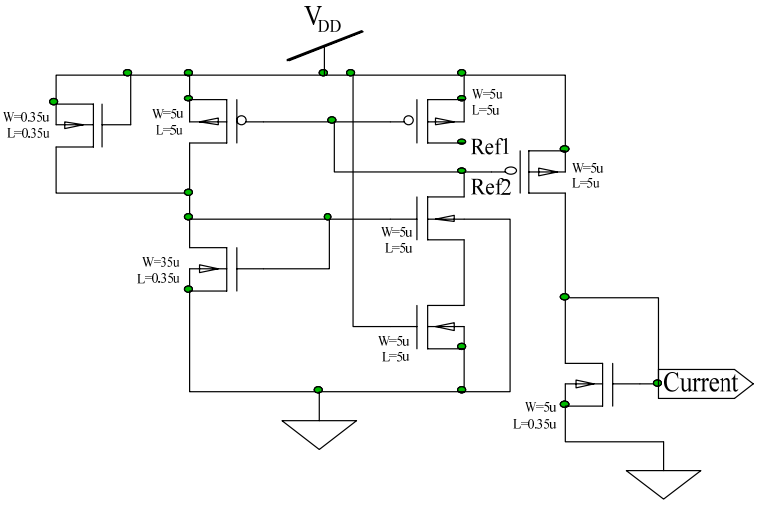
(b)

Figure 3.43 [56].

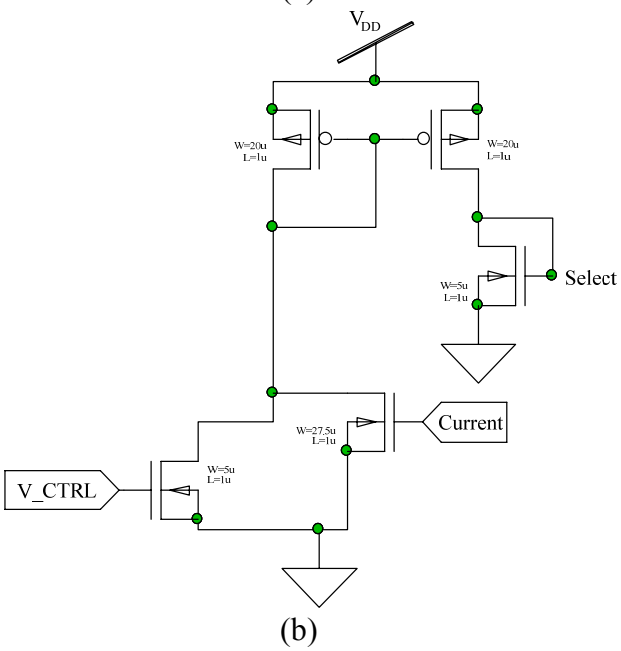
(a) Active inductor oscillator block diagram.

(b) Active inductor oscillator schematic. The current is generated as per Fig. 3.44 (a).

The frequency of oscillation was controlled by varying the resonant inductance. By biasing a transistor with an input control voltage (Fig. 3.44), the output of the current source (Fig. 3.38) could be adjusted (select input). This adjusted value was used as a reference in the biasing of the active transistor (transistors drawn in dashed lines in Fig. 3.38). By doing so the device Q-point can be shifted, allowing the adjustment of the inductive value and thus the frequency of oscillation. Figure 3.44 shows the schematic of the controlling circuit for the active inductor circuit shown in Figure 3.43. The resonant frequency of the inductor circuit is controlled by adjusting the biasing of each transistor separately to one another (current recycling) [44].



(a)



(b)

Figure 3.44.

(a) Current source (similar to the current terminal, Ref1 & Ref2 go to other points in the circuit – this has not been shown for clarity).

(b) Control circuit to adjust the frequency of oscillation for the active inductor.

The layout of the oscillator is shown in Figure 3.45.

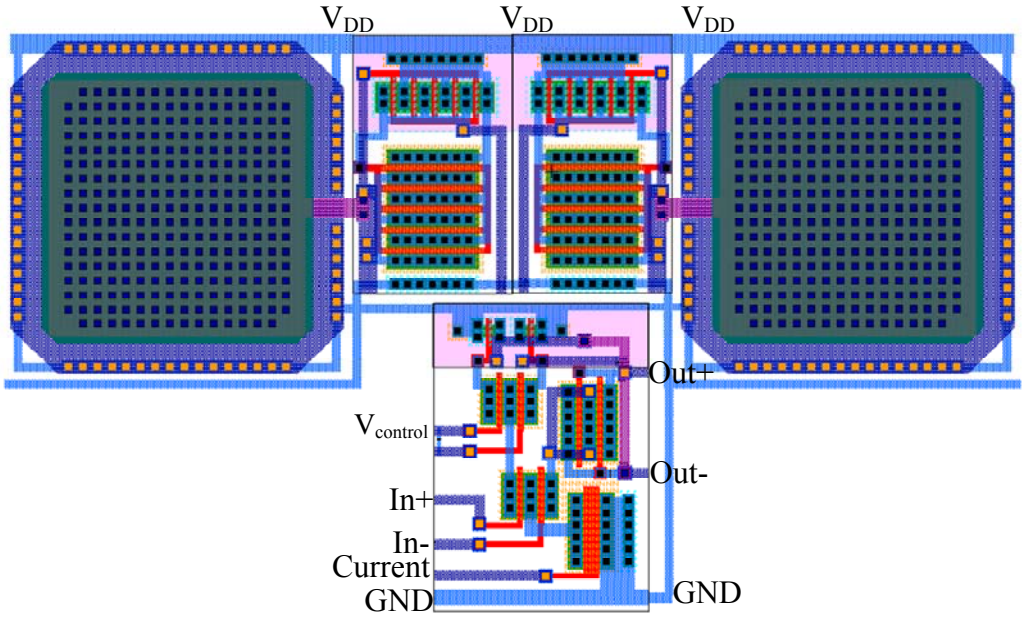


Figure 3.45.

Circuit layout for the active inductor oscillator. The output of the oscillator feeds into a mixer (also shown in this layout).

Simulation results

The frequency/voltage gain of the VCO is an important parameter, and can be depicted in form of the VCO output frequency as a function of input voltage range as shown in Figure 3.46. The output frequency of the VCO is dependant on the input current to the biasing section of the negative g_m resistor configuration.

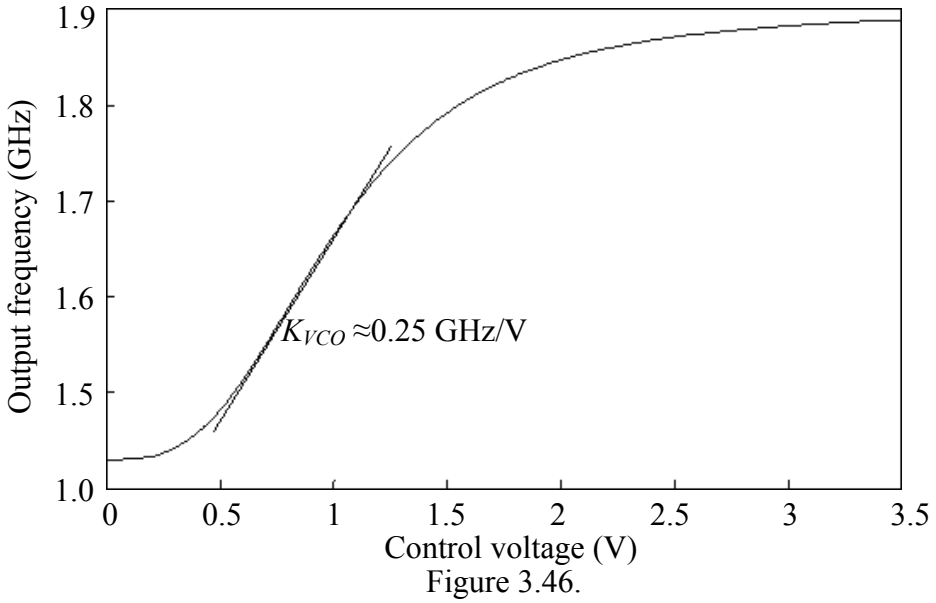


Figure 3.46.

Plot of the output frequency against the input voltage.

In Figures 3.47 and 3.48: A transient analysis is done at two different frequencies, relevant plotting is also done in the frequency domain, respectively.

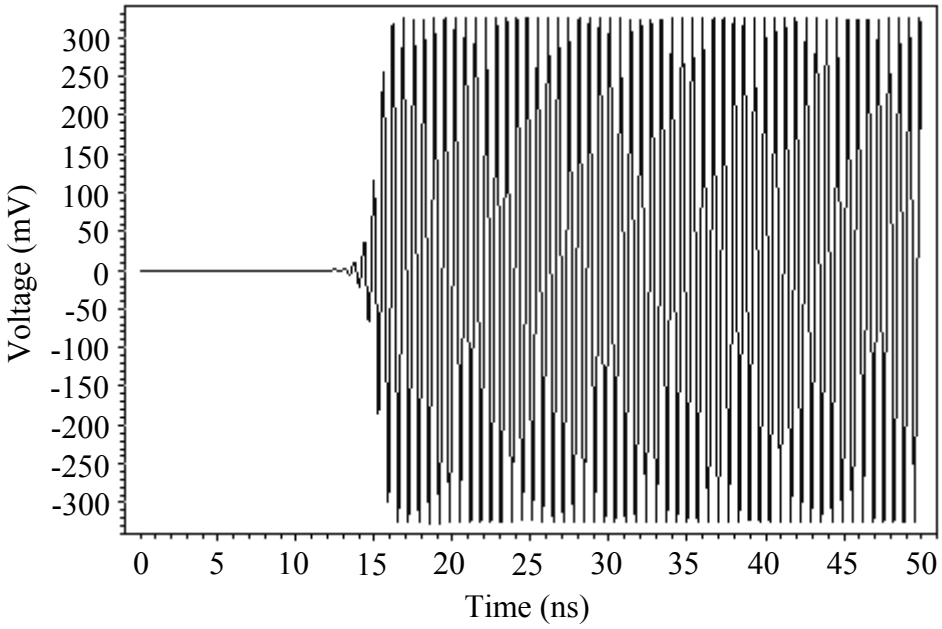


Figure 3.47.

Transient analysis to show the output signal for the 1.5 GHz active inductor oscillator.

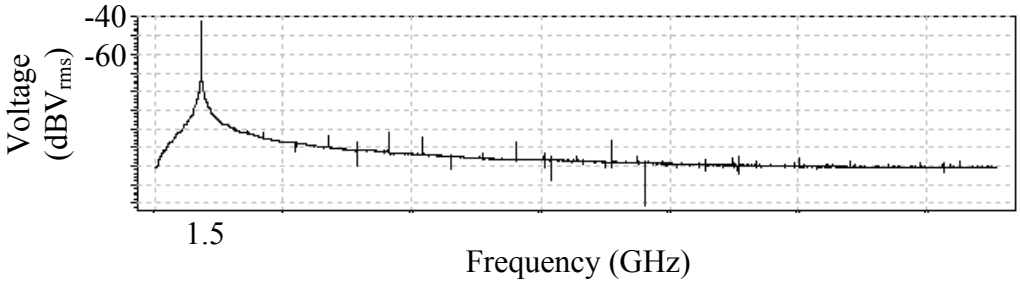


Figure 3.48.

Frequency domain analysis to show the output of the 1.5 GHz active inductor VCO.

Figure 3.47 shows the oscillator output qualifies as a sinusoidal signal. Higher frequency components cause the system output to have a slight distortion, but the first signal component is distinguished to serve as the main signal component influencing mixing (Figure 2.17).

3.8 Integrate and dump

The integrate and dump operation serves to transform the sequence representation of the bits into a ramp like signal that can be processed more easily. The integration process also removes any high frequency terms that remains after mixing and determines the bandwidth of the DDC-CRL.

Two integrate and dump circuits were considered [73], each operating on the principle that at the end of each bit period, the reactive element (a capacitor) is rapidly discharged. The two integrators considered were an active inverting integrator and a non-inverting or Deboo integrator [45]. Both make use of an op-amp as the active element. The most important aspect of the output signal of the integrator is that the signal magnitude is equal for both positive and negative inputs, this is referred to as having a balanced output. The design of the op-amp is documented in Appendix A, and a negative supply voltage is used – as discussed in the next section. The bulk connections are connected to this negative reference.

The inverting integrator has the advantage of having a lower component count and will occupy a smaller area on the silicon substrate. The output of the inverting integrator is inverted and is prone to having a DC offset. The offset is caused by the input offset voltage of the op-amp used. Realizing a balanced output with correct polarity and a stable DC offset requires excessive conditioning circuitry when compared to the non-inverting integrator.

The non-inverting integrator, or Deboo integrator, produces a non-inverted output with no DC offset. Only the input offset voltage of the op-amp must be compensated for to ensure that the output is balanced.

Figure 3.52 shows the schematic of a Deboo integrator, and Figure 3.53 shows the schematic of an inverting integrator. The transfer function of the Deboo integrator is

$$H(s) = \frac{1}{sRC} \tag{3.103}$$

and that of the inverting integrator is

$$H(s) = -\frac{1}{sRC} \tag{3.104}$$

The magnitude of RC, determines the aggressiveness of the integrator [31]. RC is chosen such that the output of the integrator is approximately a linear ramp.

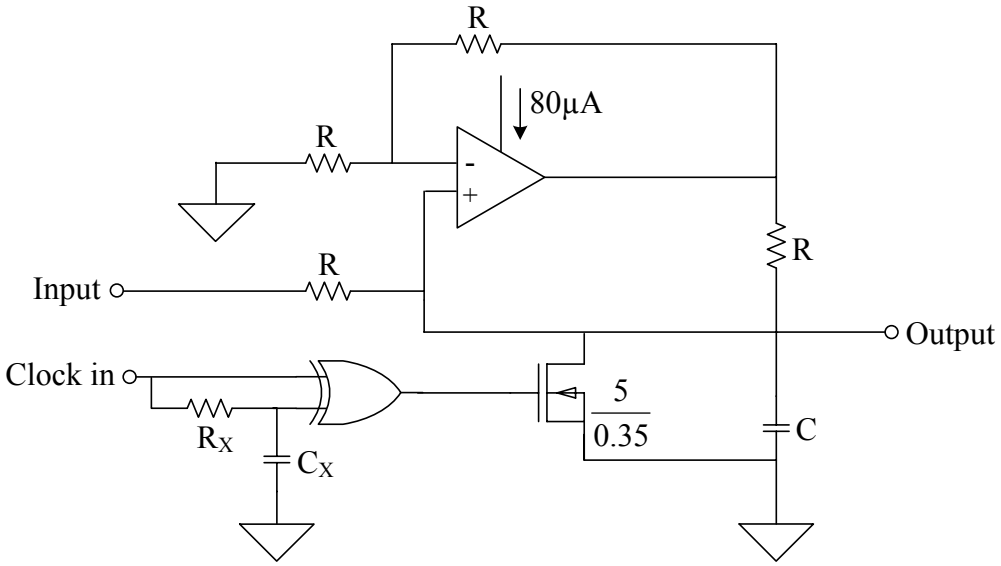


Figure 3.52.

Non-inverting or Deboo integrate and dump (C = 3.5 pF, C_X = 1 pF, R = R_x = 10 kΩ).

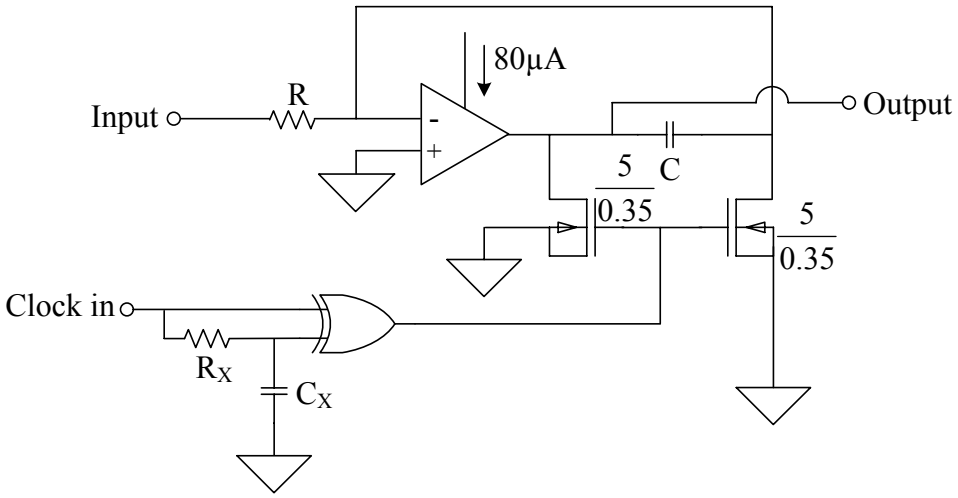


Figure 3.53.

Inverting integrate and dump (C_x = 1 pF, R_x = R = 10 kΩ, C = 3.5 pF).

Both integrators use a pulse to reset the capacitors. The pulse is generated by means of a clock signal and an exclusive OR (XOR) gate. The clock signal is XORed with a delayed version of the clock. The XOR gate outputs 3.3 V when there is a difference between its two inputs. This amounts to a pulse with duration given by

$$\tau_{delay} = R_x C_x \tag{3.105}$$

Integrator design

The pulse turns on the transistors connecting the capacitor terminals to ground, pulling the output of the integrator to ground and creating a low resistance path to ground through which the capacitor discharges.

The maximum specified bit rate for the DDC-CRL is 1 Mbps, or 1 bit every 1 µs. The discharging of the capacitor in the integrator should ideally instantaneous, but the transistors only offer a low resistive path and not a true short. To ensure that the capacitor fully discharges, the pulse must have a duration equal to the time it takes the capacitor to discharge from its maximum possible value after one integration period.

To ensure that the capacitor performing integration is always discharged at the end of each reset period without introducing excessive 'dead time' at the output, pulse length was chosen to be 10 ns, or 100th a bit period. From equation (3.105), R_x = 10 kΩ and C_x = 1 pF.

The data in the received signal occupies a maximum double sided bandwidth of 20 MHz, the demodulated signal occupies half this bandwidth, or 10 MHz. The highest frequency difference term present in the demodulated signal is assumed to not exceed 10 MHz. To acquire a linear ramp output from the integrator, integration should be linear over the signal bandwidth. This can be achieved by setting the integrators bandwidth to be 50% larger than the demodulated signal. C can the be determined from (R is fixed to 10 kΩ)

$$C = \frac{1}{1.5 f_b R} \tag{3.106}$$

which yields C = 3.5 pF.

In testing, the non-inverting or Deboo integrator was chosen above the inverting integrator. Lower total component count and a non-inverted output with 0 V DC offset made the Deboo integrator the preferred choice.

The layout of the integrate and dump circuit is shown in Figure 3.54.

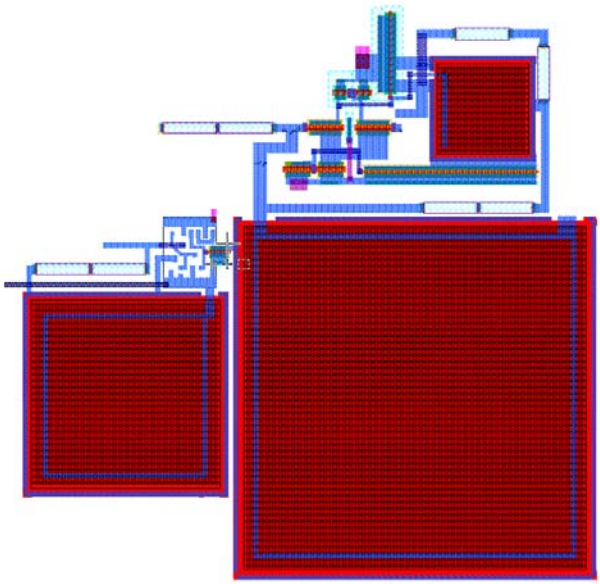


Figure 3.54.

Layout for the integrate and dump sub-system.

Simulation results

Figure 3.55 shows the simulated output of the integrate and dump circuit: the parameters under study are the linearity of the ramp produced by the integration operation as well as the reset time after each integration period.

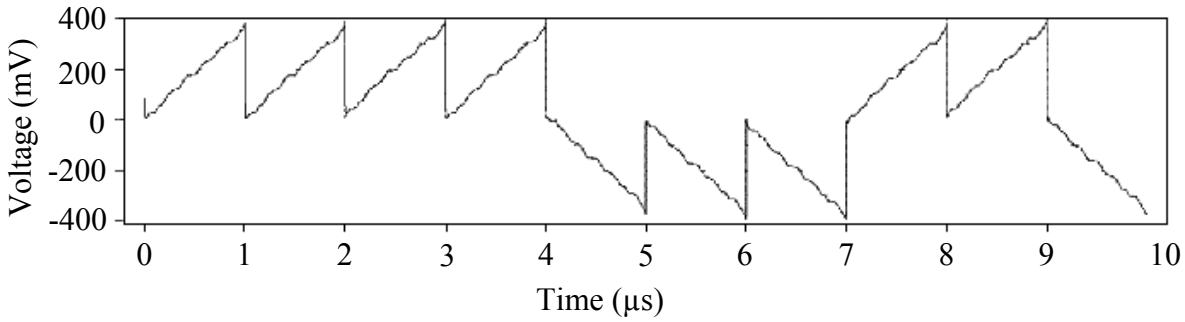


Figure 3.55.

Simulation results to validate the operation of the integrate and dump sub-system.

The reset time is within 10 ns. Certain imperfections in the ramp signal are noted, however does not affect parameters of interest to the DDC-CRL.

3.9 Comparator

Two comparator topologies were initially considered, a simple two stage comparator and a more complex comparator with hysterisis. Earlier attempts to design a comparator with hysterisis proved difficult and yielded unsatisfactory results.

Hysterisis was considered as a technique to reduce the effects of noise on the comparator output. Simulations of the integrate and dump output suggested that hysterisis would be detrimental to the system. In the case of frequency mismatch between the received signal and the local carrier reference, difference terms are produced during demodulation, hysterisis suppresses high frequency difference terms. Suppression of high frequency difference terms decreases the change in the error produced by the phase detector for a given frequency error. This decrease is not desirable.

The comparator topology implemented is shown in Figure 3.56. The design is based on a two stage comparator design [46]. The comparator topology shown in Figure 3.56 is similar to that of an operational amplifier, with some minor changes.

The comparator consists of two-stages: a differential input stage and a current sink inverter drive stage. The differential input stage is used to precisely control the point at which the comparator trips positive or negative. The inverter serves to swing the comparator positive or negative in the presence of a large capacitive load. The output stage converts the output to a form compatible with CMOS digital logic levels.

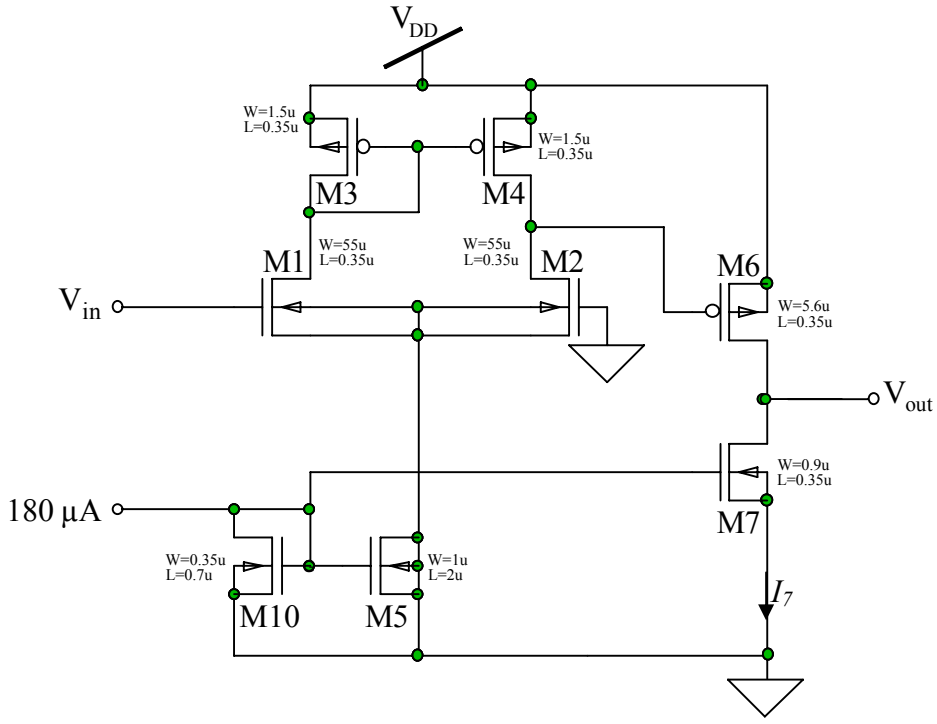


Figure 3.56.

Circuit of a two-stage comparator.

C_L is the load capacitance seen with respect to the output terminal.

Figure 3.56 has a clear resemblance to the amplifier in Figure 3.11. The most obvious differences are that there is no compensating capacitor and that the body of the two input transistors is connected to the source and not V_{SS}. By connecting the body of the transistors to the source terminal, the body effect can be exploited to make the transistor more sensitive to changes on its gate. The body effect is where the body of the transistor behaves like a second gate.

The comparator design procedure is similar to that of the telescopic amplifier. The primary specifications of the comparator are its slew rate (SR) and trip point, the input voltage at which the comparator switches its output. Comparator design starts by defining the slew rate for a specific load. This specification is used to determine the value of I_7 given by

$$I_7 = C_L\left(SR\right) \tag{3.107}$$

$(W/L)_6$ and $(W/L)_7$ are determined from the maximum desired output swing. $(W/L)_6$ and $(W/L)_7$ are determined by

$$V_{DS(sat)} = \sqrt{\frac{2I}{k`\left(\frac{W}{L}\right)}} \tag{3.108}$$

The second stage gain is calculated using

$$A_{v2} = \frac{-g_{m6}}{g_{o6} + g_{o7}} = \frac{-g_{m6}}{I_6\left(\lambda_6 + \lambda_7\right)} \tag{3.109}$$

For the comparator to have balanced operation around the reference specified at the gate of M2, the following relationship must be satisfied.

$$\frac{\left(W/L\right)_6}{\left(W/L\right)_4} = 2\frac{\left(W/L\right)_7}{\left(W/L\right)_5} \tag{3.110}$$

$(W/L)_1$ and $(W/L)_2$ are designed for a user specified gain. The open loop gain of the comparator is typically several thousand V/V, and the first stage gain must be designed to compensate for the low voltage gain in the second stage. The first stage gain is specified by

$$A_{v1} = \frac{-g_{m1}}{g_{o2} + g_{o4}} = \frac{-2g_{m1}}{I_5\left(\lambda_2 + \lambda_4\right)} \tag{3.111}$$

It is assumed that the M1, M2 transistor pair are matched as well as the M3, M4 pair. $(W/L)_5$ can be determined from the relation

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_7\left(\frac{I_5}{I_7}\right) \tag{3.112}$$

Once all ratios are calculated, $(W/L)_3$ and $(W/L)_6$ are adjusted for proper balanced operation.

Comparator design and analysis

The comparator was designed for a slew rate of 1000 V/µs for a 10 pF load capacitance and an open loop gain of 2000 V/V. Linearity and stability do not form part of the specification because they have little affect of the comparators performance.

From equations (3.108) and (3.109), $(W/L)_6$ and $(W/L)_7$ can be determined for an output swing of 2 V. Initial ratios for $(W/L)_6$ and $(W/L)_7$ are 1 and 0.5 respectively. Using these ratios a second stage gain of –10 V/V is calculated.

To meet the specification of 2000 V/V, the first stage gain is set to -200 V/V. This yields a (W/L) ratio for transistors M1 and M2 of 143 using (3.111).

The remainder transistor ratios are determined using Equations (3.110) and (3.112).

The layout of the comparator is shown in Figure 3.57.

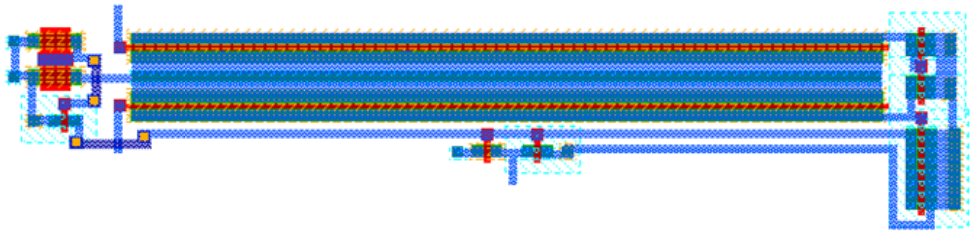


Figure 3.57.
Layout of the comparator.

Simulation results

Figure 3.58 shows a simulation of the comparator.

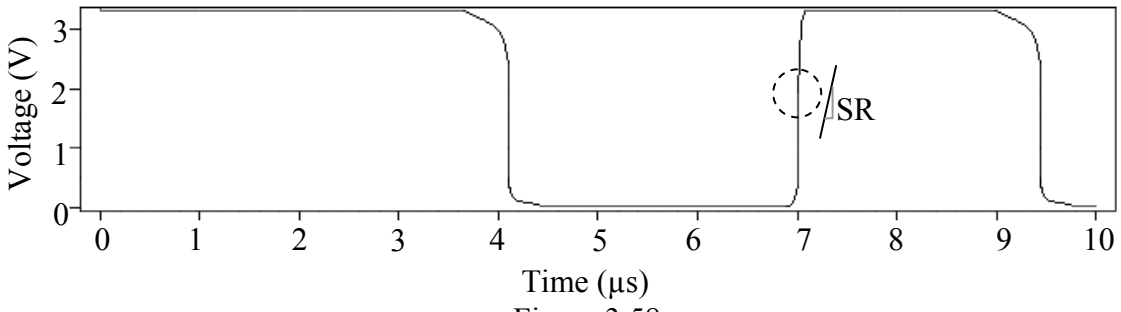


Figure 3.58.
Output waveforms of the CMOS comparator. The positive slew rate (SR) can be determined by analyzing the slope

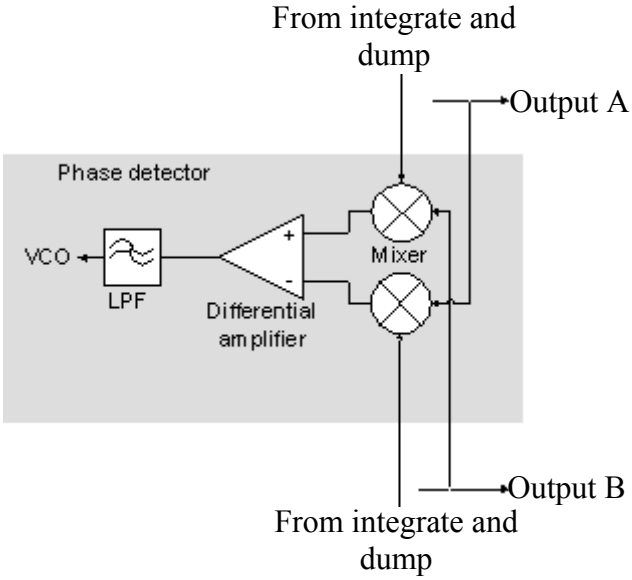
The CMOS comparator initially shows a delayed response to a bit change, but the delay decreases substantially as the system powers up. The initial delay is attributed to the combined effects of system startup and the non-ideal nature of the ramp waveform from the integrate and dump circuit. Delay is not apparent after 5 µs, suggesting that the system has stabilized after power up and comparator operation is acceptable.

3.10 Phase detector

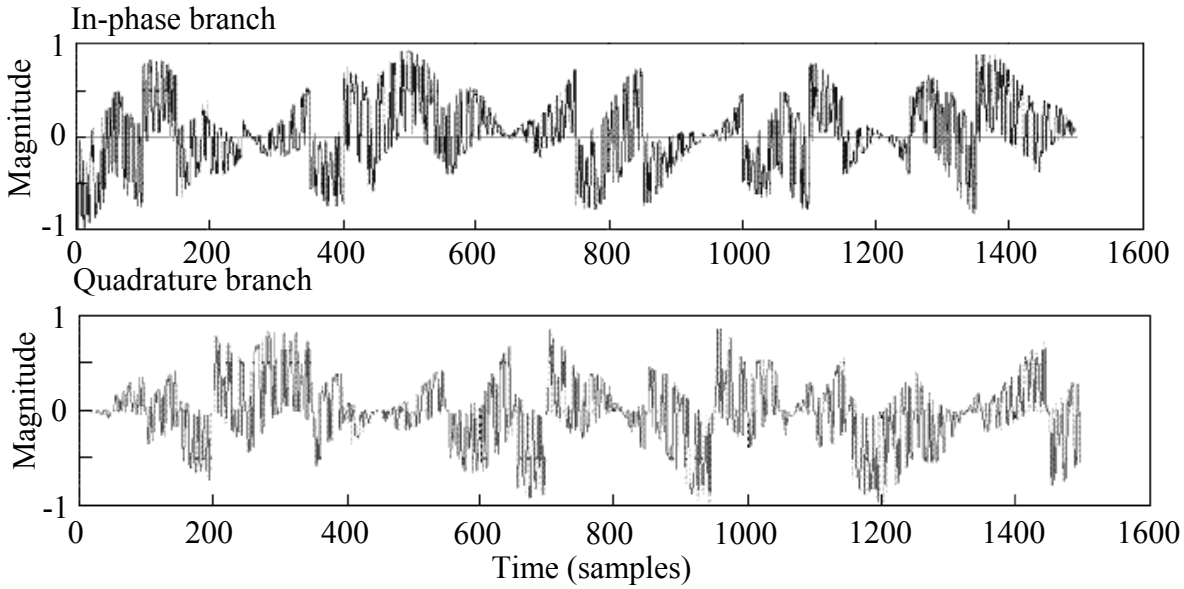
The phase detector compares the in-phase and quadrature branches and determines the magnitude and sign of the frequency difference between the received signal and the reference carrier in the receiver. The premise behind the operation of the phase detector is that increased mismatch between the in-phase and quadrature branches increases the magnitude of the error signal generated by the phase detector.

After demodulation, the difference term present on the in-phase and quadrature branch is of the same frequency but with a 90° phase difference. The effect of this term on the demodulated signal is shown in Figure 3.59 (b).

As the difference term increases or decreases, its net effect on the recovered data stream also increases or decreases. As the difference term approaches 0 Hz, the phase detectors output will stabilize around some DC value. If the phase difference between the two branches is not equal to 90°, the phase detector output will vary slowly around the DC output for a specific error. This slow variation is used to adjust the phase of the local carrier reference to match that of the received signal.



(a)



(b)

Figure 3.59 [73].

(a) A block diagram showing the position of the phase detector in the DDC-CRL.

(b) 90° phase difference between the in-phase and quadrature branches of the DDC-CRL. The variations in the magnitude are due to the sum and difference terms composed, and also due to the imperfections in the integrator.

Two phase detectors were initially considered (Chapter 2). Both were rejected in favour of a hybrid design. All phase detector designs consist of 3 stages (Figure 3.59 (a)): a multiplying stage that multiplies the integrated signal from one branch (Figure 2.20) with the comparator output of the opposite branch (Figure 2.20), a subtraction stage that calculates the difference between the outputs of the multiplying stage, and a low pass filter, which extracts the DC component from the calculated difference.

The alternatives considered only differ in the way that multiplication is performed. The first alternative used the most direct approach to multiplication, using analogue mixers to perform the multiplication. The excess amount of bias circuitry required to condition the inputs led to the rejection of the design.

A digital approach to phase detection using XOR gates to perform multiplication [45]. This method of multiplication was rejected because the input from the integrator is analogue in nature.

The design used to implement the phase detector is a hybrid of the two design

alternatives. Analogue multipliers are used to perform the multiplication, but the digital nature of the comparator output allows for the multipliers to be significantly simpler than analogue mixers.

Multiplier

Multiplication requires an analogue signal to be multiplied by a digital signal, a task that is easily performed if the digital signal is used to control a switch through which the analogue signal must pass. This is the concept used to design a hybrid phase detector that mimics the output of a phase detector based on analogue mixers. Figure 3.60 illustrates this concept.

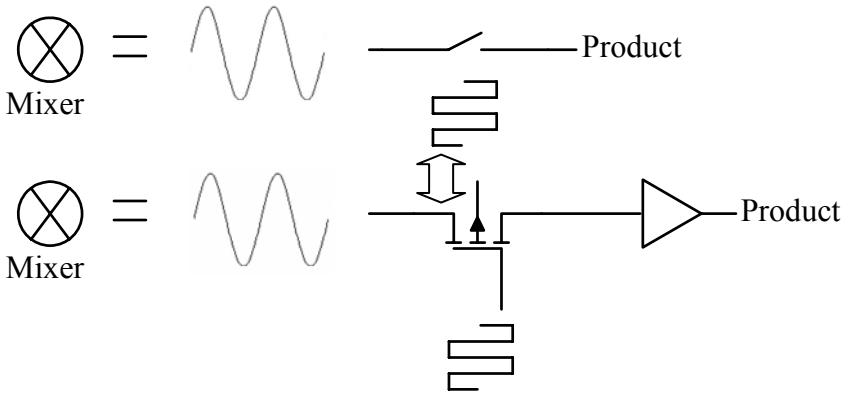


Figure 3.60.

Hybrid phase detector multiplier (as utilized in Fig. 3.59 (a)) concept.

The conceptual circuit in Figure 3.60 can be extended to provide an inverted output when a 'low' bit is present on the switch, effectively providing multiplication by –1. The multiplier shown in Figure 3.61 demonstrates this, and is the topology used in the DDC-CRL's phase detector. The amplifier used as the multiplier has each of the input terminals connected to a pair of NMOS switches. The switch pair controlling multiplication by +1 is controlled by the digital input, while the pair controlling multiplication by –1 is controlled by the inverse of the digital input.

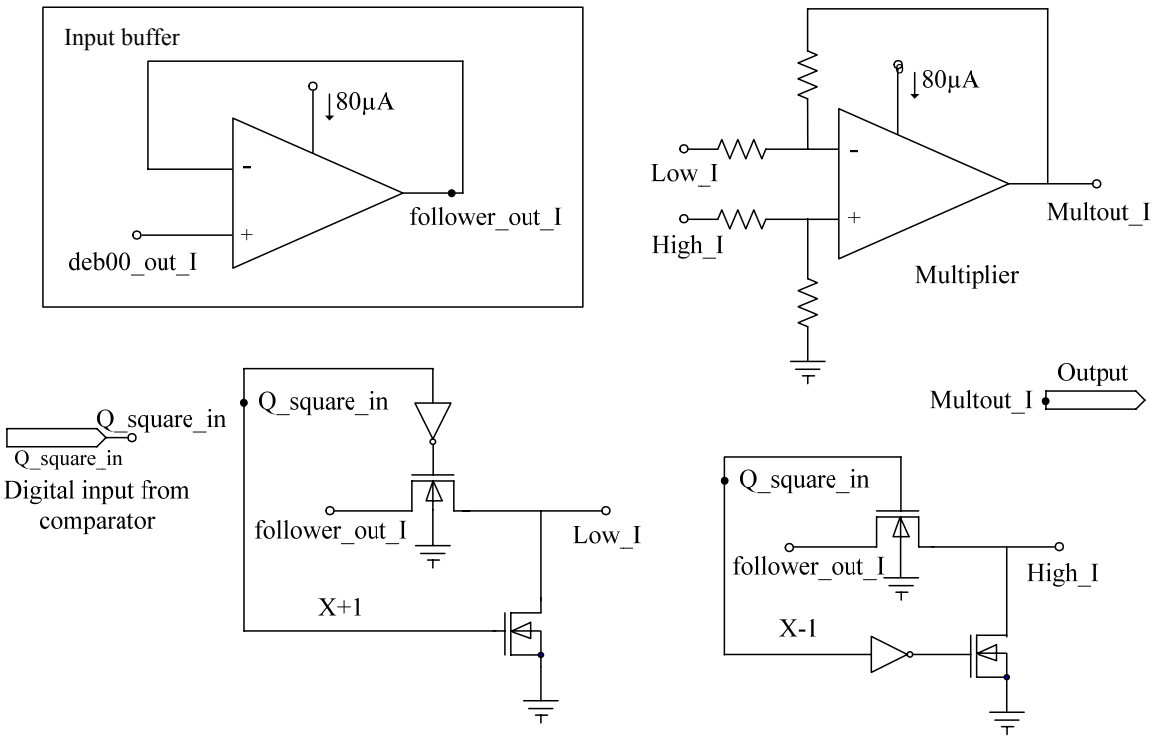


Figure 3.61.

Topology for multiplying a bi-polar digital signal with an analogue signal.

A digital high (at node `Q_square_in`) routes the analogue signal to the non-inverting terminal of the op-amp and grounds the inverting terminal, resulting in the analogue input simply passing through unchanged. Similarly, a digital low configures the multiplier to invert the input signal. This results in the output resembling the multiplication of an analogue signal with a bipolar digital signal.

The values of the resistors in the resistive network of the op-amp are 10 kΩ, providing a balance output for either configuration. The (W/L) ratios of the NMOS switches are 10. A large width increases switching speed, whereas a small length minimizes the on resistance, r_{ds}, of the transistor.

Difference amplifier

The phase detector's error signal is obtained by taking the difference of the multiplier outputs. The difference is determined by an op-amp in a difference amplifier configuration. A standard differential amplifier is not suitable because the output of a differential amplifier has an undesired DC offset. The output of a difference amplifier is given by [45]

$$v_O = \frac{R_2}{R_1}(v_2 - v_1) \tag{3.113}$$

where v_2 and v_1 are the inputs of the difference amplifier. The main advantages of the difference amplifier over a differential amplifier are the ability to weight the inputs and the use of feedback ensures a precise and stable output.

Figure 3.62 shows the difference amplifier used in the DDC-CRL. R_1 and R_2 are set to 10 kΩ.

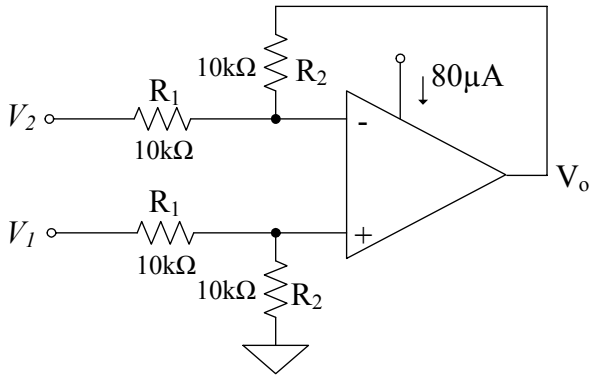


Figure 3.62.

Difference amplifier of the DDC-CRL's phase detector.

Low-pass filter

The LPF used in the DDC-CRL is a first order passive low pass filter as shown in Figure 3.63.

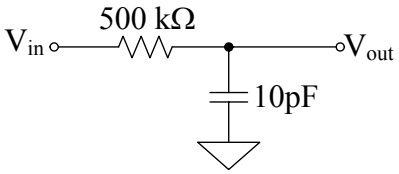


Figure 3.63.

First order passive low pass filter.

The cut off frequency of the LPF is given by

$$f_c = \frac{1}{2\pi RC} \tag{3.114}$$

where R and C are the values of the resistor and capacitor in Figure 3.63. The chosen cut off frequency is 30 kHz, which yields: R = 500 kΩ and C = 10 pF.

The large values of R and C can be implemented in CMOS, but are instead implemented externally. The value of f_c can be used as a tuning parameter to adjust the step response time of the DDC-CRL. Larger values command a faster response but with higher susceptibility to low frequency noise within the DDC-CRL. A first order passive filter is

considered suitable for rejecting the AC component of the phase detector output because higher order filters only offer greater attenuation at higher frequencies, when the primary concern is low frequency components within the pass band of the filter. The first order step response is also preferred, as an aggressive second or third order step response is characterized by a degree of overshoot, despite lower settling time. Overshoot will drive the VCO to a higher frequency than desired, introducing further error in to the system and causing the VCO output to first 'bounce' around the desired operating frequency before stabilizing. The CMOS layout of the phase detector is shown in Figure 3.64.

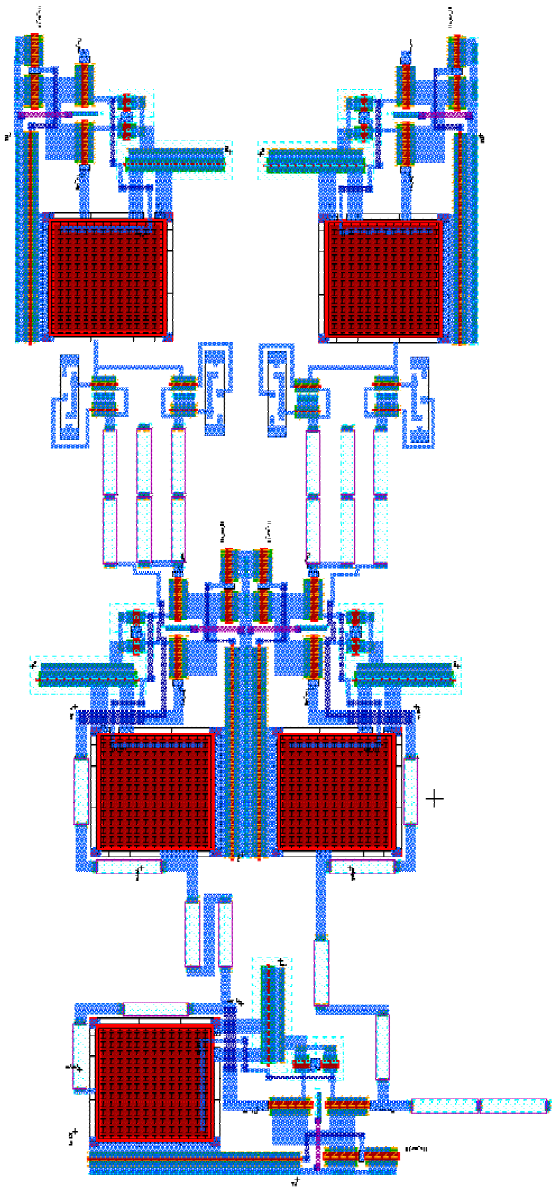


Figure 3.64.

CMOS layout of phase detector. The following sub-systems are included: multipliers, buffers, digital switching and difference amplifier.

Simulation results

The primary parameter of concern is the linearity of the error signal, i.e. the amount of distortion prior to the introduction of a frequency error into the system. This is considered critical to the operation of the system, as it directly affects the performance of the VCO generating the reference carrier.

Figure 3.65 shows the output of both phase detector multipliers (on the top axis), with the filtered and unfiltered error signals shown on the bottom axis.

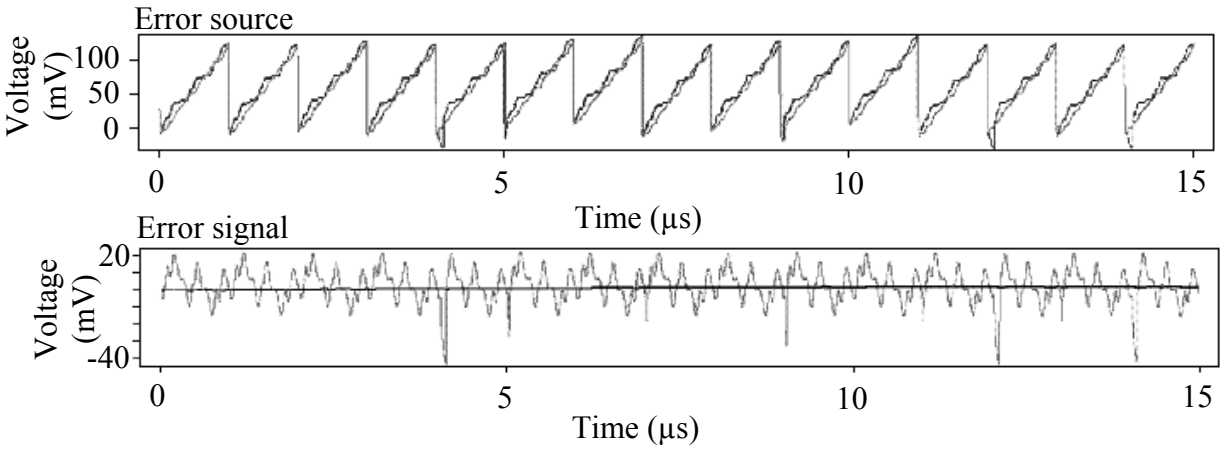


Figure 3.65.

Waveforms within the phase detector for 0 phase and frequency error when a length 13 sequence is used.

Figure 3.66 shows the phase detector output for a sequence with a length that tends to infinity for the ideal low pass filter (time constant tending to 0 s) in the phase detector. The output from both multipliers is shown on the lower set of axis, with the error signal shown on the upper axis.

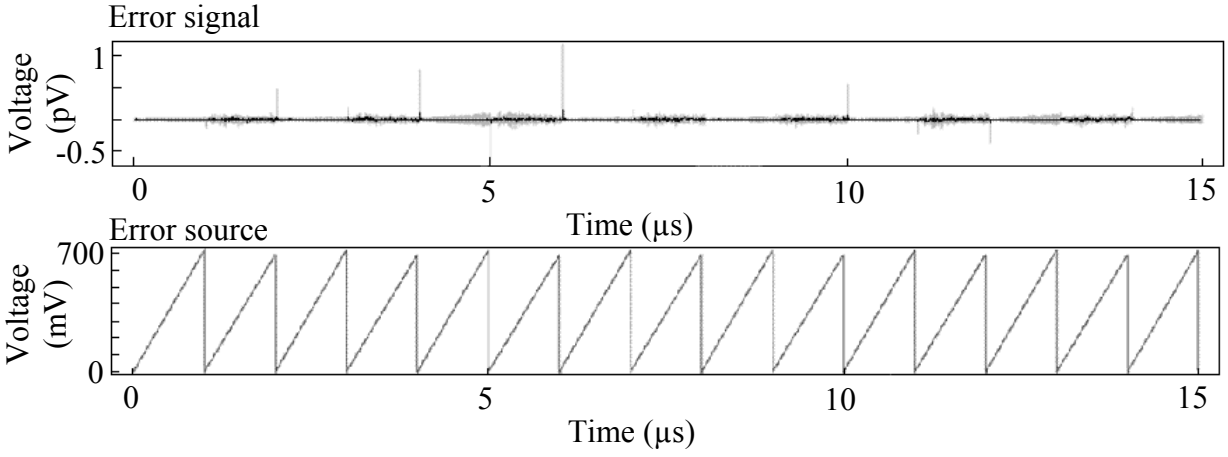


Figure 3.66.

Shown are phase detector wave forms if the sequence length tends to infinity.

The output of the phase detector multipliers is an approximate saw tooth wave for both the in-phase and quadrature branches. The error signal derived from the two saw tooth waveforms reflects the differences in the two ramps. The magnitude of the filtered error signal is approximately –2 mV. The output of the phase detector for a sequence of infinite length and ideal LPF is approximately 0 V.

The varying gradient present on the ramps generated by the integrate and dump circuit has a significant effect on the phase detectors output signal. The deviations from the desired gradient manifest as low frequency distortion on the error signal. The net effect of the distortion on the system results in phase jitter, as the VCO can not distinguish between the DC error signal and the distortion, causing the VCO output to deviate slowly about the desired frequency.

Figure 3.66 shows that if the sequence is made very long and the low pass filter ideal, the ramps generated by the integrate and dump circuit approach those generated for an infinitely long sequence. The error signal derived from these ramps is more refined, with significantly less distortion.

Figure 3.67 shows the results of a frequency error.

3.11 Summing circuit

The summing circuit is used at 2.4 GHz frequency. It adds the modulated spread signals before transmission. It can be implemented by forcing the drain currents from the amplifier in the common-source configuration into a node and by using a resistor to convert the sum current into voltage.

If a transistor is switched on, the total drain current will be [47]

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2 \ , \tag{3.115}$$

which for small signals simplifies to

$$i_D = I_D + k'_n \frac{W}{L} (V_{GS} - V_t) v_{gs} \tag{3.116}$$

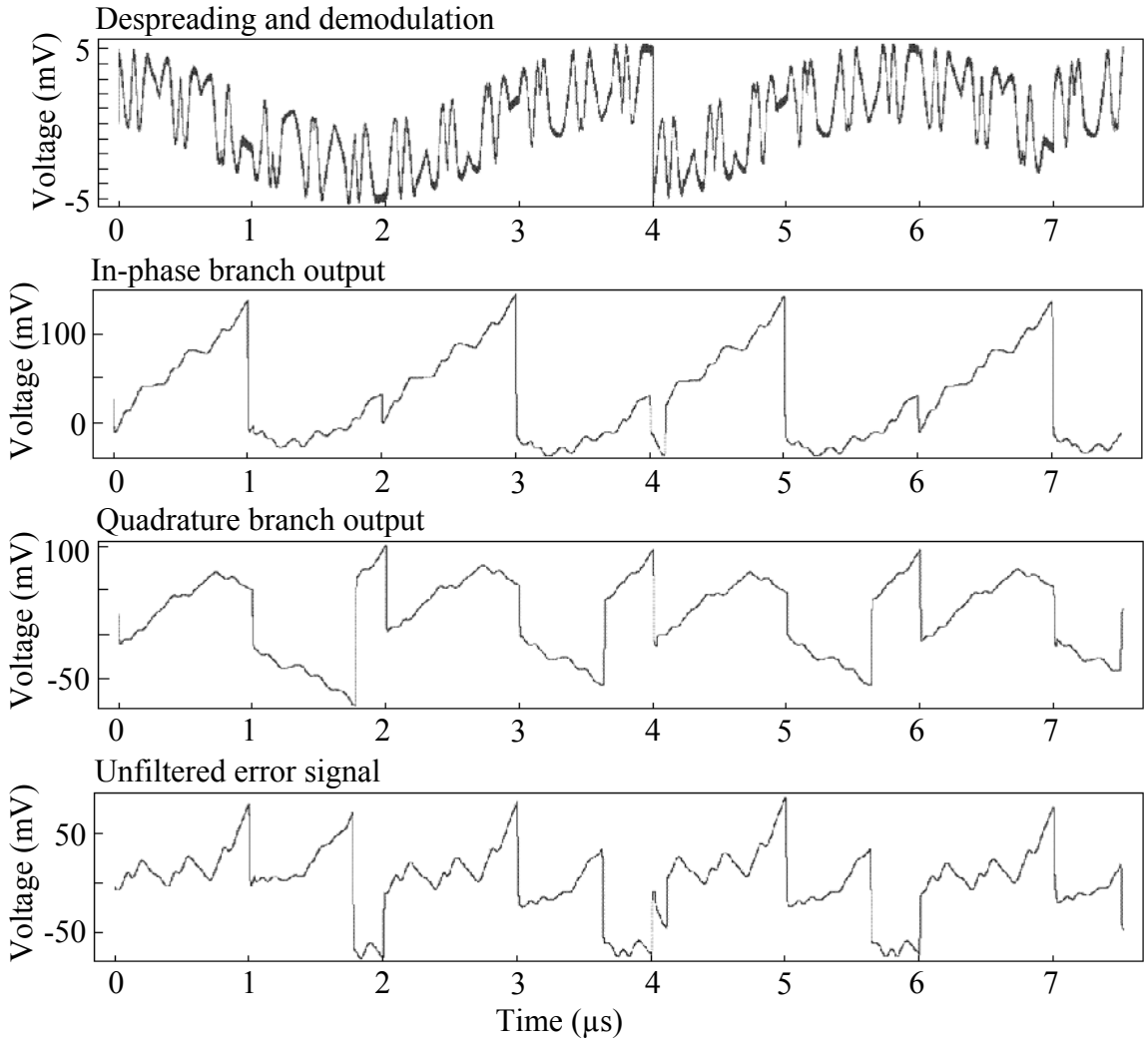


Figure 3.67.

Effect of a 250 kHz positive frequency difference on various waveforms of the DDC-CRL.

AC current, for $v_{gs} << 2(V_{GS} - V_t)$, is given by

$$i_d = k'_n \frac{W}{L}(V_{GS} - V_t)v_{gs} \tag{3.117}$$

For a specific biasing the V_{GS} is also constant, and i_d is essentially

$$i_d = g_m v_{gs}, \tag{3.118}$$

where $g_m = k'_n \frac{W}{L}(V_{GS} - V_t)$.

Forcing four currents into a node will result in the addition of AC v_{gs} (if identical biasing and transistors are assumed), i.e.

$$i_{d1} + i_{d2} + i_{d3} + i_{d4} = g_m(v_{gs1} + v_{gs2} + v_{gs3} + v_{gs4}) \tag{3.119}$$

The circuit used in the system is shown in Figure 3.68.

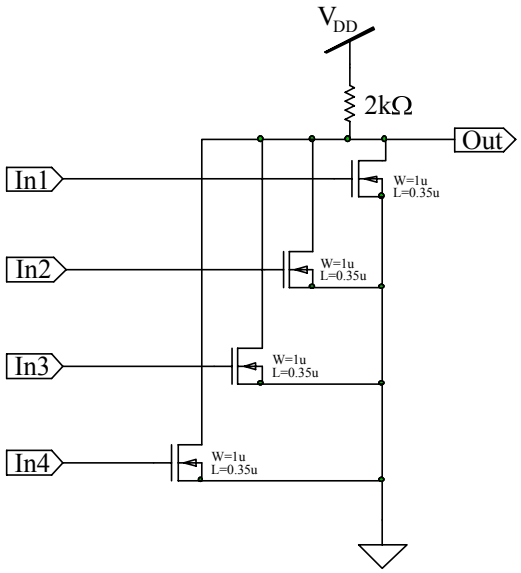


Figure 3.68.

Summing circuit.

The chosen component values (W/L=3 and R = 2 kΩ) result in the calculated AC voltage gain of about 1. The CMOS layout of the summing amplifier is shown in Figure 3.69.

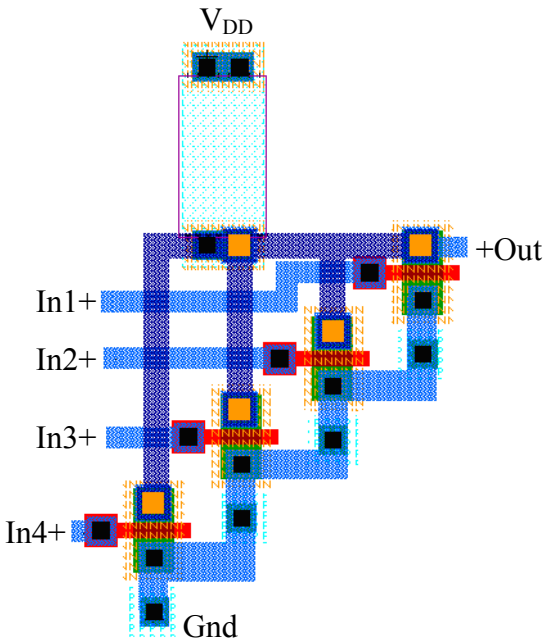


Figure 3.69.

Layout of the summing amplifier.

3.12 High-frequency buffer

Equations and parameters described in these sections present very good approximations for the low frequency operation of a transistor-based circuit. With the increased frequency of

operation, unfortunately, some approximations can no longer be used. A high-frequency model is proposed in Figure 3.70.

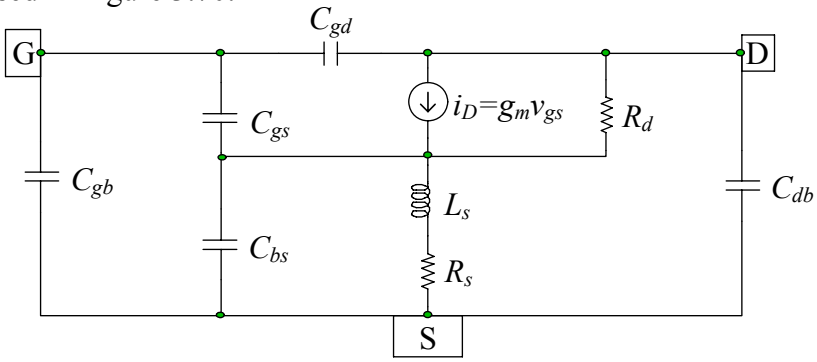


Figure 3.70.

High frequency small signal of an NMOS transistor.

The most commonly used approximation in designing transistor circuits is that the input resistance of a MOS transistor at the gate is infinite. At the low frequency operation this is true, but at high frequencies the effect of the gate-source capacitance (C_{gs}) and other parasitic capacitances becomes profound. The two-port admittance (y) parameters are applicable when analysing for the input resistance as this appears in shunt [47]. This was somewhat simplified, as shown in Figure 3.70 [48]. A few different equations for the input resistance are given in this source. One very complex equation is presented here, based only on the following approximations (X is the reactance and Z is the impedance of a passive component, and R_L is the load resistor not shown):

$$R_L \parallel X_{db} \approx R_L \tag{3.120}$$

$$R_d \gg R_s \tag{3.121}$$

$$R_d \gg R_L \tag{3.122}$$

$$X_{bs} \parallel Z_s \approx Z_s \tag{3.123}$$

$$g_m \gg 1 / R_d \tag{3.124}$$

If the quality factor of the inductor is

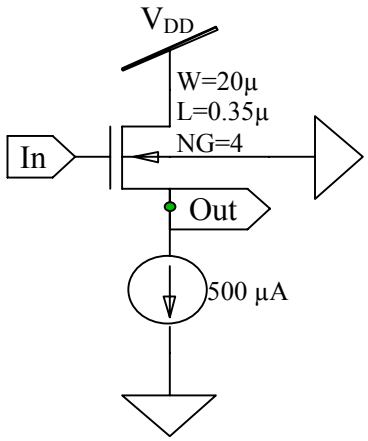
$$Q \approx 3 \tag{3.125}$$

then

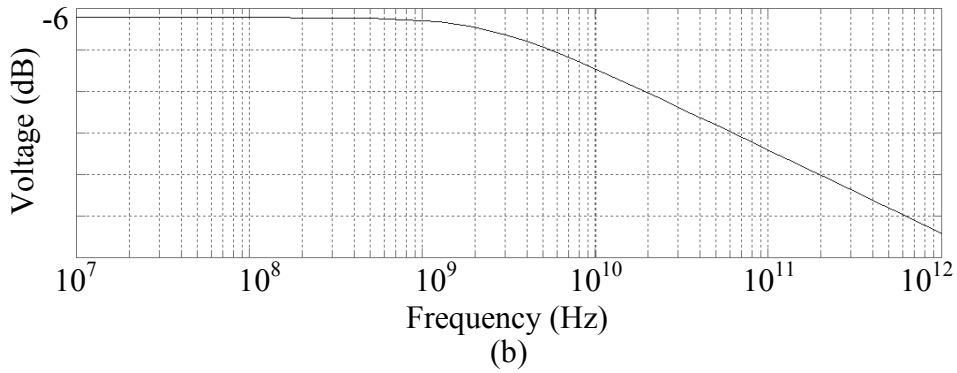
$$\mathrm{Re}(Z_{in}) = \frac{\frac{L_s}{C_{gs}} g_m \left(1+\frac{C_{gd}}{C_{gs}} g_m R_L \left(1-\omega^2 L_s (C_{gd}+C_{gb})\right)\right) + \left(1+\frac{C_{gd}}{C_{gs}} g_m R_L \left(1+\frac{C_{gd}}{C_{gs}}\left(2+g_m (R_L+R_s)\right)\right)\right)}{\left(1+\frac{C_{gd}}{C_{gs}} g_m R_L + \frac{C_{gd}+C_{gb}}{C_{gs}}(1+g_m R_s) - \omega^2 L_s (C_{gd}+C_{gb})^2\right)^2 + \left(\omega C_{gd}\left(\left(r_s+\frac{L_s}{C_{gs}} g_m\right)\left(1+\frac{C_{gb}}{C_{gd}}\right) + R_L (1-\omega^2 L_s C_{gb}) + \frac{L_s}{C_{gd} R_d}\right)\right)^2} \tag{3.126}$$

This is a very close, but tedious approximation of the input resistance of a transistor. In high frequency CMOS applications the infinite gate resistance of a transistor is replaced by the finite gate-to-source capacitance. This implies that when connecting stages the output impedance of the preceding stage must be small in order not to loose gain.

The problem of connecting stages can partially be solved by means of a high frequency buffer. This buffer must have a high bandwidth, the high level stability and lower output impedance than the preceding stage that the buffer is connected to. The source follower to be used for this application must be driven by a large current source (1 mA range). The transistor's *W*/*L* ratio must also be high, of any value from 50 to 600. The circuit diagram is shown in Figure 3.71.



(a)



(b)

Figure 3.71.

(a) High frequency buffer.

(b) Frequency sweep on the High frequency buffer.

3.13 Filter design

Whenever an LPF is required, simple RC LPF configuration of Figure 3.72 is used. This configuration has the transfer function

$$f = \frac{1}{2\pi RC} \tag{3.127}$$

This formula can be used to determine component values R and C for any cut-off frequency f specified.

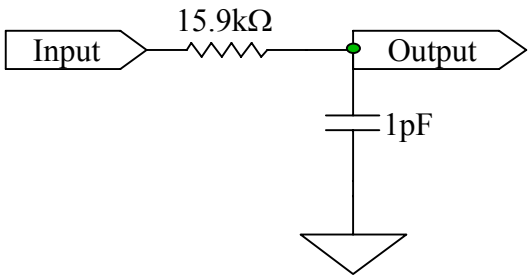


Figure 3.72.
Circuit diagram of the LPF.

3.14 Sequence processing circuit

Sequence processing circuit is an analogue circuit which is used to prepare spreading sequences for usage in the system. The same circuit is used both in the transmitter and receiver part of the system, and is connected to it via an analogue switch. Ideally, the real or imaginary part of the spreading sequence has values between -1 and 1, therefore for further processing, it has to be offset to a DC value. A simple transistor-based one-to-two voltage divider is used here. The real or imaginary part of the sequence is then used with or without inverting. For inversion, a common source inverter with enhancement load is used.

The inverter has the gain given as [47]

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \tag{3.128}$$

(disregarding the Early effect). Lengths of approximately 1 µm and widths of 1.5 µm were used to establish the gain of approximately one. The complete design is shown in Figure 3.73.

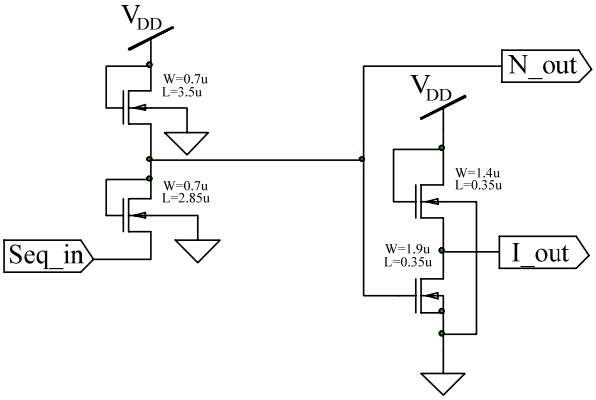


Figure 3.73.

Sequence processing circuit.

3.15 Power amplifier

In the system for this thesis, and for most communication applications, in general, only fundamental output power is considered to be allowed to reach the output load, filtering out harmonic components, thus leading to the following definition for drain efficiency η,

$$\eta = \frac{P_{out,f}}{P_{dc}} = \frac{P_{out,f}}{P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf}} \tag{3.129}$$

In this expression, P_{diss} and $P_{out,nf}$ take into account the output network characteristics. If the latter is an ideal lowpass filter, then $P_{out,nf} = 0$ for $n > 1$, while P_{diss} already accounts for the power reflected by the filter towards the device. From (3.129), maximum drain efficiency is obtained if

$$P_{diss} + \sum_{n=2}^{\infty} P_{out,nf} = 0, \tag{3.130}$$

that is, if $P_{diss} = 0$ and $\sum_{n=2}^{\infty} P_{out,nf} = 0$. Maximum drain efficiency can therefore be obtained if the fundamental output power $P_{out,f}$ is maximized, or the sum of P_{diss} and $P_{out,nf}$ $(n > 1)$ is minimized.

Class F power amplifiers can provide the highest power added efficiency while still linear enough [48]. The basic principles of operation of the Class F amplifier as illustrated in Figure 3.74 [49] are as follows.

- Fundamental-frequency drain voltage and current are shifted in phase by 180˚ from each other.
- The voltage waveform adds odd harmonics to build its shape towards a square wave.
- The current waveform adds even harmonics to build its shape towards a half sine wave.
- No power is generated at the harmonics because there is either no voltage or no current present at a given harmonic.
- At microwave frequencies, the number of harmonics is usually relatively small.
- The RF-power device acts as a saturating current source. Only when all harmonics are properly terminated can it act as a true switch.

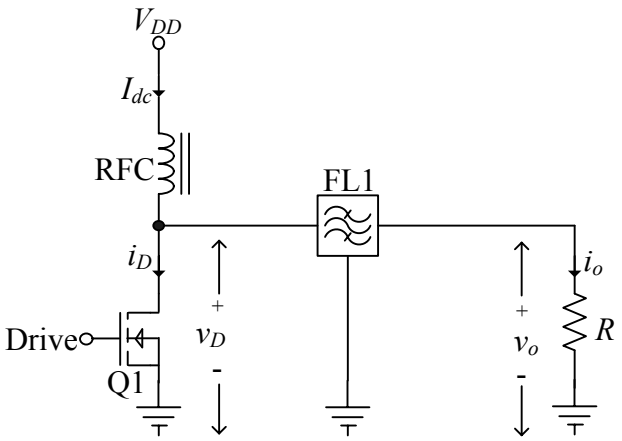


Figure 3.74.

Simplified circuit diagram for a class F amplifier [49].

The gain coefficient can be defined as the ratio between the fundamental-frequency component and the minimum value (excluding DC), assumed by the voltage waveform. It is shown that for a maximum gain coefficient, the ratio between fundamental and third harmonic drain voltage components (ε_3) must be -7.5 < ε_3 <-4.5 [51]. The DC power consumption is unaffected by third harmonic flattening, but output power drain efficiency is increased by the gain coefficient. The choice of ε_3 automatically determines the optimum third harmonic loading. It can also be noted that the power dissipation can be more than halved if a bias point close to pinch-off is selected allowing a major reduction in P_{diss}. Figure 3.75 shows that the maximum efficiency of an ideal power amplifier increases from 50 % of a class A up to 100 % for infinite harmonic traps. The power amplifier design was adapted from [72].

The input and output matching networks can be provided using passive element matching networks such as a L-network, a T-network and a Π-network. The discrete elements for the matching network can also be used as coupling capacitors and inductor chokes. A differential amplifier will act as the pre-amplifier and the biasing network [45]. Since this topic has been discussed earlier in this thesis, it will not be repeated. For the current source, a negative voltage (dc) source was required. The negative voltage source is a ring oscillator with a negative biased diode rectifier, a filter and a voltage regulator.

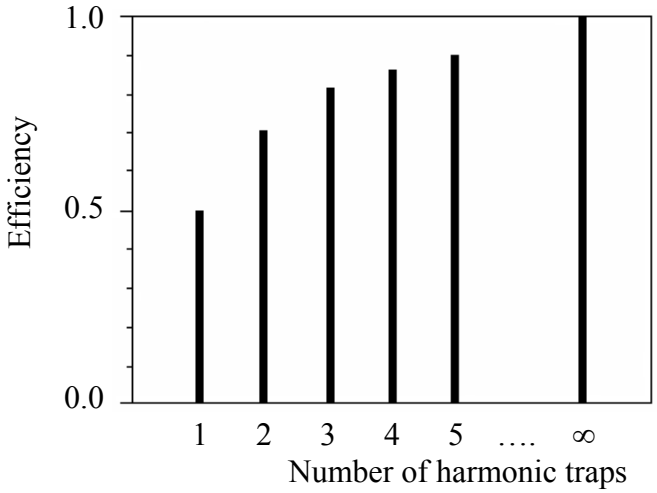


Figure 3.75.

Efficiency improvement in an ideal power amplifier as the number of harmonic traps is increased [49].

Figure 3.76 shows the schematic layout of the class F amplifier, where L_1 and L_2 are the choke inductance and C_1 and C_2 are the dc-blocking capacitors. L_1 and L_2 are seen as DC short circuits and RF open circuits, while C_1 and C_2 has the opposite behaviour. A RF NMOS transistor was used with a length of 0.35 µm and a width of 150 µm.

The filters for the odd harmonics were implemented with bandreject filters connected in series with the output of the amplifier. The impedance of an inductor in parallel with a capacitor can be calculated with

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \textbf{(3.131)}$$

were the total impedance is very high at the frequency, f and otherwise almost zero. The filters for the even harmonics were implemented with bandpass filters connected in parallel to ground. The impedance of an inductor in series with a capacitor can also be calculated with equation (3.131), but then the impedance is almost zero at the frequency, f and very high at the other frequencies.

A class F amplifier with up to the sixth harmonic was implemented for this thesis. The efficiency gained by adding more harmonics was not found worth the output-network complexity needed for higher harmonics. The third and fifth harmonics were filtered out with the circuits in Figure 3.77 (a) connected in series with the output, while the second, fourth and sixth harmonics were filtered out with the circuits in Figure 3.77 (b) connected in shunt.

The inductors of the filters at the first and second harmonics were chosen to by 1 nH to minimize the size on the IC, while the inductors of the filters at the third, forth and fifth harmonics were chosen to be 0.5 nH. The values of the capacitors were calculated from equation (3.131) and are tabulated in table 3.10.

Harmonic, n	*Frequency*	*Capacitor*	*Inductor*
2	4.28 GHZ	1.38 pF	1 nH
3	6.42 GHZ	0.615 pF	1 nH
4	8.56 GHz	0.691 pF	0.5 nH
5	10.70 GHZ	0.442 pF	0.5 nH
6	12.84 GHz	0.307 pF	0.5 nH

Table 3.10.

Values calculated for the capacitors and inductors of the LC filters for the different harmonic frequencies.

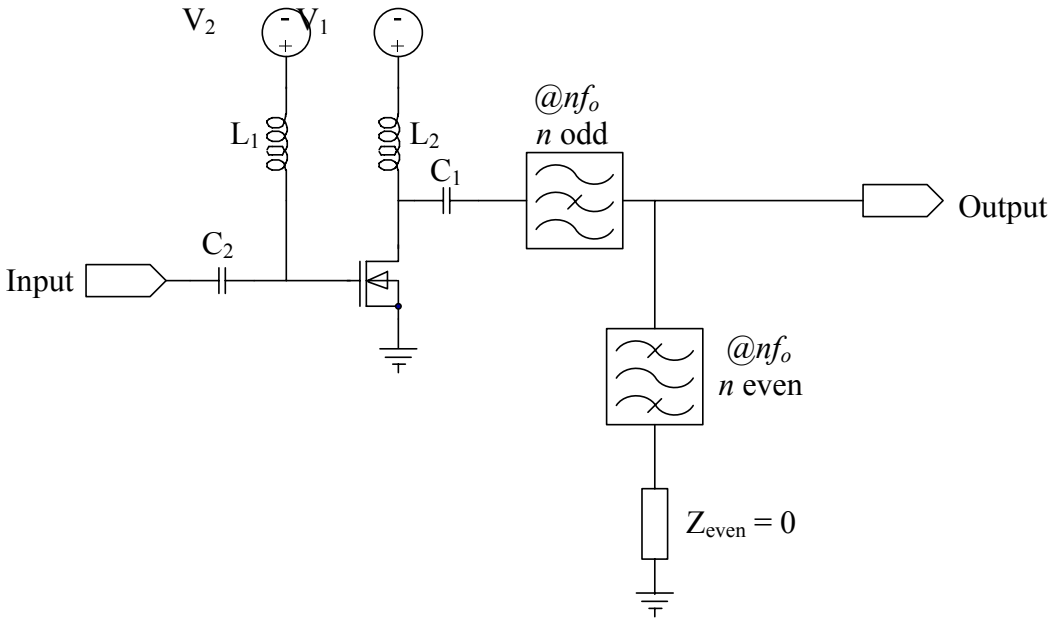
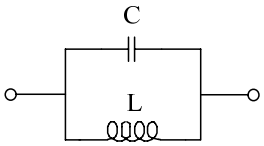
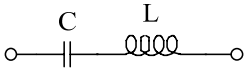


Figure 3.76.

Basic schematic of the class F amplifier.



(a)



(b)

Figure 3.77.

(a) Bandreject filter, and (b) Bandpass filter (bottom) used in the class F amplifier.

The next step towards designing the class F amplifier was to select a suitable bias point for operation. A class F amplifier can be biased as a class A, AB, B and C amplifier. Class A, AB, B and C amplifiers differ merely by their respective conduction angles.

Thus a device can be made to operate under any of these modes by adjusting the gate bias. In order to determine the bias point a DC bias point simulation was performed. Figure 3.78 shows the plot of the DC transfer characteristics for the transistor. For this thesis, the maximum drain-source voltage applicable is 3.3 V.

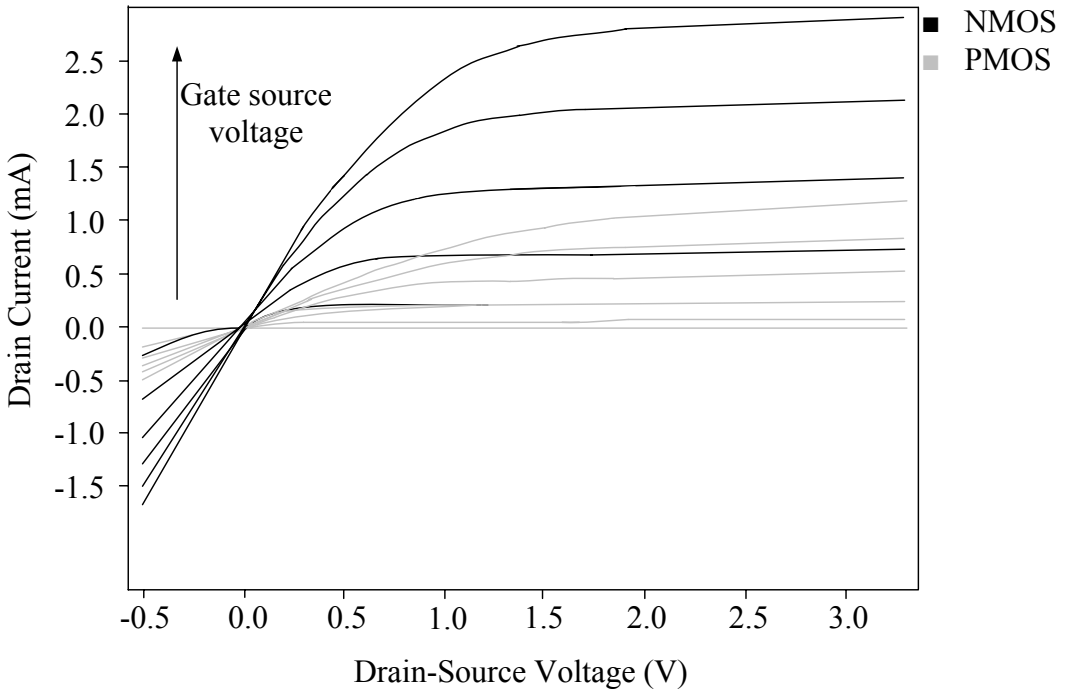


Figure 3.78.

Plot of the DC transfer characteristics for the transistor [28] as the gate source voltage is linearly increased.

Usually the Class F transistor is biased in Class B mode as it gives a better efficiency than biased as Class A or Class B due to the generation of large harmonics. However that would result in a poor linearity [50]. Hence a Class AB bias point was chosen for this thesis.

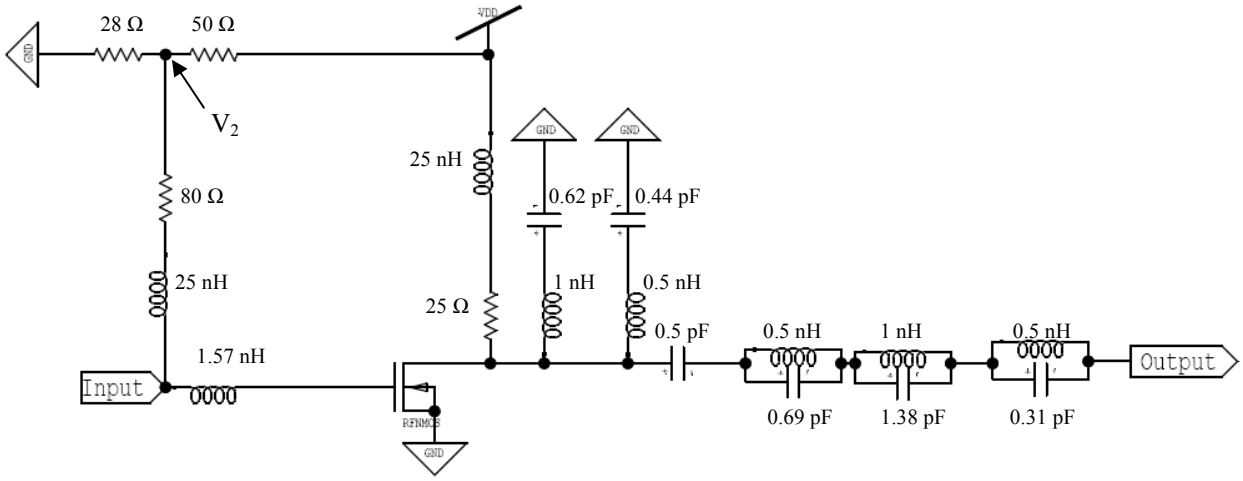


Figure 3.79.

Designed Class F amplifier [V_2 = 1.5 V & V_{DD} = 3.3 V]. Inductor design as in [62].

Difference amplifier

Figure 3.11 (a) shows the schematic of the differential amplifier. This will give the maximum gain, because the difference between v_{IN+} and v_{IN-} will be maximised. A highpass filter produces a frequency dependent leading phase shift of 90˚ at the filters corner frequency. To get a phase shift of 180˚, two highpass filters are placed in series with each other. Figure 3.80 shows the schematic of the highpass filter used for the 90˚ phase shift.

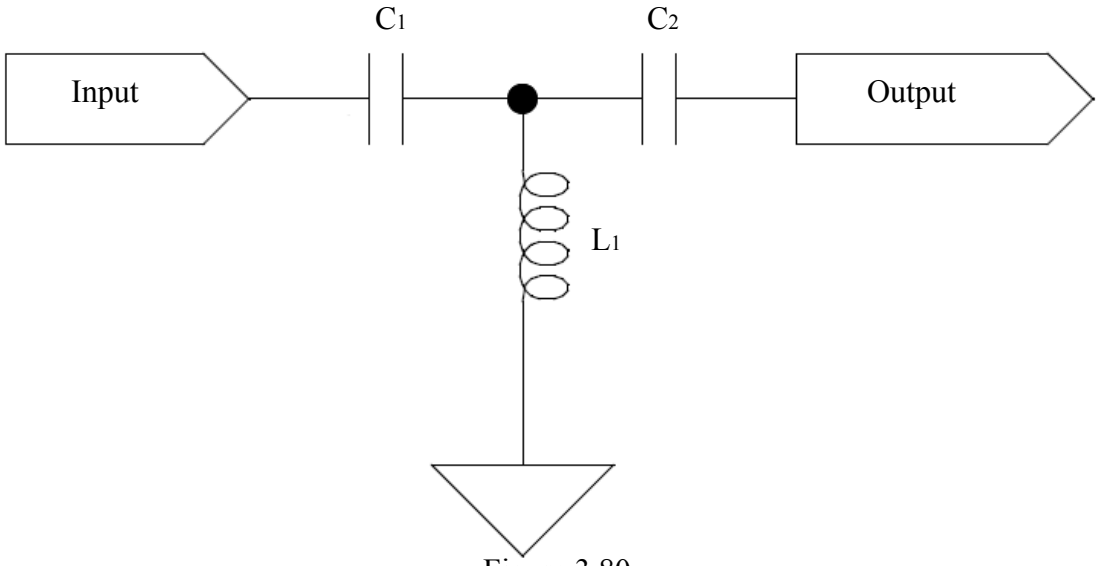


Figure 3.80.

Highpass filter used to create a 90˚ phase shift.

If R_S is the source resistance and R_L the load resistance that connects the two differential outputs to each other, then the characteristic impedance of each filter should be equal to the geometric mean of those source and termination resistances. If $C_1 = C_2$:

$$\sqrt{\frac{L_1}{C_1}} = \sqrt{R_S R_L} \Rightarrow \frac{L_1}{C_1} = R_S R_L \qquad \textbf{(3.132)}$$

The other equation needed to complete the design derives from choosing the corner frequencies of the filters equal to the centre frequency of operation:

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \qquad \textbf{(3.133)}$$

Substituting equation (3.132) into equation (3.133) and solving:

$$C_1 = \frac{1}{\omega_0 \sqrt{R_S R_L}} \qquad \textbf{(3.134)}$$

and

$$L_1 = \frac{\sqrt{R_S R_L}}{\omega_0} \qquad \textbf{(3.135)}$$

R_L is derived from the S-parameters of the 0.35 µm CMOS transistor [28]. The S-parameters are explained in detail in the section detailing the design of the input matching network. From the S-parameters R_L = 38.46 Ω, while R_S equals the 50 Ω resistance. Substituting R_S and R_L into equation (3.134) and (3.135), C_1 = 1.7 pF and L_1 = 3.26 nH. For the 180˚ phase shift, two highpass filters were added in series. A simple current mirror of 4 mA was designed for this differential amplifier [47]. The negative DC voltage is designed as per the next section.

Negative DC voltage

The negative supply was generated with an oscillator, a rectifier, a filter and a voltage regulator.

Design of the ring oscillator

Ring oscillators derive from digital-like building blocks. Compared to tuned oscillators, they have inferior phase noise performance, but their relatively large tuning range and simplicity are strong enough attributes to make them attractive [52]. The ring oscillator

consist of *n* inverters in a ring, where *n* is odd. Figure 3.81 shows the schematic of a CMOS inverter.

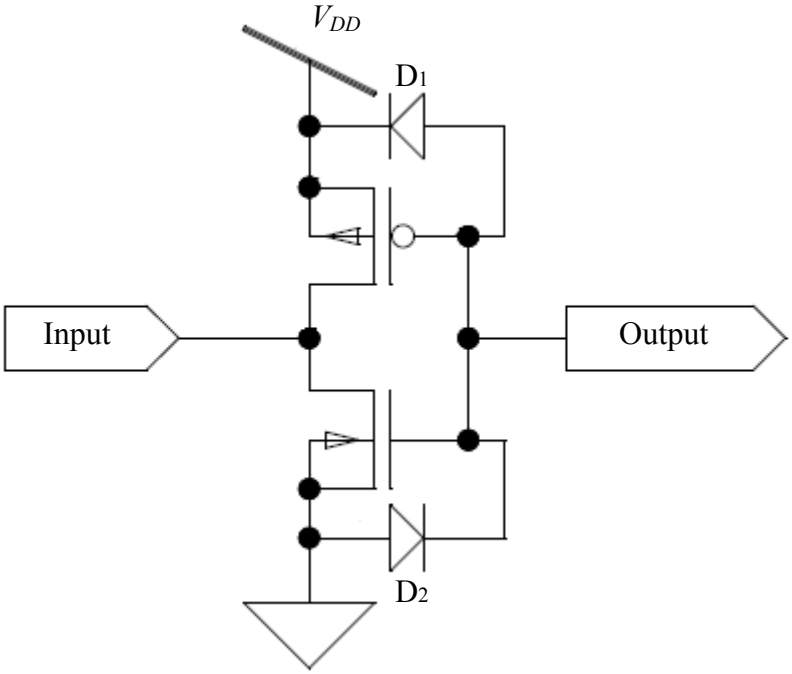


Figure 3.81.

Schematic of a typical inverter.

The inverter can be regarded as an inverting-type threshold detector. D_1 and D_2 are protective diodes. They protect the transistor against possible electrostatic discharge. The inverter inverts an input of 0 V to V_{DD} and an input of V_{DD} down to 0 V. The diodes were replaced with NMOS transistors with length of 0.35 µm and width of 50 µm, where the base of the transistor is connected to its drain and the gate is grounded (Fig. 3.94).

Figure 3.82 shows the schematic of the ring oscillator. I_1, I_2 and I_3 are the inverters shown in Figure 3.81. The ring oscillator consists of an odd number of inverters added in a ring. In its simplest analysis it is assumed that each inverter can be characterized by a propagation delay T_{pd}. No stable DC point exists, and a logic level propagates around the loop, experiencing one net inversion each traversal [52].

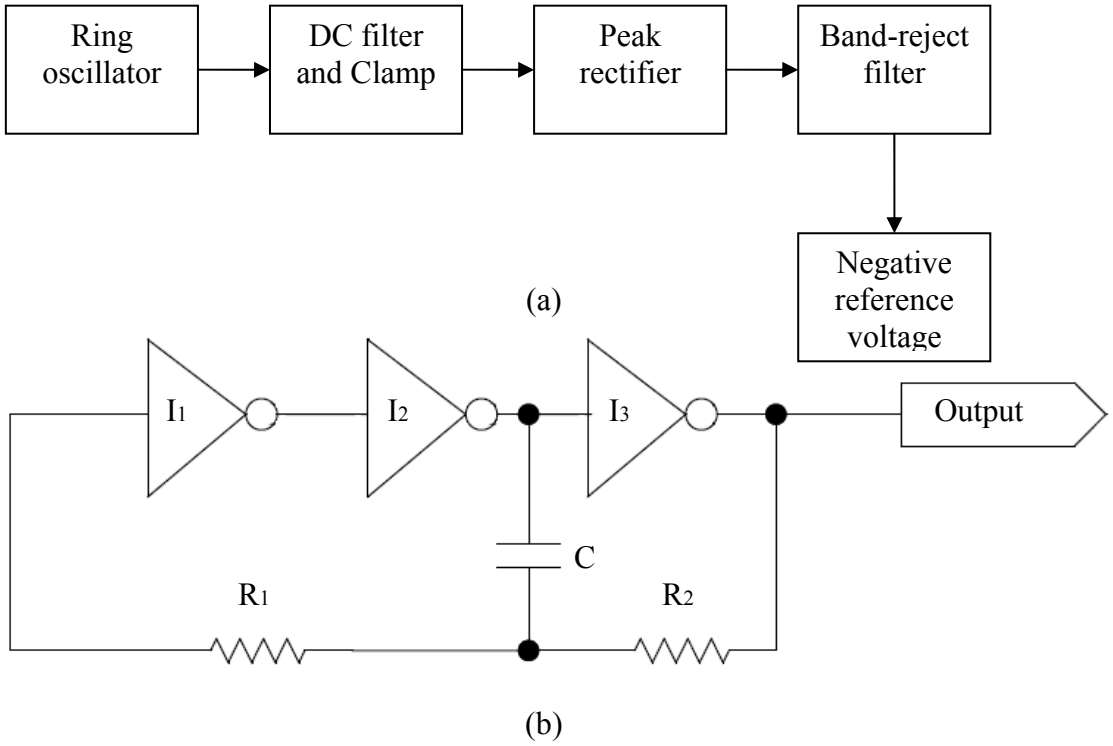


Figure 3.82.

(a) Context of the ring oscillator in generating the negative reference voltage.

(b) Schematic of the ring oscillator.

The oscillation period is therefore simply

$$f_{osc} = \frac{1}{2nT_{pd}} \tag{3.136}$$

where n is the number of inverters and f_{osc} the frequency of the oscillator. To control the oscillator, the propagation delay needs to be adjusted. The best way to adjust the propagation delay is by changing the load [45]

$$nf_{osc} = \frac{1}{R_2 C \ln\left(\frac{V_{DD}+V_T}{V_T} \times \frac{2V_{DD}-V_T}{V_{DD}-V_T}\right)} \tag{3.137}$$

where V_{DD} is the positive DC supply voltage and V_T the threshold voltage of the transistor. It is observed that if the loop was applied directly into I_1, the input protection diodes of the inverter would clamp the voltage of the loop and alter the timing significantly. This is avoided by using a decoupling resistor $R_1 >> R_2$. R_1 is chosen to be 100 Ω and R_2 is chosen as 10 Ω. The oscillator was chosen to oscillate at 1.4 GHz (large enough), as that will give a good negative voltage after the regulator. That will also keep the capacitor value

reasonably low. By substituting the values into equation (3.137), C can be calculated to give $C = 1$ pF.

Design of the rectifier circuit

Figure 3.83 shows the schematic of the rectifier circuit. The circuit is composed of two sections in cascade. That is a clamp formed by C_1, D_1 and R, and a peak rectifier formed by D_2 and C_2. C_1 of the clamp circuit also acts as the DC-blocking capacitor. A clamped circuit results when the output is taken across the diode, rather than across the capacitor. Due to the polarity in which the diode is connected, the capacitor will charge to a voltage V_P equal to the most positive peak of the input signal. A load resistance R is connected across the diode. That forces a net DC current through resistor, R. Since at this time the diode is off, this current comes from the capacitor, thus causing the capacitor to discharge and the output voltage to fall. The output voltage falls exponentially with the time constant RC.

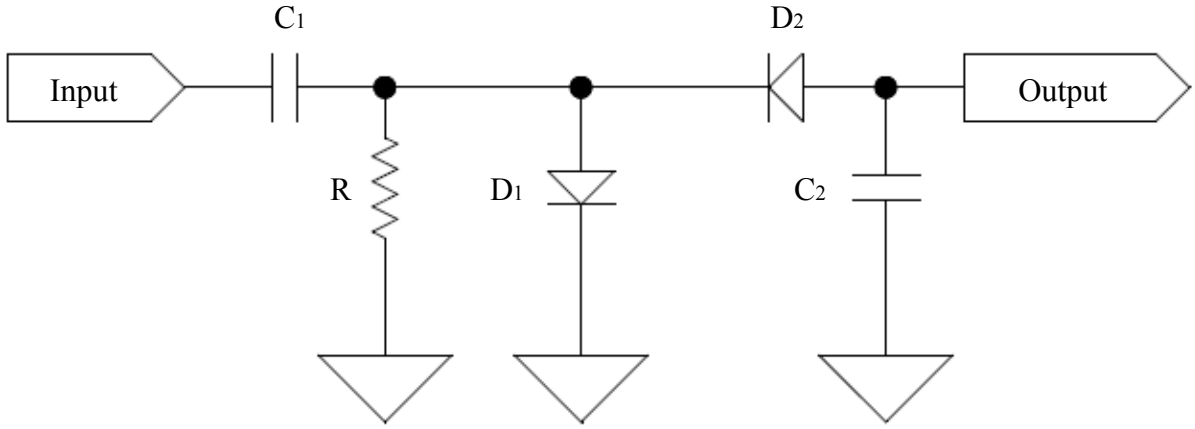


Figure 3.83.
Schematic of a rectifier. The diodes were implemented as shown in Fig. 3.91.

Note that the input voltage, excited by a sinusoid of amplitude $V_P \approx 300$ mV is clamped downwards, giving a positive peak of 0 V, while the negative peak reaches $-2V_P$.

A reversed diode peak rectifier converts the input sinusoid to a negative unipolar output. A filter is added to reduce the variations in the magnitude of the rectifier output. The filter rectifier can be discussed: let the input voltage v_{in} be a sinusoidal waveform with a peak voltage V_{peak} and assume the diode to be ideal. As v_{in} goes negative, the reverse-biased diode conducts and the capacitor is charged in order for the output voltage, $v_{out} = V_{PEAK}$. This situation continues until v_{in} reaches the negative peak value of V_{PEAK}. As v_{in} increases,

the diode cuts off and the voltage remains constant at $-V_{PEAK}$. Thus the circuit provides a DC voltage output equal to the negative peak of the input sine wave.

C_1 is chosen to be equal to C_2. With minor fine tuning on the circuit, the best results are given with R = 2 kΩ and $C_1 = C_2$ = 1 pF. Figure 3.84 shows the output of the negative DC voltage designed. A band-reject filter was added in series with the negative supply to filter out any of the oscillator's signal that leaked through.

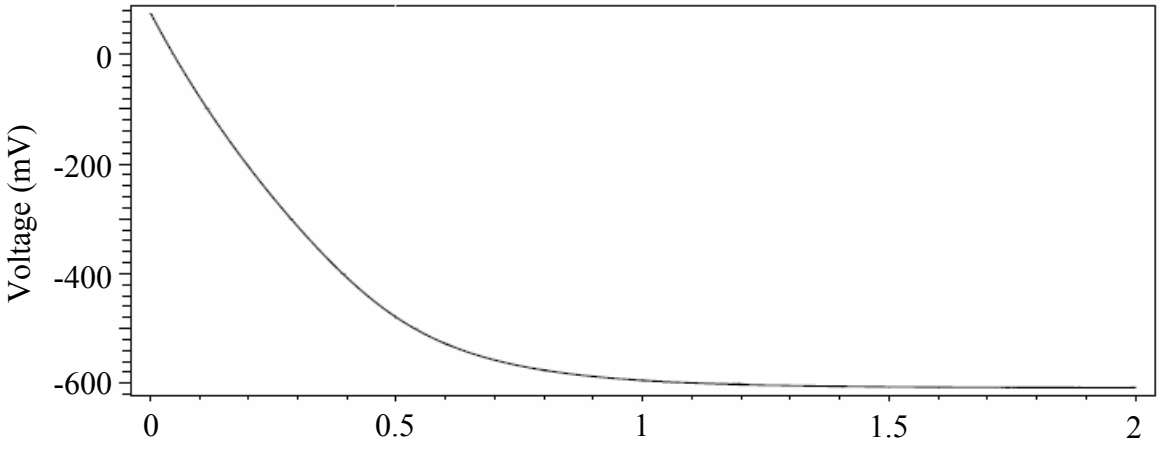


Figure 3.84.

Output from the negative supply.

Design of the input matching network

The input matching network matches the 50 Ω output impedance of the system, to the input impedance of the differential amplifier. Figure 3.85 shows the graph of the S_{11}-parameters at different frequencies for the 150 µm NMOS transistor. Interpolation was used to determine relevant parameters at 2.4 GHz.

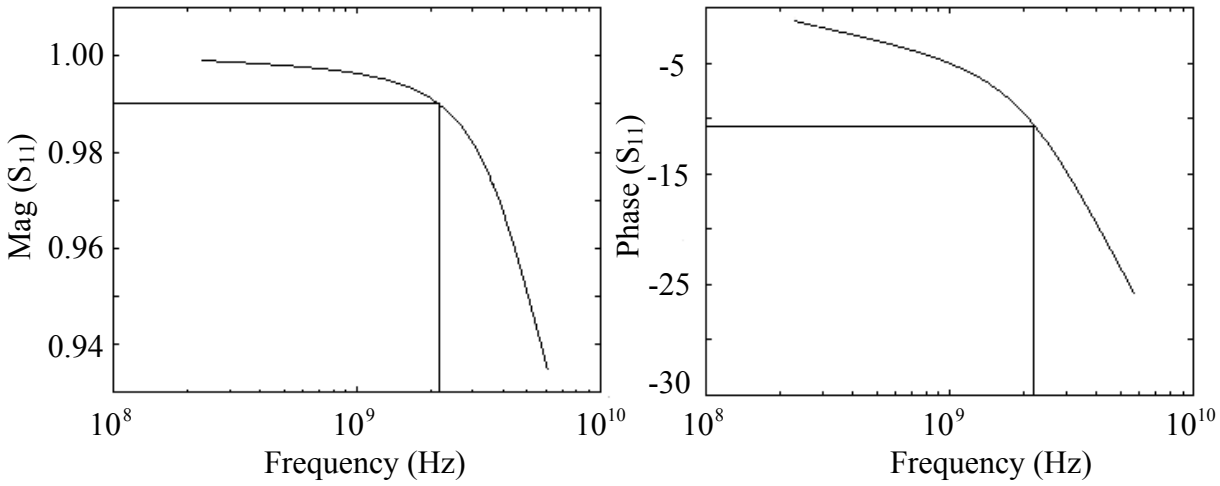


Figure 3.85.

S_{11} parameter for the 150 µm NMOS transistor [28].

Figure 3.86 shows the S_{22} parameters of the same transistor. Interpolation was used to determine relevant parameters at 2.4 GHz.

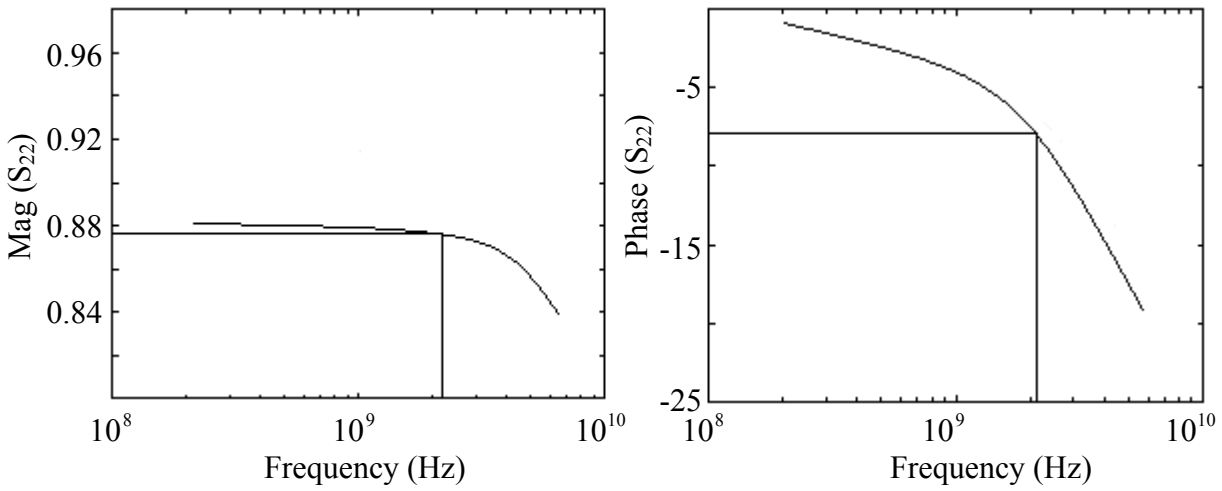


Figure 3.86.

S_{22}-parameter for the 150 µm NMOS transistor [28].

The *S_{21}*- and *S_{12}*-parameters of the NMOS transistor and all the S-parameters of the PMOS transistor were calculated in a similar way to the above. Table 3.11 shows the S-parameters of the NMOS and the PMOS transistors used at 2.4 GHz.

Transistor	**S_{11}**	**S_{22}**	**S_{12}**	**S_{21}**
NMOS (Mag)	0.99	0.875	0.03	1.695
NMOS (Phase)	-11˚	-8˚	81.5˚	167.5˚
PMOS (Mag)	0.6	0.59	0.81	0.76
PMOS (Phase)	-55˚	-53˚	-37˚	-3˚

Table 3.11.

S-parameters for the NMOS and PMOS transistors used at 2.4 GHz.

The differential amplifier (shown as part of Fig. 3.91) used a 150 µm NMOS transistor in parallel with an 18 µm PMOS transistor. For two transistors connected in parallel, the overall Y-parameter can be calculated by adding the individual Y-parameters [53].

The following equations are used to convert the S-parameters to the Y-parameters [53].

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{\Delta_6} \quad \textbf{(3.138)}$$

$$Y_{12} = \frac{-2S_{12}}{\Delta_6} \quad \textbf{(3.139)}$$

$$Y_{21} = \frac{-2S_{21}}{\Delta_6} \quad \textbf{(3.140)}$$

$$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{\Delta_6} \quad \textbf{(3.141)}$$

where

$$\Delta_6 = (1+S_{11})(1+S_{22})-S_{12}S_{21} \quad \textbf{(3.142)}$$

With these equations the Y-parameters of the two transistors were calculated and is tabulated in Table 3.12. Table 3.13 also shows the sum of the two transistor's Y-parameters.

Transistor	**Y_{11}**	**Y_{22}**	**Y_{12}**	**Y_{21}**
NMOS (Mag)	0.08	0.40	0.02	0.912
NMOS (Phase)	87.67˚	40.75˚	-90˚	-4.06˚
PMOS (Mag)	1.10	1.09	1.13	1.06
PMOS (Phase)	37.55˚	36.05˚	-178.06˚	-144.06˚
Total (Mag)	1.15	1.49	1.13	0.69
Total (Phase)	40.71˚	37.32˚	-177.25˚	-85.71˚

Table 3.12.

Y-parameters for the NMOS and PMOS transistors, together with the sum of the two transistors.

	S_{11}	**S_{22}**	**S_{12}**	**S_{21}**
Magnitude	0.26	0.25	0.52	0.32
Phase	-77.06˚	-113.49˚	-33.33˚	58.21˚

Table 3.13.

S-parameters for two transistors in parallel.

It is further given that

$$\Gamma_S = S_{11}^* \tag{3.143}$$

$$\Gamma_L = S_{22}^* \tag{3.144}$$

The input matching network is designed to match the output impedance of the transmitter to the input impedance of the differential amplifier (as shown in Figure 3.91). With the use of the computer program SMITH V1.91[7] and the new S-parameters calculated, the input impedance of the differential amplifier was calculated to be $(5 - j15)$ Ω. For an input matching network it is necessary to match the 50 Ω resistor to the input admittance. The input matching network was designed using the SMITH V1.91. It was necessary to have at least one series capacitor to be used as the DC-blocking capacitor.

The input admittance was calculated to be $(0.02 + j0.06)$ S, which means that the differential amplifier can be simulated with a resistor of 5 Ω and an inductor with an inductance of

$$L = \frac{I_M}{2\pi f} \tag{3.145}$$

where I_M equals the imaginary value of the input admittance and f the frequency of the circuit. The inductor was determined to be 3 pH. A frequency sweep simulation was done

[7] A mathematical modelling tool from the University of Berne.

on the circuit, to include 2.4 GHz. Figure 3.87 shows the schematic of the input matching network.

R_1 and v_s (200 μV_{peak}) serve to model the transmitter. R_2 and L_2 are the input admittances of the transistor as calculated earlier. C_1 and L_1 represents the input matching network. Figure 3.88 shows the result of the frequency domain simulation.

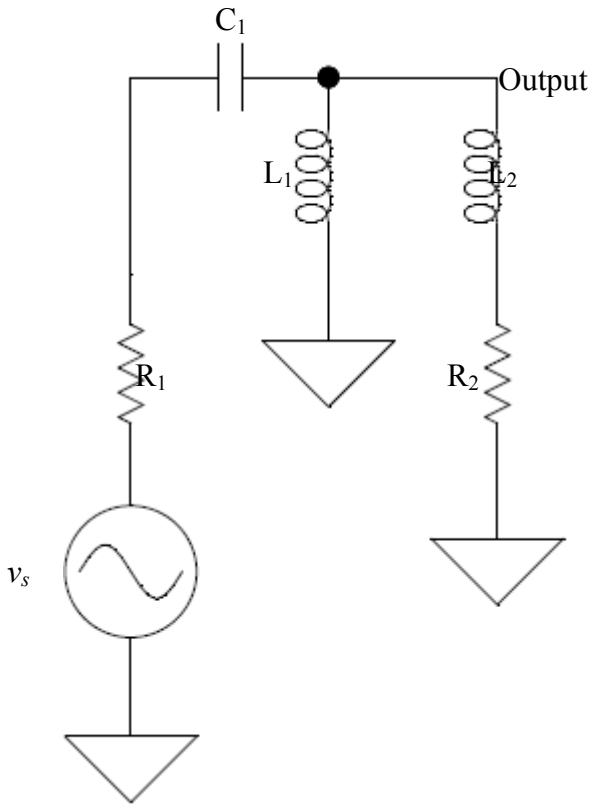


Figure 3.87.

Input matching network.

From Figure 3.88, it is clear to see that the input matching network has a voltage peak at 2.4 GHz.

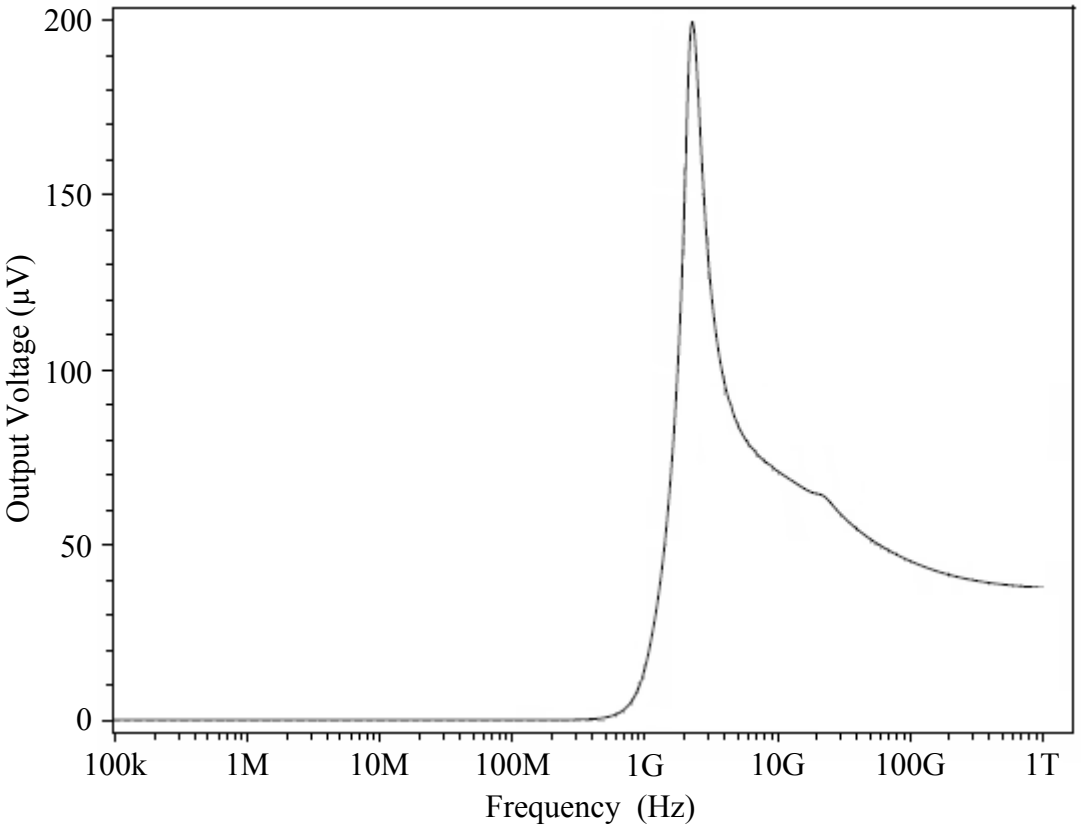


Figure 3.88.

Frequency sweep of the input matching network.

Design of the amplifier matching network

The amplifier matching network matches the output impedance of the differential amplifier to the input impedance of the class F amplifier. It was also implemented using passive elements as it needs to act as a DC-coupling capacitor, an inductor choke as well as the matching network. Figure 3.11 (a) shows that the differential amplifier is horizontally symmetric. This means that the output impedance of the differential amplifier can be calculated with the S-parameters in table 3.13. The amplifier matching network (shown in Figure 3.89) was also done using the SMITH V1.91 and the different S-parameters. It was necessary to have at least one series capacitor to be used as the DC-blocking capacitor and one parallel inductor to be used as an inductor choke. Just like the input matching network, the transistors were simulated using inductors, capacitors and resistor and a frequency sweep was done to confirm functionality. The amplifier matching network was adjusted to give the ideal peak. Figure 3.90 shows the result of the frequency sweep analysis done on the amplifier matching network circuitry. The frequency sweep shows a clear voltage peak at 2.4 GHz.

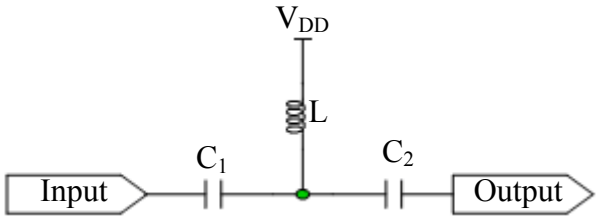


Figure 3.89.

Modified amplifier matching network. The final circuit is shown as part of Fig. 3.91.

Design of the output matching network

The output matching network was used to match the output impedance of the class F amplifier to the 50 Ω antenna. The output matching network included a DC-blocking capacitor and an inductor choke. The output matching network was designed in a similar way as the previous matching networks, using the NMOS S-parameters in table 3.11. Next the transistor was replaced with an equivalent capacitor and resistor pair, and a frequency sweep analysis was done on the circuit. The circuit was fine tuned until it gave the desired voltage peaked at the 2.4 GHz.

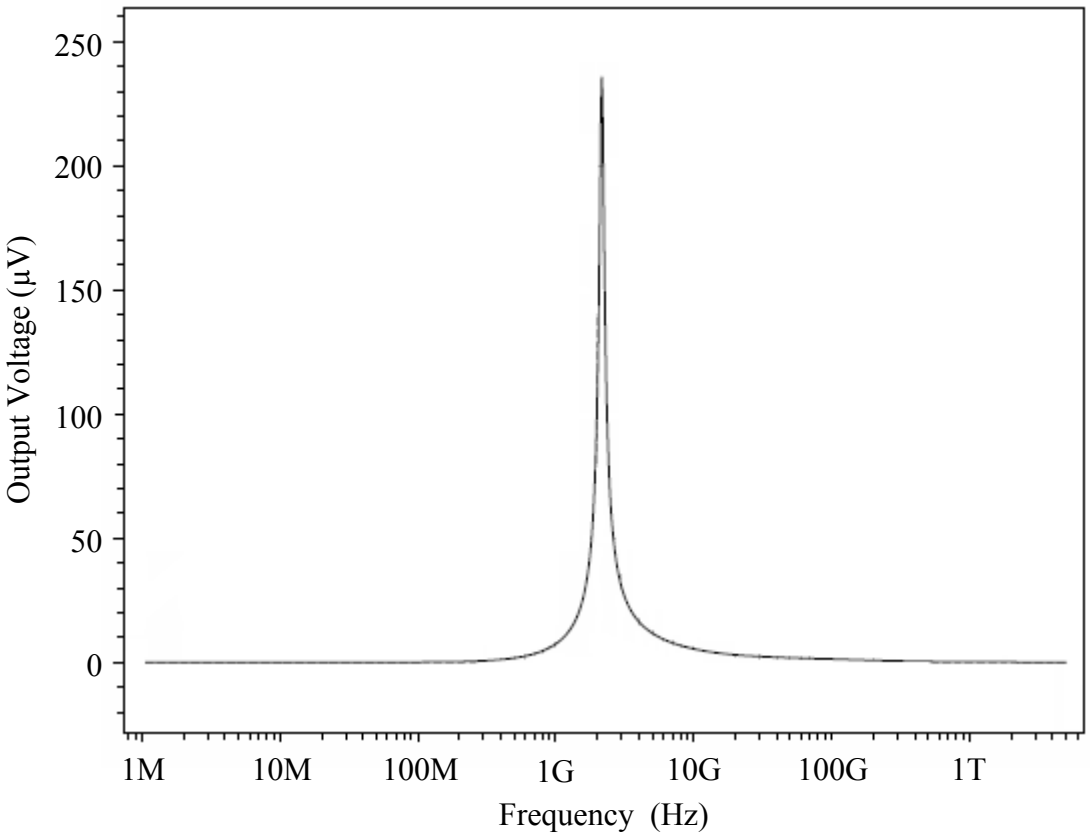


Figure 3.90.

Frequency sweep analysis of the amplifier matching network. An input signal of 250 µV was used for this simulation.

Complete implementation of the power amplifier

The various design blocks of the complete power amplifier were discussed in the previous sub-sections. The various design blocks were integrated, to also include the matching networks. Figure 3.91 shows the complete power amplifier. The values for the different components are tabulated in table 3.14.

The input (centred at about 2.4 GHz), v_s consists of 13 sine waves, each with amplitude of 10 mV spaced 50 MHz from each other. V_1 is the DC supply that controls the variable gain. V_2 and V_3 are used to bias the class F amplifier.

R1	140 Ω	C10	10 pF
R2	500 Ω	C11	12.92 pF
R3	80 Ω	C12	1 pF
R4	2 kΩ	C13	1 nF
R5	100Ω	C14	1 nF
R6	1000 Ω	L1	6.6 nH
R7	200 Ω	L2	7.32 nH
R8	50 Ω	L3	1 nH
R9	0 Ω	L4	25 nH
C1	2.91 pF	L5	1.57 nH
C2	0.44 pF	L6	25 nH
C3	1.43 pF	L7	1 nH
C4	0.50 pF	L8	0.5 nH
C5	0.62 pF	L9	0.5 nH
C6	0.44 pF	L10	1 nH
C7	0.69 pF	L11	0.5 nH
C8	1.38 pF	L12	8.4 nH
C9	0.31 pF		

Table 3.14.

Components used for the total system.

The layout of the power amplifier is shown in Figure 3.92.

Simulation results

Simulation results yielded a gain of (using a 50 Ω load impedance):

$$Gain = 10\log\left(\frac{V_o I_o}{V_i I_i}\right) \tag{3.146}$$

$$Gain = 10\log\left(\frac{(333.07mV)(194.36\mu A)}{(10mV)(8.61\mu A)}\right) \approx 28\,\text{dB} \tag{3.147}$$

The power added efficiency (PAE) was calculated with [48]

$$PAE = \frac{P_o}{P_{S1} + P_{S2} + P_i} \tag{3.148}$$

where P_o is the output power, P_{S1} is the power delivered by the source V2, is the power delivered by the source V3 and P_i is the input power. Parameters provided in table 3.15.

P_o	64.46 µW
P_i	1.90 µW
P_{S1}	5.01 µW
P_{S2}	72.94 µW

Table 3.15.

Calculated power at different stages of the amplifier.

The PAE was computed to be about 81 % (for five harmonic traps). Table 3.16 shows the variation in PAE for less harmonic traps.

ACPR is the ratio of power in the adjacent channel to the power in the main channel. ACPR values are widely used in the design of power amplifiers to serve as a measure of linearity [31]. As shown in Figure 3.93, the ACPR was computed to be -55 dB.

Total harmonic distortion (THD) is an important amplifier performance figure, a good figure for the THD for this thesis was chosen to be less than 1 % [47].

THD was calculated using:

$$THD = \frac{\sum_{n=2}^{\infty} V_{fn}}{V_{f0}} \tag{3.149}$$

where V_{fn} is the RMS voltage at the harmonics frequencies and V_{fo} is the RMS voltage at the fundamental frequency. Figure 3.94 shows the RMS value of the output voltage.

THD was computed to be about 0.6 %.

The *Q*-factor is an important measure for a power amplifier. Figure 3.95 shows a frequency sweep at the output to determine the Q-factor:

$$Q = \frac{f_O}{BW} \tag{3.150}$$

The *Q*-factor was calculated to be about 4. The low Q-value is attributed to the large number of passive on-chip inductors.

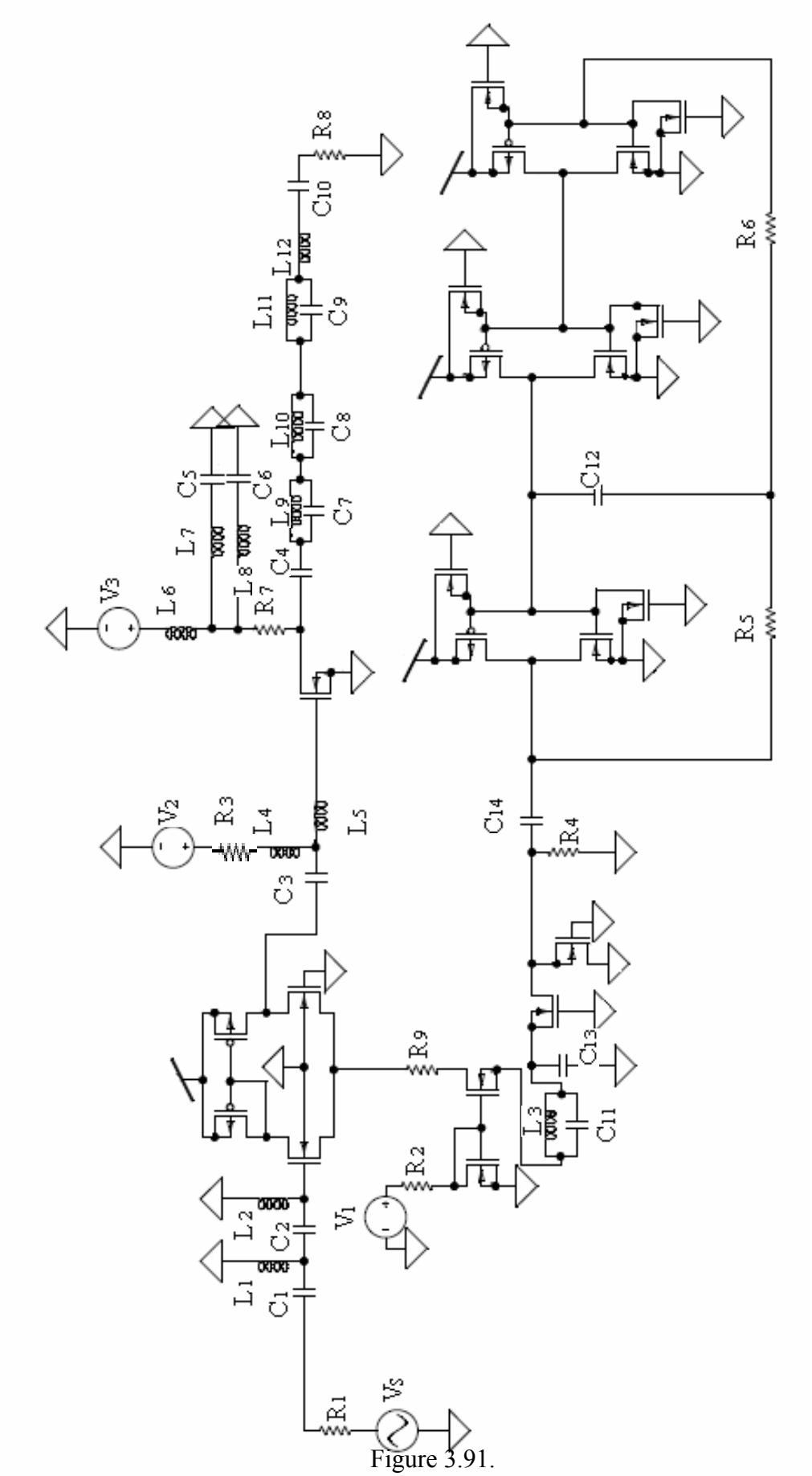


Figure 3.91.

Complete Class F power amplifier [72].

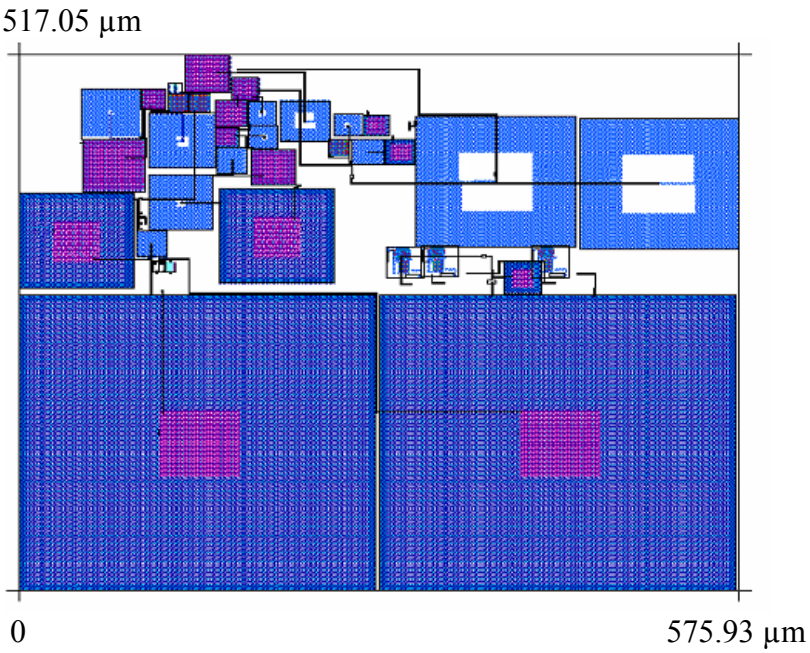


Figure 3.92.

Circuit layout for the power amplifier.

Harmonic traps	PAE
5	80.73%
4	80.27%
3	77.52 %
2	71.06 %
1	67.99 %
0	62.35 %

Table 3.16.

Effect of harmonic traps on PAE.

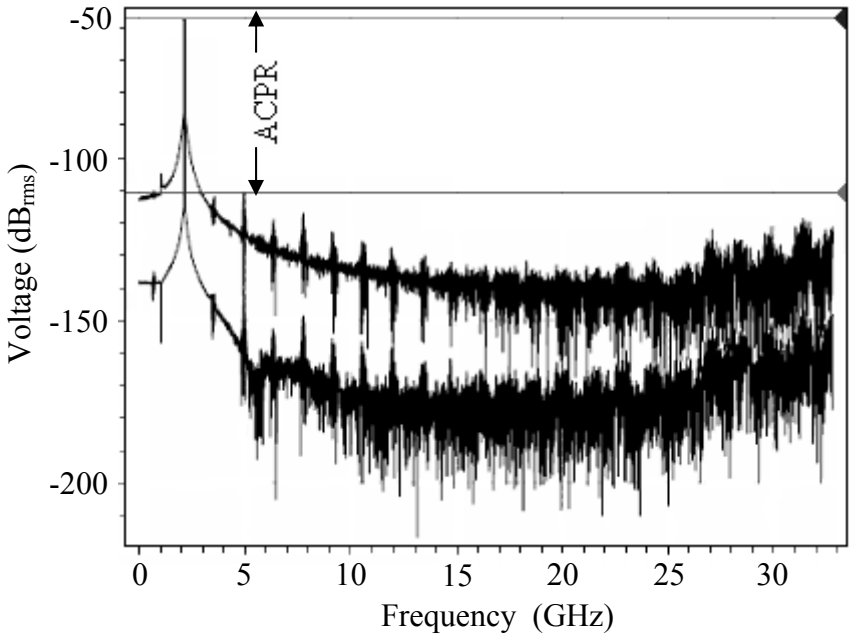


Figure 3.93.

FFT of the output voltage (top) and the input voltage (bottom).

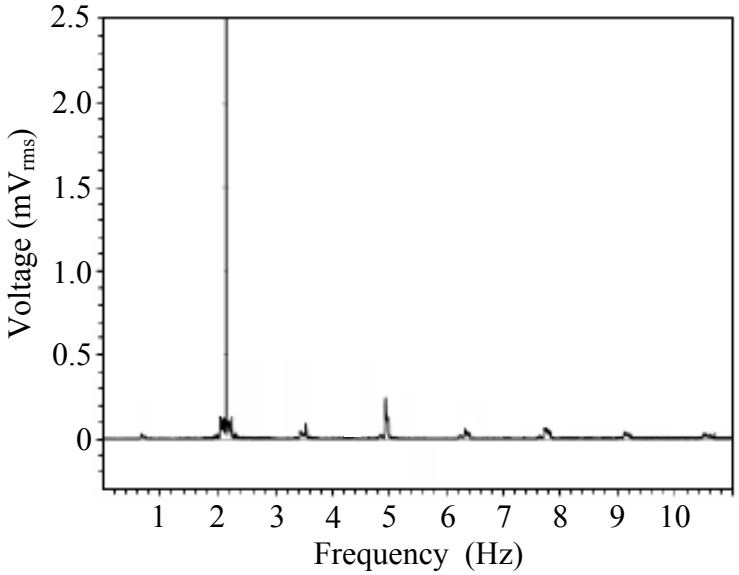


Figure 3.94.

RMS value of the output voltage.

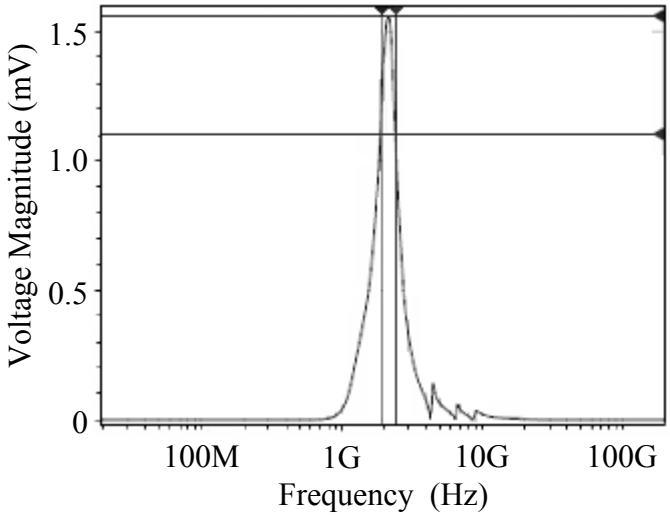


Figure 3.95.

Frequency sweep of the complete power amplifier. This figure aims to show the frequency range only – and used to determine the *Q* factor.

CHAPTER 4: DIGITAL AND MIXED SUB-SYSTEMS DESIGN

This chapter details the basic elements utilised for digital and mixed-circuit design. Since these circuits are quite common, the analysis done here is from an overview perspective only. Most textbooks on CMOS digital design cover these circuits in detail [54-55]. Furthermore, not all digital cells were designed by first principles, as AMS also provides such cells, as part of a digital library. With the exception of the digital buffer (last sub-section of this chapter), the sub-sections below represent cases where the AMS digital cells were not directly used.

4.1 Digital sub-systems

4.1.1 Bidirectional transmission gate

The switches in this thesis have been implemented as bidirectional transmission gates as shown in Figure 4.1 [55].

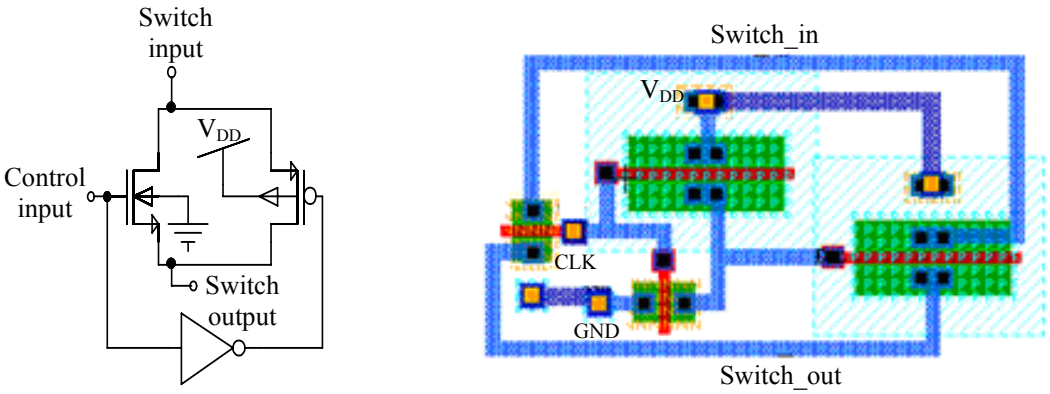


Figure 4.1.

Circuit schematic (left) for the bidirectional gate and (right) the layout of the circuit.

The advantage of using bidirectional gates instead of implementing the NMOS or PMOS as a stand alone switch is that the on resistance of the device is drastically reduced. This is given by

$$R_{on,eq} = R_{on,n} \parallel R_{on,p} \tag{4.1}$$

which is solved to yield,

$$R_{on,eq}^{-1} = \left[\mu_n C_{ox} \left(\frac{W}{L} \right)_n (V_{DD} - V_{THN}) - \left[\mu_n C_{ox} \left(\frac{W}{L} \right)_n - \mu_p C_{ox} \left(\frac{W}{L} \right)_p \right] V_{in} - \mu_p C_{ox} \left(\frac{W}{L} \right)_p |V_{THP}| \right] \tag{4.2}$$

If $\mu_n C_{ox} (W/L)_n$ is set equal to $\mu_p C_{ox} (W/L)_p$ and this factor is represented as β then equation (4.2) simplifies to

$$R_{on,eq}^{-1} = \beta \left[(V_{DD} - V_{THN}) - |V_{THP}| \right] \tag{4.3}$$

indicating that the on resistance of the switch is independent of the input voltage level. A simulation to verify the operation of this switch was generated in which the switch operated as a "chopper" on the input signal. It was found that the switch operated very well until about 500 MHz when its performance began to decline. This simulation is shown in Figure 4.2.

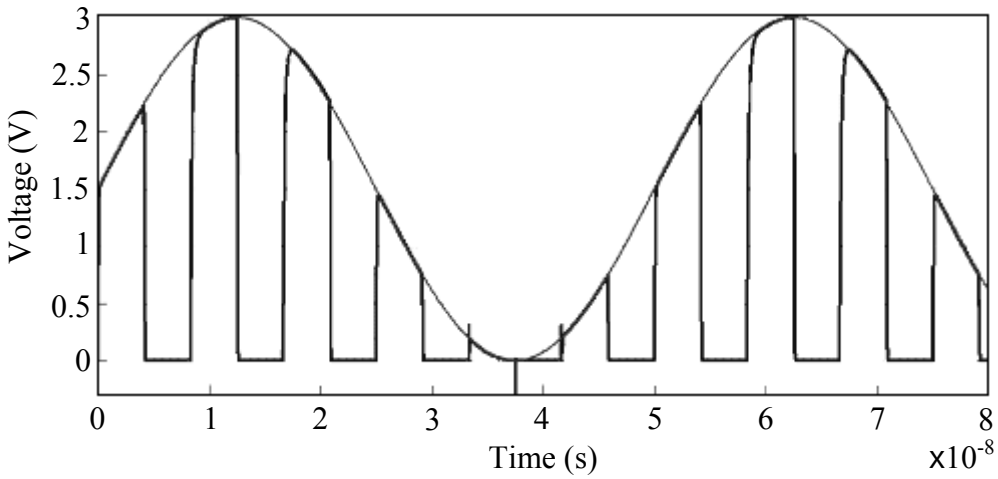


Figure 4.2.

Simulation of the switch implemented in a chopper configuration with a sinusoidal input and the chopped output shown in bold.

4.1.2 Logic gate - inverter

The CMOS logic inverter utilised uses two MOSFETs, one NMOS device and one PMOS device. The circuit schematic is shown in Figure 4.3 along with the layout.

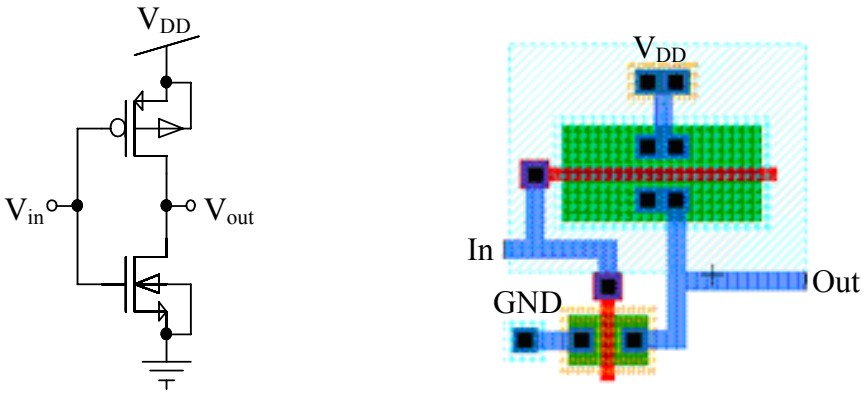


Figure 4.3.

Circuit schematic (left) and layout (right) for the CMOS logic inverter.

The circuit operates (in the extreme cases) as follows, when the input is high, the NMOS turns on and the PMOS turns off, thus pulling the output to ground. When the input is low, the NMOS turns off and the PMOS turns on pulling the input to V_{DD}.

To give the inverter symmetric transfer characteristics the widths must be set to

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \tag{4.4}$$

which was already done for the basic NMOS and PMOS transistors used for design in this thesis (see chapter 3). Using this fact, the maximum permissible input for the output to go high is given by V_{IL} can be calculated using ($V_{THP} \approx$ -0.5 V)

$$V_{IL} = \frac{3V_{DD} + 2V_{THP}}{8} \tag{4.5}$$

and the minimum permissible input for the output to go low, given by V_{IH} which can be calculated using

$$V_{IH} = \frac{5V_{DD} + 2V_{THN}}{8} \tag{4.6}$$

The transfer characteristic for the inverter is shown in Figure 4.4.

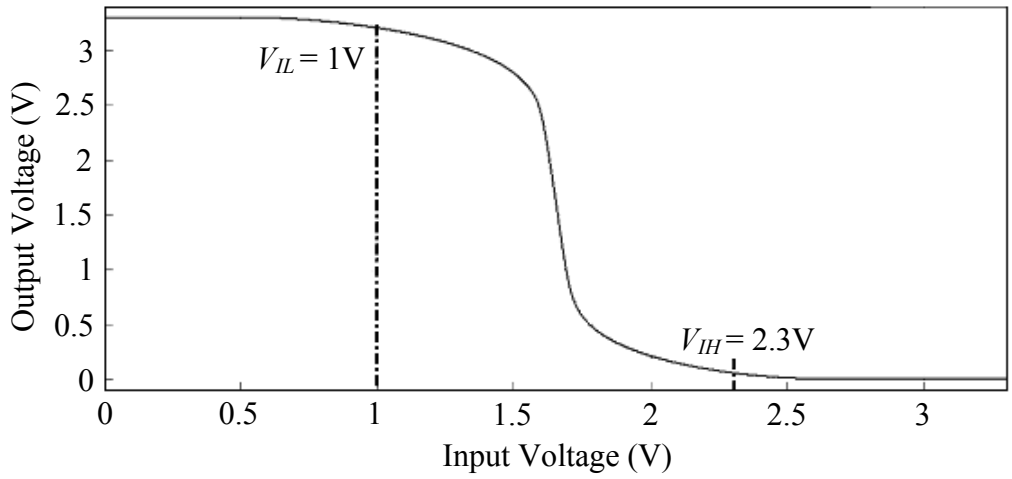


Figure 4.4.

Transfer characteristic for the logic inverter.

4.1.3 Logic gate – NAND

In the digital implementation of this circuit, 2-input NAND, 3-input NAND and 2-input AND gates were required. The switching point of the device can be determined using the fact that the two NMOS transistors in parallel are equivalent to one NMOS with $W_{n,eq} = 2W_n$ and the two PMOS devices in series are equivalent to one PMOS device with $L_{p,eq} = 2L_p$. Using these equivalences, the transconductance ratio of the two devices in the NAND gate be written as $\beta_n/4\beta_p$. Then the switching point of the NAND gate can be shown to be [55]

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{4\beta_p}} \cdot V_{THN} + \left(V_{DD} - |V_{THP}|\right)}{1 + \sqrt{\frac{\beta_n}{4\beta_p}}} \tag{4.7}$$

4.1.4 Logic gate – NOR

The NOR gate implemented for this thesis was a 2-input NOR gate, the schematic of which is shown in Figure 4.5, along with its layout. In a similar method of analysis to that of the NAND gate the transconductance ratio of a 2-input NOR logic gate can be calculated as $\sqrt{4\beta_n/\beta_p}$ and thus the switching point equation is given by

$$V_{SP} = \frac{\sqrt{\frac{4\beta_n}{\beta_p}} \cdot V_{THN} + \left(V_{DD} - |V_{THP}|\right)}{1 + \sqrt{\frac{4\beta_n}{\beta_p}}} \tag{4.8}$$

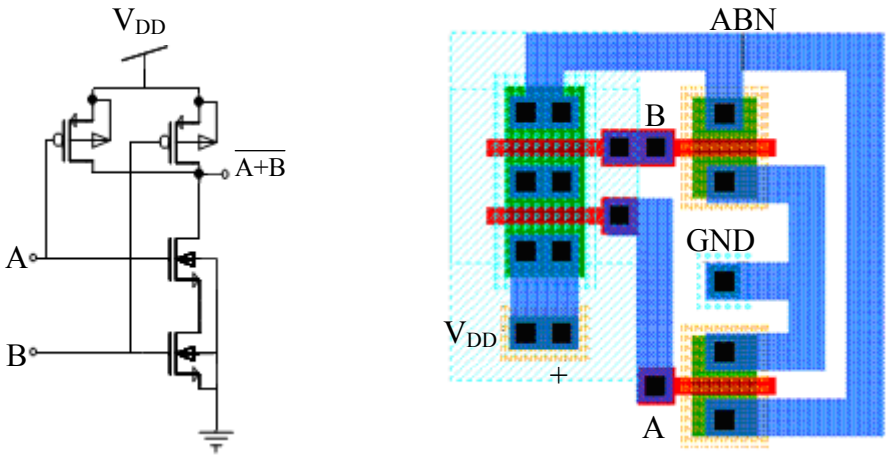


Figure 4.5.

Circuit schematic (left) and layout (right) of the logic NOR gate. All NMOS and PMOS have an aspect ratio of 5/1.

4.1.5 D-Type flip-flop (FF)

The D-FF implemented in this thesis was designed to trigger on the positive clock edge. The logic circuit for the D-FF [54] explains the functional operation of the D-FF, however to implement it using the logic gates proposed leads to many redundant circuit elements and inefficient operation of the device. A simpler implementation was used in this thesis which employs just switches and inverters to achieve the same functionality. The implemented circuit is shown in Figure 4.6 where all the switches implemented represent the transmission gate of the earlier section.

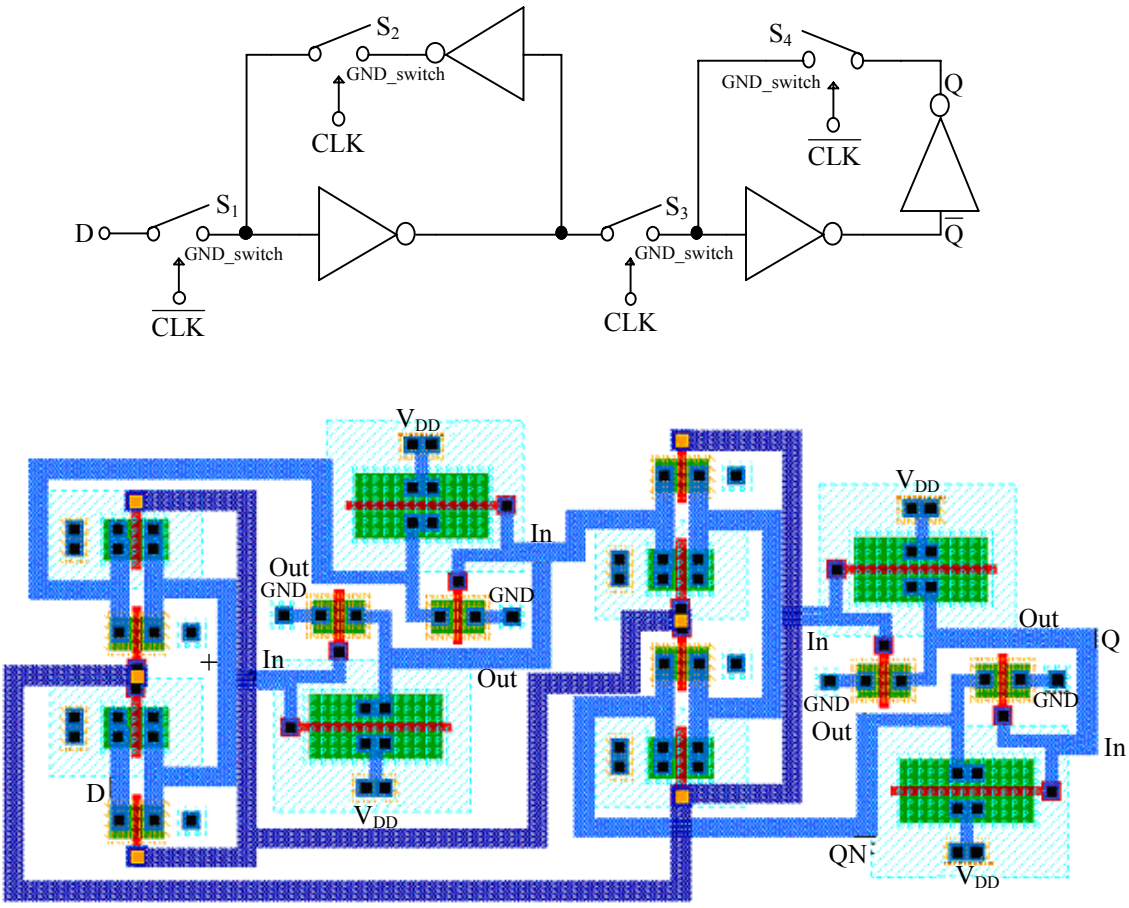


Figure 4.6.

Circuit schematic (above) of the edge triggered D-FF and (below) the layout of the circuit.

When the clock signal is low, switches S1 and S4 are on, allowing the "D" input to flow through the inverter. When the clock signal changes, S1 and S4 turn off while S2 and S3 turn on, and the inverse value of the "D" input from the previous state is passed through switch S3 and inverted again to give output "Q", which also flows through an inverter to yield its inverse. When the clock returns to low, the value of Q and its inverse circulates in the now closed loop, holding their values constant until the clock goes high again.

Implementing the circuit as described above not only increases the speed and efficiency of the D-FF, but also uses far less die area than its logic gate counterpart.

4.1.6 Counter

A synchronous 4-bit binary counter was implemented in this thesis. The choice of this counter was based on the design of a parallel-to-serial converter (section 4.1.7) which

implements two such counters [54]. The circuit schematic of the counter implemented is shown in Figure 4.7.

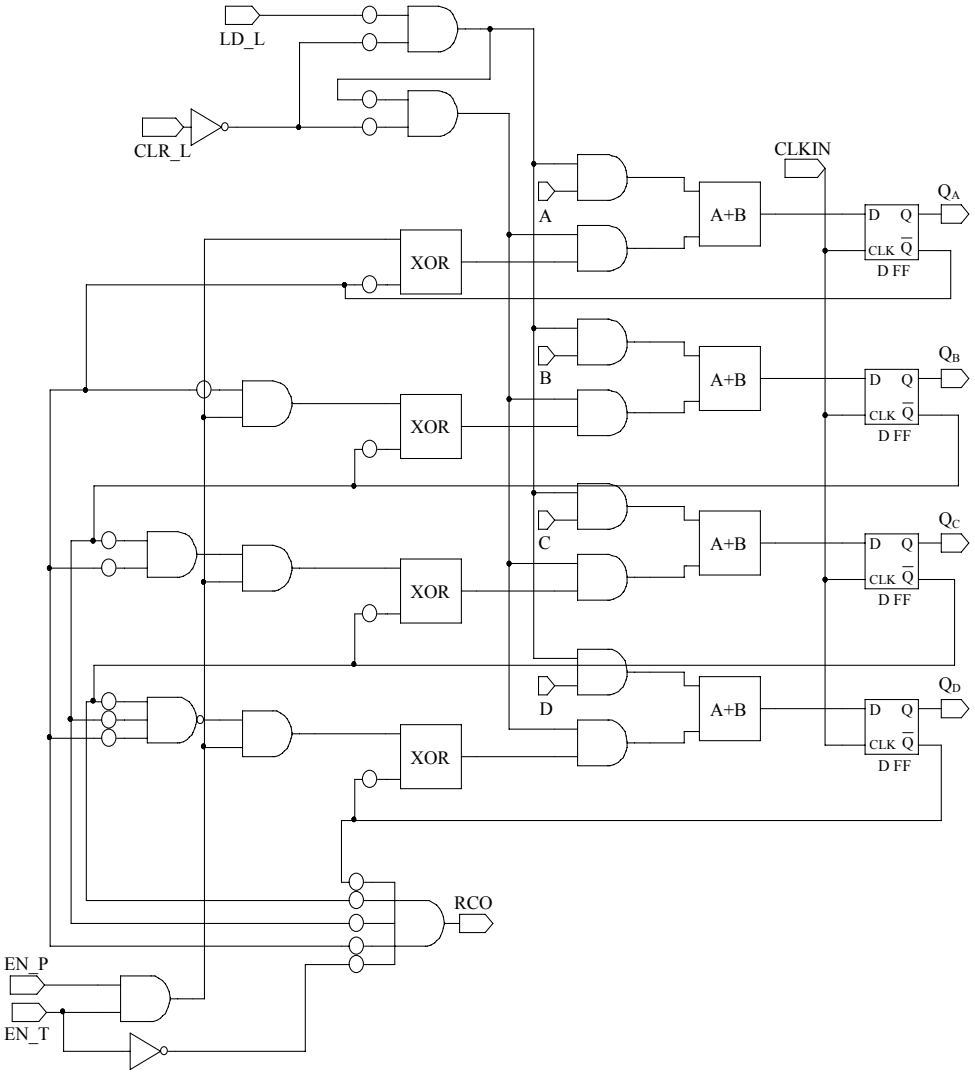


Figure 4.7.

Counter logic diagram [54].

Each input to the D-FFs shown is driven by a 2-input multiplexer (the two AND gates whose output provides the input to the OR gate). The multiplexer is controlled by the active-low clear signal and its output is cleared if the clear signal goes low. If the active-low "load" input goes low then the top AND gate in the multiplexer passes the four input signals through to the output. If both the "load" and the "clear" inputs are high (not activated) then the bottom AND gate of each multiplexer passes the output of the XNOR gate to the counter output. The actual counting performed by the device is done by the XNOR gates. The "ripple carry over" output signal indicates carry and is at logic 1 when all the output count bits are logic 1.

4.1.7 Parallel-to-serial (P/S) converter

The P/S converter combines data from many parallel streams into one serial stream [54]. It is used at the back-end of the receiver running in unbalanced mode. The circuit schematic for this register is shown in Figure 4.8. The operation is far simpler than that of the counter. The multiplexer at the input to the D-FF operates in basically the same manner as the counter, when the load signal goes low, the parallel input signals are loaded to the D-FF. When the load signal is low the clock shifts the loaded values, essentially creating the serial output.

Figure 4.10 shows simulation results (from the layout – shown in Figure 4.9) to indicate the position of each bit in the serial data stream. As can be seen from the figure, the output signal B7_L indicates the start of a new 8-bit serial word. Each bit was tested individually to show its position in the serial word, this is shown in the figure, with reference to the clock signal.

4.1.8 Serial-to-parallel (S/P) converter

S/P converter distributes data into different data lines. The number of data lines determines the reduction in data speed. It is used at the front end of the transmitter which runs in an unbalanced mode. To ensure the success of conversion, a digital clock is used. For this thesis, a 4-bit S/P conversion was deployed using one 2-bit counter, one 4-bit serial-in parallel-out shift register and one 4-bit register [54].

4.1.9 Clock recovery

Clock recovery is the only synchronisation scheme used in the system. It is used on the front-end of the transmitter to recover the clock from the data stream so that it can be used for the S/P conversion. The clock recovery circuit is shown in Figure 4.12. It is based on two sub-systems [56]:

- edge detection, where edges are detected whenever the data makes 0-to-1 or 1-to-0 transition, and
- a counter, that runs in the free mode by means of an external clock, and resets whenever an edge is detected in the data stream. The counter is driven by an external clock that is required to run approximately eight times faster than the recovered clock.

The circuit was simulated for a data bit period of 1 µs as shown in Figure 4.13.

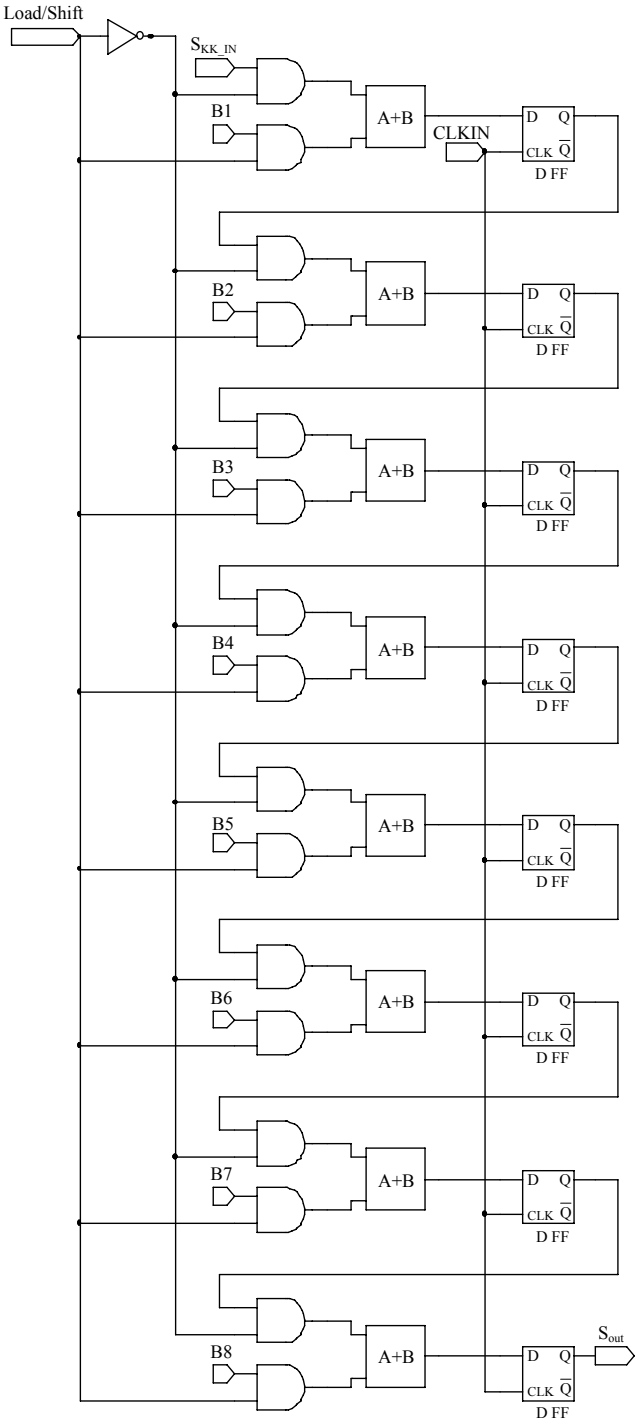


Figure 4.8.

P/S converter [54].

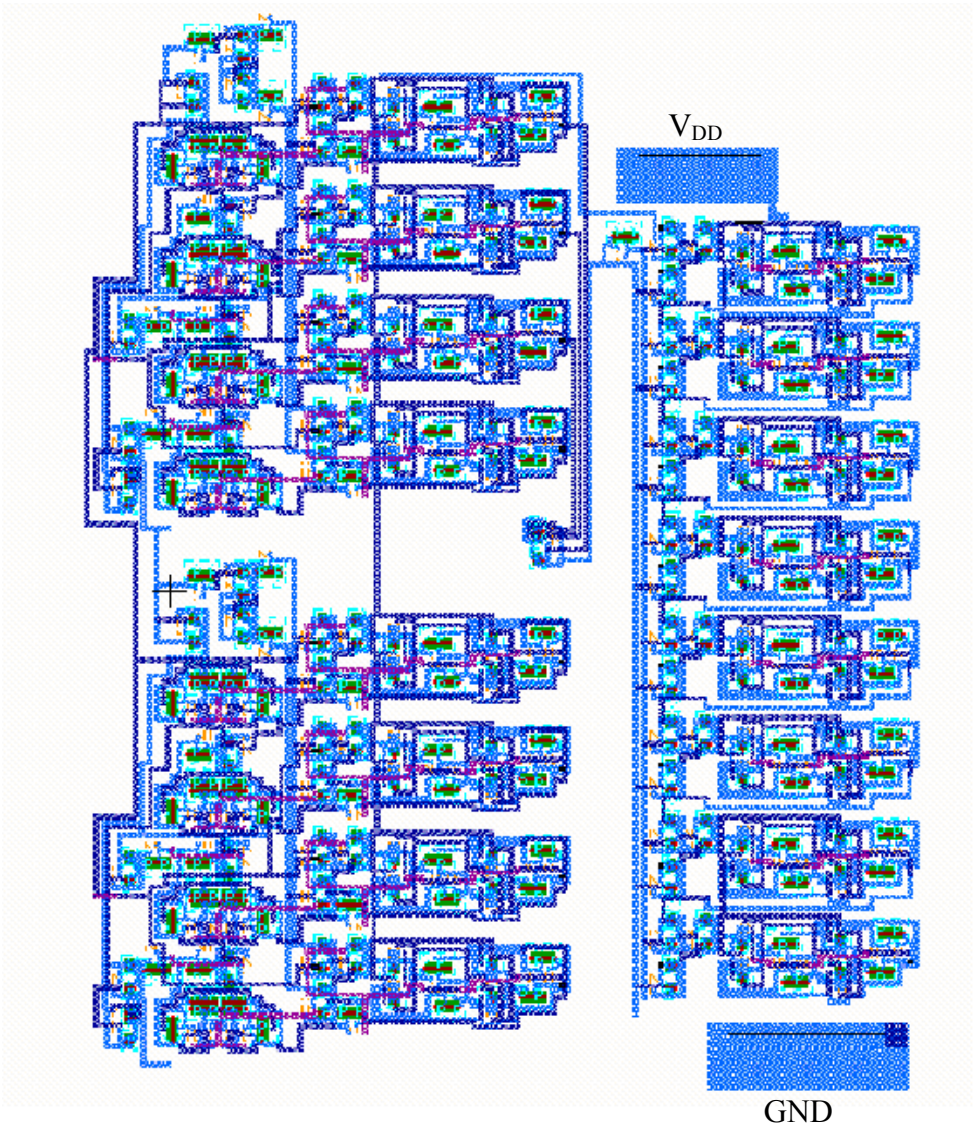


Figure 4.9.

Layout of the P/S Converter.

4.1.10 Error correction

This block is a piece of digital circuitry used to correct errors in the receiver if it is running in the balanced mode. If a bit in one of the four branches is received in error, the circuit will ignore it based on the data in other three branches. If two bits in two branches are received in error, the circuit will assume that 0 is received. If more than two branches are in error, the error will not be detected. The truth table for such a circuit is shown in table 4.1.

The function of the circuit can be derived to be

$$O = X.Y.Z + W.Y.Z + W.X.Z + W.X.Y \tag{4.9}$$

$$O = \mathbf{(}\{[(X.Y.Z)'.(W.Y.Z)']' + [(W.X.Z)'.(W.X.Y)']'\}'\mathbf{)}' \tag{4.10}$$

The implemented circuit is shown in Figure 4.14.

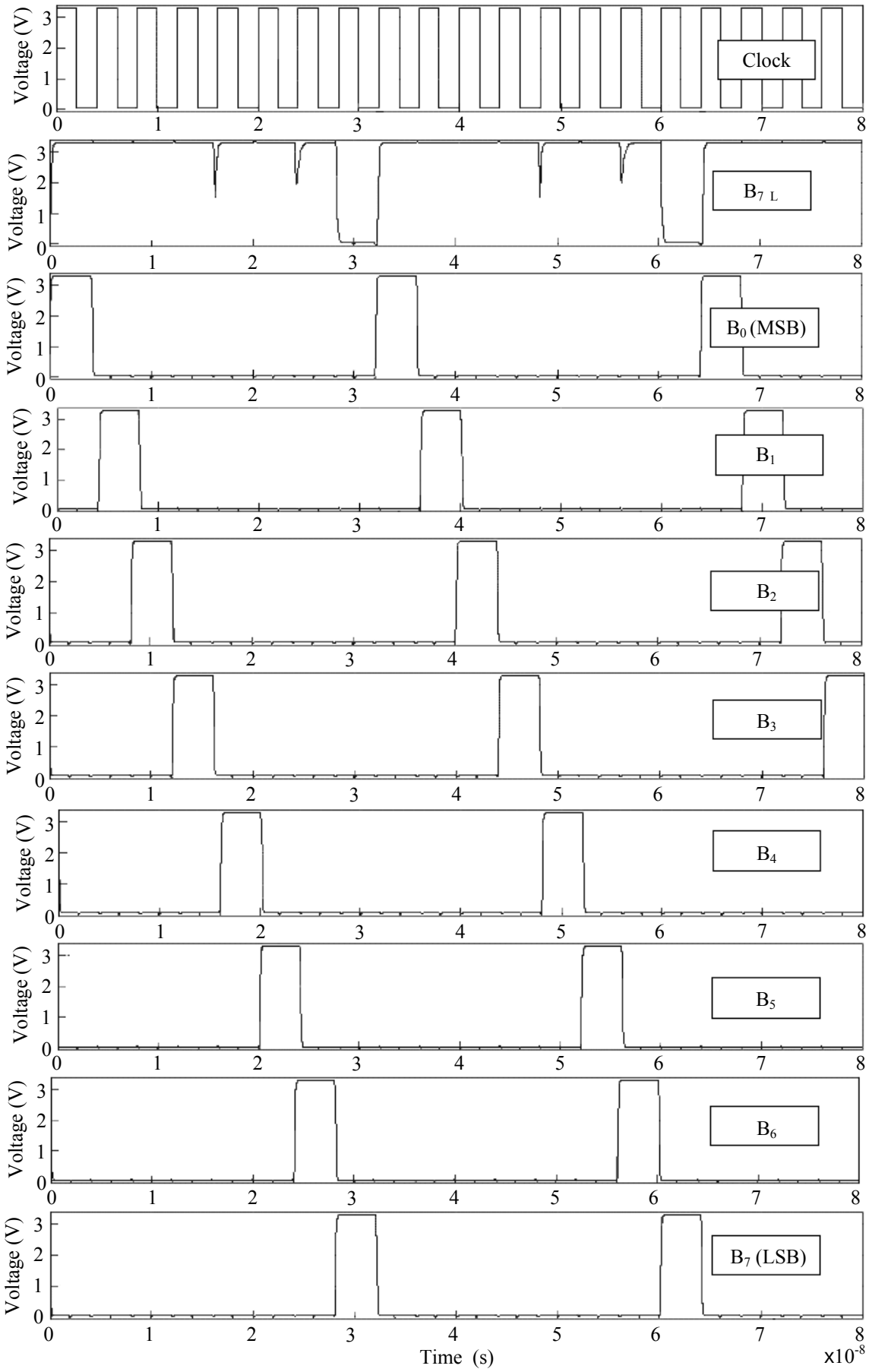


Figure 4.10.

Serial output for each of the bits that were tested for the P/S converter.

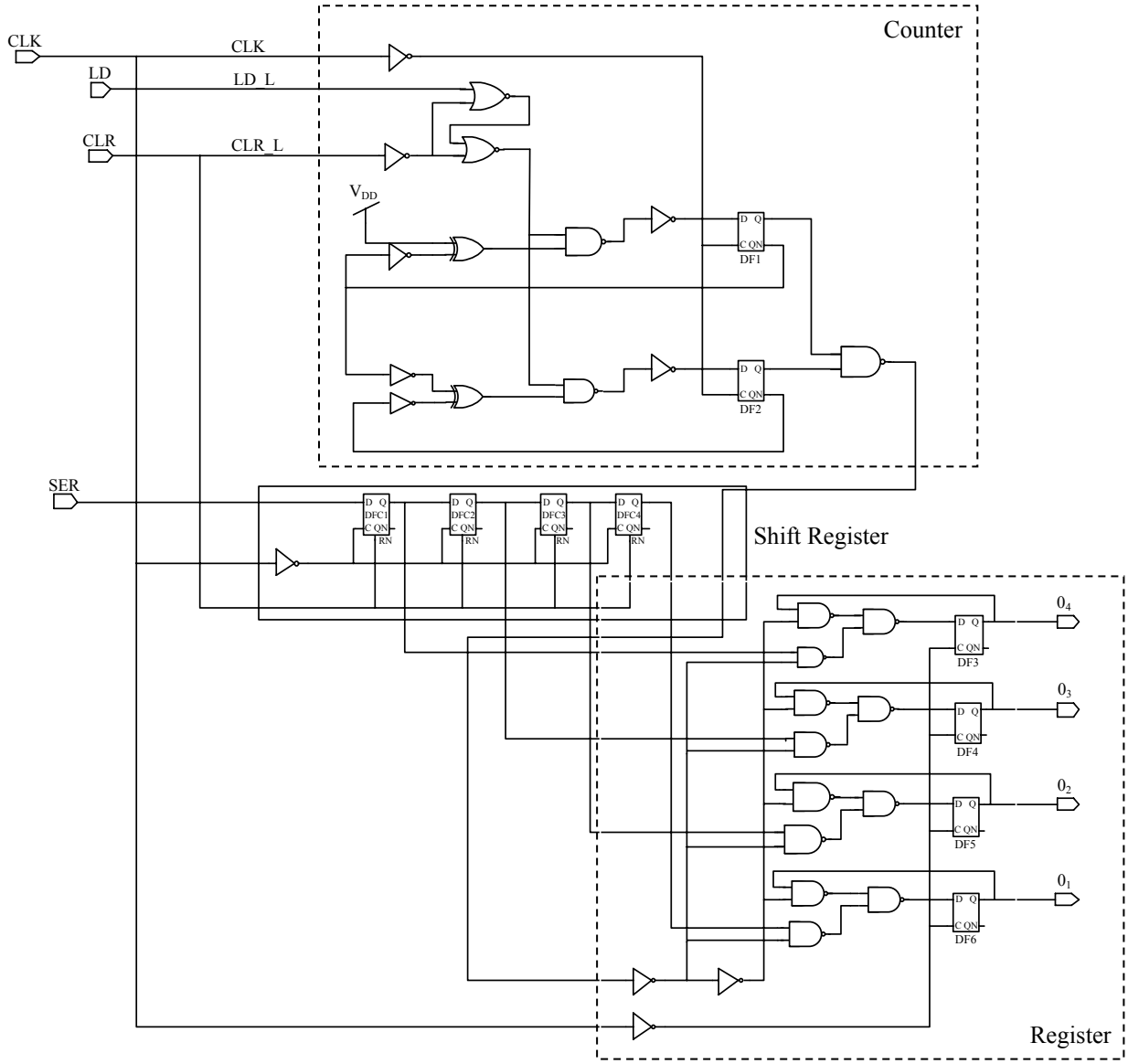


Figure 4.11.

S/P converter [54].

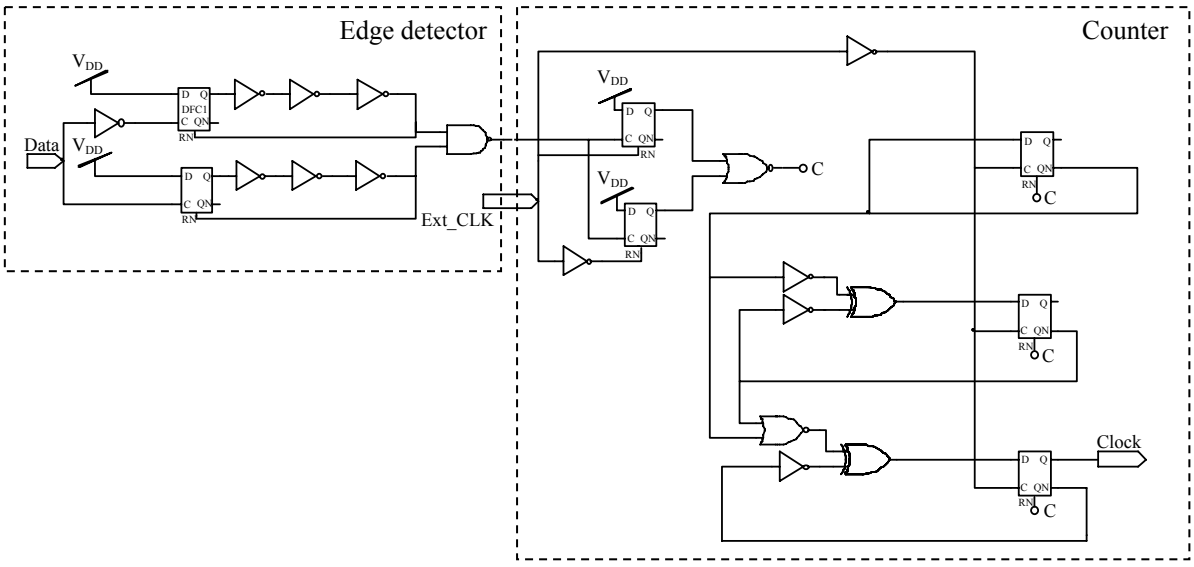


Figure 4.12.

Clock recovery circuit.

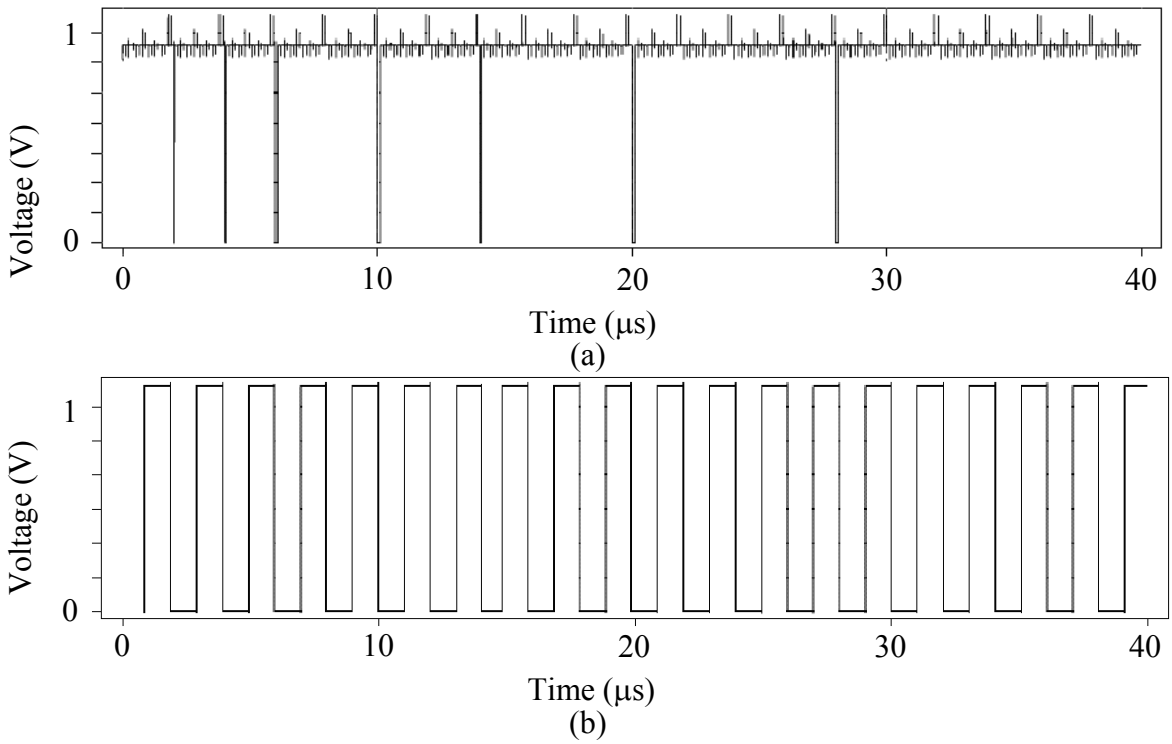


Figure 4.13.

Clock recovery circuit operation (a) shows detected edges, and (b) shows the recovered clock.

Branch 1 (W)	Branch 2 (X)	Branch 3 (Y)	Branch 4 (Z)	Common stream (O)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 4.1.

Truth table for the error correcting circuit.

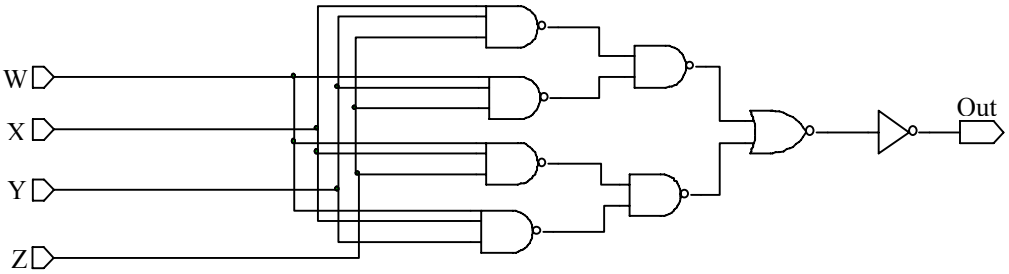


Figure 4.14.

Error correction circuit.

4.2 Mixed circuit sub-systems

4.2.1 Sequence mixer

The sequence mixer is not actually a mixer [71], but a decision circuitry that selects either a positive or a negative version of the real or imaginary part of the CSS. It is based on an analogue CMOS switch. Since the outputs of this block are differential and can be modulated later in the process, a mixing function is established. Depending on whether the data bit is 0 or 1, the CMOS switch is either ON or OFF. The switches work in pairs, so that if one is OFF, the other one is ON. In this way, either an inverted or non-inverted version of the sequence is passed through. The smallest length and width of the transistor of 0.35 µm and 0.7 µm respectively has been chosen for this thesis. The schematic of the sequence mixer is shown in Figure 4.15.

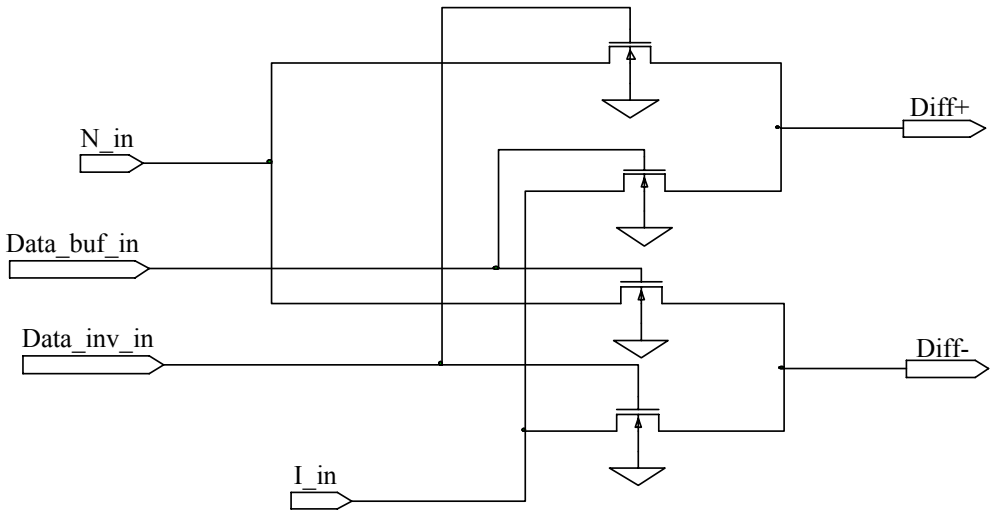


Figure 4.15.

Sequence mixer circuit.

4.2.2 Digital buffer

Buffering is needed when a signal does not exactly have the voltage level of 0 V for bit 0 and 3.3 V for bit 1. Analogue voltages close to these, when passed through a buffer, give exact digital voltages. The non-inverting buffer is a standard CMOS block available in the Tanner digital library. Its symbol is shown in Figure 4.16.

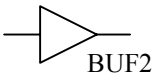


Figure 4.16.

Symbol of the buffer, as part of the AMS digital library.