CHAPTER 1: INTRODUCTION

1.1 Background to the research

Communication system engineers are often concerned with efficiency with which systems utilize signal energy and bandwidth. In most communication systems these are essential issues. However, in some cases, there exist situations in which it is necessary for the system to resist external interference, to operate at low spectral energy, to provide multiple access capability without external control, and to provide a secure channel inaccessible to outside listeners [1]. Thus, it is sometimes necessary to trade-off efficiency of a system for such enhanced features. Communication systems deploy spread spectrum techniques to achieve such features [2].

The theoretical aspects of using spread spectrum in a strong interference environment have been known for over four decades. It is only over the last decade that practical implementations became more feasible. Initially, spread spectrum techniques were developed for military purposes [3] and their implementations were exceedingly expensive. Technological advancements such as VLSI, and advanced signal processing techniques made it possible to develop cheaper spread spectrum equipment for general public use [4]. Applications of this technology include mobile phones, wireless data transmission and satellite communications [5].

Spread-spectrum systems adhere to two criteria [2]:
1. the bandwidth of the transmitted signal must be greater than the transmitted signal, and
2. transmitted bandwidth must be determined by some function that is independent of the message and is known to the receiver.

Bandwidth expansion in spread spectrum systems is achieved by using a function that is independent of the message. Spread spectrum techniques have other features that make it unique and useful. These features include [4]:

- anti-jam capability-particularly for narrow-band jamming,
- interference rejection,
- multiple-access capability,
- multi-path protection,

- covert operation or low probability of intercept (LPI),
- secure communications,
- improved spectral efficiency-in special circumstances, and
- ranging.

One of the methods of classifying spread spectrum techniques that will be used throughout this thesis is by modulation. Some of the modulation techniques employed in spread spectrum techniques include [3]:

- direct sequence spread spectrum (DSSS),
- frequency hopping spread spectrum (FHSS),
- time hopping,
- chirp, and
- hybrid methods.

Spread spectrum techniques can be used to transmit both analogue and digital data signals using an analogue signal. Essentially, a higher frequency PN sequence is used to spread an information signal over a wider bandwidth, thereby making jamming and interception of the signal more difficult as only small portions of the signal can be blocked out. Various spread spectrum techniques have been developed, as listed above; the two most popular types will be discussed in some more detail: FHSS and DSSS. In FHSS the information signal is transmitted over a series of frequencies seemingly randomly (hopping). The receiver hops between frequencies in synchronisation with the transmitter. This allows the transmitted signal to be recovered. DSSS, as used in this thesis and explained later, is a more recent development. A third, hybrid type of spread spectrum, which combines the advantages of FHSS and DSSS techniques while reducing their shortcomings - for instance, the need for power control in DSSS systems, or the probability that a FHSS system will transmit at a frequency that happens to have high interference - has also been developed. In this technique, each data bit in the message signal is spread individually using a PN sequence while the channel hops between frequencies [6].

Table 1 serves as a comparison between the two main types of spread spectrum.

DSSS	FHSS
Higher performance, data rate, and larger packets.	Lower cost, better for lower data rates, and more burst data.
Broadband continuous transmission.	Narrowband at any instant, discontinuous transmission.
More complex, more efficient PSK modulation.	Simple, less efficient FSK modulation.
Traditionally use linear power amplifiers, making it less power efficient.	Can use nonlinear power amplifiers, thus achieving higher power efficiency.
Quicker synchronization.	Requires guard band, longer sync time.
Requires less efficient linear amplifier.	Requires a more efficient nonlinear amplifier.
Near-far effect[1] is dominant, this can be reduced by employing power control in cellular systems.	Near-far effect has less influence as users are not always in the same frequency slot.
Avoids interference by spreading energy across band.	Avoids interfering source by hopping around it.

Table 1.

Comparison of DSSS techniques with FHSS techniques [6, 7].

The following excerpt [8] is an important basis for this thesis:

> "This invention relates to a multi-dimensional, DSSS communication system and method.
>
> In a DSSS system, the spectrum spreading is accomplished before transmission through the use of a spreading sequence that is independent of the data signal. The same spreading sequence is used in the receiver (operating in synchronism with the transmitter) to despread the received signal, so that the original data may be recovered.
>
> In some multiple-access communication systems, a number of independent users are required to share a common channel. It is known to use bipolar phase shift keying spread spectrum (BPSK-SS) or quadrature phase shift keying spread spectrum (QPSK-SS) modems in such systems. However, the data rate or bit error rate (BER) of these systems for a given bandwidth is not always satisfactory for many applications, for example multi-user applications and multimedia applications including voice, data and video data streams.

[1] Near-far effect: When more than one users are active on a system, the power transmitted by non-reference users is suppressed due to the correlation between the codes of the active users. The interference caused by a non-reference user close to the receiver may have more power than a distant reference user, thereby drowning out the signal from the reference user.

> Object of the invention: Accordingly, it is an object of the present invention to provide a multi-dimensional DSSS modem, a modulator and a demodulator for such a modem and associated methods with which the applicant believes the aforementioned disadvantages may at least be alleviated."

The importance of the spreading sequences to spread spectrum is difficult to overemphasize, for the type of sequences used, its length, and its chip rate set bounds on the capability of the system that can be changed only by changing the spreading sequences [9, 10]. In order for an orthogonal set of sequences to qualify for use in a spread spectrum system, it is desirable for the sequences to have good cross-correlation and auto-correlation characteristics. Ideally, the cross-correlation between two different sequences of the same family would be 0 or constant and the auto-correlation would exhibit a single peak value at 0 time lag.

Families of complex spreading sequences exist that exhibit both these qualities [11]. These sequences are in the form of a complex number, with real and imaginary parts, so only a single sequence is required per user in a two-dimensional multi-user QPSK-like modulation system as opposed to a pair of binary sequences in convolutional systems [12]. Figure 1.1 shows the auto and cross-correlation of a length 13 root-of-unity filtered (RUF) sequence.

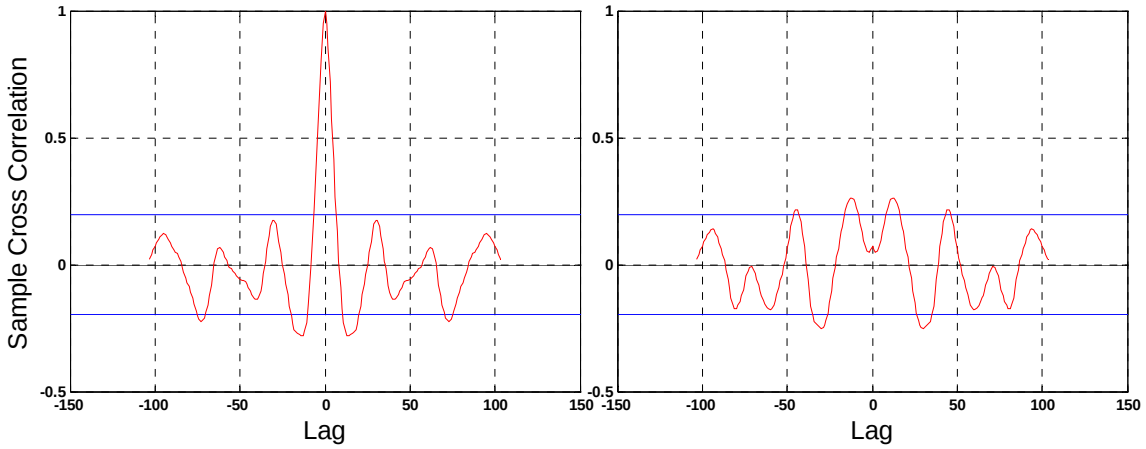


Figure 1.1.

Normalized auto-correlation and cross-correlation of a length 13 sequence. The horizontal lines indicate the 80% confidence intervals.

There is a strong market demand for cheap, but miniaturized, wireless systems. Such a system comprises of an RF transceiver that transfers antenna signals to bits and vice versa

and a digital sub-system for data processing. RF transceivers are typically realized in dedicated, expensive IC processes nowadays, whereas digital circuits are processed in the relatively cheap CMOS technology.

Parallel to the integration trend, nowadays there is the trend to integration of RF circuitry in CMOS technologies. When the technology is used without any special adaptations towards analogue design, the offering can be cheap. This is especially true if one wants to achieve the ultimate goal of full integration: the complete transceiver system on a single chip, both the analogue front-end and the digital demodulator implemented on the same die.

Due to limitations of CMOS performance in the RF range and analogue functions, bipolar CMOS (BiCMOS) technology is used most often for RF systems. BiCMOS combines the high speed and high driving capability of bipolar devices with the CMOS advantages of high density, low power and relatively low cost. BiCMOS technologies are commonly used, as bipolar transistors outperform CMOS transistors in many RF applications. This leads to smaller chip size and better design margins [13]. When comparing the relative sizes of BiCMOS, SiGe and CMOS radio design die areas, it can be seen that BiCMOS technology enables extremely small die sizes. BiCMOS also provides higher levels of integration and performance than similar CMOS solutions. The relative performances of CMOS, BiCMOS and bipolar technologies can be seen in Figure 1.2 [14].

1.2 Justification for research

It is clear from the literature that the theory regarding DSSS employing complex spreading sequences (CSS) is well developed, and several hardware and software implementations have been proposed.

The hardware implementations were either bulky [11] or required the use of a DSP, both of which are entirely digital. None of the implementations performed carrier recovery, which although treated as a trivial matter by the literature, still needs to be performed. A single chip solution does not yet exist that performs all functions required for a successful DSSS communication transceiver (implemented according to [8]). This will be the main contribution for this thesis, but the contribution is further appended by various RF design challenges: high-speed requirements make RF circuits extremely sensitive to the effects of

parasitics, including parasitic inductance, passive component modelling, as well as signal integrity issues.

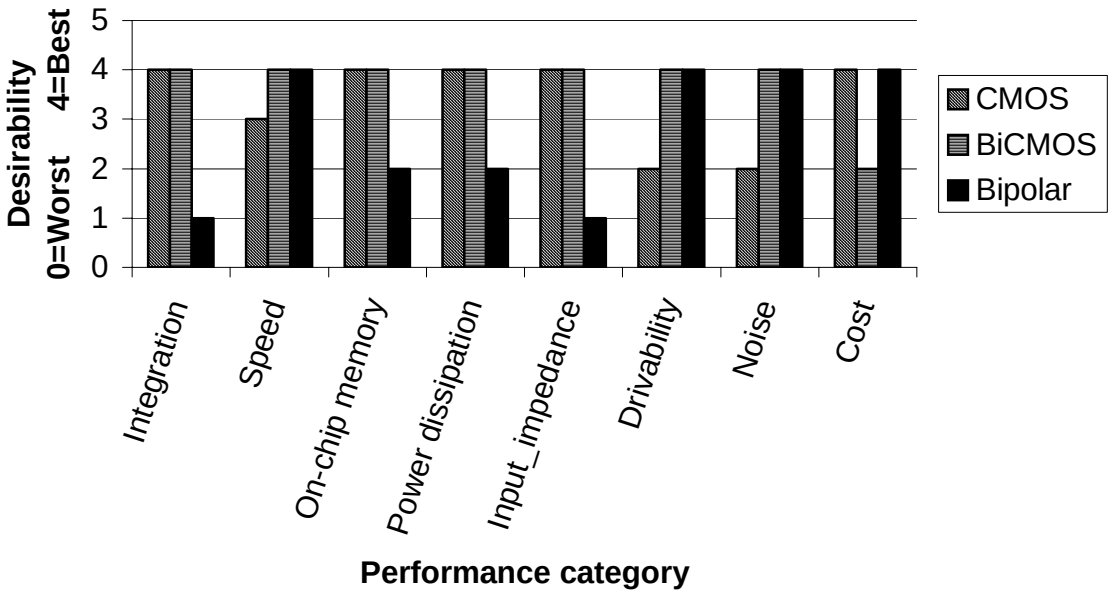


Figure 1.2.
Relative performance of CMOS, BiCMOS and bipolar technologies.

The design of a DSSS system introduces a set of trade-offs. Parameters such as power, BER, bandwidth, security and other related factors must be traded-off in order to find the optimal solution [7]. Under the DSSS scheme, each bit in the original signal is represented by multiple bits (chipping code) in the transmitted signal. The chipping code spreads the signal across a wider frequency band in direct proportion to the number of bits used [15]. The chipping code is a redundant bit pattern for each transmitted bit, thereby increasing the resistance of the signal to interference and corruption. The original data can still be recovered if a number of bits in the pattern are damaged during transmission. A longer chipping code supports more users and provides for greater security, but this is at the expense of increased bandwidth [16], as well as time to establish correlation at the receiver. This in turn decreases the efficiency with which the data is received, and should be compensated for. The PN sequence used in DSSS systems should have good cross correlation so as to support a multi-user environment, as well as good auto-correlation to allow for easy code synchronization. Various types of sequences, such as Kasami sequences and Gold sequences, are available for use in DSSS applications. However, trade-offs must be made once again when selecting the family of sequences. For instance, Gold codes provide a large sequence, whilst introducing relatively high noise levels.

Kasami sequences on the other hand introduce lower noise levels, but smaller family size. For this thesis, CSS is used (as discussed above Figure 1.1, and in Chapter 2). CMOS is further chosen from a perspective of cost (Figure 1.2), yet achieving adequate functionality for the research intended in this thesis.

The value system of the thesis will further encompass the following:

- optimize simulation time [17],
- facilitate verification,
- enable detailed analysis at the block and chip levels,
- manage and facilitate simulation with full parasitics,
- enable analysis (noise, IR, EM),
- include layout automation that can be used at appropriate points in the design, and
- enable several levels of passive modelling throughout the design process.

1.3 Methodology

The research process used in developing this thesis can be broken down to the following phases.

Phase 1: Literature studies to investigate system topologies developed elsewhere, and uniquely identify research niches (often either a system specification/topology and/or a specific circuit configuration). Challenges associated with recent device size miniaturization and associated simulation problems are included during such a study. Phase 1 was also supported by some project management, for instance development of work breakdown structures, and Gantt diagrams.

Phase 2: A system level analysis was proposed, and validated via system-level simulations (MATLAB was proposed for this purpose). The mathematical level analysis gave a good feeling of the feasibility, but was considered ideal as the circuit parasitics and stray elements cannot be modelled at this stage. An output of this phase was the system topology, system specifications, and system level simulations.

Phase 3: Upon accomplishing a system level design, the system was decomposed to gain an understanding at sub-system level, and sub-system specifications were developed. From the beginning, system integration was an important thought: hence, design was done to

include system interface specifications, too. These specifications are an output of this phase.

Phase 4: Circuit level designs were studied (to determine what exists elsewhere), and some unique solutions were proposed. Using suitable approximations, the circuits were first designed "by hand." Circuits were further tested by simulations: advanced CMOS circuit design software such as Tanner tools was deployed for this purpose. The outcome of this phase was several (sub-system) circuit schematics, and often circuit layouts (coined as part of a library). Such tools, when used with device models supplied by circuit manufacturers, could be effectively used in attaining worst case simulations.

Phase 5: The components of the library were integrated and a full-circuit layout was developed, i.e. a circuit level design and associated simulation was accomplished, and compared to the simulations output of Phase 2. A circuit netlist (including parasitic elements) was extracted from the layout, and also from the schematic, and this served as a further outcome of this phase.

Phase 6: The circuit netlist derived from layouts, and the circuit netlist derived from schematics were compared. During this phase, LVS (layout versus schematics) was performed and some more thorough, but automated, design evaluation: DRC (design rule check) was performed.

Phase 7: Via the Europractice programme, engaged by CEFIM, the IC was sent for fabrication. During this phase, the circuit models developed (in software) was used to construct some measurement printed circuit boards (PCBs). This was to enable speedy testing and measurement when the ICs are back from Europe. In parallel, the thesis was also partially completed.

Phase 8: The prototypes were received three months later, and measurements were performed. The thesis is further supported by the achieved measurement results.

Phase 9: The output of the research process was consolidated for an identified research journal, and further tested against overall international research endeavours in the field. In some cases, software will be written to archive the design process, to assist in future designs, one of the deliverables of the thesis. The thesis was fully completed thereafter.

Phases 4-6 are an important development part of this thesis, thus further discussed in Figure 1.3.

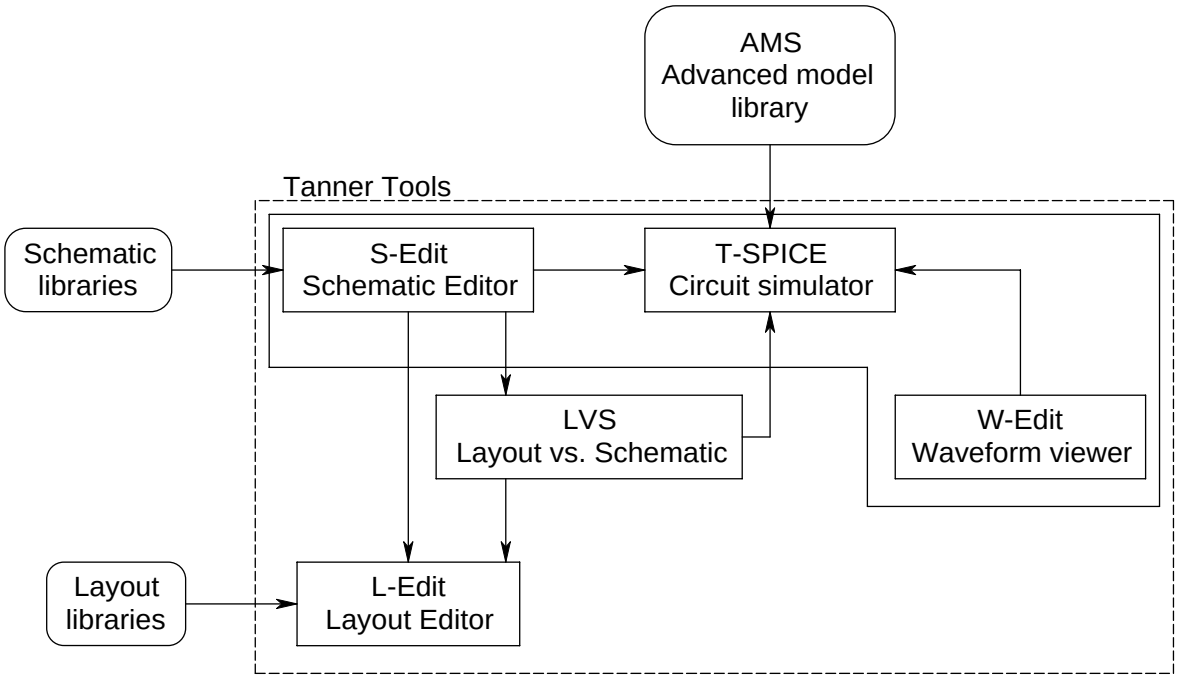


Figure 1.3.

Process followed during the design of the DSSS transceiver IC in terms circuit level design. The software tools that were used are shown at each node. The applications within the dashed frames are part of the Tanner tools.

The design carried out in this thesis involved the design of multiple stages, on a schematic and then layout basis [18]. Each sub-section was built up on a modular level, where each sub-section was simulated and verified, before being integrated. In layout a similar method of design was carried out from laying each transistor out in CMOS, however this was a far more intricate design process as factors such as parasitic capacitance had to be considered in each case. The layout was firstly verified using DRC. To complete all schematic, and layout requirements, the Tanner Tools Pro software package was utilised, as it includes all necessary software for schematic and layout design, as well as simulation. The tools included in the package that were utilised for this thesis are listed below.

S-Edit

Schematic capture was done using S-Edit, a software package included in the Tanner Tools Pro package to design schematics. The schematic contains all relevant information needed to create a netlist in various formats, including a compatible version for the use in SPICE

simulations. S-Edit exports the schematic design to a netlist using the 'SPICE OUTPUT' property of primitive devices[2].

T-SPICE

T-SPICE is a simulation engine based on Berkeley's SPICE3F5[3] simulation system. To be able to simulate a design, a netlist, as generated by S-Edit as well as the necessary model files are needed. Different types of simulations, (transient analysis, operating point determination, or frequency analysis) can be carried out, depending on the required simulation.

W-Edit

To interpret T-Spice output data, a waveform viewer named W-Edit was used. This software provided the graphical link between the simulation data and the user. W-Edit allows the user to perform various display options. W-Edit is also aimed mainly at the display of data from analogue simulation results, and was not very user-friendly in terms of displaying digital results. For this reason some of the results that were obtained from T-SPICE were exported to MATLAB which had better graph plotting capabilities, to be used for figures in this thesis.

L-Edit

L-Edit is the application within Tanner Tools used to develop the layout. At this level the transistors, capacitors and other devices are drawn in accordance with the design rules specified by the process from austriamicrosystems (AMS). The DRC module is included within L-Edit.

DRC

Due to the cost of IC manufacturing, certain rules such as spacing between tracks and minimum widths had to be carefully adhered to, in order for the manufactured IC to function properly, and according to the design process used. The DRC-engine has a database of all the rules as provided by AMS and cross-checks the layout according to these rules.

[2] A primitive device is a device which cannot be dissected to any lower level and its operation has to be defined. This includes resistors, capacitors transistors, diodes, etc.
[3] Developed at the University of Berkeley, http://www-cad.eecs.berkeley.edu

1.4 Outline of this thesis

The structure of this thesis is as follows:

- Chapter 1 (aligns with Phase 1 of the past sub-section) provides the background to the research, and provides motivation for the work. To allow for a full research investigation, a prototype is to be developed.
- Chapter 2 (Phase 2) further motivates the type of spreading sequence. A functional analysis for the prototype is proposed, and developed at a system-level. From the functional analysis, more clarity to the analogue and digital sub-systems is proposed.
- Chapter 3 (Phases 1, and 3-5) develops the analogue sub-systems at transistor level.
- Chapter 4 (Phases 1, and 3-5) develops the digital sub-systems at transistor level.
- Chapter 5 (Phases 1, and 6-8) serves to integrate the past two chapters, as per the system-level intentions of Chapter 2. The prototype is coined, in software, as an IC (a library), and an analogy is drawn to hardware. Considerations relating to device packaging are first investigated, and a qualification protocol is setup. A complete verification is done by characterizing the prototypes.
- Chapter 6 (Phases 8-9) serves to conclude the thesis by summarizing the contributions from the abovementioned process.

1.5 List of publications

Several publications have a result of works directly or indirectly relating to this thesis. A listing is provided below.

Journal publications

M. Božanić, S. Sinha, J. Schoeman, L.P. Linde, and M du Plessis, “CMOS Direct Sequence Spread Spectrum Transceiver Employing Complex Sequences,” submitted to the Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE), Oct. 2008.

M. Božanić and S. Sinha, "Software Aided Design of a CMOS Based Power Amplifier Deploying a Passive Inductor," Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 99, No. 1 (March 2008), pp 18-24.

S. Sinha and M. du Plessis, "PLL based frequency synthesizer implemented with an active inductor oscillator," Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 97, No. 3 (Sept. 2006), pp 237-242.

H.R. Swanepoel and S. Sinha, "Design of a frequency hopping spread spectrum transceiver for CDMA2000 systems", Africa Research Journal incorporating the South African Institute for Electrical Engineers (SAIEE) Transactions, Vol. 97, No. 3 (Sept. 2006), pp 248-254.

O.S. Adekeye, S. Sinha and M. du Plessis, "Design and Implementation of a CMOS Automatic Control Gain Control (AGC) Amplifier," South African Journal of Science, Vol. 102, No. 11/12 (Oct./Nov. 2006), pp. 606-608.

Peer-reviewed international conference proceedings

T.S. Elenjical, S. Sinha, and L.P. Linde, "Analogue CMOS DSSS CDLL synchronisation scheme employing complex spreading sequences," Proceedings: IEEE Melecon 2008, 5-7 May, 2008, Corsica, France, pp. 380-386.

N. Naudé, L.P. Linde, and S. Sinha, "CMOS Based Decision Directed Costas Carrier Recovery Loop (DDC-CRL) for a DSSS Communication System," Proceedings: IEEE Africon 2007, Sept. 26-28, 2007, Windhoek, Namibia.

M. Božanić and S. Sinha, "Design methodology for a CMOS based power amplifier deploying a passive inductor," Proceedings: IEEE Africon 2007, Sept. 26-28, 2007, Windhoek, Namibia.

S.W. Ross, and S. Sinha, "A pipeline analogue to digital converter in 0.35 μm CMOS," Proceedings: IEEE Eurocon 2007, Sept. 9-12, 2007, Warsaw, Poland, pp. 1096-1100

N. Naudé, S. Sinha and M. Božanić, "Design of a CMOS DSSS Transceiver with Carrier Recovery Employing Complex Spreading Sequences," University of Pretoria Research Symposium, Sanlam Auditorium, 26 Oct. 2006.

N. Naudé, M. Božanić, and S. Sinha, "Analogue CMOS Direct Sequence Spread Spectrum Transceiver with Carrier Recovery Employing Complex Spreading Sequences," Proceedings of the IEEE MELECON 2006, May 16-19, 2006, Benalmádena (Málaga), Spain, pp. 1227-1231. [Selected finalist for the IEEE Student Paper Contest – IEEE Region 8]

CHAPTER 2: SYSTEM ANALYSIS AND DESIGN

This chapter motivates this thesis by presenting the broader research context. A design motivation is proposed, developed mathematically, and verified at systems-level. Developed design specifications serve as a qualification protocol to address the research questions posed in Chapter 1.

2.1 Direct sequence spread spectrum (DSSS)

DSSS, also known as direct sequence code division multiple access (DS-CDMA), is one of two approaches to spread spectrum modulation for digital signal transmission over the airwaves. The design of a DSSS system introduces a set of trade-offs. Parameters such as power, bit error rate (BER), bandwidth, security and other related factors must be traded-off in order to find an optimal solution [19]. Under the DSSS scheme, each bit in the original signal is represented by multiple bits (chipping code) in the transmitted signal. The chipping code spreads the signal across a wider frequency band in direct proportion to the number of bits used [15]. The chipping code is a redundant bit pattern for each transmitted bit, thereby increasing the resistance of the signal to interference and corruption. The original data can be recovered if a number of bits in the pattern are damaged during transmission. A longer chipping code supports more users and provides for greater security, but this is at the expense of increased bandwidth [16], as well as time to establish correlation at the receiver. This in turn decreases the efficiency with which the data is received, and should be compensated for. The PN sequence used in DSSS systems should have good cross-correlation so as to support a multi-user environment, as well as good autocorrelation to allow for easy code synchronization. Various types of sequences, such as Kasami sequences and Gold sequences, are available for use in DSSS applications. However, trade-offs must be made once again when selecting the family of sequences. For instance, Gold codes provide a large number of codes, whilst introducing relatively high noise levels. As a rule of thumb only approximately 10% of the family size can be used whereafter the multi-user interference (MUI) would have grown to such proportions so as to render the processing gain useless [9]. Kasami sequences on the other hand introduce lower noise levels, but smaller family size. For this thesis, CSS is chosen. While CSS was proposed in 1992 [20], its usage in DSSS systems is proposed in the patent [12] for DSSS communication systems. The use of the CSS allows for various data rates by choosing

different sequence lengths and transmission bandwidths. It also allows for a choice of modulation techniques and guarantees the processing gain of 20 dB. When CSS are used, a transmitter can operate in both balanced and unbalanced fashion by using one spreading sequence for every two-dimensions utilised.

The proposed CSS are generalized-chirp like (GCL) sequences. The *r*th sequence is defined [20] as

$$c(r,k) = \begin{cases} W_N^{\frac{k^2}{2}+ql} & ; N \text{ even} \\ W_N^{\frac{k(k+1)}{2}+qk} & ; N \text{ odd} \end{cases} \tag{2.1}$$

where W_N is defined as $W_N = e^{-j\frac{2\pi r}{N}}$, $j = \sqrt{-1}$, r is any integer relatively prime to N, $k = 0, 1, 2, \ldots, N\text{-}1$, and q is an integer. Sequences must be sampled for their use in DSSS transceiver systems. The sampling rate is chosen so that the bandwidth, as determined by the IEEE 802.11 standard is

$$BW = \frac{f_{sample}}{RF\_samples\_per\_chip} \tag{2.2}$$

where BW is the bandwidth. The length of the spreading sequence is chosen arbitrarily. With increased sequence length, the number of possible users in a multi user environment increases. Alternatively, the sequence families can be used in one transmitter to increase data rates by means of serial-to-parallel conversion.

The spectrum of a long unfiltered GCL sequence is perfectly flat, as shown in Figure 2.1; therefore, for the use of such sequences in a band limited communication system, the sequences must be filtered.

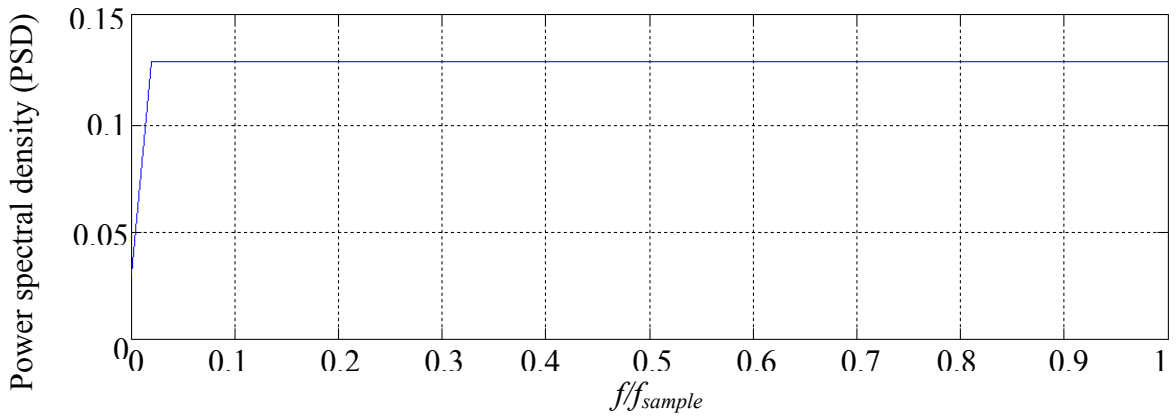


Figure 2.1.

Power spectral density (PSD) of length 49 complex sequence.

CSS exhibits two very important properties: good auto-correlation and good cross-correlation. These properties prove the orthogonality of CSS. Ideally, the cross-correlation between two sequences inside a family will be a constant, and the autocorrelation will exhibit the peak value at the zero-time lag. Filtered sequences do not have ideal properties, but the properties can be assumed within a confidence interval. The two correlation functions of length 13 sequences are shown in Figure 2.2 and Figure 2.3, respectively.

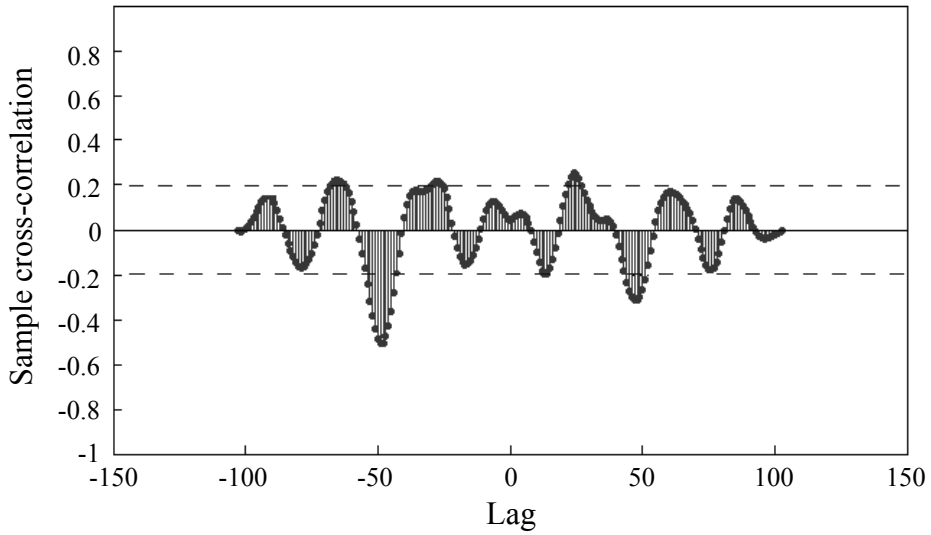


Figure 2.2.

Cross-correlation of two sequences of length 13. Lines $y = \pm 0.2$ present 80 % confidence intervals.

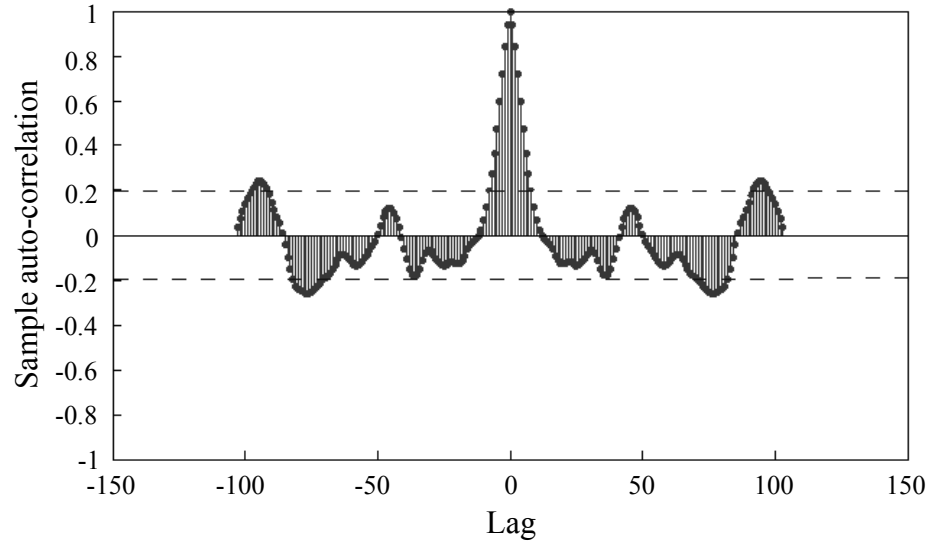


Figure 2.3.

Auto-correlation of the real part of the length 13 sequence. Lines $y = \pm 0.2$ present 80 % confidence intervals.

The exact sequences used in this thesis are protected by a non-disclosure agreement (NDA) between the author and the University of Pretoria, and will therefore not be detailed here.

2.2 System Analysis

The system analysis depends on the type of modulation scheme. Two techniques were considered, BPSK and Q^2PSK. Section 2.2.1 presents the BPSK based system analysis, which also serves to give a general system analysis, and then section 2.2.2 presents QPSK based system analysis. Furthermore, in Section 2.2.1 Gold codes of length 31 chips per data bit were chosen for the first analysis as they are easier to implement, and yield a CDMA system comparable with existing binary standards, which may also simultaneously provide some useful benchmark to compare with the CSS used in Section 2.2.2.

2.2.1 BPSK based system analysis

Figure 2.4 presents the functional analysis for a DSSS transceiver.

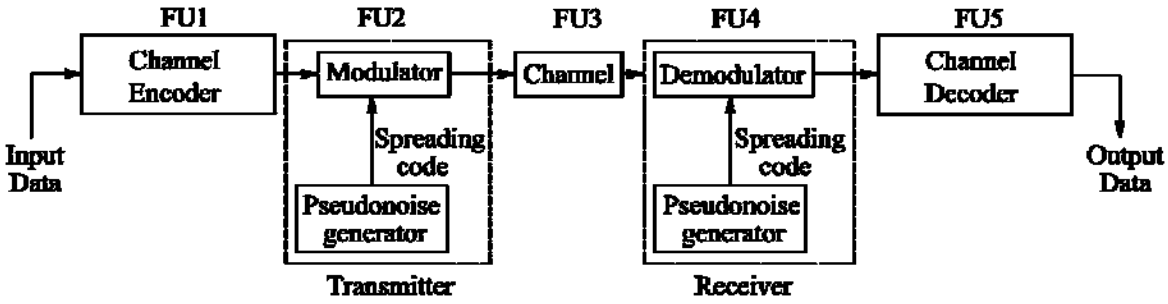
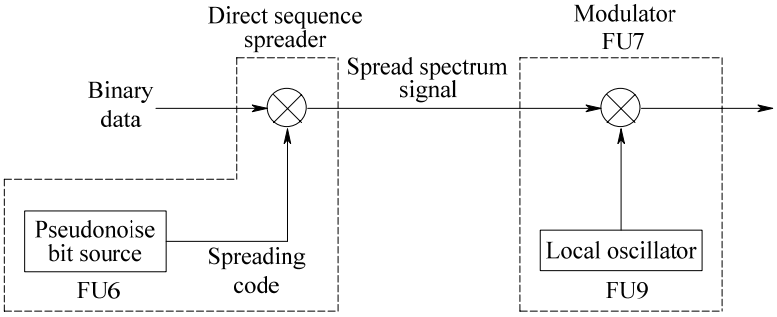


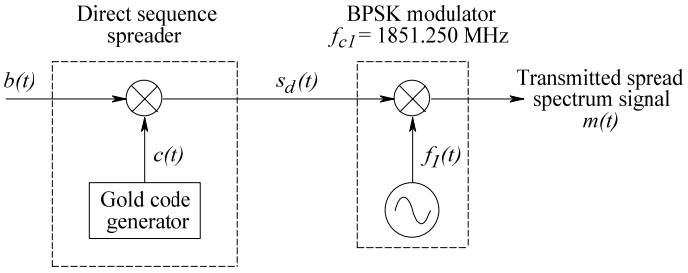
Figure 2.4

DSSS transceiver functional analysis. FU stands for functional unit.

Figure 2.5 and Figure 2.6 shows the transmitter and receiver functional analysis separately.



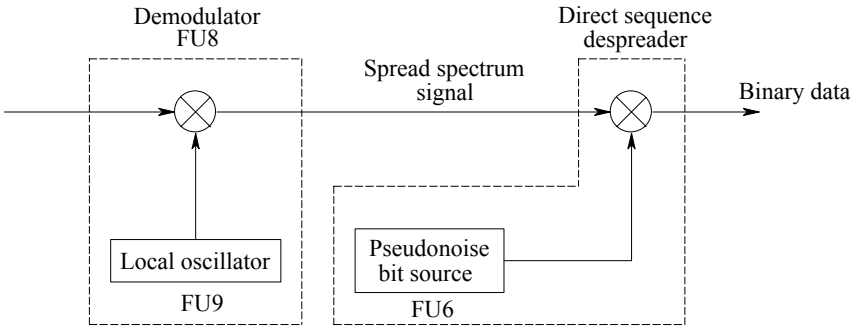
(a)



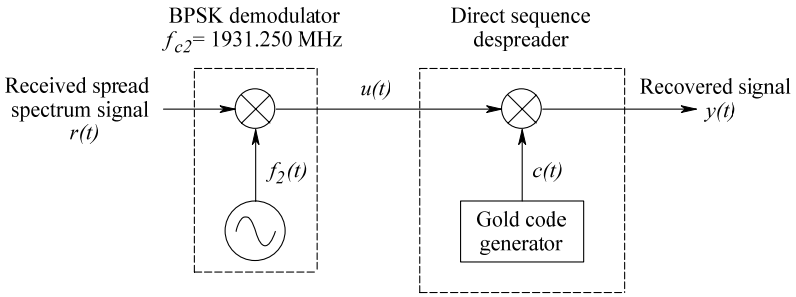
(b)

Figure 2.5.

Functional block diagram of the (a) generalized DSSS transmitter module, and (b) transmitter module employing BPSK modulation and a Gold sequence.



(a)



(b)

Figure 2.6.

Functional block diagram of the (a) generalized DSSS receiver module, and (b) receiver module employing BPSK modulation and a Gold sequence.

The system receives a digital signal as input. The channel encoder (FU1) then produces a signal with a relatively narrow bandwidth around some centre frequency. The data signal is then sent through the direct sequence (DS) spreader, which spreads the received signal using the user specific chipping code generated by the pseudonoise (PN) bit source (FU6). This serves to increase the bandwidth of the data signal, or in effect, spreads the spectrum. This signal is then sent to the transmitter (FU2), where it is subsequently modulated (FU7) with the HF output of the LO (FU9). BPSK/NRZ is used as a digital-to-analogue encoding scheme in the modulator in this subsystem. This is used to represent the phase shifted data in terms of 1's and -1's, rather than 1's and 0's.

The signal is then transmitted over the wireless channel (or air interface) (FU3) to the receiver (FU4). The received signal is then despread using the same scheme as the modulator in FU6. The channel decoder (FU5) recovers the original data signal. The signal is then despread by the DS despreader, using the same chipping code as used in the transmitter (FU2). This decreases the input signal bandwidth (or effectively despreads the spectrum of the input signal), to obtain the original encoded data signal.

The implementation discussed above assumes signal transmission between the mobile station (MS) and the base transceiver station (BTS). The demodulation of such a system requires the LO's at both the transmitter and the receiver to operate at the same frequency in order to convert the received signal to baseband.

The following paragraphs discuss the transmitter shown in Figure 2.5 (b).

The direct sequence (DS) spreader is used to spread the received binary signal, *b(t)*, with the user specific chipping code, *c(t)*, that is generated by the Gold code generator. The input signal bit rate was chosen so as to allow for transmission of good quality signals e.g. music. This spreading function serves to increase the bandwidth of the data signal, or effectively spreads the spectrum in direct proportion to the number of chips used. Spreading results in the signal in

$$s_d(t) = b(t)c(t) \tag{2.3}$$

The results of this signal spreading can be seen in Figure 2.7.

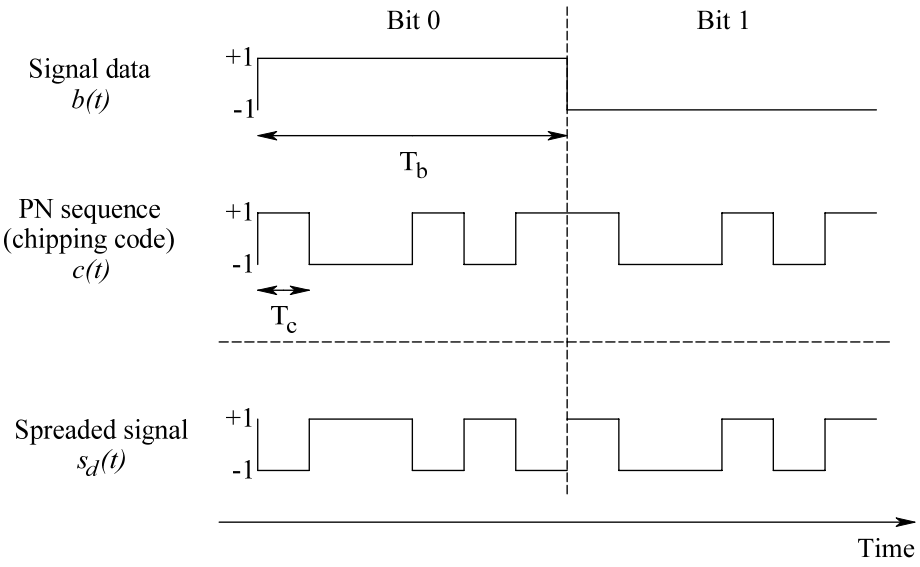


Figure 2.7.

Representation of binary data, *b(t)* and PN sequence, *c(t)* used in BPSK DSSS systems, as well as the resulting signal $s_d(t)$ when the data signal is spread.

A PN sequence of length $L = 31$ bits results in a transmitted signal rate of 31 Mcps when transmitting a high quality signal (for instance, a music signal at 1 Mbps). In the ideal case, an RF bandwidth 31 times greater than the original signal bandwidth is required for transmission of the spread spectrum signal. Thus, in this case a baseband bandwidth of 31 MHz is required for successful transmission of such a signal.

The required RF bandwidth is related to the data rates in the following way when using ideal Nyquist filtering (i.e. with roll-off, $\alpha = 0$):

$$B_T = 2f_{NYQ} = f_c = Lf_b \tag{2.4}$$

B_T is the bandwidth required for transmission (after modulation), L is the length of the chipping code, f_{NYQ} is the Nyquist frequency, f_c is the reciprocal of the chip period and f_b is the reciprocal of the data period.

Figure 2.8 serves as a graphical representation of the spreading of the signal bandwidth.

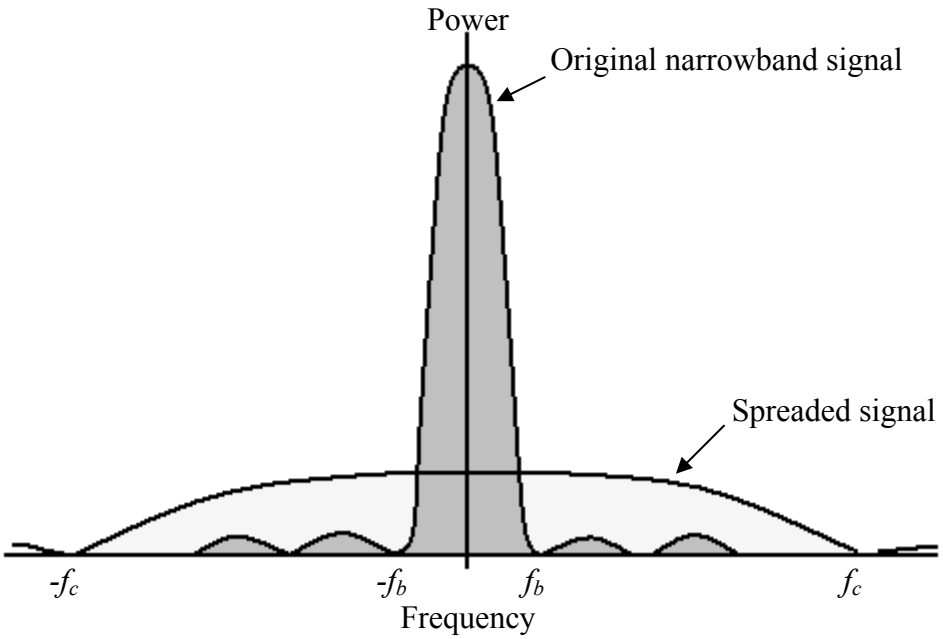


Figure 2.8.

Relative bandwidth of the original signal and the spread spectrum signal obtained by modulation with a chipping code.

The signal is subsequently modulated onto the carrier (operating) frequency. The carrier frequency of the transmitter module has been chosen to be 1851.250 MHz, to comply with CDMA2000 specifications [21]. BPSK has been used as the digital-to-analogue encoding scheme in the modulator in this subsystem as it is one of the more power efficient modulation schemes. BPSK modulation results in a signal of the form

$$m(t) = s_d(t) A \cos(2\pi f_{c1} t) \tag{2.5}$$

where A is the amplitude of carrier signal and f_{c1} is the transmitter carrier frequency.

At this point, external filtering of the signal may be done in order to reduce the transmitted bandwidth. For this function, Nyquist's criterion [15] should be considered.

The RF modulated spread spectrum signal, *m(t)*, is then transmitted over the air interface to the receiver. This channel (air interface) may add a narrow band interference signal, *i(t)*, to the transmitted signal that has been spread, as shown in Figure 2.9. The following signal results:

$$r(t) = m(t) + i(t) = s(t) A \cos(2\pi f_{c1} t) + i(t) \tag{2.6}$$

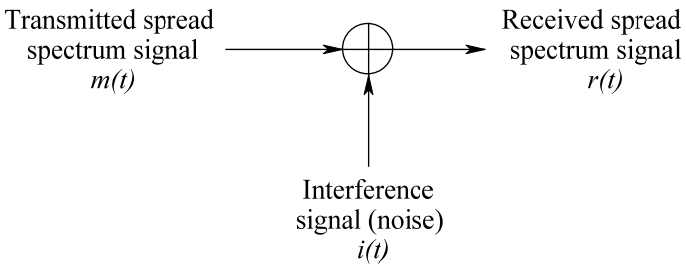


Figure 2.9.

Interference added by the transmission channel (air interface).

Despreading of the interference signal works in the same way as the original spreading of the data signal (commutative function), thus the interference signal is spread over a wider bandwidth. When the spread data signal is despread the original narrowband signal is obtained. Spreading of the received signal, therefore results in the original data signal and a wideband interference signal with low amplitude. Most of this interfering signal can then be filtered out, leaving the narrowband data signal. This interference term is however neglected in the present analysis in order to simplify the calculations.

The received signal is demodulated using the same modulation scheme as previously used to modulate the signal before transmission, as shown in Figure 2.6 (b).

In the case of the DSSS transceiver, the signal is received from the BTS. The BTS transmitter uses the same modulation scheme as the MS transmitter (i.e. BPSK), but at a frequency of 1.93125 GHz. Demodulation of the RF signal results in a signal that has components at both the sum and difference of the spread transmitted signal frequency, and the oscillator frequency (this is explained in more detail later). The high frequency signal components can be filtered out, leaving only signal components present at the spread signal frequency, $s_d(t)$.

The signal is then despread by the DS despreader which uses the same chipping code, $c(t)$, as that which was generated at the transmitter (assuming perfect code synchronisation).

The recovered signal is

$$y(t) = c(t)s_d(t) = b(t)c^2(t) \tag{2.7}$$

However

$$c(t) \cdot c(t) = 1 \tag{2.8}$$

This is true as *c(t)* takes on only two values, -1 and 1. The result is the original data signal being recovered at the system output.

$$y(t) = b(t) \tag{2.9}$$

2.2.2 QPSK based system analysis

In [22] four distinct two-dimensional (2D) modulation techniques were proposed for the DSSS system employing the CSS: QPSK, $\pi/4$-QPSK, 8-PSK and 7x1-PSK [22]. A higher processing gain is obtained when the QPSK transceiver uses SSB and is operated in balanced mode, data transmission rate cannot be increased by more than a factor of two. For these reasons, a basic QPSK design will normally employ DSB modulation. The signal constellation of the basic QPSK modulation scheme is given in Figure 2.10.

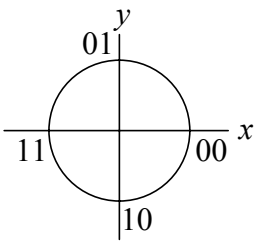


Figure 2.10.
QPSK constellation.

For this thesis, only the QPSK-based system is of importance [12], since the final Q^{2}PSK modulation scheme is derived from it (i.e., two 2D QPSK systems in parallel).

Balanced and unbalanced configurations of the Q^{2}PSK DSSS transmitter

Figure 2.11 shows a transmitter operating in the balanced configuration. With balanced transmission the same data stream is transmitted on all orthogonal bases (the inphase and quadrature components inclusive), so that whenever the signal of one or more components is lost during the transmission the original data can be recovered from other components. Thus, an inherent fourth order diversity gain is achieved with this particular configuration. If the incoming data sequence is $a(t)$, then the transmitted signal is [12]

$$\begin{aligned} u(t) &= a(t)C_r \cos\omega_c t + a(t)C_i \cos\omega_c t + a(t)C_r \sin\omega_c t + a(t)C_i \sin\omega_c t \\ &= a(t)\{\zeta_1(t) + \zeta_2(t) + \zeta_3(t) + \zeta_4(t)\} \end{aligned} \tag{2.10}$$

where C_r is the CSS real part, C_i is the CSS imaginary part, and $\{\zeta_i\}$, i =1, 2, 3, 4 constitutes the 4D orthogonal base. For this equation to be valid, $a(t)$ must have non-return

to zero (NRZ) levels of 1 and -1. This equation was expanded for further comparison with the unbalanced configuration.

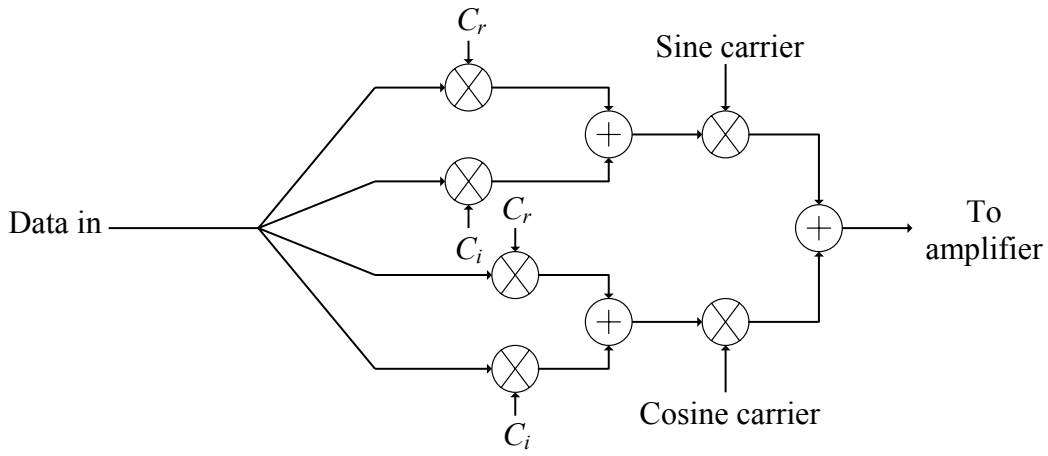


Figure 2.11.

Balanced Q^2PSK configuration of a DSSS transmitter.

Figure 2.12 shows a transmitter operating in an unbalanced configuration. The data signal is converted into four parallel data streams $a_1(t)$, $a_2(t)$, $a_3(t)$, and $a_4(t)$, and each signal is multiplied with different base-carrier combinations. The transmitted signal is now

$$\begin{aligned} u(t) &= a_1(t)C_r \cos\omega_c t + a_2(t)C_i \cos\omega_c t + a_3(t)C_r \sin\omega_c t + a_4(t)C_i \sin\omega_c t \\ &= a_1(t)\zeta_1(t) + a_2(t)\zeta_2(t) + a_3(t)\zeta_3(t) + a_4(t)\zeta_4(t) \end{aligned} \tag{2.11}$$

It can be seen from Equations (2.10) and (2.11) that the signals transmitted in the balanced and unbalanced configurations have the same form, and that by including and excluding the serial-to-parallel converter from the circuitry the transmitter (and receiver) can be made to operate in both modes.

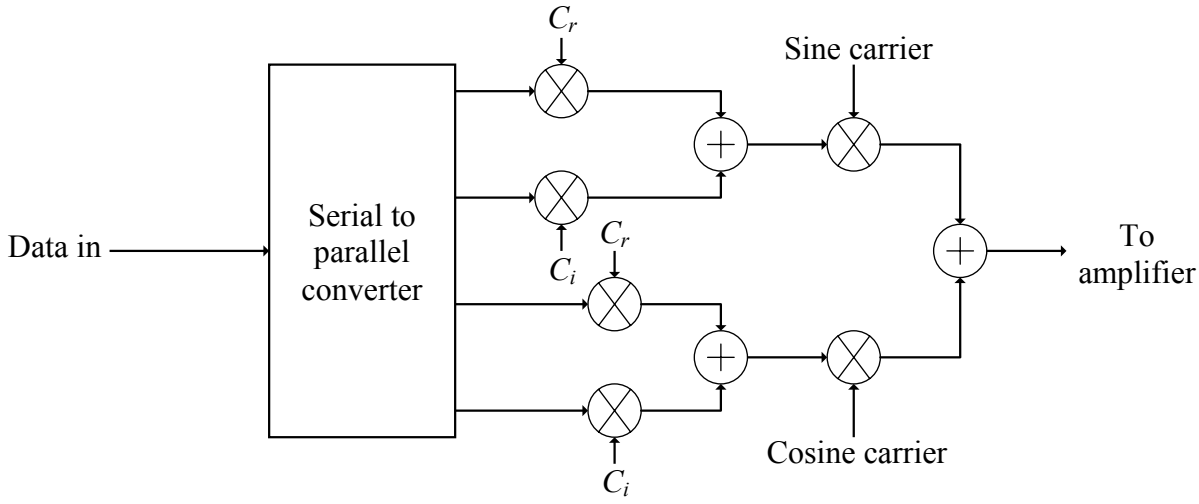


Figure 2.12.

Unbalanced Q^2PSK configuration of a DSSS transmitter.

Channel models

The DSSS transmitter operates over noisy and fading channels.

The noise in a channel can be modelled by Gaussian (normal) distribution. PDF of this distribution is given by

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}}, x \in \mathbb{R} \tag{2.12}$$

where μ is the mean and σ^2 is the variance. Noise has an additive effect on the transmitted signal.

Fading of the channel can be modelled by the Rayleigh and Rician models. The Rayleigh fading signal amplitude is described by the PDF [16]

$$f(\alpha) = \begin{cases} \frac{\alpha}{\sigma^2} e^{-\alpha^2/2\sigma^2}, \alpha \geq 0 \\ 0, \alpha < 0 \end{cases} \tag{2.13}$$

The Rician fading amplitude is given by the PDF [16]

$$f(\alpha) = \frac{\alpha}{\sigma^2} e^{-(\alpha^2+s^2)/2\sigma^2} I_0\left(\frac{s\alpha}{\sigma^2}\right), \alpha \geq 0 \tag{2.14}$$

where s^2 represents the power of the received nonfading component and $I_0(s\alpha/\sigma^2)$ is the modified Bessel function of order zero. Both the Rayleigh and Rician distributions have a multiplicative effect on the transmitted signal.

Topology trade-offs

The following is the list of trade-offs that govern the topology chosen.

- Various modulation schemes were proposed for a DSSS transceiver employing complex sequences.
- The transceiver can be operated in balanced and unbalanced modes. When the balanced mode is used, the maximum data rate that can be transmitted over the channel is determined purely by the available bandwidth, the CSS length and the roll-off factor of the Nyquist filter used for bandwidth limiting. When operated in this mode the system cannot be made faster than $BW/(1+\alpha)L$, where BW is the bandwidth, α is the roll-off factor of the Nyquist filter and L is the CSS length. However, if one of the signal components is lost in transmission, the data can still be recovered from the other signal components. When the unbalanced mode is

applied, the possible data rate is $BW/(1+\alpha)L$ times the number of the orthogonal bases used (four in the case of this thesis).

- Another trade-off exists between using single sideband (SSB) and double sideband (DSB) for modulation. SSB uses less bandwidth, yet obtains faster data transmission. However, for SSB modulation, a specific choice of the CSS must be made: sequences must be capable of annulling one sideband when real and imaginary parts are mixed with the sine and cosine carriers, and added together. A further drawback is that with SSB implementation, the transceiver cannot operate in unbalanced mode.
- There is a large number of CSS to choose from. It is possible to generate a number L of CSS in a family, where L is the CSS length (where L is a prime number). Auto-correlation and cross-correlation properties (together with information for signal recovery) improves with increase in the CSS length, but the data rate ($BW/(1+\alpha)L$) decreases.

Topology choices

The following choices from the previous subsection took precedence.

- The thesis is aimed for research purposes only. Therefore, only one CSS is used in conjunction with a sine carrier and a cosine carrier, giving effectively only four orthogonal bases (CSS real part and inphase carrier, CSS real part and quadrature carrier, CSS imaginary part and inphase carrier; and CSS imaginary part and quadrature carrier), yielding Q^2PSK (i.e., two 2D QPSK modulators in parallel, as described previously).
- Both balanced and unbalanced operation modes of the transceiver are desirable for implementation, the thesis includes a possibility to switch between the two modes of operation.
- Since the prototype device makes use of only one CSS in a family, shorter CSS are desired to obtain high data rate. Sequence of length L=13 from the Zadoff-Chu (GCL) CSS family is the most viable option [12].

In the rest of this section, the first concept design for this thesis is presented. Similar to an earlier section, a functional analysis is presented. For the purpose of the functional analysis, the transmitter (Figure 2.13) and receiver (Figure 2.14) will be considered separately.

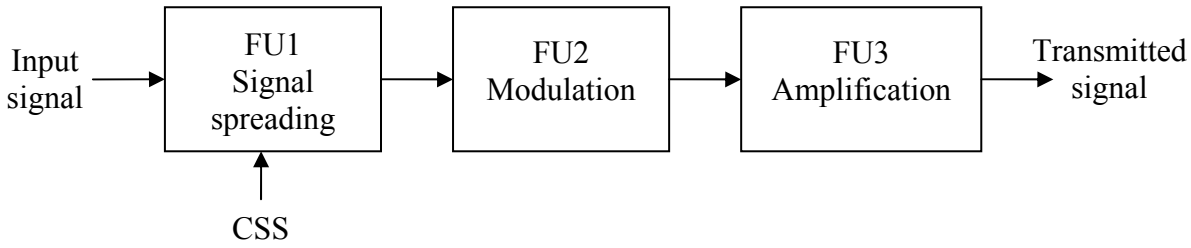


Figure 2.13.

Functional diagram of the proposed DSSS transmitter.

A binary signal is received as an input to the transmitter. Relevant complex calculations are performed in FU1. The signal is multiplied by a CSS available from the outside of the chip, which spreads it in the frequency domain. FU2 serves to modulate the output of FU1 to the required frequency band. In FU3 the output of FU2 is amplified to the power level required for the transmission.

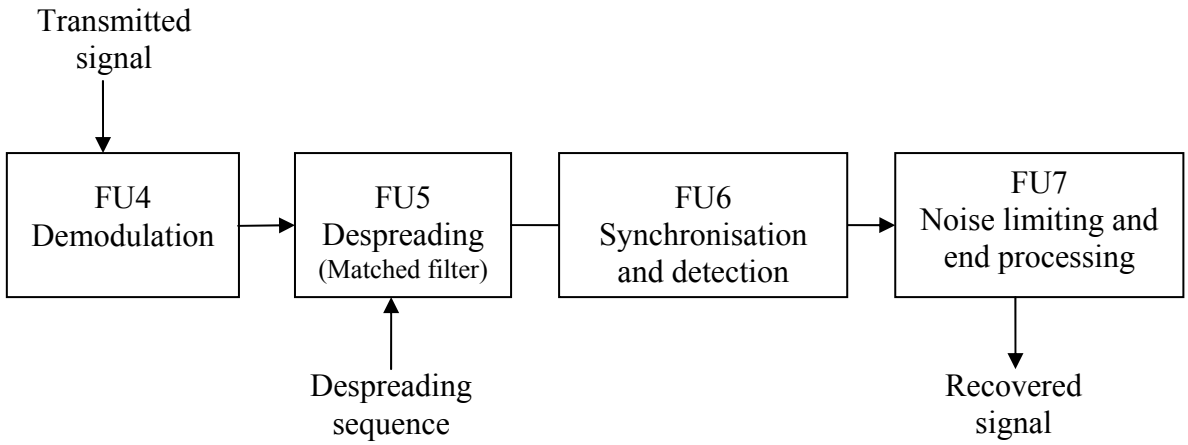


Figure 2.14.

Functional block diagram of the proposed DSSS receiver.

The transmitted signal corrupted by noise is amplified (by a low noise amplifier (LNA)) and quadrature demodulated by FU4 of the receiver. After demodulation and filtering (LPF), the signal is despread by a despreading sequence in FU5 (decorrelation matched filter). The despread signal of FU5 is sampled and level detected by FU6, thereby recovering the data as a baseband signal. Necessary signal shaping is performed in FU7. Here, the signal is filtered in order to limit the noise created in the process of demodulation. This subsystem also includes the end processing of the signal, such as the combining of the signal components (i.e., parallel-to-serial conversion) and wave shaping.

The next few paragraphs serve to analyze some of the above FUs in more detail.

In FU1, spreading of the binary data signal is performed. First, the signal is passed through a switching circuitry which determines whether the transmitter is operating in the balanced (Figure 2.11) or unbalanced (Figure 2.12) configuration. If the unbalanced mode is used the serial-to-parallel conversion is done to obtain four data streams. In the balanced mode the signal is simply fed to four lines. The four data streams are then mixed with the CSS real and imaginary parts. The CSS are available externally, either from a personal computer (PC) or from an external memory module. In simulation the root-of-unity filtered (RUF) CSS real and imaginary parts are treated as separate inputs (the so-called equivalent baseband form). Sequences are sampled at the rate as follows:

$$f_{sample} = BW \cdot samples\_per\_chip = 20\,\text{MHz} \cdot 8\,\text{samples/chip} = 160\,\text{Msamples/s} \quad (2.15)$$

The chosen spreading sequences of L=13 chips result in 8 × 13 = 104 samples for one sequence repetition.

For the block diagram of the implementation of this FU (assuming the unbalanced mode), refer to Figure 2.15.

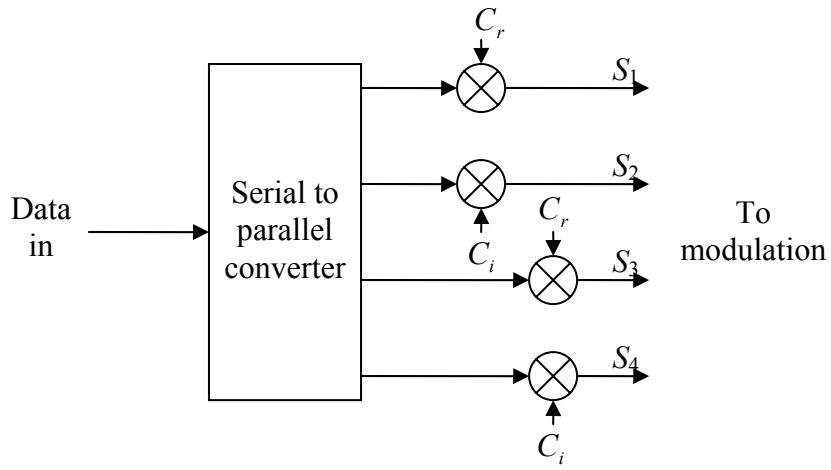


Figure 2.15.
Block diagram of FU1. C_r and C_i are the CSS RUFed real and imaginary parts and S_1 to S_4 are signal lines.

The mixers that multiply data streams S1 to S4 with the CSS real and imaginary parts, and the serial-to-parallel converter form the core of this subsystem from a microelectronics perspective.

Modulation is implemented by FU2. In this subsystem four signals are mixed with the sine and cosine carriers running at the frequency within the range of 2.4 GHz ISM band. The

four signal lines are then added and fed to the amplifier. This is shown in Figure 2.16. LO with phase shifters and mixers is used in the implementation of this subsystem.

FU3 serves as RF amplifier and transmitter of the signal. The core of this block is a power amplifier (detailed in chapter 3). This is the last bit of circuitry on the transmitter side of the transceiver IC.

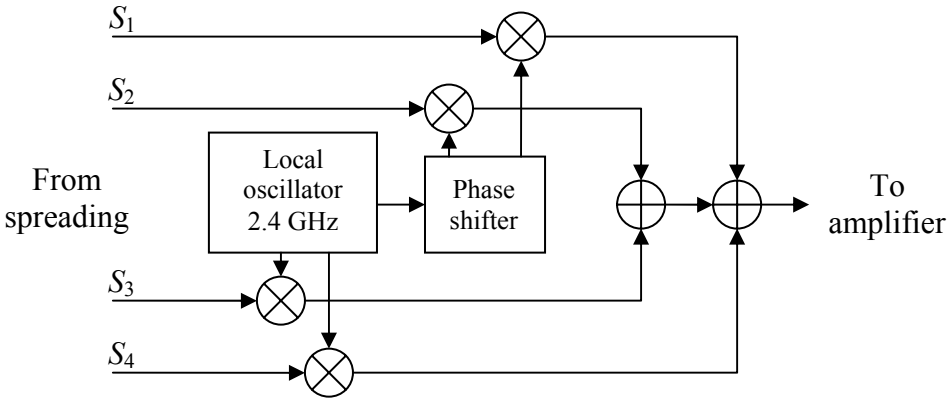


Figure 2.16.
Block diagram of FU2.

The functional block diagram of the receiver is shown in Figure 2.14. The signal is first amplified (by a LNA), and demodulated (FU4) from a noisy, fading channel at the carrier frequency (close to 2.4 GHz). This is on-chip circuitry on the receiver side of the transceiver IC.

This is followed by demodulation (FU4) and despreading (FU5). The order of despreading and demodulation assists from a perspective of implementation, since better isolation can be achieved (prevention of RF coupling). At the first concept design level the detected signal was first brought down to baseband by being split into two lines and mixed with the sine and cosine carriers at the required frequency. Signals are then filtered to eliminate the double frequency carrier components.

Each of the signals is then split again and as the CSS are pre-RUFed at the receiver (i.e., effectively interpolated and filtered on the unity circle, with roll-off factor α = 0, closely resembling a Nyquist filter), despreading is achieved in the receiver by merely decorrelating the RUF CSS sequences by a local pre-stored zero-interpolated replica of the relevant spreading sequence components, C'_r and C'_i, containing only the non-zero primary sequence samples.

Integration and dump circuitry as well as comparators are then used as the decision logic on each signal line (FU7). . In this way, four signals are created that resemble the four original parallel data streams, S_1 to S_4.

In the case of the balanced receiver configuration, all four data lines will ideally contain exactly the same signals as the input signal to the transmitter, while in the case of the unbalanced configuration the four data lines will have to be passed through a parallel-to-serial converter to obtain the original data signal.

Data and sampling rates of signals on the receiver side of the transceiver IC are identical to the data and sampling rates of the signals on the transmitter side. The core of the receiver consists of mixers, an oscillator with phase shifters, switching circuitry, integration circuitry, comparators, and a parallel-to-serial converter. The complete block diagram of the transceiver discussed so far is given in Figure 2.17 [12]. Input is marked with Data in and output with Data out. The unbalanced transceiver configuration is assumed. As discussed earlier, the primary sampled zero-interpolated CSS real (C'_r) and imaginary (C'_i) parts are input from outside the IC in the receiver.

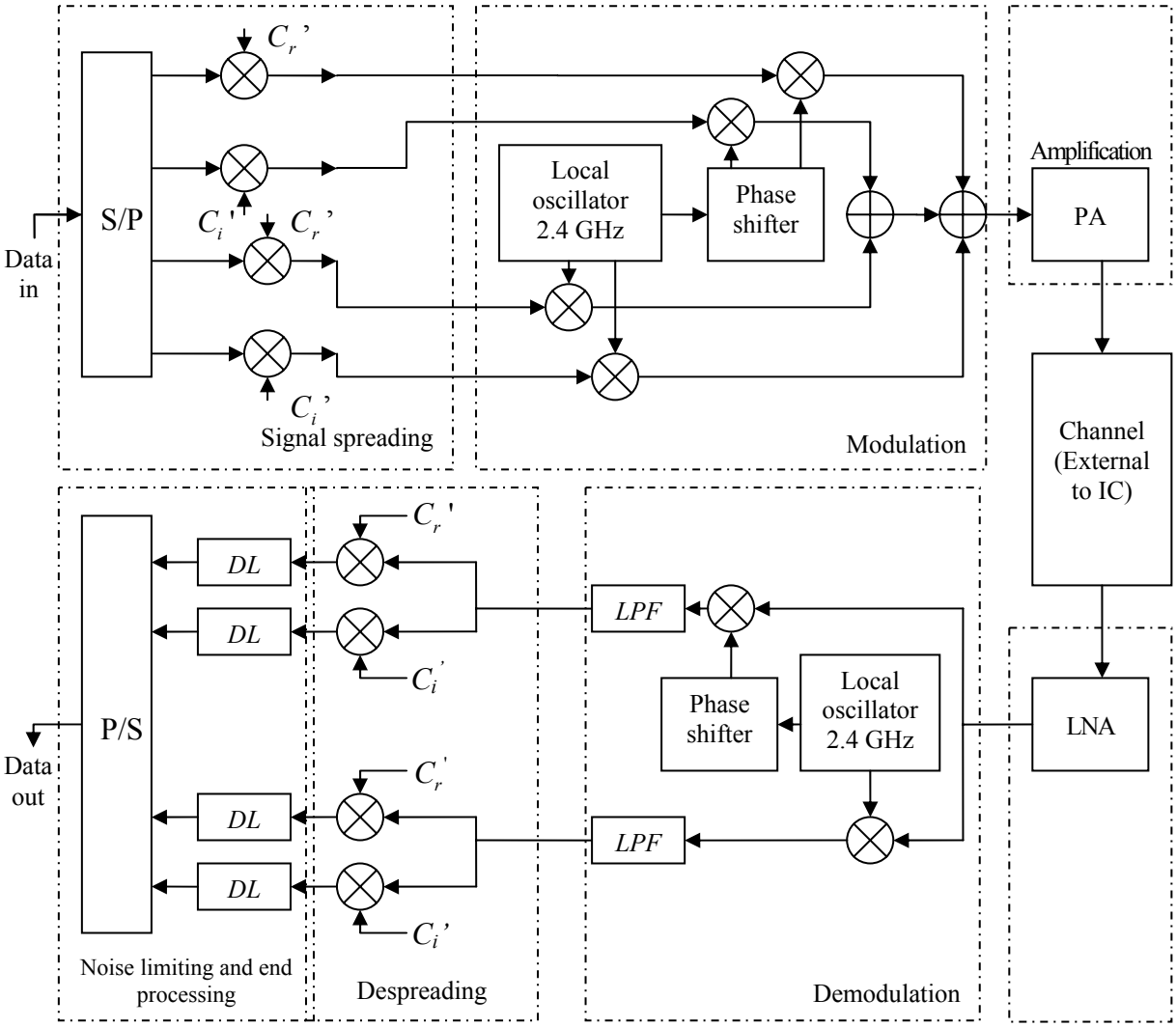


Figure 2.17.

Concept design of the transceiver. LPF stands for low-pass filter and DL for decision logic.

To simplify the discussion, thus far receiver synchronization remained a silent issue. The receiver synchronization scheme consists of three subsystems running in parallel, namely the acquisition circuitry, a decision directed Costas carrier recovery loop (DDC-CRL) and a complex delay lock loop (CDLL) [23]. The major advantages of this unique code locking scheme is that it eliminates the problem of arm imbalance, simplifies hardware, and improves tracking ability [23]. This is presented in Figure 2.18.

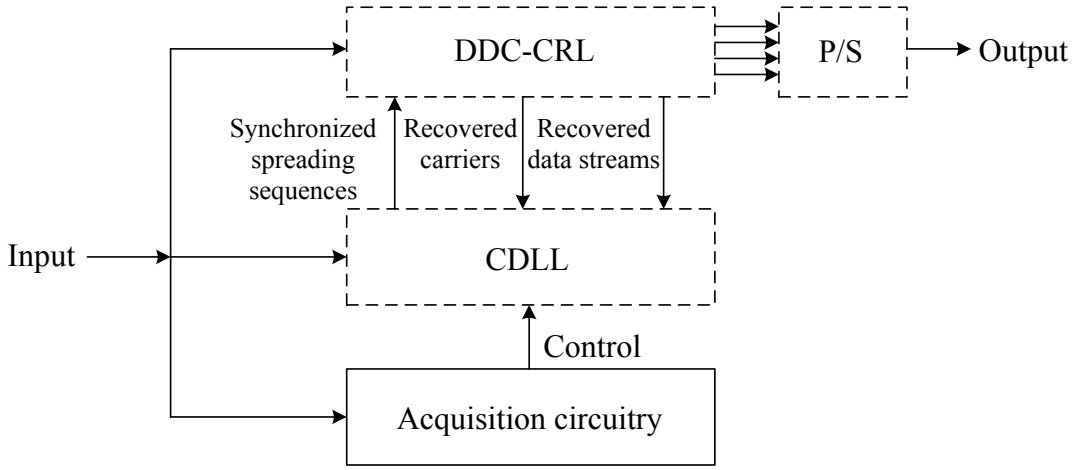


Figure 2.18.

Receiver with synchronization.

The four outputs of the DDC-CRL leading to the P/S converter are the recovered data streams. The CDLL has four inputs: the first input is the received four dimensional signal, the second input is a course clock reference control signal from the acquisition circuitry, and the third input is the recovered data stream that are outputs from the DDC-CRL. This recovered data stream serves to remove the data modulation on each of the branch signals [8], and the fourth input is the recovered carrier that is output from the DDC-CRL. The CDLL then processes these signals and outputs synchronized despreading sequences.

Figure 2.19 analyses the CDLL. FU1 serves to despread the incoming four dimensional signal. It is assumed that the incoming signal has already been band limited and amplified via a receiver front end. FU1.1 and FU1.2 serve to despread the inphase and quadrature components of the received signal, respectively. To ensure symmetry of operation, FU1.1 and FU1.2 should be matched units in terms of speed of operation and signal deterioration [8]. FU2 serves to demodulate the inphase and quadrature signals. It is assumed that the DDC-CRL has recovered the carrier signals ideally, i.e. proper demodulation and sequence matching occurs in the demodulation process. Since analogue mixing will have to be performed in FU1, mixers will be required in FU1.1 and FU1.2. FU3 serves to perform signal conditioning on the signals which includes filtering of the signal to remove unwanted signal components that may have been introduced by FU1. FU3.1 and FU3.2 are necessary functions in order to achieve the required signal conditioning. FU4 serves to modulate the incoming inphase and quadrature carriers with the recovered data that is output from the DDC-CRL. It is assumed that this recovered data is such that its characteristics are similar to the original parallel to serially converted data from the

transmitter. FU5 serves to combine the modulated inphase and quadrature components. FU6 serves to perform signal conditioning in the form of loop filtering. This is done to minimize the error signal in order to achieve minimum timing error between the incoming CSS and the locally generated despreading sequence [24]. After conditioning, FU6 outputs the recovered synchronized despreading sequence as well as a difference despreading sequence (IF6). These difference despreading sequences are equal to the difference between a late and an early replica of the recovered synchronized despreading sequence [8], and serves to increase the linear range of the S-curve[1] for improved code locking.

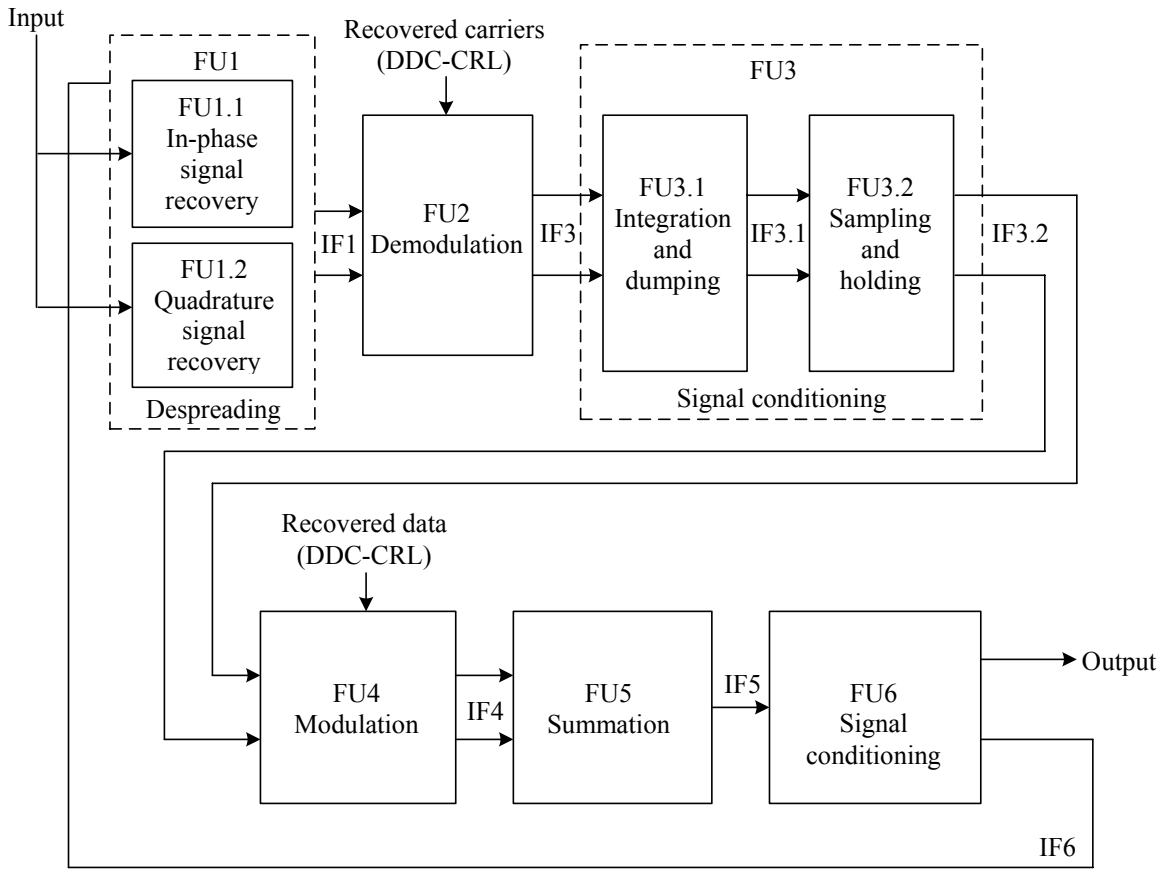


Figure 2.19.

Functional analysis of the CDLL.

The DDC-CRL and the CDLL operate as one integrated recovery loop. This combined structure recovers the quadrature carriers, synchronises the locally generated despreading sequences and recovers the different data streams [8]. Figure 2.20 depicts the DDC-CRL. The CDLL has been adapted from [27].

[1] The normalised CDLL error function, otherwise known as the S-curve [23]. Increasing the linear range of the S-curve results in an increased code locking range and therefore a decreased code timing error.

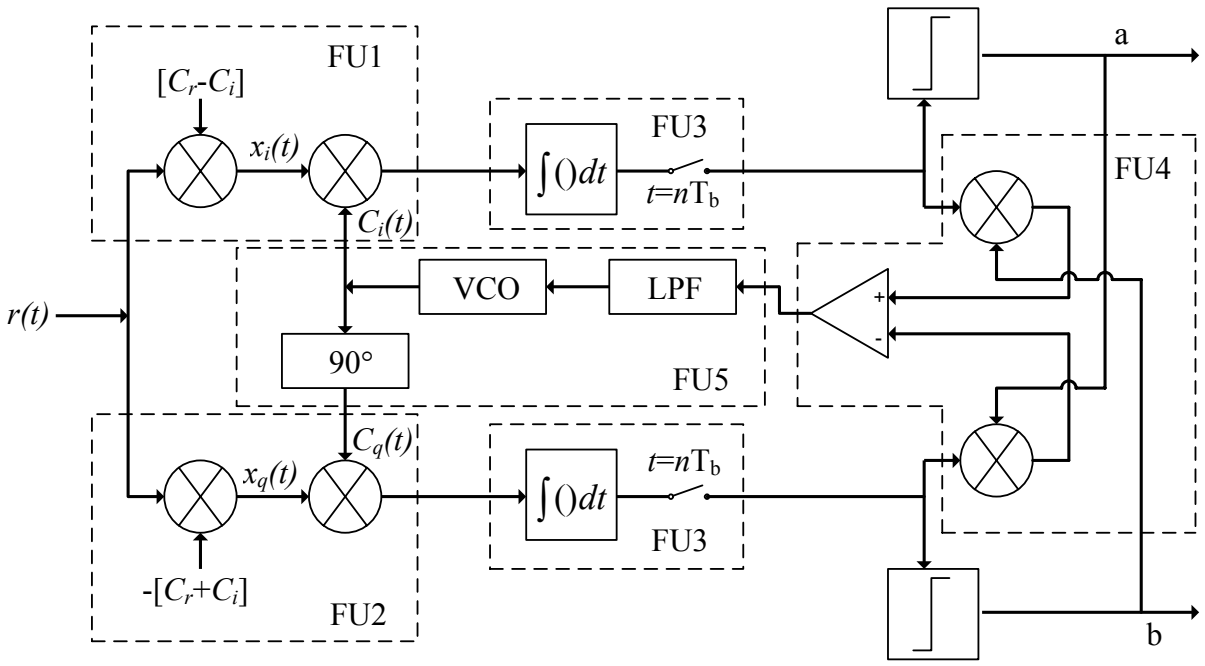


Figure 2.20.
Functional analysis of the DDC-CRL [73].

FU1 performs inphase signal recovery. Similarly, FU2 performs quadrature signal recovery. Both these functional units operate in the same way but use a different set or combination of spreading sequences. Spreading at the transmitter is performed by multiplying each bit with an appropriate spreading sequence, and despreading is performed in the same manner. Modulation at the transmitter is performed by multiplying the desired signal by a carrier at the desired frequency. Demodulation is performed in the same way, provided that the carrier frequency is at the same frequency as the received signal.

Analogue multiplication is performed using mixers. Mixers in CMOS can be implemented as current controlled current sources. Gilbert mixers [25] are most suited for the demodulation and despreading operations that need to be performed. Gilbert mixers have good linearity across their range of operation and a single design is suitable for both high and low frequency operation. Differential inputs and outputs allow Gilbert mixers to be cascaded with ease, and without any need for buffering between mixers.

Demodulation produces a term at twice the carrier frequency as well as at baseband. The double carrier frequency term must be removed since it can be seen as high frequency noise in the time domain. The high frequency terms complicate bit detection by being seen as noise spikes by the bit detector (a simple comparator), causing the bit detector to output

a series of pulses or even an incorrect value. The integrate and dump operation performed by FU3 removes the unwanted high frequency terms and also produces a distinct triangular wave that allows for easy bit detection without errors. Figure 2.21 demonstrates this operation.

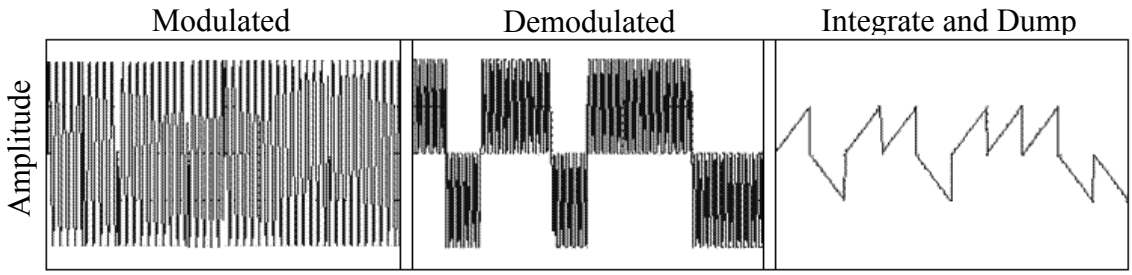


Figure 2.21.

Demodulation of a signal to illustrate the integrate and dump operation. The modulation scheme used is binary phase shift keying (BPSK).

Integration in CMOS can be performed using either inverting or non-inverting active integrators. Passive integrators offer no gain and were not considered. An integrate and dump operation is performed by rapidly discharging the capacitor used in the integrator at the end of every bit interval.

FU4 is the recovered signal comparison unit. The unit consists of a phase comparator which produces an error signal if a phase difference is detected between the two branches of the DDC-CRL. Multipliers generate an error signal based on phase difference between the two branches. Inputs to the multipliers are taken from before bit detection and after bit detection. The difference of the products generates a positive or negative error signal.

The magnitude of this error signal is proportional to the degree of phase or frequency error compared to the local reference. The sign of the error signal indicates whether the difference is positive or negative and is determined by the phase difference between branches. The phase detector can either be digital or analogue. A digital solution makes use of exclusive OR (XOR) gates and generates a square wave where the duty cycle is a function of the phase and frequency. Analogue mixers can again be used for the multiply operation required, but the digital nature of both of the input signals (from the comparators) allows for simpler multipliers to be used.

FU5 generates the carrier reference required to ensure that the carrier used to demodulate the input signal is at the same frequency as the carrier of the input. The error signal produced by the phase detector of FU4 is passed through a low pass filter to remove the AC component and pass the DC component. The filtered error signal is then passed onto a voltage controller oscillator (VCO). The VCO oscillates at a free running frequency that can increase or decrease based on the magnitude and sign of the filtered error signal.

VCOs can be implemented by changing the resonance frequency of a LC tank. Using a varactor (variable capacitor effect) to either replace the capacitor in the tank or to vary the load capacitance seen by the tank is a simple and effective technique to implement a VCO. The 90° phase shift can be implemented in one of three ways. The first is to use an all pass filter with an approximate 90° phase shift in the region of 2.4 GHz. The second is to use Havens technique [25]. The third technique is to design a VCO with quadrature outputs.

In summary, if the phase detector detects a change in phase or frequency an error signal is passed to the VCO, which will increase or decrease the frequency at which it is oscillating. In this way, a change in frequency at the input of the DDC-CRL propagates through both branches to the phase detector. The VCO then compensates for this change.

2.3 Developing the system specifications

2.3.1. System inputs

Figure 2.17 shows the overall inputs and outputs of the system. The inputs to the system consist of the data signal inputs and the sequence inputs. The primary input to the transmitter (FU1) is a binary data signal running at a bit rate proportional to the RF transmission bandwidth divided by the CSS length. The secondary input to the transmitter (FU1) is a CSS of the chosen length. In order to transmit data at a high rate the sequence length should be as small as possible, but in order to keep the quality of the transmission the sequence should not be shorter than a certain length. The sequence length of 11 is used as the lower boundary to satisfy both conditions. The CSS used are the families of the GCL sequences. These sequences are the intellectual property of the University of Pretoria [8].

The primary input to the receiver is the noise corrupted transmitted signal (FU4) running at the rate of 20 Mchips/s, which corresponds to the bandwidth of 20 MHz. Complex spreading sequences form the secondary input to the receiver at FU5.

2.3.2 System outputs

As shown in Figure 2.17, the receiver and transmitter have one output each. The transmitter output (FU3) is an amplified signal with the spread spectrum running at the chip rate specified above. The receiver output (FU7) is a recovered data signal of the same characteristics as those of the transmitter input.

2.3.3 Major subsystem specifications

The subsystems involved are shown in Figures 2.17, 2.19, and 2.20.

The system of Figure 2.17 uses spread Q^2PSK as the modulation scheme (i.e. FU2 and FU6, in Figures 2.13 and 2.16, respectively). As discussed previously, this scheme accommodates a data rate four times higher than in the case of the conventional BPSK and is sufficient to carry all the required information.

The following is the list of additional specifications (referring to Figure 2.17).

- Eight samples per chip are used as this is sufficient for sequence processing.
- The resulting sampling frequency is 160 Msamples/s. This figure is equal to the chip rate times the number of samples.
- The transmitter power is chosen as 17.5 dBm (FU3). This is a typical figure for DSSS transmitters.
- Receiver sensitivity of less than -91 dBm is chosen (FU4). This is also a typical figure.
- The chosen bit-error rate (BER) of the system is less than 10^{-3} (FU4). With this BER, simple error-correction techniques will be sufficient for the improvement of this figure to less than 10^{-6}.
- Integration and dump filtering is necessary for the quality filtering in FU7.

The specifications of the CDLL shown in Figure 2.19 are listed below.

- The received signal in FU1 must have maximum peak amplitude of magnitude 3.3 V as prescribed by the AMS process [15].
- The difference despreading sequences used by FU1.1 and FU1.2 are from the family of generalised chirp like (GCL) sequences.
- To ensure minimal interference between channels, the internal bandwidth of FU1.1 and FU1.2 is restricted to 20 MHz [26].
- The modulation scheme employed in FU2 and FU4 is Q^2PSK.

- FU3 eliminates higher-order and even harmonics from the despreaded demodulated signal.
- Analogue summation takes place in FU5.
- The recovered synchronized data provided by FU6 must have at most, a peak amplitude of 3.3 V as prescribed by the CMOS process.
- The recovered CSS which are output from FU6 should have the following two properties, a mean time to lose lock (MTLL) of at least 1 µs which is a general DLL specification, and a root mean square (rms) tracking jitter of at most 500 ps.
- The data must run at a chip rate of 5 Mchips/s since B_{spread} = 5 MHz [12].
- The sampling rate is determined by the specifications chosen above and by calculation f_{sample} is found to be 160 Msamples/s [11].
- The number of samples/chip is determined by the specifications chosen above and by calculation S is found to be 8 samples/chip which is sufficient for digital processing.
- The transmission bandwidth must be 10/12.5 MHz double side band (DSB) and 5/6.25 MHz single side band (SSB) [12].

The specifications of the DDC-CRL shown in Figure 2.20 are listed below. Specifications were chosen with reference to the IEEE 802.11 standard.

- The CSS used by FU1 and FU2 are from the family of generalised chirp like (GCL) sequences with selectable length.
- The band of operation of FU1 and FU2 should accommodate typical channel widths specified by the IEEE 802.11 standard. The IEEE 802.11 standard has numerous channels of width 5 MHz assigned within its bands of operation, thus a system based on this standard cannot assign more than 20 MHz of bandwidth to a channel. For this reason the internal CMOS operational bandwidth of the DDC-CRL is restricted to 20 MHz. Another benefit of this bandwidth selection is that it prevents the DDC-CRL from acting on adjacent channels.
- The carrier reference generated by FU5 must be able to vary across the range of the channel width to offer a large tracking range, thus has a limit of ± 10 MHz around the centre frequency of operation to prevent the reference frequency from drifting into adjacent bands.
- The centre frequency of operation of the system (FU1, FU2 and FU5) must be in the range of 2.4 GHz to 2.4835 GHz, which is one of the industrial, scientific and medical (ISM) bands specified by the IEEE 802.11 standard [27].

- The BER of the output at a bit rate of 1 Mbps should be no more than 10^{-3}. The BER can be improved by using error correcting codes [23]. However, such codes are considered to be outside the scope of this thesis.
- The maximum bit rate is dependent on the length of the CSS used and the modulation scheme employed, both of which are selectable. The maximum spreading channel width of 5 MHz also limits the bit rate.

2.4 System level simulation

2.4.1 BPSK based system modelling and simulation

SIMULINK was used to model the system to gain a better understanding of the operation of a DSSS transceiver. The total mathematical system diagram is shown in Figure 2.22. The diagram indicates the positioning of the transmitter and receiver in an ideal DSSS system.

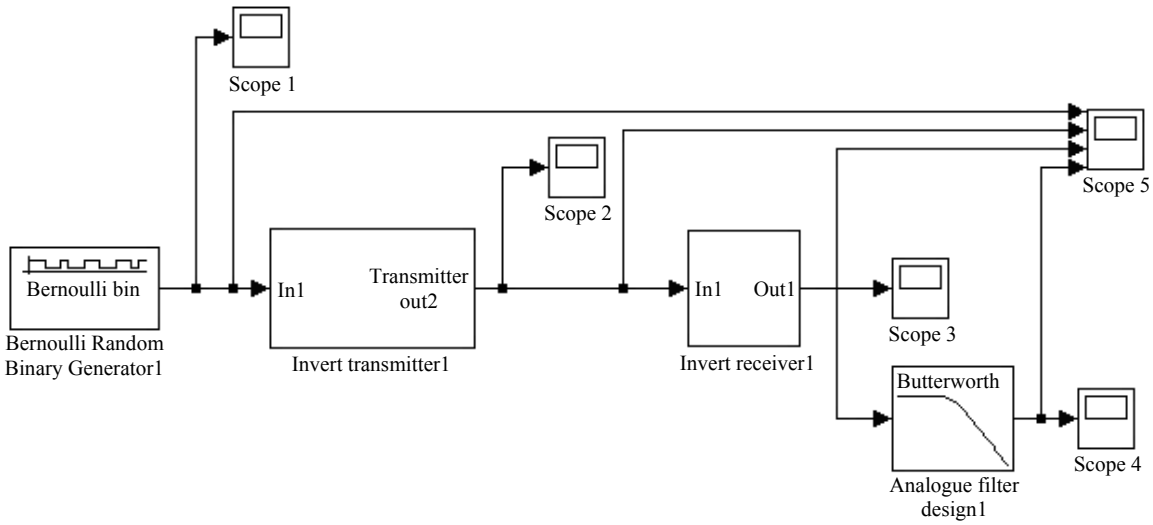


Figure 2.22.
System diagram indicating transmitter and receiver modules.

The system input is shown in Figure 2.23, and the system output is shown in Figure 2.24. By zooming into the Figures 2.23 and 2.24, as expected (Section 2.2.1), the output is a delayed version of the input (delayed by one chip).

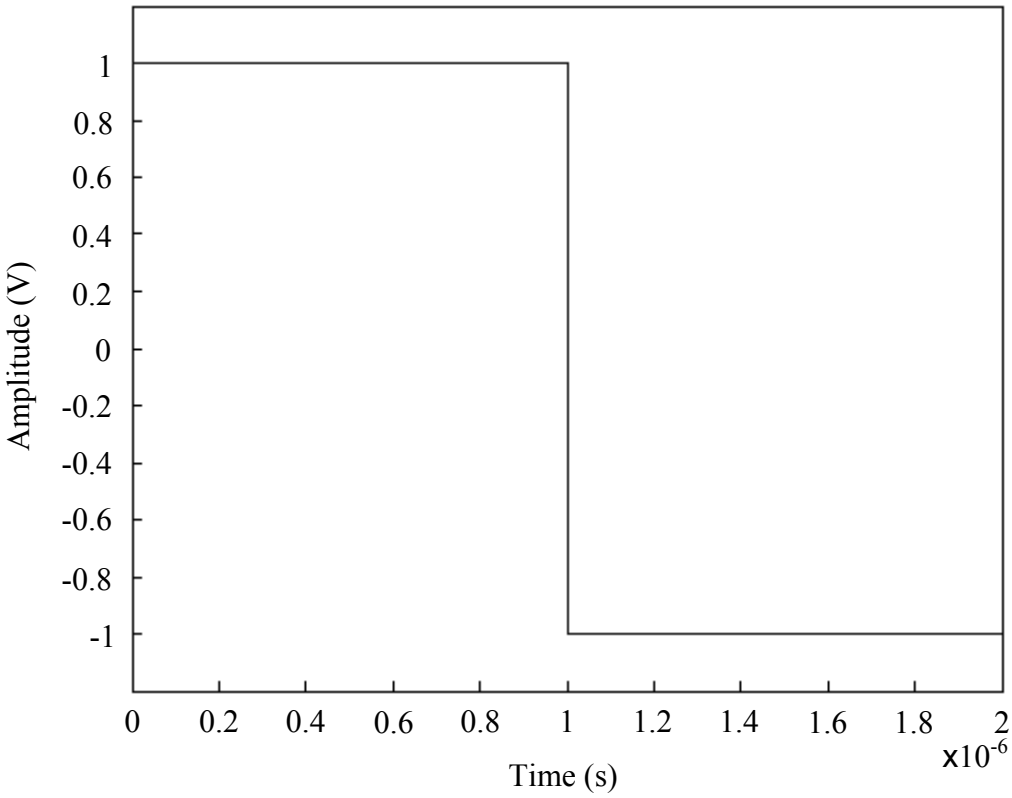


Figure 2.23.

Mathematical system input signal.

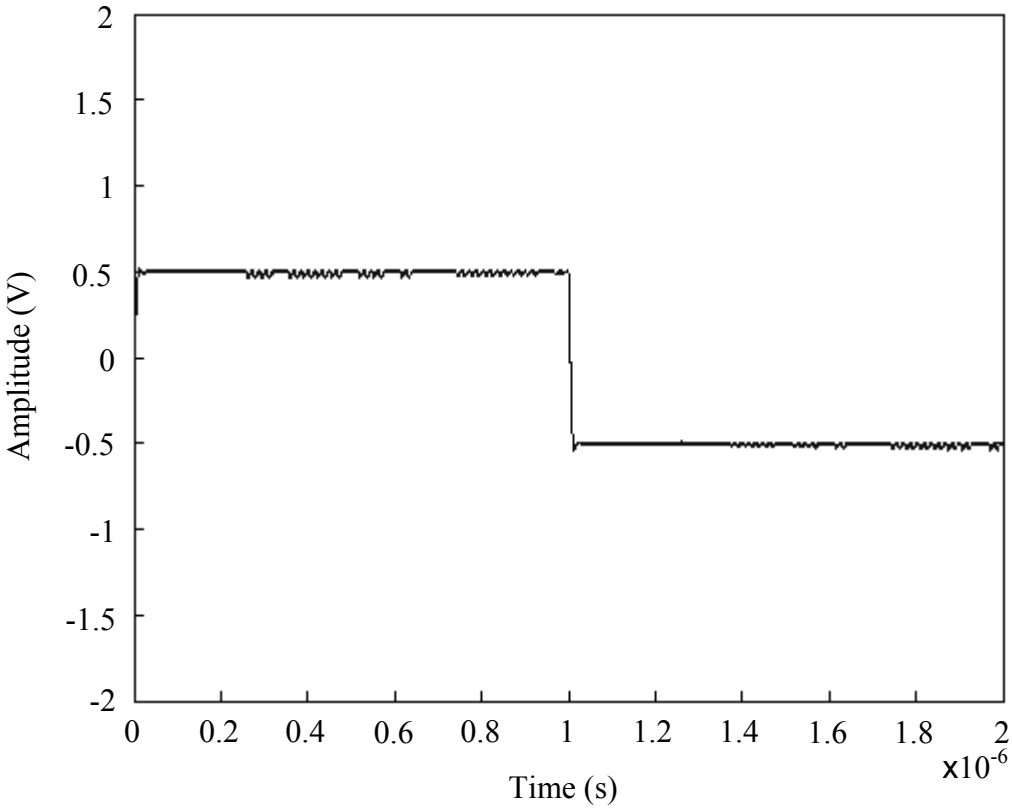


Figure 2.24.

Mathematical system output signal. A delay of 32 ns corresponds to one chip.

Figure 2.25 shows the mathematical transmitter module.

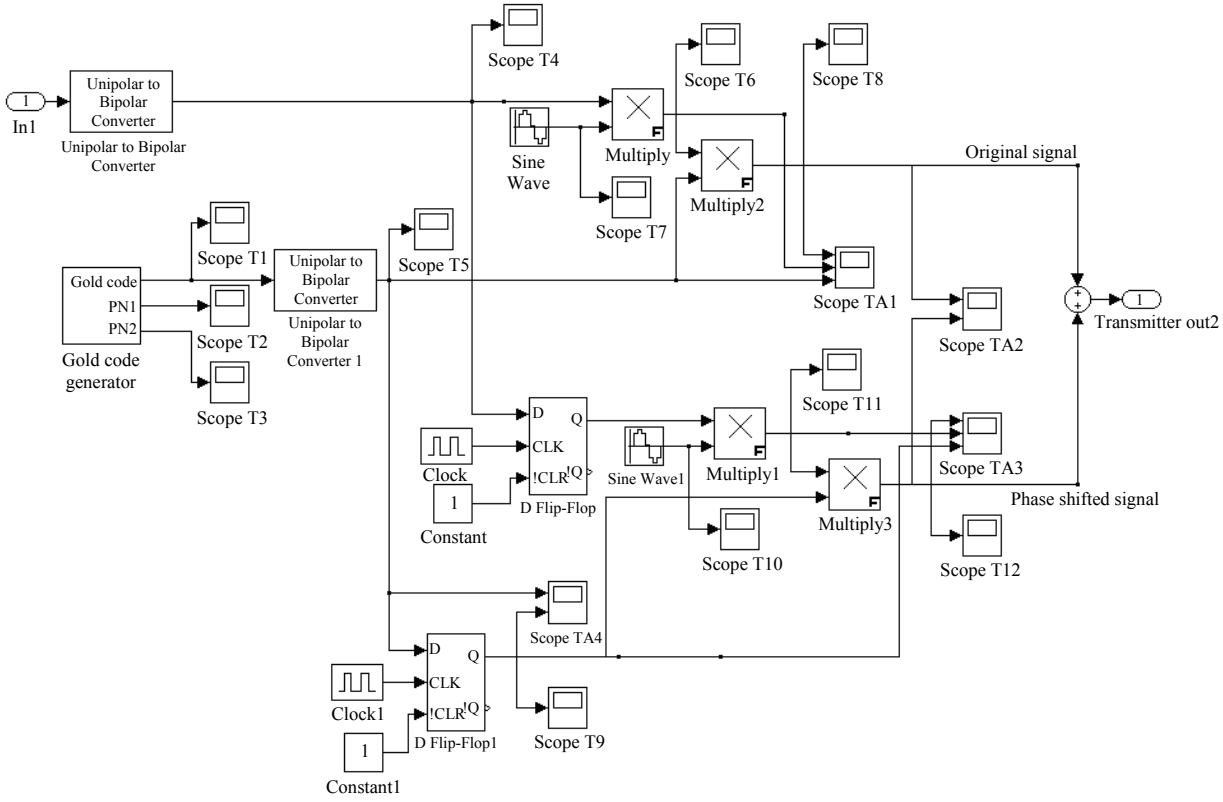


Figure 2.25.

Detailed system diagram for the transmitter.

The PN sequence outputs are shown in the Figures 2.26 and 2.27, respectively. These are then XOR'ed to produce a Gold sequence as shown in Figure 2.28.

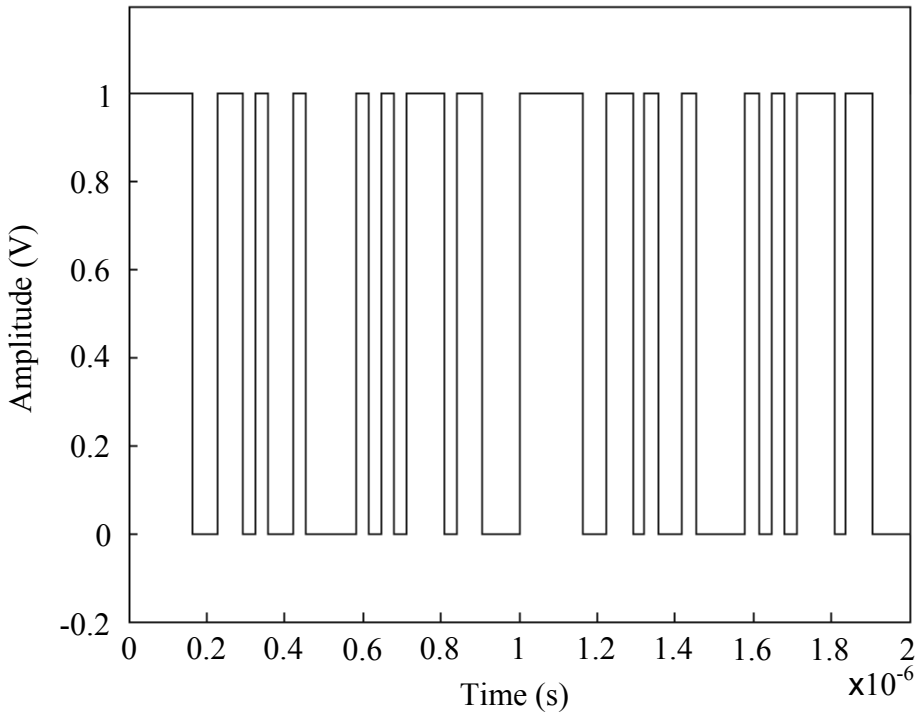


Figure 2.26.

PN sequence A output.

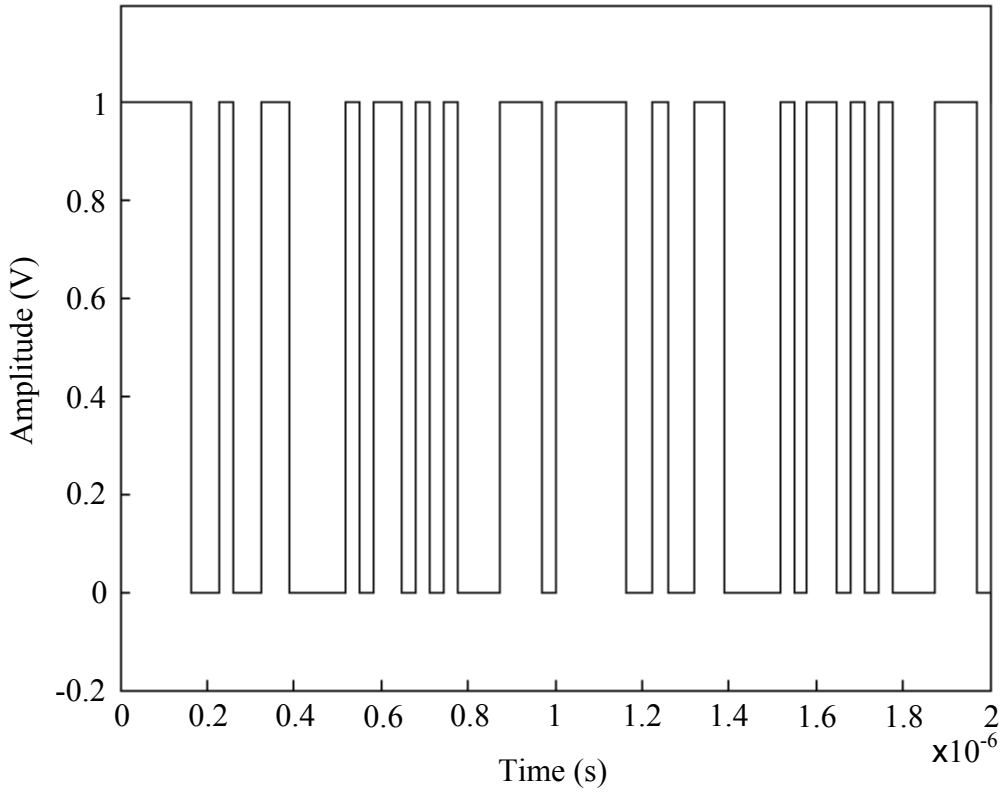


Figure 2.27.

PN sequence B output.

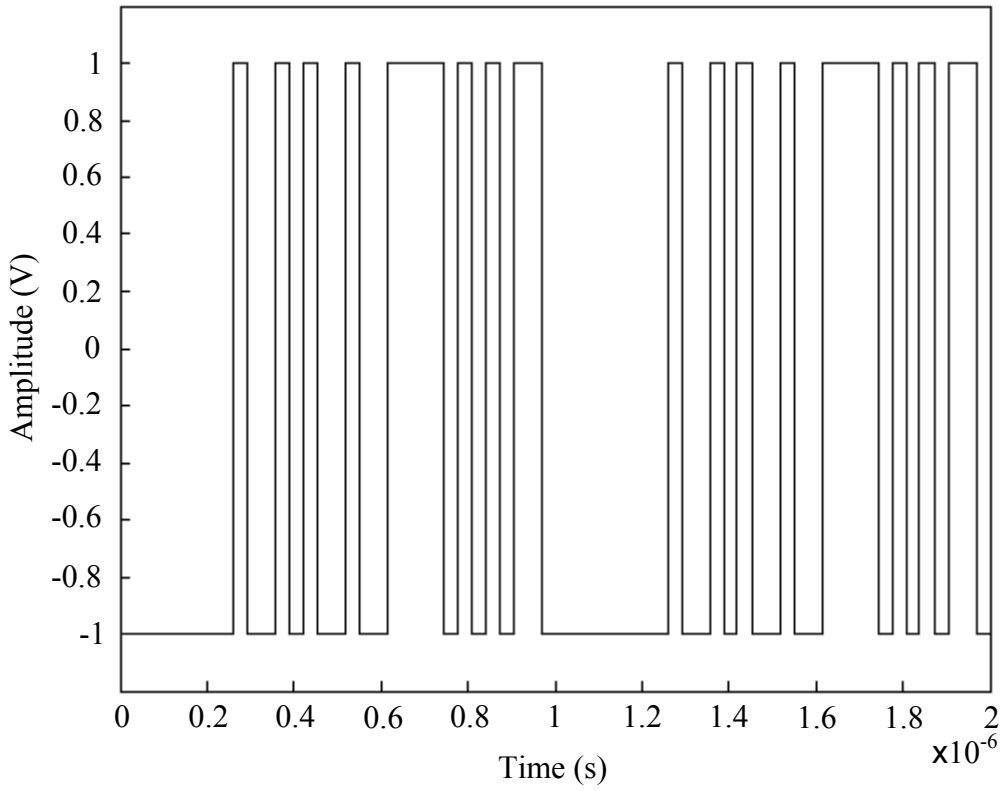


Figure 2.28.

XOR of PN sequence A output with PN sequence B output to form a Gold code.

This signal is then XOR'd (essentially multiplied) with the RF modulated data signal which is shown in Figure 2.29. The 180 phase shift at the bit change can be seen.

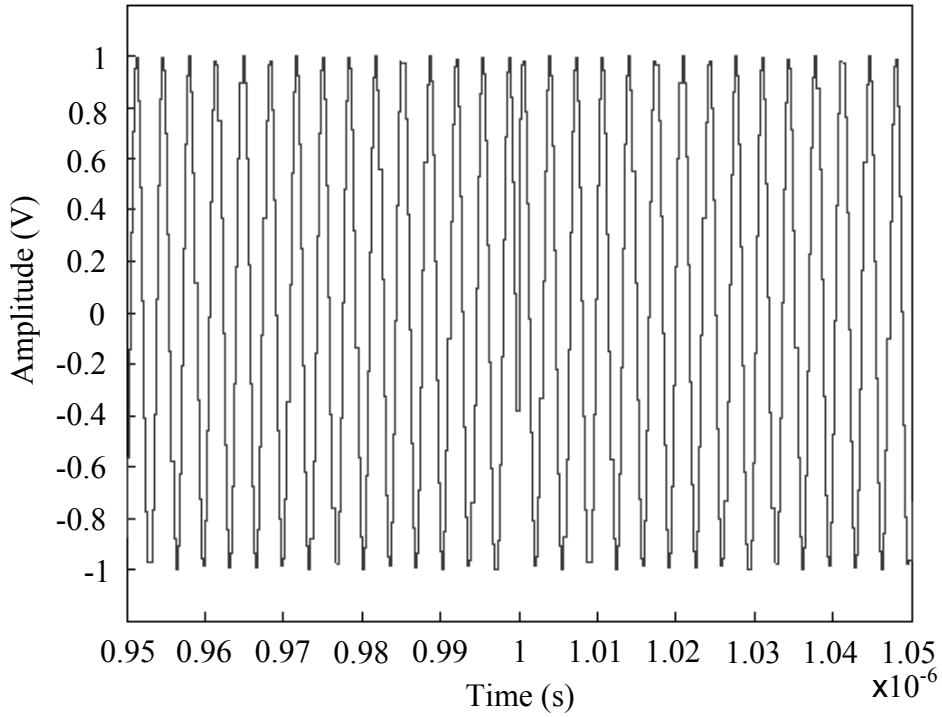


Figure 2.29.

Modulated data signal (1.85125 GHz).

The result of XORing the signal in Figure 2.28 with the Gold sequence can be seen in Figure 2.30.

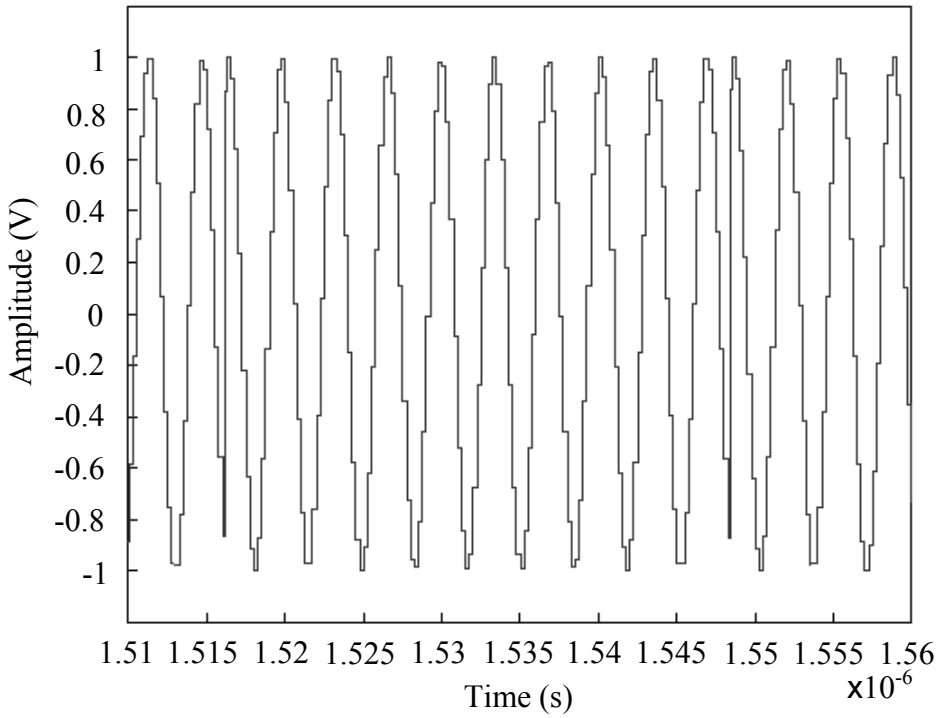


Figure 2.30.

Spreaded data signal.

Inphase and quadrature versions of both the LO and the Gold code are mathematically generated. These are then treated in a similar manner, in order to obtain inphase and quadrature components of this signal. The two similarly spreaded signals are then summed to produce a transmitter output signal at a single frequency. This signal is shown in Figure 2.31.

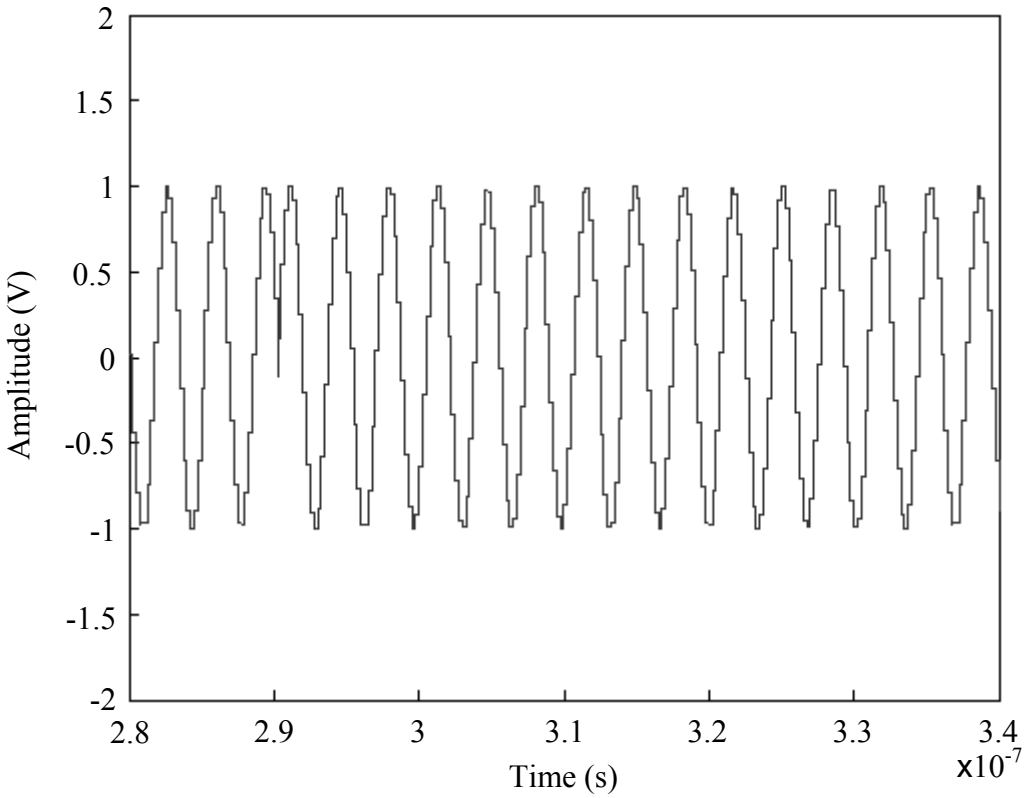


Figure 2.31.

A portion of the mathematical system transmission signal.

Figure 2.32 shows the mathematical model of the receiver module. The original signal is recovered after despreading and demodulation.

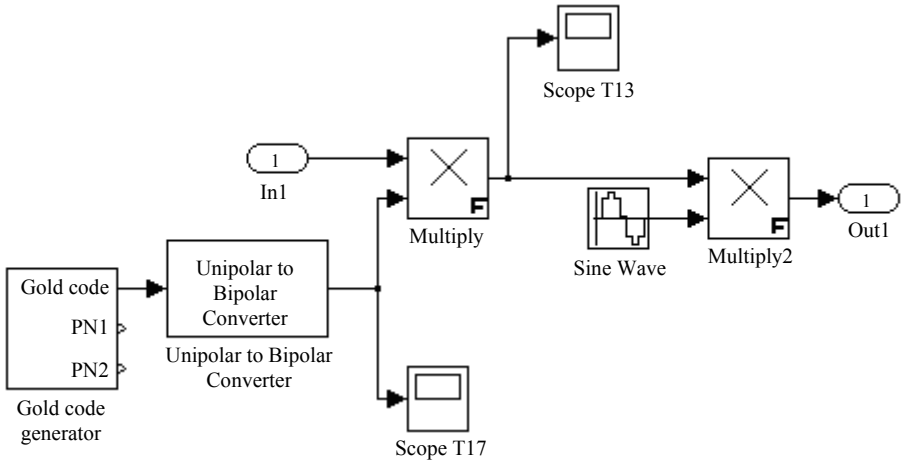


Figure 2.32.

Detailed system diagram for the receiver.

Figure 2.33 shows the signal that is generated when multiplying the Gold code with the received signal. This is also termed the despreaded signal.

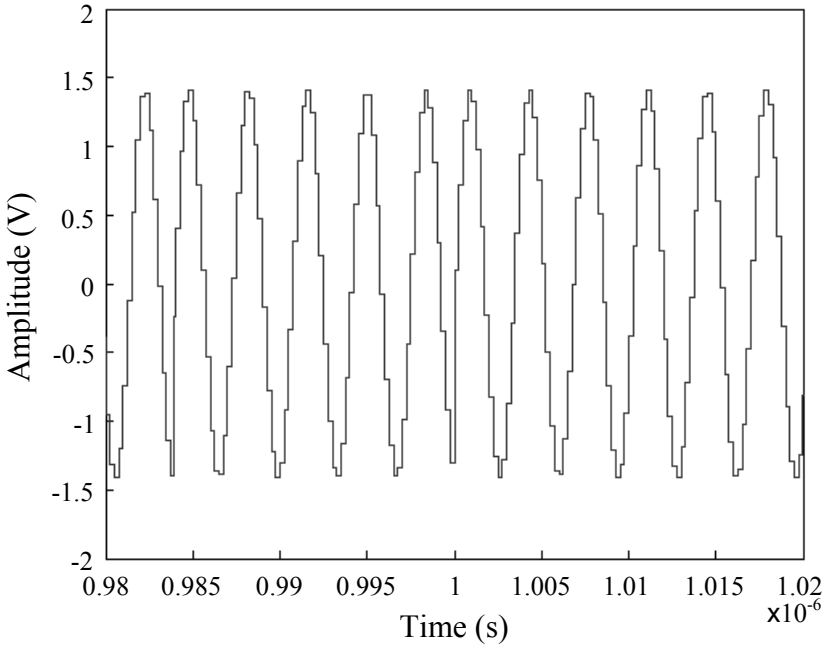


Figure 2.33.

Despreaded signal.

The despreaded signal of Figure 2.33 is then demodulated using the same carrier frequency as that which was used at the transmitter (for a test case, 1.85125 GHz is used). The resulting signal is shown in Figure 2.34. This signal should resemble the data signal, but has a high frequency component that must still be filtered out.

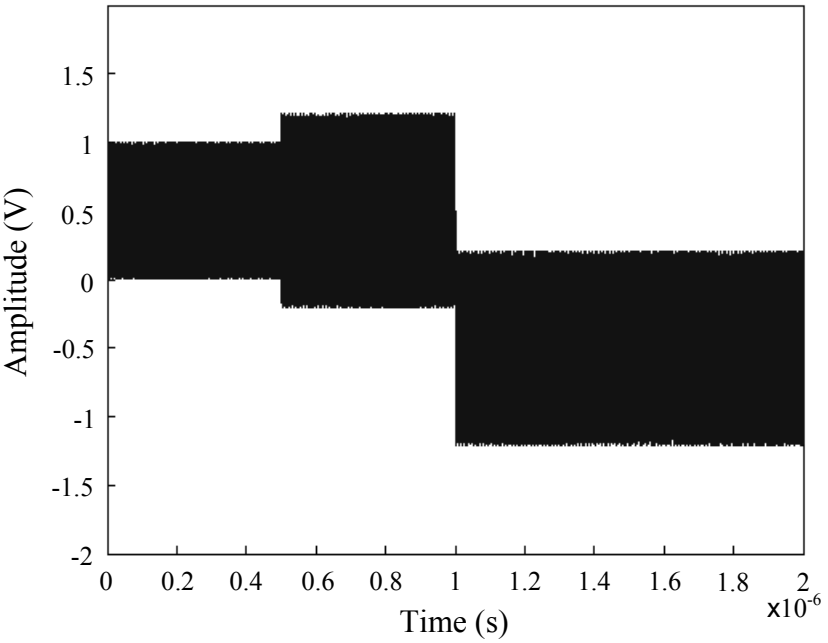


Figure 2.34.

Recovered, unfiltered signal.

This signal was then filtered using an ideal Butterworth filter. The filtered signal was shown previously in Figure 2.24, and thus it is clear that the recovered output signal resembles the original input signal (Figure 2.23).

2.4.2 Q^{2}PSK based system modelling and simulation

The operation of this system can be summarized by

$$u(t) = a(t)C_r \cos\omega_c t + a(t)C_i \cos\omega_c t + a(t)C_r \sin\omega_c t + a(t)C_i \sin\omega_c t \quad (2.17)$$

$$u(t) = a_1(t)C_r \cos\omega_c t + a_2(t)C_i \cos\omega_c t + a_3(t)C_r \sin\omega_c t + a_4(t)C_i \sin\omega_c t \quad (2.18)$$

These two equations are valid for the transmitter if it operates in balanced and unbalanced mode, respectively. $u(t)$ is the transmitted signal, $a(t)$ is the digital data with NRZ logic levels, and ω_c is the carrier frequency. These equations can be expanded to suit the receiver. The following slightly more complicated equations result and they show how each bit can be recovered from the transmitted signal:

$$a_1(t) = \begin{cases} 1,\ T_b < t < 2T_b \text{ iff } \left\{ \int_0^{T_b} \left[u(t)C_r \cos\omega_c t \otimes \Im^{-1}\prod\left(\frac{f}{BW}\right)\right] dt \right\}\Big|_{T_b} > 0 \\ -1, T_b < t < 2T_b, \text{ otherwise} \end{cases} \quad (2.19)$$

$$a_2(t) = \begin{cases} 1,\ T_b < t < 2T_b \text{ iff } \left\{ \int_0^{T_b} \left[u(t)C_i \cos\omega_c t \otimes \Im^{-1}\prod\left(\frac{f}{BW}\right)\right] dt \right\}\Big|_{T_b} > 0 \\ -1, T_b < t < 2T_b, \text{ otherwise} \end{cases} \quad (2.20)$$

$$a_2(t) = \begin{cases} 1,\ T_b < t < 2T_b \text{ iff } \left\{ \int_0^{T_b} \left[u(t)C_r \sin\omega_c t \otimes \Im^{-1}\prod\left(\frac{f}{BW}\right)\right] dt \right\}\Big|_{T_b} > 0 \\ -1, T_b < t < 2T_b, \text{ otherwise} \end{cases} \quad (2.21)$$

$$a_3(t) = \begin{cases} 1,\ T_b < t < 2T_b \text{ iff } \left\{ \int_0^{T_b} \left[u(t)C_i \sin\omega_c t \otimes \Im^{-1}\prod\left(\frac{f}{BW}\right)\right] dt \right\}\Big|_{T_b} > 0 \\ -1, T_b < t < 2T_b, \text{ otherwise} \end{cases} \quad (2.22)$$

where BW is transmission bandwidth. Equations (2.19) to (2.22) hold for the unbalanced configuration, while for the balanced configuration it is to be expected that $a(t) = a_1(t) = a_2(t) = a_3(t) = a_4(t)$.

The implementation of a DSSS transceiver system essentially scales down to implementing the following mathematical equations:

$$u(t) = a(t)C_r \cos\omega_c t + a(t)C_i \cos\omega_c t + a(t)C_r \sin\omega_c t + a(t)C_i \sin\omega_c t\,, \tag{2.23}$$

$$u(t) = a_1(t)C_r \cos\omega_c t + a_2(t)C_i \cos\omega_c t + a_3(t)C_r \sin\omega_c t + a_4(t)C_i \sin\omega_c t\,, \tag{2.24}$$

which are valid for the transmitter, and are slightly more complicated for the receiver, in a manner of the block diagram showed in Figure 2.18. This block diagram is modelled in Simulink. The developed model of the transmitter is shown in Figure 2.35, while the models of the noisy and fading channel [11] as well as the receiver are shown in Figure 2.36 and Figure 2.37, respectively.

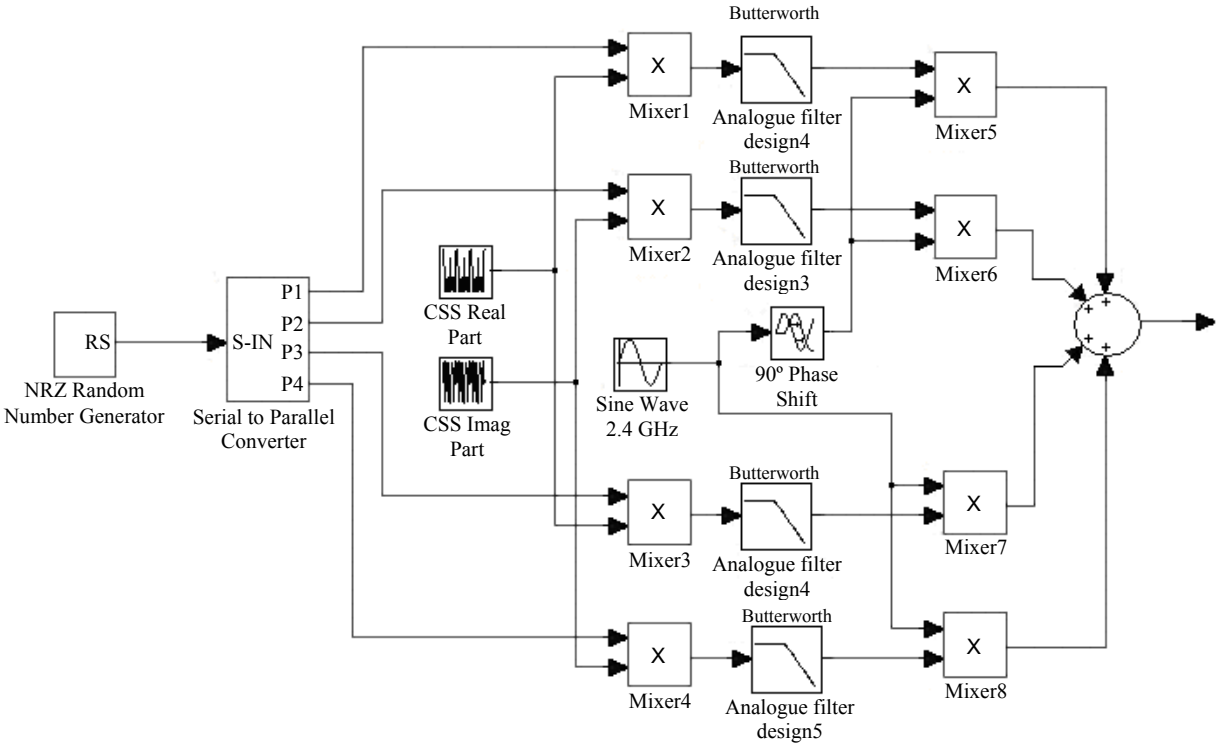


Figure 2.35.

Simulink model of the proposed transmitter.

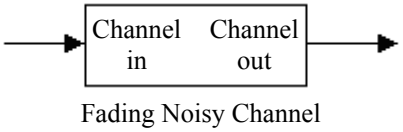


Figure 2.36.

Simulink model of a noisy fading channel.

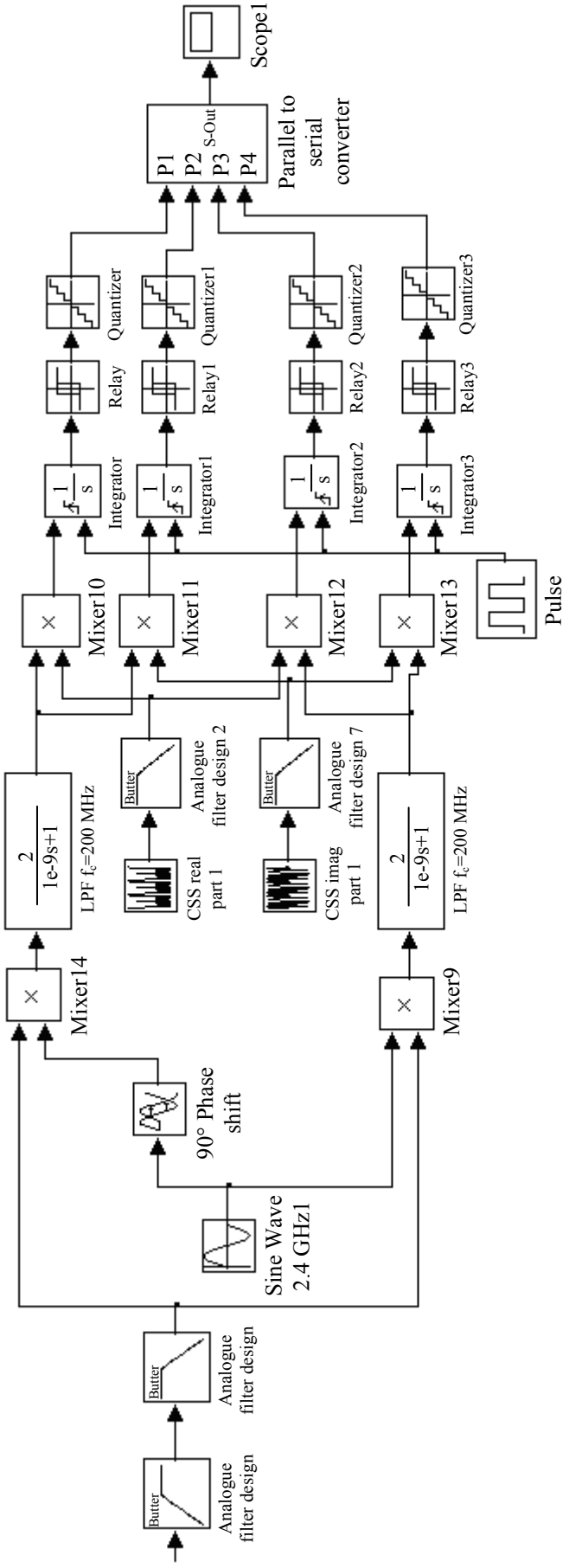


Figure 2.37.

Simulink model of the proposed receiver. CSS real & imaginary parts provided [8].

Simulation results

The shape of the signal after each stage of processing in the transmitter (Figure 2.35) and receiver (Figure 2.36), as well as the shape of the signal after the channel (Figure 2.37) are presented below. Table 2.1 shows specifications of the three signals used for simulation purposes. The simulation is run for 40 bit repetitions (6.5 µs).

Signal	**Parameter**	**Specification**
PRBS data source	Bit length	0.1625 µs
Spreading sequence	Length	13
Spreading sequence	Duration of one repetition	0.65 µs
Spreading sequence	Sampling rate	160 Msamples/s
Clock	Period	0.65 µs

Table 2.1.

Parameters of the test signals that were used to obtain Simulink results for the transceiver.

The results are organised in the following way: The CSS real and imaginary parts are shown in Figure 2.38 and Figure 2.39. The test PRBS data stream is shown in Figure 2.40. Time and, where applicable, frequency domain waveforms after propagation of the signal through the whole system are shown in Figure 2.40 through Figure 2.52, concluding with the final, recovered data signal. In the subsystems where signals are processed in four branches only the simulation of the top branch is given. No gain losses are assumed in simulation.

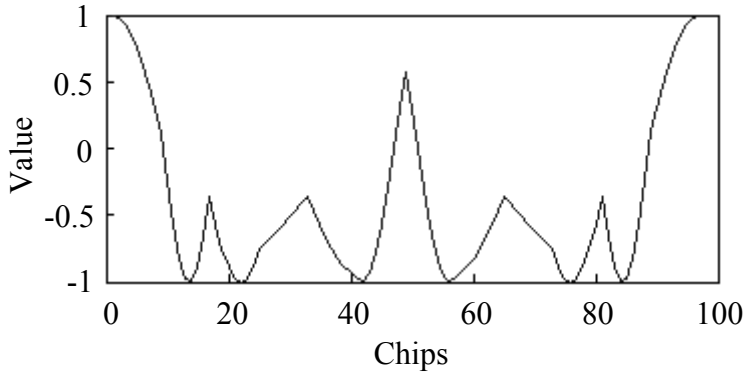


Figure 2.38.

Real part of the sequence of length 13 used in the system.

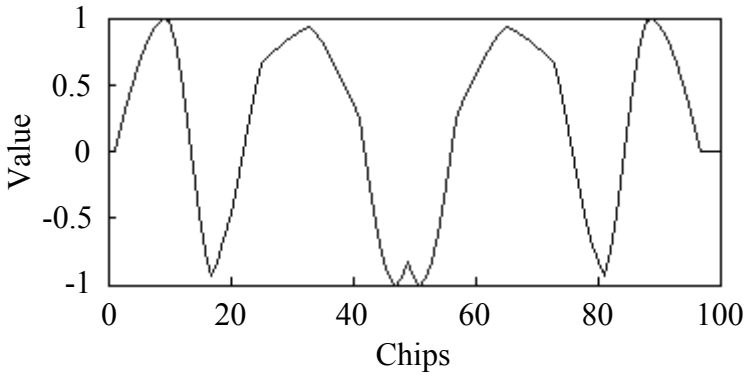


Figure 2.39.

Imaginary part of the sequence of length 13 used in the system.

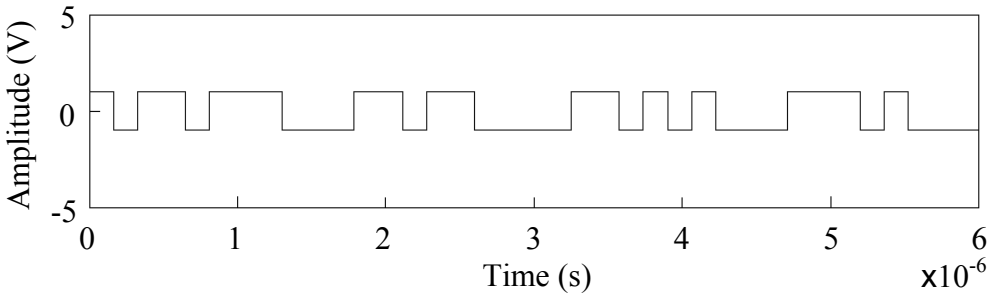


Figure 2.40.

Time-domain simulation trace of the PRBS data stream used at the input of the transmitter.

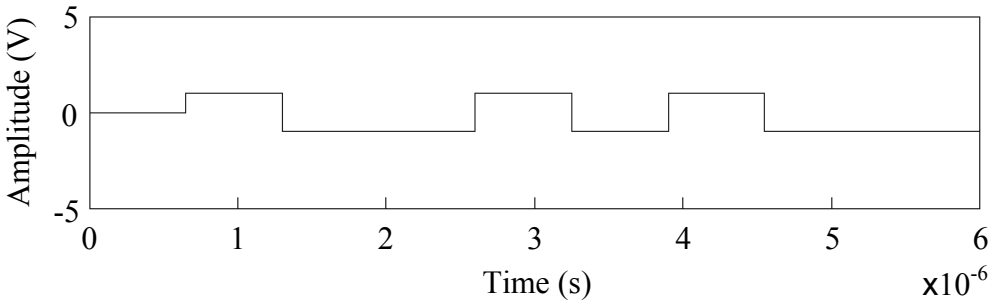


Figure 2.41.

Time-domain simulation trace of the data stream in the top branch of the transmitter after parallel-to-serial conversion.

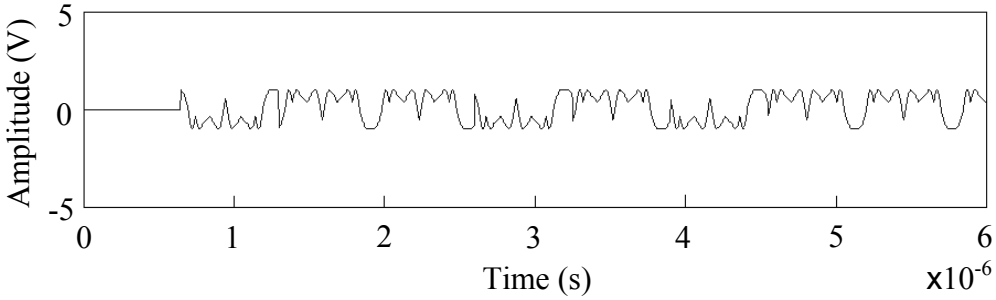


Figure 2.42.

Time-domain simulation trace of the data stream in the top branch of the transmitter after it has been spread with the real part of the CSS.

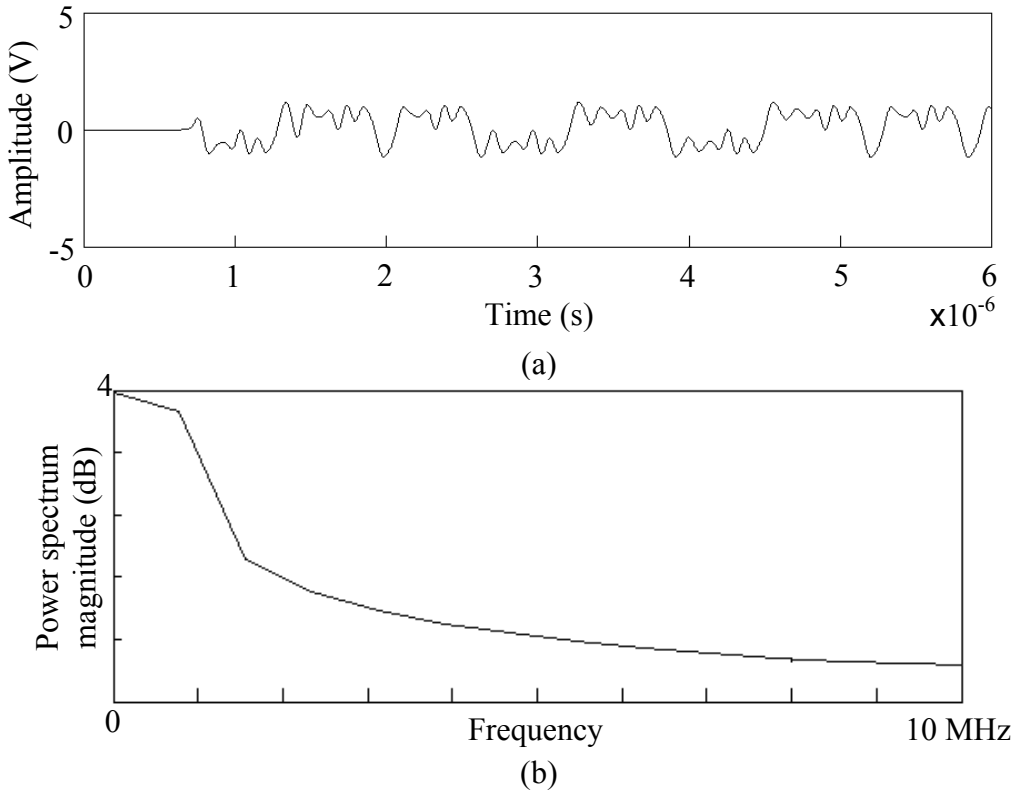


Figure 2.43.

(a) Time-domain and (b) frequency-domain simulation traces of the data stream in the top branch of the transmitter after it has been filtered.

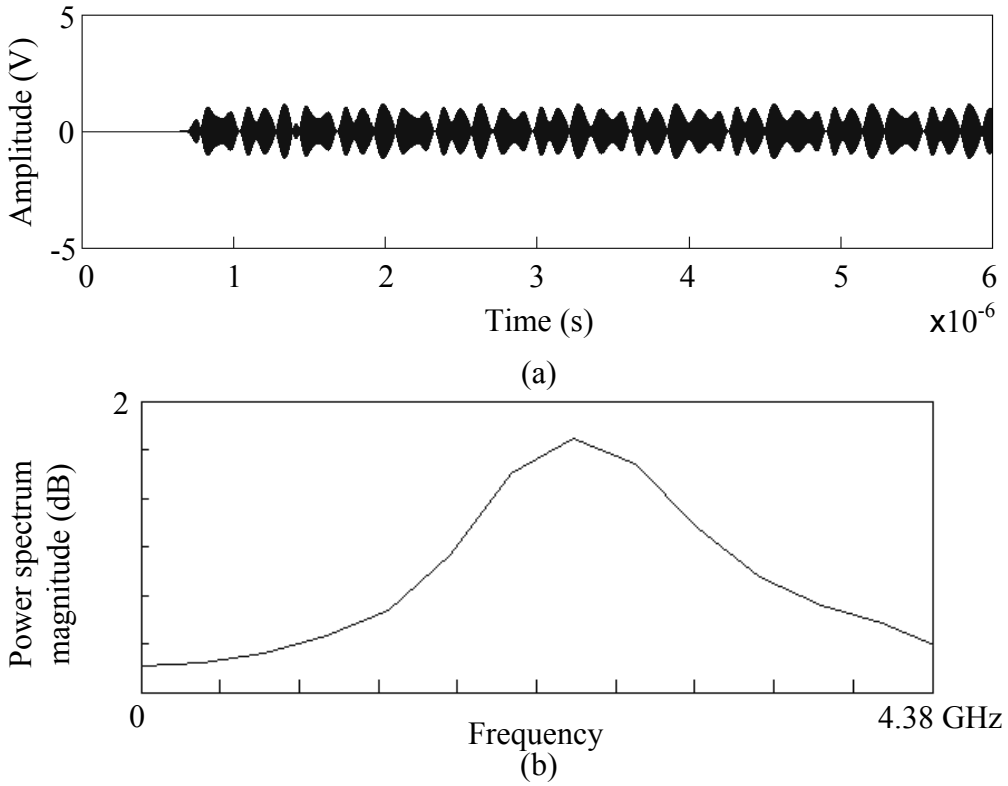


Figure 2.44.

(a) Time-domain and (b) Frequency domain simulation traces of the signal in the top branch of the transmitter after it has been modulated onto a 2.4 GHz carrier.

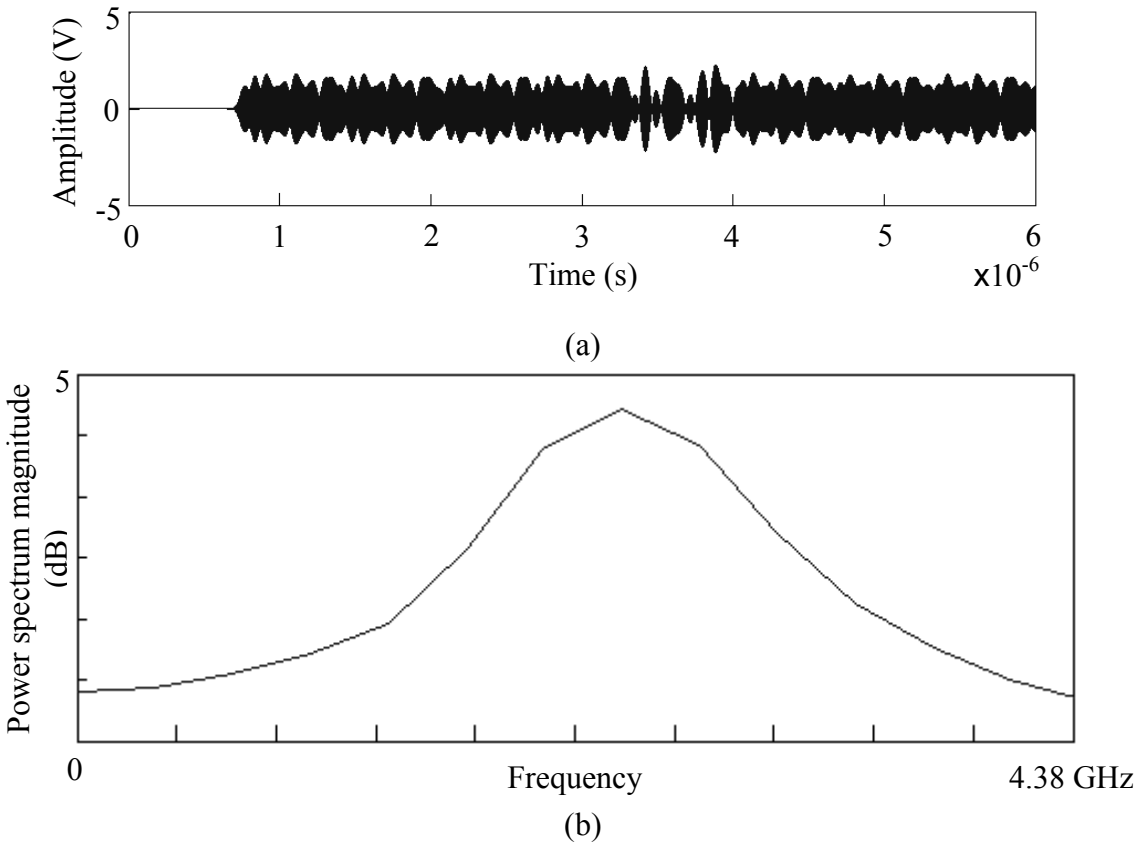


Figure 2.45.

Transmitted signal in (a) time domain and (b) frequency domain.

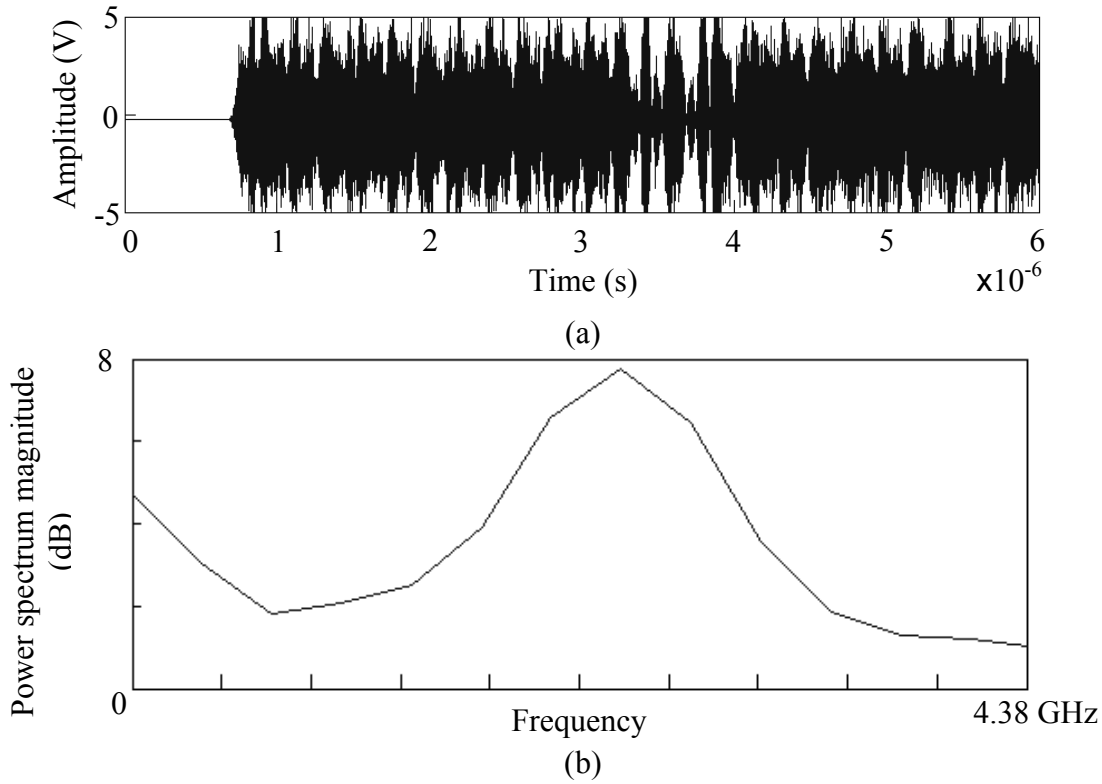


Figure 2.46.

(a) Time-domain and (b) frequency domain simulation traces of the signal after it has been passed through the noisy and fading channel (using MATLAB).

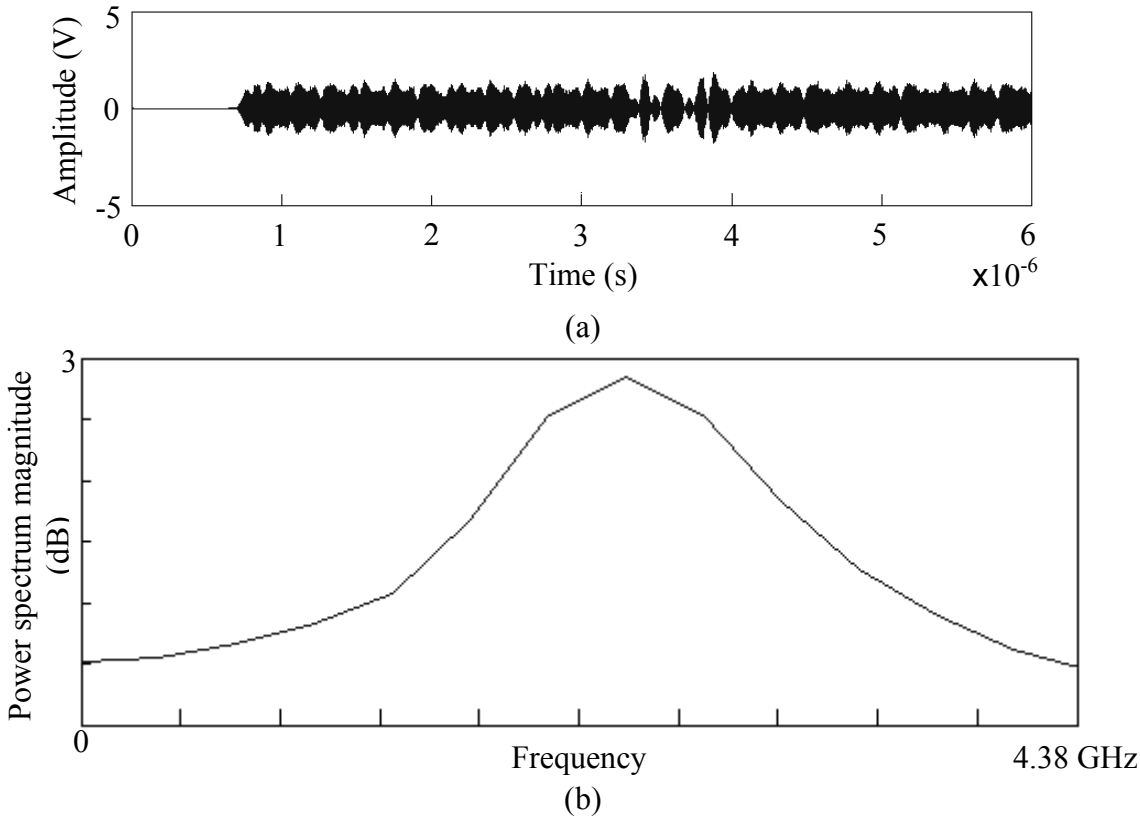


Figure 2.47.

(a) Time-domain and (b) frequency-domain simulation traces of the signal after it has been received.

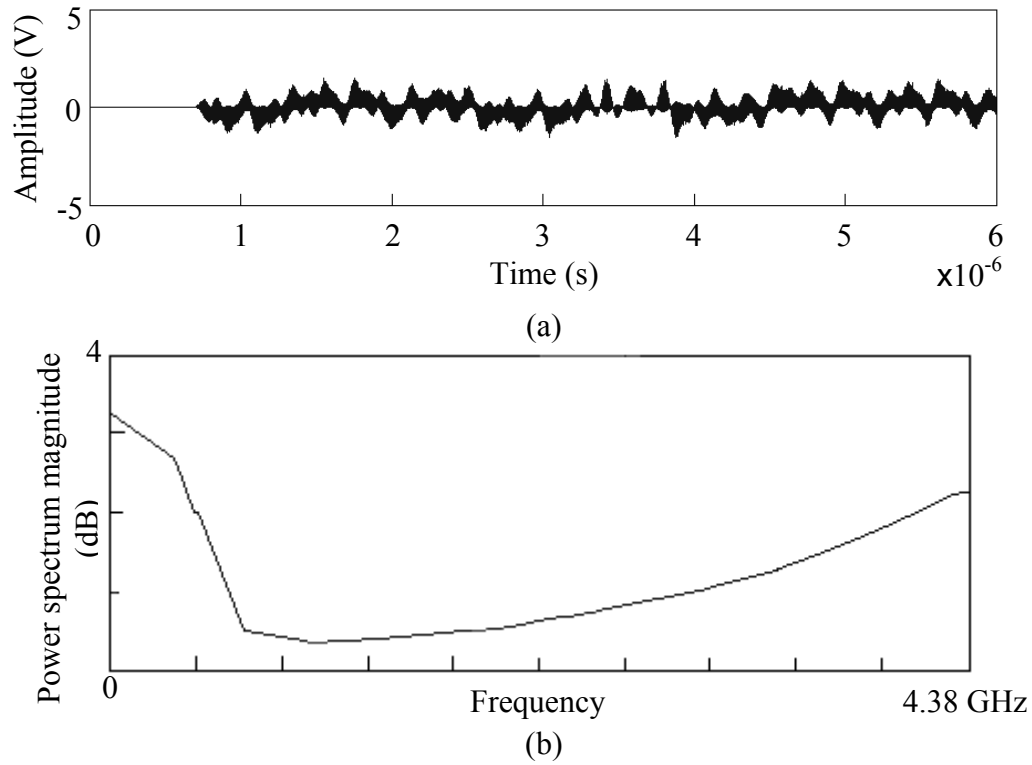
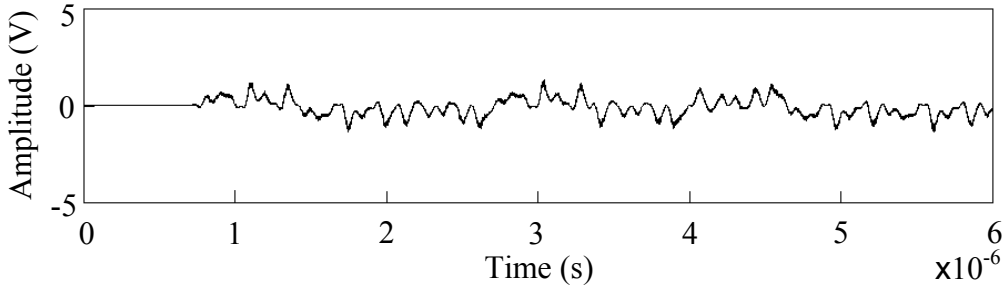
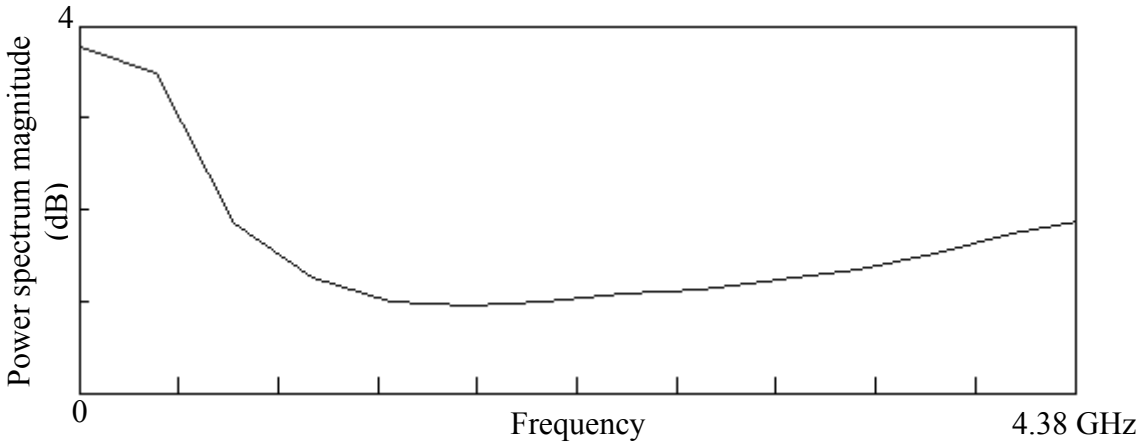


Figure 2.48.

(a) Time-domain and (b) frequency-domain simulation traces of the signal in the top branch of the receiver after demodulation.



(a)



(b)

Figure 2.49.

(a) Time-domain and (b) frequency domain simulation trace of the signal at the top branch of the receiver after despreading.

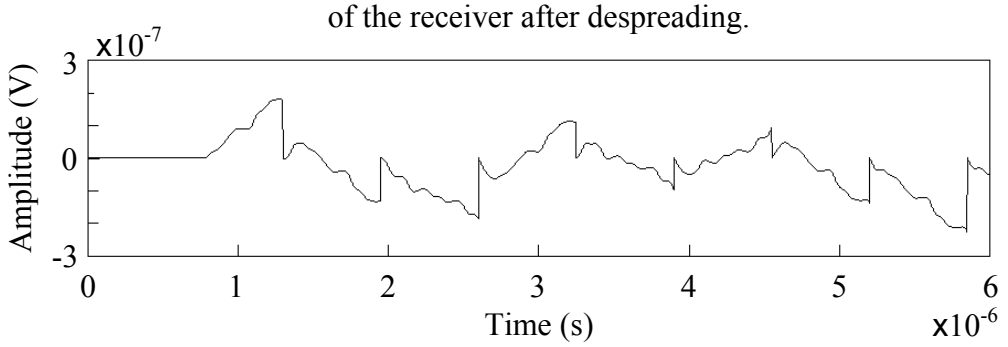


Figure 2.50.

Time-domain simulation trace of the signal in the top branch of the receiver after it has been processed by the integrate and dump subsystem.

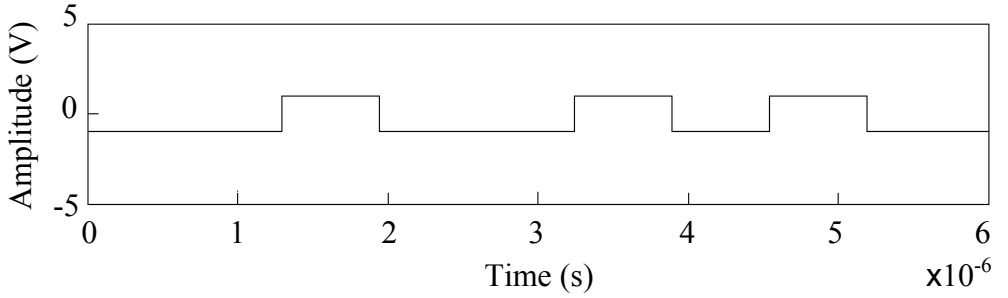


Figure 2.51.

Time-domain simulation trace of the signal after it has been passed through limiting and sampling.

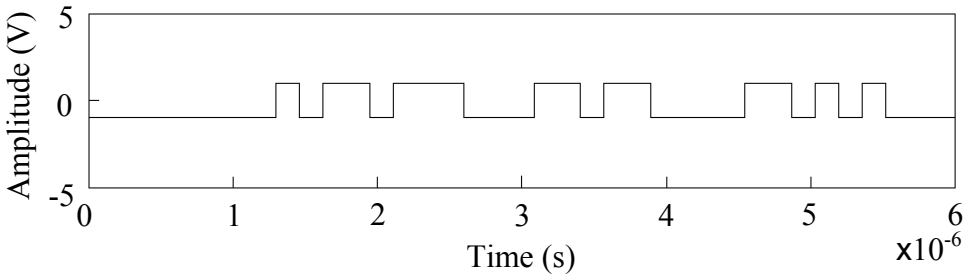


Figure 2.52.

Time-domain simulation trace of the final recovered signal.