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A MULTI-DIMENSIONAL SPREAD SPECTRUM TRANSCEIVER

by

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Submitted in partial fulfilment of the requirements for the degree

Philosophiae Doctor (Electronic Engineering)

in the

Faculty of Engineering, Built Environment & Information Technology

UNIVERSITY OF PRETORIA

October 2008

SUMMARY

A MULTI-DIMENSIONAL SPREAD SPECTRUM TRANSCEIVER BY SAURABH SINHA

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The research conducted for this thesis seeks to understand issues associated with integrating a direct spread spectrum system (DSSS) transceiver on to a single chip. Various types of sequences, such as Kasami sequences and Gold sequences, are available for use in typical spread spectrum systems. For this thesis, complex spreading sequences (CSS) are used for improved cross-correlation and autocorrelation properties that can be achieved by using such a sequence.

While CSS and DSSS are well represented in the existing body of knowledge, and discrete bulky hardware solutions exist – an effort to jointly integrate CSS and DSSS on-chip was identified to be lacking. For this thesis, spread spectrum architecture was implemented focussing on sub-systems that are specific to CSS. This will be the main contribution for this thesis, but the contribution is further appended by various RF design challenges: high-speed requirements make RF circuits sensitive to the effects of parasitics, including parasitic inductance, passive component modelling, as well as signal integrity issues.

The integration is first considered more ideally, using mathematical sub-systems, and then later implemented practically using complementary metal-oxide semiconductor (CMOS) technology. The integration involves mixed-signal and radio frequency (RF) design techniques – and final integration involves several specialized analogue sub-systems, such as a class F power amplifier (PA), a low-noise amplifier (LNA), and LC voltage-controlled oscillators (VCOs). The research also considers various issues related to on-chip inductors, and also considers an active inductor implementation as an option for the VCO. With such an inductor a better quality factor is achievable. While some conventional sub-system design techniques are deployed, several modifications are made to adapt a given sub-system to the design requirements for this thesis. The contribution of the research lies in the circuit level modifications done at sub-system level aimed towards eventual integration. For multiple-access communication systems, where a number of independent users are required to share a common channel, the transceiver proposed in this thesis, can contribute towards improved data rate or bit error rate.

The design is completed for fabrication in a standard 0.35-µm CMOS process with minimal external components. With an active chip area of about 5 mm^2, the simulated transmitter consumes about 250 mW & the receiver consumes about 200 mW.

Keywords: complementary metal-oxide semiconductor (CMOS), spread spectrum (SS), complex spreading sequences (CSS), delay locked loop (DLL), Costa's loop, voltage controlled oscillator (VCO), mixer, on-chip inductors, class F power amplifier (PA).

SAMEVATTING

'N MULTIDIMENSIONELE SPREISPEKTRUM-SENDER-ONTVANGER DEUR SAURABH SINHA

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Die navorsing wat vir hierdie tesis onderneem is, beoog om kundigheid op te bou aangaande die kwessies wat met die integrasie van 'n direkte spreispektrumstelsel (DSSS) sender-ontvanger op 'n enkele skyfie verband hou. Verskeie tipes sekwensies, soos byvoorbeeld Kasami- en Gold-sekwensies, is vir gebruik in tipiese spreispektrumstelsels beskikbaar. Vir hierdie tesis is komplekse spreisekwensies (KSS) gebruik vir verbeterde kruis- en outokorrelasie-eienskappe wat bereik kan word deur so 'n sekwensie te gebruik.

Alhoewel DSSS en KSS reeds welbekend is, en diskrete hardeware oplossings reeds bestaan, is die vraag na gesamentlike geïntegreerde DSSS en KSS op een vlokkie geïdentifiseer. Vir hierdie tesis is spreispektrumargitektuur aangewend met die klem op KSS substelsels. Dit is dan ook die belangrikste bydrae van hierdie tesis, maar die bydrae gaan verder gepaard met verskeie RF-ontwerpuitdagings: hoëspoed-vereistes maak RF-stroombane sensitief vir die uitwerking van parasitiese komponente, met inbegrip van parasitiese induktansie, passiewe komponentmodellering en ook seinintegriteitskwessies.

Die integrasie word eerstens meer idealisties oorweeg deur wiskundige substelsels te gebruik en dan later prakties te implementeer deur komplementêre metaaloksied-halfgeleiertegnologie (CMOS) te gebruik. Die integrasie behels gemengdesein- en radiofrekwensie(RF)-ontwerptegnieke – en finale integrasie behels verskeie gespesialiseerde analoë substelsels soos 'n klas F-kragversterker (KV), 'n laeruis-versterker (LRV), en LC-spanningbeheerde ossileerders (SBO's). Die navorsing oorweeg ook verskeie kwessies in verband met op-skyfie induktors en oorweeg ook 'n aktiewe induktorimplementering as 'n opsie vir die SBO. Met sodanige induktor is 'n beter kwaliteitsfaktor haalbaar. Hoewel enkele konvensionele substelsel-ontwerptegnieke aangewend word, word daar verskeie wysigings aangebring om 'n gegewe substelsel by die ontwerpvereistes vir hierdie tesis aan te pas. Die bydrae van die navorsing is hoofsaaklik die stroombaanmodifikasies wat gedoen is op substelselvlak om integrasie te vergemaklik. Vir veelvoudige-toegang kommunikasiestelsels waar 'n aantal onafhanklike

gebruikers dieselfde seinkanaal moet deel, kan die sender-ontvanger voorgestel in hierdie tesis meewerk om die datatempo en fouttempo te verbeter.

Die ontwerp is voltooi vir vervaardiging in ‘n standaard 0.35-µm CMOS-proses met minimale eksterne komponente. Met ‘n aktiewe skyfie-oppervlakte van ongeveer 5 mm^2, verbruik die gesimuleerde sender ongeveer 250 mW en die ontvanger verbruik ongeveer 200 mW.

Sleutelwoorde: komplementêre metaaloksied-halfgeleier (CMOS), spreispektrum (SS), komplekse spreisekwenssies (KSS), vertragingsluitlus (VSL), Costa se lus, spanningsbeheerde ossilleerder (SBO), menger, op-skyfie induktors, klas F-kragversterker (KV).

ACKNOWLEDGEMENT

The research work of this thesis would not be possible without the kind co-operation and support of many friends, students, and colleagues. I would like to acknowledge and extend my appreciation to all those that have contributed indirectly or directly to the research conducted in this thesis. The following names are worthy of a special mention:

- Prof. Monuko du Plessis for his technical guidance as the research supervisor,
- Prof. Louis Linde for his initiative towards the broader area of research, and serving as the research co-supervisor, and
- Prof. Wilhelm Leuschner for allowing me time (as my boss) to conduct this research.

I would also like to acknowledge the excellent resources (human and financial) provided by the Carl & Emily Fuchs Institute for Microelectronics (CEFIM), University of Pretoria. During the course of this thesis, I have also had the opportunity to serve on several IEEE committees (both at the level of Region 8 and the South Africa Section). Due to the time required for this thesis, I reduced the time that I normally spent as a volunteer, yet received immense support from some IEEE volunteers in our Section, some names that come to thought: Prof. Gerhard Hancke, Prof. Nico Beute, Prof. Tinus Pretorius, Dr Edward Chikuni, and Jacques van Wyk.

I would also like to extend a very special thanks to my RFIC microelectronics research group whose work also contributed to my own academic development; in particular I would like to thank Mladen Božanić, Calvin Coetzee, Simon Ross, Neil Naudé, John Meyer, and Tinu Elenjical.

I would also like to extend my gratitude to my parents (Pramod & Sudha Sinha) and friends for their kind support and understanding as this thesis was concluded. In particular, I would like to acknowledge my close friends, Jaco du Preez and Rina Mostert & colleagues, Jannes Venter, Johan Schoeman, Maryna Bekker, Marí Ferreira, Tilla Loubser, and Prof. Johan Hanekom.

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LIST OF ABBREVIATIONS

AC	Auto-correlation
AMS	austriamicrosystems
BER	Bit error rate
BERT	Bit error ratio test
BJT	Bipolar junction transistor
BPF	Band-pass filter
BPSK	Binary phase-shift keying
BTS	Base transceiver station
BUF	Buffer
CC	Cross-correlation
CDLL	Complex delay lock loop
CDMA	Code division multiple access
CEFIM	Carl and Emily Fuchs Institute for Microelectronics
CLK	Clock
CMOS	Complementary metal-oxide semiconductor
CMRR	Common-mode rejection ratio
CSS	Complex spreading sequences
DA	Differential amplifier
DDC-CRL	Decision directed Costas carrier recovery loop
DRC	Design rule check
DSSS	Direct sequence spread spectrum
FET	Field-effect transistor
FF	Flip-flop
FHSS	Frequency hopping spread spectrum
FM	Frequency modulation
FPGA	Field programmable graphics array
FU	Functional Unit
GCL	Generalized chirp-like
IF	Interface
IR	Infrared
LNA	Low-noise amplifier

LO	Local oscillator
LPF	Low pass filter
LPI	Low probability of intercept
LVS	Layout versus Schematic
MN	Matching network
MS	Mobile station
MTLL	Mean time to lose lock
MUI	Multi-user interference
NDA	Non-disclosure agreement
NF	Noise figure
NIC	Negative impedance converter
NRZ	Non-return-to-zero
P/S	Parallel-to-Serial
PA	Power amplifier
PCB	Printed circuit board
PCM	Pulse code modulation
PD	Phase detector
PN	Pseudonoise
PRBS	Pseudo random binary sequence
PSD	Power spectral density
QPSK	Quadrature phase-shift keying
RMS	Root-mean square
RUF	Root-of-unity filtered
S/P	Serial-to-parallel
SNR	Signal-to-noise ratio
SPICE	Simulation program with integrated circuit emphasis
VCO	Voltage controlled oscillator
VLSI	Very large-scale integration