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AN INTEGRATED CONTINUOUS OUTPUT LINEAR POWER SENSOR USING HALL EFFECT VECTOR MULTIPLICATION

by

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ABSTRACT

Keywords: Hall generator, Hall sensor, Hall voltage, Hall multiplication, Hall effect sensor, magnetic field sensor, magnetoresistance, magnetoconcentration, galvanomagnetic effects, thermomagnetic effects, thermoelectric effects, piezoresistive effects, quadrature rotation, multifinger transistors, chip on board.

A Hall generator inherently functions as a multiplier in that it yields a Hall voltage representing the cross product of the bias current vector and the perpendicular magnetic field vector. These properties can be exploited in power source systems to sense supply voltage and current and directly yield the product and thus power consumption in real-time applications. As a result, no multiplication circuitry is required. The active area and manufacturing costs are thus reduced when used within integrated circuits (IC).

This document describes the design of a linear power sensor based on Hall multiplication. The primary design goal was to design a functional linear power sensor using less circuitry and thus decreasing costs when compared to conventional methods used for power metering applications. The sensor is thus intended for integration into currently available single-chip power meter solutions through minor modification.

The sub-circuits necessary for a fully functional system has been designed and simulated. These include; i) voltage to current converters for biasing the Hall generator as a function of the source voltage, ii) bandgap reference for temperature independent on-chip referencing, iii) operational amplifiers for sensing and amplification of the Hall voltage and, iv) offset cancellation circuitry for removing offsets inherent in the amplifiers as well as the Hall generator.

The sensor has been verified on system level through both simulation and discrete component level testing.

UITTREKSEL

Sleutelwoorde: Hall-opwekker, Hall-sensor, Hall-spanning, Hall-vermenigvuldiging, Hall-effek sensor, magneetveld sensor, magnetoweerstand, magnetokonsentrasie, galvanomagnetiese effekte, termomagnetiese effekte, termoelektriese effekte, piezoweerstand effekte, kwadratuur rotasie, multivinger transistors, vlokkie-op-bord.

'n Hall-opwekker kan soos 'n vermenigvuldiger funksioneer wat 'n Hall spanning lewer. Dit kan die kruisproduk van die voorstroom vektor en loodregte magneetveld vektor voorstel. Dié eienskappe kan gebruik word in kragbronne om toevoerspanning en -stroom te meet en direk 'n produk te lewer, wat drywingsverbruik intyds voorstel. Dus word vermenigvuldiging stroombane nie benodig nie. Die aktiewe area benodig word verminder wanneer dit toegepas word in geïntegreerde stroombane, en so word vervaardigingskostes verminder.

Hierdie dokument beskryf die ontwerp van 'n liniêre drywingsensor wat op Hall-vermenigvuldiging gebasseer is. Die primêre ontwerpsdoel was om 'n funksionele liniêre drywingsensor te ontwerp, wat minder stroombane benodig om kostes te verminder wanneer vergelyk word met huidige drywingsmeting toepassings. Die sensor is ontwerp met huidige enkelvlokkie drywingsmeters in gedagte en sal slegs klein veranderings benodig om by ander stelsels aan te pas.

Die boublokke wat benodig word vir 'n volledige, werkende stelsel is ontwerp en gesimuleer. Hierdie sluit in: i) 'n spanning-na-stroom omsetter, vir voorspanning van die Hall-opwekker, wat eweredig is aan die kragbron spanning, ii) 'n bandgaping verwysing vir temperatuur onafhanklikke spanningsverwysing, wat benodig word deur verskeie stroombane, iii) operasionele versterkers, om die Hall-spanning te meet en te versterk en, iv) afset kansellasie stroombane, om wanbalanse te verwyder wat inherent voorkom in versterkers sowel as die Hall-opwekker.

Die sensor is op stelselvlak sowel as op diskrete komponent vlak gesimuleer en funksioneer korrek.

CONTENTS

1. INTRODUCTION

Generally, solid-state energy meters are based on two types of signal processing, namely analog and digital [1]. This signal processing refers to multiplication and filtering for the extraction of the information required by an energy meter and includes kWhrs, VARS etc. Typical trends are that companies with newer generation technologies can process most signals in the digital domain where older technologies have to utilize analog signal processing techniques to minimize digital circuitry. This is due to the fact that digital circuitry in older technologies tends to dominate final chip size thus making it extremely difficult for companies using these technologies to be competitive within the solid-state energy metering market. Although processing signals digitally assists easier reconfiguration to meet specific local requirements or upgrades, digital signal processing (DSP) comes at a large overhead in circuitry and is unsuitable for companies with older, larger Complementary Metal Oxide Semiconductor (CMOS) processes. For such companies to remain competitive, it is necessary to find a balance between analog and digital signal processing such that integrated circuit area is utilized cost effectively. Hall effect sensors have recently played a major role in finding a balance between the analog and digital domain. Their inherent multiplication properties can be used to calculate the product of the line voltage and current. This directly yields the power vector, which can subsequently be digitized and processed, eliminating the need for large digital multipliers and filters. Multiplication is ultimately executed "free of charge" within the Hall generator through simple signal manipulation.

1.1.1. Current Sensing Techniques

Modern solid-state power meters contain elements for sensing both voltage and current. Voltage sensing is typically achieved by dividing down the line voltage using a resistor divider or a potential transformer when isolation from the line is required. Current sensing however, poses a much more difficult problem. Due to the rich harmonic content in the current waveform, current sensors not only require a much wider measurement dynamic range, but also need to handle a much wider frequency range. There are three common current sensing technologies currently deployed in the market and these include the low resistance current shunt, the current transformer (CT), and the Hall effect sensor [2].

Low Resistance Current Shunt

The low resistance current shunt is the lowest cost solution available today and it offers simple current measurement with high accuracy. One disadvantage of the shunt resistor is that high precision current measurement is affected by the parasitic inductance of the shunt. Although this affects only the magnitude of the impedance at relatively high frequency, its affect on the phase at line frequency causes a noticeable error at a low power factor. A phase mismatch of 0.1° will lead to about 0.3% error at a power factor of 0.5.
The low cost and high reliability make the low resistance current shunt a very popular choice for energy metering. The major disadvantage to using the shunt is that fundamentally a shunt is a resistive element, the power loss is thus proportional to the square of the current passing through it and consequently it is a rarity amongst high current energy meters.

Current Transformer

The CT is based on the principle of a transformer and converts a high primary current into a smaller secondary current and is common among high current solid-state energy meters. As this device is a passive device, no extra driving circuitry is needed in its implementation. Another major advantage is that it can measure very high current while consuming little power. The disadvantage of the CT is that a very high primary current or a substantial DC component in the current can saturate the ferrite material used in the core ultimately corrupting the signal. Another problem is that once the core is magnetized, it will contain hysteresis and the accuracy will degrade unless it is demagnetized again.

Hall Effect Sensor

The advantages of the Hall effect sensor is that it has outstanding frequency response and is capable of measuring very large current and because it is an integrated circuit element, it can be integrated into a system as a whole, something not possible with the other sensing solutions. Accuracy is also improved by eliminating the phase shift errors normally associated with CT's, which are large at low power factors. The disadvantage however, is that the output can have a large temperature drift and as the system is active, additional circuitry is required for successful implementation. Many techniques exist to combat these problems but at an additional circuit overhead.

This dissertation presents a power sensor system that utilizes the multiplication properties of the Hall generator thus greatly reducing the need for digital circuitry normally required in similar systems to execute multiplication of sensed line voltage and current and thus ultimately saving chip area required. The system is implemented in a standard CMOS process and can thus easily be integrated into embedded systems. Power meters based on the Hall effect may display useful reduction in support circuitry required when compared to similar systems using other sensing techniques. The work presented in this dissertation will also form a foundation for further study into increasing the accuracy of such a system as well as compensation techniques that would assist in exploiting the properties of the Hall effect generator. The gain in area performance can thus be used to add economic value to power metering systems.

1.2. SUMMARY OF RELATED WORK

Not much literature exists in the field of Hall effect based power sensors. Although some companies are manufacturing power sensors based on the Hall effect such as Load Controls Incorporated [3], most Hall effect sensors on the market in this field are only designed for current sensing. This utilizes only half of the properties inherent in such an element and it seems that hardly any manufacturers have exploited the full potential of these Hall effect devices. An example of a product from Load Controls Incorporated is the Power Cell, designed for sensing and monitoring power in electrical motor controlled applications. Hall sensors are extremely well suited to this application as it greatly simplifies installation and will also operate on the output of variable frequency drives as well as odd wave shapes.

The system design uses well-established micro-electronic design techniques and thus some emphasis must be placed upon the Hall generator. Traditionally, Hall generators consists of the well understood square plate but new geometries are now being investigated [4, 5] to improve on the relevant properties required for applications other than direct magnetic field sensing as well as to overcome certain second order effects [4, 6, 7, 8, 9, 10, 11] inherent in the square plate configuration. Popović [8] explains the design principles behind the Hall generator. Popović is the pioneer in the field of semiconductor Hall effect generators and has played a major role in the industry regarding Hall effect sensors.

The mechanical configuration of current sensing elements is also of great importance and most techniques employ a ferrite core structure so that the magnetic field can be concentrated

over the Hall generator [12, 13, 14, 15, 16]. Some micro-magnetic field concentrators have been investigated and successfully implemented [17] but at the cost of extra manufacturing steps. Here a metal layer is deposited over the semiconductor in a very specific manner such that its physical construction concentrates the magnetic field over the Hall generator. Micro machining techniques have also been applied here for high accuracy requirements.

1.3. CONTRIBUTIONS OF THIS STUDY

The research discussed in this dissertation aims to contribute knowledge to the field of power sensing based on Hall effect multiplication as an economically competitive alternative to current power sensing techniques. The main criteria is a fully integrated sensor and thus ultimately a cost efficient alternative in an increasingly competitive market. A fully functional power sensor system is implemented and evaluated according to the International Electrotechnical Commission (IEC) 1036 standard [18, 19]. An analysis in Hall generator design is also presented so as to emphasize the important aspects to be taken into consideration for the design of this specific application.

1.4. DISSERTATION OUTLINE

Chapter 1 Introduction

Chapter 2 A discussion of the IEC 1036 standard as a basis for the power sensor system architecture and specifications as well as an explanation of the basic operation of the system.

Chapter 3 The galvanomagnetic effects in semiconductors as the basis for designing the Hall generator.

Chapter 4 A description of the design and verification of the support circuitry required to obtain the required specifications.

Chapter 5 An overview of the complete power sensor system as well as interfacing requirements and verification of specifications.

Chapter 6 Concluding summary

2. POWER SENSOR ARCHITECTURE

2.1. INTRODUCTION

The overall power sensor system consists of many basic building blocks that must be arranged into an architecture to perform according to the application requirements. Exact application requirements need to be taken into account such that the characteristics of the architecture may be exploited to the advantage of the final design specification. The design specification is deduced from the IEC 1036 standard, which is the international standard requirement for class I power meters. This chapter discusses the requirements for a class I power meter based on the IEC 1036 standard followed by the proposed sensor system architecture required to fulfill these specifications based on Hall effect multiplication including various aspects to consider during the design of the sub-system architectures such that system requirements are met.

2.2. BACKGROUND

2.2.1. The IEC 1036 Standard

Objective

The objective of the IEC is to promote international co-operation on all questions regarding the standardization in the electrical and electronic fields. The IEC is a world wide accepted organization and collaborates closely with the International Organization for Standardization (ISO). The preparation of the IEC 1036 was based on the IEC 521 and IEC 687 standards as reference. The standard covers the "standard meter" that will be used indoors and outdoors in large quantities worldwide. The standard distinguishes the accuracy of class index I and II meters, the protective class I and class II meters and also meters for use in networks equipped with or without earth fault neutralizers. Test levels in the standard are regarded as the minimum values required to guarantee the proper functioning of the meter in its normal operating environment.

General Definitions

Before we define the specifications of the power sensor, it is necessary to define the terminology used by the IEC standard. This terminology will be adhered to in any further technical description of the proposed sensor design. Although the standard describes active

energy meters as a fully completed entity, many of the specifications directly influence the design proposed in this dissertation. The standards applying to static watt-hour meters of accuracy class I for measuring alternating current (AC) electrical active energy of frequency in range 45 Hz to 65 Hz of line voltages less than 600 V will be used to define the applicable specifications for the proposed design.

- Static watt-hour meter – Meter in which current and voltage act on solid-state (electronic) elements to produce an output proportional to watt-hours.
- Continuous output linear power sensor using Hall effect vector multiplication - The design of a measuring device that senses line voltage and current and calculates the active power and satisfies the applicable minimum specifications as required by a static watt-hour meter. (Main part of the measuring element)
- Measuring element – Part of the meter that produces an output proportional to the energy.
- Current circuit – Internal connections of the meter and part of the measuring element through which flows the current of the circuit to which the meter is connected.
- Voltage circuit – Internal connections of the meter, part of the measuring element and power supply for the meter, supplied with the voltage of the circuit to which the meter is connected.

Definition of Meter Quantities

- Basic current (I_b) – Value of current in accordance with which the relevant performance of a direct connected meter is fixed.
- Maximum current (I_{max}) – Highest value of current, which the meter supports to meet the accuracy requirements of this standard.
- Reference voltage (U_n) – Value of the voltage in accordance with which the relevant performance of the meter is fixed.
- Reference frequency – Value of the frequency in accordance with which the relevant performance of the meter is fixed.
- Percentage error – Percentage error is defined by the following formula:

$$\%error = \frac{measured\_energy - true\_energy}{true\_energy} \times 100 \qquad (2.1)$$

Electrical Requirements

The standard defines the following for a class I meter using direct sensing techniques

Table 2.1 Standard references

Measured Quantity	Standard values
Voltage (V)	120-230-277-400-480
Current (A)	5-10-15-20-30-40-50
Frequency (Hz)	50-60
Temperature (°C)	-25°C to 70°C
Voltage circuit max consumption	2 W and 10 VA
Current circuit max consumption	4.0 VA
Power supply range	0.9 to 1.1 U_n

Maximum current for direct connected meter shall be preferably an integral multiple of the basic current (e.g. four times the basic current). The starting current will be 0.004 I_b.

Accuracy Requirements for Sensing Current

Table 2.2 Current sensing accuracy requirements

Value of current	Power factor	% Error limit
$0.05\ I_b \leq I \leq 0.1\ I_b$	1	±1.5
$0.1\ I_b \leq I \leq I_{max}$	1	±1.0
$0.1\ I_b \leq I \leq 0.2\ I_b$	0.5 Inductive 0.8 Capacitive	±1.5 ±1.5
$0.2\ I_b \leq I \leq 0.1\ I_{max}$	0.5 Inductive 0.8 Capacitive	±1.0 ±1.0
$0.2\ I_b \leq I \leq I_b$	0.25 Inductive 0.5 Capacitive	±3.5 ±2.5

Accuracy Requirements for Temperature Stability

Table 2.3 Temperature stability requirements

Value of current	Power factor	Mean temperature coefficient %/K
$0.1\ I_b \leq I \leq I_{max}$	1	0.05
$0.2\ I_b \leq I \leq I_{max}$	0.5 Inductive	0.07

Accuracy Requirements for Voltage and Frequency Stability

Table 2.4 Voltage and frequency stability requirements

Influence quantity	Value of current	Power factor	% Error limit
Voltage variation ± 10 %	$I_b \leq I \leq I_{max}$ $0.1\ I_b \leq I \leq I_{max}$	1 0.5 Inductive	0.7 1.0
Frequency variation ± 10 %	$I_b \leq I \leq I_{max}$ $0.1\ I_b \leq I \leq I_{max}$	1 0.5 Inductive	0.5 0.7

2.3. PROBLEM DEFINITION

With the definition of the required relevant specifications needed for a complete static watt-hour metering system in place, it is now possible to outline the requirements as needed by the linear power sensor such that the requirement for integrating the sensor into a static watt-hour meter can be fulfilled. As the Hall generator executes the main functionality of the system, it is responsible for the fulfillment of the majority of the specifications as outlined by the IEC 1036 standard. The specifications will thus be grouped in two categories namely the Hall generator itself and the system requirements necessary to obtain these specifications.

- The Hall generator's characteristics are mainly dependent upon the technology in which it will be manufactured. These characteristics need to be analyzed to determine which of them will influence the final specification.
- The geometry of a Hall generator has a major influence over performance characteristic and the designer has control over the parameters that directly influence the size and geometry of the device. It will be necessary to identify the most important characteristics that will influence the performance according to the required specifications. The proposed device geometry is the cross-shaped Hall generator and it

will be necessary to investigate the sizing ratio required to maximize the sensitivity of the device while keeping offsets and short-circuiting effects to a minimum.

As the Hall voltage generated by Hall generators is extremely small and unstable in its own capacity, certain support circuitry will be required to meet the system specifications and will require the following circuits to be designed and implemented:

- A voltage to current converter that will transform the sensed line voltage into a well defined biasing current needed by the Hall generator as well as the external requirements and changes needed to adapt to the different standard references as required by the IEC 1036 standard. (See table 2.1)
- The design of an accurate temperature independent voltage and current reference circuit that will assist in obtaining the temperature performance specifications in table 2.3.
- As mentioned earlier, the Hall voltage representing the active power is extremely small and it will thus be necessary to amplify the signal such that it can be presented at a suitable signal level and simply adapted as per requirements of future applications of the sensor.
- As the offsets inherent in the Hall generator and amplifiers are in the same order of magnitude as the generated Hall voltage, it will be necessary to design and implement offset cancellation circuitry as well as low pass filters to successfully extract the useful information from the signal.

This dissertation concentrates on the theoretical design of the proposed sensor. Core parts of the design will be implemented using a standard 1.2 µm CMOS process for experimental verification purposes only. All design parameters will be based on this process and can be seen in addendum A.

2.4. SYSTEM ARCHITECTURE

2.4.1. Traditional Watt-Hour Meter Architecture

Traditional watt-hour meters consist of a voltage sensing circuit, a current sensing circuit, an analog to digital converter, various digital filters, digital multipliers and information extraction circuitry. Figure 2.1 illustrates the typical architecture normally implemented and it can be seen that a large circuit overhead is resident in the fact that two amplifiers and AD converters are required for the voltage and current sensing circuits.

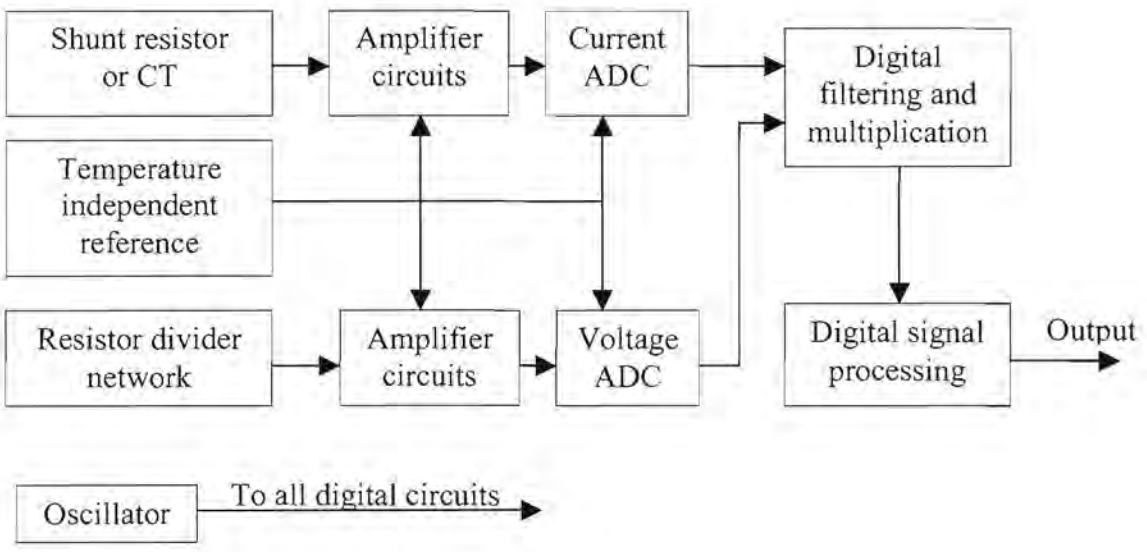

Figure 2.1 Block diagram of traditional watt-hour meters

The meters are designed such that external components are used to calibrate the meters as well as set the meter up for the different standard references as in table 2.1. Voltage and current sensing circuits typically use signal levels in the order of a few tens of mV or μA respectively.

Current Sensing

Current sensing is achieved through the use of shunt resistors or CT's. Typically shunt resistors are in the order of 500 μΩ producing a voltage drop that is linear to the current passing through it according to Ohm's law. This voltage drop would thus be a few mV and can be used directly to represent sensed current. Although this method is extremely accurate, a power of about 1 W could easily be consumed in the shunt resistor at rated currents making

the solution expensive when viewed in large quantities. The use of CT's are also extremely popular as they consume very little power during sensing, but phase errors and saturation problems must be taken into consideration during design and also contribute to circuit overhead and cost. Furthermore, it must be remembered that these devices contribute to the cost of manufacturing watt-hour meters even though these devices are manufactured in large quantities. In many cases, the use of CT's can contribute a cost equivalent to the IC itself.

Voltage Sensing

The voltage sensing circuit uses resistive divider networks to step the high line voltage down to suitable levels for solid-state electronic circuitry. This network typically consists of a few resistors in series such that the power dissipated in each resistor is distributed between them. Normally the input current of the voltage sensing input would be well defined such that the resistors are easily calculated according to Kirchoff's voltage or current laws.

2.4.2. The Hall Effect Multiplier

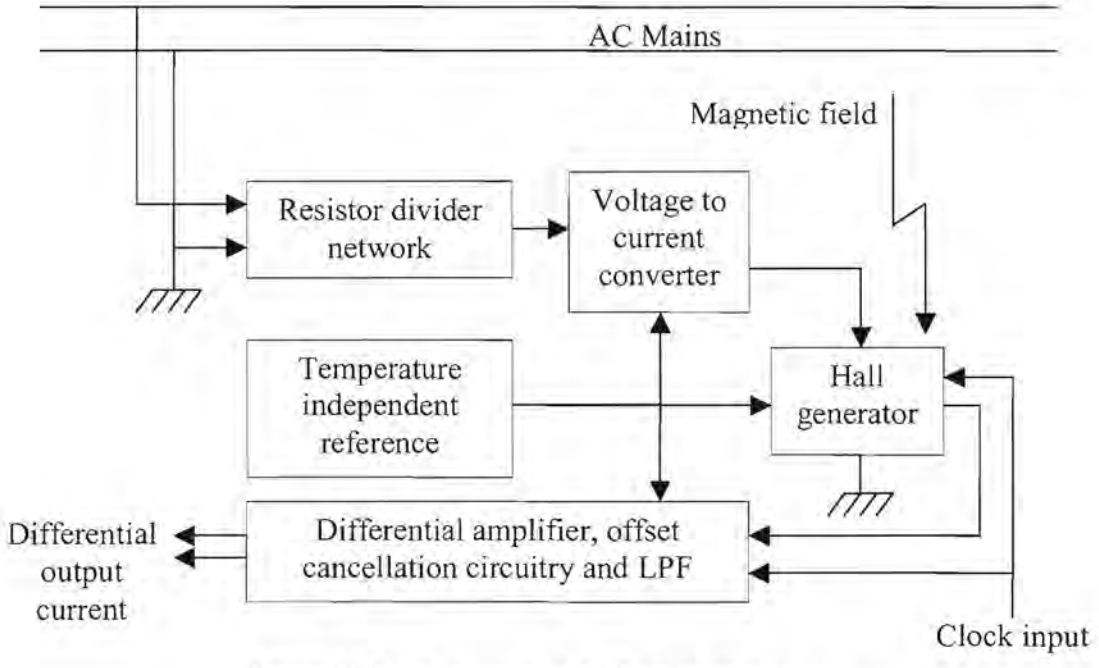

Figure 2.2 Block diagram of the linear power sensor

Figure 2.2 shows the block diagram of the Hall multiplication based linear power sensor. It can be seen that using the inherent multiplication properties of the Hall generator, the voltage and current sensing circuits are incorporated into a single unit. Furthermore, only one AD

converter is needed to encode the output signal of the Hall effect sensor. The complete system is based on differential signal processing to suppress noise and common mode signals.

2.5. SYSTEM OPERATION

2.5.1. Resistor Divider Network

This circuit represents the voltage-sensing element and has the same functionality as that of the voltage sensing element in figure 2.1. Once again the network consists of a few resistors in series for power dissipation distribution purposes. The network divides the voltage down to a value suitable for the solid-state electronics as well as assists in converting this voltage into a current signal. This current signal is used to bias the Hall generator and is linearly dependent upon the mains voltage. The Hall generator can be biased using either a biasing current or a biasing voltage. The problem however when using a voltage is that due to process variations, the Hall plate resistance itself may vary greatly thus resulting in an unpredictable biasing current. As the Hall voltage generated is directly proportional to this current, the result would be a Hall voltage signal with high tolerances. The result is to use a defined current to bias the plate thus greatly increasing the accuracy of the resultant signal.

2.5.2. Hall Generator

The Hall generator consists of an extremely thin semiconductor plate configured in such a way so as to maximize the Hall effect in the presence of a magnetic field perpendicular to the plate. Equation 2.2 shows how the Hall voltage generated is the product of the biasing current I_{bias}, the perpendicular component of a magnetic field, $\boldsymbol{B}$, approaching the plate at an angle θ, and the sensitivity, consisting of the Hall coefficient R_H, divided by the Hall plate thickness t. As the biasing current is proportional to the line voltage V_{line}, and the magnetic field is proportional to the line current I_{line}, the Hall voltage V_h, represents the instantaneous power consumed in the line as illustrated in equation 2.3.

$$V_h = \frac{R_H}{t}\left(I_{bias} B \sin\theta\right) \tag{2.2}$$

$$V_h \propto \frac{R_H}{t}\left(V_{line} I_{line}\right) \tag{2.3}$$

Figure 2.3 shows how the Hall generator is configured. It consists of a Hall plate manufactured of a semiconductor material with four leads attached. A bias current I_{bias} flows through two leads while a differential Hall voltage V_h is generated across the sensing leads.

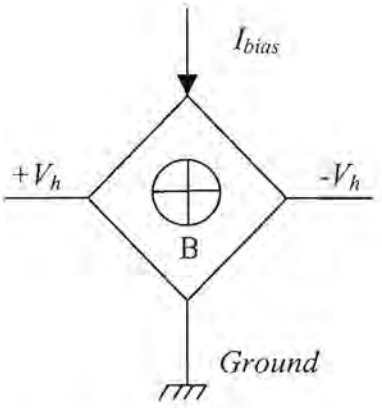

Figure 2.3 The Hall generator

An important aspect here is the fact that the Hall voltage generated is a differential signal in that the Hall voltage is the difference between $+V_h$ and $-V_h$. Furthermore, both $+V_h$ and $-V_h$ have a common mode voltage with respect to ground and is equal to the biasing current through the plate multiplied by half the plate resistance. The differential signal thus establishes the need for fully differential amplifier design and the Hall voltage will be amplified by a suitable factor such that the power information can be extracted with high accuracy.

Another problem that exists in Hall generators is offsets. In the presence of a zero magnetic field, the Hall generator ideally has a zero differential output. However, due to misalignments that occur as result of process variations as well as gradual changes in resistance gradients over the semiconductor, physical imbalances are created and when electrically stimulated result in a differential voltage being present at the output of the Hall generator in the absence of a magnetic field. These offsets can represent a significant value of the parameter under measurement and need to be compensated using offset cancellation techniques to reduce its effects. As operational amplifiers themselves produce a significant amount of offset, techniques for combining offset cancellation such that both the Hall generator and the operational amplifier's offsets are cancelled in the same signal processing step will be beneficial to minimize circuitry.

2.5.3. Temperature Independent Reference

Temperature independent referencing has become extremely important in IC design. Analog circuits extensively incorporate voltage and current referencing. These references are dc quantities exhibiting little dependence on supply voltages and process parameter variations and a well-defined dependence on temperature. This is necessary as biasing currents affect differential pair voltage gain as well as noise performance of the circuit. The circuit will thus be responsible for all required biasing currents needed by the voltage to current converter, the amplifiers and the Hall generator itself.

2.5.4. Differential Amplifier, Offset Cancellation Circuitry and Low Pass Filtering

The amplifiers to be used will be fully differential operational amplifiers. This is necessary for increasing the linearity performance of the system and to suppress the common mode noise present. The amplifier design will focus on minimizing offsets as well as common mode signal suppression. The specifications for the operational amplifier will not need to be extremely stringent in terms of speed as the lines frequency is specified by the IEC 1036 in the range 45 to 65 Hz. The specification however, requires that the power content of at least the 5^{th} harmonic also be measured, implying a minimum frequency response of 325 Hz. As the frequency response of the Hall generator itself is in the order of KHz, this specification is obtainable.

Offset cancellation will be based on differential techniques, which will be used in conjunction with the offset cancellation techniques implemented in the Hall generator itself. Offsets will be interpreted as a constant value of power being consumed and final offset specifications must be reduced such that the specification limits in current and voltage accuracy are still met as set out in table 2.2. Offset cancellation for the Hall generator will be based on the dynamic quadrature offset cancellation technique as suggested by Bilotti, Monreal and Vig [4]. Offset timing will be controlled by the clock input, a 50% duty cycle square wave signal of high frequency (in the order of tens of KHz). The signal will be generated externally such that the system effects as a result of clock variation can be studied. This however would be generated internally when integrated into a fully functional watt-hour meter and forms an important part of the stability requirements of the system as set out in the IEC 1036 standard.

Finally, as a result of the offset cancellation techniques proposed, it will be necessary to low pass filter the output signal. The IEC 1036 frequency specification will determine the –3 dB cut-off frequency of the filter, which will be in the order of 500 Hz. The filter will also assist in the filtering out of high frequency switching noise.

2.6. SYSTEM SPECIFICATIONS

The basic system requirements will now be stated. These are entirely based on the IEC 1036 standard and as mentioned before, the sensor must later form part of a watt-hour meter and thus adhere to all international standards. For experimental purposes it was necessary to define some parameters such as maximum line current I_{max} and others such that some components could be physically realized. These parameters will later form part of customer requirements and the system will be designed such that simple modifications will be possible to bring the sensor in line with these demands. Error specifications will be tested for a power factor of 1 unless otherwise specified. The following specifications make up the system performance requirements. These specifications form the basis for future research and development of the sensor.

Circuit operating voltage	5 V
Maximum supply current	< 2 mA
Operating temperature	-25°C to 70°C
Maximum Line Voltage	230 V_{rms}
Base current	20 A_{rms}
Maximum line current	80 A_{rms}
Line frequency	50 Hz
System sensitivity	0.231 µA/kW (rms)
Temperature stability for $0.1\ I_b \le I \le I_{max}$	±0.05 %/K
Accuracy for $0.05\ I_b \le I \le 0.1\ I_b$	±1.5 %
$0.1\ I_b \le I \le I_{max}$	±1.0 %
Voltage circuit max consumption	2 W and 10 VA
Current circuit max consumption	4.0 VA
Process requirements	Standard silicon 1.2 µm CMOS, double metal, double poly

2.7. CONCLUSION

This chapter presented the IEC 1036 standard according to which the proposed linear power sensor will be designed and measured. The requirements relevant to the designing and implementation of the proposed sensor have been highlighted and discussed. A traditional watt-hour meter architecture was presented and discussed explaining the functionality of the system and how the new sensor design will affect this system. The proposed sensor system architecture was presented and discussed explaining the relevant issues to take into consideration during the design phase of the sensor. These include:

- Reasons for current biasing rather than voltage biasing of the Hall generator and the implementation thereof,
- The basic operation of the Hall generator,
- Temperature independent voltage and current referencing and its basic effect on system stability,
- The differential operation of the system and the basic requirements for the differential amplifiers, offset cancellation and low pass filtering.

Finally, the system specifications were proposed for the entire system and these included all system performance requirements, operating conditions and accuracy conformance specifications in compliance with the relevant requirements from the IEC 1036 standard.

3. HALL GENERATOR

3.1. INTRODUCTION

The generation of a strong Hall effect requires a high velocity of charge carriers. This can be either achieved by a high electric field, or by a high mobility of the quasi-free charge carriers. Metal conductors as used at the time of the Hall effect discovery, fulfilled neither of these two requirements. Semiconductor technology revolutionized this. Low doped semiconductor materials possess a low density of quasi-free charge carriers. These carriers hardly interact with the ionic impurities, giving them a high mobility. Moreover, they are few enough, which permits us to apply a high electric drift field without thermally degenerating the material. Both these features lead to a high velocity and consequently to a high signal level. For this reason, Hall effect devices today, are exclusively made of semiconductor material. Since we are concerned with the designing of an integrated Hall generator in silicon that can accurately measure medium strength magnetic field intensities generated by the line current through a wire-wound ferromagnetic core, it is of particular interest for us to understand which material phenomena determine the behavior of the Hall effect in silicon for its successful design.

Semiconductor-integrated sensors has undergone major development over recent years and has been driven by the need for a reduction in size and increasing efficiency of electronic circuitry in semiconductor single chip solutions. This field has now completely revolutionized electronic sensing and holds particularly true for magnetic field sensors (MFS). Integrated silicon MFS's can now be manufactured using standard IC technologies without introducing any extra manufacturing steps or procedures such as "micromachining" or film deposition as in the case of most mechanical or chemical sensors.

The Hall generator falls under the category of magnetic field sensors and is a transducer that converts a magnetic field into a useful electronic signal. There exist two main groups of MFS applications namely *direct* (magnetic fields, reading of magnetic tapes, etc.) and *indirect* also called "tandem" transduction (mechanical displacement of magnets, current sensing, etc.). The linear power sensor thus requires the detection of magnetic fields in the micro- and millitesla (mT) range, which can be achieved with integrated semiconductor sensors. This chapter will thus focus on the magnetic properties and effects of the Hall generator upon which the design method for the Hall generator will be based.

3.2. BACKGROUND

Semiconductor MFSs are based on galvanomagnetic effects such as Hall voltage, carrier deflection, magnetoresistance and magnetoconcentration, all due to the action of the Lorentz force on the charge carriers (electrons and holes) and further magnetically form part of the low-permeability (dia- or paramagnetic) group where $\mu \approx 1$.

Silicon (Si) and gallium arsenide (GaAs) offer an advantage of inexpensive batch fabrication by the integration of single or multiple sensor elements together with appropriate support and signal processing circuitry in an advanced standard technology of established reliability, such as bipolar or CMOS technology. Many custom chip manufacturers around the globe using design rules of a standard chip manufacturing process have exploited this advantage. MFS development outside these processes requires special manufacturing techniques and appropriate test and reliability procedures. The development costs involved are usually far beyond the financial reach of small to medium sized companies.

3.3. GALVANOMAGNETIC EFFECTS IN SEMICONDUCTORS

For the designing of effective and efficient Hall generators, an understanding of the mechanism of galvanomagnetic effects in semiconductors is necessary. This chapter describes the bulk integrated Hall device for its widely explored and well-understood behavior as the benchmark for performance measurement of the proposed Hall generator. The device will be analyzed in terms of device sensitivity, noise performance, offsets, linearity, electrical functionality and technological compatibility with standard CMOS processes.

3.3.1. The Hall Effect

Figure 3.1 shows the generation of the Hall effect and is the occurrence of a current component perpendicular to a control current I_y and magnetic field B_z as a direct result of the Lorentz force [8, 9, 10, 11, 12, 20]. Charge carriers are deflected by the magnetic field. To ensure that the transverse current is zero, an electric field called the Hall field is established. If the magnetic field is zero, the two points y_1 and y_2 have the same potential, i.e., the voltage difference between the two points is zero and thus no Hall voltage is present.

If $B_z \neq 0$, there will be a voltage difference between points y_1 and y_2 which is proportional to the magnetic field and

$$V_H = R_H\left(\frac{I_y B_z}{t}\right) \qquad (3.1)$$

where I_y = current in direction y,

t = semiconductor thickness,

R_H = proportionality factor (Hall coefficient).

The Hall coefficient is inversely proportional to the density of free carriers. To obtain a large Hall voltage, a material with a small carrier density is required.

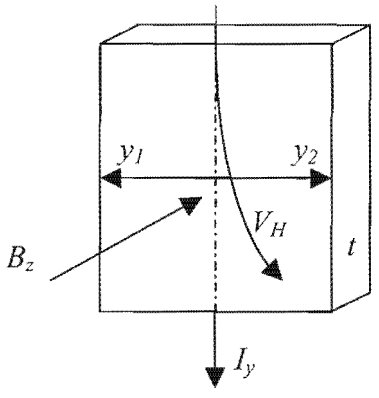

Figure 3.1 The Hall effect in a piece of semiconductor material

The Hall effect, like other galvanomagnetic effects, is thus a manifestation of the charge carrier transport phenomena in condensed matter when carriers are under the influence of the Lorentz force. We assume isotropic n-type material with zero temperature gradient. Further, we denote the electron current density for $\boldsymbol{B} = 0$ by $\boldsymbol{J}_n(\mathbf{0})$. The diffusion approximation of the Boltzmann transport equation thus reduces to [8, 9, 10, 11],

$$\boldsymbol{J}_n(0) = \sigma_n \boldsymbol{E} + qD_n \nabla n \qquad (3.2)$$

Where $\sigma_n = q\mu_n n$, denotes the electronic conductivity,

$\boldsymbol{B} = 0$, denoting the magnetic field,

$\boldsymbol{E}$, the electric field,

$q = 1.6 \times 10^{-19}\ A.s$, the magnitude of electron charge,

$D_n = \frac{\mu_n kT}{q}$, the electron diffusion constant with Boltzmann's constant, k = 1.380658 x 10^{-23} J/K and temperature T, in Kelvin,

n, the electron density and

μ_n, the electron drift mobility.

In equation (3.2) the term $\sigma_n \boldsymbol{E}$, describes the drift current and $qD_n \nabla n$, the diffusion current. For nonzero magnetic induction $\boldsymbol{B}$, the electron current density $\boldsymbol{J}_n(\boldsymbol{B})$, obeys the equation

$$\boldsymbol{J}_n(\boldsymbol{B}) = \boldsymbol{J}_n(0) - \mu_n^*(\boldsymbol{J}_n(\boldsymbol{B}) \times \boldsymbol{B}) \tag{3.3}$$

Where μ_n^* is the Hall mobility for electrons. The Hall mobility is proportional to the drift mobility μ_n and $\mu_n^* = r_n \mu_n$. The scattering factor is defined as $r_n = \frac{\langle \tau_n^2 \rangle}{\langle \tau_n \rangle^2}$, where τ_n denotes the free time between collisions. The energy-band structure and the underlying scattering processes determine the value of r_n, which is about 1.15 for n-type silicon at room temperature for low donor concentrations.

Solving equation (3.3) with respect to $\boldsymbol{J}_n(\boldsymbol{B})$ yields,

$$\boldsymbol{J}_n(\boldsymbol{B}) = \frac{\boldsymbol{J}_n(0) - \mu_n^*(\boldsymbol{B} \times \boldsymbol{J}_n(0)) + (\mu_n^*)^2(\boldsymbol{B}.\boldsymbol{J}_n(0))\boldsymbol{B}}{1 + (\mu_n^* \boldsymbol{B})^2} \tag{3.4}$$

This equation comprises the isothermal galvanomagnetic effect for electrons and accounts for the direct effects of temperature on carrier concentration, diffusion and mobility excluding thermomagnetic and thermoelectric effects. The hole current density is defined in the same way. Poisson's equation as well as the pertinent continuity equations for electrons and holes is generally solved together with the electron and hole equations.

It is evident from equation (3.4) that the Lorentz force is included in both carrier drift and diffusion terms. Neglecting carrier concentration gradients as with n-type slabs with ohmic contacts reduces equation (3.4) to,

$$\boldsymbol{J}_n(\boldsymbol{B}) = \sigma_{nB}[\boldsymbol{E} + \mu_n^*(\boldsymbol{B} \times \boldsymbol{E}) + \mu_n^{*2}(\boldsymbol{B}.\boldsymbol{E})\boldsymbol{B}] \tag{3.5}$$

where,

$$\sigma_{nB} = \frac{\sigma_n}{1+(\mu_n^* B)^2} \tag{3.6}$$

With the magnetic field parallel to the electric field, $\boldsymbol{B} \times \boldsymbol{E} = 0$, and $\boldsymbol{J_n(B)} = \sigma_n \boldsymbol{E} = \boldsymbol{J_n(0)}$. No longitudinal galvanomagnetic effect is observed in isotropic semiconductors. If the magnetic field is perpendicular to the electric field, $\boldsymbol{B}.\boldsymbol{E} = 0$, and we obtain,

$$\boldsymbol{J}_n(\boldsymbol{B}) = \sigma_{nB}[\boldsymbol{E} + \mu_n^*(\boldsymbol{B} \times \boldsymbol{E})] \tag{3.7}$$

The equation describes transverse galvanomagnetic effects with negligible diffusion. When the test piece is orientated in space such that $\boldsymbol{B} = (0,0,B)$, $\boldsymbol{E} = (E_x, E_y, 0)$, and $\boldsymbol{J_n(B)} = (J_{nx}, J_{ny}, 0)$, equation (3.7) becomes

$$\left.\begin{aligned} J_{nx} &= \sigma_{nB}(E_x - \mu_n^* B E_y) \\ J_{ny} &= \sigma_{nB}(E_y - \mu_n^* B E_x) \end{aligned}\right\} \tag{3.8}$$

The two limiting cases namely the Hall field and carrier deflection and magnetoresistance are distinguishable and are now described respectively.

Hall Field

Explaining this limiting case, a long thin rod sample is used as an approximation, such that no Hall field is produced in the y-direction, i.e. the current density vector has only an x-component. The Hall field can thus be defined by

$$E_y = -\mu_n^* B E_x = R_H J_{nx} B \tag{3.9}$$

where,

$$R_H = -\frac{\mu_n^*}{\sigma_n} = -\frac{r_n}{qn} \tag{3.10}$$

denotes the Hall coefficient [21]. The result is a rotation of the equipotential lines by the Hall angle θ_H with

$$\tan\theta_H = \frac{E_y}{E_x} = -\mu_n^* B = \sigma_n R_H B \qquad (3.11)$$

A Hall voltage of $V_H = \frac{R_H I B}{t}$, is produced for long Hall plates of thickness t carrying a current I with a sensitivity of $\frac{V_H}{IB} = \frac{R_H}{t} = \frac{r_n}{qnt}$.

As one of the primary objectives is to achieve a high sensitivity, it is necessary to minimize the carrier concentration n. This substantiates the fact that semiconductors are more usefully implemented as Hall effect sensors than metals and why only since the discovery of semiconductors, Hall effect applications became viable.

Carrier Deflection and Magnetoresistance

The second extreme case would now be to reduce the Hall field to zero. Using a short sample of wide cross section with current electrodes at the large faces, this condition can be defined, and from equations (3.8) and (3.11), the current deflection can be calculated as

$$-\frac{J_{ny}}{J_{nx}} = \mu_n^* B = \tan\theta_H \qquad (3.12)$$

As the drift path has become substantially longer, the geometrical magnetoresistance will contribute significantly and is given by

$$\frac{(\rho_{nB} - \rho_n)}{\rho_n} = (\mu_n^* B)^2 \qquad (3.13)$$

where,

$\rho_n = \frac{1}{\sigma_n}$, is the resistivity for $B = 0$, and

$\rho_{nB} = \frac{E_x}{J_{nx}} = \frac{1}{\sigma_{nB}}$, the resistivity enhanced by the magnetic induction.

Silicon typically shows a resistivity of , $\rho_{nB} \approx 1.02\rho_n$, for magnetic field intensities as high as 1 T.

Equations (3.3) to (3.13) are approximations for weak field expansion and relative errors exist of $(\mu_n^* B)^2$. These equations however, show small errors for fields below 2T of $(\mu_n^* B)^2 \leq 0.1$, and thus still yield good approximations. Analogous to n-type Si, p-type semiconductor materials are characterized by drift and Hall mobility constants μ_p and $\mu_p^* = r_p \mu_p$, with the Hall coefficient given by

$$R_H = \frac{r_p}{qp} \tag{3.14}$$

with p, denoting hole concentration. At room temperature and for low doping, the scattering factor is $r_p \approx 0.7$. Analogous to n-type, the Hall angle is given by

$$\tan\theta_H = -\mu_p^* B \tag{3.15}$$

So too, the magnetoresistance effect is

$$\frac{\rho_{pB}}{\rho_p} = 1 + \left(\mu_p^* B\right)^2 \tag{3.16}$$

where,

$$\rho_p = \frac{1}{q\mu_p p} \tag{3.17}$$

Using this information, the Hall coefficient takes on a general form given by equation (3.18) for mixed type conduction.

$$R_H = -\frac{\left[r_n\left(\frac{\mu_n}{\mu_p}\right)^2 n - r_p p\right]}{q\left[\left(\frac{\mu_n}{\mu_p}\right)n + p\right]^2} \tag{3.18}$$

3.4. THE IDEAL HALL PLATE

The ideal Hall plate is by far the most developed and well-understood semiconductor Hall effect device implemented as a magnetic sensor. They have found well-established commercial use since their discovery and have been implemented as monolithic silicon integrated devices since the early 1970s. These devices have now set the benchmark against which newly developed Hall effect devices are measured. This section describes the ideal Hall plate properties.

3.4.1. Geometrical Considerations

The Hall plate is usually manufactured using a high resistivity material (semiconductor material), and provided with four ohmic contacts for biasing and sensing. From equation (3.1), it was seen that ideally a thin rectangular shaped plate was used. When biased, the plate builds up a Hall voltage across opposite sense electrodes in the presence of a magnetic field perpendicular to the plate plane as described in paragraph 3.3.1.

$$V_H = \frac{R_H}{t} G\left(\frac{l}{w}, \frac{s}{w}, \frac{y}{l}, \theta_H\right) B_z I \qquad (3.19)$$

A new factor is introduced here and is referred to as the geometrical factor. Figure 3.2 illustrates the plate dimensions with the Hall angle given by equation (3.11). The Hall coefficient of mixed type conduction semiconductor is given by the general form of equation (3.18) but usually the Hall plates work under strong extrinsic conditions with $n >> p$, and thus equation (3.10) applies. Although the scattering parameters r_n and r_p of the Hall plates are always close to unity, they play an important role in the temperature behavior.

Equation (3.19) can thus be described as

$$|V_H| \cong \frac{r_n}{qnt} G B_z I \qquad (3.20)$$

What can be seen from equation (3.20) is that the Hall voltage is inversely proportional to the carrier density and plate thickness. This explains why Hall plates are made from thin, high resistivity materials.

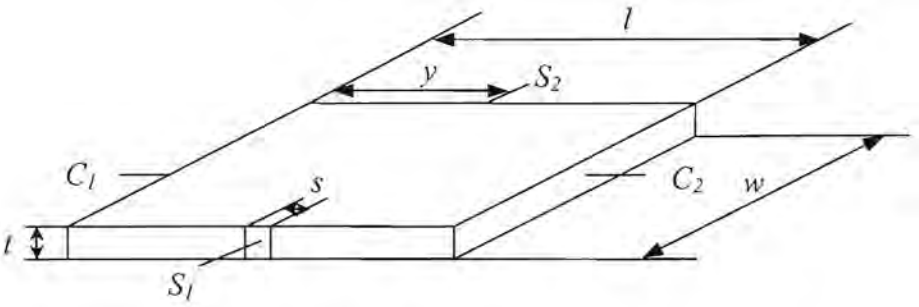

Figure 3.2 Rectangular Hall plate indicating dimensions

The geometrical factor in equation (3.19) and equation (3.20), expresses the difference between an infinitely long Hall plate and the finite one and is given by equation (3.21) and accounts for the short-circuiting effects resulting from current flowing through the sensor electrodes illustrated in figure 3.3.

$$G\left(\frac{l}{w},\frac{s}{w},\frac{y}{l},\theta_H\right)\equiv\frac{V_H}{V_{H\infty}} \qquad (3.21)$$

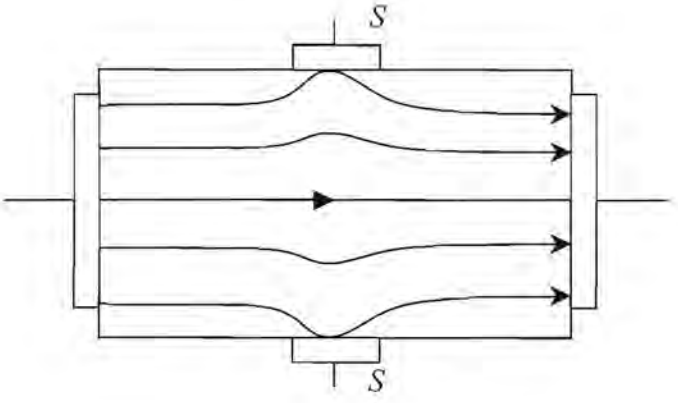

Figure 3.3 Short-circuiting effects due to sensor contacts

If it is assumed that only one type of carrier is involved and the geometry of the square plate is such that $\frac{l}{w}>1.5$, $\frac{s}{w}<0.18$ and $y=\frac{l}{2}$, G can be approximated by equation (3.22).

$$G_L = \left[1 - e^{\left(\frac{\pi}{2}\frac{l}{w}\frac{\theta_H}{\tan\theta_H}\right)}\right]\left[1 - \frac{2}{\pi}\frac{s}{w}\frac{\theta_H}{\tan\theta_H}\right] \quad (3.22)$$

Equation (3.22) approaches unity when $\frac{l}{w} > 3$ and $\frac{s}{w} < \frac{1}{20}$. With small Hall angles and short samples with point sensor electrodes, G is approximated by equation (3.23).

$$G_S \cong 0.74\frac{l}{w} \quad (3.23)$$

From equation (3.20) to equation (3.23), it can be seen that for maximizing the Hall voltage, it is necessary to maximize the plate length and minimize the thickness and carrier concentration. When analyzing the voltage drop across the plate in equation (3.24), it can be seen that a compromise is needed as maximizing the Hall voltage also increases the voltage drop across the plate.

$$V = \frac{1}{q\mu_n n}\frac{l}{wt}I \quad (3.24)$$

Substituting equation (3.24) in equation (3.20) yields the Hall voltage in terms of supply voltage and

$$V_H = \mu_n^* \frac{w}{l} G B_z V \quad (3.25)$$

The importance of high carrier mobility is evident here. It can also be seen that the Hall voltage increases with the $\frac{w}{l}$ ratio. The limit is obtained by substituting equation (3.23) into equation (3.25) and is given by equation (3.26).

$$V_{H,0} \approx 0.74\mu_n^* B_z V \quad (3.26)$$

Many other shapes have been proposed and even though Wick [9, 22] proved the invariance of Hall plate electrical efficiency with respect to geometry using his conformal mapping theory, some specific shapes have some technological advantages over others.

The two required properties for producing a more efficient Hall effect is a higher carrier mobility and lower doping. The question is now raised as to whether or not Si is an appropriate material for implementation as Hall effect devices. Si shows only a very moderate carrier mobility when operated at a given supply voltage, but materials such as InAs and InSb would be far superior in this respect. This however changes if the plate has to operate at a given power level which happens to be a considerably more important aspect of modern IC design. As high mobility materials feature small bandgaps, there is no way of obtaining at room temperature the low carrier densities that can be achieved using Si and GaAs. If the plate is operated with a constant current supply, its efficiency doesn't depend upon carrier mobility at all making both Si and GaAs well suited as Hall plate devices. Other criteria to consider are noise, offset and temperature behavior.

3.4.2. Electrical Compatibility Concerns

Electrical compatibility concerns are based on the two parasitic electrical effects [8] namely: effective plate thickness variation and leakage current and are associated with the reverse biased pn-junction associated with the Hall plate. Due to the junction field effect, the Hall plate thickness varies with the applied reverse bias junction voltage. There are two factors that come into play here, the first being the fact that the Hall plate introduces a voltage drop causing the effective junction bias to be position dependant and thus the effective plate thickness to vary across the plate. The second is the Hall voltage, due to its dependence upon the plate thickness, now too is affected and ultimately, equation (3.20) and equation (3.22) through equation (3.27) become invalid. However, in bulk Hall plates with *nt* products of more than $10^{12} cm^{-2}$, this effect is rather weak and these equations still yield good approximations. By making the reverse junction bias voltage adjustable, it is possible to vary the effective thickness of the plate and in so doing provides a means of adjusting the sensitivity of the plate. It has been reported that an adjustment range of up to $\pm 25\%$ have been achieved using this technique.

Up to this time, no major studies have been done on the influence of leakage currents on the integrated Hall plate. The main reason for this is that the leakage current is extremely small when compared to the bias current and thus has little effect. The proposed Hall generator in this design will use a plate size of approximately 8300 μm^2 (see figure 3.12). The technology specifies 0.25 $fA/\mu m^2$ leakage current for its n-well resulting in $\approx$ 2.1 pA/plate. The leakage is an order 10^6 smaller compared to the bias current of a few hundred μA and can be neglected.

3.4.3. Sensitivity

The absolute sensitivity of a Hall plate can be reported in one of two ways, supply-current-related sensitivity (equation (3.27)) and supply-voltage-related sensitivity (equation (3.28)).

$$S_{RI} \equiv \left| \frac{1}{I} \frac{\partial V_H}{\partial B_z} \right| = \frac{r_n G}{qnt} [V / A.T] \qquad (3.27)$$

$$S_{RV} \equiv \left| \frac{1}{V} \frac{\partial V_H}{\partial B_z} \right| = \mu_n^* \frac{w}{l} G[T^{-1}] \qquad (3.28)$$

The theoretical limit for the sensitivity established from equation (3.26) and taking $r_n \approx 1$, with appropriate mobility constants at room temperature yields [9],

$$S_{RV,\max} = \begin{cases} 0.128T^{-1} - Si \\ 0.725T^{-1} - GaAs \end{cases} \qquad (3.29)$$

for the two material types.

3.4.4. Noise

One of the major and dominant performance parameters of sensors is the signal to noise ratio (SNR). The voltage noise spectral density across the Hall electrodes is given by

$$S_V(f) = S_{V\alpha}(f) + S_{VT} \qquad (3.30)$$

where $S_{V\alpha}$, represents the f^{-1} noise and S_{VT}, the thermal noise, the first dominating at low frequency and the other at high frequencies respectively.

Maximizing the SNR over the frequency spectrum can thus be divided into, low and high frequencies. The SNR at low frequencies is increased when the Hall plate contains a large number of carriers and is made of a material with a high mobility and a low Hooge α-parameter. Geometrically, the SNR can be improved by designing for an aspect ratio of $\frac{l}{w} \approx 1.3$ [8].

High frequencies is dominated by thermal noise and increasing the Hall generator bias current, directly increases the SNR and is limited by the maximum allowable power dissipation in the plate. Using a high mobility material also results in a larger SNR at high frequencies.

3.4.5. Offset Voltage

Offset voltage in Hall generators embed themselves as a constant voltage present at the signal contacts in the absence of a magnetic field. The offset voltage is usually reported as an equivalent offset magnetic field or

$$B_{O,eq} = \frac{V_O}{S_A} \tag{3.31}$$

with S_A, denoting the absolute sensitivity.

Offsets in Hall plates come from a contribution of a number of factors. The dominant factors come from imperfections in the manufacturing process e.g. misalignment and fluctuations in material characteristics, and piezoresistive effects. These two effects are usually modeled as a simple resistive bridge incorporating asymmetry as shown in figure 3.4. Typical applications require offsets of $B_{O,eq} < 10$ mT.

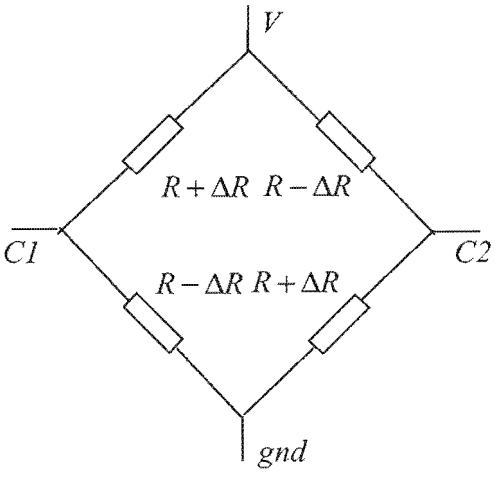

Figure 3.4 Bridge circuit model of Hall plate

The second most important source of offset voltage contribution comes in the form of mechanical stress introduced during packaging. Up to $B_{O,eq} \approx 8.4$ mT, can be introduced here

with the Hall device placed in the (110) crystal plane with current flowing in the <110> [8] direction. Consequently, a Hall plate placed in the (100) plane with a current in the <110> direction makes for a highly sensitive strain gauge [6, 7, 8]. Various techniques exist to reduce or effectively cancel offsets resident in Hall devices [4, 8, 23, 24, 25] and will be discussed in Chapter 4.

3.4.6. Linearity Error

The linearity error is defined as the ratio

$$LE = \frac{\left(V_H - V_H^0\right)}{V_H^0} \tag{3.32}$$

where V_H, is the measured Hall voltage and V_H^0, is the assumed best linear fit to the measured values. With a constant bias current, V_H^0 becomes

$$V_H^0 = \frac{V_{HL}}{B_L} B \tag{3.33}$$

with V_{HL} and B_L the values as indicated in figure 3.5 a). Figure 3.5 b) shows non-linearity represented as a variation in sensitivity versus the magnetic field.

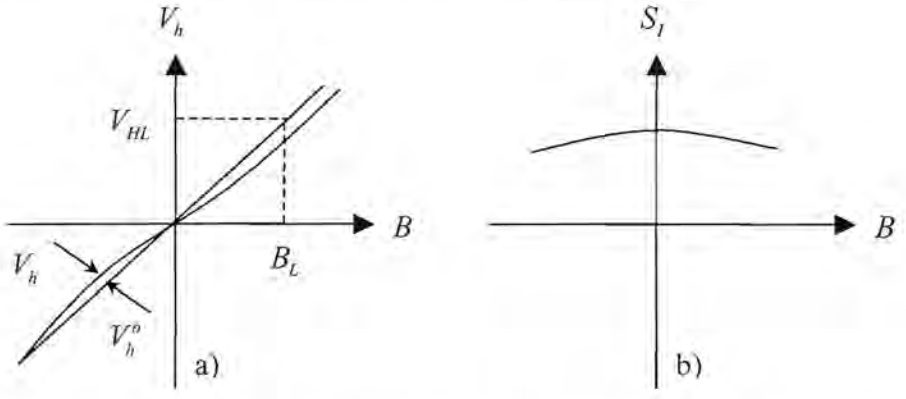

Figure 3.5 Non-linearity of Hall MFS in terms of a) Hall voltage and b) sensitivity versus magnetic field with constant current bias

This type of geometrical non-linearity is mainly due to the short-circuiting effects described by equation (3.20) and equation (3.22) and can be minimized through the proper resistive loading of the element. One of the lowest linearity error figures reported [26] was

manufactured from an implanted GaAs cross-shaped plate used in the range of less than 1 T at room temperature with an error of $LE = \pm 3 \times 10^{-4}$.

3.4.7. Temperature Coefficients

The temperature coefficients of the sensitivity are defined by

$$TC \equiv \frac{1}{S}\frac{\partial S}{\partial T} \tag{3.34}$$

with S, the absolute sensitivity or relative sensitivity as defined by equation (3.27) and equation (3.28) and T, the absolute temperature.

It is now assumed that the carrier concentration is constant, the Hall angle is very small and the junction field effect is ignored. If the Hall plate is supplied with a constant current, we obtain from equation (3.27) and equation (3.34) the pertinent temperature coefficient

$$TC_I = \frac{1}{r_n}\frac{\partial r_n}{\partial T} \tag{3.35}$$

It can thus be seen that the temperature coefficient of the sensitivity S_{RI}, is equal to that of the Hall scattering factor r_n. Typical values for Si have been experimentally determined to be around $TC_I \approx +0.8 \times 10^{-3}\ K^{-1}$ [8] for temperatures ranging from –20°C to 120°C for low-doped Si.

For a constant voltage bias across the plate,

$$TC_V = \frac{1}{\mu_n^*}\frac{\partial \mu_n^*}{\partial T} \tag{3.36}$$

Typical values for TC_V in Si, have been determined experimentally to be in the order of $-4.5 \times 10^{-3}\ K^{-1}$ [8], for the same temperature range as above. Thermal variations in Hall voltage may be compensated for by proper variation in biasing conditions. Alternatively, the junction field effect can also be used to compensate for variations in sensitivity as discussed earlier.

3.4.8. Hall Generator Design

It is desired to design the Hall generator for sensing a vertical magnetic field with the following specifications:

- An expected magnetic field range of 0.1 mT to 100 mT,
- Magnetic field frequency of 45 to 325 Hz, inclusive of the 5th harmonic,
- Within specified accuracy for a temperature range of -25°C to 70°C.

With these specifications in mind, it was found that the cross-shaped Hall plate was well suited to the design criteria and specific application. The device is discussed with reference to the different criteria namely, sensitivity, noise performance, offsets, temperature stability, linearity and technological compatibility with standard CMOS processes. The assumption made now is that the chosen process is based upon a standard silicon 1.2 µm CMOS, double metal, double poly process.

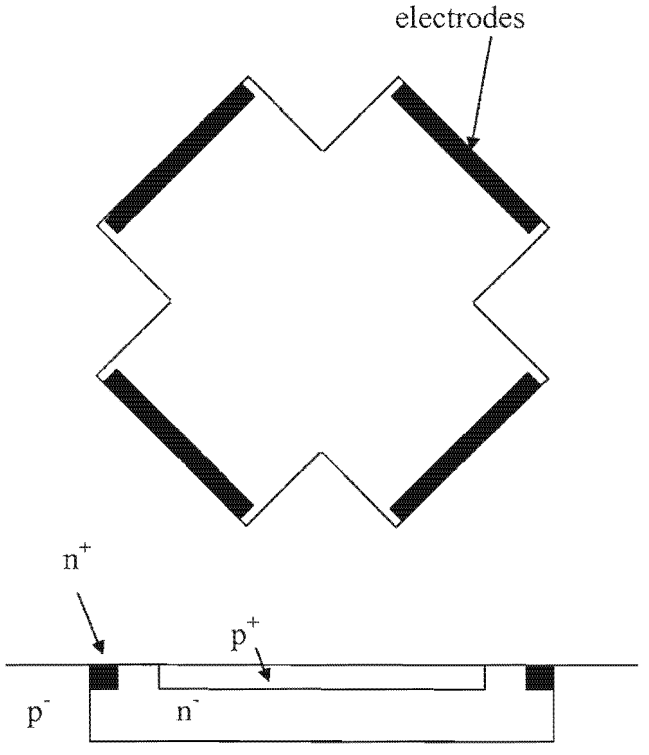

Figure 3.6 Top and cross-section view of the Hall generator geometry

Figure 3.6 shows an illustration of the geometry of the proposed Hall generator. The element is designed as a cross-shaped device. The cross-section view shows how the element is made up. The physical cross consists of an n-well layer inside the low-doped p-type substrate. Highly doped n-type contacts are placed on the n-well edges for ohmic contact into the well according to the layout design rules. Lastly, a strongly doped p-type layer covers the n-well such that a pinched, n-well structure is created. Detailed dimension are given in paragraph 3.6.

3.4.9. Sensitivity and Noise

The choice of geometry of the Hall generator can be greatly influenced by the sensitivity requirements and noise performance of the device. A device with higher sensitivity will produce better SNR performance. This does however result in higher power dissipation in the Hall generator. Investigating the theoretical noise performance of Hall plate generators, it was found that the minimum detection levels in the presence of noise was, $B_{min} \approx 3 \times 10^{-7}$ T @ 100 KHz and $B_{min} \approx 5 \times 10^{-6}$ T @ 1 Hz [27] and is typical for plates biased around 0.5 mA [8, 9]. It is desired to detect minimum magnetic field levels of 0.1 mT in the frequency range of 45 to 325 Hz. This makes the minimum detection levels required an order 10^2 higher than the minimum, low frequency detection limits. Noise will thus have little effect on the performance of the device. It can also be seen that the noise performance of Hall generators improves at higher signal frequencies.

From equation (3.10) it was seen that to maximize the Hall voltage, it was necessary to maximize the biasing current. When designed in optimum ratios, the cross-shaped Hall plate or generator will measure approximately 2 squares between terminals. (see figure 3.12). From experimental data, a pinched n-well resistor shows approximately 1.5 kΩ/ sheet resistance for the given technology. This implies a 3 kΩ resistance between biasing and sensing electrodes. To ensure minimum detection limits remain negligible, a biasing current of 0.5 mA is proposed and is below the plate's maximum power dissipation levels of 6 mW, determined from previous experimental data. Taking into consideration that the n-well sheet resistance may vary up to 20% as well as the need for low power dissipation, a maximum bias current of 300 μA will be implemented. This will also leave enough room for multiple Hall plate implementations without excessive power consumption. Lastly, this ensures that the biasing conditions of the Hall generator can be varied and used as a calibration parameter.

3.4.10. Linearity

Linearity errors are largely dependent upon the difference in contact area (short-circuiting effects) and non-uniformity of the Hall generator material. With this in mind, non-linearity becomes a practical problem that needs to be analyzed specific to the proposed technology being used. Techniques exist for reducing non-linearity such as correct resistive loading of the elements which also become process specific (doping concentrations, dopants etc.). Linearity is expected to be in the range $LE = \pm 0.03$ %. Cross-shaped Hall plates are the most suited to this application with their highly linear characteristics. This is due to the fact that the geometrical design reduces the short-circuiting effects that are the major source for non-linearity.

3.4.11. Temperature

The proposed technology uses donor concentrations of approximately 3×10^{16} cm^{-3}, and is low-doped (n-well). The temperature coefficients are thus expected to be in the order of $TC_I \approx +10^{-3}$ K^{-1} for standard Si at a temperature ranging between –25 °C and 70 °C. Temperature affects both the sensitivity as well as the offset voltage of the device. Sensitivity compensation can be achieved fairly easily through the measurement of chip temperature and varying the bias conditions of the Hall generator accordingly [8]. This will be accomplished through the use of a similar pinched, n-well resistive structure with the same temperature coefficient as the Hall generator. Offset cancellation will take place dynamically using quadrature offset cancellation techniques [4].

3.4.12. Offsets

Once again, offsets are dominated by the specific technology. It was seen that Hall plates generally show small offsets. Offset cancellation techniques will be applied to reduce any offsets inherent in the Hall generator. This once again proves to be a problem to be solved through signal conditioning external to the plate but an attempt should be made to keep offsets to a minimum, through careful design and orientation of the Hall generator itself. It is proposed to place the Hall device in the (110) crystal plane with current flowing in the <110> direction. This minimizes the piezoresistive effects and significantly reduces the offset. Furthermore, a dynamic quadrature offset cancellation technique will be implemented [4] whereby the offset signal is translated to a higher frequency and isolated through filtering.

According to the data given in addendum A and the requirements set out in this chapter, the following parameters were calculated based on equations (3.1) to (3.19).

$\mu_n = 545\ cm^2/V/s$

$\mu_n^* = 625\ cm^2/V/s$

$n = 3 \times 10^{16}\ cm^{-3} = 3 \times 10^{22}\ m^{-3}$

$t_{eff} = 1.17\ \mu m$

$r_n = 1.15$ for Si

$q = 1.6 \times 10^{-19}\ C$

Then from equation (3.10) and equation (3.27) with $G = 1$,

$R_H = 218.75\ \mu V.m/A/T$ and

$\sigma_n = 286\ (\Omega m)^{-1}$

$R_{plate} = 3\ k\Omega$

$S_{RI} = 187.5\ V/A/T$

This data can now be used to configure the simulation model required for the system design.

3.5. SIMULATION

3.5.1. Simulation Model for Hall Plate

The simulation model for the Hall plate model will be based on the model shown in figure 3.4. This model simulates a first order approximation of the Hall plate and can be used for simulating both the sensitivity and offset inherent in the devices. The model is displayed in figure 3.7 and a transient simulation was done to show how the output responds. The model uses voltage controlled voltage sources to represent the magnetic field magnitude and uses a scale factor similar to that of the gain of the Hall plate to transform the "magnetic field" into the Hall voltage. This voltage is then measured across the output terminals Vh_plus and Vh_minus.

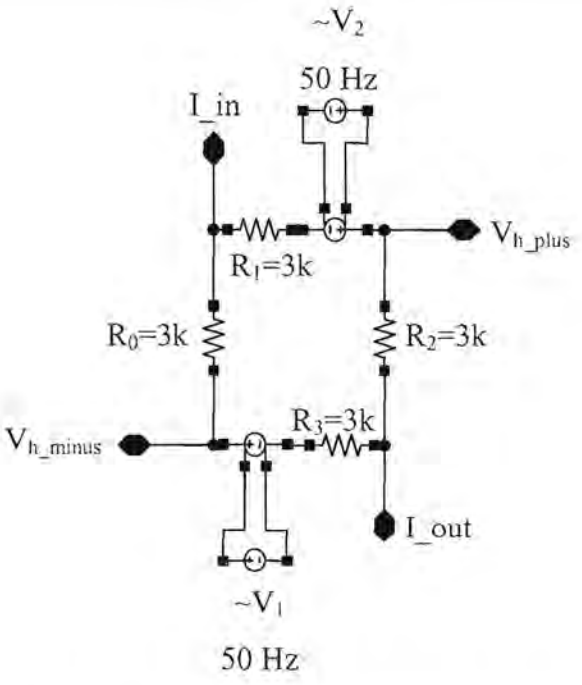

Figure 3.7 Simulation model used for Hall plate

The output simulation is shown in figure 3.8 where it can be seen how each output displays a voltage signal of 3 mV and is 180° out of phase with each other. Taking the difference in the outputs results in figure 3.9 and represents the effective Hall voltage of the Hall generator in the presence of an ac magnetic field biased at 300 µA dc. A peak magnetic field of 100 mT results in an expected output Hall voltage of 5.625 mV_{peak}.

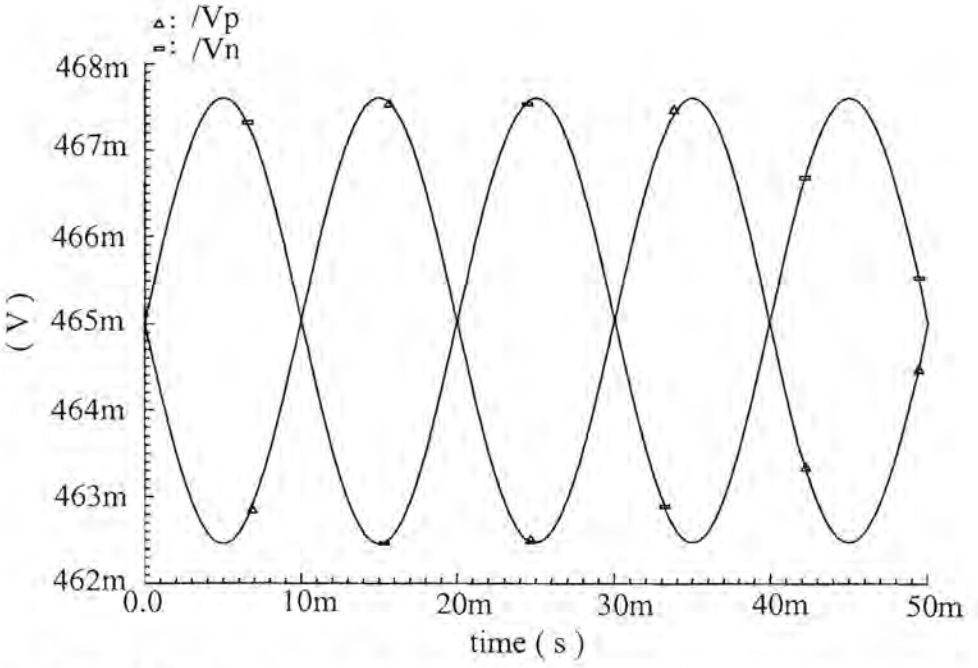

Figure 3.8 Graph displaying the output Voltages of the Hall plate versus time

Figure 3.10 shows the simulation results for a change in the resistance gradient through the Hall plate. The simulation was again based on the model in figure 3.4 and figure 3.7. The results show how much the offset can change for a gradient change of up to 2% between the four corners. This result show that offsets of up to 9 mV or almost 200 mT could result in such extreme cases. Experimental data show that the proposed technology has an average gradient variation of approximately 0.2% thus yielding expected offsets in the range of less than 2 mV or 30 mT. Although this value is small, it suggests an offset line current of about 24 A or 5.3 Kw given an assumed linear transfer of the line current to magnetic field and should thus be compensated for.

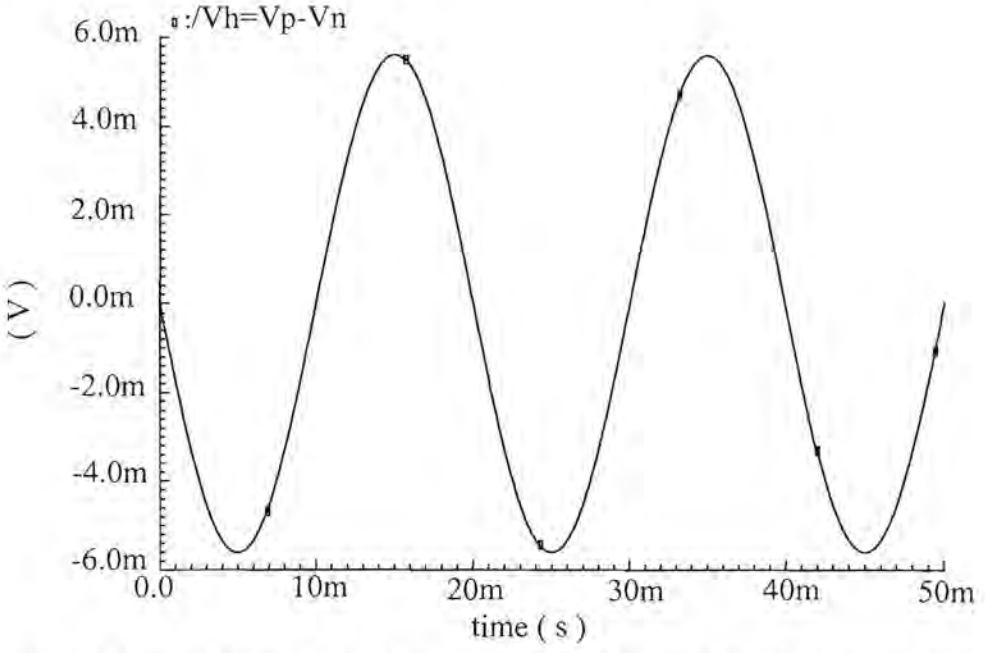

Figure 3.9 Graph displaying the differential output between V_p and V_n versus time.

Figure 3.11 shows the transfer function for the Hall plate as a DC response. The graph consists of two parts namely the upper graph illustrating the differential Hall voltage and the lower Hall voltage illustrating the separate terminal voltages both as a function of the input line current ranging between 0 and 80 A and with the line voltage held constant. Voltage sources were used to simulate the line current in the Hall simulation model, where 1 kV equates to 80 A and 0 V equates to 0 A. The Hall voltage thus represents the consumed active power in the line. It can be clearly seen that the output Hall voltage is a linear function and is directly proportional to the input current when the line voltage is held constant.

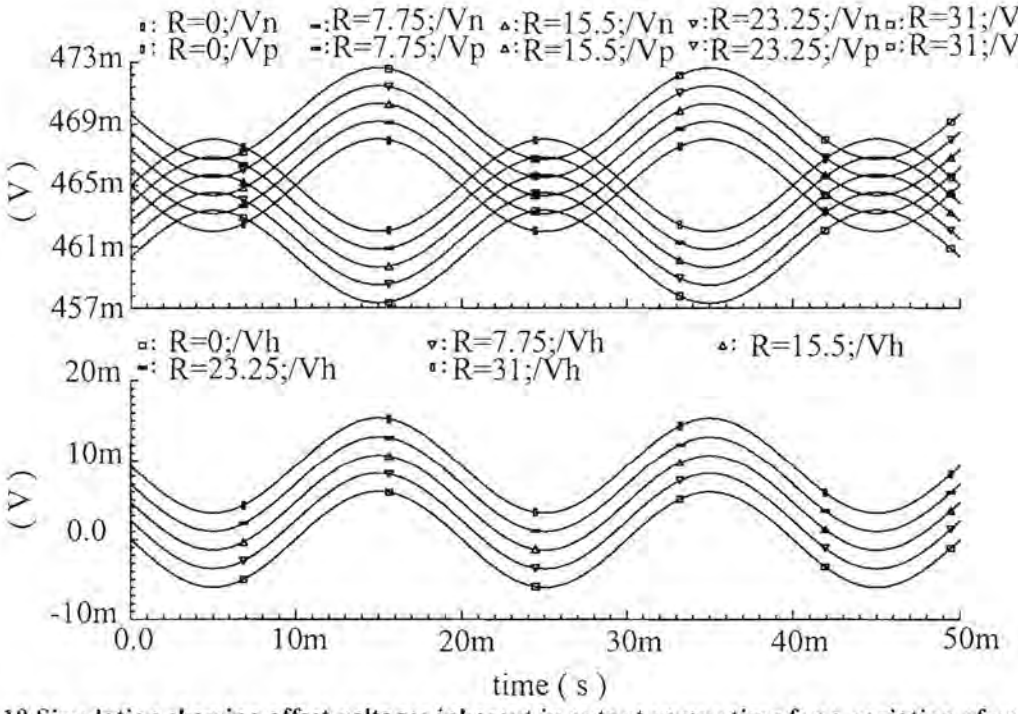

Figure 3.10 Simulation showing offset voltages inherent in output versus time for a variation of up to 2% in resistance gradient

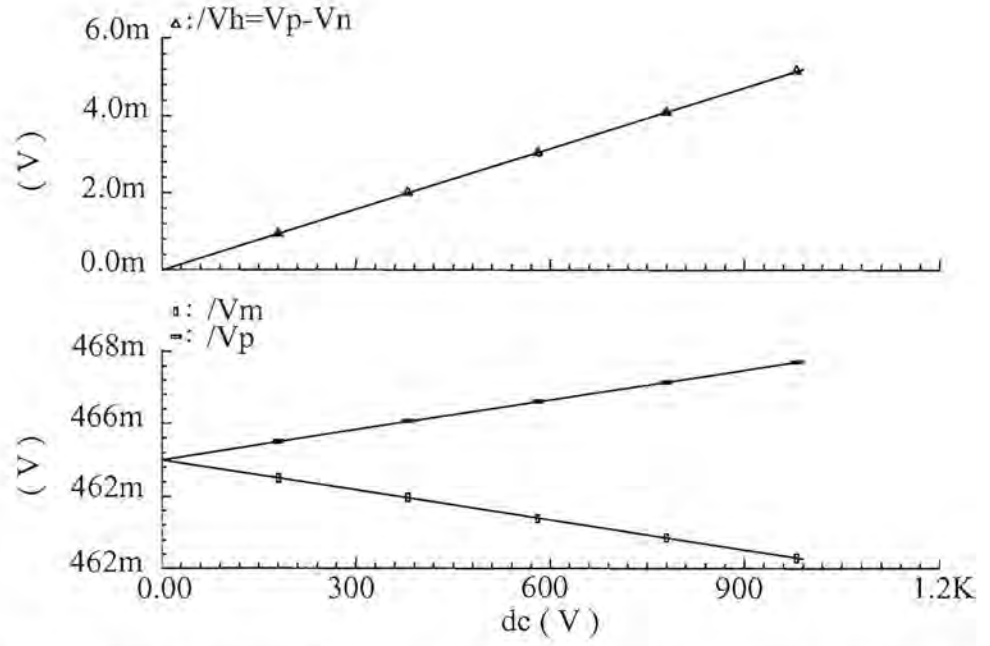

Figure 3.11 Graph showing transfer function of Hall generator with respect to changing line current where 1 kV equates to 80 A

3.6. EXPERIMENTAL VERIFICATION

A Hall effect device was manufactured in the proposed standard CMOS 1.2 µm technology and used to verify all the performance characteristics of the device. This section presents measurements of the electrical and magnetic device parameters of the cross-shaped Hall generator with dimension as illustrated in figure 3.12.

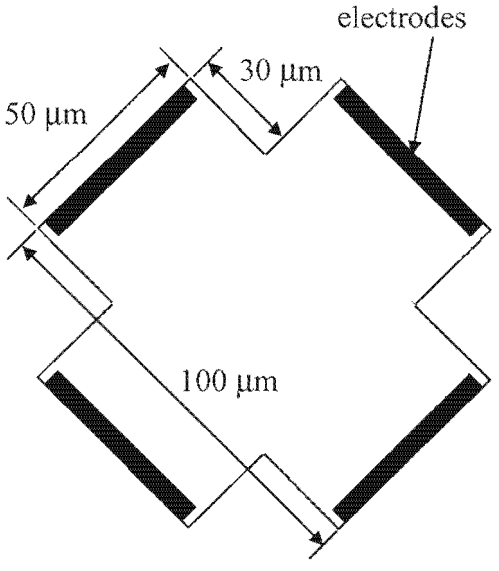

Figure 3.12 Cross-shaped Hall generator illustrating dimensions implemented

Mathematical approximations in paragraph 3.3. and 3.4. are now combined for comparison with physical behavior. Any deficiencies can thus be revealed and discussed and suggestions can be made for rectifying any under performance of the device. The device was tested according to the characteristics set out in paragraph 3.4.8. For most of the test procedure, unless otherwise specified, the characterization of the sensor was done at room temperature using a wire-wound ferromagnetic core as a magnetic transducer providing magnetic flux densities of up to 100 mT.

3.6.1. Sensitivity

The first parameter measured was the sensitivity of the device and to maximize the sensitivity for easier measurement, a biasing current of 1 mA was used. Passing current through the conductor of the wire-wound ferromagnetic core generated the magnetic field required for the measurements. A total of 12 devices were measured and the results of 4 chosen at random are presented in table 3.1 and figure 3.13.

Table 3.1 Measured sensitivity for cross-shaped Hall plate

Sensor number	Measured sensitivity S_{RI} (V/A/T)
1	158.75
2	158.33
3	157.92
4	158.75

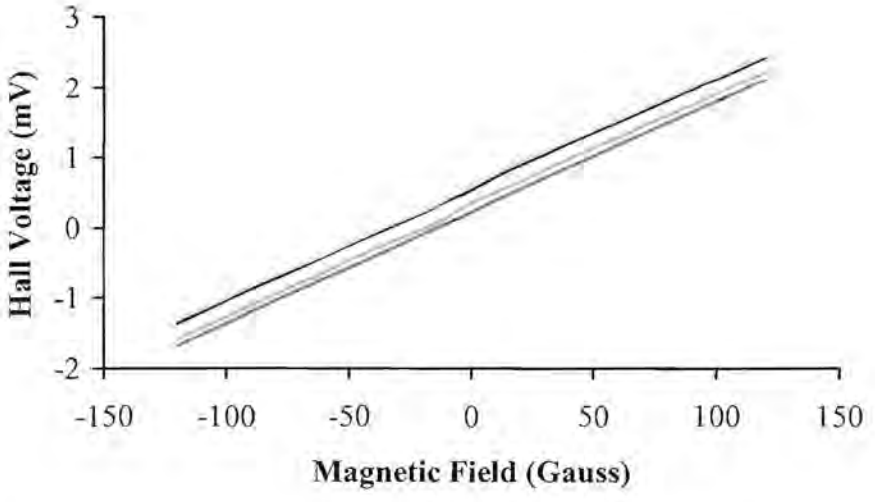

Figure 3.13 Graph showing the Hall voltage versus magnetic field of 4 independent samples

From equation (3.27) the geometrical correction factor could be determined when compared to an ideally calculated sensitivity i.e. $G = 1$. This factor was determined to be $G = 0.845$. Figure 3.14 shows the geometrical factor for a cross-shaped plate with $m = \frac{\theta_H}{\pi/2}$, and $\lambda = \frac{c}{b}$, where c = total electrode length and b = plate boundary length [8]. From figure 3.12, these values are determined as $\lambda = 0.455$, and $m \approx \frac{0.07}{\pi/2}$ (with θ_H small i.e. 2°), this factor is justified.

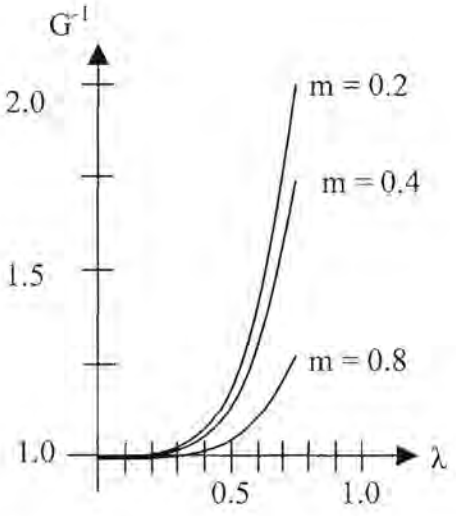

Figure 3.14 Graph showing the reciprocal value of the geometrical correction factor for the cross-shaped Hall plate

The minimum detection level was determined by the available laboratory equipment and a 10 μV change was detectable. From equation (3.27) it can be seen that this results in a magnetic field, current product of $IB = 6.3 \times 10^{-8}$ or 2.1 Gauss @ 300 μA. When translating this variable into measured current, 2.1 Gauss represents a resolution of 70 mA. Once amplified, this resolution will be increased by the gain factor incorporated. It will thus be necessary to increase the bias current to 350 μA_{peak} to compensate for this loss in sensitivity resulting from the influence of the geometrical correction factor.

3.6.2. Offsets

Table 3.2 shows the measured offsets of the 4 devices from the same wafer. Offsets were measured in two biasing directions separated by 90° as shown in figure 3.15 in the absence of a magnetic field. This will later form the dynamic behavior behind the offset cancellation scheme. These input offsets were measured for different biasing currents and the need for dynamic offset cancellation techniques was established here as the offset shows bias current dependence. The devices all showed similar offset properties and the reason for this is that the devices were all from the same wafer. This is also evident from the same polarities displayed in each sensor. As the biasing current is relatively small, the opposite polarity offsets are identical. These will however show signs of deviation under large current bias conditions.

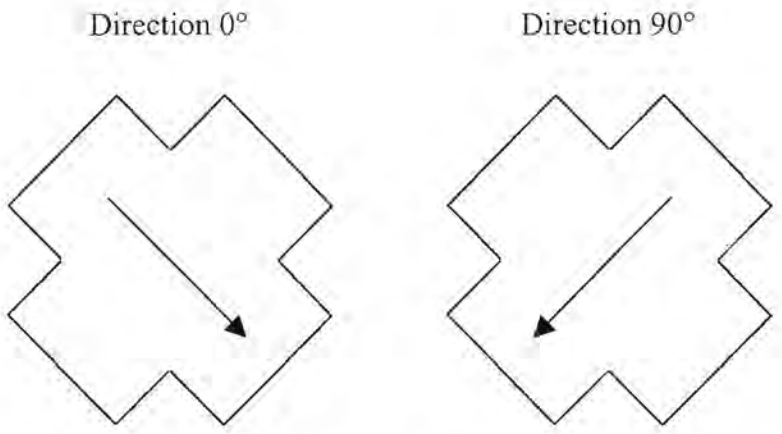

Figure 3.15 Biasing conditions showing 90° rotations in current

Table 3.2 Measured offsets under varying biasing conditions

Sensor Number	Biasing current (μA)	Direction 0° (mV)	Direction 90°
1	100	0.02	- 0.02
	200	0.03	- 0.03
	300	0.04	- 0.04
2	100	0.03	- 0.03
	200	0.04	- 0.04
	300	0.06	- 0.06
3	100	0.04	- 0.04
	200	0.06	- 0.06
	300	0.09	- 0.09
4	100	0.01	- 0.01
	200	0.02	- 0.02
	300	0.03	- 0.03

3.6.3. Linearity Errors

Linear regression models served the basis for determining the linearity and the results are shown in figure 3.16. It can be seen that $R^2 \approx 1$. This was expected as the cross-shaped geometries have high performance in this respect [26]. Furthermore, it must be mentioned that only 10 μV changes were measurable and this in itself causes a significant measuring inaccuracy.

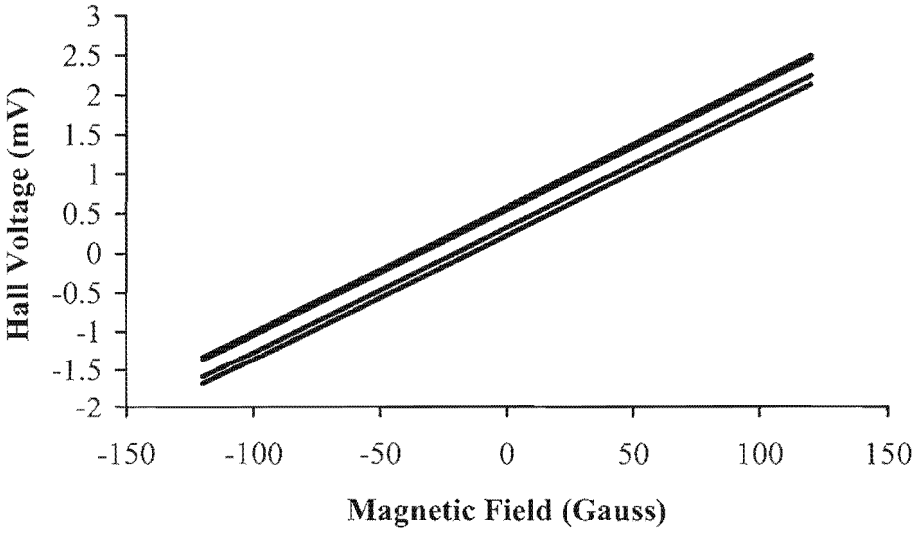

Figure 3.16 Graph showing linear regression models of the Hall generator transfer functions versus magnetic field

Table 3.3 shows the linear first-order transfer functions for devices 1 to 4 presented in figure 3.13 respectively where V, represents the predicted Hall voltage in mV for a given magnetic field strength of B Gauss. The slope indicates the sensitivity of the device in V/G and the constant offset in mV at the given bias conditions. The R^2 factor represents how well the model defines the experimental data where $R^2 = 1$ represents and ideal linear fit. As seen from this, the sensors appear to show a high degree of linearity and will be fit for the application.

Table 3.3 Table showing first-order transfer functions determined through linear regression

	Sensor 1	Sensor 2	Sensor 3	Sensor 4
Transfer function (mV)	$V_1 = 0.0159B + 0.5488$	$V_2 = 0.0159B + 0.2276$	$V_3 = 0.0159B + 0.5847$	$V_4 = 0.0159B + 0.3282$
R^2 value	$R^2_1 = 0.9999$	$R^2_2 = 1$	$R^2_3 = 0.9998$	$R^2_4 = 0.9999$

3.6.4. Temperature Behavior

The experiment was divided into two parts, the first to test the influence of temperature on the offset voltage and the second to test the influence of temperature on the sensitivity. The

results showed that the sensitivity had a temperature coefficient of $TC_I \approx +3 \times 10^{-3}\ K^{-1}$ for a temperature range of –25 °C to 70 °C and was as a direct result of a change in the Hall factor as explained in paragraph 3.4.7. The resultant effect was a directly proportional change in the sensitivity as well as the offsets. Once again the importance of dynamic offset cancellation is demonstrated as it can be seen how the offset varies with temperature. The variation in offsets with respect to temperature displayed a positive temperature coefficient. As the offset will be dynamically measured and cancelled, its magnitude has no effect. Compensation for the change in sensitivity is however of great importance as a TC_I of $+3 \times 10^{-3}\ K^{-1}$ represents a sensitivity change of 48 V/A/T across the required temperature range. Furthermore, this temperature coefficient is not completely linear and thus compensation using the same pinched, n-well resistive structure is of the essence and will be implemented in the amplifier gain stages.

3.7. CONCLUSION

In this chapter the galvanomagnetic properties of silicon leading to the formulation of the Hall effect was presented as a basis for designing, simulating and verifying the Hall generator. After a brief introduction to Hall effect based power sensors, the galvanomagnetic transport equations were discussed. From these equations it was found that for a given technology, the biasing current is the only parameter having influence on the Hall voltage. Following this, the bulk Hall effect device in silicon was presented as a basis for measuring the performance of other geometrical derivatives. The device was then analyzed in terms of electrical performance characteristics comprising of sensitivity, noise, offset characteristics, linearity and temperature behavior. These characteristics were then followed as the design procedure for the Hall generator along with the given requirements and technology data. A simulation model was developed and simulated so as to study the basic behavior of the sensor. A physical device was manufactured for experimental verification and the results of the proposed mathematical approximations agree well with the physical results. The knowledge in this chapter will be used in subsequent chapters for the design of the support circuitry required such as to complete a fully functional device.

4. SIGNAL PROCESSING CIRCUITRY

4.1. INTRODUCTION

The successful extraction of the information superimposed on the Hall voltage requires for the correct analog signal processing circuits to be developed. The objective of analog circuit design is to transform the specifications into hardware capable of attaining these specifications. As integrated circuit design is a technology driven activity, it will be necessary to base all the designs specifically with reference to the proposed technology. The Hall voltage is an extremely small signal and contains both DC and AC noise. For this reason it will be necessary to focus the design procedure to contain the relevant voltage to current converters, temperature independent voltage and current referencing circuitry, amplification circuits, offset compensation circuitry and filtering elements necessary for implementation of the power sensor. Lastly, as the device is intended for use within watt-hour meters, the mechanical requirements will be discussed for completion.

This chapter will thus be divided into four major categories covering the design aspects of the aforementioned signal processing circuits. The discussion will start with temperature independent voltage and current referencing circuitry, as most analog circuits require biasing usually derived from the referencing circuitry. This will then be followed with the design of the voltage to current converter as required for biasing the Hall plate. The amplifiers follow, along with the offset cancellation and filtering circuits. The four categories will be grouped as follows:

- Temperature independent voltage and current referencing circuitry,
- Voltage to current converter,
- Amplifier circuits,
- Offset cancellation and filtering.

4.2. TEMPERATURE INDEPENDENT BIASING

Analog circuits extensively make use of voltage and current references. These references are dc quantities that are independent of process parameters and supplies and show a well-defined behavior regarding temperature. Many circuits rely on this for proper functionality for example the gain of a differential pair is directly dependant on its biasing current. For this

reason, this section focuses on the design of a stable biasing source that can be used for biasing other analog devices within the power sensor. The core of the biasing source will be based on well-established "bandgap" techniques [28]. The section starts off with a basic explanation of the temperature independent reference as will be implemented in the biasing source. The bias source will then be presented and will be used to bias all subsequent devices.

4.2.1. The Bandgap Reference

The bandgap principle is based on the fact that if two quantities with opposite temperature coefficients (TCs) are added with proper weighting, the resultant displays a zero TC. In equation (4.1) α_1 and α_2 are chosen such that equation (4.2) is satisfied.

$$V_{ref} = \alpha_1 V_1 + \alpha_2 V_2 \tag{4.1}$$

$$0 = \alpha_1 \frac{\partial V_1}{\partial T} + \alpha_2 \frac{\partial V_2}{\partial T} \tag{4.2}$$

The characteristics of bipolar transistors have proven to be the most reliable in terms of reproducibility for producing both positive and negative TCs. These techniques have also been successfully implemented in CMOS technology.

Negative-TC Voltage

The negative TC stems from the forward bias voltage of a pn-junction diode. A diode connected bipolar transistor can perform this function. Equation (4.3) defines a diode-connected transistor's collector current and from this we can define the base-emitter voltage as a function of temperature.

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{4.3}$$

Now,

$$V_T = \frac{kT}{q} \tag{4.4}$$

and

$$I_S \propto \mu k T n_i^2 \tag{4.5}$$

where,

$$\mu \propto \mu_0 T^m \tag{4.6}$$

and $m \approx -3/2$. Also

$$n_i^2 \propto T^3 e^{\frac{-E_g}{kT}} \tag{4.7}$$

with $E_g \approx 1.12$ eV, the bandgap energy of silicon. Solving for V_{BE} in equation (4.3), substituting and taking the derivative with respect to temperature yields the temperature coefficient for the diode as in equation (4.8) with a constant collector current is assumed.

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - \frac{E_g}{q}}{T} \tag{4.8}$$

As can be seen, the temperature coefficient shows that V_{BE} itself is dependent on temperature thus a zero TC can only be achieved at a specific temperature. This is illustrated later.

Positive-TC Voltage

If two identical transistors i.e. $I_{S1} = I_{S2}$, are biased at collector currents of nI_0 and I_0 and their base currents are negligible, then the difference between the base-emitter voltages exhibits a positive-TC as in equation (4.10).

$$\Delta V_{BE} = V_T \ln n \tag{4.9}$$

and

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n \tag{4.10}$$

Where k, is Boltzmann's constant. This TC is independent of temperature or the collector currents as long as high-level injection does not occur.

These coefficients can now be combined to develop the desired reference according to equation (4.2). The base-emitter voltage of a vertical parasitic PNP bipolar transistor at 300 K

for the proposed technology is V_{BE} = 630 mV @ I_C = 12 µA. Substituting these values in equation (4.8), the temperature coefficient is calculated as –1.84 mV/°K. Also, from equation (4.10), $\partial V_T/\partial T$ = +86.17 µV/°K. Substituting these results into equation (4.2) and choosing α_1 = 1 at room temperature, then ($\alpha_2 \ln n$)(0.08617 mV/°K) = 1.84 mV/°K. Thus $\alpha_2 \ln n \approx 21.4$ and

$V_{REF} \approx V_{BE} + 21.4V_T \approx 1.16$ V @ 300K.

The circuit that will realize this function is shown in figure 4.1. In the circuit we can see that M4 and M5 keep their source potentials at the same quantity. To achieve this, M2 adjusts its drain potential such as to compensate for the difference in the currents in the two branches thus balancing the circuit. This forms part of the positive-TC component. The potential established at the gate of M1 and M2 are then added to another proportional to absolute temperature (PTAT) base-emitter voltage namely $I_{D3}R_2$, resulting in equation (4.11).

$$V_{ref} = V_{BE3} + \frac{R_2}{R_1} V_T \ln n \qquad (4.11)$$

Thus for α_1 = 1 and (R_2/R_1)ln $n \approx 21.4$, a ratio of approximately 9.28 results for R_2/R_1. As these resistors will be implemented using n-well resistors, it is necessary to keep them as small as possible such as to minimize consumed area. For repeatability, these resistors should be larger than 5 kΩ for the given technology and to maximize matching, a resistance of 90 kΩ and 10 kΩ is chosen. Although resistors exhibit incredibly high tolerances in IC's, their ratios are very well matched and matching tolerances lower than 1 % can be achieved using many different layout techniques. The technique that will be used here for all resistances will be that of the common centroid principle and thus the resistors will be broken into 10 kΩ strips and placed using this principle. The switches S1 to S6 are used for the starting up of the circuit. As there are two possibilities for reaching equilibrium within the circuit, namely zero and the bandgap voltage, it is necessary to "kick start" the circuit so as to ensure that the equilibrium point is approached from the highest supply rail. This will then force the first stable point reached to be that of the bandgap voltage. In principle, the switches are kept closed for a few milliseconds longer during power up and will be performed by a standard cell from the technology library specifically designed to perform this operation. The switches will be a minimum size of 4µm/1.5µm. A 9 pF capacitor is added for stability purposes. The transistors are designed such that they are capable of carrying the current expected in the circuit.

Furthermore, all PMOS transistors have double the width/length ratio as compared to the NMOS transistors to compensate for the difference in carrier mobility between them.

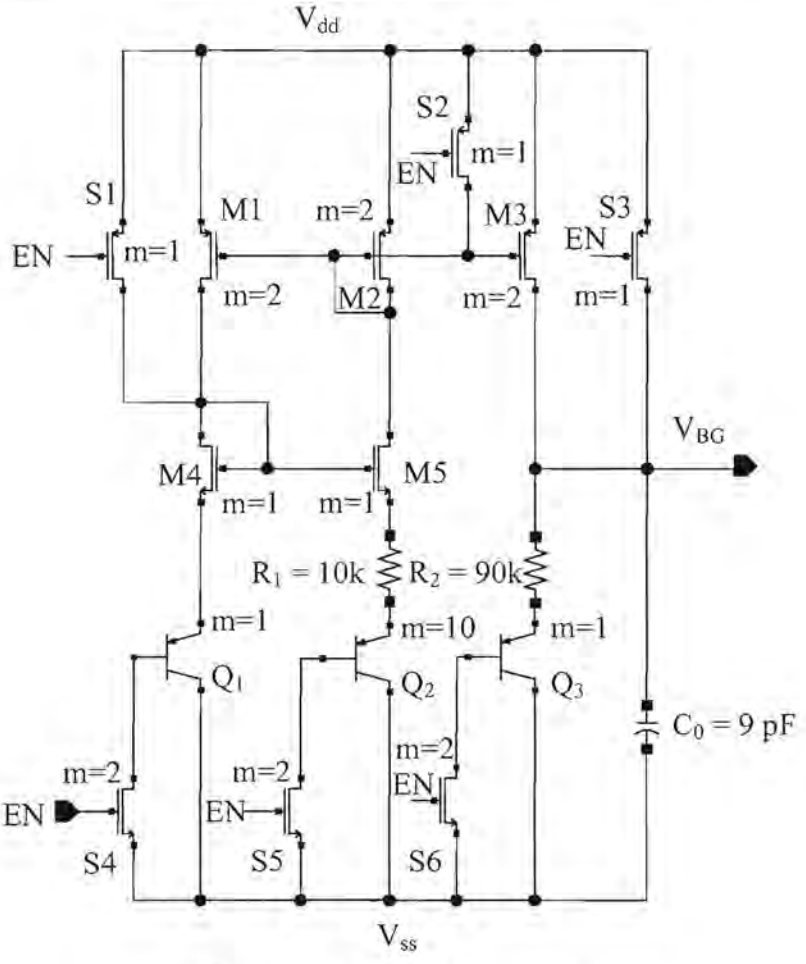

Figure 4.1 Bandgap reference circuit

4.2.2. The Current Reference

The current reference circuit is based on the current mirror principle [28, 29]. The ideal current reference (source or sink) reproduces a reference current that is equal in magnitude and displays an infinitely high output resistance. As we are working with real quantities and technological parameters, a current reference circuit displays finite small-signal output impedance and an output current close to the reference current. Furthermore, the output voltage at the current reference node in which this relation is valid is also not rail-to-rail.

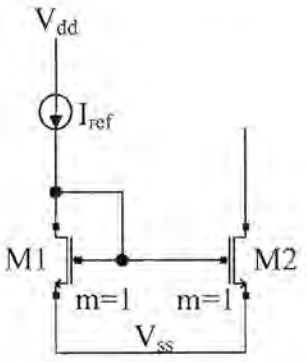

Figure 4.2 Simple current mirror

Figure 4.2 shows the architecture of a simple current mirror. The current ratio between M1 and M2 is derived from the drain current relationship for a transistor in saturation and is shown in equation (4.12) and (4.13). If the gate voltages are kept equal, the current through each transistor will be equal if the process parameters are closely matched and the width/length ratio is equal. Furthermore, it can be seen that it is possible to scale the current between the transistors simply by varying the width/length ratio.

$$I_D = \frac{k}{2}\frac{W}{L}\left(V_{gs} - V_t\right)^2 \qquad (4.12)$$

$$\frac{I_{D1}}{I_{D2}} = \frac{k_1}{k_2}\left(\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}}\right)\frac{\left(V_{gs1} - V_{t1}\right)^2}{\left(V_{gs2} - V_{t2}\right)^2} \qquad (4.13)$$

The output impedance is taken at the drain of M2 and is given according to the small signal analysis model as

$$r_{out} = \frac{1}{g_{ds2}} \approx \frac{1}{\lambda I_{D2}} \qquad (4.14)$$

From equation (4.14) it is seen that the output impedance is dependent on the channel length modulation factor of the process. Making the length of the transistor somewhat larger than the minimum specified size of the transistor will effectively reduce this effect. As the proposed technology uses a minimum width of 1.2 µm, experimentation has shown that a length of at least two to three times more than this is sufficient to reduce this effect such that it is

negligible. Figure 4.3 show the proposed current referencing circuit and are based on the more improved cascode configuration. This implies that the output impedance is significantly improved by a factor $g_{m\_out}r_{ds\_out}$, as seen in equation (4.15).

$$r_{out} = \frac{g_{m\_out}r_{ds\_out}}{g_{m\_out\_old}} \qquad (4.15)$$

The stability of the current source is thus significantly increased. The circuit uses an operational amplifier to generate an accurate reference voltage according to the bandgap reference voltage. This voltage is then applied to an external resistance according to Ohm's law to generate an accurate reference current that will be mirrored into all subsequent devices. In doing so, the high tolerances of on chip resistors are eliminated and the possibility for trimming and calibrating the system is created. In an attempt to keep the consumed power low, the biasing current was chosen to be 25 µA and is a figure that has yielded satisfactory lower power design results for the given 1.2 µm technology. The circuit was designed for generating a current of 12.5 µA, which will then be scaled up by a factor of two. This was done so as to minimize the wasted power consumed by the primary mirror circuit. Transistors M12, M13, M14 and M15 will thus generate the necessary gate voltages needed to bias all transistors in the other devices and will take on a similar cascode configuration.

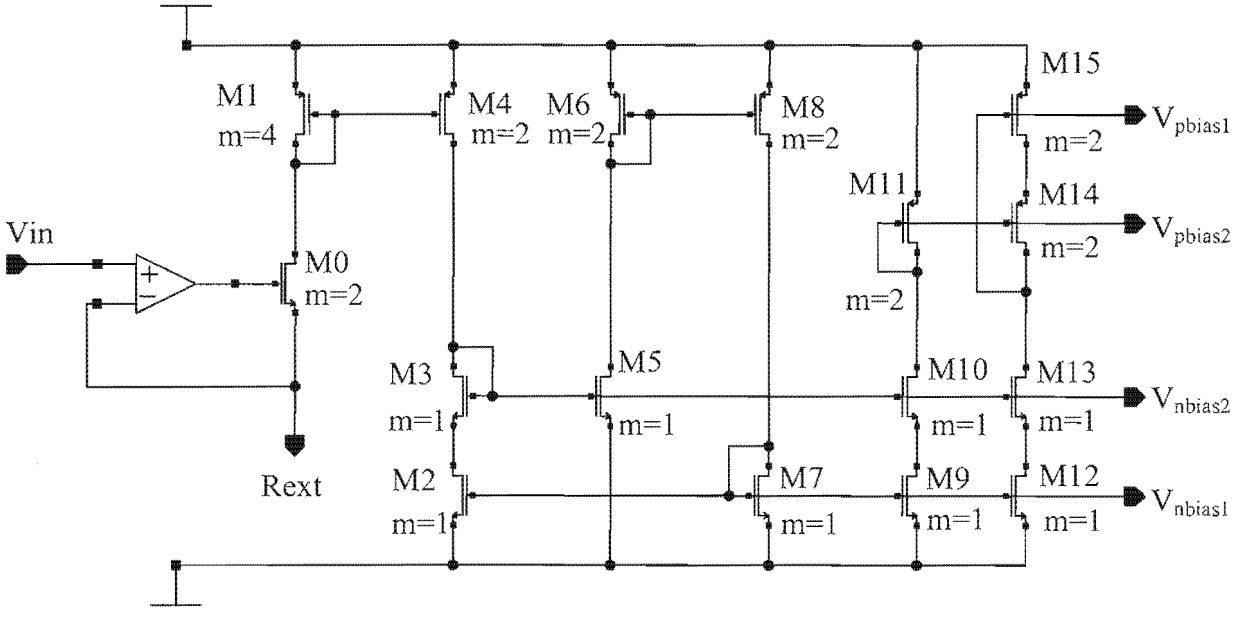

Figure 4.3 Current reference generator

The circuit has 2 inputs and 4 outputs. The first input V_{in}, will use the bandgap voltage as input. The operational amplifier in figure 4.3 will be used to create a virtual short circuit for the external resistor connected to the second input, R_{ext}. This resistor must be selected such that a current of 25 µA flows through it. Following simple Ohm's law calculations with a bandgap voltage of 1.16 V, its value will be approximately 46.4 kΩ. Taking operational amplifier input offsets into account, this resistor value can be calibrated for a 25 µA current flow.

4.3. VOLTAGE TO CURRENT CONVERTER

Voltage to current conversion is necessary so as to bias the Hall generators with a current directly proportional to the line voltage with high accuracy but more important stability. An instrumentation amplifier configuration will be used with strong output transistors. This is to ensure enough current driving capability for biasing the Hall generator. Figure 4.4 shows the configuration along with its equivalent symbol. An increase in potential at the non-inverting input results in a larger negative signal current i_s, at the $-i_{out}$ node. This is due to a larger differential voltage across R_1 and consequently the current through it. As the output current is simply a mirrored sample of this current with a larger ratio, the differential signal current follows the current through R_1.

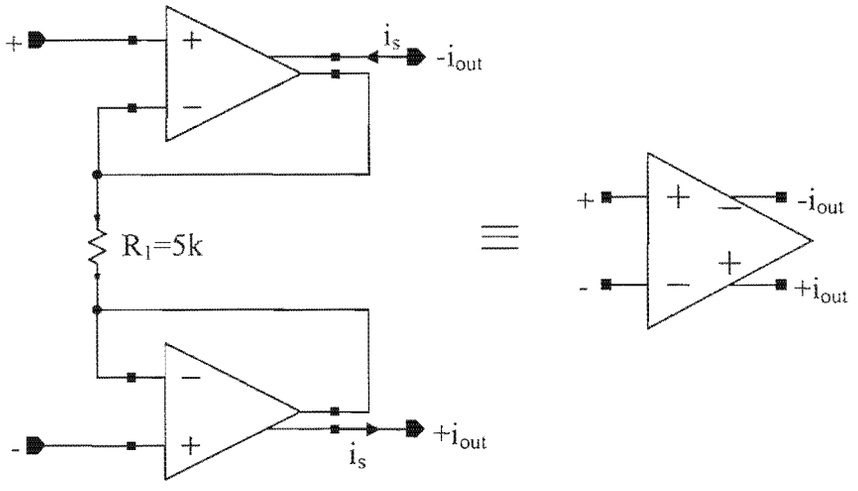

Figure 4.4 Voltage to current converter used for biasing the Hall generators

The external voltage divider network must be designed such that the saturation limit of the operational amplifier is not exceeded. The architecture is used such as to minimize offsets as well as lowering the sensitivity resulting from the changing Hall generator resistance due to process variations. R_1 will be implemented using a poly-silicon resistor to reduce temperature

dependencies in comparison to n-well resistors. The operational amplifiers will be biased using the temperature compensated current bias circuit. Simulation verification is the same as for the output instrumentation amplifier. The circuit functionality will be given in more detail in chapter 5.

4.4. AMPLIFIER

The main criteria for the operational amplifier are stability and linearity. As the system will work with low frequency (≤ 325 Hz), it will not be necessary for a high slew rate specification. The design principles used will now be discussed. The detailed design is given in addendum B.

4.4.1. Operational Amplifier Architecture

Operational amplifiers are built up from operational transconductance amplifiers (OTAs) [28, 29]. An OTA can be seen as a voltage controlled current source with a transfer function of $i_{out} = g_m v_{in}$, with a differential input voltage. Figure 4.5 shows the symbol as well as the two possible configurations for an OTA. Operational amplifiers can thus be realized using these building blocks.

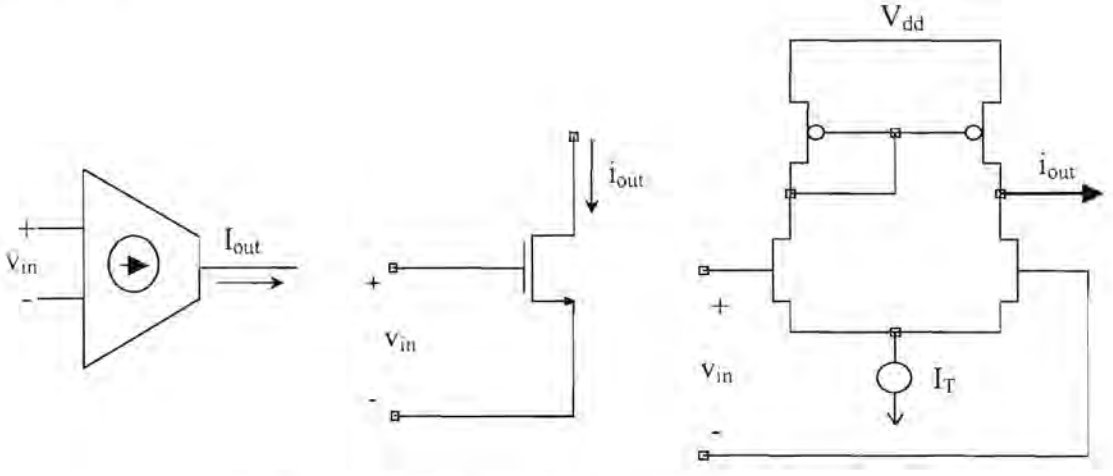

Figure 4.5 Different configurations for OTAs

The architecture for such a two-stage operational amplifier is shown in figure 4.6. The reason for multi-stage operational amplifiers is due to the fact that a single stage cannot yield useful gain by itself as required for the open-loop gain of an operational amplifier. Thus more than one stage is used. Due to high frequency poles being introduced, anything more than two stages will yield closed-loop instability. The configuration used in figure 4.6 is thus a standard

architecture. The first stage is a differential input, single ended output stage with a transconductance of g_{m1}. Its duty is to provide a differential input relatively immune to common mode inputs, high input resistance and provide some voltage gain as a single-ended output. It drives a single-ended input/output stage. This second stage is usually that of a common source stage that provides a large voltage gain. The final stage is simply a voltage follower that is capable of driving resistive and capacitive loads. This is to prevent the output stage from loading the gain stage.

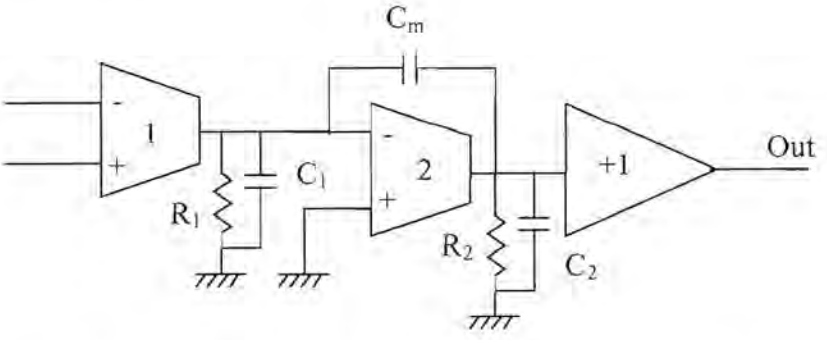

Figure 4.6 Single ended output, two-stage operational amplifier

A suitable MOSFET circuit diagram is shown in figure 4.7. R_1, C_1, R_2, C_2 represent the resistances and capacitances of the connected node at the output of each OTA.

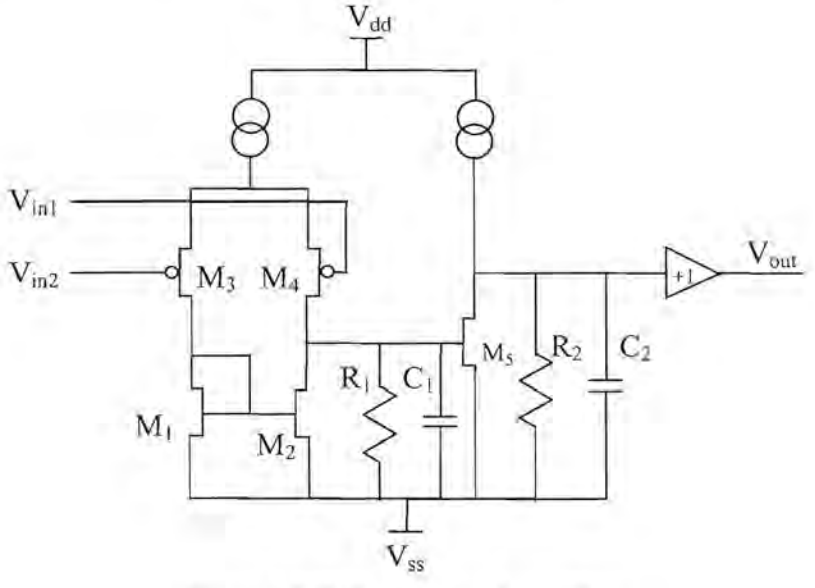

Figure 4.7 MOS operational amplifier

At low frequency, the capacitive loading of each input stage is not of significance. The resistors R_1 and R_2 are the output resistors of each stage respectively where;

$$R_1 = r_{op1} \,||\, r_{on1} \tag{4.16}$$

and

$$R_2 = r_{op2} \,||\, r_{on2} \tag{4.17}$$

Here, r_{on} an r_{op} is the small signal resistances of the two output transistor of each OTA stage.

The low frequency gain of the circuit is thus:

$$A_V = (g_{m1}R_1)(g_{m2}R_2)(1) \tag{4.18}$$

M_1 to M_4 is the first stage, M_5 the second followed by the buffer. If v_{in2} is increased in potential, the PMOS has a smaller gate source driving voltage and this results in the transistor to conduct less. As the current in M_1 is equal to that of M_3, the voltage at the drain of M_1 decreases. This results in a decrease in current through M_2 (mirror). This decrease in current raises the potential at the drain of M_2. The voltage then increases the gate source voltage of M_5 causing it to conduct more strongly. The drain voltage of M_5 thus decreases and is buffered by the unity gain stage. The net output voltage thus decreases as a result of the increased potential at v_{in2}. This input is thus referred to as the inverting input. A similar analysis on v_{in1} will show an increase in the output voltage for an increase in the input voltage and is similarly referred to as the non-inverting input.

4.4.2. Frequency Response

Figure 4.8 shows the open-loop transfer function of an operational amplifier. It can be seen at low frequencies, that the operational amplifier yields a high gain given by equation (4.18). As the frequency increases however, the poles introduced by the load capacitors between each stage become more significant. Good design practices yield two dominant poles through the capacitive loading between each stage. Important information can be retrieved from the open loop transfer function.

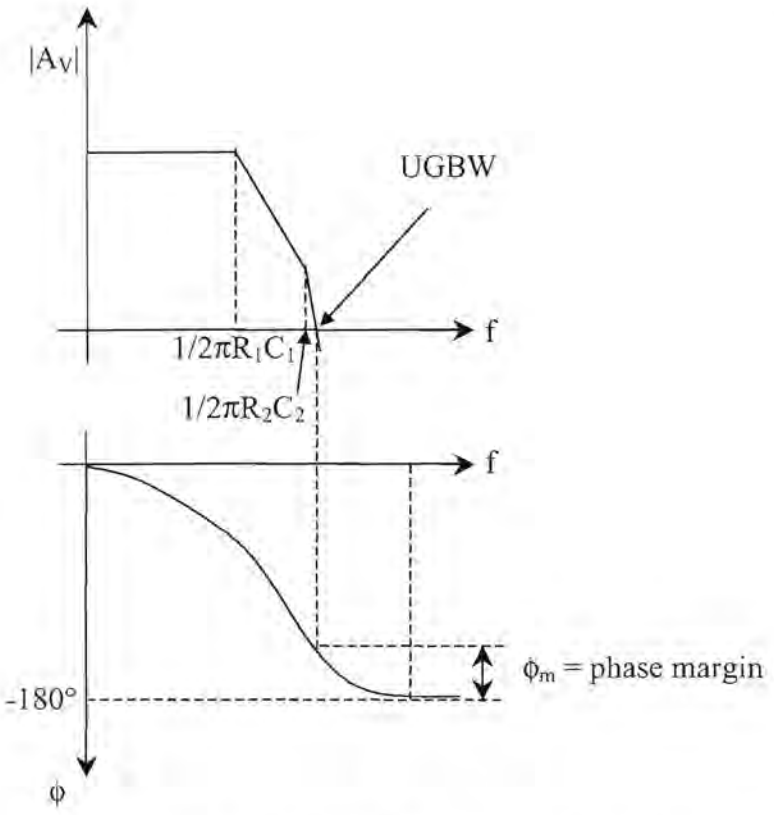

Figure 4.8 Bode diagrams of the open-loop transfer function

The first is the two poles and their relative frequencies at which they occur and are given by equation (4.19).

$$A_V = (g_{m1}Z_1)(g_{m2}Z_2) = \frac{g_{m1}R_1 g_{m2}R_2}{(1 + sC_1R_1)(1 + sC_1R_2)} \quad (4.19)$$

The 0 dB cross point is called the unity gain bandwidth. Equation (4.20) gives the gain bandwidth product.

$$G_{BW} = A_V . f \quad (4.20)$$

Typical operational amplifier circuits contain many poles. In folded-cascode topologies, for example, both the folding node and the output node contribute poles. Thus, operational amplifiers must usually be "compensated" so that their open-loop transfer function is

modified such that the closed-loop circuit is stable and the time-response of the system is well behaved.

The need to compensate a circuit is due to the fact that the gain crossover point is not well before the phase crossover point. It is thus possible to achieve stability by either minimizing the overall phase shift thus moving the phase crossover *out* or dropping the gain thus pushing the gain crossover *in*. The first approach is an attempt to minimize the number of poles in the signal path by proper design. Since each additional stage in an operational amplifier adds at least one pole, the number of stages must be minimized and thus results in low voltage gain and/or limited output swings. The second approach maintains low frequency gain and output swing but reduces bandwidth due to the gain falling to lower frequencies.

Considering figure 4.6 as an example, though there are high frequency poles due to the transistors (small signal impedances), the output resistance of the amplifier is much higher than the small signal resistance seen at the other nodes in the circuit. It is obvious thus that even with a moderate capacitive load on the first stage, the first pole $\omega_{p,1}$ is closest to the origin and also usually sets the 3-dB bandwidth thus making it the dominant pole. The second most dominant pole is due to C_2 and is usually closer to the unity gain bandwidth point and if not so, the aim is to get it there. If C_1 were to increase, i.e. by adding a parallel capacitor to the input of the second stage, it is evident that it is possible to move the most dominant pole closer to the origin. This results in better stability but at the price of a loss in gain at upper frequencies as well as reduction in bandwidth. A more ideal approach is to split the poles from each other such that stability is obtained while keeping bandwidth. This is done using the Miller capacitor effect technique. By adding a capacitor across the input and output of the second stage, two dominant poles are produced, the first close to the origin, the second close to the unity gain crossover point. The resultant bode plots are shown in figure 4.10.

A problem however is that a zero is also introduced but its effects will be discussed later. Using Kirchoff's current laws as well as the assumption that the two dominant poles are widely spread from each other (which is exactly what we want to achieve), from figure 4.9 it can be shown that the two poles are described by the following equations:

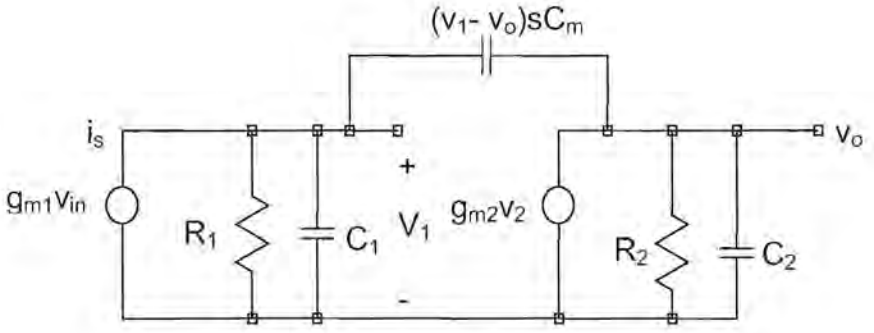

Figure 4.9 Small signal equivalent of the second OTA stage

$$i_s = \frac{v_1}{R_1} + v_1 sC_1 + (v_1 - v_o)sC_m \qquad (4.21)$$

$$(v_o - v_1)sC_m = g_{m2}v_1 + v_o sC_2 + \frac{v_o}{R_2} \qquad (4.22)$$

Eliminating v_1 yields

$$\frac{v_o}{i_s} = \frac{g_{m2}R_1R_2(1 - \frac{sC_m}{g_{m2}})}{\{1 + s[(C_m + C_2)R_2 + (C_1 + C_m)R_1 + g_{m2}R_2R_1C_m] + s_2R_2R_1(C_1C_2 + C_mC_2 + C_mC_1)\}} \qquad (4.23)$$

The previous equation consists of a numerator (zero) and denominator (poles). Rewriting the denominator yields

$$D(s) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s_2}{p_1p_2} \qquad (4.24)$$

thus

$$D(s) \approx 1 - \frac{s}{p_1} + \frac{s_2}{p_1p_2} \qquad (4.25)$$

The Effects of the Poles

As the poles are widely spread, p_1 reduces to equation (4.26).

$$p_1 = \frac{1}{(C_m + C_2)R_2 + (C_1 + C_m)R_1 + g_{m2}R_2R_1C_m} \quad (4.26)$$

The DC gain of the second stage is high and thus

$$p_1 = \frac{1}{g_{m2}R_2R_1C_m} \quad (4.27)$$

and

$$p_2 = \frac{g_{m2}C_m}{C_1C_2 + C_m(C_1 + C_2)} \quad (4.28)$$

This is true if the dominant poles are widely separated and thus C_1 and C_2 can be ignored. At high frequencies, C_m dominates the frequency response as it short circuits the second OTA and as a result,

$$v_o = -\frac{g_{m1}v_{in}}{sC_m} \quad (4.29)$$

and the high frequency response (from the first pole) is given by equation (4.30) and the low frequency gain response by equation (4.31).

$$|A_V| = \left| \frac{v_{out}}{v_{in}} \right| = g_{m1}\omega C_m \quad (4.30)$$

$$|A_v| = (g_{m1}R_1)(g_{m2}R_2) \quad (4.31)$$

These results are indicated in figure 4.10. The first pole occurs when

$$g_{m1}R_1g_{m2}R_2 = \frac{g_{m1}}{2\pi fC_m} \quad (4.32)$$

where,

$$f_{p1} = \frac{1}{R_1 g_{m2} R_2 2\pi C_m} \quad (4.33)$$

and the unity gain bandwidth (UGBW) is at a frequency of

$$1 = \frac{g_{m1}}{2\pi f C_m} \quad (4.34)$$

where,

$$UGBW = \frac{g_{m1}}{2\pi C_m} \quad (4.35)$$

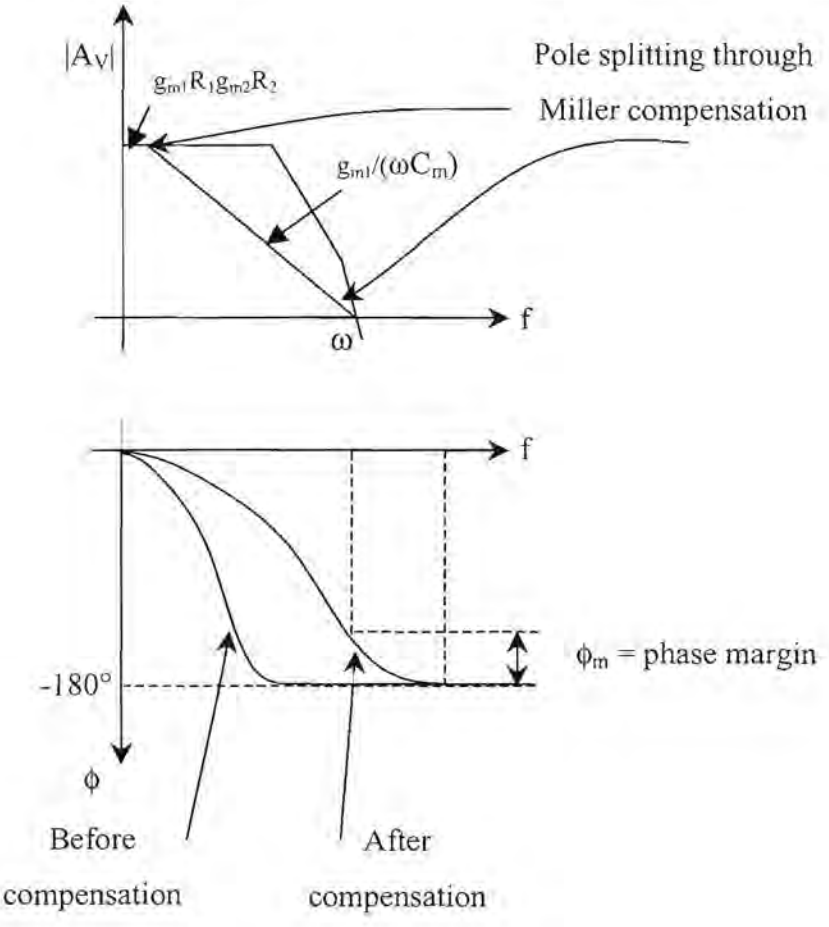

Figure 4.10 Frequency compensation

It can thus be seen by increasing C_m causes a greater splitting between the two dominant poles, which thus also satisfies the original assumption. The reason for the poles splitting is seen for both cases as the following. Firstly, the Miller effect causes a multiplication of the Miller capacitor to virtually appear in parallel with C_1, which was seen before to shift the first pole closer to the origin. The cause for the shift in the second pole is due to the fact that at high frequencies, C_m tends to short out the second stage causing the resistance when looking back into the g_{m2} stage from C_2 to decrease and thus has the effect of reducing R_2 and ultimately to shift the second pole to a higher frequency.

Effect of the Right Half Plane Zero

As the gain of bipolar stages is high, the zero usually has no effect on bipolar operational amplifiers as its effects occur long after the unity gain point. This problem resides mainly in CMOS devices due to the low gain of individual stages as the zero causes 20 dB/dec increase in gain at the zero point frequency. The problem is larger than this as a further 90° phase shift is also associated with this zero. As a result, the gain crossover point is much earlier than the phase crossover point and causes instability. The right half plane zero thus acts as a left half plane pole regarding the phase response and as a left half plane zero regarding the open loop frequency response. This is illustrated in figure 4.11.

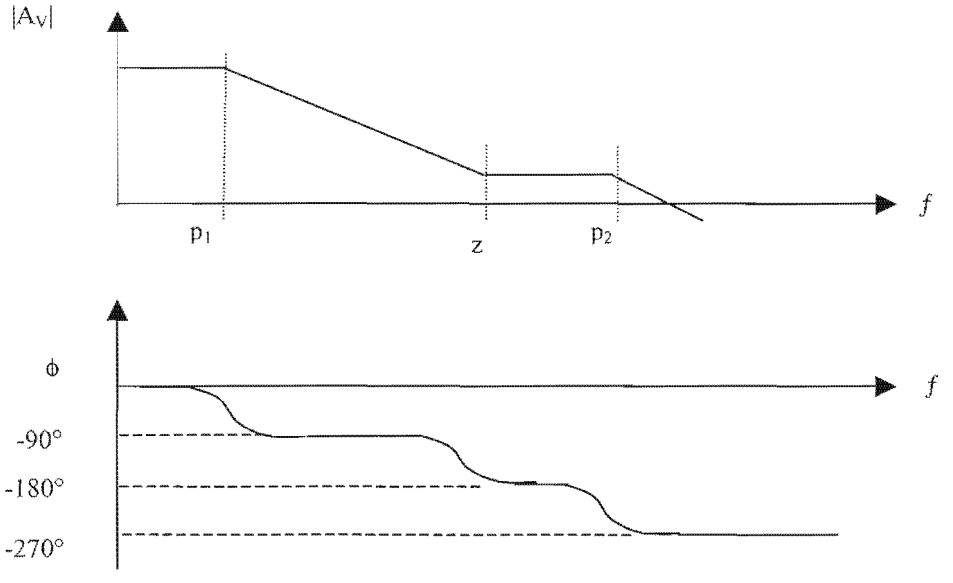

Figure 4.11 Effect of the right half plane zero

The problem can easily be solved by adding a series resistor to C_m with a value of $R_z = 1/g_{m2}$ which results in moving the zero to $+\infty$.

$$z = \frac{1}{C_m\left(\frac{1}{g_{m2}} - R_z\right)} \qquad (4.36)$$

Due to mismatching, it will not always be possible to achieve an exact resistor value and thus choosing $R_2 > 1/g_{m2}$, will result in moving the zero from the right half plane to the left half plane close to the second dominant pole, where stability can once again be achieved. Here, the zero contributes a positive 90° phase shift and is shown in figure 4.12.

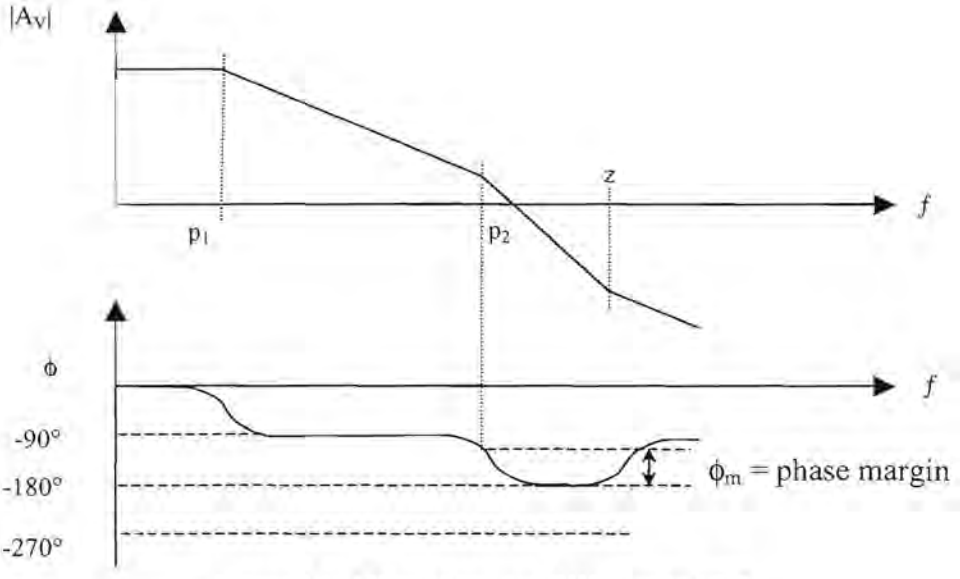

Figure 4.12 Effect of moving RHP zero to LHP

4.4.3. Design of the Operational Amplifier

The following specifications are proposed and are fairly general-purpose specifications for an operational amplifier that will still yield conformance of global specifications.

- $V_{DD} = 5$ V
- $A_{V(opoen\text{-}loop)} > 80$ dB
- UGBW prod > 1 MHz (stable)
- Slew-rate = 2V/µs
- Phase margin > 45°

Figure 4.13 shows the proposed circuit of the operational amplifier inclusive of compensation. This amplifier will be implemented in the current reference circuit shown in figure 4.3. This amplifier needs to be self biased for implementation in the current bias circuit. The amplifier will be used to drive only a very small capacitive load.

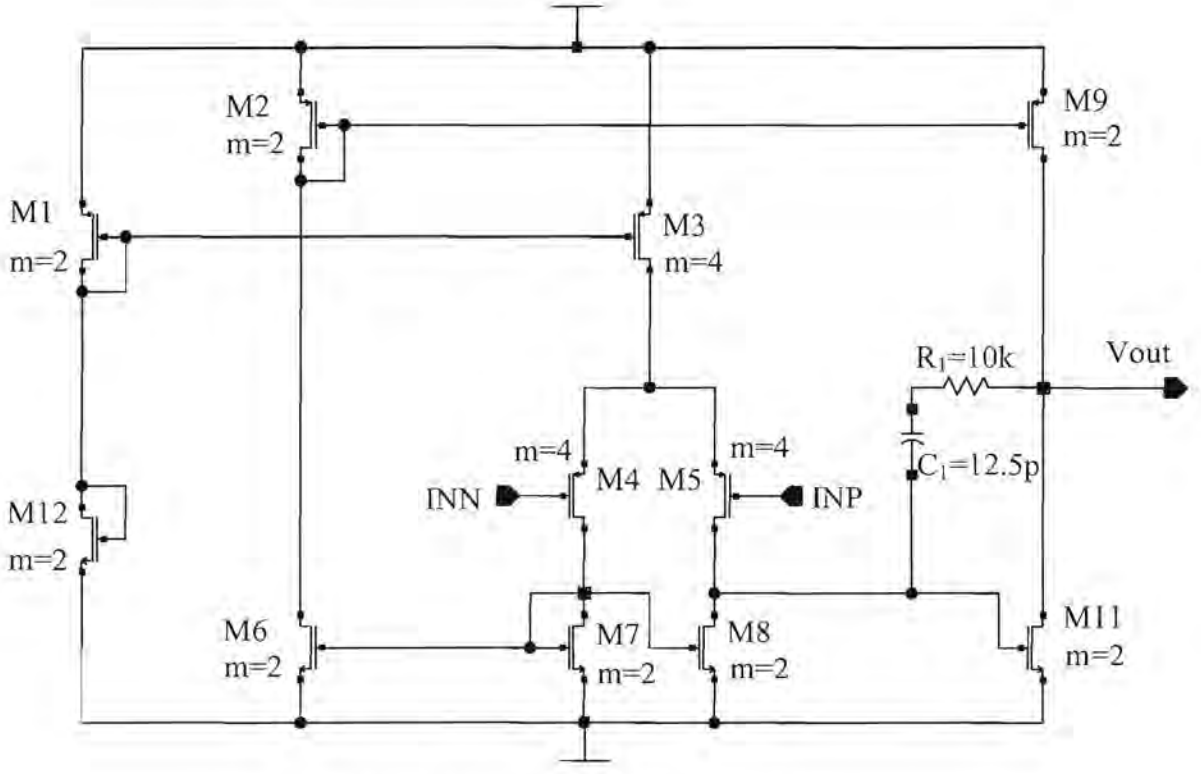

Figure 4.13 CMOS operational amplifier

A slight modification will be done to this operational amplifier so as to convert the output into a current, which will be used to implement the instrumentation amplifiers of both the voltage-to-current converter and output stage amplifier. The principle is once again based on current mirrors and the output branch will simply drive an output current with the same ratio as that of the output stage. This is achieved by the modification in the circuit comprising of transistors M4, M5, M6, M16, M17, M18 and M19. This is to ensure that the gain stage is not loaded by external components thus decreasing the output impedance. The circuit is shown in figure 4.14. The two inputs V_{nbia1} and V_{nbia2} will be driven from the two outputs, V_{nbia1} and V_{nbia2} of the bias circuit in figure 4.3. These transistors will then establish the 25 µA bias current which will be consequently mirrored into the circuit through M1.

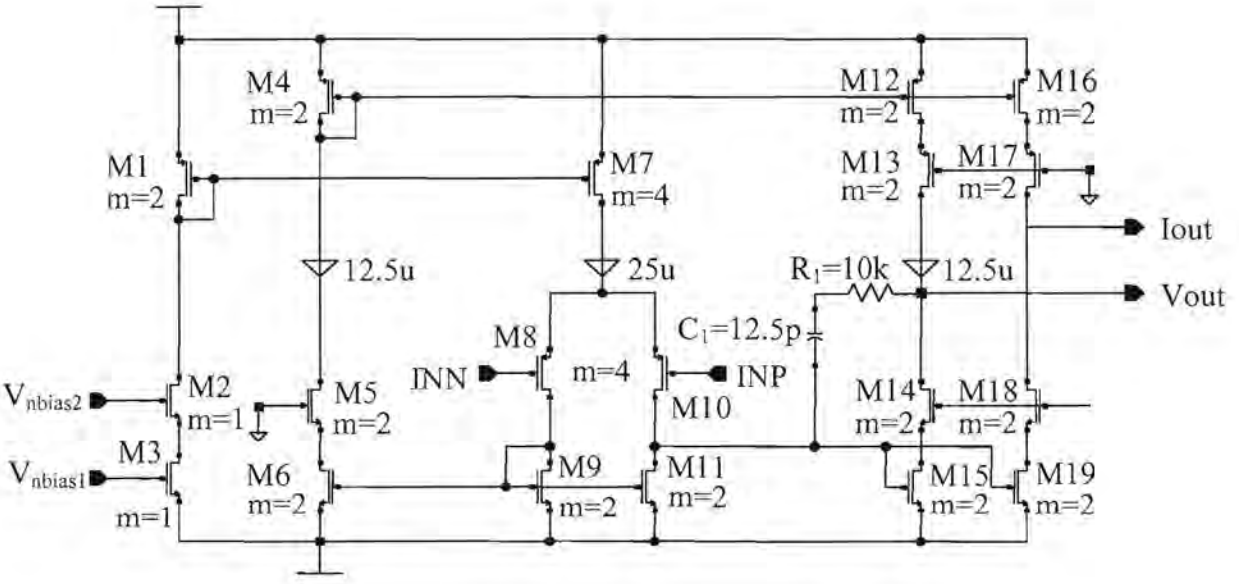

Figure 4.14 Operational amplifier based current converter

The circuits were designed based on the required operational amplifier specifications and the following data was calculated for implementation on the proposed technology. A detailed mathematical analysis can be seen in addendum B.

- $A_{V(open\text{-}loop)} = 95$ dB
- Input transistor ratio of $W_5/L_5 = 38$ and of type PMOS
- A compensation capacitor of 12.5 pF
- First Pole at 273 Hz
- Second Pole at 180 Mhz
- A LHP zero at 10 MHz
- A phase margin of 90°

4.4.4. Output Instrumentation Amplifier

These specifications will satisfy the requirements needed by the system to function correctly. The instrumentation amplifier configuration is shown in figure 4.15. Based on previous experimentation results, the Hall generator is expected to deliver an output signal of between 0 and 6 mV and will be represented by an output current signal of 0 to 6 µA suggesting a gain of 1 mA/V. R_1 will thus be 1 kΩ for a current ratio of 1:1 consisting of five 5 kΩ n-well resistors in parallel to satisfy the technological design rules for the CMOS process. Typically

the input offset of an operational amplifier is not good enough for the required application and consists of two components. The first is a systematic offset, which is in the order of 5 to 30 mV, with the second type being the statistical offset, which could contribute up to 10 mV. The configuration used in figure 4.15 overcomes the systematic offset problem through differential implementation. The statistical offset however will still remain. The minimization of the systematic offset is achieved through the design of well-matched operational amplifiers.

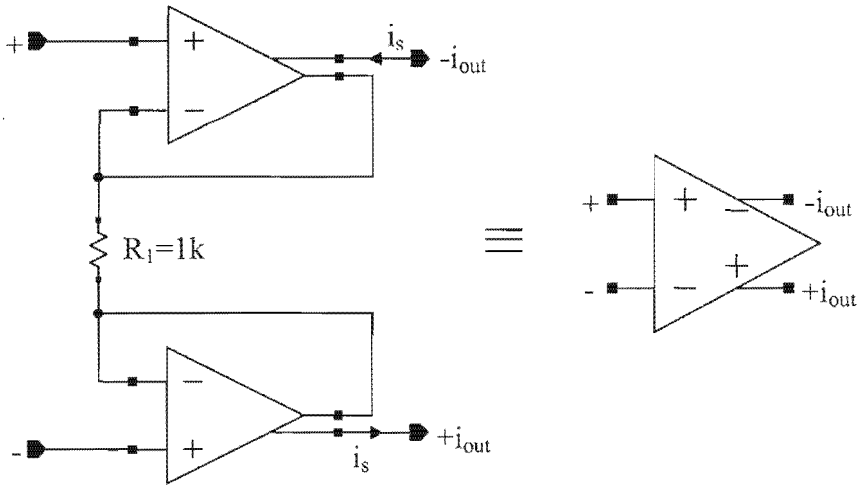

Figure 4.15 Output instrumentation amplifier

As mentioned earlier, the resistor used for this configuration will be a pinched, n-well type, as this makes it possible to compensate for temperature as well as process variances within the Hall generator. A semiconductor resistor is manufactured using regions with specific doping concentrations such that the resistance behaves in a way that is acceptable for the application. The amount of resistance required in an n-well resistor is based on equation (4.37). From chapter 3 it was seen that the Hall voltage in terms of current as well as voltage sensitivities were proportional to the same factors and thus any variation in temperature or process parameters are compensated for by the same amount when the absolute value of this resistance is used.

$$R = \frac{1}{q\mu_n nt}\frac{W}{L} \qquad (4.37)$$

4.5. OFFSET CANCELLATION AND FILTERING

The Hall generator, as with all semiconductor devices, is not a perfect device. The element, from an electrical point of view, will show unavoidable imbalances due to resistive gradients, geometrical asymmetries [4, 6, 7] and piezoresistive effects [4, 6, 7]. Furthermore, the offset is a function of the biasing current making it difficult to isolate the offset from the useful signal. These imbalances can generate a non-negligible offset voltage (V_{op} in figure 4.16) of between 0.5 mV - 5 mV for a 5 V supply. For this reason, static offset cancellation techniques such as electrically erasable programmable read only memory (EEPROM) cannot be used due to the fact that this offset itself dynamically changes with respect to time. This is due to the fact that the bias current will be a sinusoidal signal proportional to the line voltage. Furthermore, switching offset cancellation techniques as used in amplifiers cannot be used, as there is no available state where V_{offset} can be isolated from V_h except through the removal of the magnetic field making it a nonviable option.

By making use of the fact that the Hall generator behaves similar to a distributed resistive Wheatstone bridge from a dc point of view, it is possible to geometrically arrange the Hall generators and electrically connect them such that the imbalance source that remains invariant and fixed in solid space be equal but of opposite polarity and thus achieving the desired cancellation effect. This reduces signal-conditioning circuitry but establishes the need for multiple elements, which could use up large resources in terms of die area. Alternatively, it could be possible to use only one plate to generate the quadrature states by periodic supply and output contact permutations [4, 8, 11]. This method does however require the use of more complicated signal processing circuitry but takes advantage of reducing the residual offset and its production spread as compared with multi-element sensors. This is a significant advantage as zero-level deviations are degraded due to element mismatches between physically different elements and are mostly generated by package and temperature-dependant built in stresses.

4.5.1. The Switched Hall Plate

The simplest form of dynamic offset cancellation in Hall plates uses a Hall generator with four contacts where the quadrature states are generated by periodically connecting the biasing current to one pair of contacts or to the other as shown in figure 4.16. The technique can take on one of a few forms. It has already been mentioned that a 90°-direction change in current through the plate will result in an equal but opposite offset voltage [4]. In this way, it is

possible to superimpose the offset voltage of the element onto the useful Hall voltage signal at a higher frequency thus resulting in the offset being distinguishable from the information-carrying signal in the frequency domain and is illustrated in figure 4.17. The output signal can thus be low-pass filtered to extract the Hall voltage and any variations in the offset voltage with respect to different parameters such as bias current, temperature or varying stresses will be distinguishable. Other techniques include switching in all four directions along with polarity reversal of amplifier inputs thus creating a technique that functions in conjunction with chopper stabilized offset cancellation techniques as implemented in low input offset amplifiers [23, 24, 25, 30, 31]. This method is very effective but at the cost of increased circuit complexity for marginally better performance. The last method will be to switch the element such that the offset voltage remains quasi-constant with an alternating Hall voltage and can be a useful method with systems requiring the output in this form.

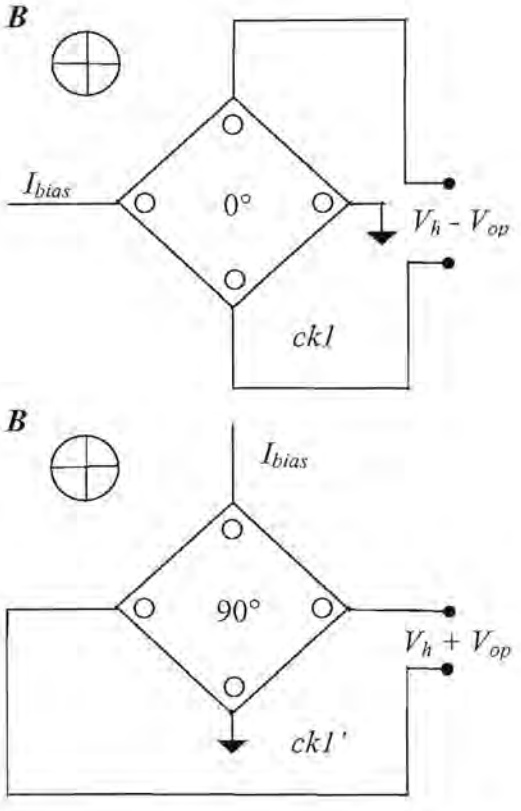

Figure 4.16 Periodic 90° bias current direction switching

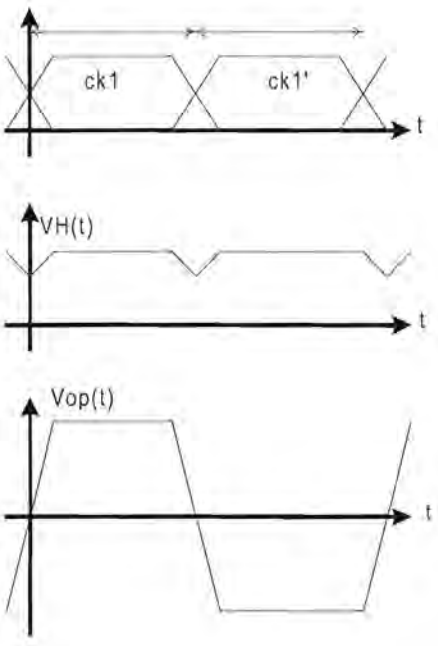

Figure 4.17 Clock, Hall voltage and plate offset waveforms

Figure 4.18 shows the circuit diagram of the implementation of the switching circuitry. The switches comprise of complimentary transmission gates of minimum size of which the W/L ratio for the NMOS, and PMOS transistors are equal. This is to ensure that equal amounts of opposite charge packets are injected resulting from clock feed through cancel each other [28]. This method thus reduces charge injection. Equation (4.38) shows the speed limitation of these switches and will be dominated by the PMOS transistor, as its mobility is less than that of the NMOS. Typically this speed is in the order of MHz and will not affect this application with the harmonic content of a few hundred Hz.

$$f = \frac{\mu_p}{L^2} \qquad (4.38)$$

The switching circuit has clock inputs, T<0:1> and TN<0:1>. Two 50 % duty cycle clocks, 180° out of phase with one another, drive these inputs. PCH and NCH are the input and output nodes for the bias current respectively and INP and INM are the positive and negative sensing nodes for sensing of the Hall voltage. Let the two clock phases be represented by the states CLK_1 and CLK_2, and let CLK_1 represent the condition where T<0> = '0', T<1> = '1', TN<0> = '1' and TN<1> = '0', then CLK_2 suggests that T<0> = '1', T<1> = '0', TN<0> = '0' and TN<1> = '1'. From this analysis, it can be seen that during CK_1, the bias current flows through the Hall generator from terminal A, to terminal D, and that the Hall sensing nodes are

connected via terminals B and C. Similarly, during CK_2, current flows from terminal B to terminal C, and sensing nodes are between terminals A and D. This then physically realizes the explanation given in figure 4.16.

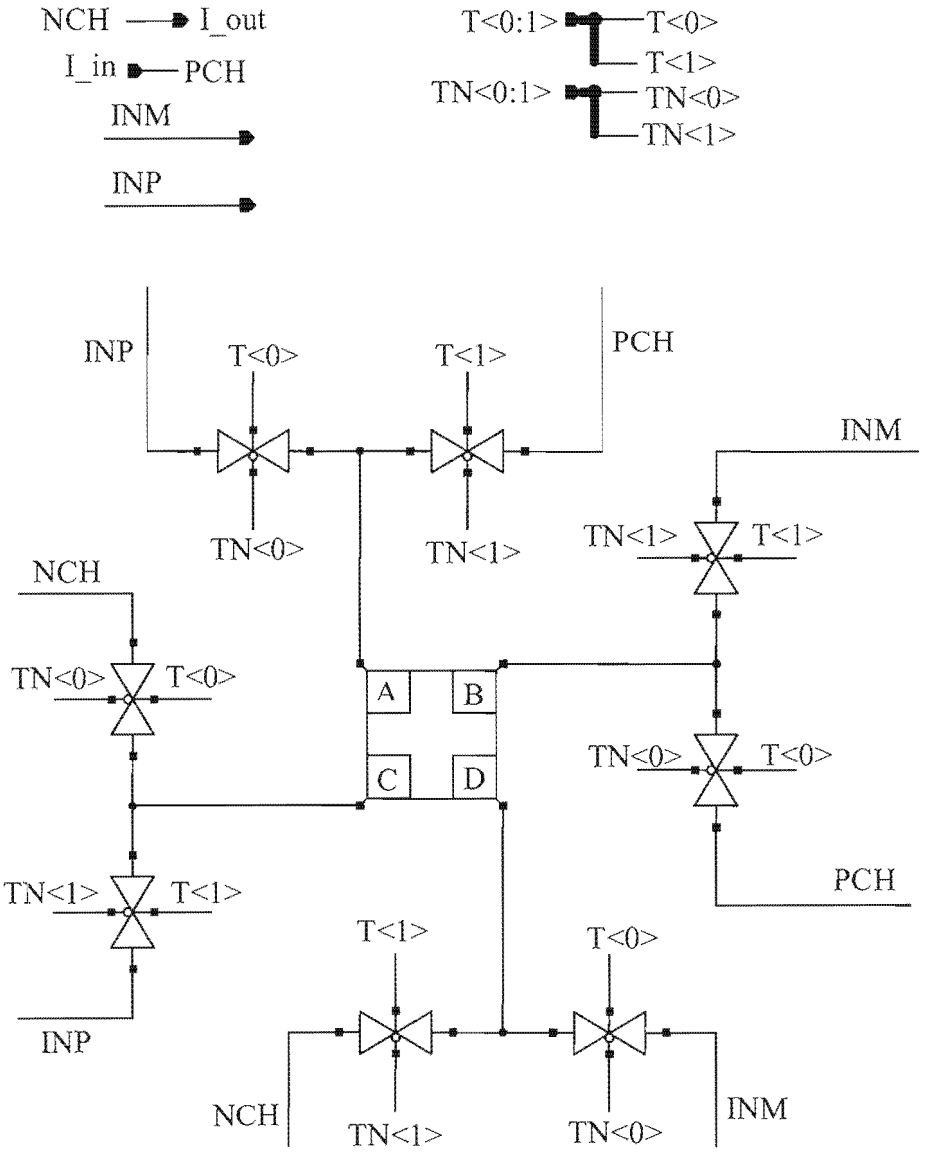

Figure 4.18 Circuit diagram showing switching arrangement using transmission gates

4.5.2. Filtering

It is proposed to use passive low-pass filtering at the output of the Hall generator. Maximum switching frequency of the quadrature states for highest efficiency must be determined through experimentation and it was found in literature [4] that common upper limits for switching frequencies are in the order of 100 KHz and is governed by the minimum time required by the Hall generator to redistribute the charges through the plate such that the

output signal is settled for validity. A frequency of 10 KHz will thus be assumed for the switching speed and a –3 dB cutoff frequency of 500 Hz will be used for the design of the filter elements. This will ensure that the 45 – 325 Hz measured signal remains undisturbed and that the superimposed offset voltage signal along with higher frequency switching noise is removed. The low-pass filter is shown in figure 4.19. The elements are designed according to equation (4.39).

$$f_c = \frac{1}{2\pi RC} \qquad (4.39)$$

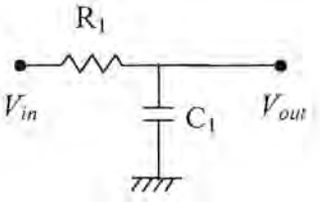

Figure 4.19 Passive low-pass filter

It was decided to use an external passive filter, as the optimum switching characteristics for the Hall generator must still be determined through experimentation. This filter would in future be replaced by an on-chip active system [30, 32], as the passive elements required for such low cut-off frequencies require an impractically large die area. The resistance and capacitance was calculated as 1 MΩ and 320 pF respectively.

4.6. SIMULATION

The following paragraph describes all the simulation results obtained for the individual components. These simulation results support the theoretical calculations for each component.

4.6.1. The Bandgap Reference

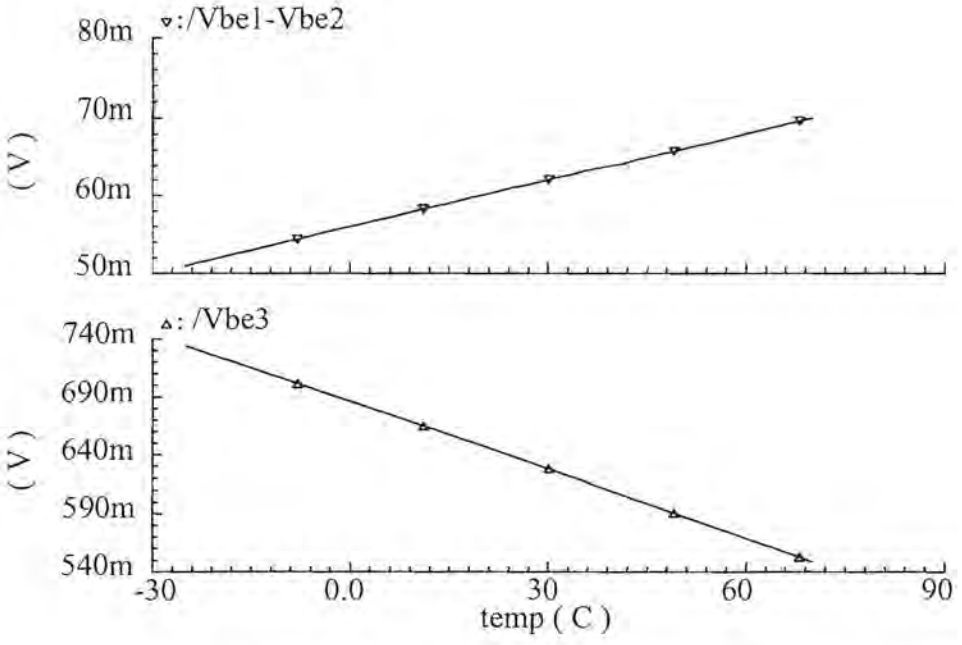

Figure 4.20 Simulation results showing temperature coefficients

Figure 4.20 shows the validity of equation (4.8) and equation (4.10). The following temperature coefficients were obtained:

$$\frac{\Delta(V_{be1}-V_{be2})}{\Delta T}=0.08685mV/°K \qquad (4.40)$$

$$\frac{\Delta V_{be3}}{\Delta T}=1.89mV/°K \qquad (4.41)$$

Figure 4.21 shows the bandgap reference output voltage V_{bg} with $\Delta V_{bg}/\Delta T$ = 2.2 mV/95 K. This results in a variation in the output of 0.16 % over the required temperature range or 0.0017 %/K and conforms well to the required specification of 0.05 %/K as required by the IEC standard. Two factors worth noting here is the output voltage is higher than designed for and secondly the zero TC is not at 27 °C and could be the result of the simulation models not

being accurately defined for temperature simulations, as there are many higher order effects that are not accounted for in the models that were used.

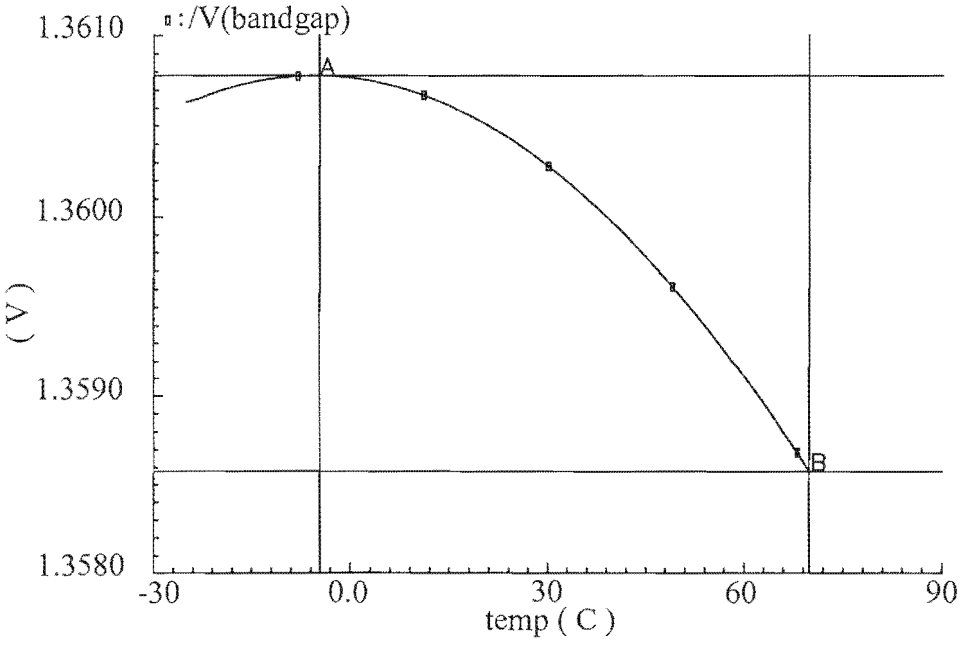

Figure 4.21 Bandgap reference output voltage

4.6.2. Bias Current Reference

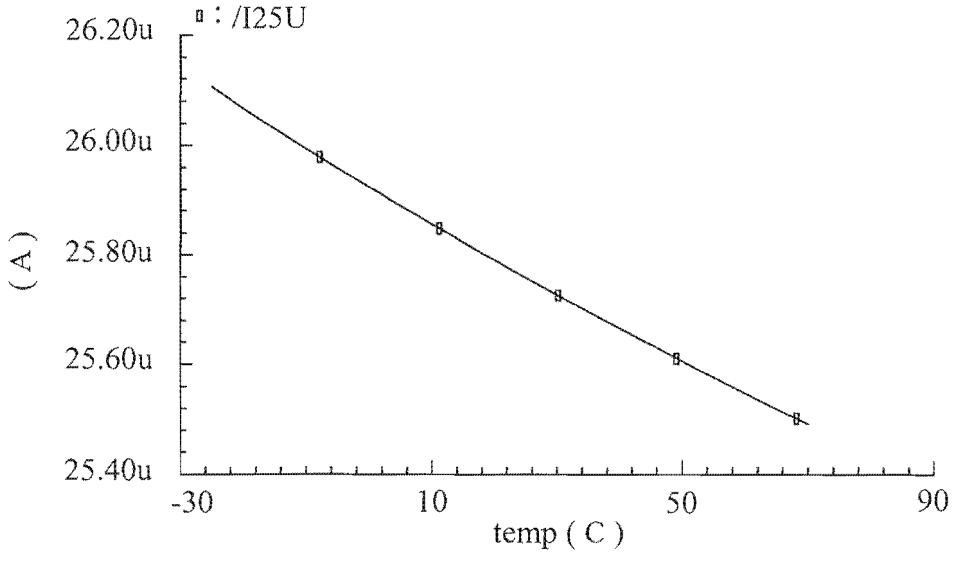

Figure 4.22 Simulation showing bias current dependence on temperature

Figure 4.22 shows the current reference circuit dependency on temperature showing that the total variation results to 2.3 % over the temperature range or 0.024 %/K. This is still within the specified 0.05 %/K as required by the IEC standard. The reason for the slightly higher temperature dependence in this circuit is the fact that the operational amplifier used must be self-biased as this circuit generates all the biasing voltages for subsequent circuitry. The use of an external calibrating resistor becomes useful here as inherent offsets in the operational amplifier can be compensated for, as well as any variations in the bandgap voltage. Furthermore, this resistor will set the overall gain of the system and this will be used for accurate calibration of the sensor. The circuit was simulated using the bandgap voltage of the circuit in figure 4.1 as a reference to the current referencing circuit. Thus, the temperature coefficient shown here contains the temperature dependence of both the bandgap and the current referencing circuit exclusive of the external resistor temperature coefficient. The reason for this is that the temperature coefficient for the external resistor is very small in comparison to the internal components. Also, should this become a problem, it will be possible to acquire more stable resistors to analyze its influence on the final sensor performance.

4.6.3. The Operational Amplifier

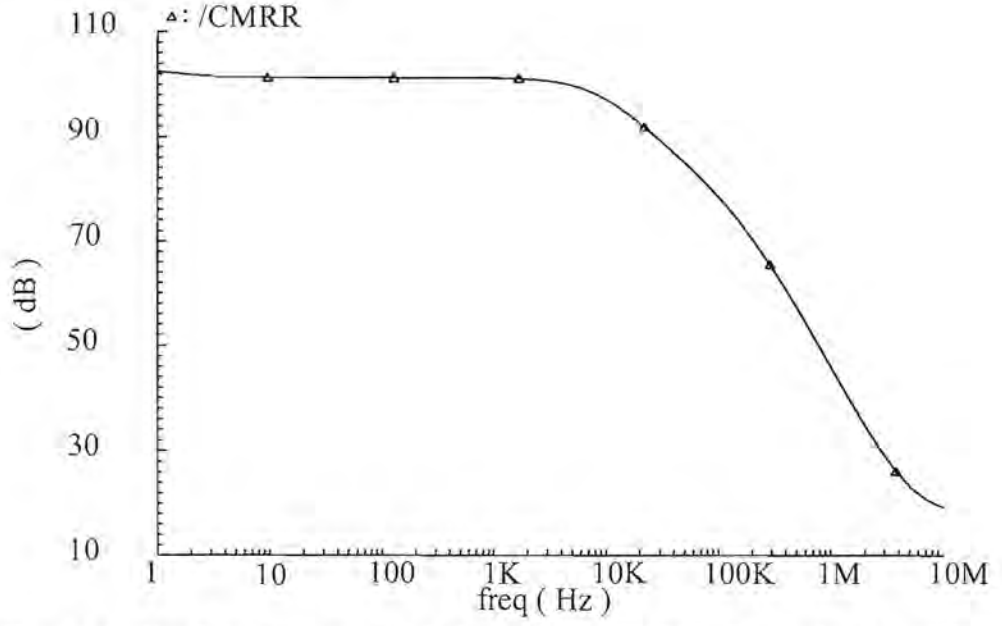

Figure 4.23 Simulated common mode rejection ratio (CMRR) of operational amplifier

Figure 4.23 shows the CMRR of the operational amplifier and it can be seen here that the value is fairly large and consistent at approximately 100 dB up to a frequency around 10 KHz.

The result compares well with a typical CMRR > 60 dB for general purpose unbuffered operational amplifiers. The CMRR is an important value and directly relates to the linearity of the operational amplifiers and thus the higher this value, the better the expected linearity. The most important influence regarding CMRR will be the 10 KHz clock used to switch the Hall generator. As this switching will be present as noise in the power supplies, it is necessary to take into account. Typically the dominant 10 KHz components will be fairly well suppressed by the amplifier. The CMRR will still remain within typical values up to 1 MHz, at which switching transients will become insignificant. Furthermore, the clock speed can be reduced to much slower speeds. The lower limit will be dominated by the Nyquist theorem that states that sampling rate must be at least twice the maximum measured signal frequency. This frequency component is that of the 5th harmonic in the line current and is around 400 Hz. The low pass filter will also limit the input frequency into the amplifier.

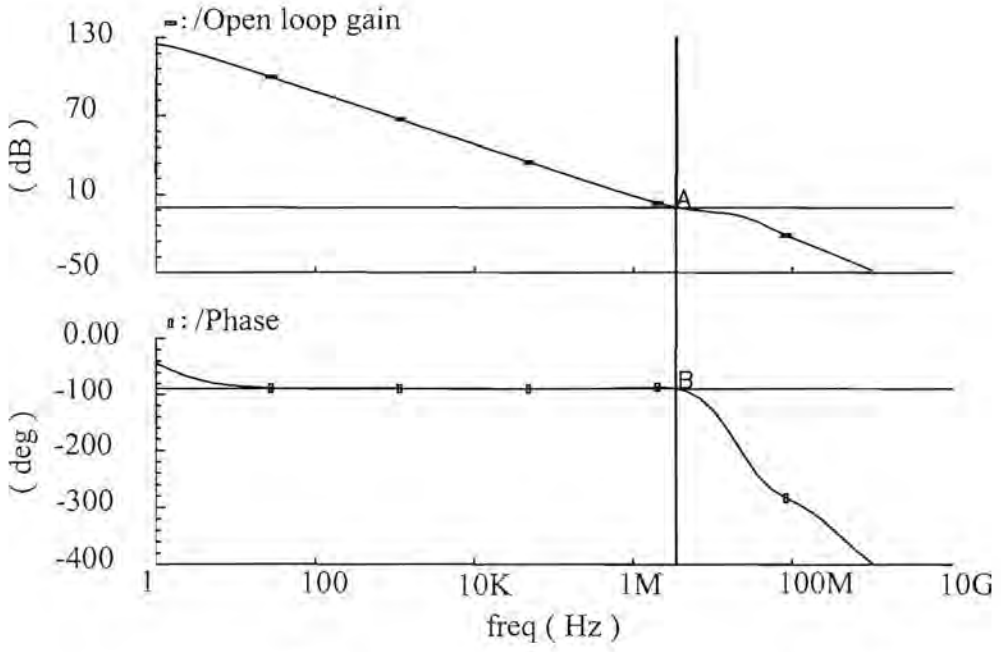

Figure 4.24 Frequency response of operational amplifier

Figure 4.24 shows a simulation of the open loop frequency response of the operational amplifier. The low frequency gain is seen to be around 125 dB and compares well with the aimed for 95 dB. It must be remembered that the mathematical models are only first-order calculations thus accounting for the difference. As a result of the higher gain, it can be seen that the "pole-splitting" effect has also caused the first most dominant pole to move below the designed for 273 Hz to around 5 Hz. The UGBW = 3.5 MHz and is stable with a phase margin of around 90°. A phase margin of around 45° is usually desired as this yields a time

step response that is critically damped and desired. The step response will thus result in a fairly over-damped response but as we are once again working with such low frequencies, this is not of major concern. The UGBW agrees with the aimed value of ≥ 1MHz. The zero was designed to be around 10 MHz as can be seen in the simulation result. In figure 4.25 it can be seen that the slew rate is almost 2.2 V/µs, which is slightly better than the aimed 2 V/µs.

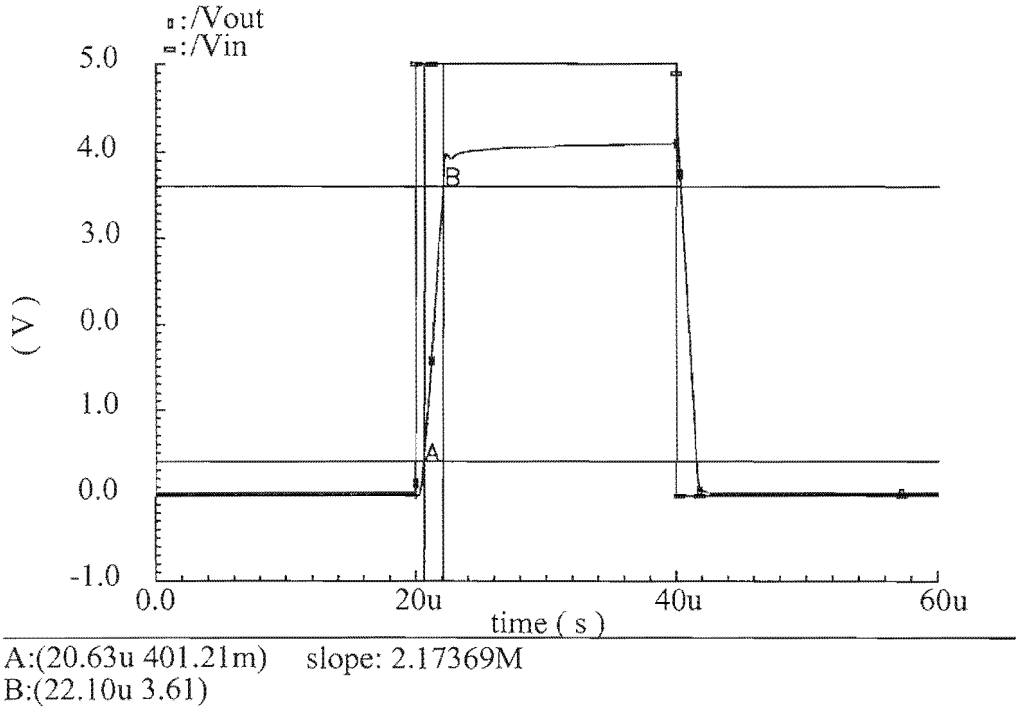

Figure 4.25 Step response characteristics of operational amplifier

The linearity results of the instrumentation amplifier in figure 4.26 show that amplification characteristics are very linear for larger differential inputs but that the linearity deteriorates around a zero differential input to about 1 %. The major disadvantage here is that the linearity around the lower limit will decrease for the sensor system but should still be within the required 1.5 %. The discontinuity appears to be a modeling characteristic around the origin. These results also describe the voltage to current converter but with a gain of 8 mA/V.

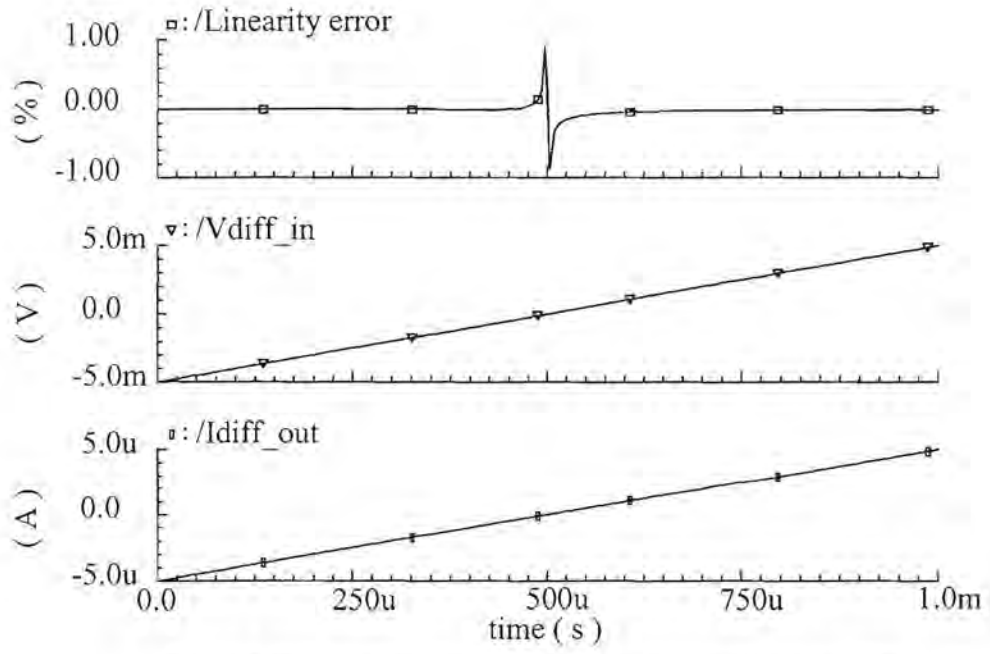

Figure 4.26 Linearity characteristics of instrumentation amplifier

4.7. EXPERIMENTAL VERIFICATION

The use of the CMOS manufacturing process allowed for only a limited area per run for test devices and thus not all devices could be manufactured and tested as separate entities. The following paragraph thus describes those devices that were produced and the results that were obtained and include a similar voltage to current converter and instrumentation amplifier circuit. Some devices similar in architecture were used to acquire data relevant to the system and the voltage to current converter is one such device.

4.7.1. Instrumentation Amplifier

The instrumentation amplifier was tested in terms of linearity and differential offsets between the amplifiers. It was found that the referred input differential offset between the amplifiers had an average value of < 1 mV and the contributing factors are mainly due to mismatches between separate operational amplifiers as well as differences in the biasing conditions of each amplifier.

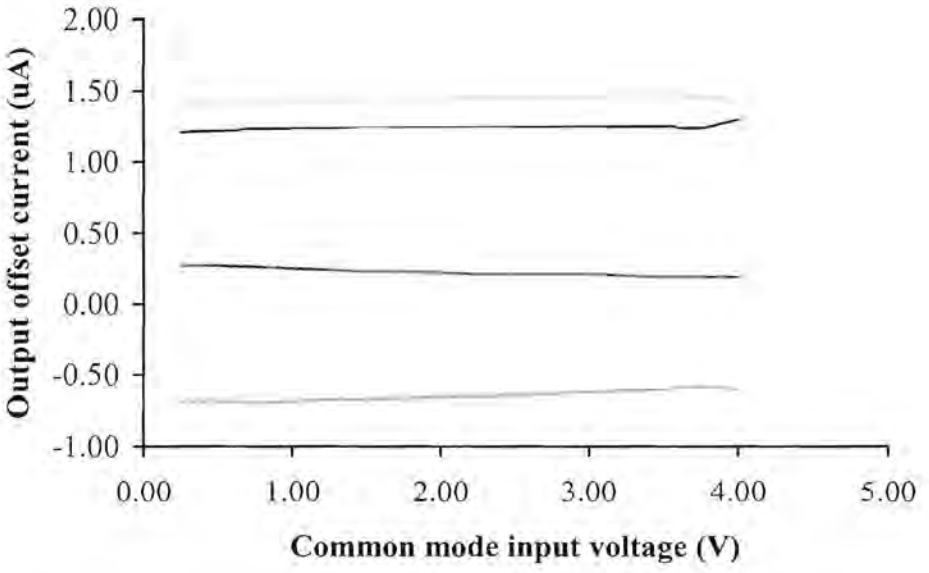

Figure 4.27 Graph showing output offset current versus common mode input voltage

Figure 4.27 shows a graph of the output-offset current present in four, randomly selected devices that were tested. The output current can be seen to be very stable over the entire common mode range up to 4 V, and ultimately displays the stability of the tail current in each operational amplifier. This is the most important factor to consider with this configuration, as it is the largest contributor of non-linear properties. The common mode operating conditions for this amplifier will be around 2.5 V with an expected common mode variation of ± 2.5 mV. Under these conditions, the amplifier tail current maintained very high accuracy and changes could not be measured with the available instrumentation with a resolution of ± 10 nA. As mentioned in the previous paragraph, the better the biasing currents are matched between separate amplifiers, the better the resulting linearity would be as the transconductance of the amplifying stages are directly dependent on the bias currents.

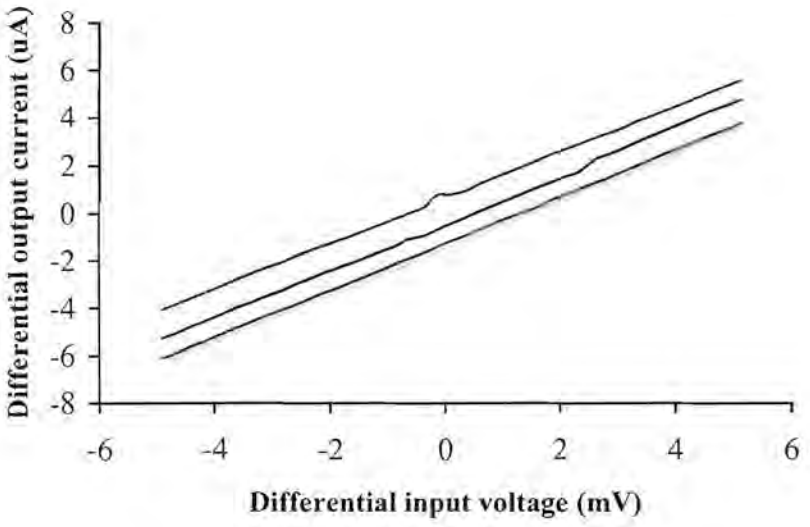

Figure 4.28 Graph showing output current versus differential input voltage

The curves in figure 4.28 illustrate the output differential current as a function of the input differential voltage. The test was done using a power supply with ±1 mV resolution. The non-inverting input was held at a constant 2.5 V while the inverting input was varied within a differential range of ±5 mV at its input. To increase the input resolution, an accurate resistive dividing network was used such that the input resolution was increased by a factor of 4. The worst linearity figures were calculated at 1.2 % with an average value at 0.7 %. Once again, linearity was mainly dependant on matching and differences in biasing conditions between the amplifiers. From this figure, the offsets are also visible where the curves cross the x-axis. It can be seen that these offsets are within ±1.5 mV. This was expected as these offsets represent typical statistical offset figures. Generally, all aspects of the instrumentation amplifier performance characteristics yielded good results in comparison to simulations.

4.8. CONCLUSION

This chapter focused on the design of the entire analog building blocks required by the power sensor, such that a fully functional device can be manufactured. The chapter started with an explanation of the sub-systems required by the sensor and the importance of well-defined temperature behavior in biasing circuits. The design of a bandgap reference that would be suitable to the application was given followed by the design of supplementary circuitry that would establish the biasing currents required by the amplifiers and other analog blocks. The

voltage to current converter necessary for the biasing of the Hall generator as a function of the mains voltage was then presented that based its foundation on the current referencing circuit. The following few paragraphs were dedicated to detailed operational amplifier design principles that were used to design a general-purpose amplifier that would later form the building block of the instrumentation amplifier. The working philosophy of the instrumentation amplifier was explained along with the basic principles of the compensation techniques that were exploited using this specific architecture.

All sub-systems were verified in simulation using simulation models based on a standard double metal, double poly, 1.2 μm CMOS process and the resultant characteristics were compared to theoretical calculations and basic principles. Some of these sub-systems were then manufactured using this standard CMOS process and verified in a laboratory under similar conditions as used in the simulations. The results were then compared to both simulation and theoretical models and discrepancies were clarified. Due to limitations in manufacturing resources, only a few devices were manufactured for testing purposes. Similar devices manufactured in this technology where available, were characterized to clarify assumptions and gather relative design information for remaining devices.

5. HALL MULTIPLICATION BASED POWER SENSOR SYSTEM

5.1. INTRODUCTION

The following chapter is devoted to the integration of the Hall generator with the analog signal processing circuitry. Although all the sub-systems for the integrated power sensor have now been proven, it is necessary to verify the fully functional system and verify in both simulation and experimentation that the system performs as designed and within specification. The chapter commences with the system interfacing in which a functional description is given. The system is then verified in simulation according to the IEC standard followed by the experimental verification. Some layout issues will be presented along with the layout of the sensor system. The proposed sensor performance results will then be compared with that of similar such systems and the chapter will be concluded with a concluding summary.

5.2. SYSTEM INTERFACE

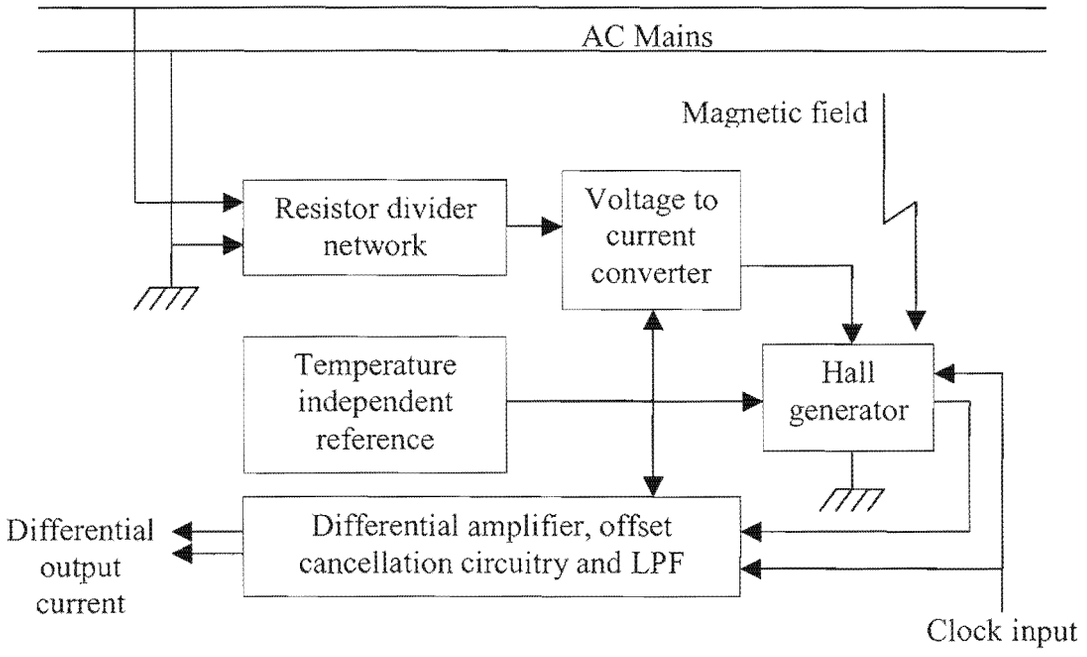

Figure 5.1 Schematic of integrated power sensor system

Figure 5.1 shows the block diagram of the proposed integrated power sensor system. The system implements a bandgap to generate a voltage required by the current biasing circuit. This circuit is used to bias the operational amplifiers in both the voltage to current converter as well as the output instrumentation amplifier. The system consists of 4 inputs and 3 outputs

namely the mains voltage, mains current (via the magnetic field), bandgap enable and clock making up the inputs and the output differential current and bias resistor making up the outputs. A detailed schematic of the system is given in addendum C.

The line voltage of 230 V_{rms} ac, has been scaled down to a 33.1 mV_{rms} signal using a resistor divider network. This is illustrated in figure 5.2 below. The resistors have been calculated according to Ohm's law, such that the rms current through the network is kept extremely small and has an rms value of 150 µA. R_4 can be used to calibrate the gain of the sensor, through adjusting the gain of the Hall generator. The divider network output is then fed into the voltage-to-current converter as illustrated in the block diagram above.

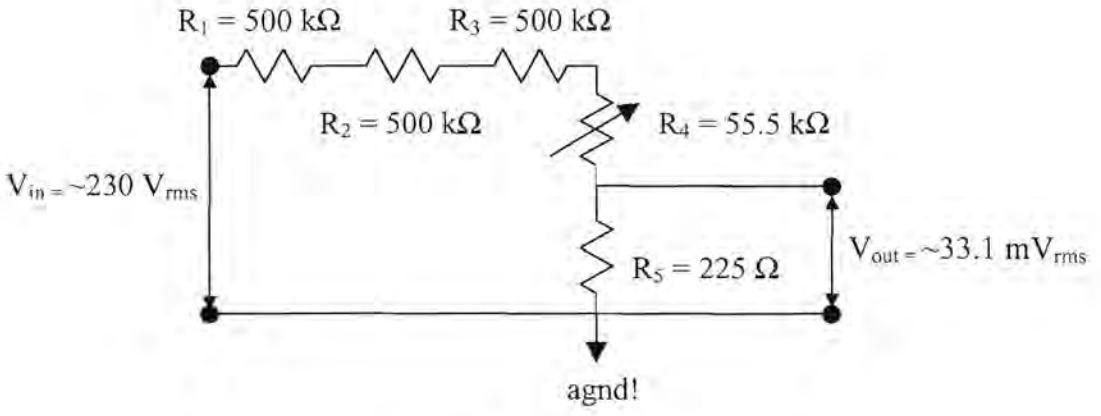

Figure 5.2 Resistor divider network

Figure 4.4 showed that resistor R_1, used to convert the input voltage into a current, had a value of 5 kΩ. The output transistor M16 to M19 in figure 4.14 have been scaled for a current gain of 40, thus biasing the Hall generator with the required 265 μA_{rms} or rather, an alternating current of 375 µA peak. The higher biasing current than the initial 300 µA that was suggested in paragraph 3.4.9, is due to the lower sensitivity of the Hall generator resulting from the influence of the geometrical correction factor determined in paragraph 3.6.1. With this gain, a peak Hall voltage of 6 mV is expected at rated conditions. The line current is sensed indirectly through a magnetic field with an expected peak value of 100 mT. The bandgap enable signal is generated by a standard cell from the digital library of the given process, that outputs a logic high, approximately 100 µs after the power supply has attained its maximum value of 5 V. This is to ensure that the bandgap output voltage is approached from the highest supply rail and that the output does not settle in its other stable state of 0 V. The final input consists of a standard logic square wave used to switch the Hall generator bias

and sensing terminal through 90°. This is implemented using the transmission gate network of figure 4.18. The gates are switched at a rate given by the clock frequency of 10 KHz. The differential output signal will consist of a differential current signal peaking at around 6 µA. The external resistor will be used to set up the reference bias current and was calculated to be 50 kΩ such that a current of 25 µA is generated using the bandgap voltage.

5.3. SIMULATION

The system must be verified in simulation before any manufacturing takes place, as this is a lengthy and expensive exercise. The system was simulated in union with all its components necessary for meeting the system specifications as described in paragraph 2. This chapter describes the simulations and results obtained. Certain specific circuit behavior scenarios with respect to the Hall generator were not possible to simulate, especially temperature dependencies as these behaviors have not yet been captured in a simulation model and were based solely on knowledge gained during the creation of this document. Compensation in this regard was taken into consideration where possible.

The specifications achieved in simulation are as follows:

Circuit operating voltage	5 V
Power supply range	0.9 to 1.1 U_n
Maximum supply current	typically < 1.9 mA
Operating temperature	-25°C to 70°C
Maximum Line Voltage	230 V_{rms}
Base current	20 A_{rms}
Maximum line current	80 A_{rms}
Line frequency	50 Hz
System sensitivity (Typical)	0.229 µA/kW (rms)
Temperature stability for 0.1 $I_b \leq I \leq I_{max}$	-0.042 %/K
Accuracy for 0.05 $I_b \leq I \leq 0.1\ I_b$	< 1.0 %
0.1 $I_b \leq I \leq I_{max}$	< 0.8 %
Voltage circuit max consumption	< 50 mW and 0 VA
Current circuit max consumption	Negligible
Process requirements	Standard silicon 1.2 µm CMOS, double metal, double poly

A large part of the typical current consumed in the circuit is a direct result of the factors involved in biasing the Hall generator. There exists a trade off between sensitivity and power consumption and maximizing the Hall sensitivity through an increased bias current, also increases the power consumed. The larger part of this current is consumed by the biasing of the output transistors M16, M17, M18 and M19 in figure 4.14 and can contribute more than 50 % of the total current required.

The system sensitivity was achieved and is better described by the accuracy figure obtained. As can be seen, the lower end accuracy was well within 1.0 % and compares well with the desired 1.5 %. The higher end specification was better than 0.8 %. The reason for a worse lower end specification presents itself in that when the output current is extremely small it becomes comparable in size to other undesired signals, dominated mainly by offsets. From the simulations regarding linearity of the instrumentation amplifier configuration, it was also noted that the linearity deteriorated around the origin of the amplifier and this behavior was expected. As two of these amplifiers are implemented in this circuit, both play a contributing role in this regard. As can be seen, the linearity quoted here display better results than the worst-case values of separate entities simulated earlier. This is because once the circuit is implemented in a kW/hr meter, the linearity becomes a function of time. This non-linearity presents itself as short pulses in time closely around the origin of the current and voltage signals and thus contributes very little to the root mean square (rms) value of the power signal. This will thus have a significantly smaller effect on linearity errors when averaged over time and hence, average linearity values are stated in the specifications.

Simulations showed that the Hall generators based on an n-well resistive model shows a linearity of 0.002 % within the given range of the specified magnetic field. In practice, this figure is expected to still be better than 0.05 %. It can thus be deduced that any improvement in linearity would present itself in the improvement of the instrumentation amplifiers.

The major advantage gained from the Hall generator is that as the voltage and current circuits are purely resistive with high impedances, the power consumed by these circuits become minimal. The major contributor to power consumed in the voltage circuit is the voltage divider network and is only 1.5 % of the maximum permitted 2 W.

The current circuit depends only on the measured magnetic field of the supply and its power contribution is thus negligible. As mentioned, the circuits are resistive and the Hall voltage reacts directly to the magnetic field and thus no phase shift occurs. This makes it possible to measure phase shifts in the supply line and eliminates the need for compensation of phase errors as with current transformers.

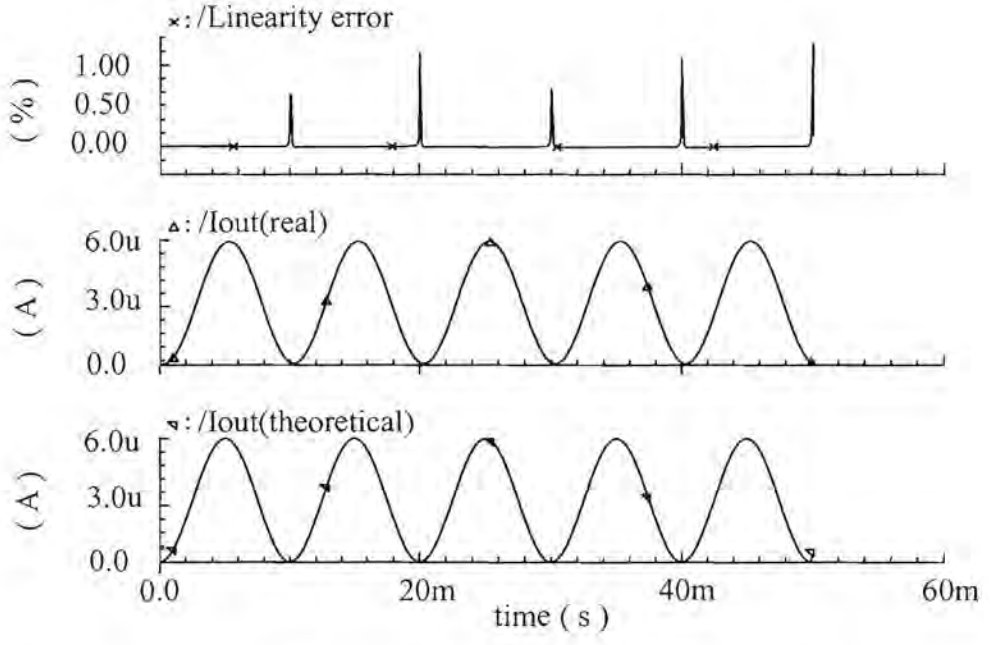

Figure 5.3 Simulation results showing the linearity error of the real current output versus the theoretically calculated model with no offset

Figure 5.3 shows the simulation results of the differential output current signal for a maximum line current and a line voltage of 230 V_{rms} versus the theoretically calculated model with no inherent offset present. These signals are then used to calculate the linearity error and it can be seen how the linearity is largest in the vicinity of the origin, a phenomenon that was expected based on previous simulations of the instrumentation amplifier. Once again, this also explains the reason for larger linearity errors at smaller signal levels where this problem has a larger contribution to the error.

Figure 5.4 shows the effect that the offset inherent in the Hall multiplier has on the output signal. The signal is severely distorted when compared to the expected sinusoidal output. The reason for this distortion lies in the fact that the offset is a function of the bias current and is analyzed as follows.

$$V_{offset} \propto I_{bias} \tag{5.1}$$

Also,

$$V_{hall} \propto I_{bias} B + V_{offset} \tag{5.2}$$

From Equation (5.1) it can be seen that the offset voltage is directly proportional to the bias current and that the Hall voltage is the sum of the cross product of the bias current and the perpendicular magnetic field and the offset voltage as shown in Equation (5.2). Now we know that if the bias current and the magnetic field are both sinusoidal, the resultant product is of the form $\cos^2(\omega t)$ but that the offset is of the form $\cos(\omega t)$. The resultant output will thus be a function of two frequency components, one consisting of *f* and the other of *2f* and the larger the inherent offset, the larger will be its contribution to the resultant output.

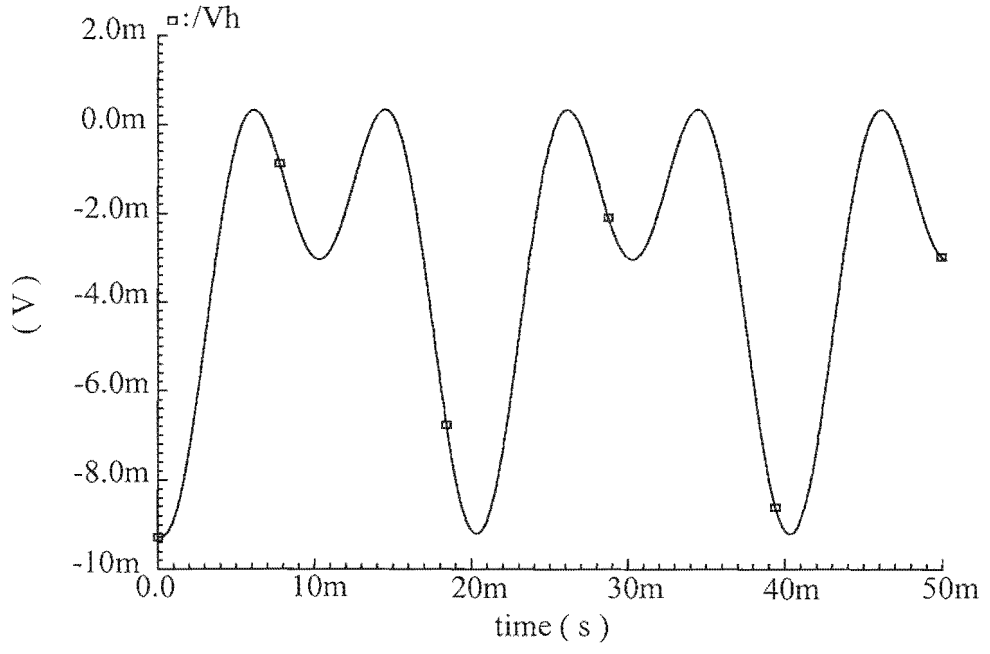

Figure 5.4 Simulation showing the effects of offsets on the Hall voltage signal

The resultant output with implementation of the offset cancellation technique is shown in figure 5.5 whereby the Hall generator is electrically rotated by 90° at a frequency of 10 KHz, taking advantage of the fact that a 90° rotation causes a 180° phase shift in the offset voltage and a 0° shift in the Hall voltage thus isolating the offset voltage from the Hall voltage. The net result is that the offset voltage signal is translated to the much higher frequency at which

the Hall generator is being switched and the information-carrying signal can be retrieved through low-pass filtering.

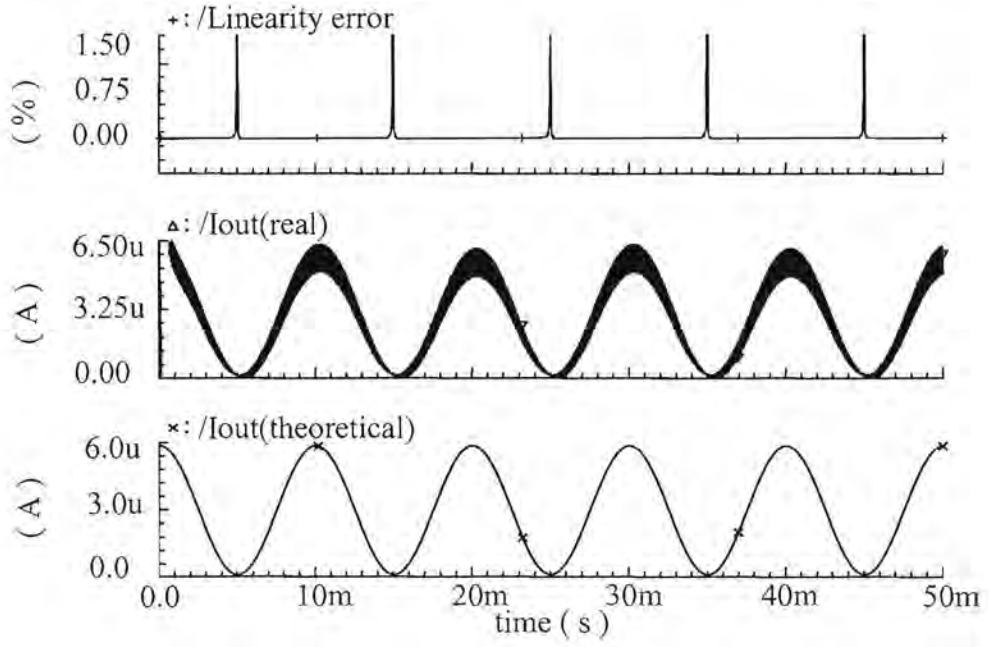

Figure 5.5 Simulation results showing the linearity error of the real current output versus the theoretically calculated model inclusive of offset after filtering

Figure 5.6 shows a closer view of the switching transients present in the output signal. The clock frequency used is a 10 KHz clock, for quadrature rotation of the Hall generators.

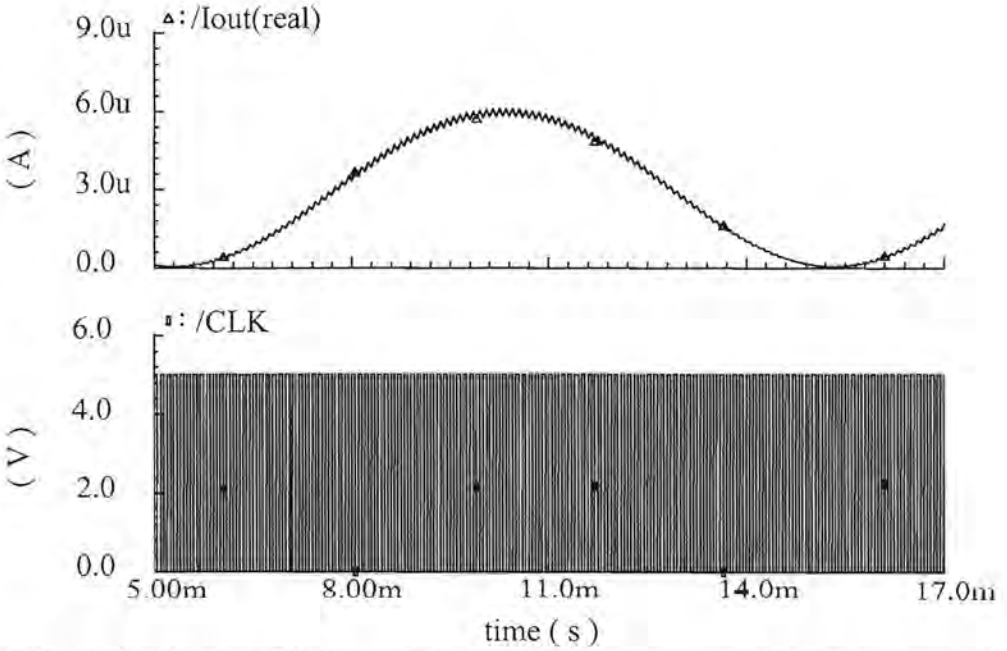

Figure 5.6 Simulation showing switching noise present in the output current in the presence of a 10 KHz clock frequency

Figure 5.7 shows the dependence of the output signal to a variation in temperature for an input signal of V_{mains} = 220 V_{rms} and I_{max} = 80 A. The difference in current between markers A and B show that the output varies by 200 nA over the temperature range of –25 °C to 70 °C. This translates to a temperature dependency for the output current of -0.035 %/K, which falls within the specification requirements. Similar simulations over the line current range showed the worst coefficient to be -0.042 %/K. The coefficient still falls within the requirements however, the behavior is extremely close to the limits and process variations could place this value outside the required specification. The temperature coefficient indicates that the overall system sensitivity decreases with an increase in temperature.

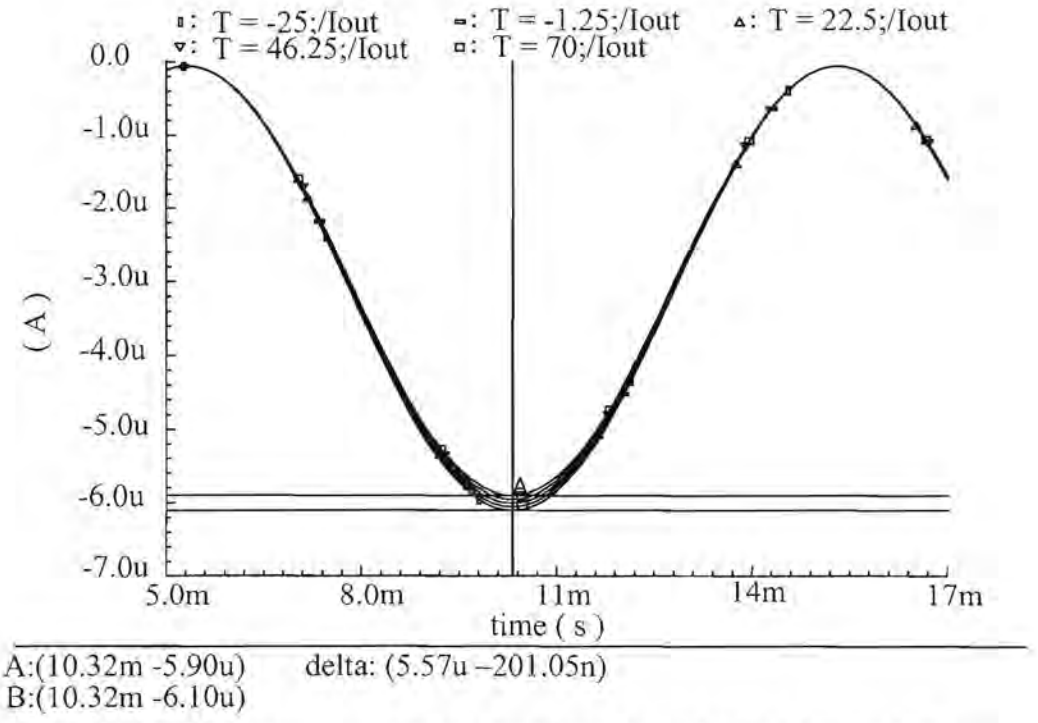

Figure 5.7 Simulation results of output signal dependence on temperature

Figure 5.8 shows the simulation result of the supply current consumed in the sensor circuit. The current has an average value of approximately 1.88 mA at a supply voltage of 5 V. This translates into a power consumption figure of < 9.4 mW.

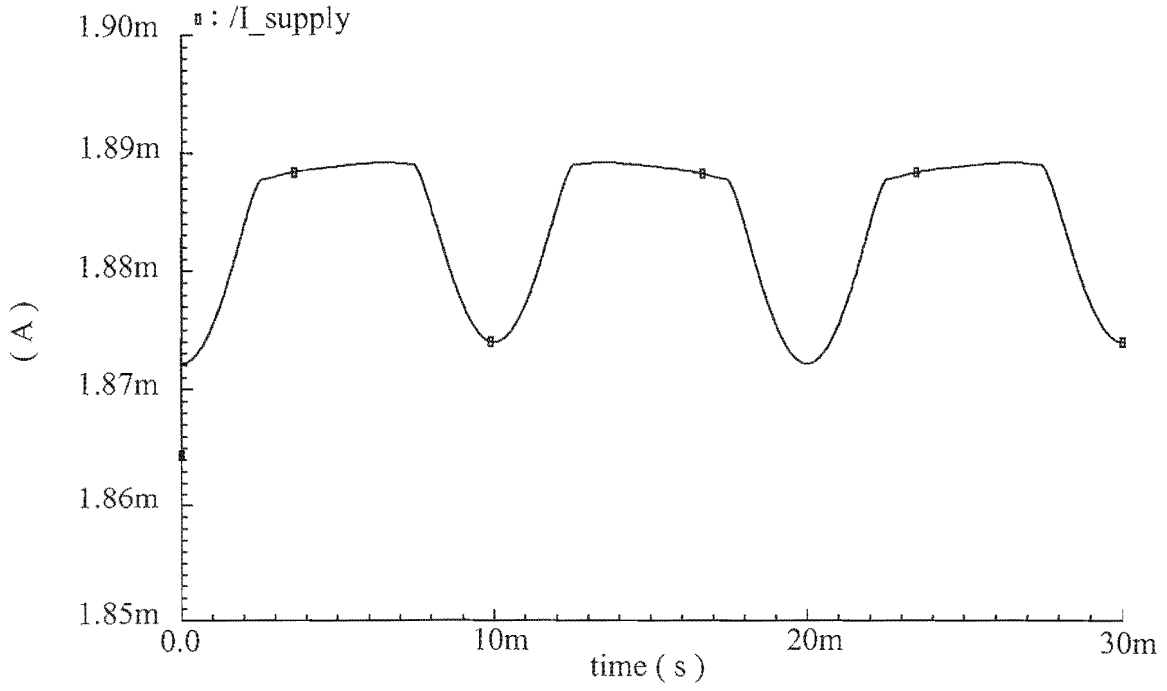

Figure 5.8 Simulation result showing supply current versus time

5.4. EXPERIMENTAL VERIFICATION

The experimental verification was done under standard room temperature conditions using the suggested wire-wound ferromagnetic core to generate a magnetic field. A discrete voltage to current converter with similar specifications as the suggested component in this document was used, the only difference being that the resistor was implemented externally. Once again, the system was assembled with the components available as in the previous chapter due to a limitation in resources. The principle could still be tested and sufficient knowledge was gained so as to assess the extent of performance compliance as well as the required guidelines necessary for the development of future circuit architectures.

5.4.1. The Hall multiplier

The Hall sensor used for the verification of the design data, was configured slightly differently to that required by this specific design. The element was configured such that the output Hall voltage changed its phase by 180° with a quasi-constant offset voltage. Furthermore, one of the biasing terminals was permanently tied down to V_{SS}. This configuration is typically used in linear sensing applications whereby the sensor is biased with

a dc current. This creates a major problem for power sensing applications as a negative swinging bias current results in the Hall generator being forward biased across its n-well to substrate, or rather, the n-well to substrate acts as a normal forward biased diode. To overcome this problem, the bias current through the Hall generator was rectified. Figure 5.9 illustrate the results captured on an oscilloscope. The figure shows two signals; 1) showing an amplified signal of the Hall generator and 2) the rectified mains voltage used to bias the Hall generator itself. From this it is evident that the rectification in the mains voltage and not the mains current causes the output to be negative on all even cycles. It can also be seen that the offset causes a distortion in the zero crossings and can be seen in the different levels at which the zero crossings occur.

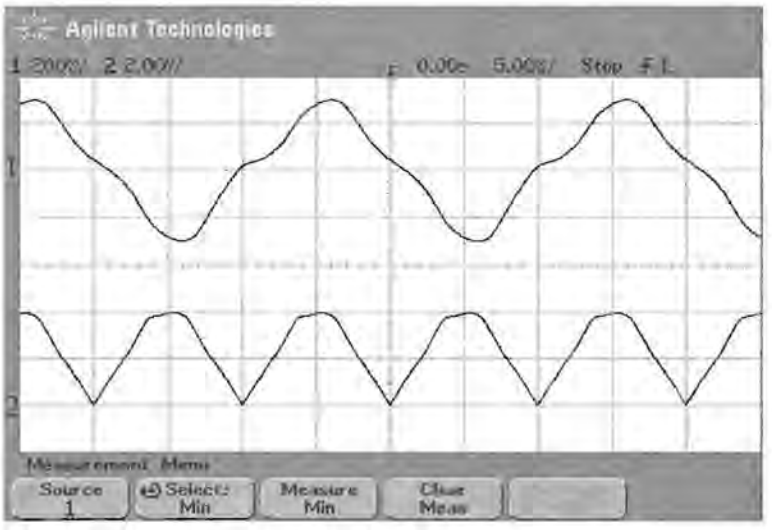

Figure 5.9 Graph showing measured results of 1) the amplified Hall generator output and 2) the rectified signal used to bias the Hall generator

The problem of the offset inherent in the output signal becomes a larger problem in this type of configuration, as the offset itself now too is a component of 100 Hz due to the rectified line voltage now being a 100 Hz signal. The offset now becomes part of the signal representing power output making it indistinguishable from the desired information. This illustrates the importance of a switching scheme implementing a quasi-constant Hall voltage as suggested in this document. This will make it possible to translate the offset signal to a much higher frequency and simply low-pass filtering the output signal. For illustration purpose, the Hall generator was switched with a 50 Hz signal in phase with the line voltage thus making it possible to rectify the line current. Figure 5.10 shows the physical results captured on an oscilloscope with a line current of 5 A_{rms}. The offsets can now be seen in the first signal at the

lower end, with a 100 Hz repetition rate. The offsets at the zero-crossings are also worsened by non-linearity in zero crossings in both the magnetic field during switching and rectification of the line voltage due to simple bridge rectifier forward voltages.

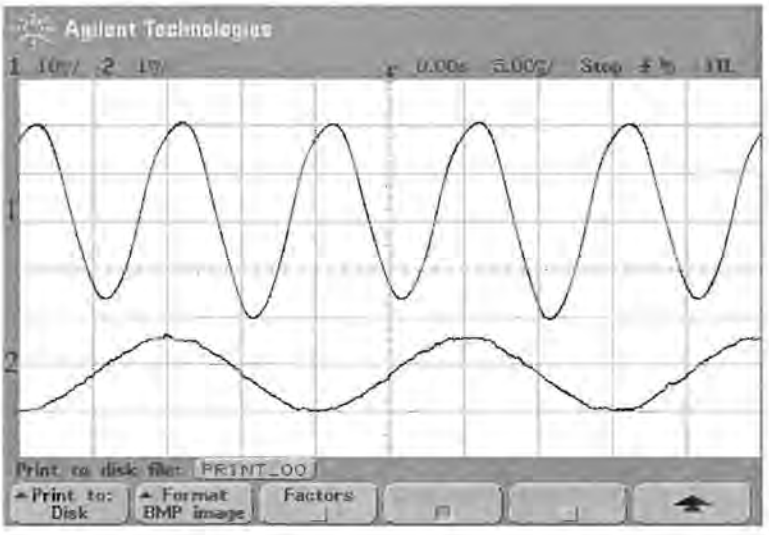

Figure 5.10 Graph showing measured results of 1) the Hall generator signal and 2) a voltage representation of the line current used to generate the magnetic field over the Hall generator

5.4.2. Linearity

The first experiment was aimed at establishing what the linearity of the sensor was, and consisted of the Hall sensor combined with the amplifiers. As the equipment available for the measurements could only supply a maximum of 10 A_{rms}, the test results show only the lower end linearity tests. Figure 5.11 shows the results obtained for the lower end linearity of the sensor. The data shows the results obtained for the 4 A to 8 A, lower end current specification. The linearity proved to be between ±0.5 %. This thus proves that the time average will also fall within the required ±1.5 % maximum. As more circuitry is required for implementing the sensor within an energy meter, the extra headroom is necessary for allowing non-linearity inherent in these circuits. Once again, it can be seen how the non-linear characteristics of the instrumentation amplifiers affects the extreme lower end accuracy.

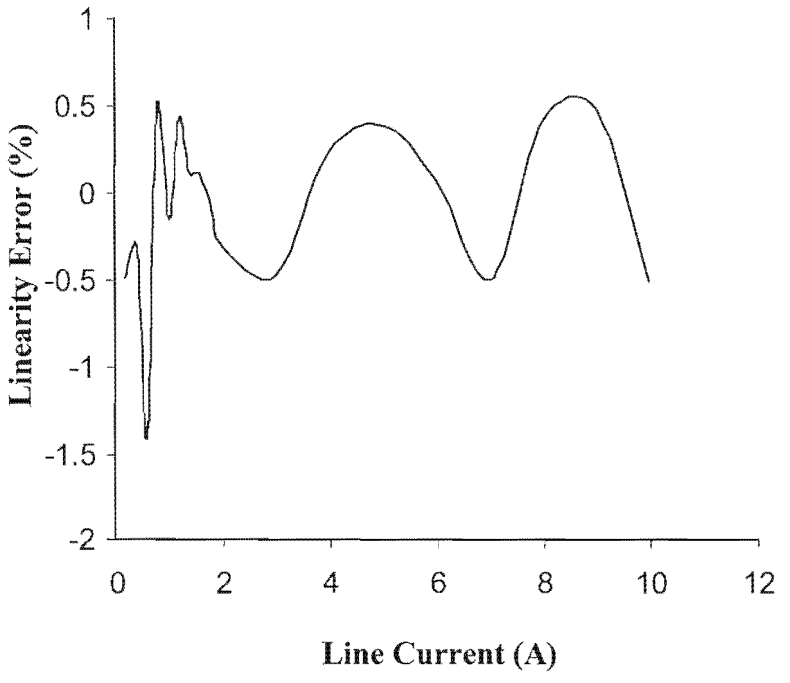

Figure 5.11 Graph illustrating the lower end linearity figures for the sensor versus line current

Figure 5.12 shows the transfer function used to calculate the linearity. The system sensitivity yielded a transfer function of 0.2302 µA/kW and is slightly higher than was simulated. This could be the contribution of various factors such as variations in the expected magnetic field produced in the ferromagnetic core, gain variations etc. This shows the importance for the need for calibration of such systems.

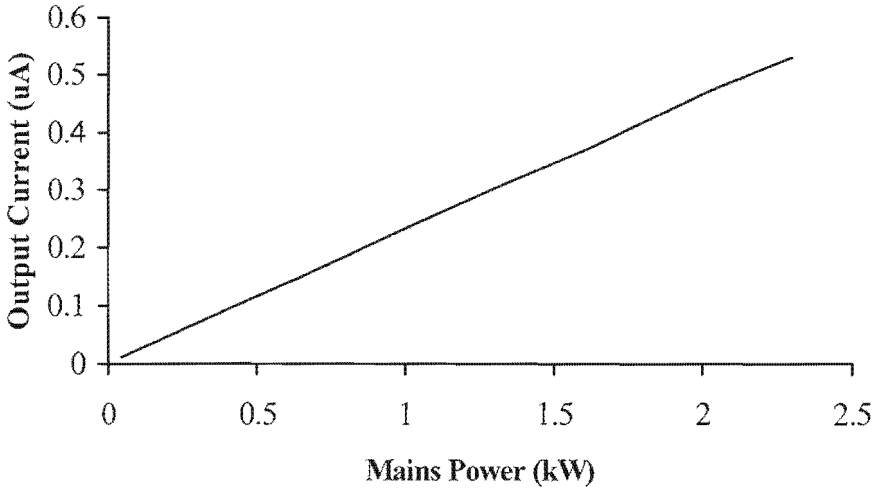

Figure 5.12 Graph illustrating the transfer function of the output current versus the input power

5.4.3. Temperature Stability

A series of experiments were performed regarding temperature tests of the Hall generator. It was found that the compensation method described in paragraphs 3.4.11 and 4.4.4 was indeed an effective solution. Although the method proved successful, more information was gathered regarding an effective placement of the compensation resistors. If the orientation of the chip shown in figure 5.15 can be defined as having its origin at the lower left hand corner of the chip, then the vertical dimension makes up the y-axis, and the horizontal, the x-axis. The following was found using this orientation as definition for the analysis. Figure 5.13 show the temperature compensated results of 3 random samples. The graphs illustrate how the temperature coefficient of the compensation resistor, compensates for the Hall generator sensitivity temperature coefficient, as a percentage of the difference between them. A 0 % result would be the ideal. The negative figures thus indicate an overcompensation of the sensitivity over the temperature range. This comparison is valid as the Hall generator and compensation resistor is manufactured of the same structure type namely pinched, n-well. The compensation resistors were strategically placed on both the same x and y-axis in close proximity to the Hall generator. It was found that the structures lying in the same y-axis yielded best matching properties. As the wafers are always orientated such that the crystal direction of the wafer is the same during processing ((100) crystal orientation), it will be possible to reproduce these results consistently, as the behavior is now defined and predictable.

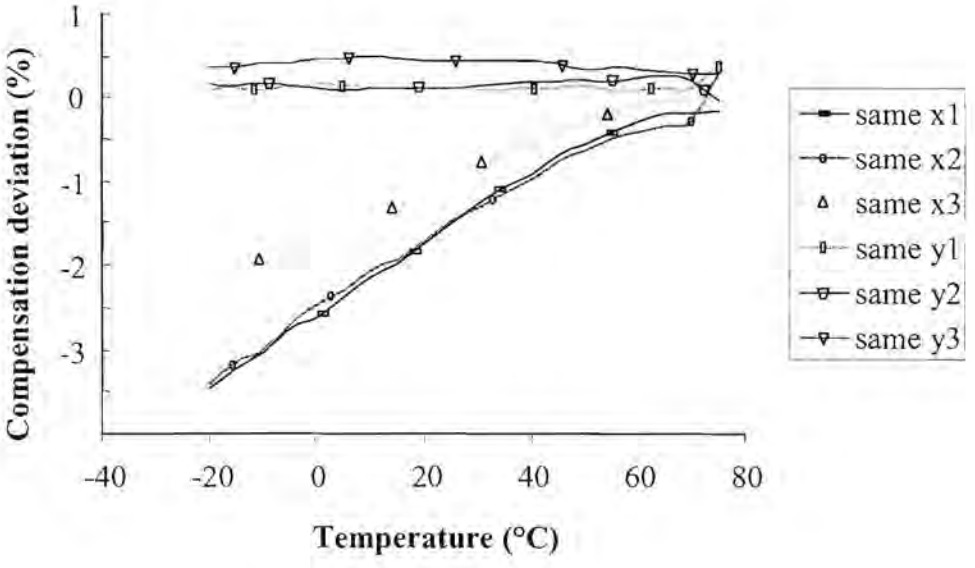

Figure 5.13 Graph illustrating compensation resistor effect when place in the same x and y-axis of the Hall generator

It can thus be seen that the same y-axis orientation of the Hall generator and compensation resistor, yields compensation capabilities of around + 0.005 %/K compared to same x-axis orientation of - 0.036 %/K. These results thus only include the temperature coefficients of the Hall generator and output amplifier with the compensation resistor, as they will dominate the temperature behavior of the sensor.

Figure 5.14 shows the results obtained for the temperature behavior of the sensor tested and include the Hall generator and output amplifier with its compensation resistor. The compensation resistor was orientation in the same x-axis direction as can be seen in figure 5.15. The sensitivity showed a temperature coefficient of - 0.055 %/K over the required temperature range. It can be seen that the result is slightly outside the required specification and that over compensation of the positive temperature coefficient of the Hall generator sensitivity has occurred. When looking at the typical voltage biased sensitivity of the Hall generator given by equation (3.36), this was to be expected. The voltage-biased sensitivity is not only negative, but also has a typical absolute value larger than that of the current biased sensitivity variation. As the compensation method is based on the change in voltage over the compensation resistor, the behavior is justified. Furthermore, the results could be improved with the same y-axis orientation of the compensation resistor.

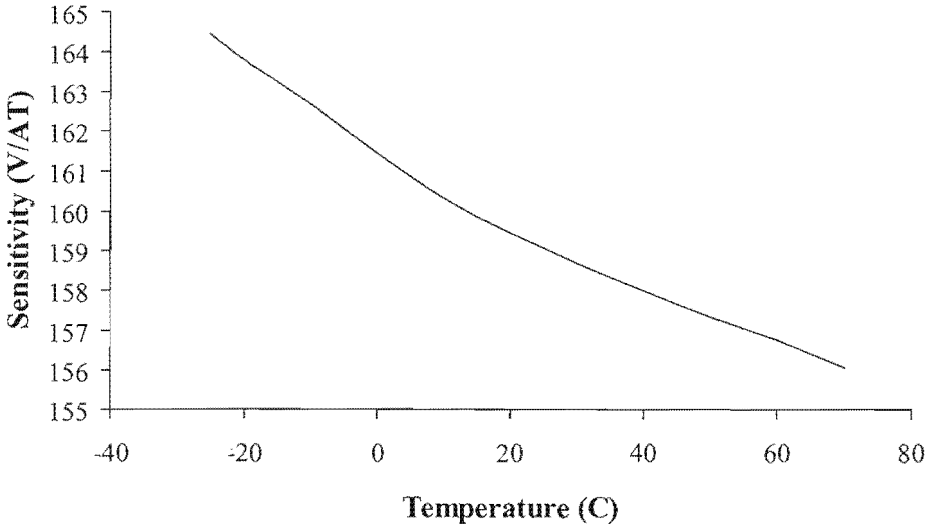

Figure 5.14 Graph showing temperature behavior of sensor sensitivity

5.5. LAYOUT AND PACKAGING

5.5.1. General Layout Considerations

The layout of an integrated circuit defines the geometries that appear on the masks used in fabrication. Micro-electronic layouts play an extremely important role in the performance characteristics of systems and can greatly influence the performance of a system to both its advantage and disadvantage. Care must thus be taken to properly plan the outlay of the device such that advantage can be taken of all relevant aspects that can have a positive effect on the performance of the final device. Aspects involved during the layout process involve adhering to the design rules for the given process used and the manufacturer involved supplies this data. Design rules incorporate aspects such as minimum sizes, spacing, enclosure and extensions as well as antenna effects. These rules aim to maximize the yield of devices manufactured as well as consistency in performance characteristics.

5.5.2. Analog Layout Techniques

The need for analog layout techniques are due to the fact that analog systems are more sensitive to negative effects caused by parasitic resistive and capacitive components such as crosstalk, mismatches, noise etc [28]. The most common techniques used during the layout included the likes of multifinger transistors for the reduction in parasitic gate resistance for increasing noise performance; symmetry for the reduction in input referred offsets and consists of matching device geometries as well as surrounding environment. Lastly, guard-band structures were implemented to separate the few digital components from the analog structures thus assisting in the reduction of switching noise induced in analog devices. Figure 5.15 shows a micrograph of the layout for the test chip used.

5.5.3. Packaging

It was mentioned before that the Hall generator suffers from piezoresistive effects. The effect presents itself through a change in the electrical resistance of the semiconductor upon the application of mechanical stress. The mechanism is as a result of the change in the interatomic distances in a crystal under stress [4, 6, 8]. A shift in the interatomic distances produces a change in the periodic field of the lattice and thus causing a change in the bandgap and effective masses of the carriers. This change in the mass thus causes a change in the mobility resulting in a mechanically dependent change in the Hall voltage signal. This mechanical

dependency can be minimized as mentioned before by biasing the Hall generator in a (110) direction to the crystal lattice of the semiconductor, defined as a (100) wafer, which can be clearly seen in figure 5.15. The layout legend is given in addendum D. Here, the Hall generator was placed at 45° to the vertical plane for the given layout rules of the process. The perpendicular stresses are thus completely minimized and the stresses caused by packaging are significantly reduced. These packaging stresses are the main causes of stress on the die.

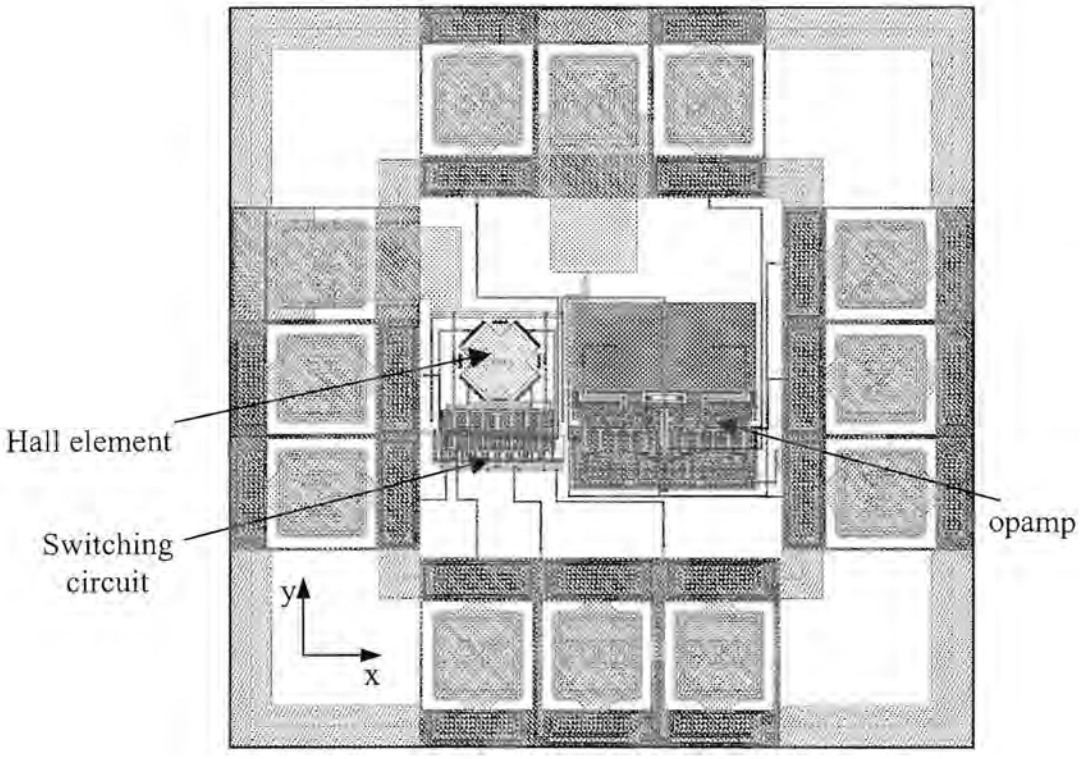

Figure 5.15 Micrograph of the layout of the test chip

A second packaging issue is a problem regarding the lead frames used in the packaging process. Firstly, the lead frames used in standard dual inline packaged (DIP) devices as well as small outline integrated circuit (SOIC) packages normally use paramagnetic materials such as aluminum and thus influence the magnetic field around the element on the die and secondly, for use with the ferromagnetic core, these and other standard packages are not mechanically suitable for the application. As a result, it was necessary to devise an alternative method for packaging the device to be tested. A cheap solution presented itself in the form of chip on board (COB) whereby the die is mounted on a standard printed circuit board (PCB) and "glob topped" for protection. This method proved an excellent solution as the PCB uses copper tracks (diamagnetic) for electrical connectivity and thus has no influence on the magnetic field under measurement. Furthermore, the final product is compact and thin

yielding easy access for the magnetic transducer over the interested die area. The test chip shown above resulted in a pad-limited design with dimension of 1330 µm x 1340 µm. Future layouts will also implement the y-axis matching principle.

Figure 5.16 shows the diagram of the physical test setup used to produce a perpendicular magnetic field over the Hall generator.

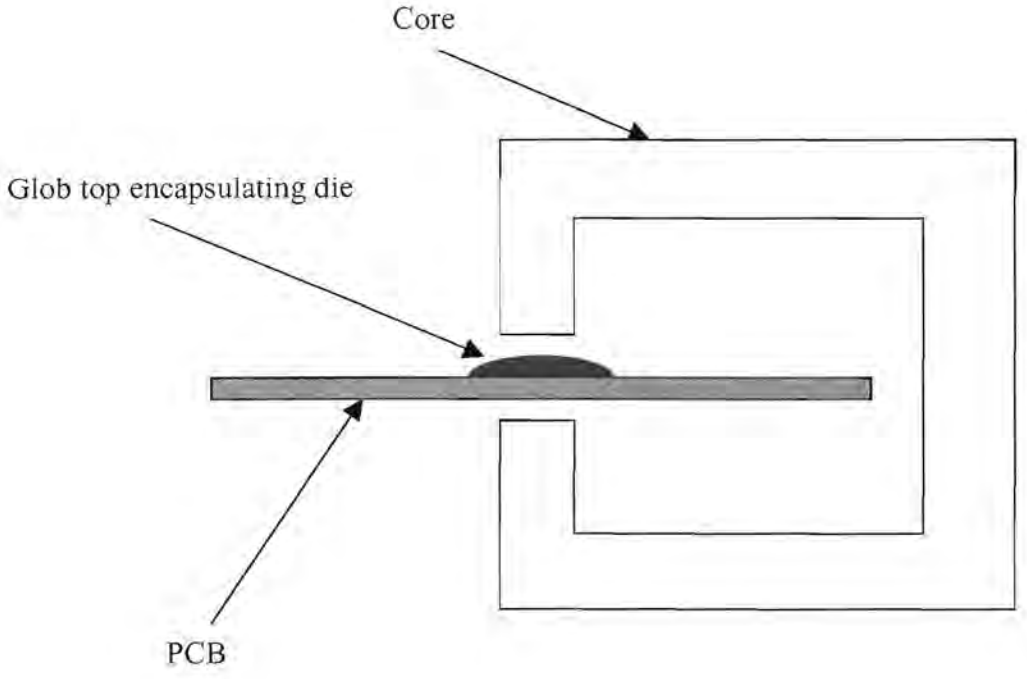

Figure 5.16 Mechanical arrangement for testing of Hall generator

5.6. COMPARISON TO SIMILAR SYSTEMS

It has been noted up to now that the major short fall of the device that was tested was that the signal processing circuitry limited the performance of the power sensor. The comparison has thus been drawn up to include performance specifications of fully integrated power sensor systems on the market using alternative methods of current and voltage sensing as well as the a direct comparison of the Hall generator with respect to the likes of CT's and shunt resistances. The voltage circuits of most power sensors use a similar architecture as proposed in this document.

The most dominant companies in the energy measurement market are our local semiconductor manufacturer South African Micro-Electronic Systems (SAMES) as well as the American based Analog Devices (AD). A comparable product from each company has been used for

comparison with the Hall effect device and will be referred to as the (SAMES) SA2002 [33] and the (AD) AD7755 [34]. These performance specifications will be given in their typical application set up.

5.6.1. SA2002

Circuit operating voltage	5 V
Maximum supply current	typically 3 mA
Operating temperature	-25°C to 85°C
Maximum Line Voltage	230 V_{rms}
Base current	25 A_{rms}
Maximum line current	100 A_{rms}
Line frequency	45 - 65 Hz
Output	Digital pulses proportional to power consumed
System sensitivity (Typical)	18.4 kW/1360 Hz (peak)
Temperature stability for 0.1 $I_b \leq I \leq I_{max}$	< 0.025 %/K
Accuracy for 0.05 $I_b \leq I \leq I_{max}$	< 0.5 % Dynamic range 1000:1
Circuit max consumption	± 25 mW and 4 VA
Current circuit power consumption	1 W (Shunt)

5.6.2. AD7755

Circuit operating voltage	5 V
Maximum supply current	typically 3 mA
Operating temperature	-25°C to 85°C
Maximum Line Voltage	230 V_{rms}
Base current	25 A_{rms}
Maximum line current	100 A_{rms}
Line frequency	45 - 65 Hz
Output	Digital pulses proportional to power consumed
System sensitivity (Typical)	18.4 kW/1360 Hz (peak)
Temperature stability for 0.1 $I_b \leq I \leq I_{max}$	< 0.01 %/K
Accuracy for 0.05 $I_b \leq I \leq I_{max}$	< 0.2 % dynamic range 500:1
Circuit max consumption	± 20 mW
Current circuit power consumption	1 W (Shunt)

Both systems achieve higher performance specifications for use within energy measurement systems. It must however be remembered that the systems mentioned here have evolved over many years and have been market driven into their current state of performance. The most noticeable difference however is that the devices above have to take into consideration all the disadvantages stated in the introduction of this document with respect to higher power consumption in shunt resistors, higher complexity due to phase shift correction needed caused by the CT's implemented as well as the need for these external devices. It will thus be advantageous to rather make a comparison to the sensing elements themselves as signal process circuit development will always evolve such as to drastically improve circuit performance in the future.

CT's are expensive but have the advantage of circuit isolation between line current and measurement device and also consume negligible power. Their disadvantage is that they introduce significant phase shift error that needs to be corrected. The CT's typically used with the above energy measurement devices have typical ratings as illustrated in Table 5.1.

Table 5.1 Table showing linearity and phase errors for current transformers

Contents	Linearity Error (%)			Phase Shift (′) (minutes)		
Current	0.25 A	3 A	5 A	0.25 A	3 A	5 A
Accuracy	0.50 %	0.50 %	0.20 %	25′	25′	10′

A typical shunt resistor can be up to 625 μΩ and thus has its major disadvantage in high power consumption with losses of $P = I^2R$. They are however cheap devices and surface-mount shunts have made for compact systems. Shunt resistors are inserted in series into the current line and thus do not isolate the current sensing circuit from the main line. Linearity for these devices is extremely good. The results are shown in Table 5.2.

Table 5.2 Table showing linearity error and power consumed for a 625 μΩ shunt resistor

Contents	Linearity Error (%)			Power Consumed (W)		
Current	0.25 A	3 A	80 A	0.25 A	3 A	80 A
Accuracy	Excellent			39 μW	5.63 mW	1 W

Table 5.3 shows the specifications for the Hall generator proposed in this dissertation including its amplifiers and the advantages of this system become clear once compared to the equivalent CT and shunt resistor. It can be deduced that with more accurate amplification

circuits, the device shows great potential to replace its counterparts in certain applications. The power consumed in the device will only be a function of the bias current needed in the element and it can be seen that no phase shift errors are introduced. Furthermore, the linearity of the device is directly comparable with the other devices. The system however has the advantages that it is now fully integrated into the power sensor system and thus eliminates the need for these external devices at the cost of increased die area. The only disadvantage is that the linearity deteriorates quickly at low current levels but many ways exist to compensate for this.

Table 5.3 Table showing linearity error, power consumed and phase error for the Hall generator

Contents	Linearity Error (%)			Phase Shift (′) (minutes)			Power Consumed (W)
Current	0.25 A	3 A	5 A	0.25 A	3 A	5 A	Biased @ 300 μA_{peak}
Accuracy at given current	<1.00 %	<0.5 %	<0.5 %	0′	0′	0′	< 150 μ W

5.7. CONCLUSION

This chapter focused on the Hall multiplication based power sensor system in which the complete sensor system was described. The system was described with reference to the initial system design proposed in chapter 2. The complete system interface was discussed and the final circuit operation was presented. The complete system was simulated and relevant performance specifications were presented and analyzed with specific reference to linearity and temperature based performance characteristics. Specific weaknesses were identified and the underlying reasons for these discussed. Some subsystems of the design were manufactured using the proposed 1.2 μm CMOS process, characterized and compared to simulation data. The IC layout and packaging problems were discussed and methods for overcoming these specific known problems were presented. A micrograph of the design to be manufactured was shown implementing all these strategies discussed. The data was then used to place the work presented here into perspective when compared to other similar systems such that the initial hypothesis of advantages and disadvantages could be analyzed.

6. CONCLUSION

6.1. WHAT WAS GIVEN?

Modern solid-state power meters contain elements for sensing both voltage and current. Resistor dividers are typically used for voltage sensing and current sensing technologies currently deployed in the market include low resistance current shunts, current transformer (CT) and the Hall effect sensor. In energy measurement systems, analog and digital multiplication require circuit overhead and complexity when compared to the use of an integrated Hall generator. This is due to the inherent multiplication properties of the Hall generator and can be implemented such that the output directly represents active power through indirect measurement of the line current and voltage. This reduction in complexity as well as expensive external devices has created the need for investigation into the replacement of conventional sensing methods with the Hall effect multiplier.

6.2. WHAT WAS THE AIM?

Implementing the Hall generator as a two-vector multiplier was the core topic of the research described in this document. It was proposed to design a complete active power sensor based on Hall effect multiplication. The work would thus establish the foundation for implementation into energy measurement systems. It would thus also be established whether the Hall generator would be sufficient as a sensing element and whether its properties can be transformed into an overall system advantage regarding increased economic value, decreased complexity and chip area.

6.3. WHAT HAS BEEN ACCOMPLISHED?

This document described the design of an active power sensor system that utilized the multiplication properties of the Hall generator. Firstly the power sensor architecture was proposed and all circuit requirements were highlighted and discussed. The implementation within traditional watt-hour meters were presented along with the IEC 1036 standard according to which the system performance specifications were measured. The most relevant design considerations were analyzed and were followed by the system requirements for the entire system based on performance, operating conditions and accuracy conformance.

The Hall generator itself was investigated based on the study of well-developed models for galvanomagnetic effects in semiconductors. It was discovered that different geometrical

shapes for Hall generators produce different advantages under different circumstances and that the cross-shape Hall generator was well suited to highly linear applications. A cross-shaped Hall generator was designed for the proposed application, manufactured and tested in a standard 1.2 µm CMOS technology.

The analog signal processing circuitry required by the Hall generator was designed and consisted of the temperature independent reference, biasing circuitry, operational amplifiers, voltage to current converter and instrumentation amplifier. The offset compensation technique was also designed based on the quadrature rotation of the Hall generator that of which was filtered out by the low pass filter circuitry. Transmission gates were used to implement the quadrature rotation. Temperature compensation was implemented using techniques that assist in maintaining constant sensitivity of the Hall generator under varying temperature conditions.

The final system was then designed whereby self-start circuitry was added as required by the bandgap reference as well as the necessary clock buffers necessary for driving the switching circuitry required for offset cancellation. The system was compared to energy measurement devices currently employed on the market with respect to only the relevant factors. The sensor was also compared to other current measurement sensing devices so as to establish grounds for potential improvement. It was found that the energy measurement devices outperformed the proposed sensor even though the IEC specifications were attained but that the Hall sensor itself performed well in comparison to other current sensors.

6.4. WHAT CAN BE LEARNED FROM THIS?

It can be seen that the Hall sensor system as a whole entity did not achieve the performance specifications as those achieved by current energy measurement devices. The system did however achieve the requirements set out by the IEC 1036 standard and it was established that these high performance specifications have been driven by market competitiveness.

By comparing the Hall generator performance to other sensing elements, it was found that the element itself outperforms mainly CT's and has a few advantages over shunt resistors in terms of reduced power consumption. It could thus be established that the limiting factor in terms of circuit performance was mainly the cause of under performing analog circuitry. The result however would be to raise the performance expectations for each individual building block

such that the overall system performance would benefit accordingly. Poor linearity performance of the instrumentation amplifiers serve as the main focus point for potential performance enhancements as more than 90 % of the linearity error was contributed by the configuration.

This iteration served as the foundation for performance specifications as well as a circuit configuration for a fully functional power sensor system. The design was based on specifications set out by the IEC 1036 standard governing such device performance specifics and an attempt was made to implement a design that would comfortably attain these. The interrelationship between different blocks were taken into consideration during the design such as compensation techniques and offset cancellation and data was gathered regarding further improvement steps required by the system. As little literature exists on the subject of Hall effect multipliers, the complete system serves as a basis for greater understanding of the multiplying effect and its implementation.

6.5. WHAT IS THE NEXT STEP?

The step following this design would be to design the system described in this document for use with a suitable analog to digital converter. This would require the final output stage to be modified according to the input requirement of the AD converter. This could entail simple gain settings or even a voltage rather than a current output format. Should the output be required in the form of a voltage signal, temperature compensation would have to be implemented within the Hall generator biasing circuit whereby the biasing current is increased or decreased thus changing the element sensitivity accordingly. Furthermore, better implementations for the voltage to current conversion would be suggested as well as final gain stages as this would dramatically reduce the linearity error and also dominates minimum linearity error restrictions.

The low pass filter was designed as an external sub-system and this would be replaced by an on-chip equivalent. Due to the large values required by passive filters, the system would have to be implemented as an active switched-capacitor system and can potentially be integrated into the final amplification stage [30, 32].

The Hall generator itself presents significant enhancement potential in terms of gain whereby the elements can be physically reduced in size to increase sensitivity. This poses a major

opportunity for performance increases as the sensitivity could be more than doubled this way. The limiting factor here would be established by the technology design rules. Care must be exercised, as this would require a trade-off between device reproducibility versus increased sensitivity as larger variations between devices may be caused as a result of limitations in manufacturing accuracy. This along with certain layout enhancements such as fully integrated instrumentation amplifiers whereby the input pairs of the whole device are integrated as one entity instead of two as implemented in this solution could yield significantly improved performance.

Finally, the whole system would be implemented into an energy measurement device whereby all the performance specifications of similar devices as mentioned in this document will serve as the benchmark of achievement. Attaining these specifications would result in a product of high economical value when compared with these devices.

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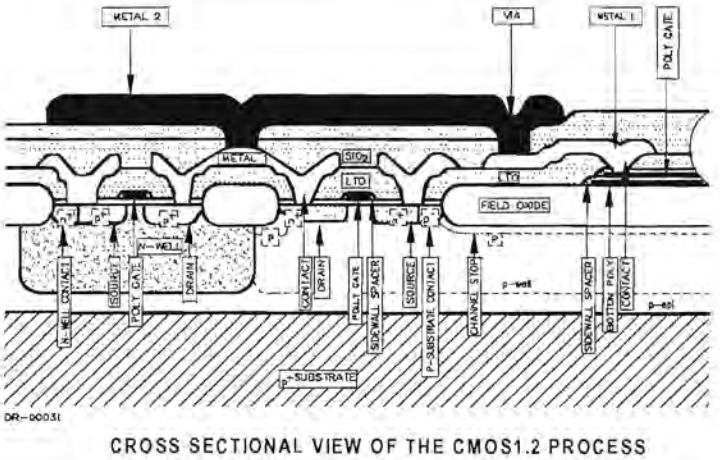
ADDENDUM A: 1.2µM CMOS PROCESS PARAMETERS

sames

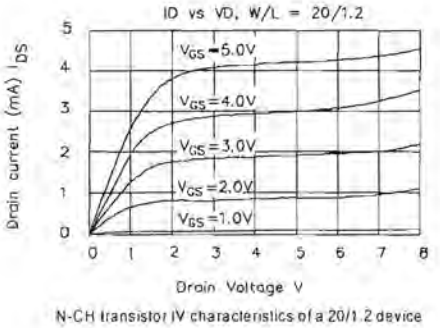
CMOS1.2 Process

Physical Characteristics

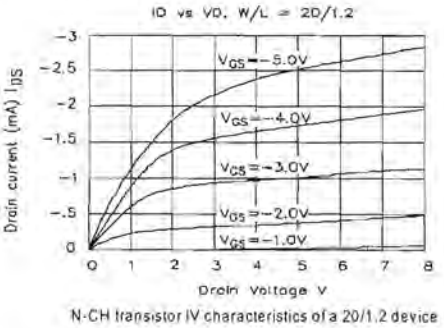
Process Geometry	1.2 Micron	Metal II Width	2.0µ
Process Number	C1201(S.M)/C1202(D.M)	Metal II Space	2.0µ
Operating Voltage	5v	Gate Poly Width	1.2µ
Well Doping	N-WELL	Gate Poly Space	1.8µ
Metal Layers	2	Bottom Poly Width	3.0µ
Poly Layers	2	Bottom Poly Space	2.0µ
Contact	1.5µ	N+/P+Space	2.0µ
Via	1.5µ	N+ to N-WELL	7µ
Metal I Width	2.0µ	N+ to P+	9µ
Metal I Space	2.0µ		



CROSS SECTIONAL VIEW OF THE CMOS1.2 PROCESS



N-CH transistor IV characteristics of a 20/1.2 device



N-CH transistor IV characteristics of a 20/1.2 device

CMOS1.2 Process

Electrical Characteristics

n-ch transistor (T = +25°C unless otherwise noted)

Parameters	Sym	Min	Typ	Max	Unit	Comments
Threshold Voltage (linear extrapolated)	VTO_N	0.55	0.75	0.95	V	100/1.2 device
Body Factor	γ		0.35		$V^{1/2}$	100/1.2 device
Conduction factor (normalized)	b_N	60	75	90	µA/V²	100/100 device
Effective Channel Length	$Leff_N$	0.7	0.9	1.1	µm	100/1.2 device
Width Encroachment	DW_N		0.6		µm	per side
Punch Through Voltage	$BVDSS_N$	9			V	100/1.2 device
Poly Field Threshold	$VTF_{P(N)}$	10			V	
Threshold Voltage Offset (two sigmas)	DVT_N		5		mV	100/10 device

p-ch transistor

Threshold Voltage (linear extrapolated)	VTO_P	-1.1	-0.9	-0.7	V	100/1.2 device
Body Factor	γ		0.4		$V^{1/2}$	100/1.2 device
Conduction Factor (normalized)	b_P	20	25	30	µA/V²	100/100 device
Effective Channel Length	$Leff_P$	0.8	1.0	1.2	µm	100/1.2 device
Width Encroachment	DW_P		0.6		µm	per side
Punch Through Voltage	$BVDSS_P$			-9	V	100/1.2 device
Poly Field Threshold	$VTF_{P(P)}$			-10	V	
Threshold Voltage Offset (two sigmas)	DVT_P		5		mV	100/10 device

diffusion & thin films

Well (field) Sheet Resistance	$R_{W(+I)}$	0.5	1	1.5	kW/□	n-well
N+ Sheet Resistance	R_{N+}	20	30	40	W/□	
N+ Junction Depth	X_{jN+}		0.3		µm	
P+ Sheet Resistance	R_{P+}	60	80	100	W/□	
P+ Junction Depth	X_{jP+}		0.3		µm	
Gate Poly Sheet Resistance (n-ch)	R_{POLYN}	15	25	35	W/□	
Gate Poly Sheet Resistance (p-ch)	R_{POLYP}	15	25	35	W/□	
Bottom Poly Sheet Resistance	R_{POLYB}	15	25	35	W/□	
Metal 1 Sheet Resistance (SLM)	R_{M1}		30		mW/□	
Metal 1 Sheet Resistance (DLM)	R_{M2}		50		mW/□	
Metal 2 Sheet Resistance (DLM)	R_{M2}		30		mW/□	

capacitance

Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Poly Gate To Bottom Poly	C_{PP}		0.86		fF/µm²	interpoly capacitor
Metal 1 to Poly	C_{M1P}		0.057		fF/µm²	
Metal 2 to Metal 1	C_{MM}		0.035		fF/µm²	

SAMES

M68-1780

-2/2-

ADDENDUM B: OPERATIONAL AMPLIFIER DESIGN

Specifications:

- $V_{DD} = 5$ V
- $A_{V(opoen\text{-}loop)} > 80$ dB
- UGBW prod = 1 MHz (stable)
- Slew-rate = 2V/µs

Figure B.6.1 shows the proposed circuit.

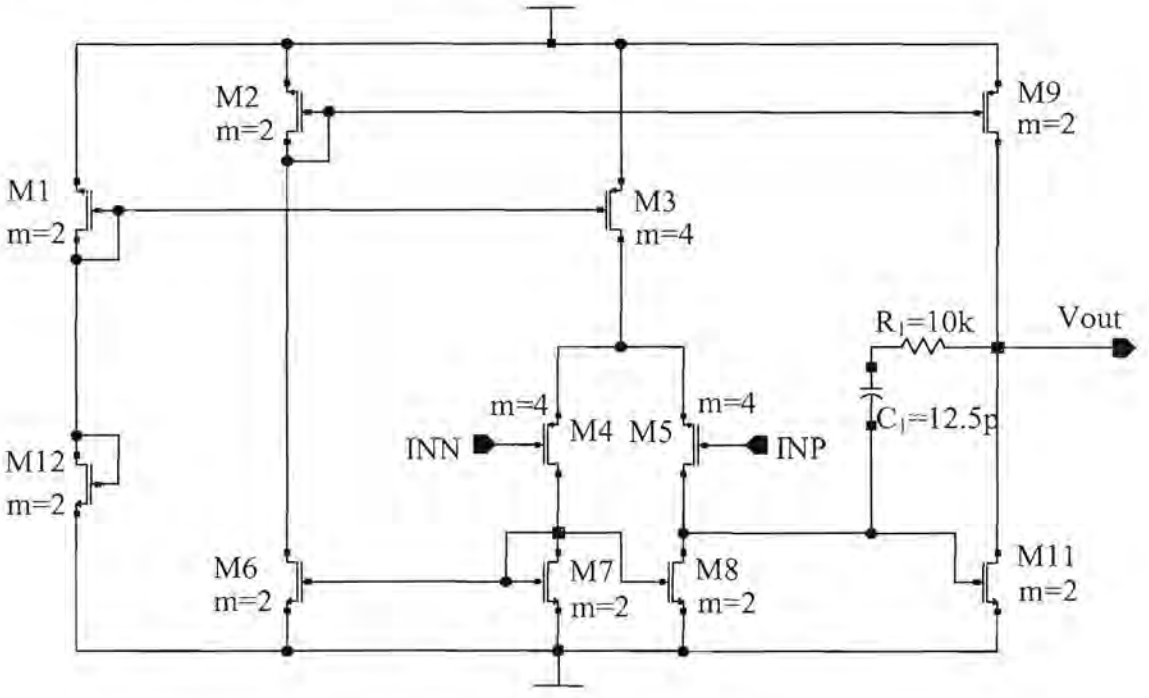


Figure B.6.1 CMOS operational amplifier

Design equations:

$$\frac{SR}{UGBW} = 2\pi\left(V_{GS} - V_t\right) \qquad \text{(B. 1)}$$

$$V_{GS} = \frac{SR}{\left(2\pi\left(UGBW\right)\right)} + V_t \qquad \text{(B. 2)}$$

$$A_V = (A_{V1})(A_{V2})(1) \qquad \text{(B. 3)}$$

The input stage's gate-source voltage can thus be calculated from equation B.3 as

$$V_{GS5} = \frac{2}{2\pi} + 1.0 \qquad (B.4)$$
$$= 1.318V$$

but, we know that

$$A_{V1} = g_{m5}(r_{o5} \,||\, r_{o8}) \qquad (B.5)$$
$$= \frac{g_{m8}}{g_{o8} + g_{o5}}$$

where,

$$g_{m5} = \sqrt{\left(2I_{D5}k_{p'}\frac{W_5}{L_5}\right)} \qquad (B.6)$$

$$g_{o5} = \frac{I_{D5}}{V_{AP}} \qquad (B.7)$$

$$g_{o8} = \frac{I_{D8}}{V_{AN}} \qquad (B.8)$$

From figure B.6.1, it can be seen that

$$I_{D8} = I_{D5} \qquad (B.9)$$

thus,

$$A_{V1} = \frac{\sqrt{\left(2I_{D5}k_p\frac{W_5}{L_5}\right)}}{\left(\frac{2I_{D5}}{V_{AP}}\right)} \qquad (B.10)$$

and so too,

$$A_{V2} = \frac{\sqrt{\left(2I_{D11}k_n\frac{W_{11}}{L_{11}}\right)}}{\left(\frac{2I_{D11}}{V_{AN}}\right)} \qquad (B.11)$$

where,

$$I_{D11} = I_{D5} = \frac{I_3}{2} = 12.5\,\mu\mu \qquad \textbf{(B. 12)}$$

But we know that $\frac{W_{11}}{L_{11}} = 7$, from the bias ratios and thus from equation B.3,

$$\begin{aligned} A_V &= 95dB \approx 56000 \\ &= A_{V1}A_{V2} \\ &= \frac{\sqrt{\left(2I_{D5}k_p\frac{W_5}{L_5}\right)}}{\left(\frac{2I_{D5}}{V_{AP}}\right)} \times \frac{\sqrt{\left(2I_{D11}k_n\frac{W_{11}}{L_{11}}\right)}}{\left(\frac{2I_{D11}}{V_{AN}}\right)} \end{aligned} \qquad \textbf{(B. 13)}$$

From this we can calculate $\frac{W_5}{L_5} < 46.1$. A width/length ratio of approximately $\frac{W_5}{L_5} = 38$, was chosen such as to accommodate for the 1.2 µm process. This will assist in the matching of the devices within the operational amplifier. M_4 is biased the same as M_5 and symmetry is required in the differential stage such that the inverting and non-inverting input transistors amplify symmetrically.

$$I_{D11} = \frac{\mu C_{OX}}{2}\frac{W_{11}}{L_{11}}(V_{GS11} - V_t)^2 \qquad \textbf{(B. 14)}$$

$$12.5 = \left(\frac{75}{2}\right)(7)(V_{GS11} - 0.7)^2 \qquad \textbf{(B. 15)}$$

and thus,

$$V_{GS11} = 0.92\ V \qquad \textbf{(B. 16)}$$

As M_8 is biased under the same conditions as M_7, $V_{DG} = 0$ and thus M_8 will remain in saturation.

Compensation

The compensation capacitor needed is calculated from

$$C_m = \frac{I_T}{SR} \qquad \text{(B. 17)}$$
$$= \frac{25\mu A}{2V/\mu/}$$
$$= 12.5\,pF$$

The resultant pole positions are thus as follows;

$$p_1 = \frac{1}{((C_m + C_2)R_2 + (C_1 + C_m)R_1 + g_2 R_2 R_1 C_m)} \qquad \text{(B. 18)}$$

But the DC gain of the second stage is high and thus

$$p_1 \approx \frac{1}{(g_2 R_1 R_2 C_m)} \qquad \text{(B. 19)}$$

And so;

$$g_8 = \sqrt{2 I_{D5} k_n \frac{W_5}{L_5}} \qquad \text{(B. 20)}$$
$$= \sqrt{(2)(12.5\mu)(75\mu)(7)}$$
$$= 114.56\ \mu A/V$$

$$R_1 = R_2 = r_{OP} || r_{ON} \qquad \text{(B. 21)}$$
$$= \left(\frac{V_{AP}}{I_{D8}}\right) || \left(\frac{V_{AN}}{I_{D8}}\right)$$
$$= \left(\frac{30}{12.5\mu A}\right) || \left(\frac{60}{12.5\mu A}\right)$$
$$= 1.6\ M\Omega$$

$$p_1 \approx \frac{1}{g_2 R_2 R_1 C_m} \qquad \text{(B. 22)}$$
$$= \frac{1}{(14.56\ e\text{-}6)(1.6\ e6)(1.6\ e6)(12.5\ e\text{-}12)}$$
$$= 273\ Hz$$

The second pole is given by

$$p_2 \approx \frac{g_8 C_m}{C_1 C_2 + (C_1 + C_2) C_m} \quad \text{(B. 23)}$$

It was given that μC_{OX} for PMOS and NMOS transistors were 25 µA/V^2 and 75 µA/V^2 respectively. From addendum A the gate capacitance is seen to be 1.4 fF/µm^2 and thus the mobility constants are calculated as μ_e = 536 cm^2/Vs and μ_h = 179 cm^2/Vs.

Now,

$$C_1 = 112\ x\ 3\ x\ 1.4\ e\text{-}15 = 470\ fF \quad \text{(B. 24)}$$

$$C_2 = 28\ x\ 4\ x\ 1.4\ e\text{-}15 = 160\ fF \quad \text{(B. 25)}$$

$$p_2 = \frac{114.56\ \mu A/V \times 12.5\ pF}{470\ fF \times 160\ fF} + 470\ fF + 160\ fF \times 12.5\ pF = 180.1\ MHz \quad \text{(B. 26)}$$

As was mentioned before, the zero introduced by the compensation capacitor does influence CMOS operational amplifiers, thus:

$$z = \frac{g_8}{C_m} = \frac{114.56\ e\text{-}6}{12.5\ e\text{-}12} = 9.2\ MHz \quad \text{(B. 27)}$$

This is not to say that the zero will not affect the stability, as more phase is introduced. To ensure this will be the case, a compensation resistor will be implemented with the value of

$$z = \frac{1}{C_m\left(\frac{1}{g_{m2}} - R_z\right)} \quad \text{(B. 28)}$$

Choosing $R_z > 1/g_{m2}$, will result in moving the zero from the right half plane to the left half plane close to the second dominant pole, where stability can once again be achieved. Here, the zero contributes to positive phase shift. Thus choosing R_z = 10kΩ, results in the zero frequency to be at approximately 10 MHz. This will also affect the UGBW to move as the zero now occurs after the uncompensated RHP zero.

ADDENDUM C: SYSTEM SCHEMATICS

System Simulation

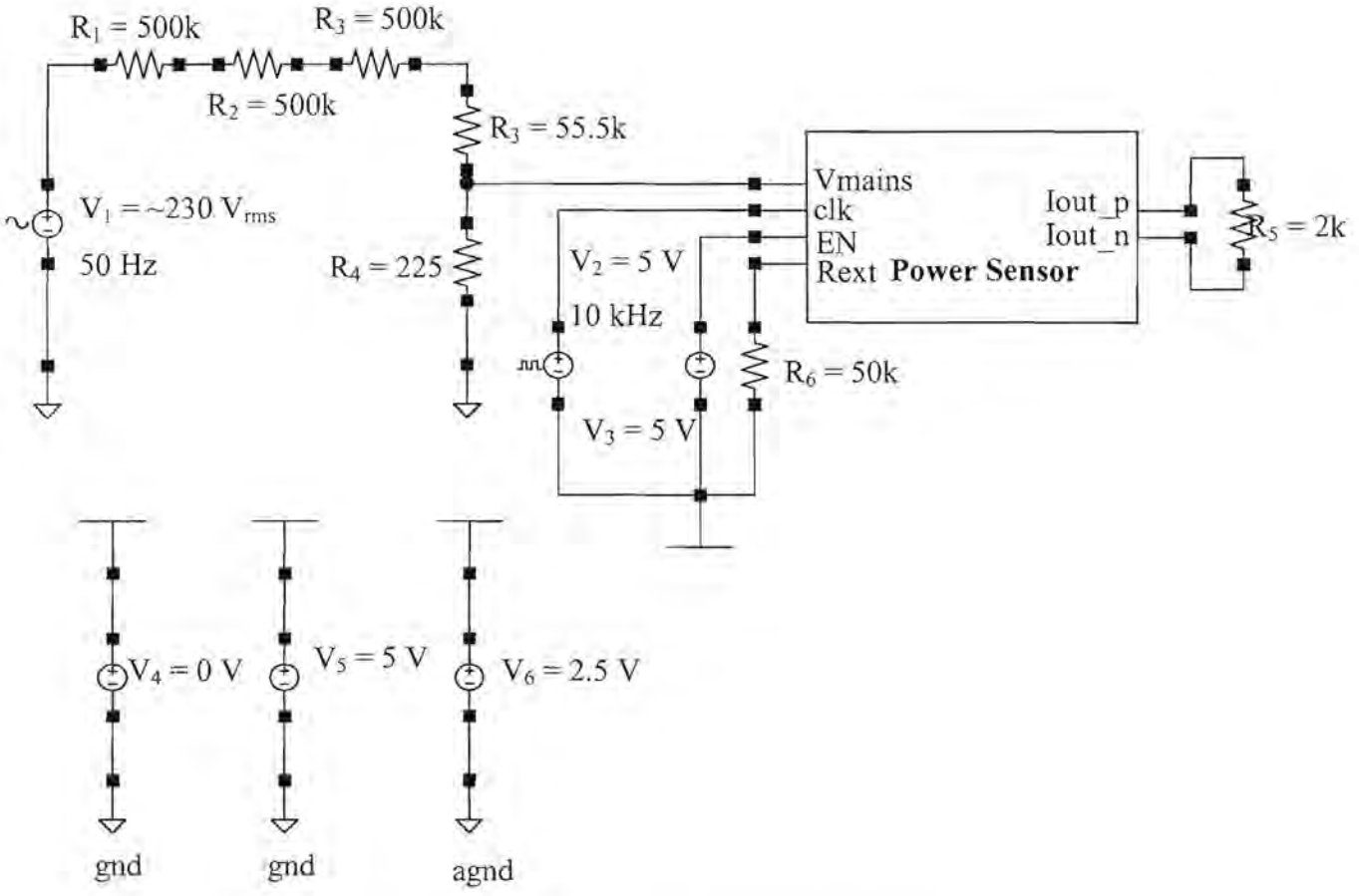


Figure C.1 Schematic illustrating simulation test bench

Figure C.1 illustrates the simulation setup used to simulate the sensor. The voltage divider network can be clearly seen. An external resistor of 50 kΩ is used for calibrating the current bias circuit. The output of the circuit was loaded with a 2 kΩ resistance for simpler result calculations.

Power Sensor

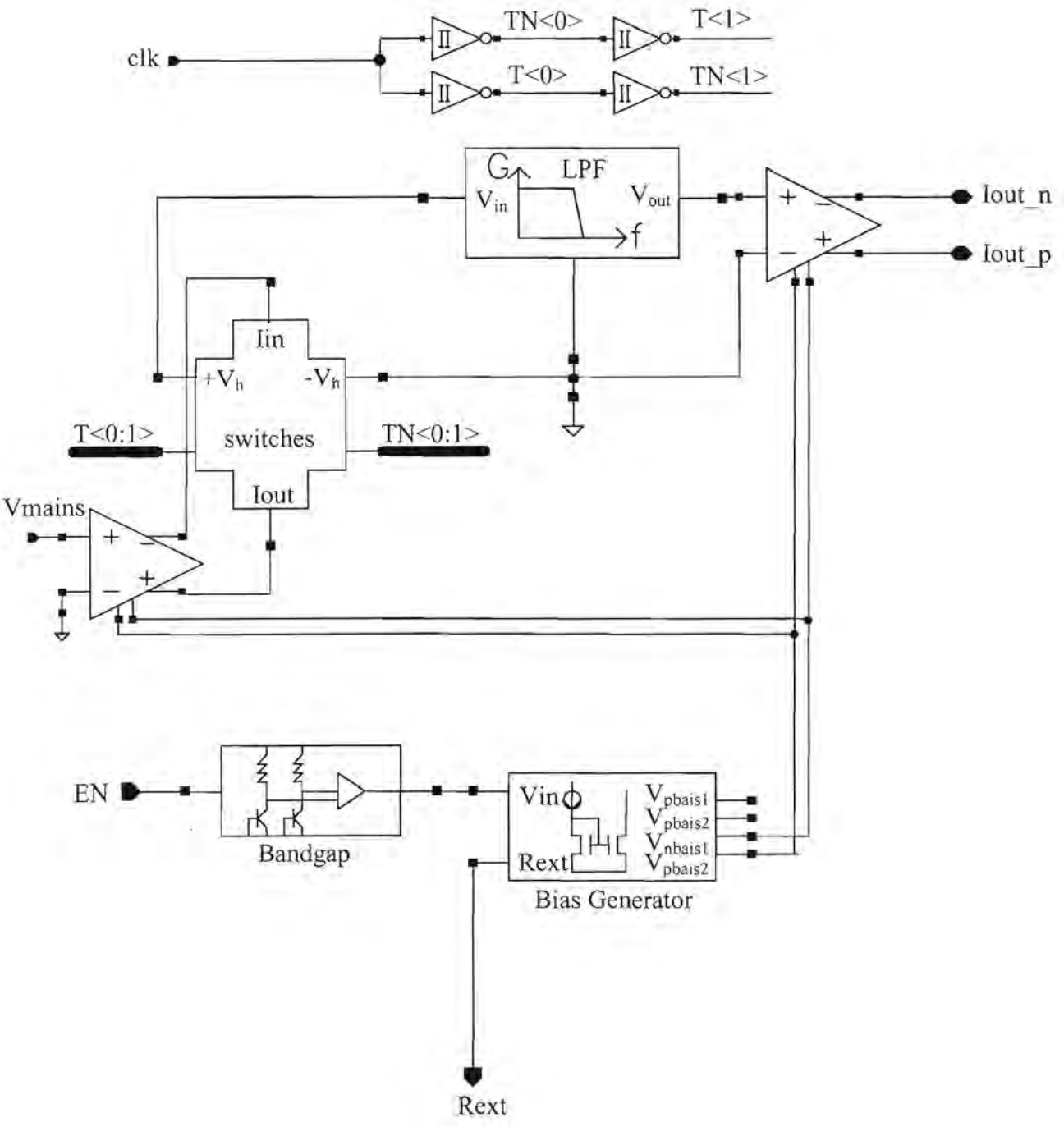


Figure C.2 Schematic of the power sensor system

Figure C.2 shows the entire system schematic of the power sensor. The inputs and outputs are indicated in figure C.1. The amplifier biasing circuits comprises of the bandgap generator (figure C.3) and the current reference generator (figure C.4). The current reference generator uses a self-biased amplifier shown in figure C.5. The biasing amplifier (figure C.6) drives the

Hall generator via the transmission gate switches (figure C.8). The switches are configured such that quadrature rotation is implemented on the Hall generator (figure C.9). This amplifier uses two operational amplifiers shown in figure C.7. The Hall output is low passed filtered (figure C.10) and finally amplified by the final output stage (figure C.6). The 4 inverters generate the clock cycles required by the transmission gates.

Bandgap reference

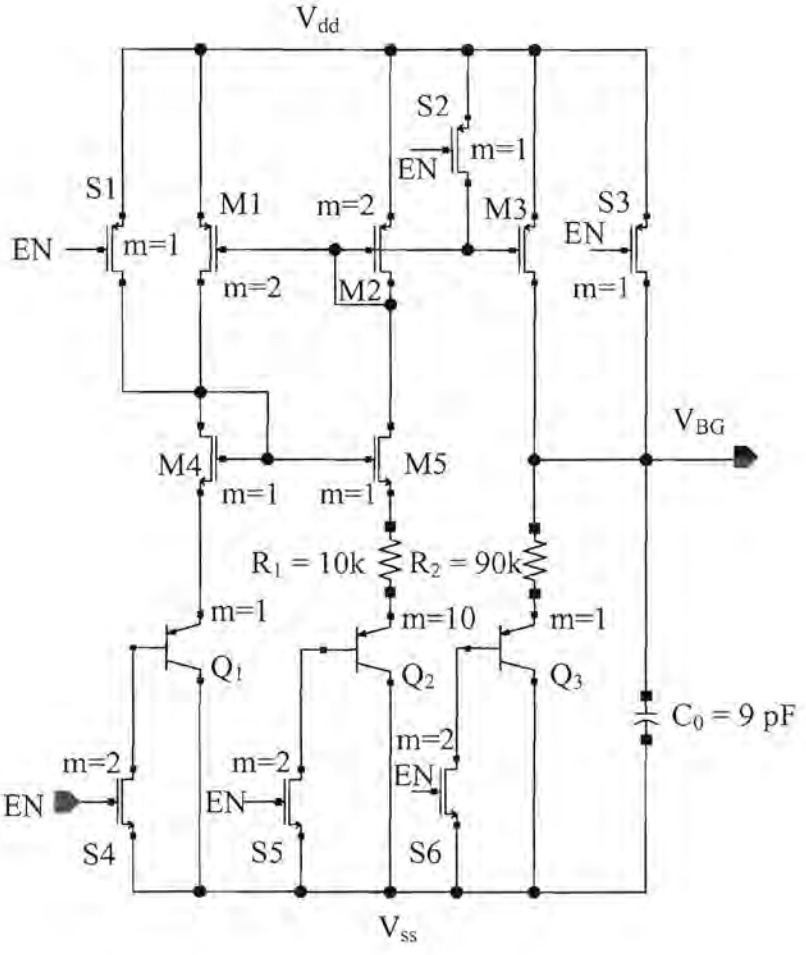


Figure C.3 Bandgap reference schematic

Current bias generator

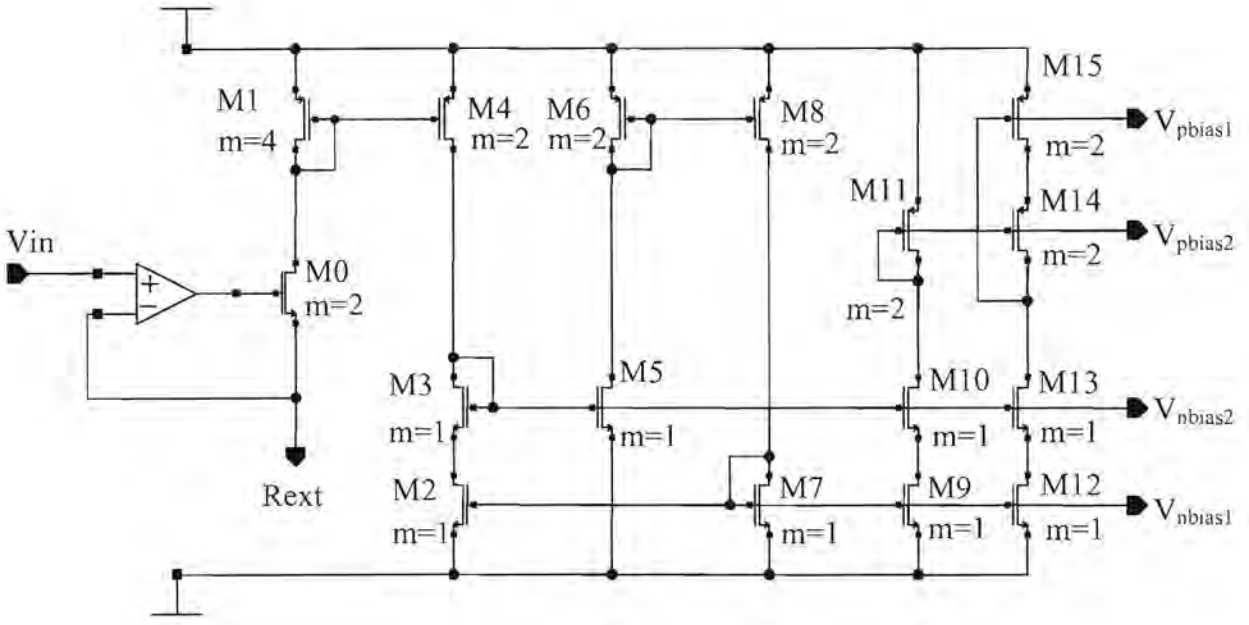


Figure C.4 Current reference generator

Self biased operational amplifier

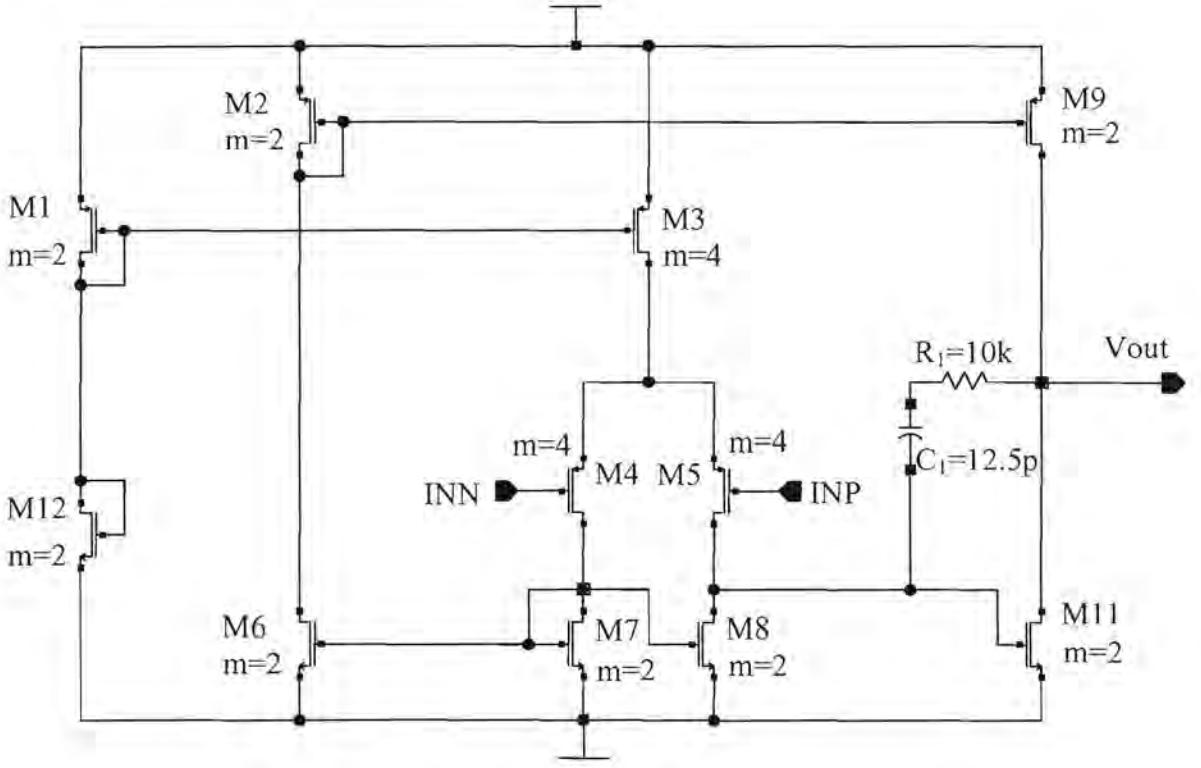


Figure C.5 Operational amplifier used in current reference circuit

Instrumentation amplifier

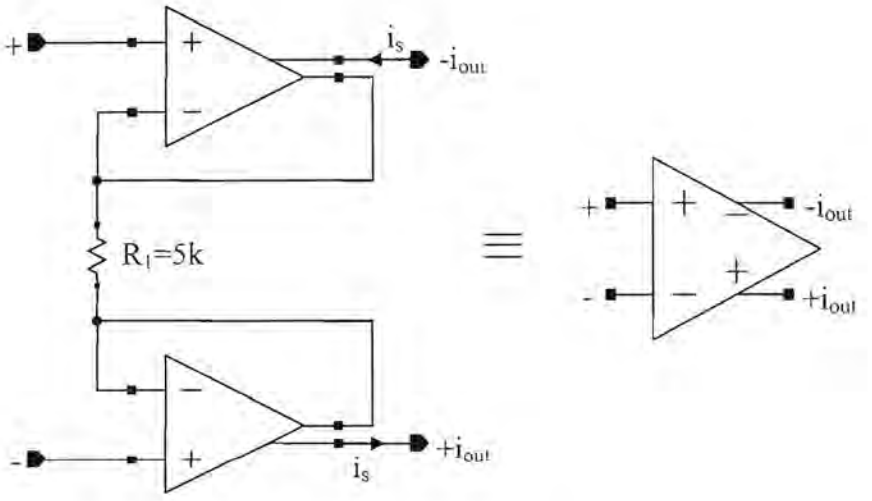


Figure C.6 Instrumentation amplifier

Voltage-to-current converting operational amplifier

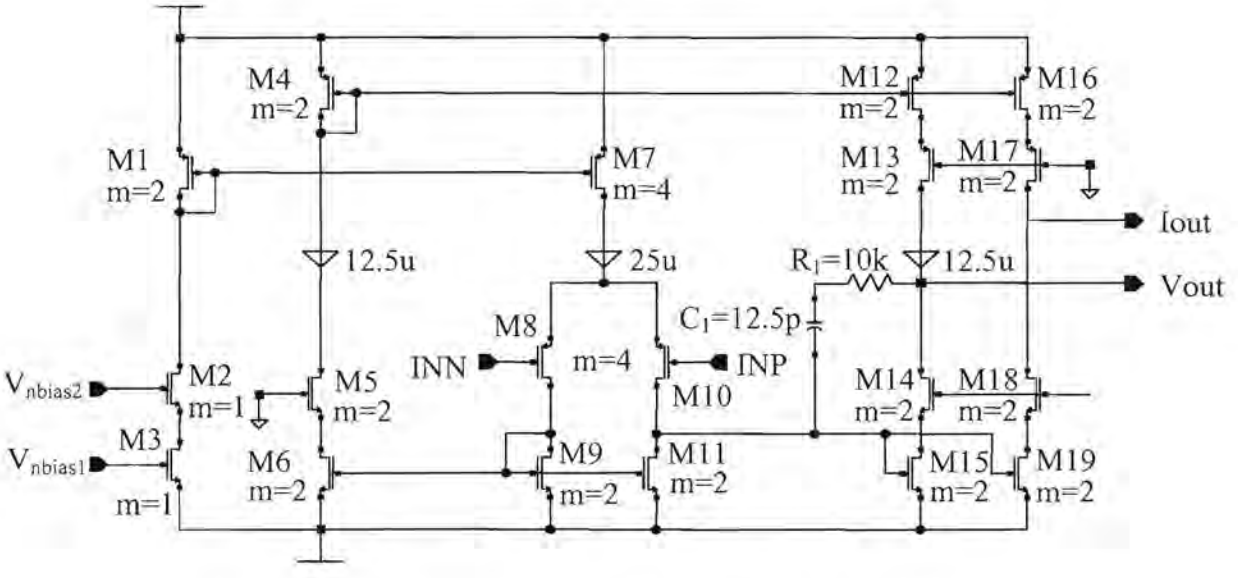


Figure C.7 Operational amplifier implemented in instrumentation amplifiers

Quadrature rotation switching circuitry

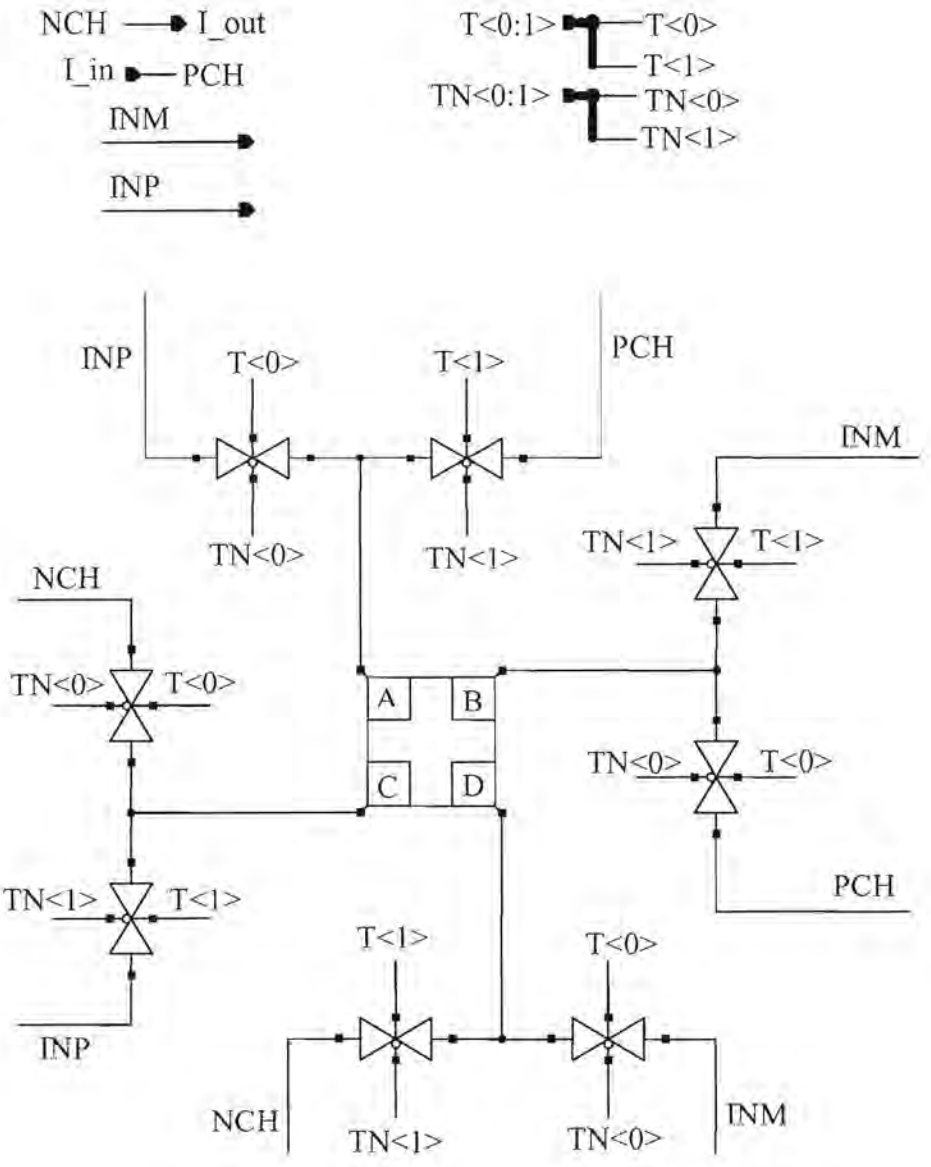


Figure C.8 Transmission gate switching circuitry

Hall generator simulation model

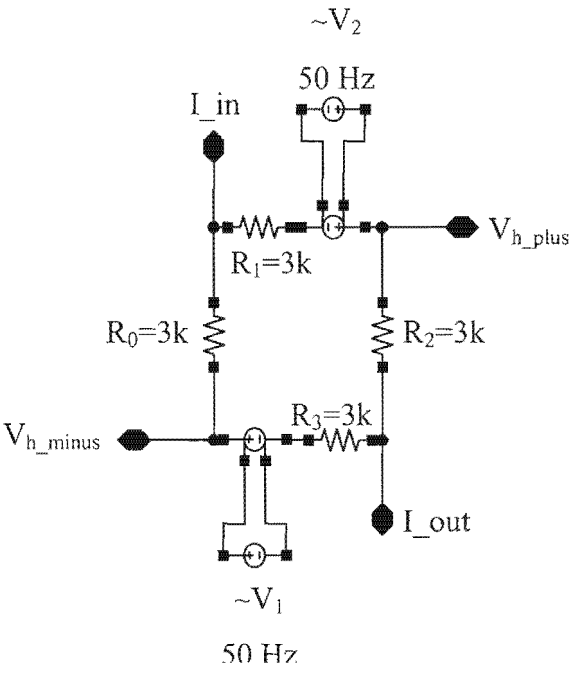


Figure C.9 Hall generator simulation model

Low pass filter

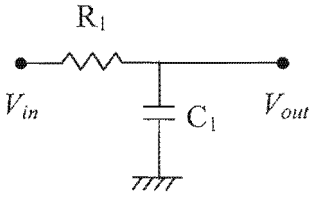
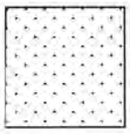


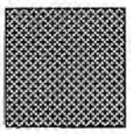
Figure C.10 Passive low-pass filter

ADDENDUM D: LAYOUT LEGEND

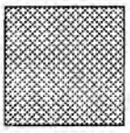

N-Well


N-Active

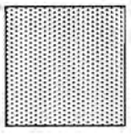

P-Active


Poly 1


Contact


Metal 1


Via


Metal 2