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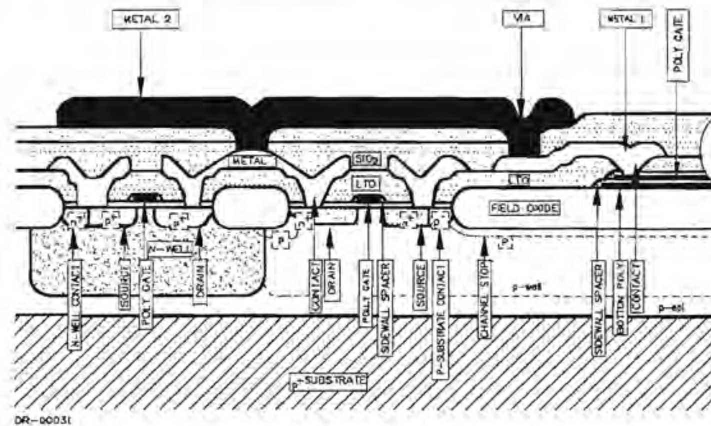
ADDENDUM A: 1.2µM CMOS PROCESS PARAMETERS

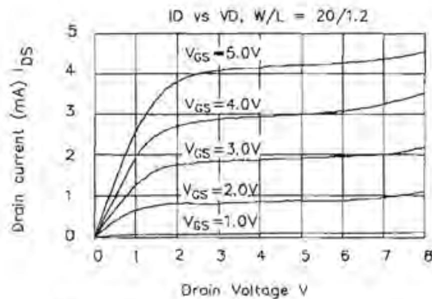
CMOS1.2 Process

Physical Characteristics

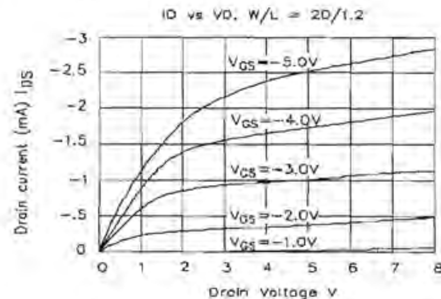
Parameter	Value	Parameter	Value
Process Geometry	1.2 Micron	Metal II Width	2.0µ
Process Number	C1201(S.M)/C1202(D.M)	Metal II Space	2.0µ
Operating Voltage	5v	Gate Poly Width	1.2µ
Well Doping	N-WELL	Gate Poly Space	1.8µ
Metal Layers	2	Bottom Poly Width	3.0µ
Poly Layers	2	Bottom Poly Space	2.0µ
Contact	1.5µ	N+/P+Space	2.0µ
Via	1.5µ	N+ to N-WELL	7µ
Metal I Width	2.0µ	N+ to P+	9µ
Metal I Space	2.0µ		



CROSS SECTIONAL VIEW OF THE CMOS1.2 PROCESS



N-CH transistor IV characteristics of a 20/1.2 device



N-CH transistor IV characteristics of a 20/1.2 device

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CMOS1.2 Process

Electrical Characteristics

n-ch transistor (T = +25°C unless otherwise noted)

Parameters	Sym	Min	Typ	Max	Unit	Comments
Threshold Voltage (linear extrapolated)	VTO_N	0.55	0.75	0.95	V	100/1.2 device
Body Factor	g		0.35		$V^{1/2}$	100/1.2 device
Conduction factor (normalized)	b_N	60	75	90	µA/V²	100/100 device
Effective Channel Length	$Leff_N$	0.7	0.9	1.1	µm	100/1.2 device
Width Encroachment	DW_N		0.6		µm	per side
Punch Through Voltage	$BVDSS_N$	9			V	100/1.2 device
Poly Field Threshold	$VTF_{P(N)}$	10			V	
Threshold Voltage Offset (two sigmas)	DVT_N		5		mV	100/10 device

p-ch transistor

Parameters	Sym	Min	Typ	Max	Unit	Comments
Threshold Voltage (linear extrapolated)	VTO_P	-1.1	-0.9	-0.7	V	100/1.2 device
Body Factor	g		0.4		$V^{1/2}$	100/1.2 device
Conduction Factor (normalized)	b_P	20	25	30	µA/V²	100/100 device
Effective Channel Length	$Leff_P$	0.8	1.0	1.2	µm	100/1.2 device
Width Encroachment	DW_P		0.6		µm	per side
Punch Through Voltage	$BVDSS_P$			-9	V	100/1.2 device
Poly Field Threshold	$VTF_{P(P)}$			-10	V	
Threshold Voltage Offset (two sigmas)	DVT_P		5		mV	100/10 device

diffusion & thin films

Parameters	Sym	Min	Typ	Max	Unit	Comments
Well (field) Sheet Resistance	$R_{W(+f)}$	0.5	1	1.5	kW/□	n-well
N+ Sheet Resistance	R_{N+}	20	30	40	W/□	
N+ Junction Depth	X_{jN+}		0.3		µm	
P+ Sheet Resistance	R_{P+}	60	80	100	W/□	
P+ Junction Depth	X_{jP+}		0.3		µm	
Gate Poly Sheet Resistance (n-ch)	R_{POLYN}	15	25	35	W/□	
Gate Poly Sheet Resistance (p-ch)	R_{POLYP}	15	25	35	W/□	
Bottom Poly Sheet Resistance	R_{POLYB}	15	25	35	W/□	
Metal 1 Sheet Resistance (SLM)	R_{M1}		30		mW/□	
Metal 1 Sheet Resistance (DLM)	R_{M2}		50		mW/□	
Metal 2 Sheet Resistance (DLM)	R_{M2}		30		mW/□	

capacitance

Parameters	Sym	Min	Typ	Max	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Poly Gate To Bottom Poly	C_{PP}		0.86		fF/µm²	interpoly capacitor
Metal 1 to Poly	C_{M1P}		0.057		fF/µm²	
Metal 2 to Metal 1	C_{MM}		0.035		fF/µm²	

ADDENDUM B: OPERATIONAL AMPLIFIER DESIGN

Specifications:

- $V_{DD} = 5$ V
- $A_{V(opoen\text{-}loop)} > 80$ dB
- UGBW prod = 1 MHz (stable)
- Slew-rate = 2V/µs

Figure B.6.1 shows the proposed circuit.

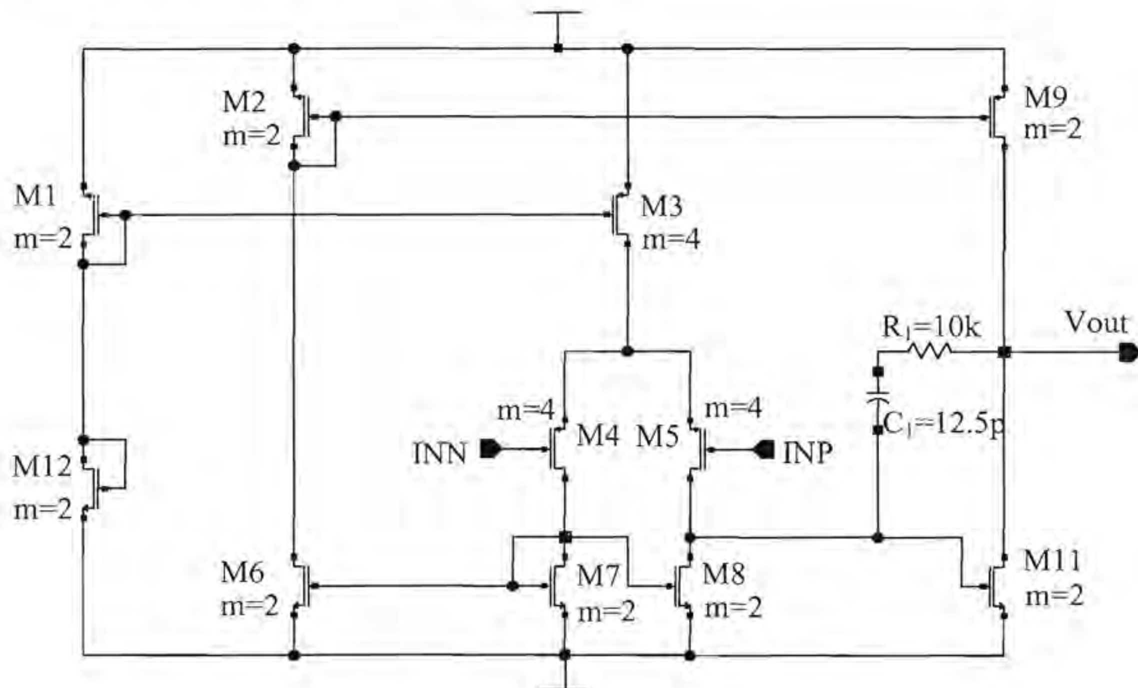


Figure B.6.1 CMOS operational amplifier

Design equations:

$$\frac{SR}{UGBW} = 2\pi(V_{GS} - V_t) \tag{B. 1}$$

$$V_{GS} = \frac{SR}{(2\pi(UGBW))} + V_t \tag{B. 2}$$

$$A_V = (A_{V1})(A_{V2})(1) \tag{B. 3}$$

The input stage's gate-source voltage can thus be calculated from equation B.3 as

$$V_{GS5} = \frac{2}{2\pi} + 1.0 \\ = 1{,}318V \tag{B. 4}$$

but, we know that

$$A_{V1} = g_{m5}(r_{o5} \,||\, r_{o8}) \\ = \frac{g_{m8}}{g_{o8} + g_{o5}} \tag{B. 5}$$

where,

$$g_{m5} = \sqrt{\left(2I_{D5}k_{p} \cdot \frac{W_5}{L_5}\right)} \tag{B. 6}$$

$$g_{o5} = \frac{I_{D5}}{V_{AP}} \tag{B. 7}$$

$$g_{o8} = \frac{I_{D8}}{V_{AN}} \tag{B. 8}$$

From figure B.6.1, it can be seen that

$$I_{D8} = I_{D5} \tag{B. 9}$$

thus,

$$A_{V1} = \frac{\sqrt{\left(2I_{D5}k_p \frac{W_5}{L_5}\right)}}{\left(\frac{2I_{D5}}{V_{AP}}\right)} \tag{B. 10}$$

and so too,

$$A_{V2} = \frac{\sqrt{\left(2I_{D11}k_n \frac{W_{11}}{L_{11}}\right)}}{\left(\frac{2I_{D11}}{V_{AN}}\right)} \tag{B. 11}$$

where,

$$I_{D11} = I_{D5} = \frac{I_3}{2} = 12.5\ \mu\mu \quad \text{(B. 12)}$$

But we know that $\frac{W_{11}}{L_{11}} = 7$, from the bias ratios and thus from equation B.3,

$$\begin{aligned} A_V &= 95dB \approx 56000 \\ &= A_{V1}A_{V2} \\ &= \frac{\sqrt{\left(2I_{D5}k_p\frac{W_5}{L_5}\right)}}{\left(\frac{2I_{D5}}{V_{AP}}\right)} \times \frac{\sqrt{\left(2I_{D11}k_n\frac{W_{11}}{L_{11}}\right)}}{\left(\frac{2I_{D11}}{V_{AN}}\right)} \end{aligned} \quad \text{(B. 13)}$$

From this we can calculate $\frac{W_5}{L_5} < 46.1$. A width/length ratio of approximately $\frac{W_5}{L_5} = 38$, was chosen such as to accommodate for the 1.2 μm process. This will assist in the matching of the devices within the operational amplifier. M_4 is biased the same as M_5 and symmetry is required in the differential stage such that the inverting and non-inverting input transistors amplify symmetrically.

$$I_{D11} = \frac{\mu C_{OX}}{2}\frac{W_{11}}{L_{11}}(V_{GS11} - V_t)^2 \quad \text{(B. 14)}$$

$$12.5 = \left(\frac{75}{2}\right)(7)(V_{GS11} - 0.7)^2 \quad \text{(B. 15)}$$

and thus,

$$V_{GS11} = 0.92\ V \quad \text{(B. 16)}$$

As M_8 is biased under the same conditions as M_7, $V_{DG} = 0$ and thus M_8 will remain in saturation.

Compensation

The compensation capacitor needed is calculated from

$$C_m = \frac{I_T}{SR} = \frac{25\mu A}{2V/\mu/} = 12.5\,pF \tag{B.17}$$

The resultant pole positions are thus as follows;

$$p_1 = \frac{1}{((C_m + C_2)R_2 + (C_1 + C_m)R_1 + g_2 R_2 R_1 C_m)} \tag{B.18}$$

But the DC gain of the second stage is high and thus

$$p_1 \approx \frac{1}{(g_2 R_1 R_2 C_m)} \tag{B.19}$$

And so;

$$g_8 = \sqrt{2 I_{D5} k_n \frac{W_5}{L_5}} = \sqrt{(2)(12.5\mu)(75\mu)(7)} = 114.56\,\mu A/V \tag{B.20}$$

$$R_1 = R_2 = r_{OP} || r_{ON} = \left(\frac{V_{AP}}{I_{D8}}\right) || \left(\frac{V_{AN}}{I_{D8}}\right) = \left(\frac{30}{12.5\mu A}\right) || \left(\frac{60}{12.5\mu A}\right) = 1.6\,M\Omega \tag{B.21}$$

$$p_1 \approx \frac{1}{g_2 R_2 R_1 C_m} = \frac{1}{(14.56\,e\text{-}6)(1.6\,e6)(1.6\,e6)(12.5\,e\text{-}12)} = 273\,Hz \tag{B.22}$$

The second pole is given by

$$p_2 \approx \frac{g_8 C_m}{C_1 C_2 + (C_1 + C_2) C_m} \quad \text{(B. 23)}$$

It was given that μC_{OX} for PMOS and NMOS transistors were 25 μA/V^2 and 75 μA/V^2 respectively. From addendum A the gate capacitance is seen to be 1.4 fF/μm^2 and thus the mobility constants are calculated as μ_e = 536 cm^2/Vs and μ_h = 179 cm^2/Vs.

Now,

$$\begin{aligned} C_1 &= 112 \, x \, 3 \, x \, 1.4 \, e\text{-}15 \\ &= 470 \, fF \end{aligned} \quad \text{(B. 24)}$$

$$\begin{aligned} C_2 &= 28 \, x \, 4 \, x \, 1.4 \, e\text{-}15 \\ &= 160 \, fF \end{aligned} \quad \text{(B. 25)}$$

$$\begin{aligned} p_2 &= \frac{114.56 \mu A/V \times 12.5 \, pF}{470 \, fF \times 160 \, fF} + 470 \, fF + 160 \, fF \times 12.5 \, pF \\ &= 180.1 \, MHz \end{aligned} \quad \text{(B. 26)}$$

As was mentioned before, the zero introduced by the compensation capacitor does influence CMOS operational amplifiers, thus:

$$\begin{aligned} z &= \frac{g_8}{C_m} \\ &= \frac{114.56 \, e\text{-}6}{12.5 \, e\text{-}12} \\ &= 9.2 \, MHz \end{aligned} \quad \text{(B. 27)}$$

This is not to say that the zero will not affect the stability, as more phase is introduced. To ensure this will be the case, a compensation resistor will be implemented with the value of

$$z = \frac{1}{C_m \left(\frac{1}{g_{m2}} - R_z \right)} \quad \text{(B. 28)}$$

Choosing $R_z > 1/g_{m2}$, will result in moving the zero from the right half plane to the left half plane close to the second dominant pole, where stability can once again be achieved. Here, the zero contributes to positive phase shift. Thus choosing R_z = 10kΩ, results in the zero frequency to be at approximately 10 MHz. This will also affect the UGBW to move as the zero now occurs after the uncompensated RHP zero.

ADDENDUM C: SYSTEM SCHEMATICS

System Simulation

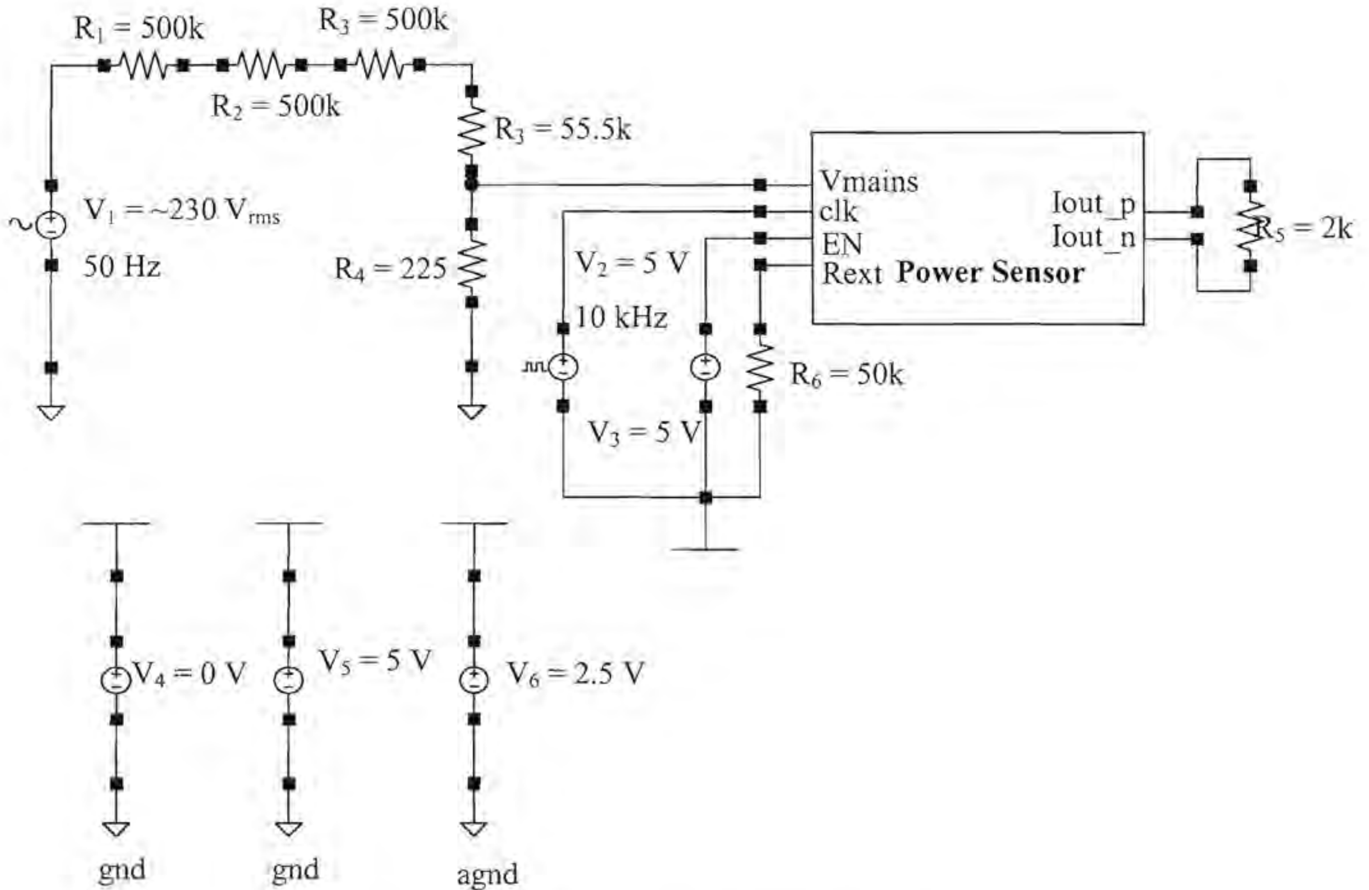


Figure C.1 Schematic illustrating simulation test bench

Figure C.1 illustrates the simulation setup used to simulate the sensor. The voltage divider network can be clearly seen. An external resistor of 50 kΩ is used for calibrating the current bias circuit. The output of the circuit was loaded with a 2 kΩ resistance for simpler result calculations.

Power Sensor

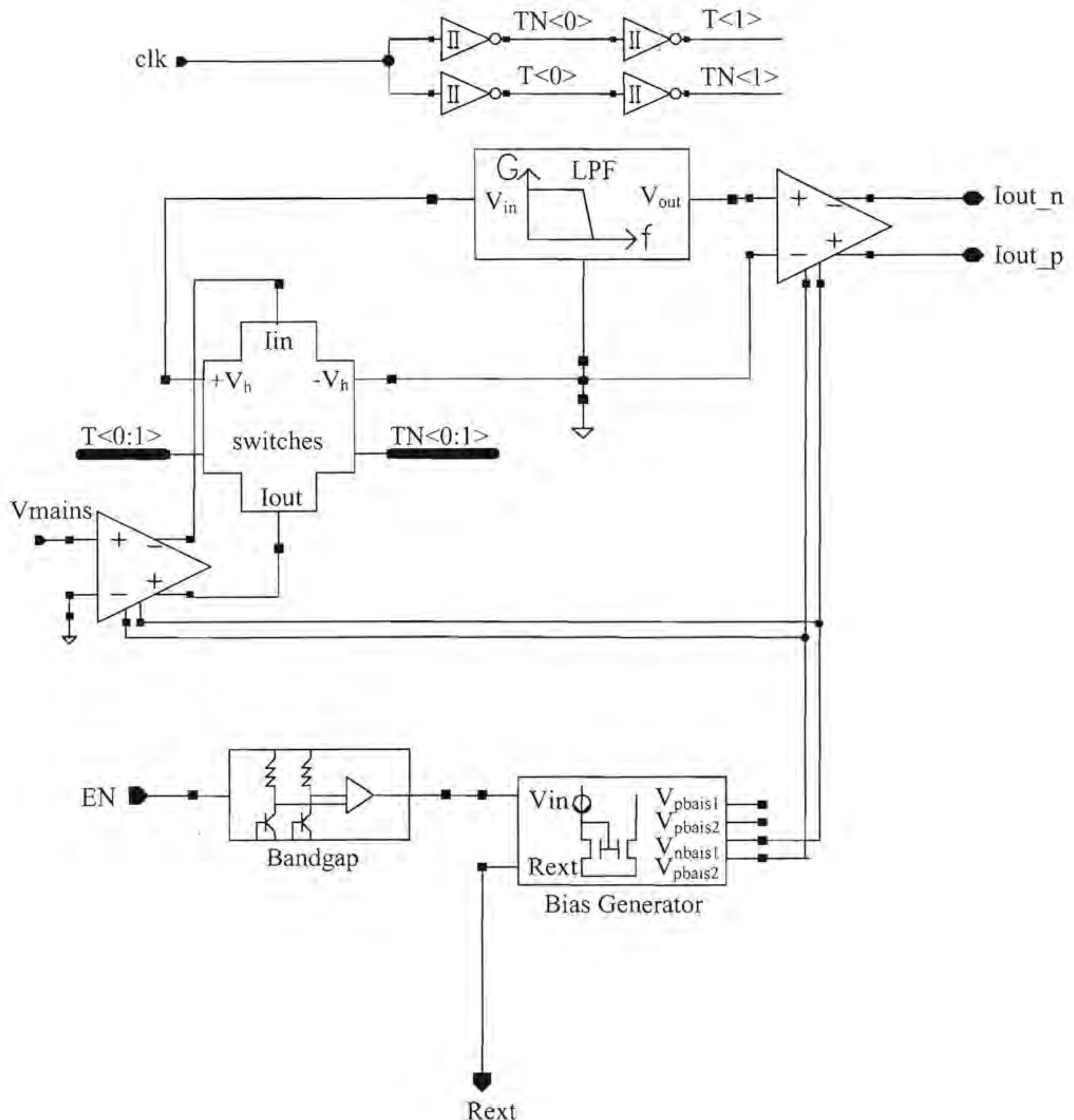


Figure C.2 Schematic of the power sensor system

Figure C.2 shows the entire system schematic of the power sensor. The inputs and outputs are indicated in figure C.1. The amplifier biasing circuits comprises of the bandgap generator (figure C.3) and the current reference generator (figure C.4). The current reference generator uses a self-biased amplifier shown in figure C.5. The biasing amplifier (figure C.6) drives the

Hall generator via the transmission gate switches (figure C.8). The switches are configured such that quadrature rotation is implemented on the Hall generator (figure C.9). This amplifier uses two operational amplifiers shown in figure C.7. The Hall output is low passed filtered (figure C.10) and finally amplified by the final output stage (figure C.6). The 4 inverters generate the clock cycles required by the transmission gates.

Bandgap reference

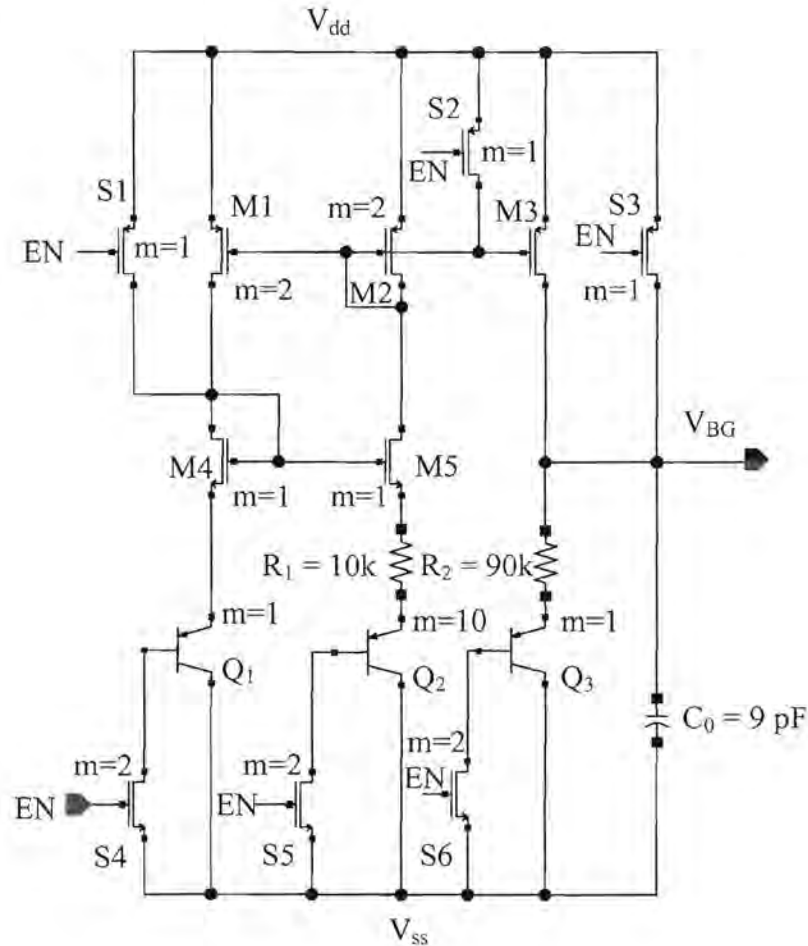


Figure C.3 Bandgap reference schematic

Current bias generator

Figure C.4 Current reference generator

Self biased operational amplifier

Figure C.5 Operational amplifier used in current reference circuit

Instrumentation amplifier

Figure C.6 Instrumentation amplifier

Voltage-to-current converting operational amplifier

Figure C.7 Operational amplifier implemented in instrumentation amplifiers

Quadrature rotation switching circuitry

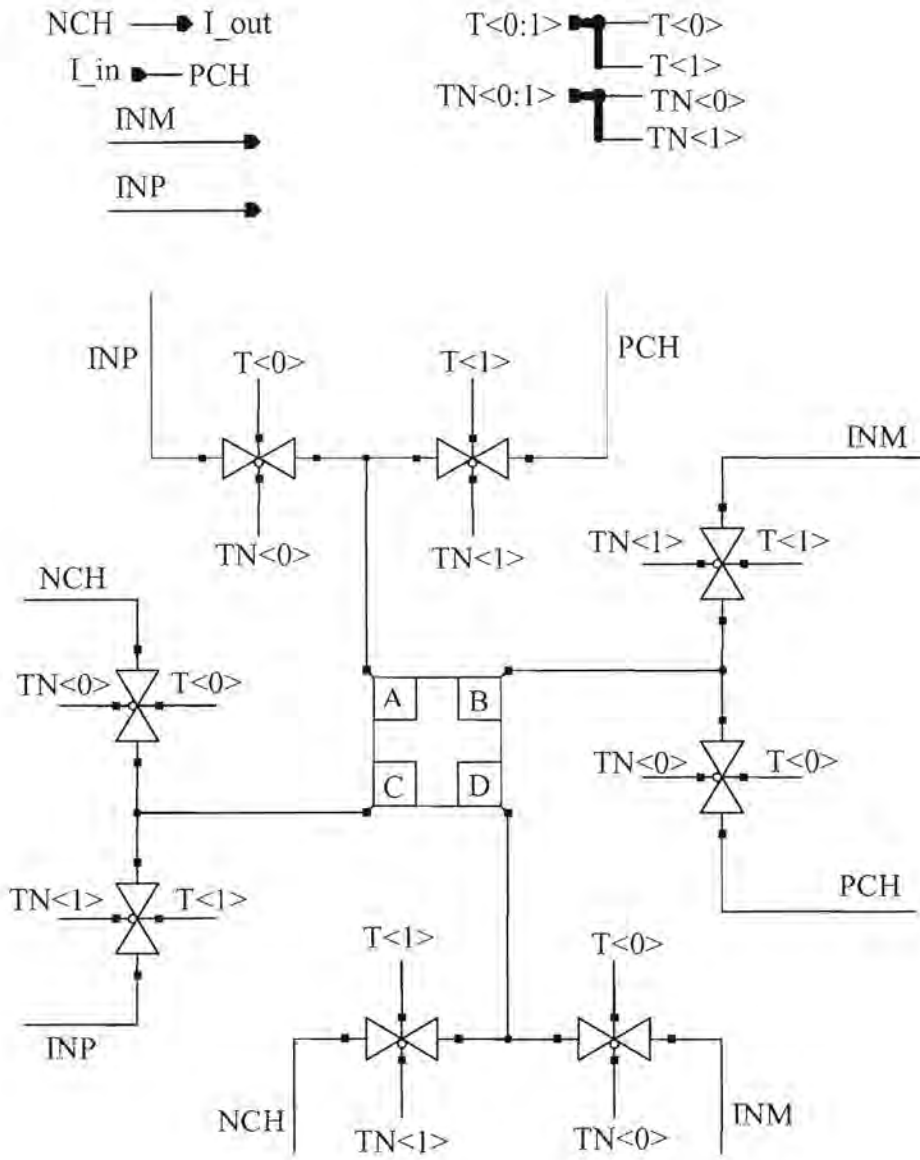


Figure C.8 Transmission gate switching circuitry

Hall generator simulation model

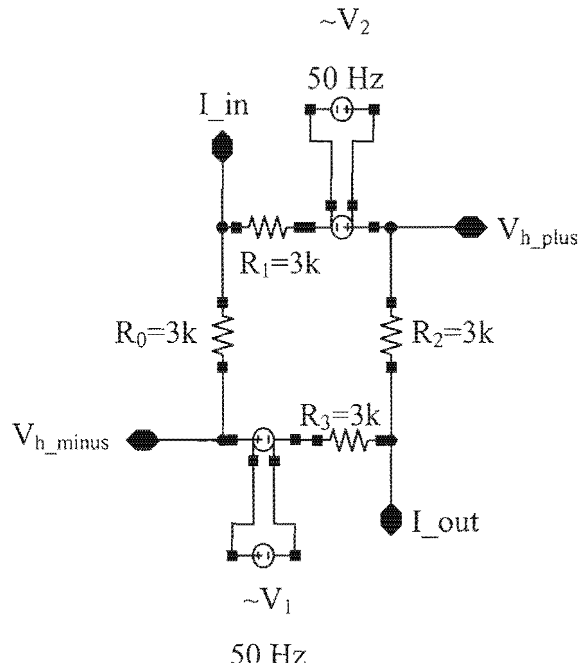


Figure C.9 Hall generator simulation model

Low pass filter

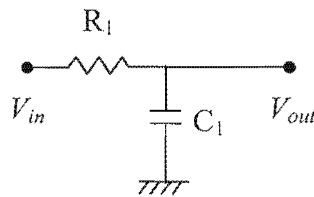
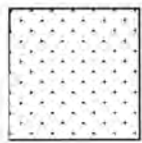


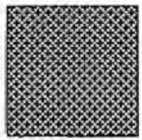
Figure C.10 Passive low-pass filter

ADDENDUM D: LAYOUT LEGEND

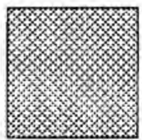

N-Well

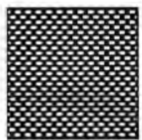
N-Active

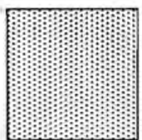
P-Active


Poly 1

Contact


Metal 1


Via


Metal 2