4. SIGNAL PROCESSING CIRCUITRY

4.1. INTRODUCTION

The successful extraction of the information superimposed on the Hall voltage requires for the correct analog signal processing circuits to be developed. The objective of analog circuit design is to transform the specifications into hardware capable of attaining these specifications. As integrated circuit design is a technology driven activity, it will be necessary to base all the designs specifically with reference to the proposed technology. The Hall voltage is an extremely small signal and contains both DC and AC noise. For this reason it will be necessary to focus the design procedure to contain the relevant voltage to current converters, temperature independent voltage and current referencing circuitry, amplification circuits, offset compensation circuitry and filtering elements necessary for implementation of the power sensor. Lastly, as the device is intended for use within watt-hour meters, the mechanical requirements will be discussed for completion.

This chapter will thus be divided into four major categories covering the design aspects of the aforementioned signal processing circuits. The discussion will start with temperature independent voltage and current referencing circuitry, as most analog circuits require biasing usually derived from the referencing circuitry. This will then be followed with the design of the voltage to current converter as required for biasing the Hall plate. The amplifiers follow, along with the offset cancellation and filtering circuits. The four categories will be grouped as follows:

- Temperature independent voltage and current referencing circuitry,
- Voltage to current converter,
- Amplifier circuits,
- Offset cancellation and filtering.

4.2. TEMPERATURE INDEPENDENT BIASING

Analog circuits extensively make use of voltage and current references. These references are dc quantities that are independent of process parameters and supplies and show a well-defined behavior regarding temperature. Many circuits rely on this for proper functionality for example the gain of a differential pair is directly dependant on its biasing current. For this

reason, this section focuses on the design of a stable biasing source that can be used for biasing other analog devices within the power sensor. The core of the biasing source will be based on well-established "bandgap" techniques [28]. The section starts off with a basic explanation of the temperature independent reference as will be implemented in the biasing source. The bias source will then be presented and will be used to bias all subsequent devices.

4.2.1. The Bandgap Reference

The bandgap principle is based on the fact that if two quantities with opposite temperature coefficients (TCs) are added with proper weighting, the resultant displays a zero TC. In equation (4.1) α_1 and α_2 are chosen such that equation (4.2) is satisfied.

$$V_{ref} = \alpha_1 V_1 + \alpha_2 V_2 \tag{4.1}$$

$$0 = \alpha_1 \frac{\partial V_1}{\partial T} + \alpha_2 \frac{\partial V_2}{\partial T} \tag{4.2}$$

The characteristics of bipolar transistors have proven to be the most reliable in terms of reproducibility for producing both positive and negative TCs. These techniques have also been successfully implemented in CMOS technology.

Negative-TC Voltage

The negative TC stems from the forward bias voltage of a pn-junction diode. A diode connected bipolar transistor can perform this function. Equation (4.3) defines a diode-connected transistor's collector current and from this we can define the base-emitter voltage as a function of temperature.

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{4.3}$$

Now,

$$V_T = \frac{kT}{q} \tag{4.4}$$

and

$$I_S \propto \mu k T n_i^2 \tag{4.5}$$

where,

$$\mu \propto \mu_0 T^m \tag{4.6}$$

and $m \approx -3/2$. Also

$$n_i^2 \propto T^3 e^{\frac{-E_g}{kT}} \tag{4.7}$$

with $E_g \approx 1.12$ eV, the bandgap energy of silicon. Solving for V_{BE} in equation (4.3), substituting and taking the derivative with respect to temperature yields the temperature coefficient for the diode as in equation (4.8) with a constant collector current is assumed.

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - \frac{E_g}{q}}{T} \tag{4.8}$$

As can be seen, the temperature coefficient shows that V_{BE} itself is dependent on temperature thus a zero TC can only be achieved at a specific temperature. This is illustrated later.

Positive-TC Voltage

If two identical transistors i.e. $I_{S1} = I_{S2}$, are biased at collector currents of nI_0 and I_0 and their base currents are negligible, then the difference between the base-emitter voltages exhibits a positive-TC as in equation (4.10).

$$\Delta V_{BE} = V_T \ln n \tag{4.9}$$

and

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n \tag{4.10}$$

Where k, is Boltzmann's constant. This TC is independent of temperature or the collector currents as long as high-level injection does not occur.

These coefficients can now be combined to develop the desired reference according to equation (4.2). The base-emitter voltage of a vertical parasitic PNP bipolar transistor at 300 K

for the proposed technology is V_{BE} = 630 mV @ I_C = 12 µA. Substituting these values in equation (4.8), the temperature coefficient is calculated as –1.84 mV/°K. Also, from equation (4.10), $\partial V_T/\partial T$ = +86.17 µV/°K. Substituting these results into equation (4.2) and choosing α_1 = 1 at room temperature, then ($\alpha_2 \ln n$)(0.08617 mV/°K) = 1.84 mV/°K. Thus $\alpha_2 \ln n \approx 21.4$ and

$V_{REF} \approx V_{BE} + 21.4V_T \approx 1.16$ V @ 300K.

The circuit that will realize this function is shown in figure 4.1. In the circuit we can see that M4 and M5 keep their source potentials at the same quantity. To achieve this, M2 adjusts its drain potential such as to compensate for the difference in the currents in the two branches thus balancing the circuit. This forms part of the positive-TC component. The potential established at the gate of M1 and M2 are then added to another proportional to absolute temperature (PTAT) base-emitter voltage namely $I_{D3}R_2$, resulting in equation (4.11).

$$V_{ref} = V_{BE3} + \frac{R_2}{R_1} V_T \ln n \qquad (4.11)$$

Thus for α_1 = 1 and (R_2/R_1)ln $n \approx 21.4$, a ratio of approximately 9.28 results for R_2/R_1. As these resistors will be implemented using n-well resistors, it is necessary to keep them as small as possible such as to minimize consumed area. For repeatability, these resistors should be larger than 5 kΩ for the given technology and to maximize matching, a resistance of 90 kΩ and 10 kΩ is chosen. Although resistors exhibit incredibly high tolerances in IC's, their ratios are very well matched and matching tolerances lower than 1 % can be achieved using many different layout techniques. The technique that will be used here for all resistances will be that of the common centroid principle and thus the resistors will be broken into 10 kΩ strips and placed using this principle. The switches S1 to S6 are used for the starting up of the circuit. As there are two possibilities for reaching equilibrium within the circuit, namely zero and the bandgap voltage, it is necessary to "kick start" the circuit so as to ensure that the equilibrium point is approached from the highest supply rail. This will then force the first stable point reached to be that of the bandgap voltage. In principle, the switches are kept closed for a few milliseconds longer during power up and will be performed by a standard cell from the technology library specifically designed to perform this operation. The switches will be a minimum size of 4µm/1.5µm. A 9 pF capacitor is added for stability purposes. The transistors are designed such that they are capable of carrying the current expected in the circuit.

Furthermore, all PMOS transistors have double the width/length ratio as compared to the NMOS transistors to compensate for the difference in carrier mobility between them.

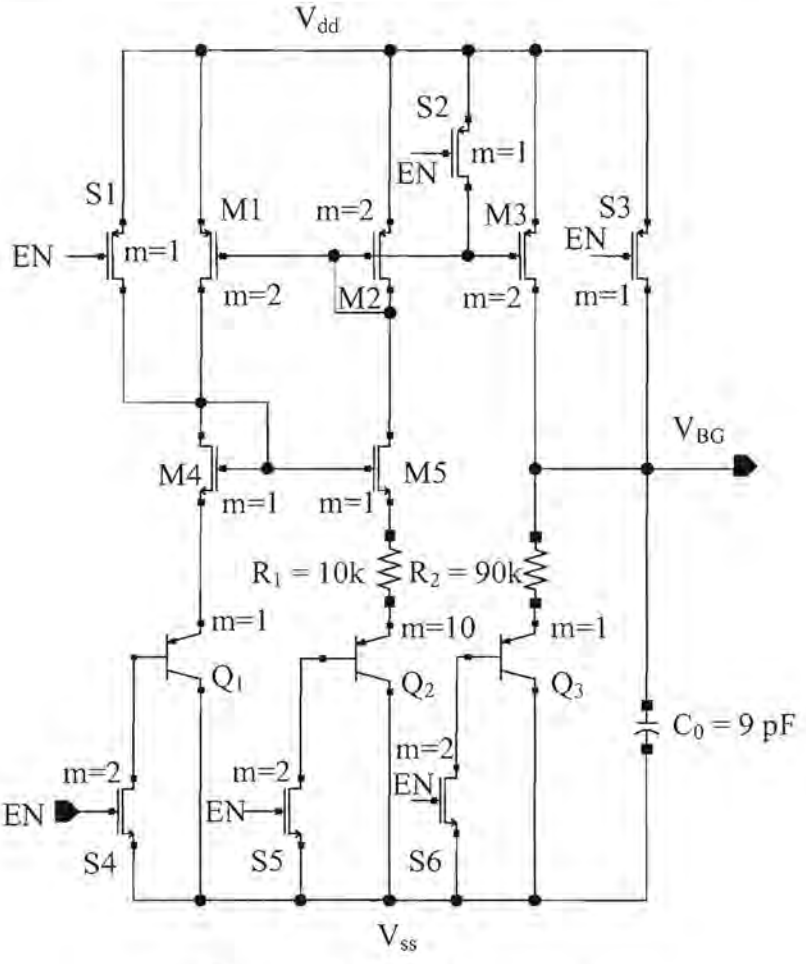

Figure 4.1 Bandgap reference circuit

4.2.2. The Current Reference

The current reference circuit is based on the current mirror principle [28, 29]. The ideal current reference (source or sink) reproduces a reference current that is equal in magnitude and displays an infinitely high output resistance. As we are working with real quantities and technological parameters, a current reference circuit displays finite small-signal output impedance and an output current close to the reference current. Furthermore, the output voltage at the current reference node in which this relation is valid is also not rail-to-rail.

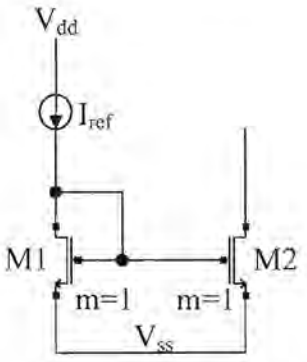

Figure 4.2 Simple current mirror

Figure 4.2 shows the architecture of a simple current mirror. The current ratio between M1 and M2 is derived from the drain current relationship for a transistor in saturation and is shown in equation (4.12) and (4.13). If the gate voltages are kept equal, the current through each transistor will be equal if the process parameters are closely matched and the width/length ratio is equal. Furthermore, it can be seen that it is possible to scale the current between the transistors simply by varying the width/length ratio.

$$I_D = \frac{k}{2}\frac{W}{L}\left(V_{gs} - V_t\right)^2 \qquad (4.12)$$

$$\frac{I_{D1}}{I_{D2}} = \frac{k_1}{k_2}\left(\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}}\right)\frac{\left(V_{gs1} - V_{t1}\right)^2}{\left(V_{gs2} - V_{t2}\right)^2} \qquad (4.13)$$

The output impedance is taken at the drain of M2 and is given according to the small signal analysis model as

$$r_{out} = \frac{1}{g_{ds2}} \approx \frac{1}{\lambda I_{D2}} \qquad (4.14)$$

From equation (4.14) it is seen that the output impedance is dependent on the channel length modulation factor of the process. Making the length of the transistor somewhat larger than the minimum specified size of the transistor will effectively reduce this effect. As the proposed technology uses a minimum width of 1.2 µm, experimentation has shown that a length of at least two to three times more than this is sufficient to reduce this effect such that it is

negligible. Figure 4.3 show the proposed current referencing circuit and are based on the more improved cascode configuration. This implies that the output impedance is significantly improved by a factor $g_{m\_out}r_{ds\_out}$, as seen in equation (4.15).

$$r_{out} = \frac{g_{m\_out}r_{ds\_out}}{g_{m\_out\_old}} \qquad (4.15)$$

The stability of the current source is thus significantly increased. The circuit uses an operational amplifier to generate an accurate reference voltage according to the bandgap reference voltage. This voltage is then applied to an external resistance according to Ohm's law to generate an accurate reference current that will be mirrored into all subsequent devices. In doing so, the high tolerances of on chip resistors are eliminated and the possibility for trimming and calibrating the system is created. In an attempt to keep the consumed power low, the biasing current was chosen to be 25 µA and is a figure that has yielded satisfactory lower power design results for the given 1.2 µm technology. The circuit was designed for generating a current of 12.5 µA, which will then be scaled up by a factor of two. This was done so as to minimize the wasted power consumed by the primary mirror circuit. Transistors M12, M13, M14 and M15 will thus generate the necessary gate voltages needed to bias all transistors in the other devices and will take on a similar cascode configuration.

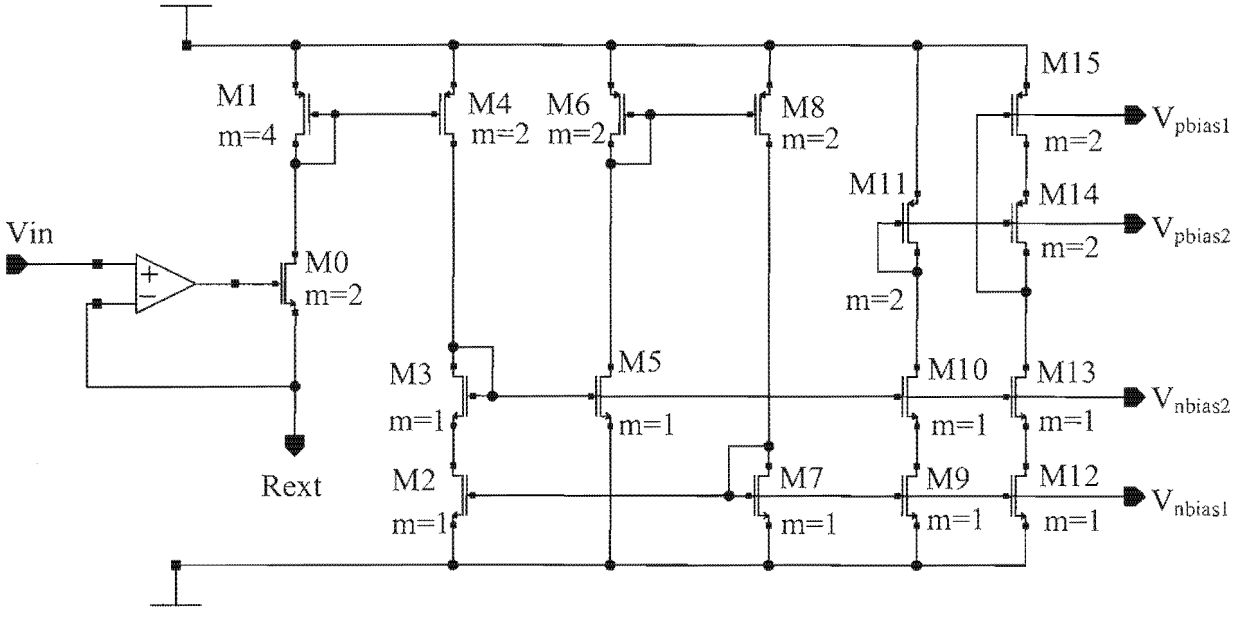

Figure 4.3 Current reference generator

The circuit has 2 inputs and 4 outputs. The first input V_{in}, will use the bandgap voltage as input. The operational amplifier in figure 4.3 will be used to create a virtual short circuit for the external resistor connected to the second input, R_{ext}. This resistor must be selected such that a current of 25 µA flows through it. Following simple Ohm's law calculations with a bandgap voltage of 1.16 V, its value will be approximately 46.4 kΩ. Taking operational amplifier input offsets into account, this resistor value can be calibrated for a 25 µA current flow.

4.3. VOLTAGE TO CURRENT CONVERTER

Voltage to current conversion is necessary so as to bias the Hall generators with a current directly proportional to the line voltage with high accuracy but more important stability. An instrumentation amplifier configuration will be used with strong output transistors. This is to ensure enough current driving capability for biasing the Hall generator. Figure 4.4 shows the configuration along with its equivalent symbol. An increase in potential at the non-inverting input results in a larger negative signal current i_s, at the $-i_{out}$ node. This is due to a larger differential voltage across R_1 and consequently the current through it. As the output current is simply a mirrored sample of this current with a larger ratio, the differential signal current follows the current through R_1.

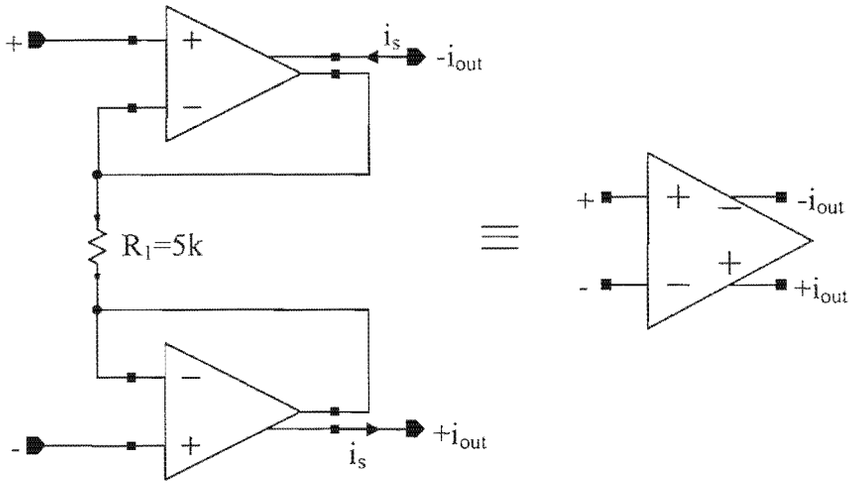

Figure 4.4 Voltage to current converter used for biasing the Hall generators

The external voltage divider network must be designed such that the saturation limit of the operational amplifier is not exceeded. The architecture is used such as to minimize offsets as well as lowering the sensitivity resulting from the changing Hall generator resistance due to process variations. R_1 will be implemented using a poly-silicon resistor to reduce temperature

dependencies in comparison to n-well resistors. The operational amplifiers will be biased using the temperature compensated current bias circuit. Simulation verification is the same as for the output instrumentation amplifier. The circuit functionality will be given in more detail in chapter 5.

4.4. AMPLIFIER

The main criteria for the operational amplifier are stability and linearity. As the system will work with low frequency (≤ 325 Hz), it will not be necessary for a high slew rate specification. The design principles used will now be discussed. The detailed design is given in addendum B.

4.4.1. Operational Amplifier Architecture

Operational amplifiers are built up from operational transconductance amplifiers (OTAs) [28, 29]. An OTA can be seen as a voltage controlled current source with a transfer function of $i_{out} = g_m v_{in}$, with a differential input voltage. Figure 4.5 shows the symbol as well as the two possible configurations for an OTA. Operational amplifiers can thus be realized using these building blocks.

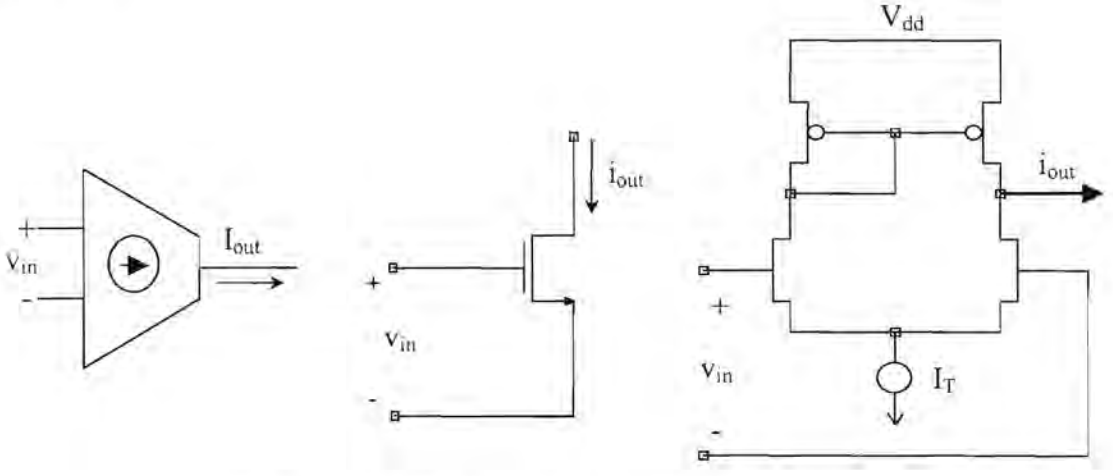

Figure 4.5 Different configurations for OTAs

The architecture for such a two-stage operational amplifier is shown in figure 4.6. The reason for multi-stage operational amplifiers is due to the fact that a single stage cannot yield useful gain by itself as required for the open-loop gain of an operational amplifier. Thus more than one stage is used. Due to high frequency poles being introduced, anything more than two stages will yield closed-loop instability. The configuration used in figure 4.6 is thus a standard

architecture. The first stage is a differential input, single ended output stage with a transconductance of g_{m1}. Its duty is to provide a differential input relatively immune to common mode inputs, high input resistance and provide some voltage gain as a single-ended output. It drives a single-ended input/output stage. This second stage is usually that of a common source stage that provides a large voltage gain. The final stage is simply a voltage follower that is capable of driving resistive and capacitive loads. This is to prevent the output stage from loading the gain stage.

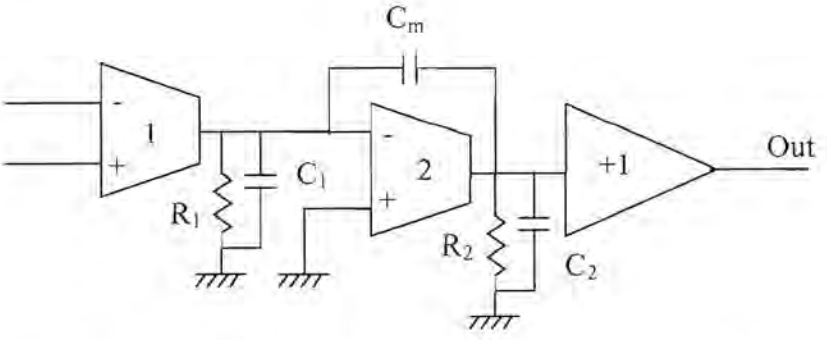

Figure 4.6 Single ended output, two-stage operational amplifier

A suitable MOSFET circuit diagram is shown in figure 4.7. R_1, C_1, R_2, C_2 represent the resistances and capacitances of the connected node at the output of each OTA.

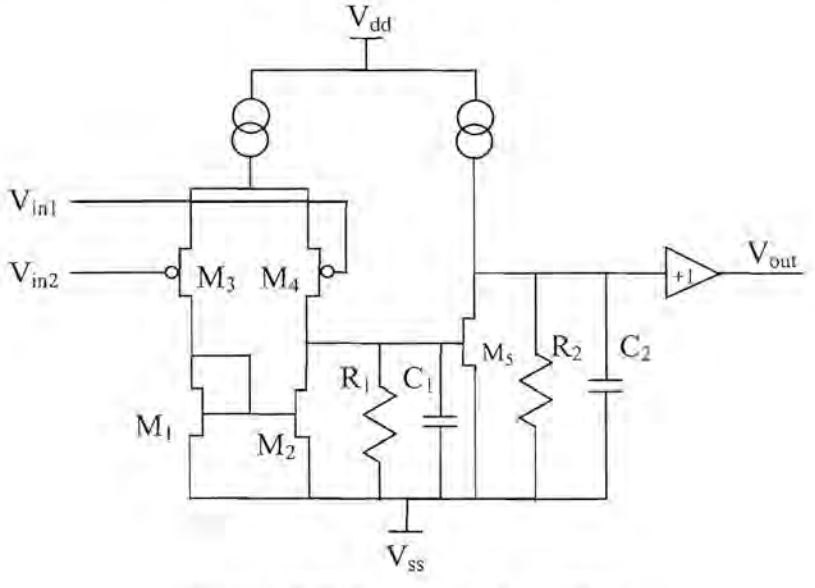

Figure 4.7 MOS operational amplifier

At low frequency, the capacitive loading of each input stage is not of significance. The resistors R_1 and R_2 are the output resistors of each stage respectively where;

$$R_1 = r_{op1} \,||\, r_{on1} \tag{4.16}$$

and

$$R_2 = r_{op2} \,||\, r_{on2} \tag{4.17}$$

Here, r_{on} an r_{op} is the small signal resistances of the two output transistor of each OTA stage.

The low frequency gain of the circuit is thus:

$$A_V = (g_{m1}R_1)(g_{m2}R_2)(1) \tag{4.18}$$

M_1 to M_4 is the first stage, M_5 the second followed by the buffer. If v_{in2} is increased in potential, the PMOS has a smaller gate source driving voltage and this results in the transistor to conduct less. As the current in M_1 is equal to that of M_3, the voltage at the drain of M_1 decreases. This results in a decrease in current through M_2 (mirror). This decrease in current raises the potential at the drain of M_2. The voltage then increases the gate source voltage of M_5 causing it to conduct more strongly. The drain voltage of M_5 thus decreases and is buffered by the unity gain stage. The net output voltage thus decreases as a result of the increased potential at v_{in2}. This input is thus referred to as the inverting input. A similar analysis on v_{in1} will show an increase in the output voltage for an increase in the input voltage and is similarly referred to as the non-inverting input.

4.4.2. Frequency Response

Figure 4.8 shows the open-loop transfer function of an operational amplifier. It can be seen at low frequencies, that the operational amplifier yields a high gain given by equation (4.18). As the frequency increases however, the poles introduced by the load capacitors between each stage become more significant. Good design practices yield two dominant poles through the capacitive loading between each stage. Important information can be retrieved from the open loop transfer function.

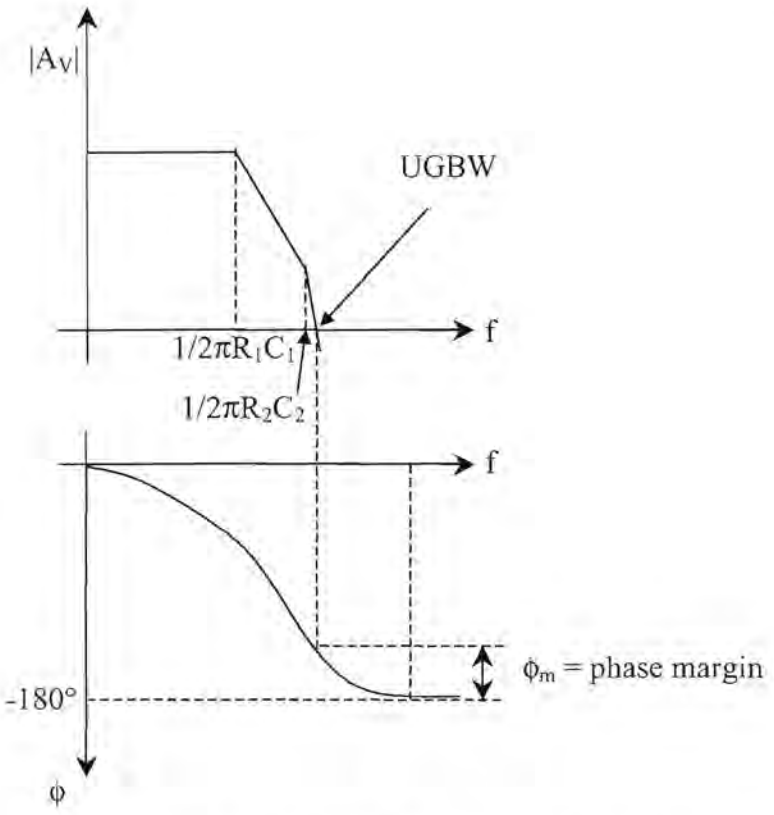

Figure 4.8 Bode diagrams of the open-loop transfer function

The first is the two poles and their relative frequencies at which they occur and are given by equation (4.19).

$$A_V = (g_{m1}Z_1)(g_{m2}Z_2) = \frac{g_{m1}R_1 g_{m2}R_2}{(1 + sC_1R_1)(1 + sC_1R_2)} \quad (4.19)$$

The 0 dB cross point is called the unity gain bandwidth. Equation (4.20) gives the gain bandwidth product.

$$G_{BW} = A_V . f \quad (4.20)$$

Typical operational amplifier circuits contain many poles. In folded-cascode topologies, for example, both the folding node and the output node contribute poles. Thus, operational amplifiers must usually be "compensated" so that their open-loop transfer function is

modified such that the closed-loop circuit is stable and the time-response of the system is well behaved.

The need to compensate a circuit is due to the fact that the gain crossover point is not well before the phase crossover point. It is thus possible to achieve stability by either minimizing the overall phase shift thus moving the phase crossover *out* or dropping the gain thus pushing the gain crossover *in*. The first approach is an attempt to minimize the number of poles in the signal path by proper design. Since each additional stage in an operational amplifier adds at least one pole, the number of stages must be minimized and thus results in low voltage gain and/or limited output swings. The second approach maintains low frequency gain and output swing but reduces bandwidth due to the gain falling to lower frequencies.

Considering figure 4.6 as an example, though there are high frequency poles due to the transistors (small signal impedances), the output resistance of the amplifier is much higher than the small signal resistance seen at the other nodes in the circuit. It is obvious thus that even with a moderate capacitive load on the first stage, the first pole $\omega_{p,1}$ is closest to the origin and also usually sets the 3-dB bandwidth thus making it the dominant pole. The second most dominant pole is due to C_2 and is usually closer to the unity gain bandwidth point and if not so, the aim is to get it there. If C_1 were to increase, i.e. by adding a parallel capacitor to the input of the second stage, it is evident that it is possible to move the most dominant pole closer to the origin. This results in better stability but at the price of a loss in gain at upper frequencies as well as reduction in bandwidth. A more ideal approach is to split the poles from each other such that stability is obtained while keeping bandwidth. This is done using the Miller capacitor effect technique. By adding a capacitor across the input and output of the second stage, two dominant poles are produced, the first close to the origin, the second close to the unity gain crossover point. The resultant bode plots are shown in figure 4.10.

A problem however is that a zero is also introduced but its effects will be discussed later. Using Kirchoff's current laws as well as the assumption that the two dominant poles are widely spread from each other (which is exactly what we want to achieve), from figure 4.9 it can be shown that the two poles are described by the following equations:

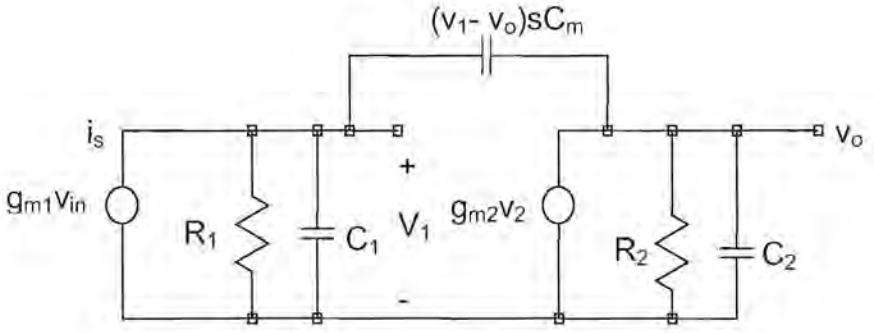

Figure 4.9 Small signal equivalent of the second OTA stage

$$i_s = \frac{v_1}{R_1} + v_1 sC_1 + (v_1 - v_o)sC_m \qquad (4.21)$$

$$(v_o - v_1)sC_m = g_{m2}v_1 + v_o sC_2 + \frac{v_o}{R_2} \qquad (4.22)$$

Eliminating v_1 yields

$$\frac{v_o}{i_s} = \frac{g_{m2}R_1R_2(1 - \frac{sC_m}{g_{m2}})}{\{1 + s[(C_m + C_2)R_2 + (C_1 + C_m)R_1 + g_{m2}R_2R_1C_m] + s_2R_2R_1(C_1C_2 + C_mC_2 + C_mC_1)\}} \qquad (4.23)$$

The previous equation consists of a numerator (zero) and denominator (poles). Rewriting the denominator yields

$$D(s) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s_2}{p_1p_2} \qquad (4.24)$$

thus

$$D(s) \approx 1 - \frac{s}{p_1} + \frac{s_2}{p_1p_2} \qquad (4.25)$$

The Effects of the Poles

As the poles are widely spread, p_1 reduces to equation (4.26).

$$p_1 = \frac{1}{(C_m + C_2)R_2 + (C_1 + C_m)R_1 + g_{m2}R_2R_1C_m} \quad (4.26)$$

The DC gain of the second stage is high and thus

$$p_1 = \frac{1}{g_{m2}R_2R_1C_m} \quad (4.27)$$

and

$$p_2 = \frac{g_{m2}C_m}{C_1C_2 + C_m(C_1 + C_2)} \quad (4.28)$$

This is true if the dominant poles are widely separated and thus C_1 and C_2 can be ignored. At high frequencies, C_m dominates the frequency response as it short circuits the second OTA and as a result,

$$v_o = -\frac{g_{m1}v_{in}}{sC_m} \quad (4.29)$$

and the high frequency response (from the first pole) is given by equation (4.30) and the low frequency gain response by equation (4.31).

$$|A_V| = \left| \frac{v_{out}}{v_{in}} \right| = g_{m1}\omega C_m \quad (4.30)$$

$$|A_v| = (g_{m1}R_1)(g_{m2}R_2) \quad (4.31)$$

These results are indicated in figure 4.10. The first pole occurs when

$$g_{m1}R_1g_{m2}R_2 = \frac{g_{m1}}{2\pi fC_m} \quad (4.32)$$

where,

$$f_{p1} = \frac{1}{R_1 g_{m2} R_2 2\pi C_m} \quad (4.33)$$

and the unity gain bandwidth (UGBW) is at a frequency of

$$1 = \frac{g_{m1}}{2\pi f C_m} \quad (4.34)$$

where,

$$UGBW = \frac{g_{m1}}{2\pi C_m} \quad (4.35)$$

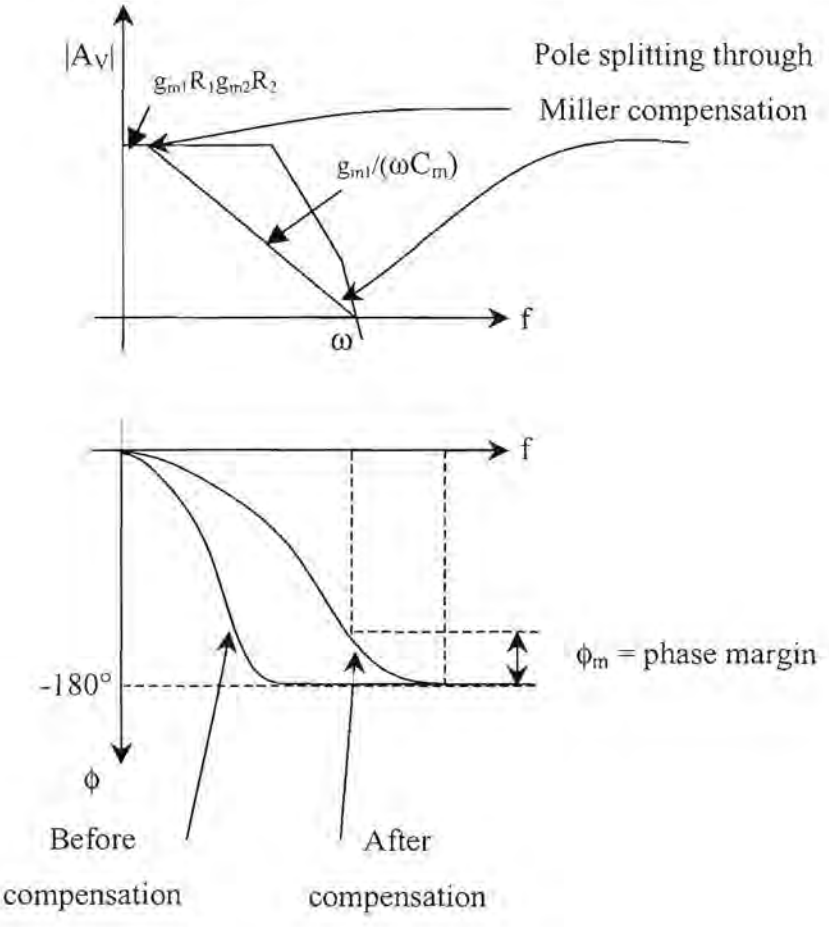

Figure 4.10 Frequency compensation

It can thus be seen by increasing C_m causes a greater splitting between the two dominant poles, which thus also satisfies the original assumption. The reason for the poles splitting is seen for both cases as the following. Firstly, the Miller effect causes a multiplication of the Miller capacitor to virtually appear in parallel with C_1, which was seen before to shift the first pole closer to the origin. The cause for the shift in the second pole is due to the fact that at high frequencies, C_m tends to short out the second stage causing the resistance when looking back into the g_{m2} stage from C_2 to decrease and thus has the effect of reducing R_2 and ultimately to shift the second pole to a higher frequency.

Effect of the Right Half Plane Zero

As the gain of bipolar stages is high, the zero usually has no effect on bipolar operational amplifiers as its effects occur long after the unity gain point. This problem resides mainly in CMOS devices due to the low gain of individual stages as the zero causes 20 dB/dec increase in gain at the zero point frequency. The problem is larger than this as a further 90° phase shift is also associated with this zero. As a result, the gain crossover point is much earlier than the phase crossover point and causes instability. The right half plane zero thus acts as a left half plane pole regarding the phase response and as a left half plane zero regarding the open loop frequency response. This is illustrated in figure 4.11.

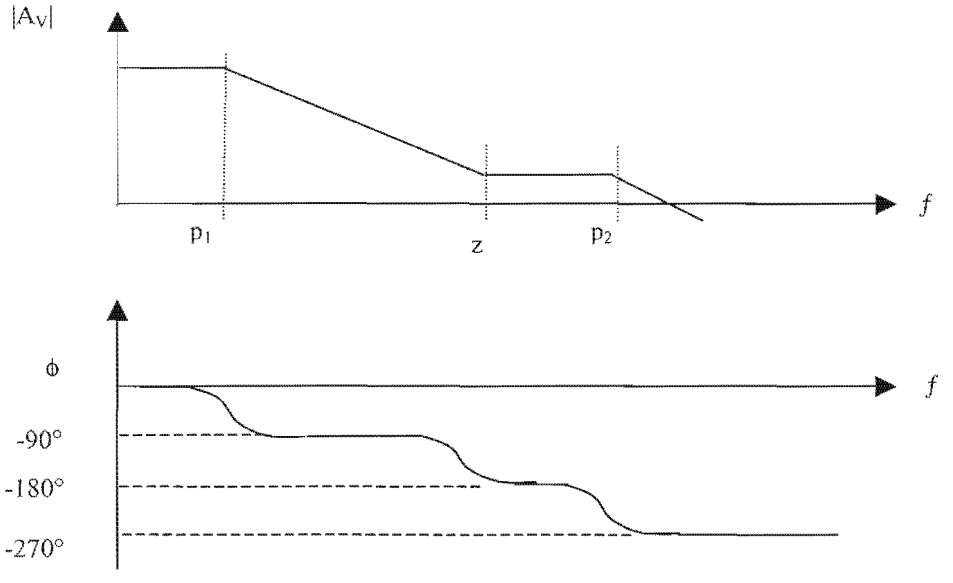

Figure 4.11 Effect of the right half plane zero

The problem can easily be solved by adding a series resistor to C_m with a value of $R_z = 1/g_{m2}$ which results in moving the zero to $+\infty$.

$$z = \frac{1}{C_m\left(\frac{1}{g_{m2}} - R_z\right)} \qquad (4.36)$$

Due to mismatching, it will not always be possible to achieve an exact resistor value and thus choosing $R_2 > 1/g_{m2}$, will result in moving the zero from the right half plane to the left half plane close to the second dominant pole, where stability can once again be achieved. Here, the zero contributes a positive 90° phase shift and is shown in figure 4.12.

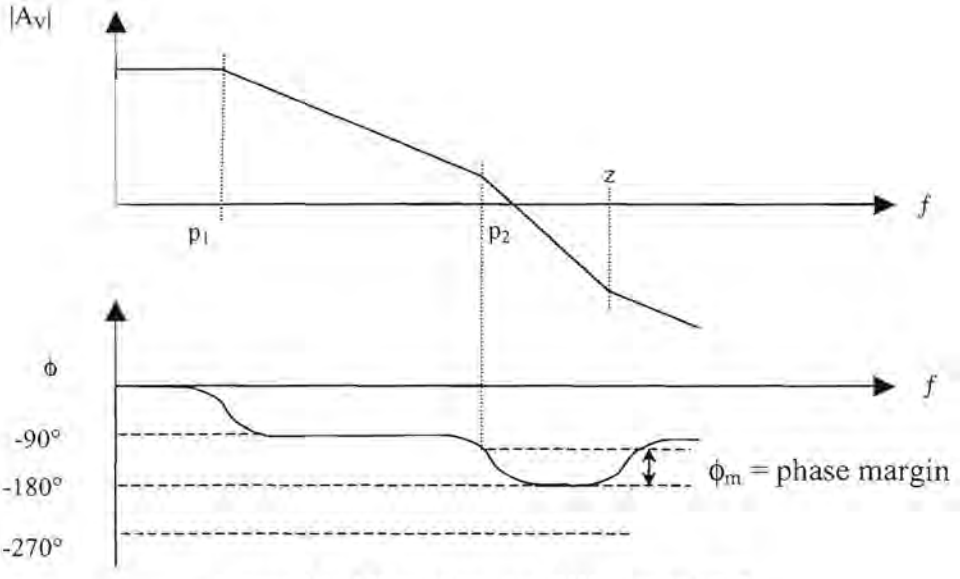

Figure 4.12 Effect of moving RHP zero to LHP

4.4.3. Design of the Operational Amplifier

The following specifications are proposed and are fairly general-purpose specifications for an operational amplifier that will still yield conformance of global specifications.

- $V_{DD} = 5$ V
- $A_{V(opoen\text{-}loop)} > 80$ dB
- UGBW prod > 1 MHz (stable)
- Slew-rate = 2V/µs
- Phase margin > 45°

Figure 4.13 shows the proposed circuit of the operational amplifier inclusive of compensation. This amplifier will be implemented in the current reference circuit shown in figure 4.3. This amplifier needs to be self biased for implementation in the current bias circuit. The amplifier will be used to drive only a very small capacitive load.

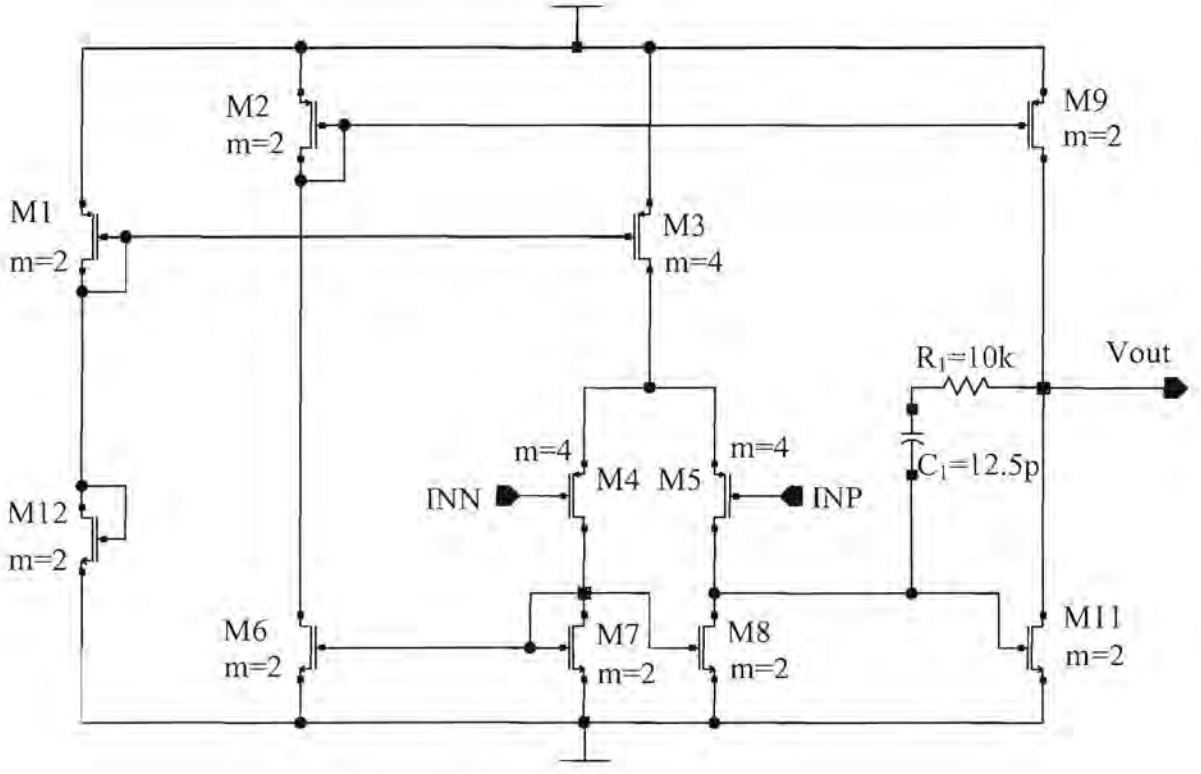

Figure 4.13 CMOS operational amplifier

A slight modification will be done to this operational amplifier so as to convert the output into a current, which will be used to implement the instrumentation amplifiers of both the voltage-to-current converter and output stage amplifier. The principle is once again based on current mirrors and the output branch will simply drive an output current with the same ratio as that of the output stage. This is achieved by the modification in the circuit comprising of transistors M4, M5, M6, M16, M17, M18 and M19. This is to ensure that the gain stage is not loaded by external components thus decreasing the output impedance. The circuit is shown in figure 4.14. The two inputs V_{nbia1} and V_{nbia2} will be driven from the two outputs, V_{nbia1} and V_{nbia2} of the bias circuit in figure 4.3. These transistors will then establish the 25 µA bias current which will be consequently mirrored into the circuit through M1.

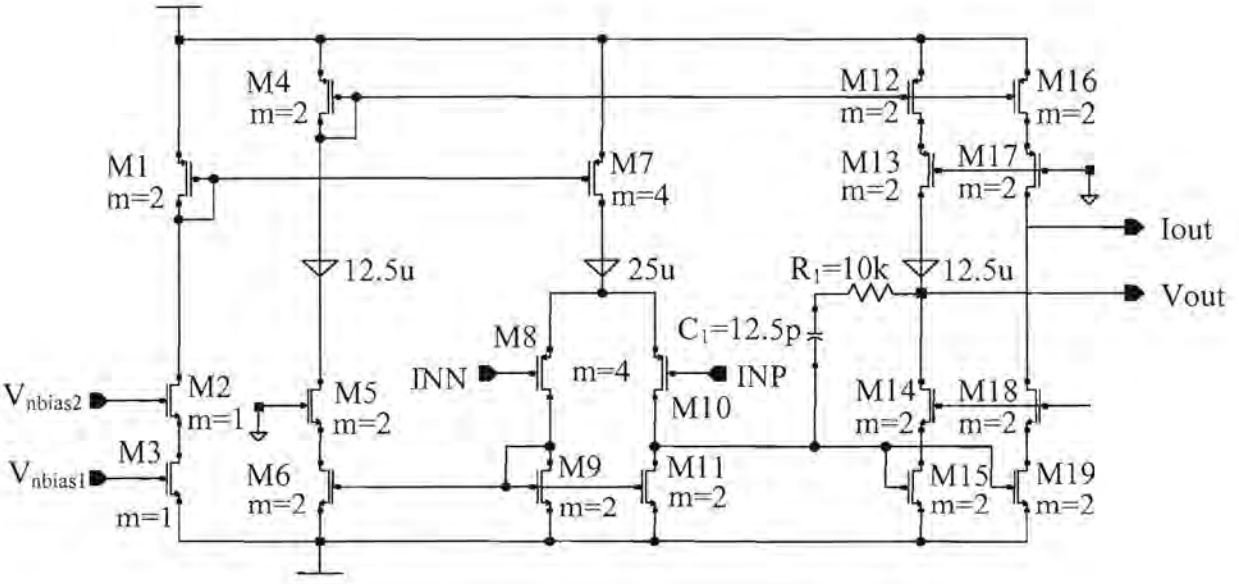

Figure 4.14 Operational amplifier based current converter

The circuits were designed based on the required operational amplifier specifications and the following data was calculated for implementation on the proposed technology. A detailed mathematical analysis can be seen in addendum B.

- $A_{V(open\text{-}loop)} = 95$ dB
- Input transistor ratio of $W_5/L_5 = 38$ and of type PMOS
- A compensation capacitor of 12.5 pF
- First Pole at 273 Hz
- Second Pole at 180 Mhz
- A LHP zero at 10 MHz
- A phase margin of 90°

4.4.4. Output Instrumentation Amplifier

These specifications will satisfy the requirements needed by the system to function correctly. The instrumentation amplifier configuration is shown in figure 4.15. Based on previous experimentation results, the Hall generator is expected to deliver an output signal of between 0 and 6 mV and will be represented by an output current signal of 0 to 6 µA suggesting a gain of 1 mA/V. R_1 will thus be 1 kΩ for a current ratio of 1:1 consisting of five 5 kΩ n-well resistors in parallel to satisfy the technological design rules for the CMOS process. Typically

the input offset of an operational amplifier is not good enough for the required application and consists of two components. The first is a systematic offset, which is in the order of 5 to 30 mV, with the second type being the statistical offset, which could contribute up to 10 mV. The configuration used in figure 4.15 overcomes the systematic offset problem through differential implementation. The statistical offset however will still remain. The minimization of the systematic offset is achieved through the design of well-matched operational amplifiers.

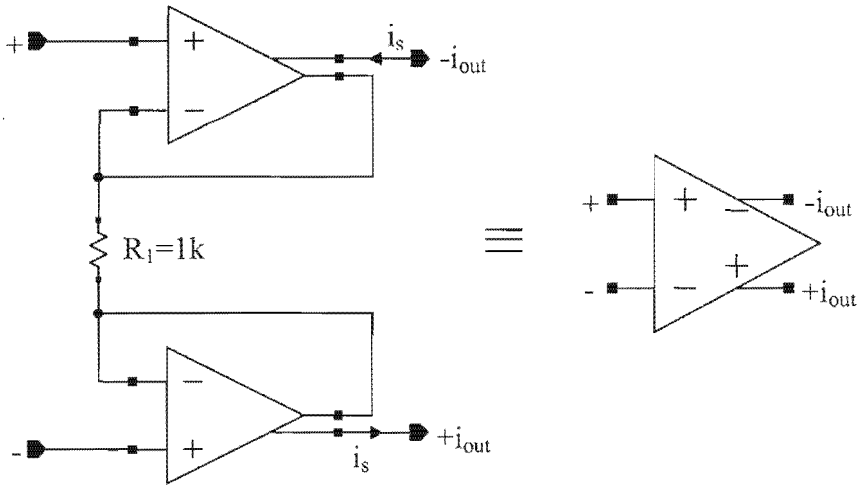

Figure 4.15 Output instrumentation amplifier

As mentioned earlier, the resistor used for this configuration will be a pinched, n-well type, as this makes it possible to compensate for temperature as well as process variances within the Hall generator. A semiconductor resistor is manufactured using regions with specific doping concentrations such that the resistance behaves in a way that is acceptable for the application. The amount of resistance required in an n-well resistor is based on equation (4.37). From chapter 3 it was seen that the Hall voltage in terms of current as well as voltage sensitivities were proportional to the same factors and thus any variation in temperature or process parameters are compensated for by the same amount when the absolute value of this resistance is used.

$$R = \frac{1}{q\mu_n nt}\frac{W}{L} \qquad (4.37)$$

4.5. OFFSET CANCELLATION AND FILTERING

The Hall generator, as with all semiconductor devices, is not a perfect device. The element, from an electrical point of view, will show unavoidable imbalances due to resistive gradients, geometrical asymmetries [4, 6, 7] and piezoresistive effects [4, 6, 7]. Furthermore, the offset is a function of the biasing current making it difficult to isolate the offset from the useful signal. These imbalances can generate a non-negligible offset voltage (V_{op} in figure 4.16) of between 0.5 mV - 5 mV for a 5 V supply. For this reason, static offset cancellation techniques such as electrically erasable programmable read only memory (EEPROM) cannot be used due to the fact that this offset itself dynamically changes with respect to time. This is due to the fact that the bias current will be a sinusoidal signal proportional to the line voltage. Furthermore, switching offset cancellation techniques as used in amplifiers cannot be used, as there is no available state where V_{offset} can be isolated from V_h except through the removal of the magnetic field making it a nonviable option.

By making use of the fact that the Hall generator behaves similar to a distributed resistive Wheatstone bridge from a dc point of view, it is possible to geometrically arrange the Hall generators and electrically connect them such that the imbalance source that remains invariant and fixed in solid space be equal but of opposite polarity and thus achieving the desired cancellation effect. This reduces signal-conditioning circuitry but establishes the need for multiple elements, which could use up large resources in terms of die area. Alternatively, it could be possible to use only one plate to generate the quadrature states by periodic supply and output contact permutations [4, 8, 11]. This method does however require the use of more complicated signal processing circuitry but takes advantage of reducing the residual offset and its production spread as compared with multi-element sensors. This is a significant advantage as zero-level deviations are degraded due to element mismatches between physically different elements and are mostly generated by package and temperature-dependant built in stresses.

4.5.1. The Switched Hall Plate

The simplest form of dynamic offset cancellation in Hall plates uses a Hall generator with four contacts where the quadrature states are generated by periodically connecting the biasing current to one pair of contacts or to the other as shown in figure 4.16. The technique can take on one of a few forms. It has already been mentioned that a 90°-direction change in current through the plate will result in an equal but opposite offset voltage [4]. In this way, it is

possible to superimpose the offset voltage of the element onto the useful Hall voltage signal at a higher frequency thus resulting in the offset being distinguishable from the information-carrying signal in the frequency domain and is illustrated in figure 4.17. The output signal can thus be low-pass filtered to extract the Hall voltage and any variations in the offset voltage with respect to different parameters such as bias current, temperature or varying stresses will be distinguishable. Other techniques include switching in all four directions along with polarity reversal of amplifier inputs thus creating a technique that functions in conjunction with chopper stabilized offset cancellation techniques as implemented in low input offset amplifiers [23, 24, 25, 30, 31]. This method is very effective but at the cost of increased circuit complexity for marginally better performance. The last method will be to switch the element such that the offset voltage remains quasi-constant with an alternating Hall voltage and can be a useful method with systems requiring the output in this form.

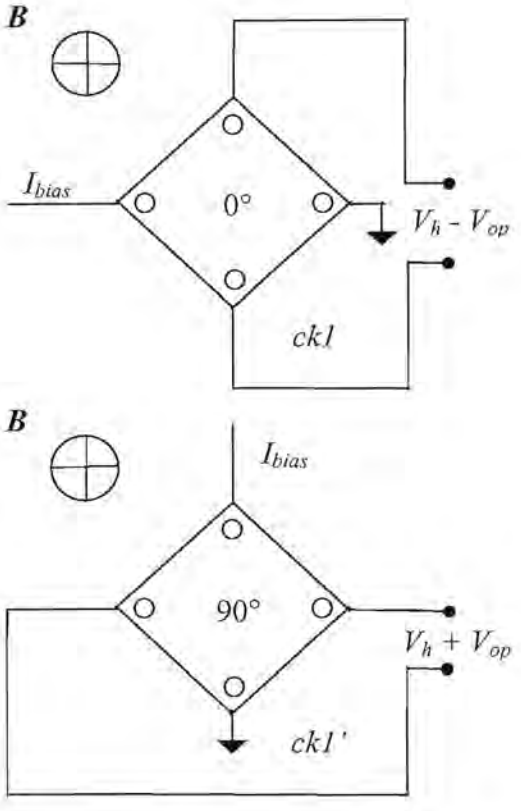

Figure 4.16 Periodic 90° bias current direction switching

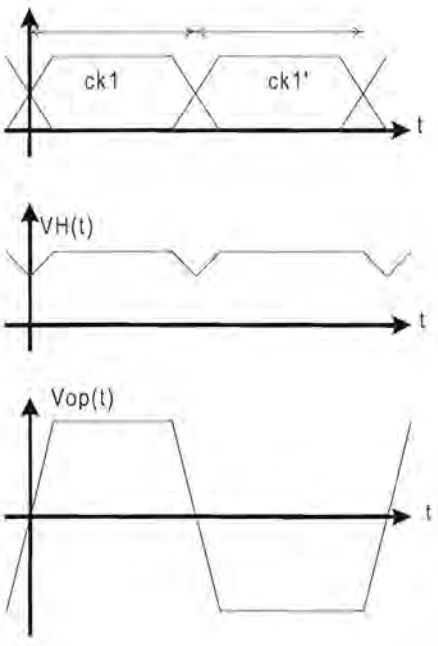

Figure 4.17 Clock, Hall voltage and plate offset waveforms

Figure 4.18 shows the circuit diagram of the implementation of the switching circuitry. The switches comprise of complimentary transmission gates of minimum size of which the W/L ratio for the NMOS, and PMOS transistors are equal. This is to ensure that equal amounts of opposite charge packets are injected resulting from clock feed through cancel each other [28]. This method thus reduces charge injection. Equation (4.38) shows the speed limitation of these switches and will be dominated by the PMOS transistor, as its mobility is less than that of the NMOS. Typically this speed is in the order of MHz and will not affect this application with the harmonic content of a few hundred Hz.

$$f = \frac{\mu_p}{L^2} \qquad (4.38)$$

The switching circuit has clock inputs, T<0:1> and TN<0:1>. Two 50 % duty cycle clocks, 180° out of phase with one another, drive these inputs. PCH and NCH are the input and output nodes for the bias current respectively and INP and INM are the positive and negative sensing nodes for sensing of the Hall voltage. Let the two clock phases be represented by the states CLK_1 and CLK_2, and let CLK_1 represent the condition where T<0> = '0', T<1> = '1', TN<0> = '1' and TN<1> = '0', then CLK_2 suggests that T<0> = '1', T<1> = '0', TN<0> = '0' and TN<1> = '1'. From this analysis, it can be seen that during CK_1, the bias current flows through the Hall generator from terminal A, to terminal D, and that the Hall sensing nodes are

connected via terminals B and C. Similarly, during CK_2, current flows from terminal B to terminal C, and sensing nodes are between terminals A and D. This then physically realizes the explanation given in figure 4.16.

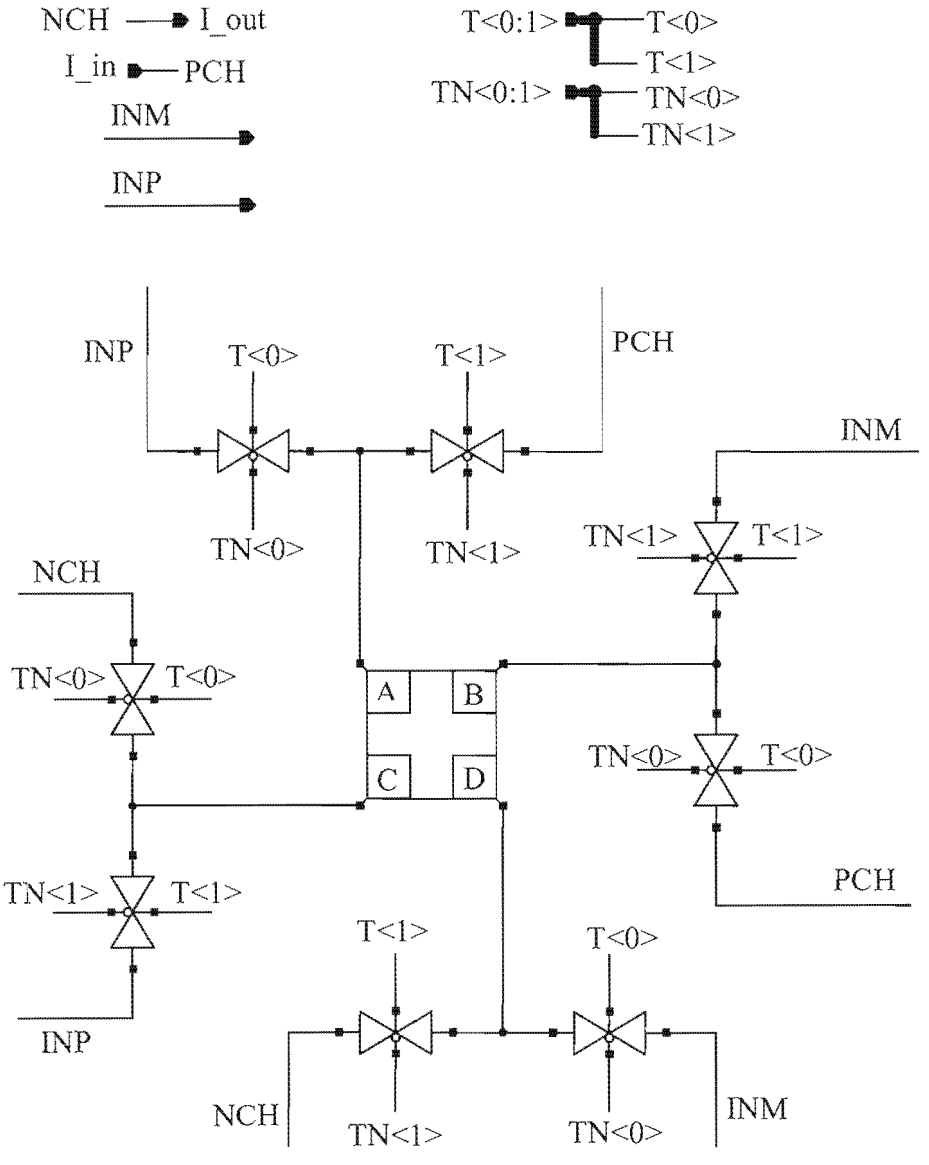

Figure 4.18 Circuit diagram showing switching arrangement using transmission gates

4.5.2. Filtering

It is proposed to use passive low-pass filtering at the output of the Hall generator. Maximum switching frequency of the quadrature states for highest efficiency must be determined through experimentation and it was found in literature [4] that common upper limits for switching frequencies are in the order of 100 KHz and is governed by the minimum time required by the Hall generator to redistribute the charges through the plate such that the

output signal is settled for validity. A frequency of 10 KHz will thus be assumed for the switching speed and a –3 dB cutoff frequency of 500 Hz will be used for the design of the filter elements. This will ensure that the 45 – 325 Hz measured signal remains undisturbed and that the superimposed offset voltage signal along with higher frequency switching noise is removed. The low-pass filter is shown in figure 4.19. The elements are designed according to equation (4.39).

$$f_c = \frac{1}{2\pi RC} \qquad (4.39)$$

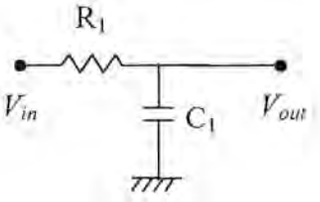

Figure 4.19 Passive low-pass filter

It was decided to use an external passive filter, as the optimum switching characteristics for the Hall generator must still be determined through experimentation. This filter would in future be replaced by an on-chip active system [30, 32], as the passive elements required for such low cut-off frequencies require an impractically large die area. The resistance and capacitance was calculated as 1 MΩ and 320 pF respectively.

4.6. SIMULATION

The following paragraph describes all the simulation results obtained for the individual components. These simulation results support the theoretical calculations for each component.

4.6.1. The Bandgap Reference

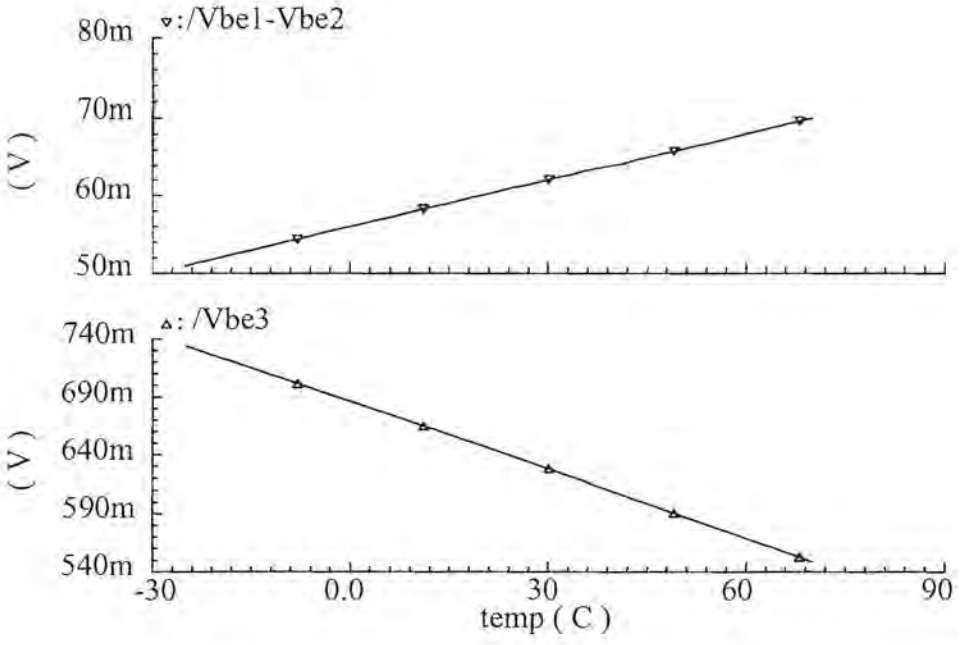

Figure 4.20 Simulation results showing temperature coefficients

Figure 4.20 shows the validity of equation (4.8) and equation (4.10). The following temperature coefficients were obtained:

$$\frac{\Delta(V_{be1}-V_{be2})}{\Delta T}=0.08685mV/°K \qquad (4.40)$$

$$\frac{\Delta V_{be3}}{\Delta T}=1.89mV/°K \qquad (4.41)$$

Figure 4.21 shows the bandgap reference output voltage V_{bg} with $\Delta V_{bg}/\Delta T$ = 2.2 mV/95 K. This results in a variation in the output of 0.16 % over the required temperature range or 0.0017 %/K and conforms well to the required specification of 0.05 %/K as required by the IEC standard. Two factors worth noting here is the output voltage is higher than designed for and secondly the zero TC is not at 27 °C and could be the result of the simulation models not

being accurately defined for temperature simulations, as there are many higher order effects that are not accounted for in the models that were used.

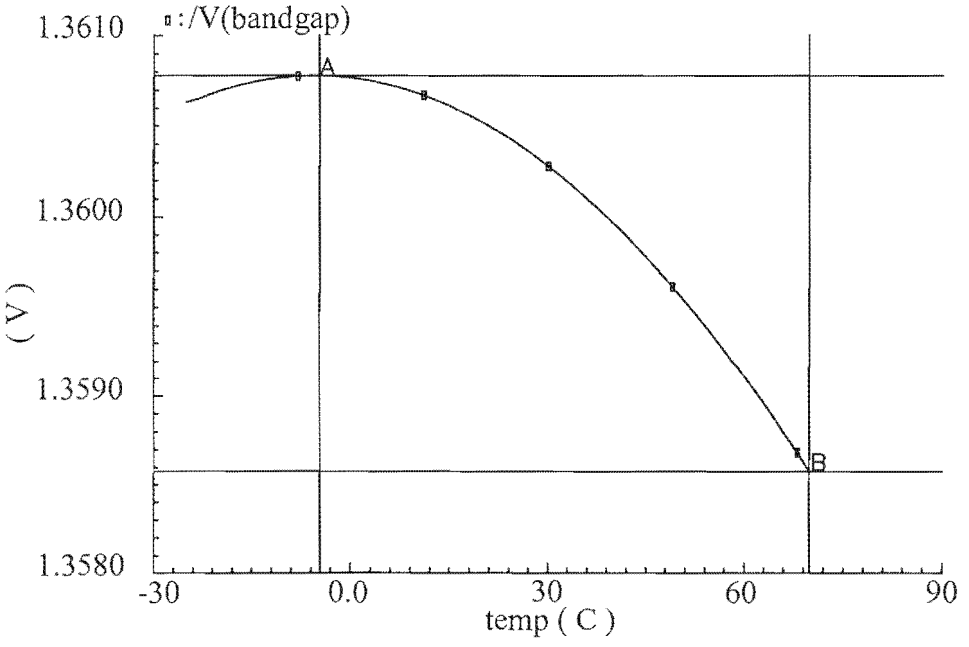

Figure 4.21 Bandgap reference output voltage

4.6.2. Bias Current Reference

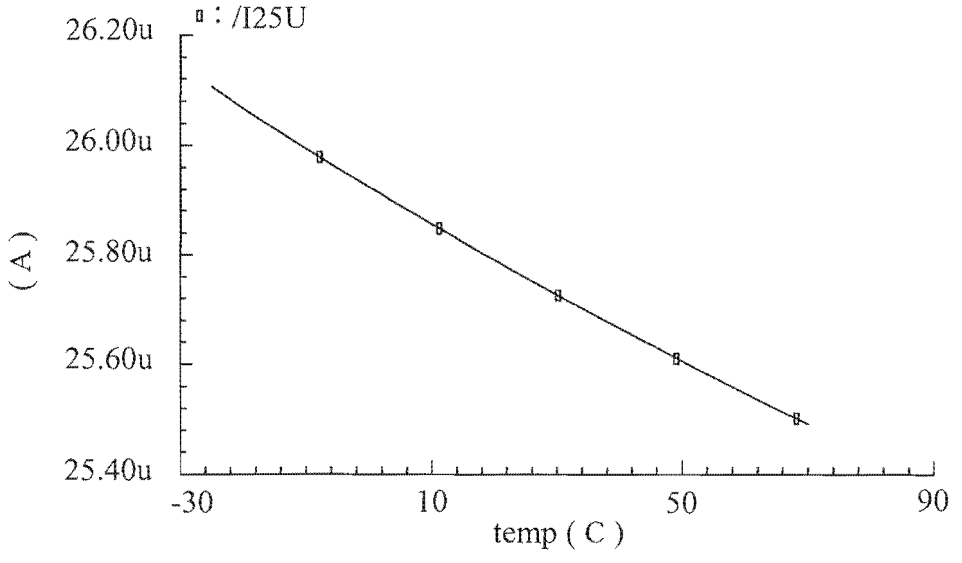

Figure 4.22 Simulation showing bias current dependence on temperature

Figure 4.22 shows the current reference circuit dependency on temperature showing that the total variation results to 2.3 % over the temperature range or 0.024 %/K. This is still within the specified 0.05 %/K as required by the IEC standard. The reason for the slightly higher temperature dependence in this circuit is the fact that the operational amplifier used must be self-biased as this circuit generates all the biasing voltages for subsequent circuitry. The use of an external calibrating resistor becomes useful here as inherent offsets in the operational amplifier can be compensated for, as well as any variations in the bandgap voltage. Furthermore, this resistor will set the overall gain of the system and this will be used for accurate calibration of the sensor. The circuit was simulated using the bandgap voltage of the circuit in figure 4.1 as a reference to the current referencing circuit. Thus, the temperature coefficient shown here contains the temperature dependence of both the bandgap and the current referencing circuit exclusive of the external resistor temperature coefficient. The reason for this is that the temperature coefficient for the external resistor is very small in comparison to the internal components. Also, should this become a problem, it will be possible to acquire more stable resistors to analyze its influence on the final sensor performance.

4.6.3. The Operational Amplifier

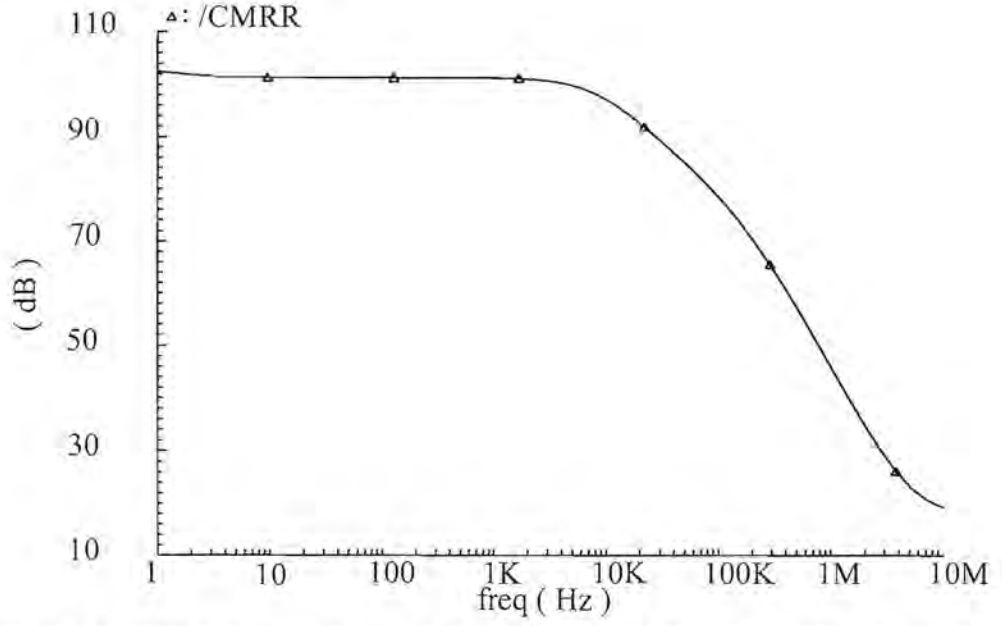

Figure 4.23 Simulated common mode rejection ratio (CMRR) of operational amplifier

Figure 4.23 shows the CMRR of the operational amplifier and it can be seen here that the value is fairly large and consistent at approximately 100 dB up to a frequency around 10 KHz.

The result compares well with a typical CMRR > 60 dB for general purpose unbuffered operational amplifiers. The CMRR is an important value and directly relates to the linearity of the operational amplifiers and thus the higher this value, the better the expected linearity. The most important influence regarding CMRR will be the 10 KHz clock used to switch the Hall generator. As this switching will be present as noise in the power supplies, it is necessary to take into account. Typically the dominant 10 KHz components will be fairly well suppressed by the amplifier. The CMRR will still remain within typical values up to 1 MHz, at which switching transients will become insignificant. Furthermore, the clock speed can be reduced to much slower speeds. The lower limit will be dominated by the Nyquist theorem that states that sampling rate must be at least twice the maximum measured signal frequency. This frequency component is that of the 5th harmonic in the line current and is around 400 Hz. The low pass filter will also limit the input frequency into the amplifier.

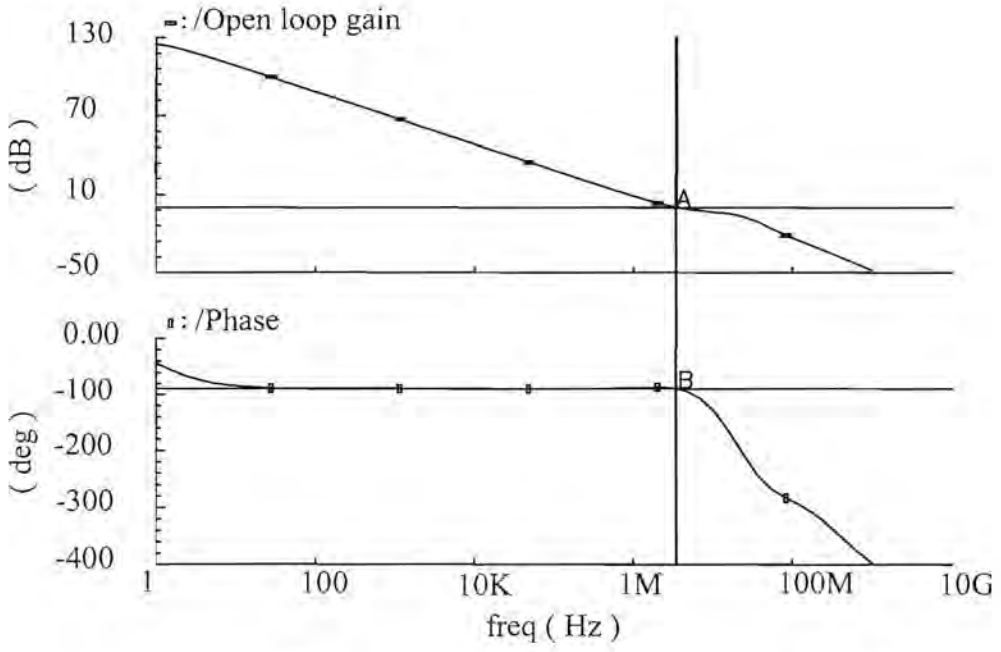

Figure 4.24 Frequency response of operational amplifier

Figure 4.24 shows a simulation of the open loop frequency response of the operational amplifier. The low frequency gain is seen to be around 125 dB and compares well with the aimed for 95 dB. It must be remembered that the mathematical models are only first-order calculations thus accounting for the difference. As a result of the higher gain, it can be seen that the "pole-splitting" effect has also caused the first most dominant pole to move below the designed for 273 Hz to around 5 Hz. The UGBW = 3.5 MHz and is stable with a phase margin of around 90°. A phase margin of around 45° is usually desired as this yields a time

step response that is critically damped and desired. The step response will thus result in a fairly over-damped response but as we are once again working with such low frequencies, this is not of major concern. The UGBW agrees with the aimed value of ≥ 1MHz. The zero was designed to be around 10 MHz as can be seen in the simulation result. In figure 4.25 it can be seen that the slew rate is almost 2.2 V/µs, which is slightly better than the aimed 2 V/µs.

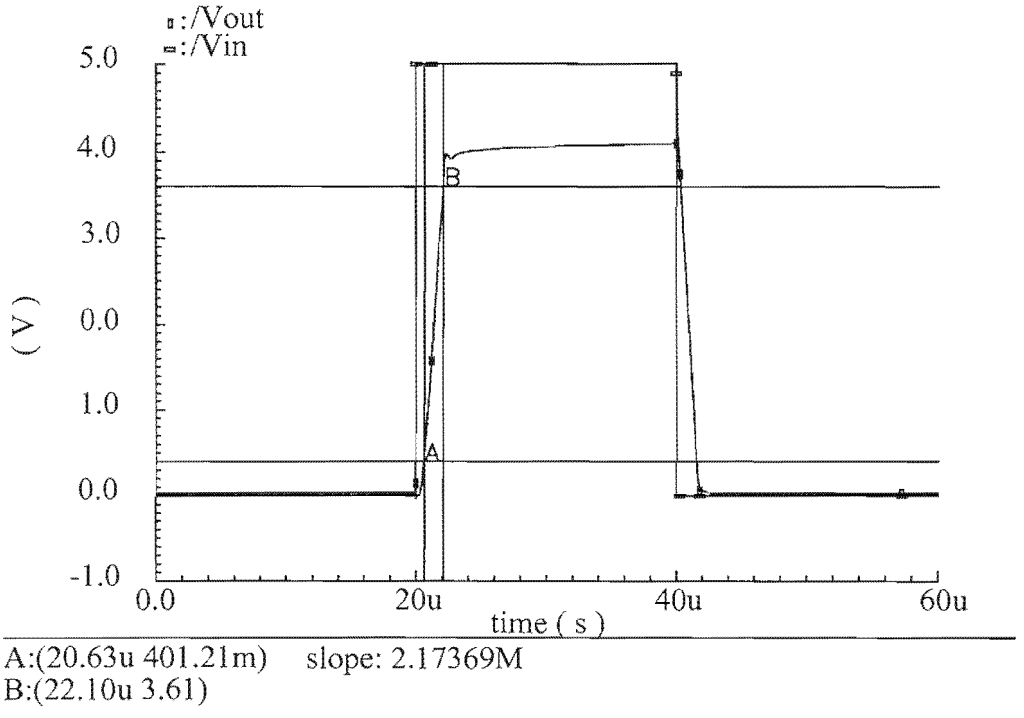

Figure 4.25 Step response characteristics of operational amplifier

The linearity results of the instrumentation amplifier in figure 4.26 show that amplification characteristics are very linear for larger differential inputs but that the linearity deteriorates around a zero differential input to about 1 %. The major disadvantage here is that the linearity around the lower limit will decrease for the sensor system but should still be within the required 1.5 %. The discontinuity appears to be a modeling characteristic around the origin. These results also describe the voltage to current converter but with a gain of 8 mA/V.

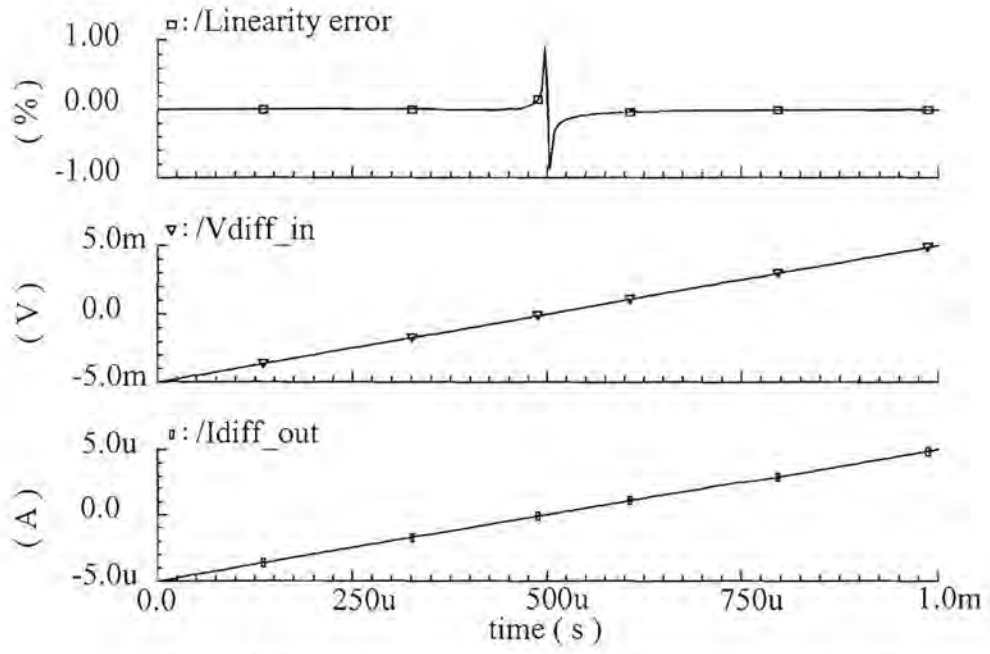

Figure 4.26 Linearity characteristics of instrumentation amplifier

4.7. EXPERIMENTAL VERIFICATION

The use of the CMOS manufacturing process allowed for only a limited area per run for test devices and thus not all devices could be manufactured and tested as separate entities. The following paragraph thus describes those devices that were produced and the results that were obtained and include a similar voltage to current converter and instrumentation amplifier circuit. Some devices similar in architecture were used to acquire data relevant to the system and the voltage to current converter is one such device.

4.7.1. Instrumentation Amplifier

The instrumentation amplifier was tested in terms of linearity and differential offsets between the amplifiers. It was found that the referred input differential offset between the amplifiers had an average value of < 1 mV and the contributing factors are mainly due to mismatches between separate operational amplifiers as well as differences in the biasing conditions of each amplifier.

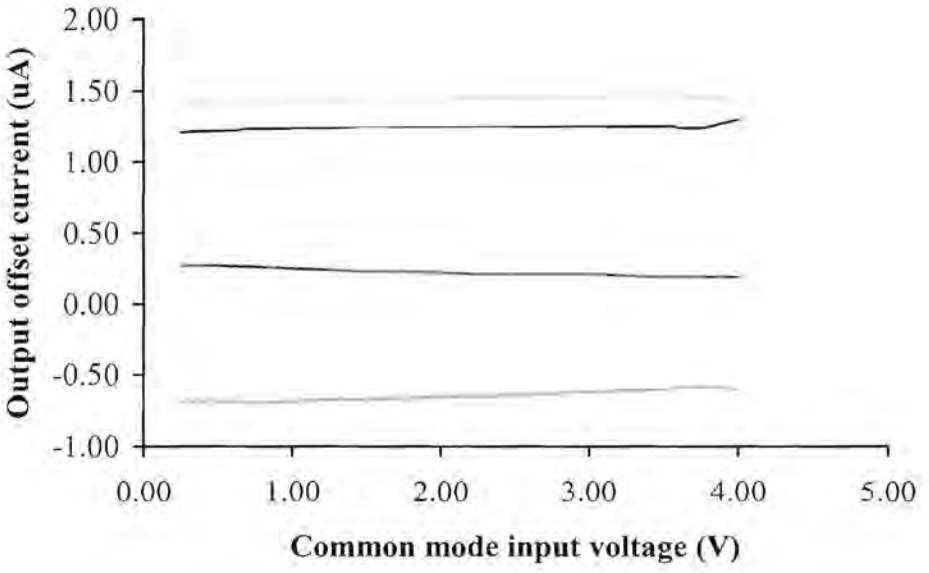

Figure 4.27 Graph showing output offset current versus common mode input voltage

Figure 4.27 shows a graph of the output-offset current present in four, randomly selected devices that were tested. The output current can be seen to be very stable over the entire common mode range up to 4 V, and ultimately displays the stability of the tail current in each operational amplifier. This is the most important factor to consider with this configuration, as it is the largest contributor of non-linear properties. The common mode operating conditions for this amplifier will be around 2.5 V with an expected common mode variation of ± 2.5 mV. Under these conditions, the amplifier tail current maintained very high accuracy and changes could not be measured with the available instrumentation with a resolution of ± 10 nA. As mentioned in the previous paragraph, the better the biasing currents are matched between separate amplifiers, the better the resulting linearity would be as the transconductance of the amplifying stages are directly dependent on the bias currents.

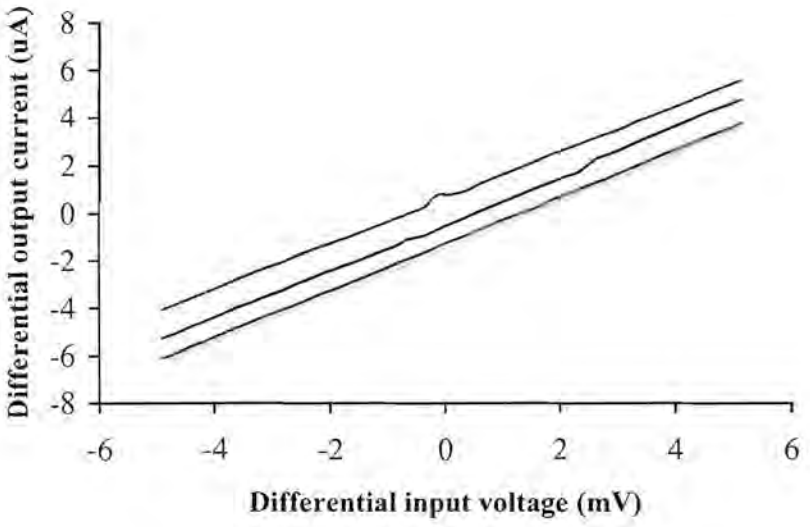

Figure 4.28 Graph showing output current versus differential input voltage

The curves in figure 4.28 illustrate the output differential current as a function of the input differential voltage. The test was done using a power supply with ±1 mV resolution. The non-inverting input was held at a constant 2.5 V while the inverting input was varied within a differential range of ±5 mV at its input. To increase the input resolution, an accurate resistive dividing network was used such that the input resolution was increased by a factor of 4. The worst linearity figures were calculated at 1.2 % with an average value at 0.7 %. Once again, linearity was mainly dependant on matching and differences in biasing conditions between the amplifiers. From this figure, the offsets are also visible where the curves cross the x-axis. It can be seen that these offsets are within ±1.5 mV. This was expected as these offsets represent typical statistical offset figures. Generally, all aspects of the instrumentation amplifier performance characteristics yielded good results in comparison to simulations.

4.8. CONCLUSION

This chapter focused on the design of the entire analog building blocks required by the power sensor, such that a fully functional device can be manufactured. The chapter started with an explanation of the sub-systems required by the sensor and the importance of well-defined temperature behavior in biasing circuits. The design of a bandgap reference that would be suitable to the application was given followed by the design of supplementary circuitry that would establish the biasing currents required by the amplifiers and other analog blocks. The

voltage to current converter necessary for the biasing of the Hall generator as a function of the mains voltage was then presented that based its foundation on the current referencing circuit. The following few paragraphs were dedicated to detailed operational amplifier design principles that were used to design a general-purpose amplifier that would later form the building block of the instrumentation amplifier. The working philosophy of the instrumentation amplifier was explained along with the basic principles of the compensation techniques that were exploited using this specific architecture.

All sub-systems were verified in simulation using simulation models based on a standard double metal, double poly, 1.2 μm CMOS process and the resultant characteristics were compared to theoretical calculations and basic principles. Some of these sub-systems were then manufactured using this standard CMOS process and verified in a laboratory under similar conditions as used in the simulations. The results were then compared to both simulation and theoretical models and discrepancies were clarified. Due to limitations in manufacturing resources, only a few devices were manufactured for testing purposes. Similar devices manufactured in this technology where available, were characterized to clarify assumptions and gather relative design information for remaining devices.

5. HALL MULTIPLICATION BASED POWER SENSOR SYSTEM

5.1. INTRODUCTION

The following chapter is devoted to the integration of the Hall generator with the analog signal processing circuitry. Although all the sub-systems for the integrated power sensor have now been proven, it is necessary to verify the fully functional system and verify in both simulation and experimentation that the system performs as designed and within specification. The chapter commences with the system interfacing in which a functional description is given. The system is then verified in simulation according to the IEC standard followed by the experimental verification. Some layout issues will be presented along with the layout of the sensor system. The proposed sensor performance results will then be compared with that of similar such systems and the chapter will be concluded with a concluding summary.

5.2. SYSTEM INTERFACE

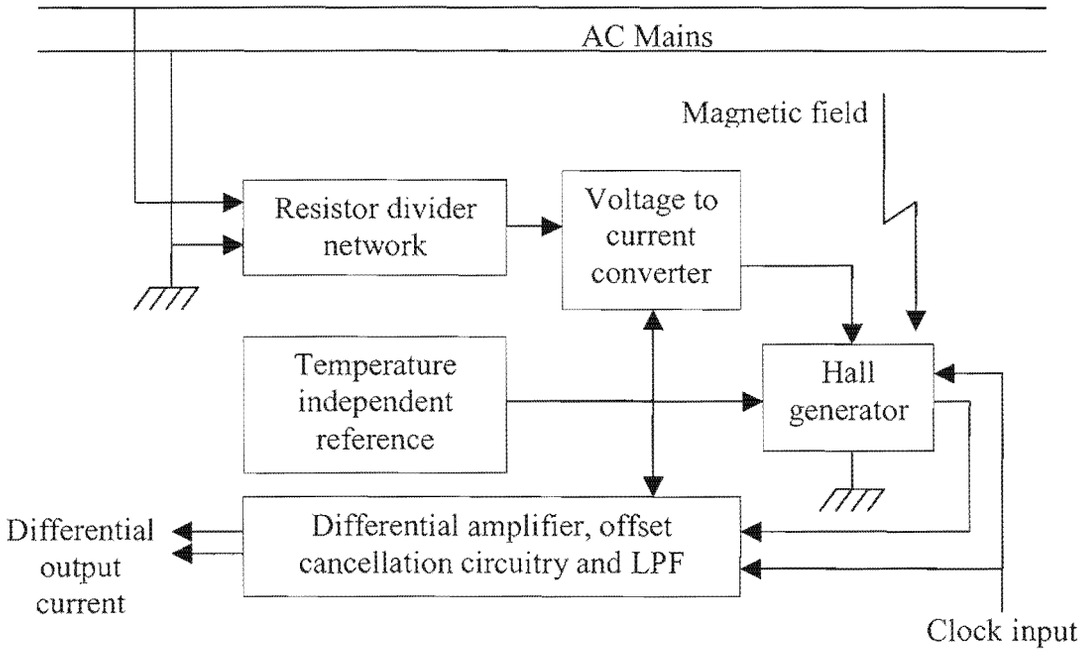

Figure 5.1 Schematic of integrated power sensor system

Figure 5.1 shows the block diagram of the proposed integrated power sensor system. The system implements a bandgap to generate a voltage required by the current biasing circuit. This circuit is used to bias the operational amplifiers in both the voltage to current converter as well as the output instrumentation amplifier. The system consists of 4 inputs and 3 outputs

namely the mains voltage, mains current (via the magnetic field), bandgap enable and clock making up the inputs and the output differential current and bias resistor making up the outputs. A detailed schematic of the system is given in addendum C.

The line voltage of 230 V_{rms} ac, has been scaled down to a 33.1 mV_{rms} signal using a resistor divider network. This is illustrated in figure 5.2 below. The resistors have been calculated according to Ohm's law, such that the rms current through the network is kept extremely small and has an rms value of 150 µA. R_4 can be used to calibrate the gain of the sensor, through adjusting the gain of the Hall generator. The divider network output is then fed into the voltage-to-current converter as illustrated in the block diagram above.

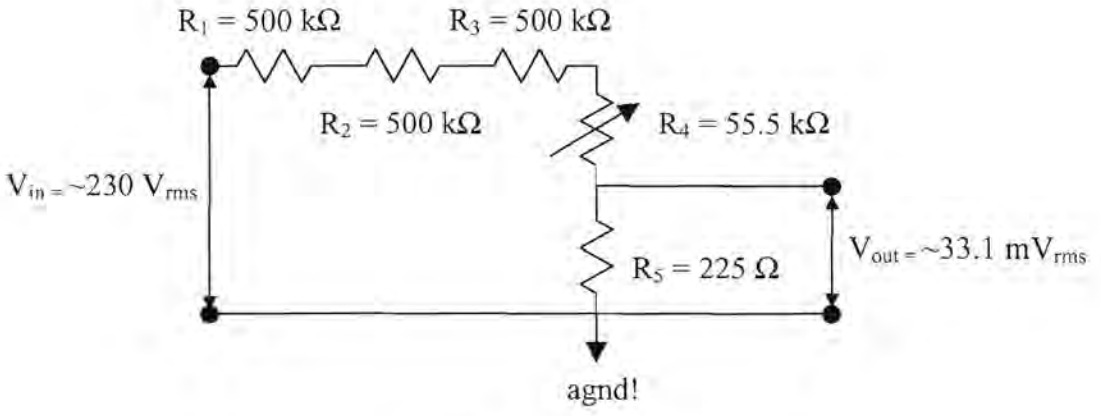

Figure 5.2 Resistor divider network

Figure 4.4 showed that resistor R_1, used to convert the input voltage into a current, had a value of 5 kΩ. The output transistor M16 to M19 in figure 4.14 have been scaled for a current gain of 40, thus biasing the Hall generator with the required 265 μA_{rms} or rather, an alternating current of 375 µA peak. The higher biasing current than the initial 300 µA that was suggested in paragraph 3.4.9, is due to the lower sensitivity of the Hall generator resulting from the influence of the geometrical correction factor determined in paragraph 3.6.1. With this gain, a peak Hall voltage of 6 mV is expected at rated conditions. The line current is sensed indirectly through a magnetic field with an expected peak value of 100 mT. The bandgap enable signal is generated by a standard cell from the digital library of the given process, that outputs a logic high, approximately 100 µs after the power supply has attained its maximum value of 5 V. This is to ensure that the bandgap output voltage is approached from the highest supply rail and that the output does not settle in its other stable state of 0 V. The final input consists of a standard logic square wave used to switch the Hall generator bias

and sensing terminal through 90°. This is implemented using the transmission gate network of figure 4.18. The gates are switched at a rate given by the clock frequency of 10 KHz. The differential output signal will consist of a differential current signal peaking at around 6 µA. The external resistor will be used to set up the reference bias current and was calculated to be 50 kΩ such that a current of 25 µA is generated using the bandgap voltage.

5.3. SIMULATION

The system must be verified in simulation before any manufacturing takes place, as this is a lengthy and expensive exercise. The system was simulated in union with all its components necessary for meeting the system specifications as described in paragraph 2. This chapter describes the simulations and results obtained. Certain specific circuit behavior scenarios with respect to the Hall generator were not possible to simulate, especially temperature dependencies as these behaviors have not yet been captured in a simulation model and were based solely on knowledge gained during the creation of this document. Compensation in this regard was taken into consideration where possible.

The specifications achieved in simulation are as follows:

Circuit operating voltage	5 V
Power supply range	0.9 to 1.1 U_n
Maximum supply current	typically < 1.9 mA
Operating temperature	-25°C to 70°C
Maximum Line Voltage	230 V_{rms}
Base current	20 A_{rms}
Maximum line current	80 A_{rms}
Line frequency	50 Hz
System sensitivity (Typical)	0.229 µA/kW (rms)
Temperature stability for 0.1 $I_b \leq I \leq I_{max}$	-0.042 %/K
Accuracy for 0.05 $I_b \leq I \leq 0.1\ I_b$	< 1.0 %
0.1 $I_b \leq I \leq I_{max}$	< 0.8 %
Voltage circuit max consumption	< 50 mW and 0 VA
Current circuit max consumption	Negligible
Process requirements	Standard silicon 1.2 µm CMOS, double metal, double poly

A large part of the typical current consumed in the circuit is a direct result of the factors involved in biasing the Hall generator. There exists a trade off between sensitivity and power consumption and maximizing the Hall sensitivity through an increased bias current, also increases the power consumed. The larger part of this current is consumed by the biasing of the output transistors M16, M17, M18 and M19 in figure 4.14 and can contribute more than 50 % of the total current required.

The system sensitivity was achieved and is better described by the accuracy figure obtained. As can be seen, the lower end accuracy was well within 1.0 % and compares well with the desired 1.5 %. The higher end specification was better than 0.8 %. The reason for a worse lower end specification presents itself in that when the output current is extremely small it becomes comparable in size to other undesired signals, dominated mainly by offsets. From the simulations regarding linearity of the instrumentation amplifier configuration, it was also noted that the linearity deteriorated around the origin of the amplifier and this behavior was expected. As two of these amplifiers are implemented in this circuit, both play a contributing role in this regard. As can be seen, the linearity quoted here display better results than the worst-case values of separate entities simulated earlier. This is because once the circuit is implemented in a kW/hr meter, the linearity becomes a function of time. This non-linearity presents itself as short pulses in time closely around the origin of the current and voltage signals and thus contributes very little to the root mean square (rms) value of the power signal. This will thus have a significantly smaller effect on linearity errors when averaged over time and hence, average linearity values are stated in the specifications.

Simulations showed that the Hall generators based on an n-well resistive model shows a linearity of 0.002 % within the given range of the specified magnetic field. In practice, this figure is expected to still be better than 0.05 %. It can thus be deduced that any improvement in linearity would present itself in the improvement of the instrumentation amplifiers.

The major advantage gained from the Hall generator is that as the voltage and current circuits are purely resistive with high impedances, the power consumed by these circuits become minimal. The major contributor to power consumed in the voltage circuit is the voltage divider network and is only 1.5 % of the maximum permitted 2 W.

The current circuit depends only on the measured magnetic field of the supply and its power contribution is thus negligible. As mentioned, the circuits are resistive and the Hall voltage reacts directly to the magnetic field and thus no phase shift occurs. This makes it possible to measure phase shifts in the supply line and eliminates the need for compensation of phase errors as with current transformers.

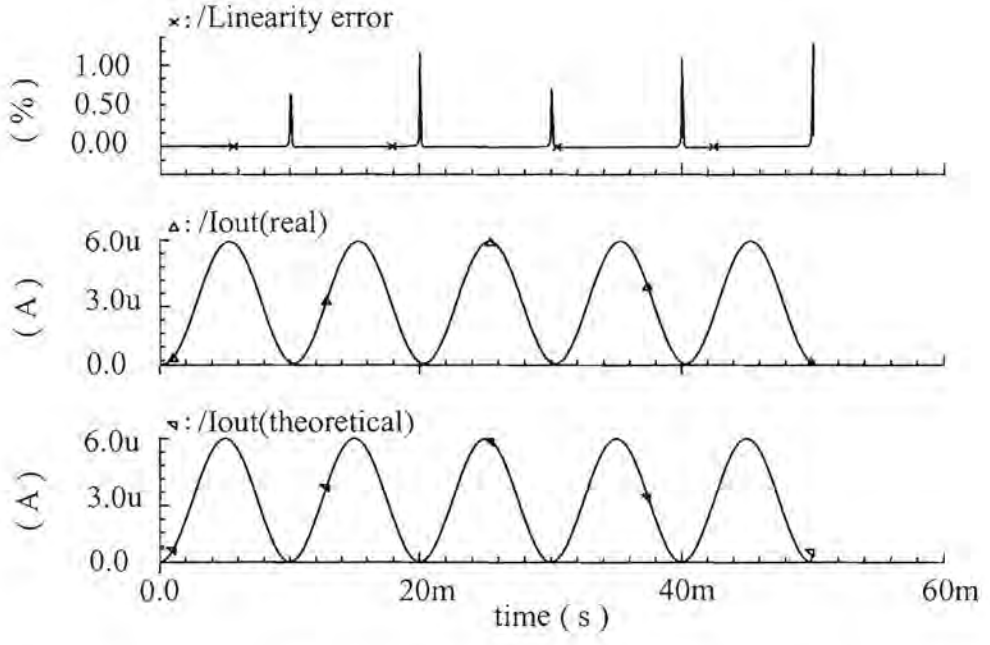

Figure 5.3 Simulation results showing the linearity error of the real current output versus the theoretically calculated model with no offset

Figure 5.3 shows the simulation results of the differential output current signal for a maximum line current and a line voltage of 230 V_{rms} versus the theoretically calculated model with no inherent offset present. These signals are then used to calculate the linearity error and it can be seen how the linearity is largest in the vicinity of the origin, a phenomenon that was expected based on previous simulations of the instrumentation amplifier. Once again, this also explains the reason for larger linearity errors at smaller signal levels where this problem has a larger contribution to the error.

Figure 5.4 shows the effect that the offset inherent in the Hall multiplier has on the output signal. The signal is severely distorted when compared to the expected sinusoidal output. The reason for this distortion lies in the fact that the offset is a function of the bias current and is analyzed as follows.

$$V_{offset} \propto I_{bias} \tag{5.1}$$

Also,

$$V_{hall} \propto I_{bias} B + V_{offset} \tag{5.2}$$

From Equation (5.1) it can be seen that the offset voltage is directly proportional to the bias current and that the Hall voltage is the sum of the cross product of the bias current and the perpendicular magnetic field and the offset voltage as shown in Equation (5.2). Now we know that if the bias current and the magnetic field are both sinusoidal, the resultant product is of the form $\cos^2(\omega t)$ but that the offset is of the form $\cos(\omega t)$. The resultant output will thus be a function of two frequency components, one consisting of *f* and the other of *2f* and the larger the inherent offset, the larger will be its contribution to the resultant output.

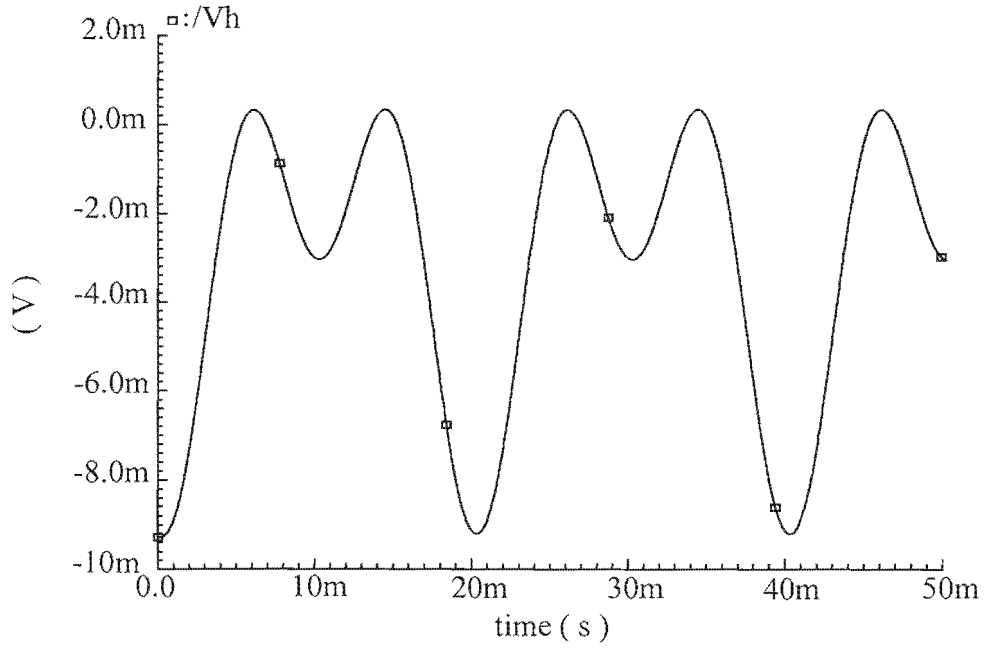

Figure 5.4 Simulation showing the effects of offsets on the Hall voltage signal

The resultant output with implementation of the offset cancellation technique is shown in figure 5.5 whereby the Hall generator is electrically rotated by 90° at a frequency of 10 KHz, taking advantage of the fact that a 90° rotation causes a 180° phase shift in the offset voltage and a 0° shift in the Hall voltage thus isolating the offset voltage from the Hall voltage. The net result is that the offset voltage signal is translated to the much higher frequency at which

the Hall generator is being switched and the information-carrying signal can be retrieved through low-pass filtering.

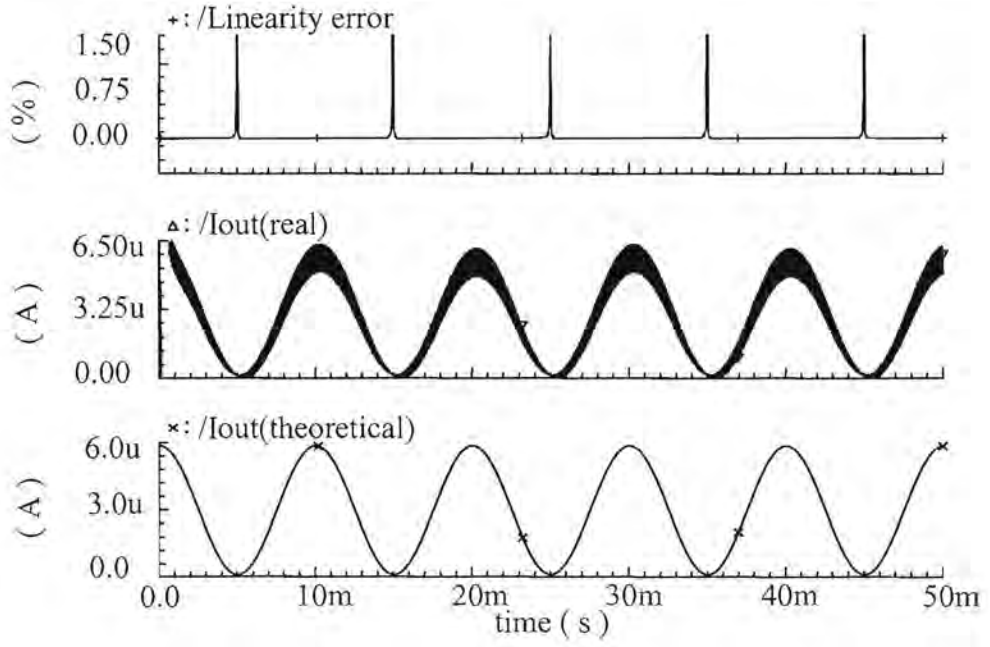

Figure 5.5 Simulation results showing the linearity error of the real current output versus the theoretically calculated model inclusive of offset after filtering

Figure 5.6 shows a closer view of the switching transients present in the output signal. The clock frequency used is a 10 KHz clock, for quadrature rotation of the Hall generators.

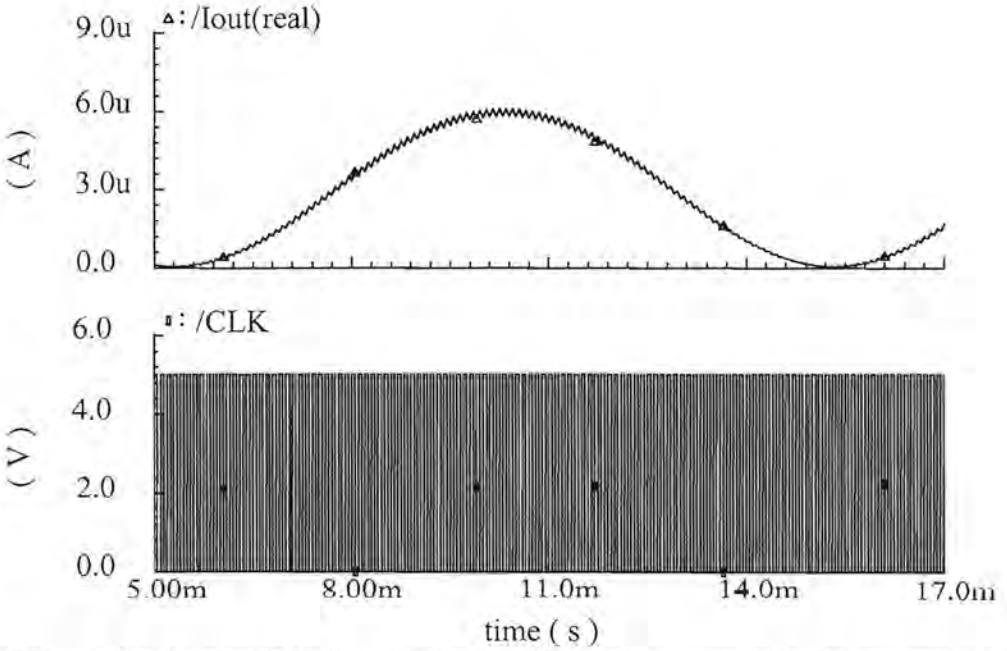

Figure 5.6 Simulation showing switching noise present in the output current in the presence of a 10 KHz clock frequency

Figure 5.7 shows the dependence of the output signal to a variation in temperature for an input signal of V_{mains} = 220 V_{rms} and I_{max} = 80 A. The difference in current between markers A and B show that the output varies by 200 nA over the temperature range of –25 °C to 70 °C. This translates to a temperature dependency for the output current of -0.035 %/K, which falls within the specification requirements. Similar simulations over the line current range showed the worst coefficient to be -0.042 %/K. The coefficient still falls within the requirements however, the behavior is extremely close to the limits and process variations could place this value outside the required specification. The temperature coefficient indicates that the overall system sensitivity decreases with an increase in temperature.

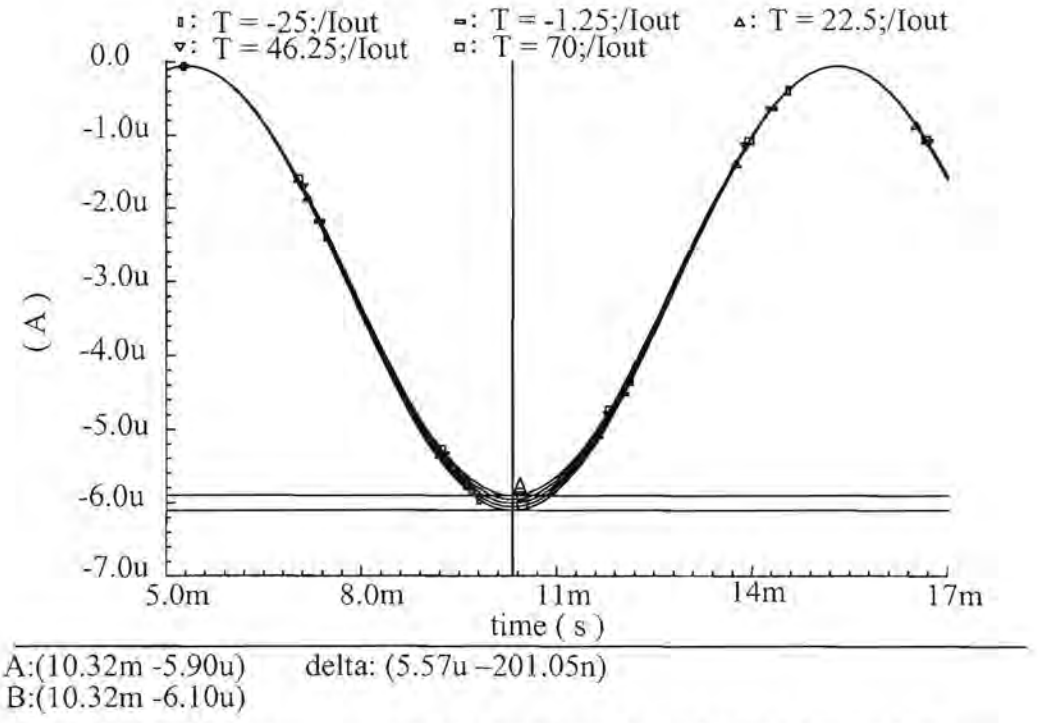

Figure 5.7 Simulation results of output signal dependence on temperature

Figure 5.8 shows the simulation result of the supply current consumed in the sensor circuit. The current has an average value of approximately 1.88 mA at a supply voltage of 5 V. This translates into a power consumption figure of < 9.4 mW.

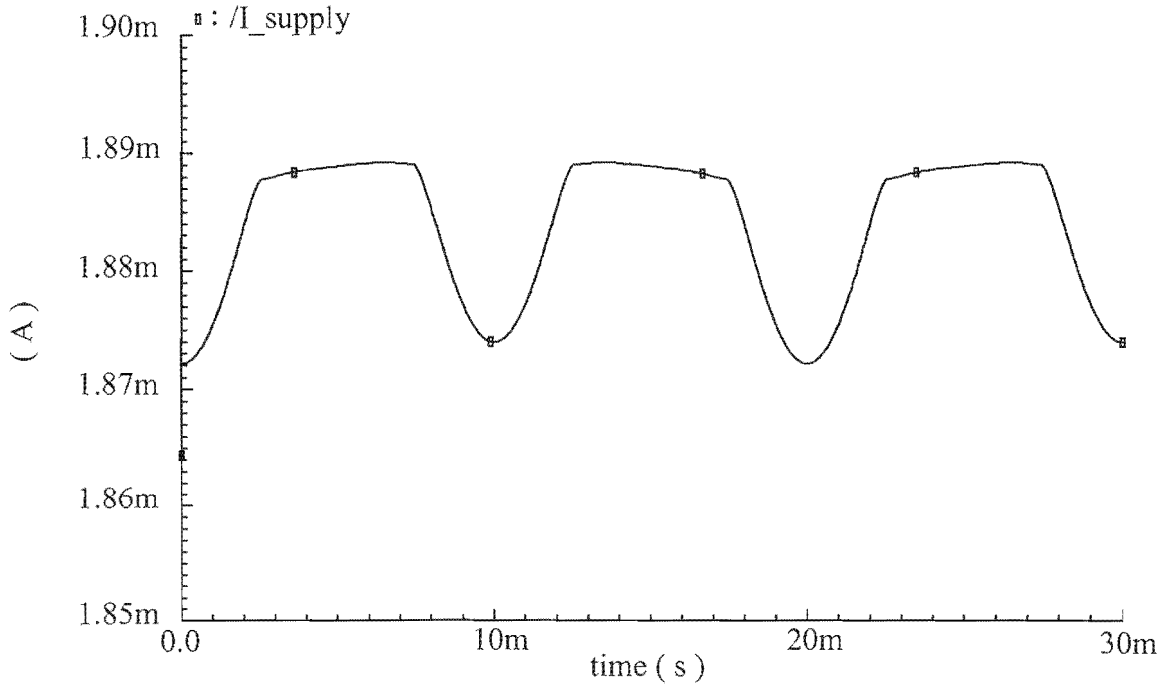

Figure 5.8 Simulation result showing supply current versus time

5.4. EXPERIMENTAL VERIFICATION

The experimental verification was done under standard room temperature conditions using the suggested wire-wound ferromagnetic core to generate a magnetic field. A discrete voltage to current converter with similar specifications as the suggested component in this document was used, the only difference being that the resistor was implemented externally. Once again, the system was assembled with the components available as in the previous chapter due to a limitation in resources. The principle could still be tested and sufficient knowledge was gained so as to assess the extent of performance compliance as well as the required guidelines necessary for the development of future circuit architectures.

5.4.1. The Hall multiplier

The Hall sensor used for the verification of the design data, was configured slightly differently to that required by this specific design. The element was configured such that the output Hall voltage changed its phase by 180° with a quasi-constant offset voltage. Furthermore, one of the biasing terminals was permanently tied down to V_{SS}. This configuration is typically used in linear sensing applications whereby the sensor is biased with

a dc current. This creates a major problem for power sensing applications as a negative swinging bias current results in the Hall generator being forward biased across its n-well to substrate, or rather, the n-well to substrate acts as a normal forward biased diode. To overcome this problem, the bias current through the Hall generator was rectified. Figure 5.9 illustrate the results captured on an oscilloscope. The figure shows two signals; 1) showing an amplified signal of the Hall generator and 2) the rectified mains voltage used to bias the Hall generator itself. From this it is evident that the rectification in the mains voltage and not the mains current causes the output to be negative on all even cycles. It can also be seen that the offset causes a distortion in the zero crossings and can be seen in the different levels at which the zero crossings occur.

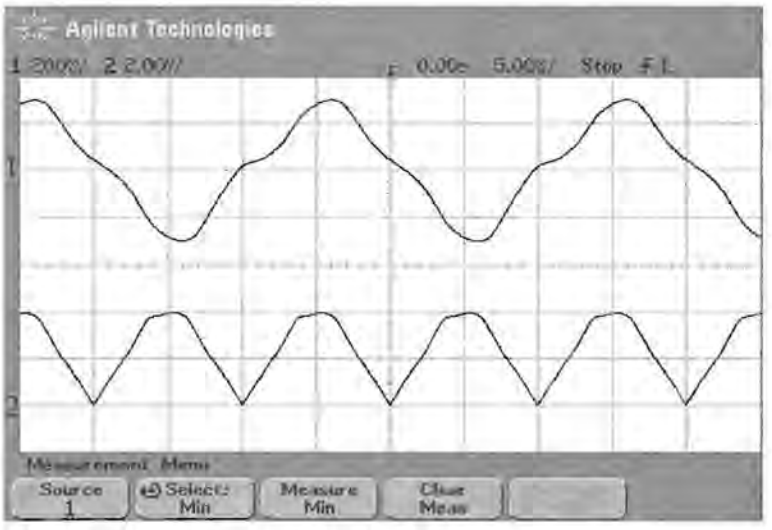

Figure 5.9 Graph showing measured results of 1) the amplified Hall generator output and 2) the rectified signal used to bias the Hall generator

The problem of the offset inherent in the output signal becomes a larger problem in this type of configuration, as the offset itself now too is a component of 100 Hz due to the rectified line voltage now being a 100 Hz signal. The offset now becomes part of the signal representing power output making it indistinguishable from the desired information. This illustrates the importance of a switching scheme implementing a quasi-constant Hall voltage as suggested in this document. This will make it possible to translate the offset signal to a much higher frequency and simply low-pass filtering the output signal. For illustration purpose, the Hall generator was switched with a 50 Hz signal in phase with the line voltage thus making it possible to rectify the line current. Figure 5.10 shows the physical results captured on an oscilloscope with a line current of 5 A_{rms}. The offsets can now be seen in the first signal at the

lower end, with a 100 Hz repetition rate. The offsets at the zero-crossings are also worsened by non-linearity in zero crossings in both the magnetic field during switching and rectification of the line voltage due to simple bridge rectifier forward voltages.

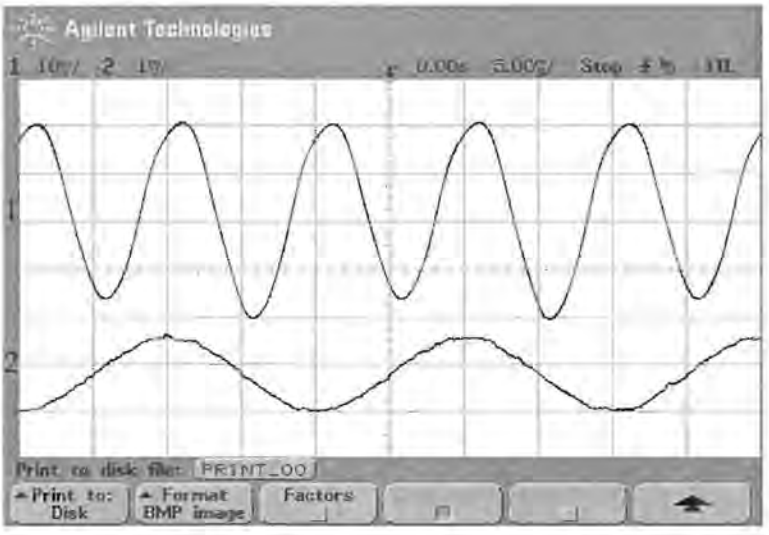

Figure 5.10 Graph showing measured results of 1) the Hall generator signal and 2) a voltage representation of the line current used to generate the magnetic field over the Hall generator

5.4.2. Linearity

The first experiment was aimed at establishing what the linearity of the sensor was, and consisted of the Hall sensor combined with the amplifiers. As the equipment available for the measurements could only supply a maximum of 10 A_{rms}, the test results show only the lower end linearity tests. Figure 5.11 shows the results obtained for the lower end linearity of the sensor. The data shows the results obtained for the 4 A to 8 A, lower end current specification. The linearity proved to be between ±0.5 %. This thus proves that the time average will also fall within the required ±1.5 % maximum. As more circuitry is required for implementing the sensor within an energy meter, the extra headroom is necessary for allowing non-linearity inherent in these circuits. Once again, it can be seen how the non-linear characteristics of the instrumentation amplifiers affects the extreme lower end accuracy.

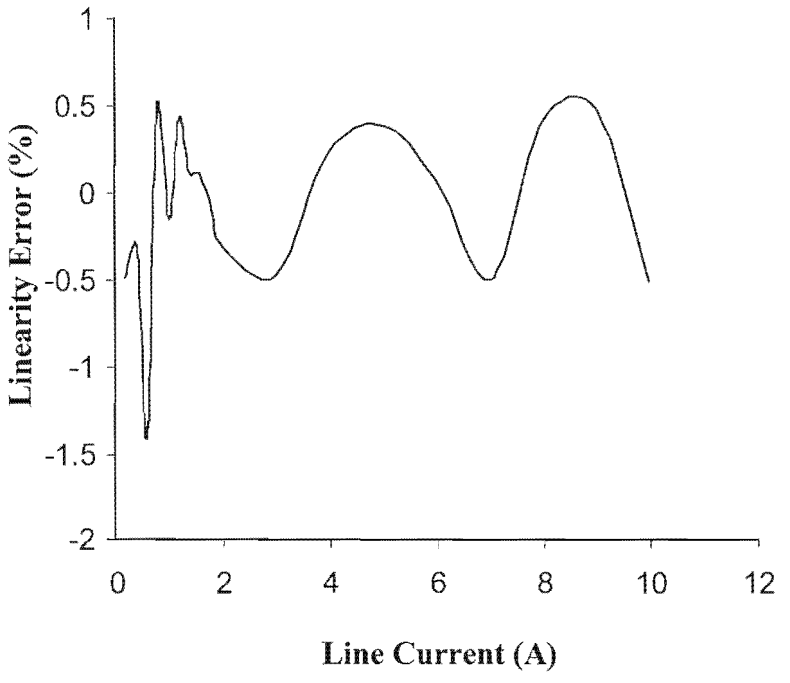

Figure 5.11 Graph illustrating the lower end linearity figures for the sensor versus line current

Figure 5.12 shows the transfer function used to calculate the linearity. The system sensitivity yielded a transfer function of 0.2302 µA/kW and is slightly higher than was simulated. This could be the contribution of various factors such as variations in the expected magnetic field produced in the ferromagnetic core, gain variations etc. This shows the importance for the need for calibration of such systems.

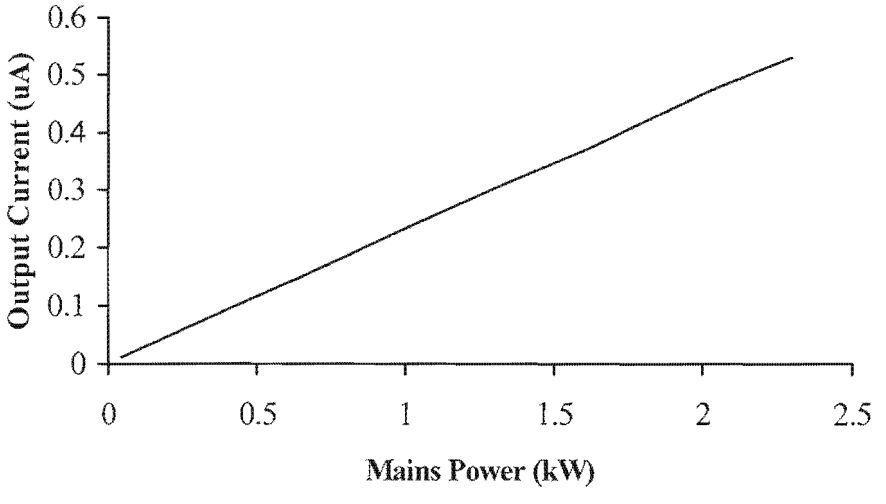

Figure 5.12 Graph illustrating the transfer function of the output current versus the input power

5.4.3. Temperature Stability

A series of experiments were performed regarding temperature tests of the Hall generator. It was found that the compensation method described in paragraphs 3.4.11 and 4.4.4 was indeed an effective solution. Although the method proved successful, more information was gathered regarding an effective placement of the compensation resistors. If the orientation of the chip shown in figure 5.15 can be defined as having its origin at the lower left hand corner of the chip, then the vertical dimension makes up the y-axis, and the horizontal, the x-axis. The following was found using this orientation as definition for the analysis. Figure 5.13 show the temperature compensated results of 3 random samples. The graphs illustrate how the temperature coefficient of the compensation resistor, compensates for the Hall generator sensitivity temperature coefficient, as a percentage of the difference between them. A 0 % result would be the ideal. The negative figures thus indicate an overcompensation of the sensitivity over the temperature range. This comparison is valid as the Hall generator and compensation resistor is manufactured of the same structure type namely pinched, n-well. The compensation resistors were strategically placed on both the same x and y-axis in close proximity to the Hall generator. It was found that the structures lying in the same y-axis yielded best matching properties. As the wafers are always orientated such that the crystal direction of the wafer is the same during processing ((100) crystal orientation), it will be possible to reproduce these results consistently, as the behavior is now defined and predictable.

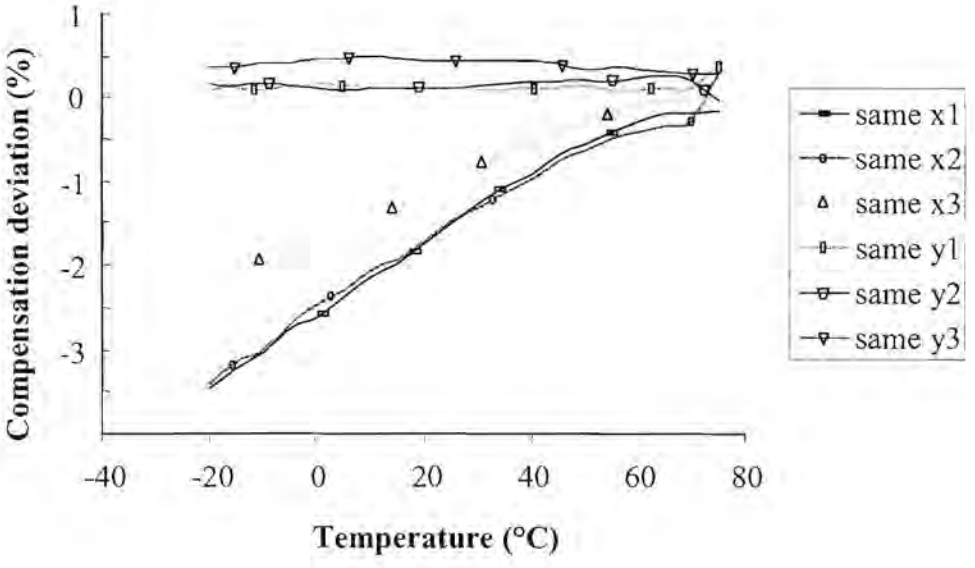

Figure 5.13 Graph illustrating compensation resistor effect when place in the same x and y-axis of the Hall generator

It can thus be seen that the same y-axis orientation of the Hall generator and compensation resistor, yields compensation capabilities of around + 0.005 %/K compared to same x-axis orientation of - 0.036 %/K. These results thus only include the temperature coefficients of the Hall generator and output amplifier with the compensation resistor, as they will dominate the temperature behavior of the sensor.

Figure 5.14 shows the results obtained for the temperature behavior of the sensor tested and include the Hall generator and output amplifier with its compensation resistor. The compensation resistor was orientation in the same x-axis direction as can be seen in figure 5.15. The sensitivity showed a temperature coefficient of - 0.055 %/K over the required temperature range. It can be seen that the result is slightly outside the required specification and that over compensation of the positive temperature coefficient of the Hall generator sensitivity has occurred. When looking at the typical voltage biased sensitivity of the Hall generator given by equation (3.36), this was to be expected. The voltage-biased sensitivity is not only negative, but also has a typical absolute value larger than that of the current biased sensitivity variation. As the compensation method is based on the change in voltage over the compensation resistor, the behavior is justified. Furthermore, the results could be improved with the same y-axis orientation of the compensation resistor.

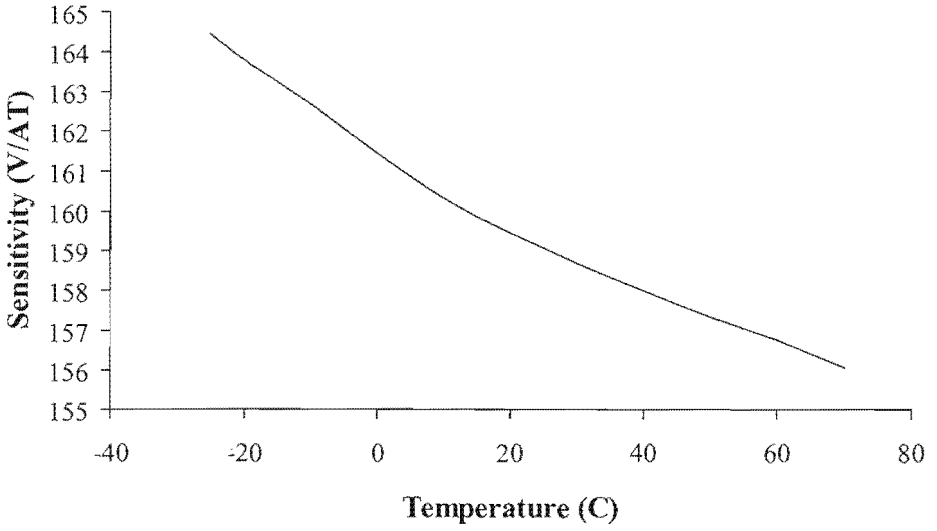

Figure 5.14 Graph showing temperature behavior of sensor sensitivity

5.5. LAYOUT AND PACKAGING

5.5.1. General Layout Considerations

The layout of an integrated circuit defines the geometries that appear on the masks used in fabrication. Micro-electronic layouts play an extremely important role in the performance characteristics of systems and can greatly influence the performance of a system to both its advantage and disadvantage. Care must thus be taken to properly plan the outlay of the device such that advantage can be taken of all relevant aspects that can have a positive effect on the performance of the final device. Aspects involved during the layout process involve adhering to the design rules for the given process used and the manufacturer involved supplies this data. Design rules incorporate aspects such as minimum sizes, spacing, enclosure and extensions as well as antenna effects. These rules aim to maximize the yield of devices manufactured as well as consistency in performance characteristics.

5.5.2. Analog Layout Techniques

The need for analog layout techniques are due to the fact that analog systems are more sensitive to negative effects caused by parasitic resistive and capacitive components such as crosstalk, mismatches, noise etc [28]. The most common techniques used during the layout included the likes of multifinger transistors for the reduction in parasitic gate resistance for increasing noise performance; symmetry for the reduction in input referred offsets and consists of matching device geometries as well as surrounding environment. Lastly, guard-band structures were implemented to separate the few digital components from the analog structures thus assisting in the reduction of switching noise induced in analog devices. Figure 5.15 shows a micrograph of the layout for the test chip used.

5.5.3. Packaging

It was mentioned before that the Hall generator suffers from piezoresistive effects. The effect presents itself through a change in the electrical resistance of the semiconductor upon the application of mechanical stress. The mechanism is as a result of the change in the interatomic distances in a crystal under stress [4, 6, 8]. A shift in the interatomic distances produces a change in the periodic field of the lattice and thus causing a change in the bandgap and effective masses of the carriers. This change in the mass thus causes a change in the mobility resulting in a mechanically dependent change in the Hall voltage signal. This mechanical

dependency can be minimized as mentioned before by biasing the Hall generator in a (110) direction to the crystal lattice of the semiconductor, defined as a (100) wafer, which can be clearly seen in figure 5.15. The layout legend is given in addendum D. Here, the Hall generator was placed at 45° to the vertical plane for the given layout rules of the process. The perpendicular stresses are thus completely minimized and the stresses caused by packaging are significantly reduced. These packaging stresses are the main causes of stress on the die.

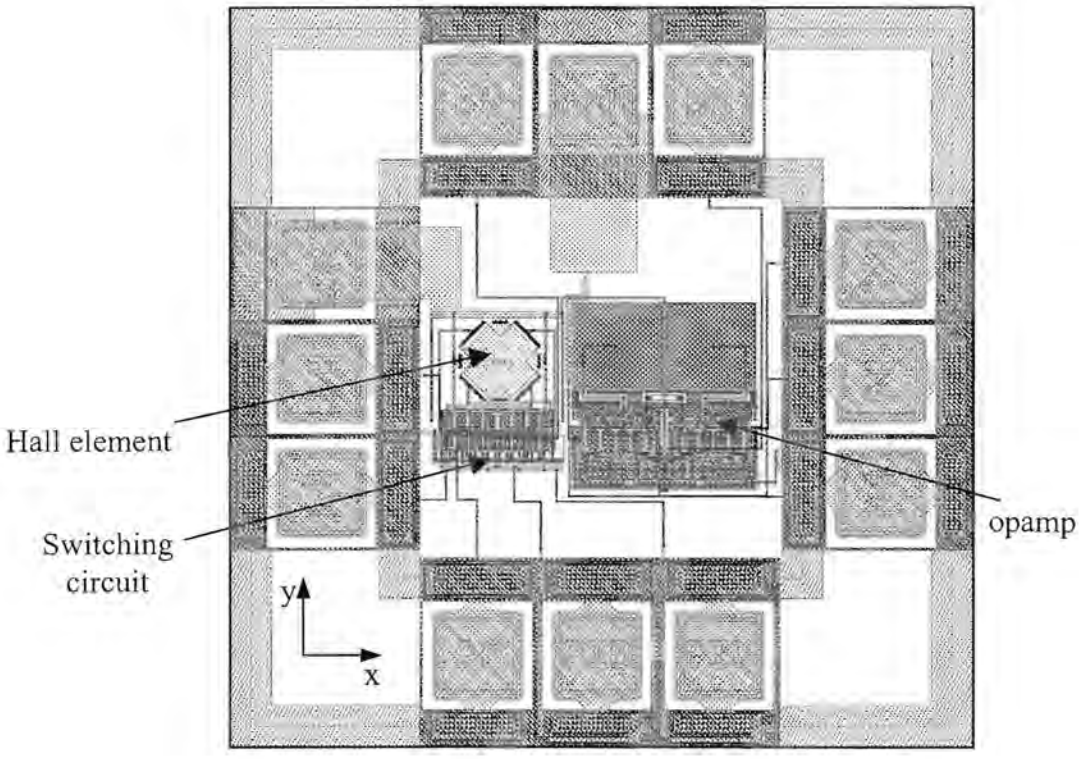

Figure 5.15 Micrograph of the layout of the test chip

A second packaging issue is a problem regarding the lead frames used in the packaging process. Firstly, the lead frames used in standard dual inline packaged (DIP) devices as well as small outline integrated circuit (SOIC) packages normally use paramagnetic materials such as aluminum and thus influence the magnetic field around the element on the die and secondly, for use with the ferromagnetic core, these and other standard packages are not mechanically suitable for the application. As a result, it was necessary to devise an alternative method for packaging the device to be tested. A cheap solution presented itself in the form of chip on board (COB) whereby the die is mounted on a standard printed circuit board (PCB) and "glob topped" for protection. This method proved an excellent solution as the PCB uses copper tracks (diamagnetic) for electrical connectivity and thus has no influence on the magnetic field under measurement. Furthermore, the final product is compact and thin

yielding easy access for the magnetic transducer over the interested die area. The test chip shown above resulted in a pad-limited design with dimension of 1330 µm x 1340 µm. Future layouts will also implement the y-axis matching principle.

Figure 5.16 shows the diagram of the physical test setup used to produce a perpendicular magnetic field over the Hall generator.

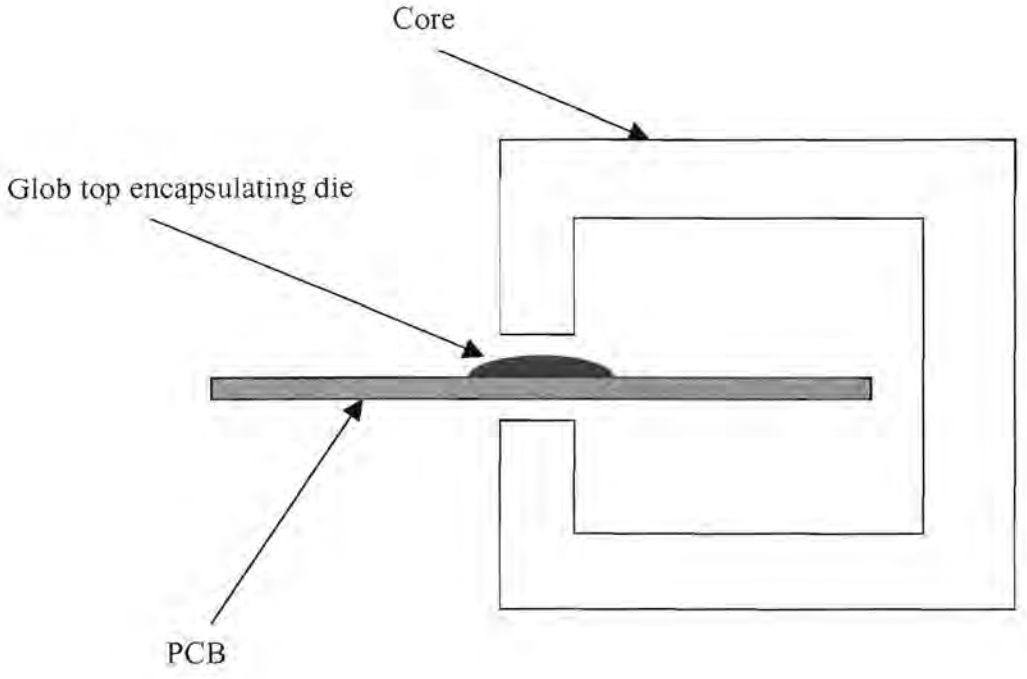

Figure 5.16 Mechanical arrangement for testing of Hall generator

5.6. COMPARISON TO SIMILAR SYSTEMS

It has been noted up to now that the major short fall of the device that was tested was that the signal processing circuitry limited the performance of the power sensor. The comparison has thus been drawn up to include performance specifications of fully integrated power sensor systems on the market using alternative methods of current and voltage sensing as well as the a direct comparison of the Hall generator with respect to the likes of CT's and shunt resistances. The voltage circuits of most power sensors use a similar architecture as proposed in this document.

The most dominant companies in the energy measurement market are our local semiconductor manufacturer South African Micro-Electronic Systems (SAMES) as well as the American based Analog Devices (AD). A comparable product from each company has been used for

comparison with the Hall effect device and will be referred to as the (SAMES) SA2002 [33] and the (AD) AD7755 [34]. These performance specifications will be given in their typical application set up.

5.6.1. SA2002

Circuit operating voltage	5 V
Maximum supply current	typically 3 mA
Operating temperature	-25°C to 85°C
Maximum Line Voltage	230 V_{rms}
Base current	25 A_{rms}
Maximum line current	100 A_{rms}
Line frequency	45 - 65 Hz
Output	Digital pulses proportional to power consumed
System sensitivity (Typical)	18.4 kW/1360 Hz (peak)
Temperature stability for 0.1 $I_b \leq I \leq I_{max}$	< 0.025 %/K
Accuracy for 0.05 $I_b \leq I \leq I_{max}$	< 0.5 % Dynamic range 1000:1
Circuit max consumption	± 25 mW and 4 VA
Current circuit power consumption	1 W (Shunt)

5.6.2. AD7755

Circuit operating voltage	5 V
Maximum supply current	typically 3 mA
Operating temperature	-25°C to 85°C
Maximum Line Voltage	230 V_{rms}
Base current	25 A_{rms}
Maximum line current	100 A_{rms}
Line frequency	45 - 65 Hz
Output	Digital pulses proportional to power consumed
System sensitivity (Typical)	18.4 kW/1360 Hz (peak)
Temperature stability for 0.1 $I_b \leq I \leq I_{max}$	< 0.01 %/K
Accuracy for 0.05 $I_b \leq I \leq I_{max}$	< 0.2 % dynamic range 500:1
Circuit max consumption	± 20 mW
Current circuit power consumption	1 W (Shunt)

Both systems achieve higher performance specifications for use within energy measurement systems. It must however be remembered that the systems mentioned here have evolved over many years and have been market driven into their current state of performance. The most noticeable difference however is that the devices above have to take into consideration all the disadvantages stated in the introduction of this document with respect to higher power consumption in shunt resistors, higher complexity due to phase shift correction needed caused by the CT's implemented as well as the need for these external devices. It will thus be advantageous to rather make a comparison to the sensing elements themselves as signal process circuit development will always evolve such as to drastically improve circuit performance in the future.

CT's are expensive but have the advantage of circuit isolation between line current and measurement device and also consume negligible power. Their disadvantage is that they introduce significant phase shift error that needs to be corrected. The CT's typically used with the above energy measurement devices have typical ratings as illustrated in Table 5.1.

Table 5.1 Table showing linearity and phase errors for current transformers

Contents	Linearity Error (%)			Phase Shift (′) (minutes)		
Current	0.25 A	3 A	5 A	0.25 A	3 A	5 A
Accuracy	0.50 %	0.50 %	0.20 %	25′	25′	10′

A typical shunt resistor can be up to 625 μΩ and thus has its major disadvantage in high power consumption with losses of $P = I^2R$. They are however cheap devices and surface-mount shunts have made for compact systems. Shunt resistors are inserted in series into the current line and thus do not isolate the current sensing circuit from the main line. Linearity for these devices is extremely good. The results are shown in Table 5.2.

Table 5.2 Table showing linearity error and power consumed for a 625 μΩ shunt resistor

Contents	Linearity Error (%)			Power Consumed (W)		
Current	0.25 A	3 A	80 A	0.25 A	3 A	80 A
Accuracy	Excellent			39 μW	5.63 mW	1 W

Table 5.3 shows the specifications for the Hall generator proposed in this dissertation including its amplifiers and the advantages of this system become clear once compared to the equivalent CT and shunt resistor. It can be deduced that with more accurate amplification

circuits, the device shows great potential to replace its counterparts in certain applications. The power consumed in the device will only be a function of the bias current needed in the element and it can be seen that no phase shift errors are introduced. Furthermore, the linearity of the device is directly comparable with the other devices. The system however has the advantages that it is now fully integrated into the power sensor system and thus eliminates the need for these external devices at the cost of increased die area. The only disadvantage is that the linearity deteriorates quickly at low current levels but many ways exist to compensate for this.

Table 5.3 Table showing linearity error, power consumed and phase error for the Hall generator

Contents	Linearity Error (%)			Phase Shift (′) (minutes)			Power Consumed (W)
Current	0.25 A	3 A	5 A	0.25 A	3 A	5 A	Biased @ 300 μA_{peak}
Accuracy at given current	<1.00 %	<0.5 %	<0.5 %	0′	0′	0′	< 150 μ W

5.7. CONCLUSION

This chapter focused on the Hall multiplication based power sensor system in which the complete sensor system was described. The system was described with reference to the initial system design proposed in chapter 2. The complete system interface was discussed and the final circuit operation was presented. The complete system was simulated and relevant performance specifications were presented and analyzed with specific reference to linearity and temperature based performance characteristics. Specific weaknesses were identified and the underlying reasons for these discussed. Some subsystems of the design were manufactured using the proposed 1.2 μm CMOS process, characterized and compared to simulation data. The IC layout and packaging problems were discussed and methods for overcoming these specific known problems were presented. A micrograph of the design to be manufactured was shown implementing all these strategies discussed. The data was then used to place the work presented here into perspective when compared to other similar systems such that the initial hypothesis of advantages and disadvantages could be analyzed.

6. CONCLUSION

6.1. WHAT WAS GIVEN?

Modern solid-state power meters contain elements for sensing both voltage and current. Resistor dividers are typically used for voltage sensing and current sensing technologies currently deployed in the market include low resistance current shunts, current transformer (CT) and the Hall effect sensor. In energy measurement systems, analog and digital multiplication require circuit overhead and complexity when compared to the use of an integrated Hall generator. This is due to the inherent multiplication properties of the Hall generator and can be implemented such that the output directly represents active power through indirect measurement of the line current and voltage. This reduction in complexity as well as expensive external devices has created the need for investigation into the replacement of conventional sensing methods with the Hall effect multiplier.

6.2. WHAT WAS THE AIM?

Implementing the Hall generator as a two-vector multiplier was the core topic of the research described in this document. It was proposed to design a complete active power sensor based on Hall effect multiplication. The work would thus establish the foundation for implementation into energy measurement systems. It would thus also be established whether the Hall generator would be sufficient as a sensing element and whether its properties can be transformed into an overall system advantage regarding increased economic value, decreased complexity and chip area.

6.3. WHAT HAS BEEN ACCOMPLISHED?

This document described the design of an active power sensor system that utilized the multiplication properties of the Hall generator. Firstly the power sensor architecture was proposed and all circuit requirements were highlighted and discussed. The implementation within traditional watt-hour meters were presented along with the IEC 1036 standard according to which the system performance specifications were measured. The most relevant design considerations were analyzed and were followed by the system requirements for the entire system based on performance, operating conditions and accuracy conformance.

The Hall generator itself was investigated based on the study of well-developed models for galvanomagnetic effects in semiconductors. It was discovered that different geometrical

shapes for Hall generators produce different advantages under different circumstances and that the cross-shape Hall generator was well suited to highly linear applications. A cross-shaped Hall generator was designed for the proposed application, manufactured and tested in a standard 1.2 µm CMOS technology.

The analog signal processing circuitry required by the Hall generator was designed and consisted of the temperature independent reference, biasing circuitry, operational amplifiers, voltage to current converter and instrumentation amplifier. The offset compensation technique was also designed based on the quadrature rotation of the Hall generator that of which was filtered out by the low pass filter circuitry. Transmission gates were used to implement the quadrature rotation. Temperature compensation was implemented using techniques that assist in maintaining constant sensitivity of the Hall generator under varying temperature conditions.

The final system was then designed whereby self-start circuitry was added as required by the bandgap reference as well as the necessary clock buffers necessary for driving the switching circuitry required for offset cancellation. The system was compared to energy measurement devices currently employed on the market with respect to only the relevant factors. The sensor was also compared to other current measurement sensing devices so as to establish grounds for potential improvement. It was found that the energy measurement devices outperformed the proposed sensor even though the IEC specifications were attained but that the Hall sensor itself performed well in comparison to other current sensors.

6.4. WHAT CAN BE LEARNED FROM THIS?

It can be seen that the Hall sensor system as a whole entity did not achieve the performance specifications as those achieved by current energy measurement devices. The system did however achieve the requirements set out by the IEC 1036 standard and it was established that these high performance specifications have been driven by market competitiveness.

By comparing the Hall generator performance to other sensing elements, it was found that the element itself outperforms mainly CT's and has a few advantages over shunt resistors in terms of reduced power consumption. It could thus be established that the limiting factor in terms of circuit performance was mainly the cause of under performing analog circuitry. The result however would be to raise the performance expectations for each individual building block

such that the overall system performance would benefit accordingly. Poor linearity performance of the instrumentation amplifiers serve as the main focus point for potential performance enhancements as more than 90 % of the linearity error was contributed by the configuration.

This iteration served as the foundation for performance specifications as well as a circuit configuration for a fully functional power sensor system. The design was based on specifications set out by the IEC 1036 standard governing such device performance specifics and an attempt was made to implement a design that would comfortably attain these. The interrelationship between different blocks were taken into consideration during the design such as compensation techniques and offset cancellation and data was gathered regarding further improvement steps required by the system. As little literature exists on the subject of Hall effect multipliers, the complete system serves as a basis for greater understanding of the multiplying effect and its implementation.

6.5. WHAT IS THE NEXT STEP?

The step following this design would be to design the system described in this document for use with a suitable analog to digital converter. This would require the final output stage to be modified according to the input requirement of the AD converter. This could entail simple gain settings or even a voltage rather than a current output format. Should the output be required in the form of a voltage signal, temperature compensation would have to be implemented within the Hall generator biasing circuit whereby the biasing current is increased or decreased thus changing the element sensitivity accordingly. Furthermore, better implementations for the voltage to current conversion would be suggested as well as final gain stages as this would dramatically reduce the linearity error and also dominates minimum linearity error restrictions.

The low pass filter was designed as an external sub-system and this would be replaced by an on-chip equivalent. Due to the large values required by passive filters, the system would have to be implemented as an active switched-capacitor system and can potentially be integrated into the final amplification stage [30, 32].

The Hall generator itself presents significant enhancement potential in terms of gain whereby the elements can be physically reduced in size to increase sensitivity. This poses a major

opportunity for performance increases as the sensitivity could be more than doubled this way. The limiting factor here would be established by the technology design rules. Care must be exercised, as this would require a trade-off between device reproducibility versus increased sensitivity as larger variations between devices may be caused as a result of limitations in manufacturing accuracy. This along with certain layout enhancements such as fully integrated instrumentation amplifiers whereby the input pairs of the whole device are integrated as one entity instead of two as implemented in this solution could yield significantly improved performance.

Finally, the whole system would be implemented into an energy measurement device whereby all the performance specifications of similar devices as mentioned in this document will serve as the benchmark of achievement. Attaining these specifications would result in a product of high economical value when compared with these devices.