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DESIGN METHODS FOR INTEGRATED SWITCHING-MODE POWER AMPLIFIERS

by

Mladen Božanić

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SUMMARY

DESIGN METHODS FOR INTEGRATED SWITCHING-MODE POWER AMPLIFIERS

by

Mladen Božanić

Supervisor: Prof S Sinha

Department: Electrical, Electronic and Computer Engineering

University: University of Pretoria

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Keywords: Power amplifier, spiral inductor, switch-mode amplifier, Class-E amplifier, Class-F amplifier, impedance matching, streamlined design, SPICE netlist, BiCMOS, 0.35 µm process, 180 nm process, software routine.

While a lot of time and resources have been placed into transceiver design, due to the pace of a conventional engineering design process, the design of a power amplifier is often completed using scattered resources; and not always in a methodological manner, and frequently even by an iterative trial and error process.

In this thesis, a research question is posed which enables for the investigation of the possibility of streamlining the design flow for power amplifiers. After thorough theoretical investigation of existing power amplifier design methods and modelling, inductors inevitably used in power amplifier design were identified as a major drawback to efficient design, even when examples of inductors are packaged in design HIT-Kits. The main contribution of this research is engineering of an inductor design process, which in-effect contributes towards enhancing conventional power amplifiers. This inductance search algorithm finds the highest quality factor configuration of a single-layer square spiral inductor within certain tolerance using formulae for inductance and inductor parasitics of traditional single-π inductor model. Further contribution of this research is a set of algorithms for the complete design of switch-mode (Class-E and Class-F) power amplifiers and their output matching networks. These algorithms make use of classic deterministic design equations so that values of parasitic components can be calculated given input parameters, including required output power, centre frequency, supply voltage, and choice of class of operation.

The hypothesis was satisfied for SiGe BiCMOS S35 process from Austriamicrosystems (AMS). Several metal-3 and thick-metal inductors were designed using the abovementioned algorithm and compared with experimental results provided by AMS. Correspondence was established between designed, experimental and EM simulation results, enabling qualification of inductors other than those with experimental results

available from AMS by means of EM simulations with average relative errors of 3.7 % for inductance and 21 % for the Q factor at its peak frequency. For a wide range of inductors, Q-factors of 10 and more were readily experienced. Furthermore, simulations were performed for number of Class-E and Class-F amplifier configurations with HBTs with f_t greater than 60 GHz and total emitter area of 96 μm^2 as driving transistors to complete the hypothesis testing. For the complete PA system design (including inductors), simulations showed that switch-mode power amplifiers for 50 Ω load at 2.4 GHz centre frequency can be designed using the streamlined method of this research for the output power of about 6 dB less than aimed. This power loss was expected, since it can be attributed to non-ideal properties of the driving transistor and Q-factor limitations of the integrated inductors, assumptions which the computations of the routine were based on. Although these results were obtained for a single micro-process, it was further speculated that outcome of this research has a general contribution, since streamlined method can be used with a much wider range of CMOS and BiCMOS processes, when low-gigahertz operating power amplifiers are needed. This theory was confirmed by means of simulation and fabrication in 180 nm BiCMOS process from IBM, results of which were also presented. The work presented here, was combined with algorithms for SPICE netlist extraction and the spiral inductor layout extraction (CIF and GDSII formats). This secondary research outcome further contributed to the completeness of the design flow.

All the above features showed that the routine developed here is substantially better than cut-and-try methods for design of power amplifiers found in the existing body of knowledge.

OPSOMMING

ONWERPMETODES VIR GEÏNTEGREERDE SKAKELMODUS-DRYWINGSVERSTERKERS

deur

Mladen Božanić

Studieleier: Prof S Sinha

Departement: Elektriese, Elektroniese en Rekenaaringenieurswese

Universiteit: Universiteit van Pretoria

Graad: PhD (Elektroniese-Ingenieurswese)

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Alhoewel baie tyd en hulpbronne spandeer word op die ontwerp van sender/ontvangers, word die onwerp van drywingsversterkers dikwels voltooi met verspreide hulpbronne as gevolg van die tempo van die konvensionele ingenieursontwerpsproses en ook nie altyd op ’n metodiese manier nie, wat daartoe lei dat dit soms ’n iteratiewe proses raak.

In hierdie tesis word ’n navorsingsvraag gevra wat lei tot die ondersoek van die moontlikheid om die ontwerpsvloei van drywingsversterkers te optimeer. Na ’n sorgvuldige ondersoek van bestaande drywingsversterkerontwerpmetodes en modellering is die noodwendige gebruik van induktors geïdentifiseer as een van die groot struikelblokke in doeltreffende ontwerp, selfs wanneer induktorvoorbeelde deel vorm van die hoëprestasie-koppelvlakpakket (HIT-kit). Die grootste bydra van hierdie navorsing is die formulering van ’n ontwerpproses vir induktors, wat dan ook bydra tot die verbetering van konvensionele drywingsversterkers. Hierdie soekalgoritme vind die uitleg van ’n enkellaag- reghoekige spiraalinduktor met die hoogste kwaliteitfaktor binne sekere toleransies deur die formules vir die induktansie- en induktor- parasitiese komponente van die tradisionele enkel-π-induktormodel te gebruik. ’n Verdere bydrae van die navorsing is ’n stel algoritmes vir die volledige ontwerp van skakelmodus- (Klas-E en Klas-F) drywingsversterkers sowel as uitset-aanpasnetwerke. Hierdie algoritmes maak gebruik van die klassieke deterministiese ontwerpsvergelykings sodat die waardes van die parasitiese komponente bereken kan word vir gegewe insetparameters, wat die vereiste uitsetdrywing, werksfrekwensie, toevoerspanning en keuse van versterkerklas insluit.

Die hipotese is bewys in ’n SiGe BiCMOS S35-proses van Austriamicrosystems (AMS). Verskeie drie-metaal en dikmetaal-induktors is ontwerp deur bogenoemde algoritmes te gebruik en is vergelyk met die eksperimentele resultate wat deur AMS voorsien is.

Ooreenstemming is gevind tussen die ontwerps-, eksperimentele en elektromagnetiese simulasieresultate, wat die kwalifikasie van induktors, anders as dié waarvoor eksperimentele resultate van AMS beskikbaar is, moontlik maak deur die gebruik van EM-simulasies met ’n gemiddelde fout van 3.7 % vir die induktansie en 21 % vir die kwaliteitfaktor by die piekfrekwensie. Vir ’n wye verskeidenheid induktors is kwaliteitfaktors van 10 of meer gevind. Verder is simulasies gedoen vir ’n aantal Klas-E en Klas-F versterkerkonfigurasies met hetero-voegvlaktransistors met f_T groter as 60 GHz en ’n totale emitterarea van 96 μm^2 as drywingstransistor om die hipotesetoetsing te voltooi. Vir die drywingsversterkerstelselontwerp (wat induktors insluit) het simulasies gewys dat skakelmodusdrywingsversterkers vir ’n 50 Ω las by ’n 2.4 GHz-werksfrekwensie ontwerp kan word deur die geoptimeerde metode in hierdie navorsing te gebruik, in welke geval die uitsetdrywing ongeveer 6 dB minder is as waarvoor ontwerp is. Hierdie drywingsverlies is verwag, aangesien dit toegeskryf kan word aan die nie-ideale eienskappe van die drywingstransistor en die kwaliteitfaktorbeperkings van die geïntegreerde induktors, sowel as die aannames wat gemaak is in die berekeninge in die ontwerpproses. Alhoewel hierdie resultate vir ’n enkele mikroproses verkry is, is gevind dat hierdie navorsingsuitset steeds ’n algemene bydrae is deurdat die proses gebruik kan word vir ’n verskeidenheid CMOS- en BiCMOS-prosesse, wanneer laegigahertz-drywingsversterkers vereis word. Hierdie teorie is bevestig deur middel van simulasie en vervaardiging in die 180-nm BICMOS-proses van IBM, waarvan die resultate ook voorgelê is. Die werk wat hier aangebied word, is gekombineerd met algoritmes wat SPICE netlyste formuleer en ook die spiraalinduktoruitleg skryf in die CIF- en GDSII-formate.

Al bogenoemde kenmerke wys dat die roetine wat geformuleer is, aansienlik beter is as lukrake iteratiewe metodes vir drywingsversterkerontwerp wat in die bestaande literatuur gevind word.

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LIST OF ABBREVIATIONS

2-D	Two-dimensional
3-D	Three-dimensional
3-G	Third generation
3M	Third metal
AC	Alternating current
ADE	Analog Design Environment
AMS	Austriamicrosystems
BiCMOS	Bipolar complementary metal-oxide semiconductor
BJT	Bipolar junction transistor
CAD	Computer-aided design
CDMA	Code divison multiple access
CMOS	Complementary metal-oxide semiconductor
CIF	Caltech intermediate form
DAT	Distributed active transformer
DC	Direct current
DRC	Design rules check
DSSS	Direct sequence spread spectrum
EDA	Electronic design automation
EM	Electromagnetic
GaAs	Gallium-arsenide
GDS	Graphic Data System
GUI	Graphical user interface
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility-transistor
HIT-Kit	High Performance Interface Tool Kit
HS	High speed
HV	High voltage
IBM	International Business Machines
ISI	Institute for Scientific Information
ISM	Industrial, Scientific and Medical
LF	Low frequency
LNA	Low-noise amplifier

LVS	Layout versus schematic
MEMS	Microelectro-mechanical system
MEP	MOSIS Education Programme
MESFET	Metal-semiconductor field-effect transistor
MOSFET	Metal-oxide semiconductor field-effect transistor
MOSIS	Metal Oxide Semiconductor Implementation Service
MPW	Multi-purpose wafer
NDA	Non-disclosure agreement
NMOS	n-channel MOS
PA	Power amplifier
PAE	Power added efficiency
PCB	Printed circuit board
PDA	Personal data assistant
PEEC	Partial Element Equivalent Circuit
pHEMT	Pseudomorphic HEMT
PMOS	p-channel MOS
PWM	Pulse-width modulated
Q-factor, Q	Quality factor
QFN	Quad flat no-lead
RF	Radio frequency
RFC	Radio-frequency choke
RFIC	Radio-frequency integrated circuit
RFID	Radio-frequency identification
Si	Silicon
SiGe	Silicon-germanium
SMA	SubMiniature version A
SPICE	Simulation program with integrated-circuit emphasis
THD	Total harmonic distortion
TM	Thick metal
VBIC	Vertical Bipolar Inter-Company
VCO	Voltage-controlled oscillator
WLAN	Wireless local area network

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CHAPTER 1 INTRODUCTION

1.1 BACKGROUND TO THE RESEARCH

In the recent mobile telecommunication history, a number of wireless modulation schemes have found commercial use. Transmitter devices employing these schemes all demand a power amplifier (PA) for their successful operation. Figure 1.1 shows the PA as a part of a simple telecommunication system [1]. Bulky and high-power off-the-shelf component-based PAs are being replaced by radio-frequency (RF) integrated circuit (RFIC) PAs [2], operating from low-voltage power supplies [3]. This trend is evident in a wide spectrum of analogue and digital applications, starting from short distance (cordless phones, Bluetooth, wireless local area networks (WLANs)), to medium (RF identification (RFID)) and long distance applications (cellular phones, third generation (3G) devices) [4]. The PA remains a bottleneck in the full integration of wireless transceivers, especially if integration is done in pure silicon complementary metal-oxide semiconductor (CMOS) processes. For this reason, most commercial wireless devices use an external PA to drive an antenna. This external device is usually fabricated in technologies superior to the silicon (Si) CMOS, such as gallium-arsenide (GaAs) heterojunction bipolar transistor (HBT) technology [5].

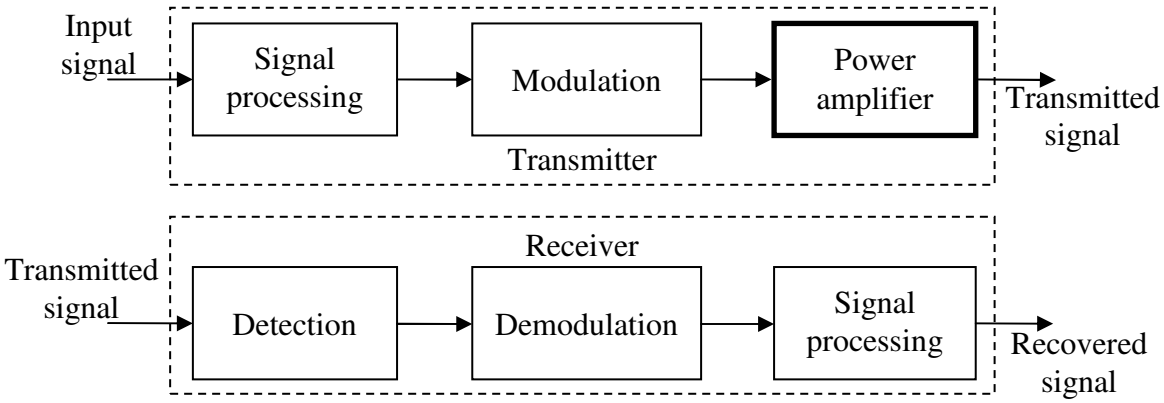


Figure 1.1. PA as a part of a simple telecommunication system [1].

Nevertheless, it is not always possible to separate a PA from the rest of the system, so that designers often have to be satisfied with a simple PA design in a pure CMOS process, or alternatively, a hybrid processes such as silicon-germanium (SiGe) bipolar-CMOS (BiCMOS) process [6].

In many RF modulation schemes, such as the direct sequence spread spectrum (DSSS) technique, it is necessary to design several PAs in order to ensure operation over different channels of the same band. For example, for a system based on DSSS [7], transmission is possible over a number of channels in Industrial, Scientific and Medical (ISM) band; their centre frequencies ranging from 2.4000 GHz to 2.4835 GHz. If a correct design methodology is not employed, designing of all PAs for all channels can be quite time consuming.

Basic PA is designed around one or more active devices, either metal-oxide semiconductor field-effect transistors (MOSFETs), bipolar junction transistors (BJTs) or HBTs. Several PA output stages are commonly used in telecommunications, with Class E and Class F widely used [8].

Irrespective of the output stage, and additional to the active devices, a number of passive components (inductors and capacitors) must be included. At the schematic design level this does not present a problem, because ideal capacitors and inductors can be used for the first design. However, translating of the design onto the layout level (where layout refers to actual drawing of components on a silicon wafer) becomes more intricate. Here, designing of an inductor poses a special problem, because of a great number of inductor options [9].

Even with a proper integrated inductor topology selected, the more affordable electronic design automation (EDA) software packages do not have built-in procedures for integrated inductor netlist extraction, but designers have to rely on inductors, if any, provided in High Performance Interface Tool Kits (HIT-kits). Furthermore, the built-in netlist extractors usually interpret an inductor as simply a long piece of metal or wire (which short-circuits the nodes placed at the two ends of an inductor), thus making the extracted netlists incorrect. Although there are a few models of integrated inductors described in literature [10-12], they are often not used by designers who are either satisfied by simulations at the schematic level or replace actual inductors with ideal inductors in order to proceed with the post-layout simulations. Drawbacks of such an approach might not be apparent at low frequencies, but they become particularly important in the design of PAs at RF, due to the fact that even small differences between actual and designed values of inductance can strongly affect the centre frequency, gain or efficiency of the amplifier. Often, these

mismatches can only be seen after the fabrication of the chip is completed, thus introducing additional unnecessary chip fabrication iterations.

1.2 RESEARCH PROBLEM AND HYPOTHESIS

In the description in Section 1.1, the following research problem can be identified:

> *What kind of methodology can be employed to speed up the design of power amplifiers together with their passives (inductors) for a range of wireless applications, at the same time taking care that high quality of amplification is maintained?*

To answer the research question, the following hypothesis is formulated:

> *If the performance of a power amplifier system is related to optimising its subsystems, then implementing a methodology that uses software algorithms to perform the optimization will produce better quality power amplifiers.*

To test the hypothesis, various PA and inductor options were investigated and those of Class E, and Class F identified as most commonly used topologies in RF design, because of their predisposition for high efficiencies and high power. Inductors were modelled as monolithic spiral inductors. Equations describing the PA and inductor models were used as a starting point when developing a method that allows that for a given a set of specifications such as PA bandwidth, centre frequency and class of operation, the best possible PA is found and designed. It is speculated, inter alia, that this method can be coined as a software routine. The same routine determines a geometry of a spiral inductor that gives the highest possible Q (quality) factor, using process parameters for a particular process. In parallel with the development of the software routine, a number of PAs were designed in the SiGe S35 (0.35 µm BiCMOS) process from Austriamicrosystems (AMS) [13] and simulated in order to verify the correctness of developed algorithms. Finally, the layouts of designed systems were prepared and then sent for fabrication to an auxiliary process from IBM[1] (IBM 7WL) process [14], in order to investigate aspects that cannot be

[1] IBM is the short name for International Business Machines.

covered in simulations, such as influence of parasitics, as well as correctness of the quality factor and inductance values of spiral inductors.

1.3 JUSTIFICATION FOR THE RESEARCH

Computer-aided design (CAD) is not uncommon in circuit design. Conceptual design is usually performed in a mathematical package, which can be followed by schematic design in a schematic editor. Performance of the circuit is normally simulated in SPICE[2] [15] based simulators. However, there are often various missing links, and the designer needs to resort to hand design to complete the design cycle. Being a common example of this problem, the design of PAs leaves an opportunity for a software routine to be developed that will aid this task.

1.4 METHODOLOGY

Various PA concepts were explored in depth to identify a few commonly used simple PA models to be used as a starting point for automating a PA design. A number of PAs based on these models were designed from the first principles in MATLAB from Mathworks [16], and then simulated with the aid of a Cadence Virtuoso circuit design and simulation package from Cadence Design Systems [17]. Knowledge gained from the design and simulation was at the same time used to design a program in MATLAB that automates this design. Layouts for several good circuits were drawn (in Virtuoso Layout Editor which is also a part of Cadence Virtuoso), and then the IC was sent for fabrication in the 180 nm BiCMOS process.

The detailed methodology followed in this thesis is described in Chapter 3.

1.5 DEFINITIONS

Definitions adopted by researchers are often not uniform; therefore the key and controversial terms have been defined to establish positions taken in PhD research.

As it will be explained in detail in Section 2.2.5, the PAs are grouped in classes, for example *Class A*, *Class E.* etc. If the letter naming the class follows the keyword *Class* without a dash (*Class A*), the keyword-letter combination is used as a noun. If a hyphen is

[2] SPICE stands for simulation program with integrated-circuit emphasis.

used, the combination is an adjective (*Class-A amplifier*). The keyword *Class* is capitalized in most cases, in order to point out that it is part of the name of the particular PA.

1.6 DELIMITATIONS OF SCOPE AND KEY ASSUMPTIONS

Although concepts developed in this thesis can be transferred to a vast number of fabrication technologies, due to the time and financial constraints for obtaining prototypes, the use of only two (SiGe BiCMOS) technologies was possible. Application of the developed methodology to other technologies is proposed, but testing of this idea was only possible from conceptual perspective.

1.7 CONTRIBUTION OF THE RESEARCH

A new method for the design of the full PA systems has been proposed for the use in the low-gigahertz integrated applications. A detailed list of the resulting contributions to the body of knowledge is given here.

- Inductors have been identified as being traditionally difficult to integrate due to low quality factors and their indeterministic behaviour. Main contribution of this research is engineering of an inductor design process. This inductance search algorithm finds the highest quality factor configuration of a single-layer square spiral inductor within a certain tolerance using formulae for inductance and inductor parasitics of traditional single-π inductor model. This algorithm in effect contributes towards enhancing conventional PA design and is a major improvement over the common trial-and-error methods used by current designers.

- An algorithm for calculating inductance, parasitics and Q-factor of the existing square geometries, has also been developed, so that the feature for the quick analysis of existing inductor structures can be retained.

- This research also shows that in fact, with the correct design methodology, which includes optimisation for operation at correct frequency, quality factors in excess of 10 can be obtained for on-chip inductors without modification to the process or flow of fabrication.

- Several inductors have been designed using the above mentioned algorithm and comparisons made with the experimental results for the AMS S35 process provided by the AMS foundry. Correspondence is established between designed, experimental and EM simulation results. EM simulations enabled qualification of inductors other than those with experimental results available. Average relative errors of 3.7 % for inductance and 21 % for the Q factor at its peak frequency were obtained for both metal-3 and thick-metal inductor options available.

- Although intended for the use with PAs, the spiral inductor design algorithms can contribute in any other application that might require integrated inductors, for example the low-noise amplifiers (LNAs) [18], DC to DC converters [19] or voltage-controlled oscillators (VCOs) [20].

- Further contribution of this research is a set of algorithms for the complete design of the switching-mode (Class-E and Class-F) PAs. These algorithms make use of the classic design equations so that the values of the parasitic components can be calculated given input parameters, including the required output power, centre frequency, supply voltage, and choice of class of operation (Class E or Class F). These design equations are brought forward from the existing body of knowledge and combined into a single routine which makes them easier to handle during the design process.

- In high power and low voltage supply applications, antenna resistances reaching values of less than 10 Ω would be needed. To overcome this impracticality this thesis provides algorithms that automate impedance matching from optimum to standard antenna impedances (50 Ω).

- Simulations showed that, for the complete PA system design, output matching and real (spiral) inductors, switch-mode PAs for 50 Ω load at 2.4 GHz centre frequency can be designed using the streamlined method of this research for the power output of about 6 dB less than aimed. This power loss was expected, and it can be attributed to non-ideal properties of the driving transistor and Q-factor limitations of the integrated inductors.

- While these results were obtained for only two fabrication processes, it has been found that principles devised in this thesis are technology independent and can be used with a range of CMOS and BiCMOS processes.

- Additional algorithms, such as the one for the SPICE netlist extraction and spiral inductor layout extraction (CIF and GDSII formats), were found extremely beneficial for the completeness of the design flow and integration into a compact EDA tool.

Table 1.1 shows some PA and spiral inductor designs found in literature and their design methods, while focusing on strengths and weaknesses of each employed method. This table also shows where and how the research presented in this thesis extends the existing body of knowledge by overcoming the identified weaknesses.

Table 1.1. Comparison of the PA design methods found in literature with the one proposed in this thesis.

Ref	Impact factor[1]	Topic	Strengths	Weaknesses
[21]	2.043	Class-E PA design	• Single ended Class-E PA design is performed while taking the advantages of the BiCMOS process over inferior CMOS processes. • Design is optimised for high efficiency.	• Simulation-driven cut-and-try approach for the PA design is used. • Although the bond wire used for the resonant tank of the PA exhibits high Q-factor, such an approach cannot be extended to wider set of applications since the range of inductance values obtainable by bond wires is limited.
[22]	2.043	Two-stage Class-E design optimization tool	• Template-driven simulation-based methodology coined as software tool is presented. • The effects of parasitics for both active (transistors) and passive devices (inductors) are included.	• The tool seems to be too detailed for the goal that it accomplishes: the design of only one topology, viz. two-stage Class-E PA.
[23]	2.043	Class-E PA in 65 nm CMOS	• The design employs a differential topology. • Finite DC feed inductance reduces high-voltage stress.	• No design methodology for inductors is presented. • Although available switch-mode topologies are well researched, a repeatable design method is not speculated.
[24]	1.140	Class-F PA for low-voltage supplies	• Class-F PA utilizes a simple single-ended topology with input and output harmonic terminations. • High gain and high efficiency are accomplished.	• No design methodology for inductors presented • A repeatable PA design method is not speculated.
[25]	1.436	Optimizing the design of spiral inductors	• Analysis of the spiral inductor model leads to inductor width that maximises the Q-factor. • It is identified that the width is dependent on the spiral length	• Spiral length depends on input and output diameters making optimisation method impractical.

[1] ISI Web of Knowledge - Journal Citation Reports (Published by Thomson Reuters)

Table 1.1 (Continued). Comparison of the PA design methods found in literature with the one proposed in this thesis.

Ref	Impact factor	Topic	Strengths	Weaknesses
[26]	2.730	Analysis and synthesis of spiral inductors	• Advanced inductor modelling. • Full web-based inductor tool employs a search algorithm to synthesize inductors. • Both synthesis and analysis are performed.	• Although designs have been optimised for different parameters, little discussion pertaining Q-factors has been carried out.
[27]	2.730	Inductor layout design optimisation	• The method looks into the effects of core diameter, turn spacing and turn width on the overall performance of inductors.	• Multiple fabrication runs and wafer testing are necessary to optimise inductor designs.
[28]	2.730	Enhancement of the inductor Q-factor with low temperature annealing	• Although the substrate resistance is decreased which also decreases the Q-factor of the inductor, resistance of the spiral is decreased, resulting in overall inductor Q-factor increase.	• Substrate resistance decrease apart from decreasing inductor Q-factor, could be influential on other components of a PA.
[29]	2.302	Q-factor improvement by means of deep-trench-mesh substrate	• Decreased capacitive coupling and resistive losses lead to Q-factor improvements up to 28 % in 0.35 µm BiCMOS process.	• Cut-and-try method is used to optimise inductor designs. • Deep-trench-mesh might not be available in all technologies.
This work	-	Design methodology for switch-mode PA design	• Fully streamlined PA design method is presented for two-most common high-power high-frequency stages (Class F, Class E). • Matching and inductor design are presented. • Theory is fully backed up by means of simulations and experimental results (where applicable).	• The method only includes the design of the output stage.
This work	-	Optimisation of Q-factors of spiral inductors for square geometries	• All geometry parameters are taken into consideration and total geometry search is performed. • Search is governed by inductance and Q-factor. • Technology independent. • Simulation/model oriented (no fabrication is needed for test runs).	• No post-processing has been attempted.

1.8 PUBLICATIONS LEADING FROM THIS RESEARCH

The following journal articles have been published as part of research activities of the author:

- Božanić, M., Sinha, S., and Müller, A., 2010. Streamlined Design of SiGe Based Power Amplifiers. *Romanian Journal of Information Science and Technology (RJIST)*, Vol. 13, No. 1, pp. 22-32.
- Božanić, M. and Sinha, S., 2009. Design Approach to CMOS Based Class-E and Class-F Power Amplifier. *SAIEE Africa Research Journal*, Vol. 100, No. 3, pp. 79-86.
- Božanić, M. and Sinha, S., 2008. Software Aided Design of a CMOS Based Power Amplifier Deploying a Passive Inductor. *SAIEE Africa Research Journal*, Vol. 99, No. 1, pp. 18-24.

The following peer-reviewed international conference articles have been published and presented by the author:

- Božanić, M, Sinha, S., Müller, A. and du Plessis, M., 2009. Design Flow for A SiGe BiCMOS Based Power Amplifier, *Proceedings: IEEE International Semiconductor Conference (CAS) 2009*, 12-14 October, Sinaia, pp. 311-314.
- Božanić M. and Sinha, S., 2009. Design Flow for CMOS Based Class-E and Class-F Power Amplifiers, *Proceedings: IEEE AFRICON 2009*, 23-26 September, Nairobi, pp. 1-6.
- Božanić M. and Sinha, S., 2009. Design methodology for SiGe-based Class E power amplifier, *Proceedings: South African Conference on Semi and Superconductor Technology (SACSST)*, 8-9 April, Stellenbosch, pp. 31-36.
- Božanić, M. and Sinha, S., 2007. Design methodology for a CMOS based power amplifier deploying a passive inductor, *Proceedings: IEEE AFRICON 2007*, 26-28 September, Windhoek, pp. 1-7.

The following article was submitted to an ISI-listed peer-reviewed journal:

- Božanić, M. and Sinha, S., 2011. Switch-Mode Power Amplifier Design Method, submitted for publication in *Microwave and Optical Technology Letters*.

Program developed during the course of this research has also been commercialized (Appendix C).

1.9 OUTLINE OF THIS THESIS

Chapter 1 includes introduction to the thesis and a brief background for the research. The research question and hypothesis are clearly stated and justification for the research and its contributions are provided.

Chapter 2 provides the review of body of knowledge related to the context of this research. A brief discussion on PAs is given, followed by the more detailed discussion on the Class-A, Class-B, Class-C, Class-E and Class-F amplifiers, as well as on some hybrid classes. This is followed by a detailed discussion on inductors for PA applications, with special attention paid to the spiral inductor, its modelling, and techniques for increased quality factor integrated inductor design. Subsequently, some fabrication processes have been discussed in brief, with a more detailed discussion on the SiGe BiCMOS process and its relation to the silicon CMOS and GaAs HBT processes. The chapter concludes with the discussion on the importance of the rapid PA design.

Chapter 3 describes the methodology applied for the successful completion of the research presented in this thesis. It includes the research methodology outline, details on the software packages and design suites used for both research and development, background to the design process as well as description of the HBT SPICE model.

Chapter 4 describes concepts behind the MATLAB-routine based method for a rapid PA design. Flow diagrams of algorithms for the design of the Class-E and Class-F output stages, spiral inductor design, output impedance matching, as well as the flow diagram of the routine for the full PA system design are given here. For the complete program listings, the reader is referred to Appendix A. For the commercial version of the program, the reader is referred to Appendix C.

Chapter 5 describes the circuit level design and simulation of various PA systems used for testing of the first (MATLAB) version of the PA design routine. Circuit diagrams and simulation test benches and results constitute the bulk of this chapter. Inductor model and

inductance search algorithm are verified by means of EM simulations, as well as by comparison to the measured results. The streamlined use of the complete PA design routine is demonstrated by designing one Class-E and one Class-F output stage complete with input and output matching as well as biasing with minimum optimisation effort. For the technology files needed for completion of EM simulations, the reader is referred to Appendix B.

Chapter 6 presents layouts and photographs of the PA circuits submitted for fabrication as well the experimental results. The packaging and circuit board design issues are also discussed.

Chapter 7 concludes this thesis and gives suggestions for future research.

1.10 CONCLUSION

Chapter 1 laid the core foundations for this thesis. The research problem, viz. the need for a method to perform the tedious design of PAs and spiral inductors, has been formulated as a hypothesis, followed by the introduction to the research background. Solution to the research problem was proposed in the form of set of algorithms (initially developed in MATLAB) that will cover many aspects of a switch-mode PA design. Algorithms will additionally be able to handle modelling and design of the most important component of a PA – the passive inductor.

This chapter also briefly dealt with justification for the research and methodology used to carry out the research as well its contributions and research outputs to date. Finally, the outline of the thesis has been given. Chapter 2 follows with the review of literature.

CHAPTER 2 LITERATURE REVIEW

2.1 INTRODUCTION

Chapter 1 dealt with the introduction to the research performed in this thesis. In this chapter, a literature review is presented to place this into context of available knowledge. A few key concepts seminal to this study are identified and presented. Firstly, basic concepts of power amplification are listed, including some examples of good PA designs from the second part of the first decade of the twenty-first century. Secondly, a very important component of any PA, the inductor, is explored in depth, because a large number of different implementations and models available in literature make identifying a suitable inductor a time-consuming task. Thirdly, available fabrication technologies are investigated because understanding of the technology available for testing forms the foundation of this study. The fourth section of this review deals with the gap in knowledge when it comes to automating the task of rapid PA and passive inductor design. Finally, the conclusion of the chapter is drawn.

2.2 POWER AMPLIFICATION

PAs are used on the transmit side of RF circuit, typically to drive antennas with high power [8]. In such a scenario, the scaled-up versions of small-signal amplifiers used in the low-power low-frequency CMOS circuits are fundamentally incapable of high frequency, and other approaches must be considered [30]. In the monolithic PA implementations, the trade-off between efficiency and linearity is very significant [8]. In addition to these two determining factors for the PA integration, some other challenges, such as the limited supply voltage and heat generation, are also present. These factors often lead to the discrete PA designs or integration separate from the rest of the front end of the RF circuit.

Figure 2.1 shows a general single-ended PA model [31]. In this model, V_{DD} is the voltage supply, R_L is the load and *RFC* is the RF choke, and inductor is large enough to ensure the substantially constant current through the drain. In some designs, this inductor can be replaced by a finite one, if it forms a part of the output filter, also shown in this figure [32]. The output filter can include harmonic tuning and wave shaping, impedance matching or any other passive circuitry. The transistor T_1 is shown as an n-channel MOS (NMOS)

transistor, but it can be any power transistor (HBT, MOS, BJT or other) used in a particular PA application.

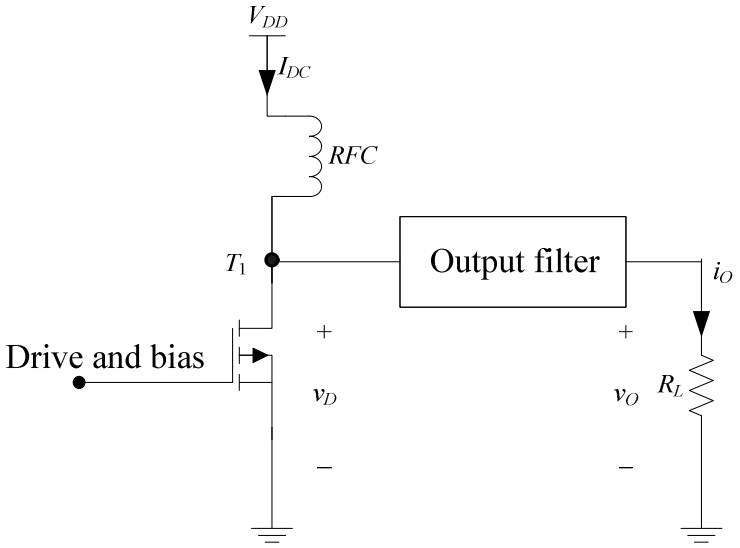


Figure 2.1. General model of PA [31].

2.2.1 Power capability

The task of a PA is to deliver a given power into the load [1]. This power is determined by the power supply voltage and the load. Maximum power that can be delivered is

$$P = \frac{V_{DD}^{\ 2}}{2R_L} \tag{2.1}$$

In case of Class-E and Class-F PAs, somewhat larger power can be delivered to the load. This will be detailed in Chapter 4.

2.2.2 Power consumption

Total DC power consumption is an important quantity in PA design, especially for battery powered portable devices. DC input power of a PA is the current drawn from the voltage supply over a period of time, or

$$P_{dc} = \frac{1}{T}\int_0^T V_{DD} i_D dt = \frac{V_{DD}}{T}\int_0^T i_D dt = V_{DD} I_{DC}, \tag{2.2}$$

where i_D is the drain current and I_{DC} is the DC component of the current waveform.

2.2.3 Power efficiency

Efficiency is a measure of performance of a PA. The performance of a PA will be better if efficiency is higher, irrespective of its definition. There are several definitions of efficiency commonly used with the PAs [8, 30, 31]. Drain (or collector) efficiency η is defined as the ratio of RF output power (P_{out}) to DC input power (P_{dc}), or

$$\eta = \frac{P_{out}}{P_{dc}} \tag{2.3}$$

Assuming sinusoidal voltage and current, the RF output power is given by

$$P_{out} = v_{eff} i_{eff} = \frac{i_1 v_1}{2} = \frac{i_1^2 R_L}{2}, \tag{2.4}$$

where i_{eff} and v_{eff} are effective and i_1 and v_1 are the peak fundamental components of current and voltage respectively, and the DC input power is given by Equation (2.2).

Power added efficiency (PAE) takes into account the input power (P_{in}) by subtracting it from the output power:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out} - \frac{P_{out}}{G}}{P_{dc}} = \eta\left(1 - \frac{1}{G}\right), \tag{2.5}$$

where $G = P_{out}/P_{in}$ is the gain of the PA. The PAE will give a good indication of the performance of a PA for high amplifier gains but it can even become negative for low gains. This relationship is shown in Figure 2.2.

The third type of efficiency is overall efficiency, the ratio of output power to the sum of input power and DC input power:

$$OE = \frac{P_{out}}{P_{dc} + P_{in}} \tag{2.6}$$

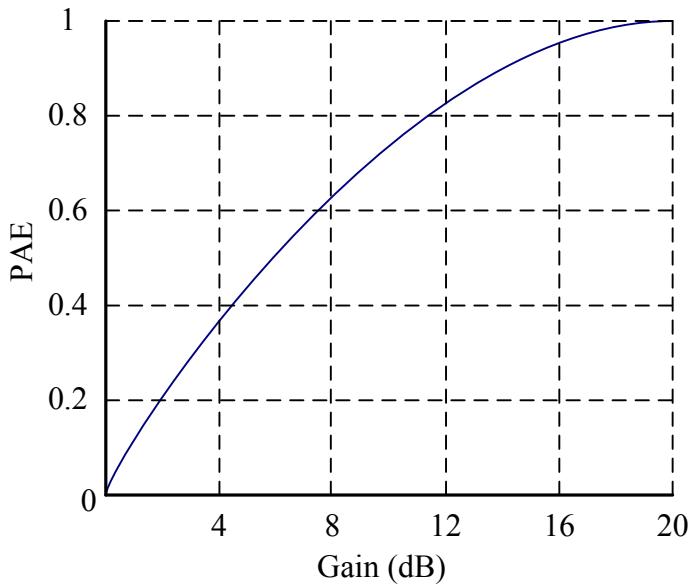


Figure 2.2. Normalized PAE versus the PA gain [1].

The above efficiencies are instantaneous quantities. The instantaneous efficiency is highest at the peak output power. Instead of instantaneous efficiencies, average efficiency can be used for the signals with time varying amplitudes:

$$\eta_{AVG} = \frac{\overline{P}_{out}}{\overline{P}_{dc}}, \tag{2.7}$$

where $\overline{P}_{out}$ is average output power and $\overline{P}_{dc}$ is average DC input power.

2.2.4 Matching for desired power

The maximum power transfer theorem, commonly used in RF electronics for optimal power transfer by means of conjugate matching, can only be used at the input side of a PA [1, 30], but it does not apply at the output side. At the input side, the PA has to be designed so that correct current and voltage waveforms are delivered at the gate or base of the transistor (biasing). At the output side load has to be correctly chosen. From Equation (2.1), it is obvious that the only two parameters influencing the output power are the voltage supply, V_{DD} or V_{CC} and the load impedance, R_L. The supply is normally fixed for a given application, so that the only degree of freedom left to the designer is the impedance of the load. Looking for correct impedance for maximum power output is called load pull. This impedance will often differ from standard impedances of 50 or 75 Ω.

Impedance matching networks are used to convert standard impedances to required impedances. At microwave frequencies, where wavelengths are correspondingly small, this matching can be accomplished with microstrip lines [33]. At low gigahertz frequencies, the microstrip lines are impractically long to be used on a chip, so that impedance matching using discrete components is employed. The two-component networks (L networks) and three-component networks (T and Π networks) are commonly used. Eight L-network configurations are possible, as shown in Figure 2.3 (a) and (b), where X_1 and X_2 can be any combination of inductors and capacitors, Z_S is the source impedance and Z_L is the load impedance. Such an L network is a broadband (high-pass or low-pass) network. Conversely, the T and Π networks with passives X_1, X_2 and X_3, shown in Figure 2.4 (a) and (b), are narrowband networks.

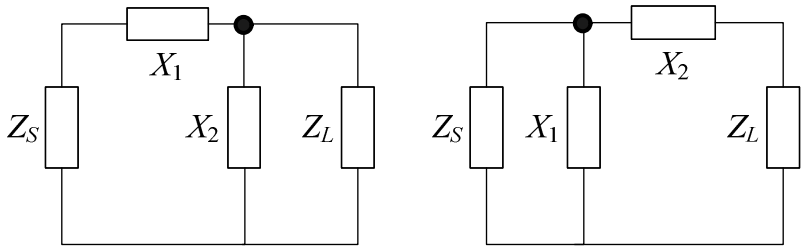


Figure 2.3. Two-component matching networks where passive component is parallel to (a) load and (b) source [33].

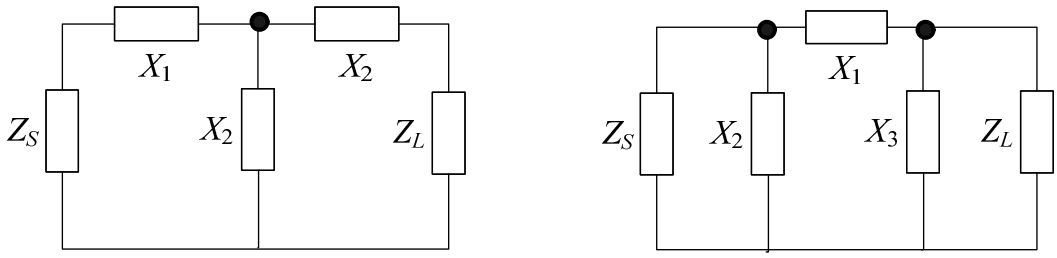


Figure 2.4. Three component matching networks: (a) T network and (b) Π network [33].

2.2.5 Classification of PAs

PAs can be divided into several categories. They are commonly grouped into broadband and narrowband amplifiers. Alternatively, they can be grouped depending on whether they are intended for the linear or constant envelope operation [30]. However, the most common grouping of PAs is grouping into classes according to the nature of their voltage and current waveforms. The variety of PA classes reflects the inability of any single circuit to satisfy stringent requirements for linearity, power gain, output power and efficiency.

Each class is designated with a letter or a combination of letters of the alphabet. The following classes are commonly used for different applications: A, B, AB, C, D, DE, E, F, FE, G, H and S [1, 8, 34]. Inverse classes, where the shape of voltage and current waveforms across the power transistors are inverted, are also possible. Common examples are inverse Class-C (C^{-1}) and inverse Class-F (F^{-1}) amplifiers [35]. Most of the real-life PAs are operating with current and voltage waveforms that lie between two different classes.

Not all of the classes are suitable for use at RF. For example, Class-D amplifiers are the switching-mode PAs generally used in low-frequency applications [36]. One such PA and its waveforms is shown in Figure 2.5 [37]. Ideally, only one of the two transistors in this figure is switched at a time and efficiency is 100% [31]. However, the use of this PA at high frequencies is limited due to prominent parasitic reactances that lead to substantial losses. This high-frequency performance degradation is less severe in current-mode Class-D implementations [36]. Class-S amplifiers are similar to those of Class D, but their input is driven with pulse-width modulated (PWM) waveform. This class needs transistors Q_1 and Q_2 to be switched with frequencies much higher than the signal frequency, thus making them impractical in RF range [1]. Class-G and Class-H amplifiers are also commonly used for audio applications, with some limited use in digital telephony and for code divison multiple access (CDMA) at low megahertz frequencies.

Traditionally, power amplification at RF was done with amplifier classes A through C, often termed classic amplifiers [8]. Class-E and Class-F amplifiers are considered modern amplifiers since they can be used in many hi-end applications. Because of their importance, all these amplifiers will be presented in separate sections.

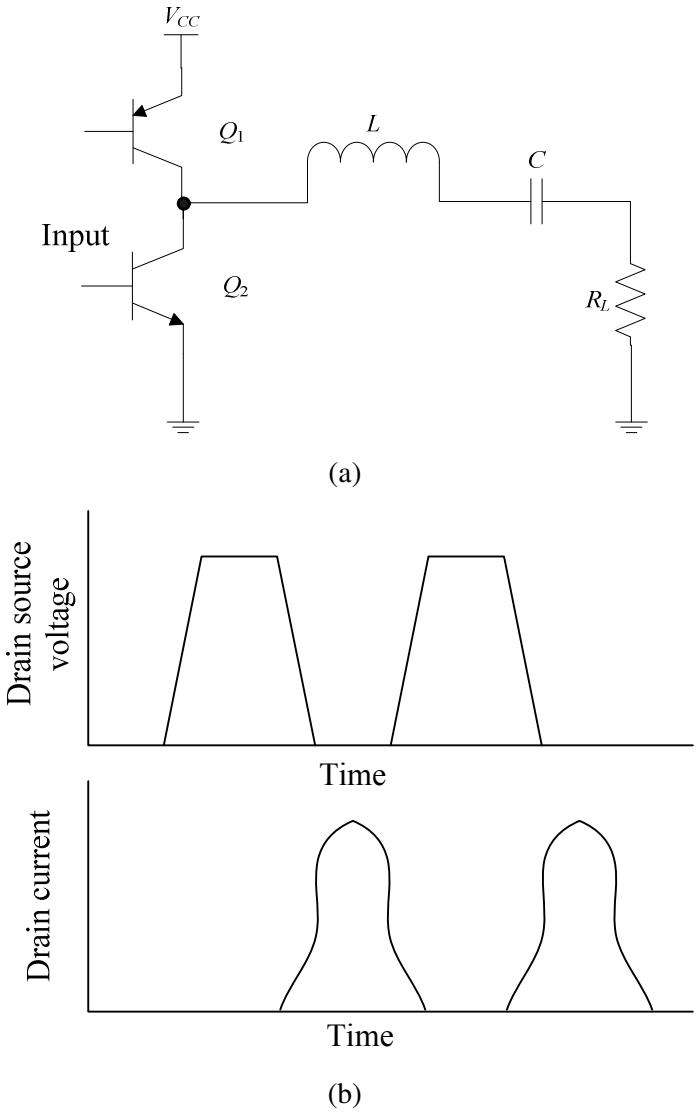


Figure 2.5. General Class-D amplifier: (a) circuit, (b) voltage and current waveforms.

2.2.5.1 Classes A through C

Class-A, B, AB and C amplifiers, or classic amplifiers, are usually analyzed together because of the minimal differences in their waveforms. Figure 2.6 shows a circuit operating as either Class-A, Class-AB, Class-B or Class-C amplifier [8]. Depending on the biasing, the fraction of the cycle during which the current through the PA is flowing (defined as conduction angle or 2θ) is different resulting in different class operation, as analyzed in Table 2.1, with efficiency to be explained later in this section. The voltage (v_c) and current (i_c) waveforms marked in Figure 2.6 are shown in Figure 2.7 for each class. In this figure, current i_c is sinusoidal waveform in all cases, with its bottom part cut off by biasing (V_b) for classes B and C. The waveform for the Class-AB amplifier, shaped between the Class-A and B waveforms, is not shown in this figure.

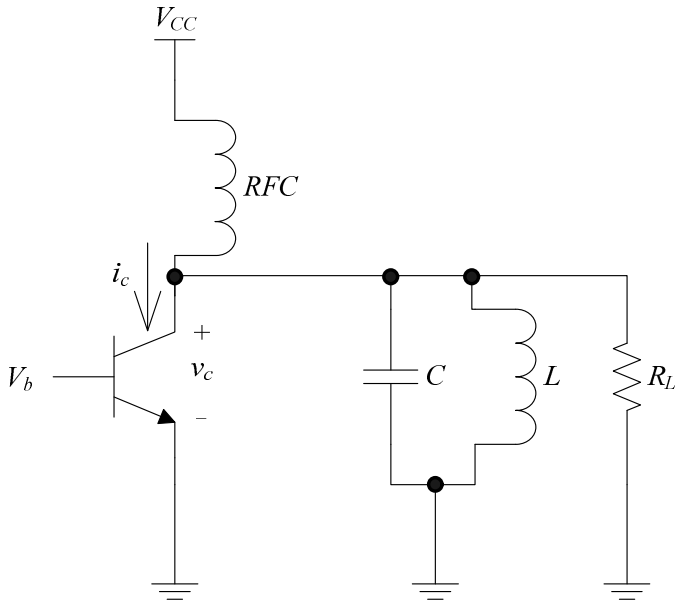


Figure 2.6. Circuit schematic of a single ended Class-A, AB, B or C PA used for theoretical analysis [8].

Table 2.1. Comparison of conduction angles and efficiencies for Class-A through C PAs [1].

Class	Conduction angle (°)	Maximum theoretical efficiency (%)	Normalized output power
A	360	50	1
AB	360 – 180	50 – 78.5	1
B	180	78.5	1
C	180 – 0	78.5 – 100	1 – 0

Classic PAs can be analyzed for efficiency as follows [1]. The DC component of the current, I_{DC}, can be derived as

$$I_{DC} = \frac{I_{CC}}{\pi}(\sin\theta - \theta\cos\theta), \tag{2.8}$$

where θ is a half of the conduction angle and I_{CC} is the peak of the current waveform across the transistor if it was operating in the Class-A mode (Figure 2.7 (b)). Power from the power supply is given by

$$P_{dc} = V_{CC} I_{DC} = \frac{V_{CC} I_{CC}}{\pi}(\sin\theta - \theta\cos\theta) \tag{2.9}$$

Fundamental current i_1 is derived as

$$i_1 = \frac{I_{CC}}{2\pi}(2\theta - \sin 2\theta) \tag{2.10}$$

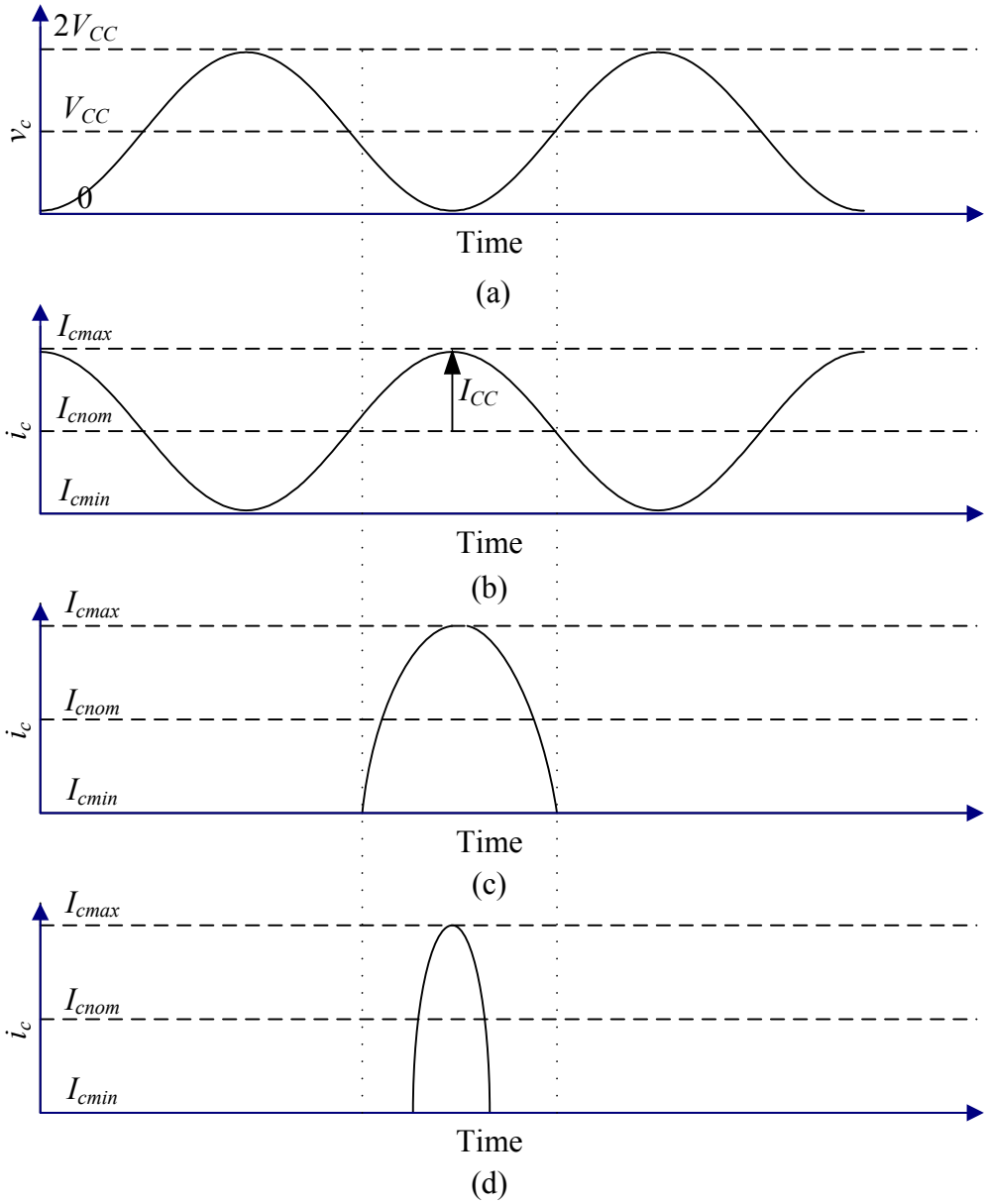


Figure 2.7. Voltage and current waveforms for classic amplifiers: (a) voltage for classes A, B and C, (b) current for Class A, (b) current for Class B and (c) current for Class C [8].

Output power is

$$P_{out} = \frac{v_{peak} i_{peak}}{2} \tag{2.11}$$

Maximum power will be reached if $v_{peak} = V_{CC}$. Hence (assuming $V_{CEsat} = 0$),

$$P_{out,\max} = \frac{V_{CC} i_{peak}}{2} = \frac{V_{CC} I_{CC}}{4\pi}(2\theta - \sin 2\theta) \tag{2.12}$$

The maximum possible efficiency is then

$$\eta = \frac{P_{out,\max}}{P_{DC}} = \frac{2\theta - \sin 2\theta}{4(\sin\theta - \theta\cos 2\theta)} \tag{2.13}$$

Figure 2.8 shows the plot of maximum normalized output power versus θ. Maximum possible efficiencies and regions of operation are also marked on the figure. From this figure, it is clear that maximum efficiency of 100% can be obtained with the Class-C operation, but with zero output power, which makes such configuration impractical. Usually, the compromise between efficiency and output power is considered optimum design solution, resulting in θ lying in 30 to 60 degrees range. It should be noted that linearity of this amplifier is highest with the Class-A operation, while it decreases for the Class-AB, B and C operation. The passives *C* and *L* in Figure 2.6 are not explicitly defined by the PA formulae as in the case of the Class-E amplifiers described in Section 2.2.5.2, but they must be chosen for the amplifier to operate at correct resonant frequency given by

$$f_o = \frac{1}{2\pi\sqrt{LC}}, \tag{2.14}$$

with acceptable Q-factor

$$Q = \frac{2\pi fL}{R_L} \tag{2.15}$$

Efficiencies for monolithic Class-A through C PAs are much lower than ideal values due to a number of factors: low quality factor of inductors, saturation voltage in the transistors, tuning errors and temperature variations. Because high efficiencies are possible only at low conduction angles which are difficult in ICs, fully integrated classic PAs are rare, but not impossible. One example is a Class-AB amplifier for Bluetooth applications [38].

2.2.5.2 Class E

Class-E amplifiers were proposed by Sokal and Sokal in 1975 [39] and together with the Class F amplifiers [40] have been used in communication ever since. They are classified as switching amplifiers and as such they can exhibit efficiencies close to 100%. A single ended Class-E PA is shown in Figure 2.9 [37]. A simple PA analysis can be performed if the following is assumed:

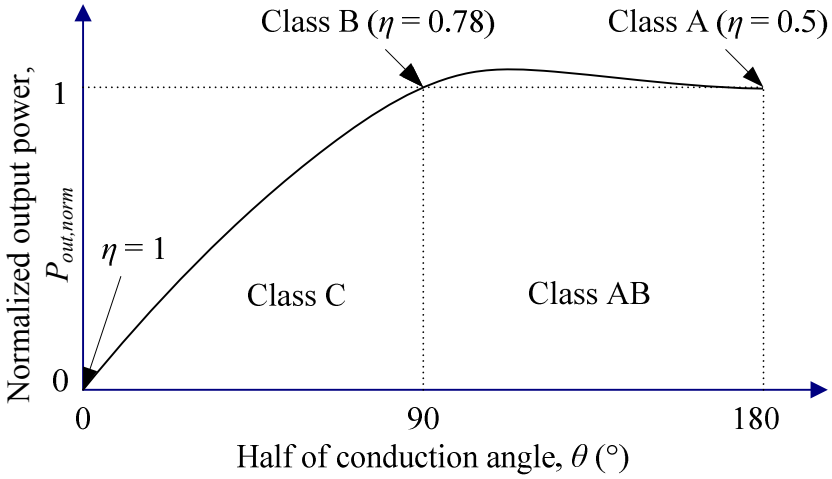


Figure 2.8. Maximum normalized output power versus half of conduction angle for the classic PAs [1].

- Inductance of the RF choke (L_1) is very high;
- Output capacitance of the transistor is independent of the switching voltage;
- Transistor is an ideal switch with zero resistance and zero switching time, open for half of the signal period.

From [39], the value of the optimum load resistance to deliver the highest power to the load with $v_{peak} = V_{CC}$ and non-zero V_{CEsat} is

$$R_L = \frac{2}{\frac{\pi^2}{4}+1}\frac{(V_{CC}-V_{CEsat})^2}{P} = 0.577\frac{(V_{CC}-V_{CEsat})^2}{P} \tag{2.16}$$

For desired Q-factor of the output resonant tank, inductance L_2 can be calculated:

$$L_2 = \frac{Q_L R_L}{2\pi f} \tag{2.17}$$

Shunt capacitance C_1 is given by

$$C_1 = \frac{1}{2\pi f R_L\left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right)} = \frac{1}{5.447(2\pi f R_L)} \tag{2.18}$$

and resonant capacitance C_2 is given by

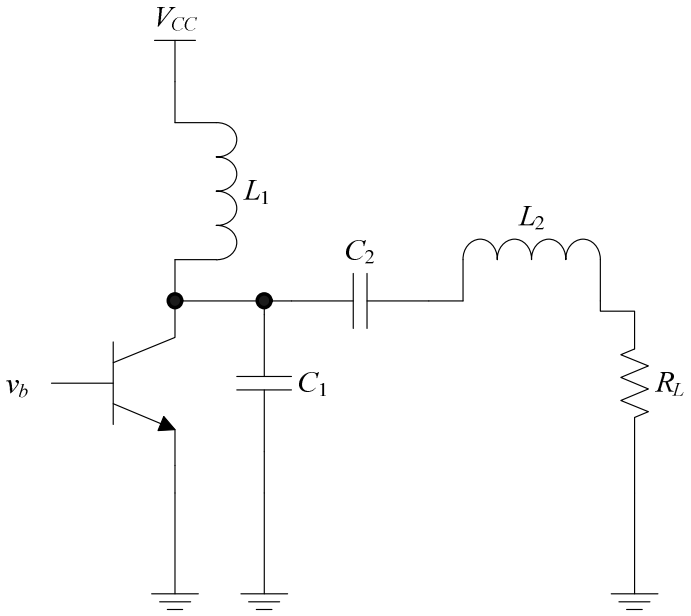


Figure 2.9. Circuit diagram of a single ended Class-E PA used for theoretical analysis [37].

$$C_2 = \frac{1}{(2\pi f)^2 L_2}\cdot\left(1+\frac{1.42}{Q_L-2.08}\right) = C_1\left(\frac{5.447}{Q_L}\right)\cdot\left(1+\frac{1.42}{Q_L-2.08}\right) \tag{2.19}$$

Capacitance C_1 includes parasitic capacitances of the transistor.

Efficiency of Class E is

$$\eta = \frac{1-\frac{(2\pi A)^2}{6}-\frac{V_{CEsat}}{V_{CC}}\left[1+A-\frac{(2\pi A)^2}{6}\right]}{1-\frac{(2\pi A)^2}{12}}, \tag{2.20}$$

where

$$A = \left(1+\frac{0.82}{Q_L}\right)ft_f \tag{2.21}$$

and t_f is the collector current fall time. For the ideal PA t_f and V_{CEsat} are zero, and efficiency is 100%. This efficiency is obtained at 78.5% of the Class-AB output power [1]. Practical waveforms for this topology with transistor turned on and off are shown in Figure 2.10.

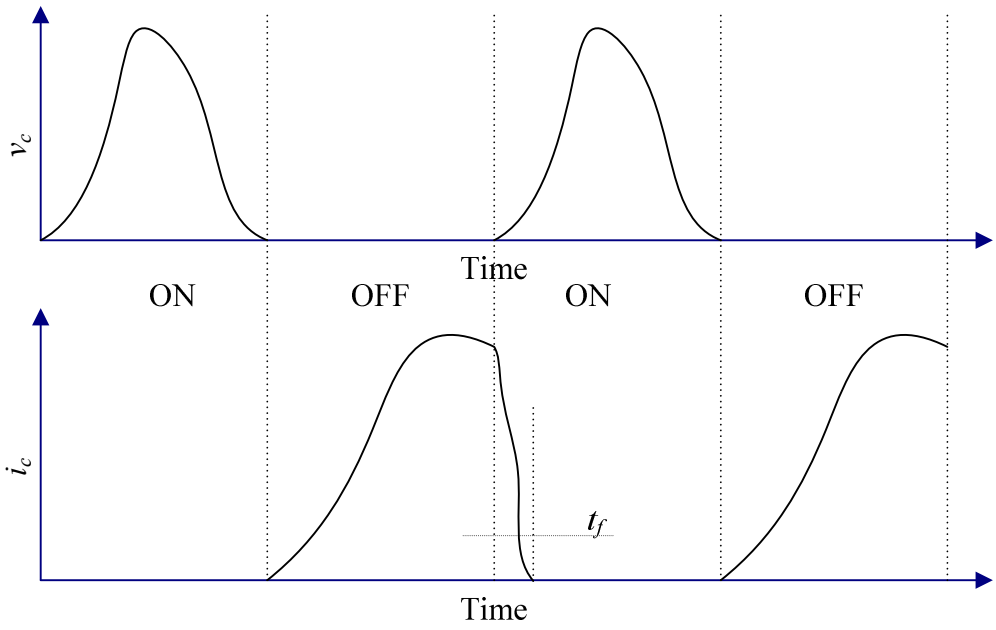


Figure 2.10. Voltage and current waveforms for the Class-E amplifiers when transistor is ON and OFF [39].

Although the Class-E amplifiers have output powers typically a few dB less than their Class-AB counterparts, they are used because of their high efficiency and swing that is more than three times the supply voltage. A recent example of the Class-E amplifier design can be found in [41].

2.2.5.3 Class F and F^{-1}

The Class-F amplifier is similar to that of the Class E in a sense that it can also result in 100% efficiency. However, at the same time, the output power can be similar to that of the Class-AB amplifiers [42]. This efficiency and power boost is a result of the presence of harmonic resonators in the output networks that shape drain (collector) waveforms in such a way that load appears to be short at even harmonics and open at odd harmonics, as shown in the general model in Figure 2.11. As a result, the ideal collector voltage waveform approximates a square wave, while collector current waveform approximates a half-sine wave. There is no overlap between the two waveforms. In case of the Class-F^{-1} amplifier resonators are swapped around, and the collector voltage is shaped as a half-sinusoid and collector current is shaped as a square wave.

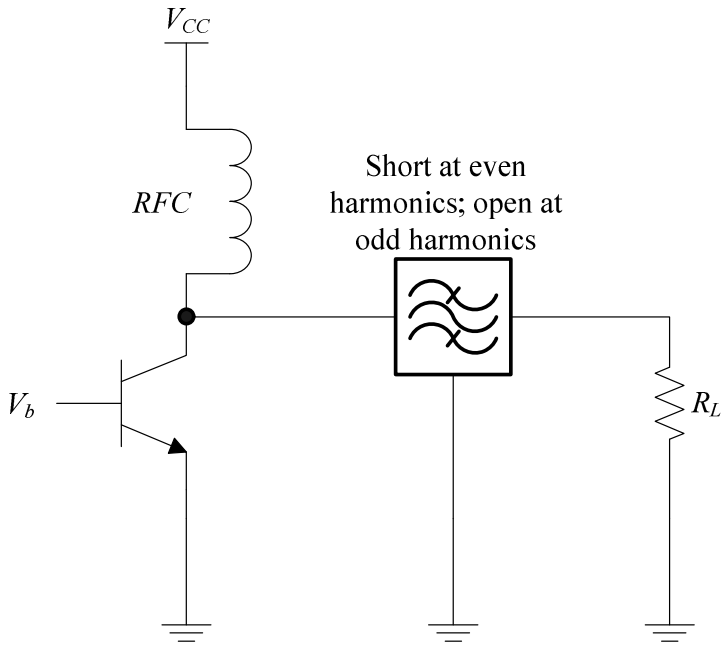


Figure 2.11. General Class-F amplifier model [42].

Shaping of waveforms can be done by means of transmission lines, as the case is with the Class-F amplifier with the quarter-wave transmission line. However, this is not a practical implementation for the low-gigahertz integration. Instead, passive resonators are used. Monolithic implementations of the Class-F amplifiers would require an infinite number of resonators to correctly shape output waveforms. Figure 2.12 shows efficiencies that can be obtained with increasing number of harmonic traps [43]. If only first harmonic trap is implemented, amplifier behaves as a Class-A amplifier, with maximum efficiency of 50%.

Most real life integrated Class-F amplifier implementations consider only a few harmonics, usually two or three. Figure 2.13 shows the third harmonic peaking circuit [42]. In this circuit, the tank at $3f_o$ provides an open circuit at $3f_o$ and short circuit at $2f_o$. A resonant tank at f_o ensures optimum load at f_o.

If fundamental frequency components of voltage and current are V_{om} and I_{om}, waveform factors that relate them to the fundamental frequency components V_{CC} and I_{DC} can be defined as [42]

$$V_{om} = \gamma_V V_{CC} \tag{2.22}$$

and

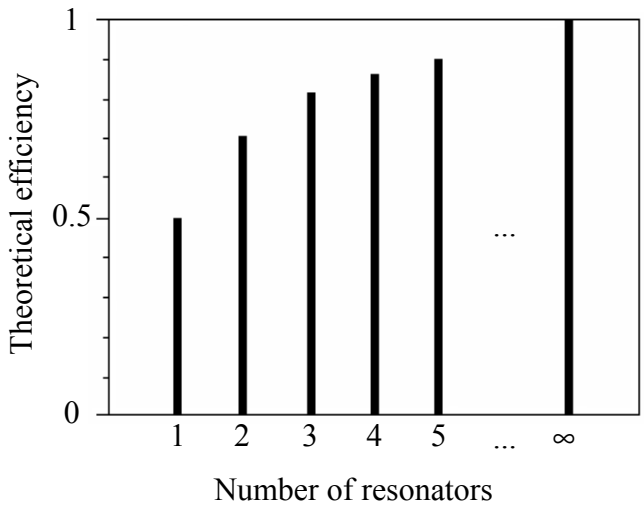


Figure 2.12. Efficiency of a Class-F amplifier versus a number of resonators [43].

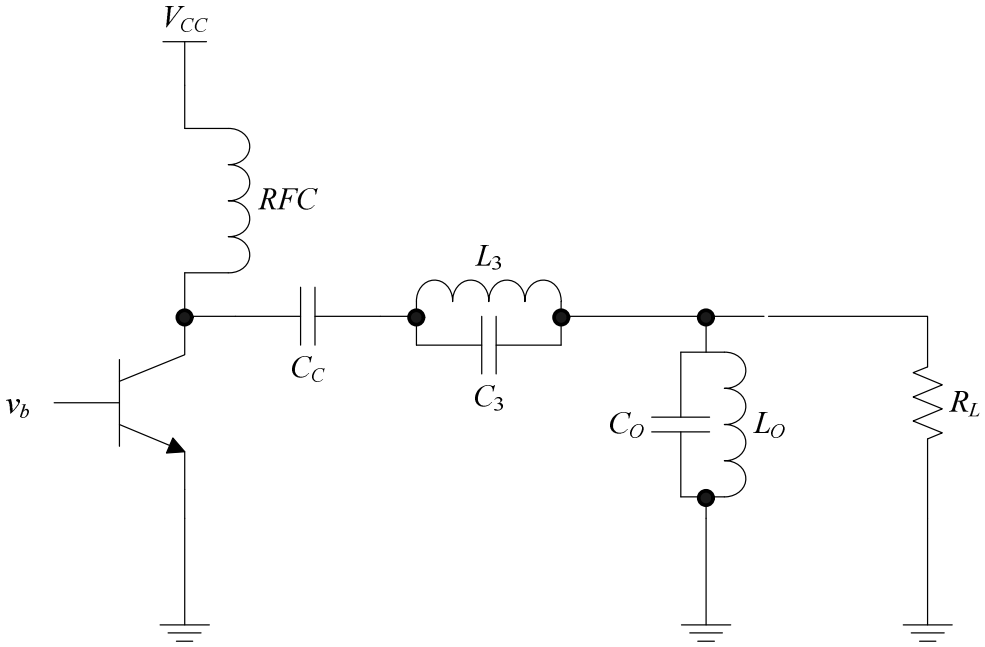


Figure 2.13. Class-F third harmonic peaking circuit [43].

$$I_{om} = \gamma_I I_{DC}, \tag{2.23}$$

whilst the efficiency of a Class-F circuit is

$$\eta = \frac{\gamma_V \gamma_I}{2} \tag{2.24}$$

For the third harmonic peaking circuit, γ_V and γ_I are calculated in [43] for the highest possible efficiency as 1.1574 and 1.4142 respectively, resulting in an efficiency of $\eta = 81.65\%$.

As it is the case with other classes, the Class-F amplifiers also exhibit efficiencies lower than predicted, mostly because of the presence of a large number of resonant circuits that suffer a loss because of the low Q-factors possible for on-chip inductors. A recent monolithic Class-AB/Class-F implementation in the InGaP/GaAs HBT process can be found in [44].

2.2.6 Techniques for performance improvement of PAs

Quality of the PA output is usually improved by various linearization techniques [45-47]. These include feedback, feedforward, pre- and postdistortion outphasing, as well as PWM and supply modulation. Efficiency can be boosted by means of adaptive bias and Doherty techniques [48]. Power combining is usually used to increase the total output power of a PA system. This can be performed on- and off-chip [1]. A good example of a high power amplifier that employs power combining can be found in [49]. The circuit uses distributed active transformer (DAT) architecture to deliver 35 dBm of power from an IC fabricated in 130 nm CMOS technology. Further two power combining transformer configurations are described in [50].

2.2.7 Temperature aspects of PAs

Efficiency, discussed in Section 2.2.3, is the ability of the PA to convert the electrical energy into output power. Excess power is converted to heat, which can limit the performance of an amplifier [51]. With increased efficiency, the amount of heat generated decreases. However, even with high efficiency, high output power configurations such as DAT architecture [49] will dissipate significant amounts of heat. The amount of heat generated and the way in which that heat is dissipated in a PA system depends on the technology in which the IC is fabricated and on the type of the active device (transistor) used for power amplification.

As detailed later in Section 2.4, SiGe technology is better choice than the rival GaAs technology from perspective of heating because the high conductive silicon substrate [52] facilitates heat distribution around the chip.

MOS transistor is less prone to heating than a BJT (HBT) because of its negative temperature coefficient [53]. This negative coefficient causes the drain current of the

MOSFET to decrease with temperature, which allows multiple MOSFETs to be connected in parallel. In HBTs, the situation is reversed. If multiple emitter fingers are used and are not perfectly balanced, the emitter with higher current will tend to take up even higher proportion of current, which gives rise to local hot spots and possibly permanent device damage [51]. Because current is flowing only in a small hot region, the total gain of the device decreases [54]. Normally, to compensate for this current gain decrease, ballast resistors are added in series with the emitter or base electrodes. This acts as negative feedback, since with the increase in current, the voltage across ballast resistors will also increase, counter-effecting the current increase. Including ballasting resistors, however, decreases the output power, power gain and the efficiency of the amplifier.

Typically, if heating poses a problem, the excess heat can be removed by means of heat sinks. The ground bondings should be adopted to favour heat sinks [55]. Usually, the chip is glued to a gold- or nickel-plated copper heat sink using a conductive adhesive [56].

2.2.8 Biasing

In preceding sections, it has always been assumed that the correct drive level is applied at the input of the PA. Input impedance matching, described in Section 2.2.4, is used to ensure that correct amplitudes of AC signals appear at input. Biasing, described in this section, provides the appropriate quiescent point for the PA [33].

Biasing point should remain constant irrespective of transistor parameter variations or temperature fluctuations. Active and passive biasing networks are possible. Figure 2.14 shows two passive biasing networks commonly used with BJT PAs.

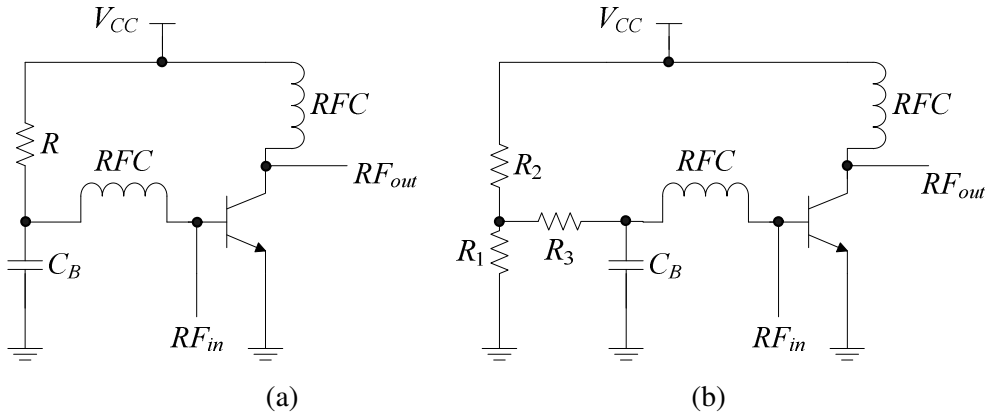


Figure 2.14. Passive biasing networks for a BJT PA: (a) One-resistor configuration, (b) Three-resistor configuration [33].

2.3 INDUCTORS FOR POWER AMPLIFIER IMPLEMENTATIONS

The demand for low-cost ICs has generated a high interest in integrated passive components. Passive components include resistors, capacitors and inductors.

A real inductor is usually modelled as an ideal inductor L_S in series with a resistor R_S, both in parallel with capacitor C_S, as shown in Figure 2.15 [33]. Inclusion of the series resistor and parallel capacitor is necessary to model the losses of the inductor even at frequencies below RF because Q-factor is in general much lower for the inductor then for other passive components. The Q-factor of the inductor is defined as 2π times the ratio of energy stored in the device and energy lost in one oscillation cycle. If Z is defined as impedance of an inductor, then the Q-factor is given by equation

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \tag{2.25}$$

For the simple circuit in Figure 2.15, Equation (2.25) reduces to

$$Q = \frac{X}{R_S}, \tag{2.26}$$

where X is total reactance of the inductor. Q-factor is heavily dependent on frequency and exhibits a peak Q_{max}.

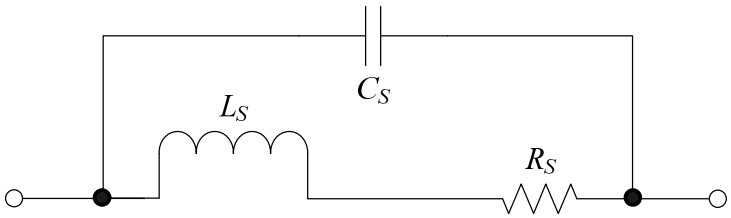


Figure 2.15. General high frequency model of an inductor [33].

While an ideal inductor exhibits constant impedance value for all frequencies, every non-ideal inductor exhibits impedance value dependent on frequency, as shown in Figure 2.16. Frequency where magnitude of impedance (|Z|) peaks is called the resonant frequency of an inductor. The resonant frequency, $f_r = \frac{1}{2\pi\sqrt{L_S C_S}}$ should ideally peak at infinity, but the finite value of the peak is due to the resistance R_S. Similarly, capacitance

C_S is the reason the inductor exhibits capacitive instead of inductive behaviour at frequencies above the resonance.

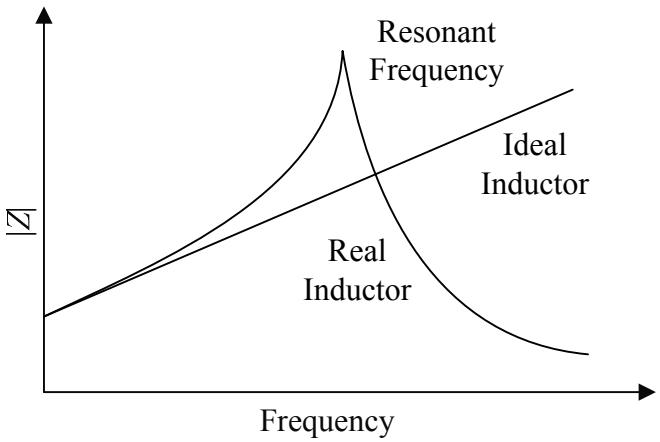


Figure 2.16. Frequency response of the impedance of ideal and real inductors [33].

2.3.1 Inductor implementation options

Traditionally, capacitor and resistor implementations are easily accomplished in CMOS and BiCMOS and are almost exclusively fabricated on-chip. In case of inductors, integrated passive (spiral) inductors are not such an obvious choice. Various factors, such as inductor size and low Q-factor of integrated passive inductors often result in one of the following inductor alternative implementations:

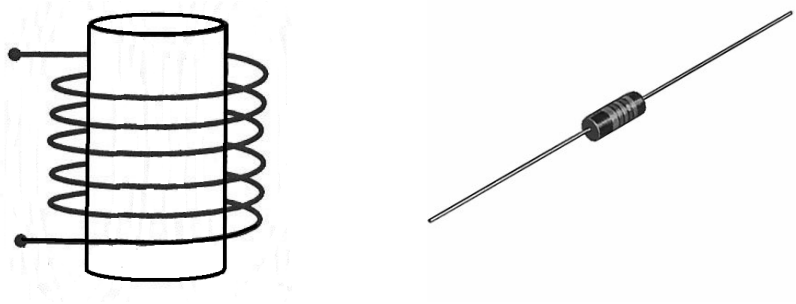
- External inductors,
- Active integrated inductors,
- Microelectro-mechanical systems (MEMS) inductors,
- Bond wires, or
- Other on-chip implementations.

Each of the above possibilities is considered as an alternative to the passive inductor implementation presented in this thesis and is discussed in more detail in the subsections that follow.

2.3.1.1 External inductors

External or off-chip inductors are connected to a system outside of the IC package. They are usually implemented as a solenoidal coil or a toroid, with a structure and a photo of a solenoid shown in Figure 2.17 [9]. Their usage at high frequencies also implies careful printed circuit board (PCB) modelling and design. Although high quality inductors are

widely obtainable from suppliers [57], inductance values available are usually limited to standard values of 10 nH and higher. Frequency of the Q-factor peak (typically in range of hundreds) is also predefined and is usually located in either high megahertz or low gigahertz range. Another drawback for integrated design is that the value obtained in real-life will differ from the anticipated value due to parasitics involving PCB tracks, IC bonding, and others.



(a) (b)

Figure 2.17. A solenoidal off-chip inductor: (a) structure, (b) photo [9].

2.3.1.2 Active integrated inductors

Active inductors are a good alternative to integrated passive inductors because of their higher Q-factor. Typical Q-factors that can be obtained for this configuration are between 10 and 100, which is up to ten times that of spiral inductors [58]. Active inductors also take up much smaller area on the chip than spiral inductors. The main disadvantages of active inductors are increased power consumption, presence of electrical noise from active devices and limited dynamic range. A design requiring only six transistors has been proposed [59], which makes active inductor much more compact compared to traditional designs requiring ten transistors or more. Active die area of this topology is only 30 µm by 65 µm, and it achieves a Q-factor of about 20 at 1 GHz whilst exhibiting differential inductance of 20 nH.

Many active inductors employ a gyrator approach [60]. An ideal gyrator is a linear two-port network that neither absorbs nor dissipates energy. Linearized model of an ideal gyrator is shown in Figure 2.18.

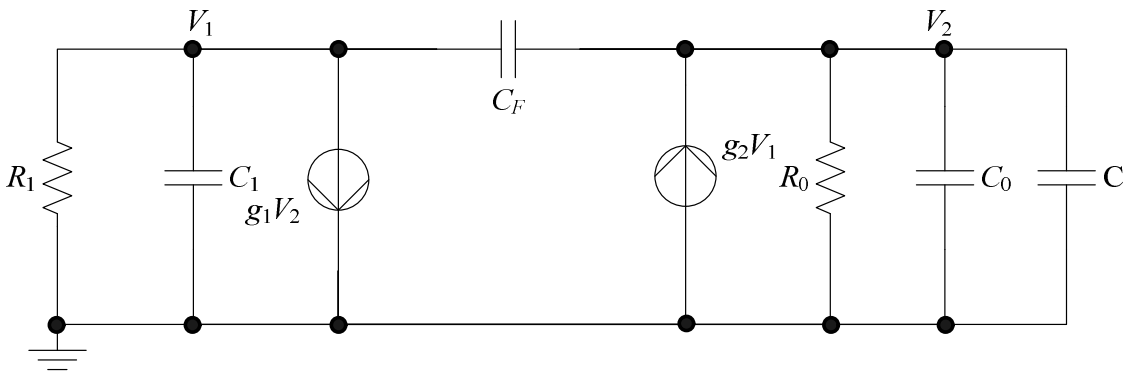


Figure 2.18. High frequency two-port equivalent model of an active inductor [60].

At low frequencies the effective inductance and series resistance can be accurately modelled in terms of capacitances (C_1, C_0 and C), output resistance (R_0) and transconductances (g_1 and g_2) represented in Figure 2.18. At higher frequencies, the parasitics become more prominent and the linearized model cannot be used any longer. In this case, the analysis of active inductors becomes specific to a given configuration. Real-life examples of active inductor implementations are included in references [58] and [59].

2.3.1.3 MEMS inductors

MEMS is an IC fabrication technique that empowers conventional two-dimensional (2-D) circuits to expand into the third dimension (3-D) [61]. This principle becomes particularly useful in inductor fabrication, because substrate parasitics can be reduced significantly. In later sections of this chapter it will be discussed that substrate losses are the main contributor to the low Q-factor of integrated passive inductors. A number of techniques for producing MEMS devices exist, of which bulk and surface micromachining are most commonly used for inductors. In bulk micromachining, a 3-D structure is created on the wafer by etching different atomic crystallographic planes in the wafer. In surface micromachining, the 3-D structure is created by the sequential addition and removal of thin film structural and sacrificial layers to and from the wafer while preserving the integrity of structural layers [61]. Effectively, silicon below the inductor is replaced by air which has the lowest possible relative permittivity (ε_r = 1), which allows the Q-factor and resonant frequency to approach the values of off-chip inductors. Typical obtainable Qs range from 10 to 30 for 1 nH inductors at multi-gigahertz frequencies.

An example of a high-Q micromachined inductor can be found in [62]. In this paper, a robust micromachined spiral inductor with a cross-shaped sandwich membrane support is

fabricated for RFIC applications. This inductor achieves a Q-factor of 50 for 4 nH inductor at 5 GHz. The photograph in Figure 2.19 illustrates the substrate removal at the corner of this robust inductor.

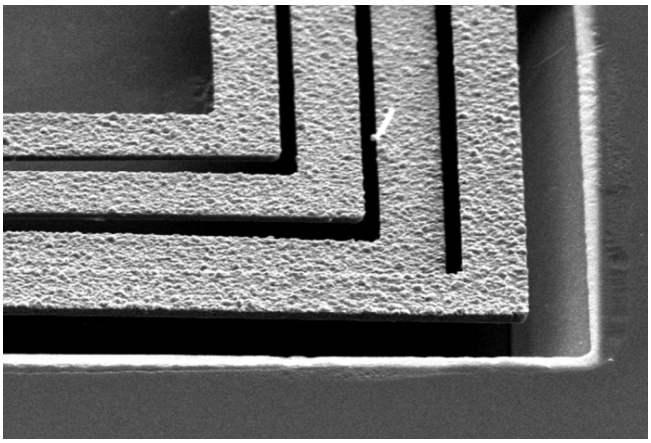


Figure 2.19. Photograph of the enlarged view of the corner region of the robust inductor illustrating removal of the substrate [62].

Alternative to spiral MEMS inductors, solenoidal inductors suspended on-chip can be used with various degrees of chip stability [63]. Several advantages over conventional (or MEMS) spiral inductors can be identified, which include a lower stray capacitance due to the fact that only a part of the inductor is lying on the silicon substrate, a simple design equation and greater possibilities for flexible layout. Advanced micromachining techniques for solenoidal inductors have been proposed, including the 3-D laser lithography, multiple-trenched sidewalls, the U-shaped solenoidal shape and a concave-suspending MEMS process.

The second alternative to the MEMS spiral inductors are out-of-plane inductors [64]. Coils are fabricated using stress-engineered thin films. Stress gradient is induced by changing the ambient pressure during film deposition. When released, a stress-graded film curls up in a circular trajectory as photographed in Figure 2.20 [64]. Typical Q-factor of this configuration is over 70 at 1 GHz.

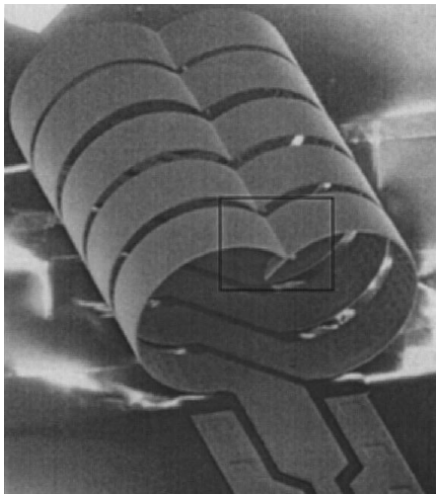


Figure 2.20. Out-of-plane inductor [64].

Although MEMS devices present an attractive alternative to conventional passive inductors, particularly because of the high Q-factors, the micromachining and suspending require modifications to standard fabrication procedures and/or modifications to the wafer after fabrication. Because after such modifications the repeatability [65], important for mass production of these devices, is not assured, MEMS will not be considered any further in this study.

2.3.1.4 Bond wires

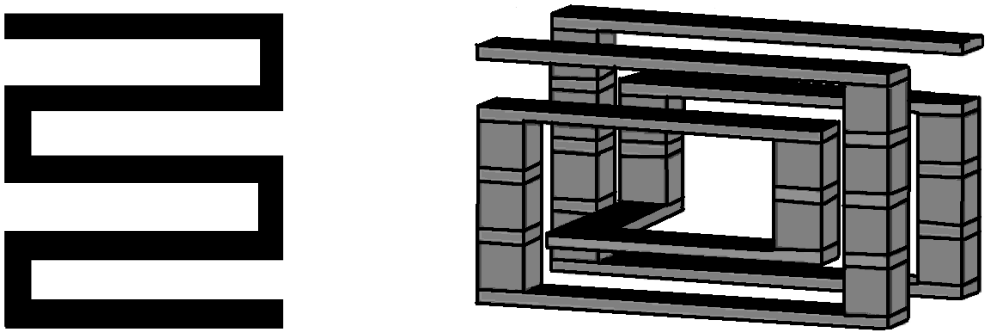
Bond wires, which usually present a parasitic quantity for signals communicating between systems on the packaged chip and the outside world, reflect inductive behaviour that impacts module performance [66]. Electrical characteristics of bond wires depend on the material of which they are made of and its cross-section, the height above the die-plane, horizontal length and the pitch between the adjacent wires [67]. These characteristics can be used accurately to determine the Q-factor and inductance of bond wires in order to use them in RF applications. Although bond wires with Q-factors of 50 have been reported, their inductances will typically be less than 1 nH [67]. This limits their usability in gigahertz range where well controlled inductances of 1 nH and more are often needed.

2.3.1.5 Other on-chip implementations

Other inductor implementations are worth mentioning in a separate section since some fundamental differences from standard inductor types can be identified.

Masu, Okada and Ito [68] discuss two types of inductors not commonly found in literature. First type of inductor is a meander inductor. It is a flat passive inductor consisting of a long piece of metal that is not wound as in the case of the spiral inductor which will be described in detail later, but meanders as shown in Figure 2.21 (a). This inductor occupies a small area, but its measured Q-factor is quite low (about 2.1 for inductance of 1.3 nH). Such trade-off between the area and Q-factor is acceptable for matching network applications. The second type of inductor is a snake inductor similar to the previously mentioned MEMS solenoidal inductor, but wound as shown in Figure 2.21 (b). It occupies even smaller area than the meander inductor and its Q-factor lies in the same range.

Vroubel *et al.* discusses electrically tuneable solenoidal on-chip inductors [69]. Other tuneable inductors are commonly seen as implemented in active configuration, such as in the case of the inductor in [70]. The toroid inductors can also be implemented on-chip by means of micromachining. One such integrated inductor is shown in Figure 2.22 [71].



(a) (b)

Figure 2.21. The meander (a) and snake (b) inductors [68].

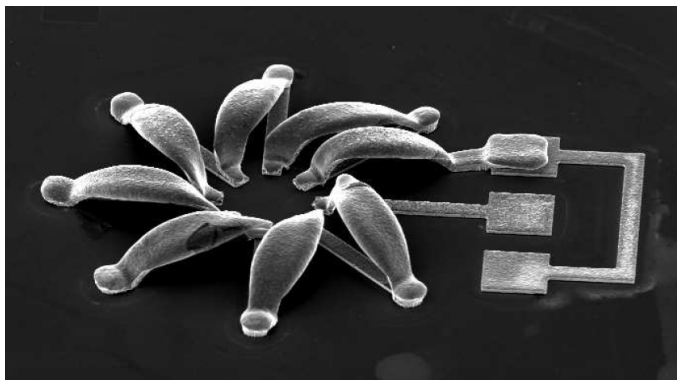


Figure 2.22. Photograph of an integrated toroid inductor [71].

2.3.2 Spiral inductors on silicon and SiGe

Although inductor implementations described in the previous section are widely used due to their advantages over passive integrated inductors, they are normally too complex to implement and make the PA devices too bulky and expensive. This leaves passive spiral inductors as a reasonable choice for PAs.

2.3.2.1 Common spiral inductor geometries

There are several spiral inductor geometries commonly used. These include square and circular inductors as well as various polygons [72]. The square spiral has traditionally been more popular since some IC processes constrain all angles to 90° [9], but it generally has lower Q-factor than the circular spiral, which most closely resembles the common off-chip solenoidal inductors but is difficult to lay out. A polygon spiral is a compromise between the two. Drawings of these geometries are shown in Figure 2.23.

The geometries shown in Figure 2.23 are asymmetric, and require only a single metal layer for fabrication. Additional layers are only needed to bring the signal lines to the outside of an inductor and are universally known as underpasses. Symmetrical inductors are also possible, but they require more than one underpass, in this case known as metal-level interchange. Such geometry is presented in Figure 2.24 [9].

The second metal layer can be used as part of the core of the inductors. An example of such multilayer geometry is a two-layer square inductor shown in Figure 2.25 [73]. The multi-layer geometries can deliver higher quality factors than a single layer inductor due to their more significant inductance coupling.

Another common geometry is a taper geometry, where inner spirals of inductors decrease in width in respect to the outer spirals [74] (Figure 2.26). Tapering is done to suppress eddy current losses in the inner turns in order to increase the Q-factor [74], but it is most effective when substrate losses are negligible [9].

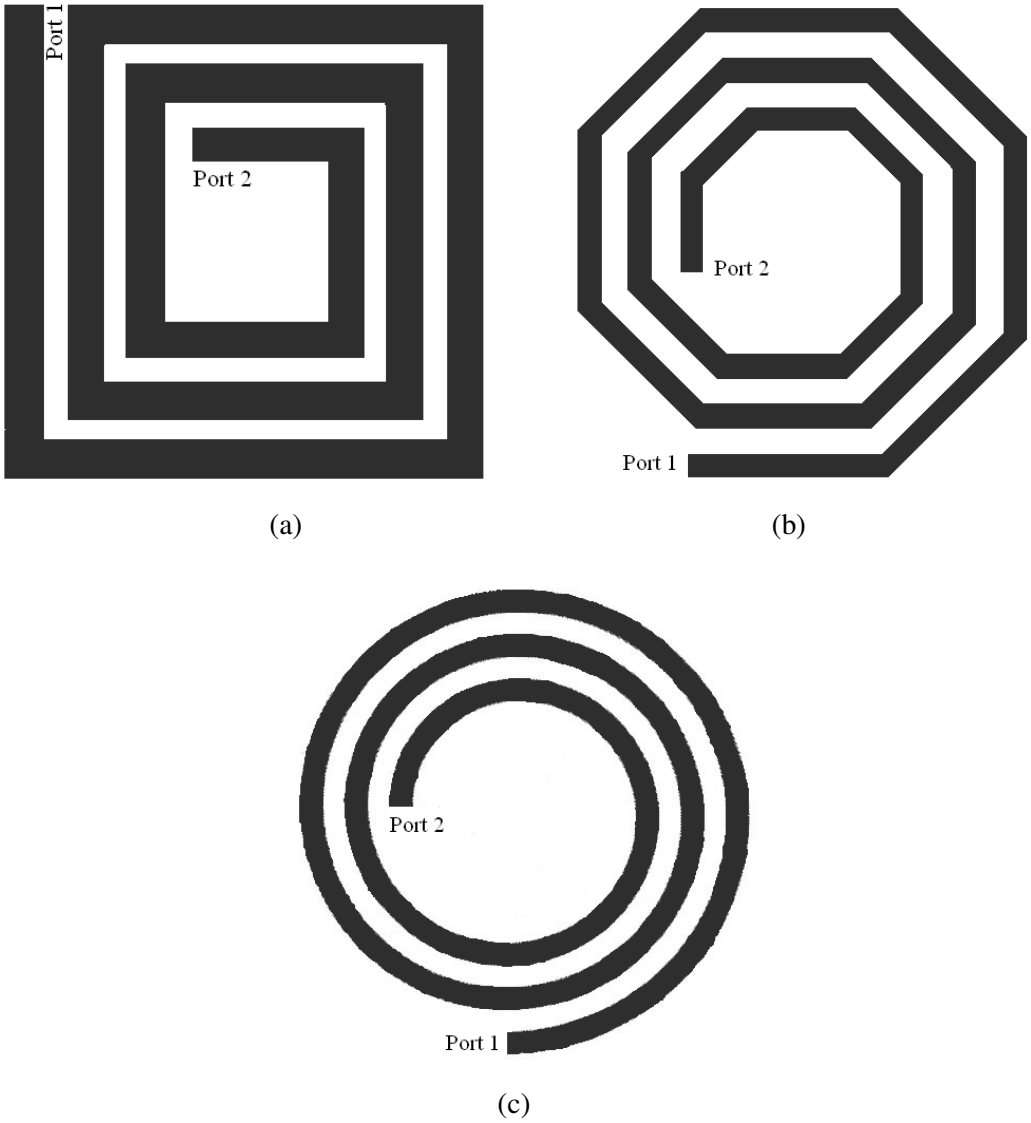


Figure 2.23. The square (a), polygonal (octagonal) (b) and circular (c) spiral inductors [9].

2.3.2.2 Spiral inductor geometry parameters

For a given geometry, a spiral inductor is fully specified by the number of turns (n), the turn width (w) and two of the following: inner, outer or average diameter (d_{in}, d_{out} or $d_{avg} = (d_{in} + d_{out})/2$), as shown in Figure 2.27 for the square and circular inductors. Spacing between turns, s, can be calculated from other geometry parameters. Another commonly used geometry parameter is the fill ratio, defined as

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{2.27}$$

Total length of a spiral is also important for calculations. It is dependent on inductor geometry. For a square inductor it can be calculated as

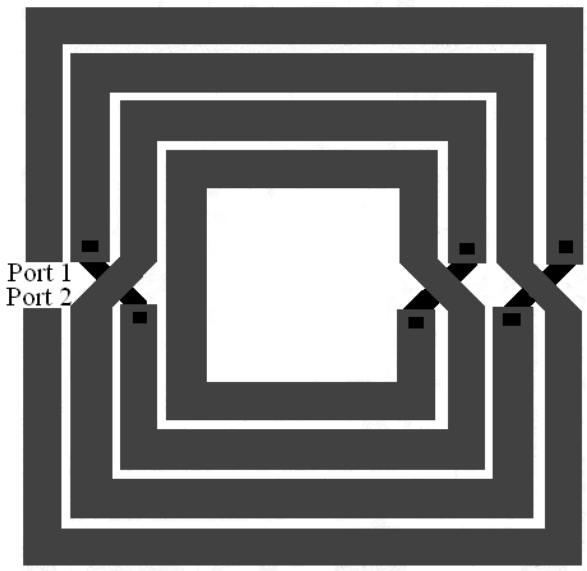


Figure 2.24. The symmetrical spiral inductor [9].

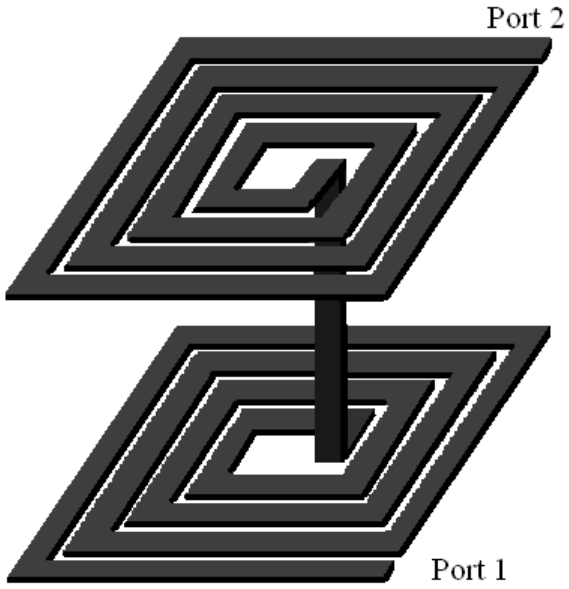


Figure 2.25. A multilayer (two-layer) spiral inductor [73].

$$l = 4(d_{in} + w) + 2n(2n-1)(s+w) \tag{2.28}$$

2.3.2.3 Spiral inductor models

Several spiral inductor models are widely used. In this section, a single-π, segmented, double-π and third-order models will be described.

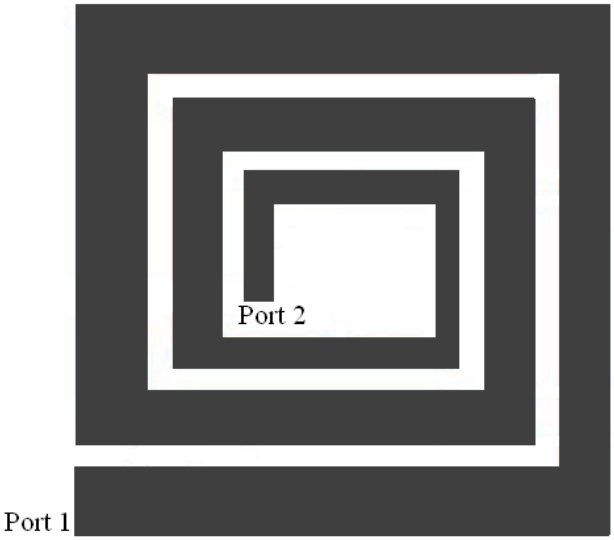
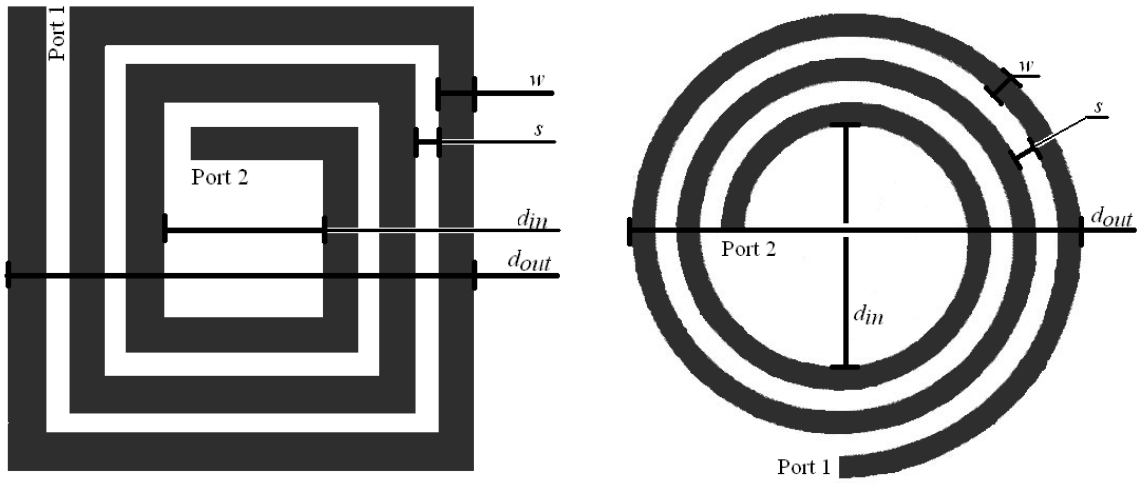


Figure 2.26. A taper spiral inductor [74].



(a) (b)

Figure 2.27. Geometry parameters of the (a) square and (b) circular spiral inductors.

Single-π model

Most commonly used model is a lumped single-π nine-component configuration shown in Figure 2.28 [10, 72]. In this model, L_S is the inductance at the given frequency, R_S is the parasitic resistance and C_S is the parasitic capacitance of the spiral inductor structure. C_{ox} is the parasitic capacitance due to oxide layers directly under the metal inductor spiral. Finally, C_{Si} and R_{Si} represent the parasitic resistance and capacitance due to the silicon substrate. This topology does not model the distributive capacitive effects, but it models correctly for parasitic effects of the metal spiral and the oxide below the spiral, as well as for substrate effects.

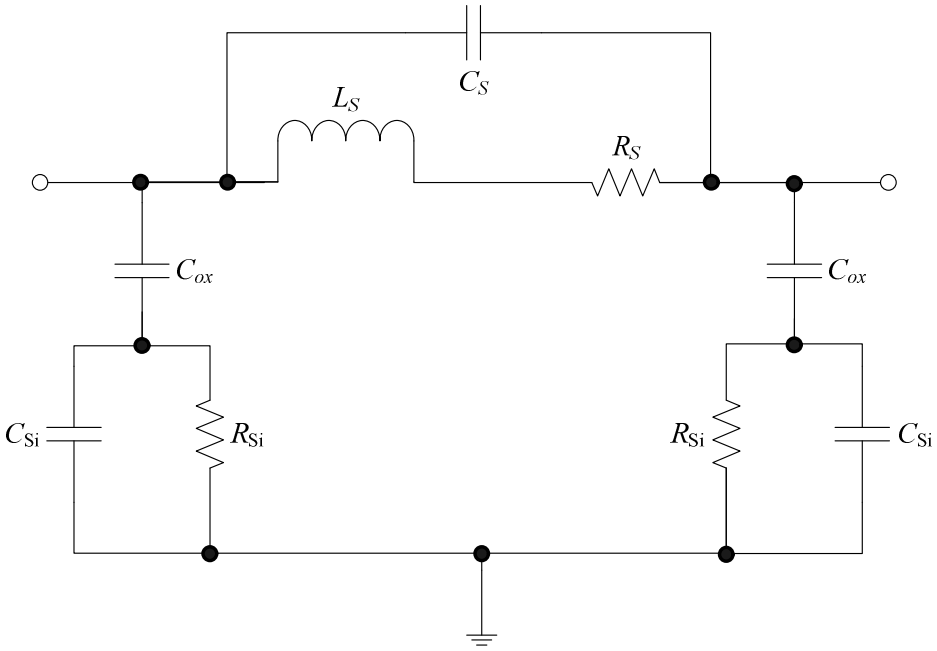


Figure 2.28. A commonly used nine-component spiral inductor model [72].

Segmented model

Somewhat more complicated model is the model presented in [75]. Each segment of the inductor is modelled separately with a circuit given in Figure 2.29. In this model, parasitics C_{ox}, C_{Si} and R_{Si} represent parasitics of only one inductor segment, L_S and R_S represent inductance and parasitic capacitance of one segment coupled to all segments, whilst capacitances C_{f1} and C_{f2} are added to represent coupling to adjacent segment nodes.

Double-π distributed model

The standard single-π model can also be extended into distributed double-π model shown in Figure 2.30 [11, 76]. A second order ladder (with third grounded branch) is used to model the distributive characteristics of metal windings. The interwinding capacitance (C_w) is included to model the capacitive effects between metal windings of the inductor. The transformer loops (M_{S1} and M_{S2}) represent the frequency-dependent series loss effects.

Third order transmission-line model

The second order model shown in Figure 2.30 is valid for the inductor up to the first resonance frequency. If a third order model is used, it is possible to accurately predict inductor behaviour even beyond the resonant frequency. One such model is presented in [12]. An equivalent circuit diagram for this configuration is given in Figure 2.31. Extrinsic admittances are used and all circuit components are self-explanatory from this figure.

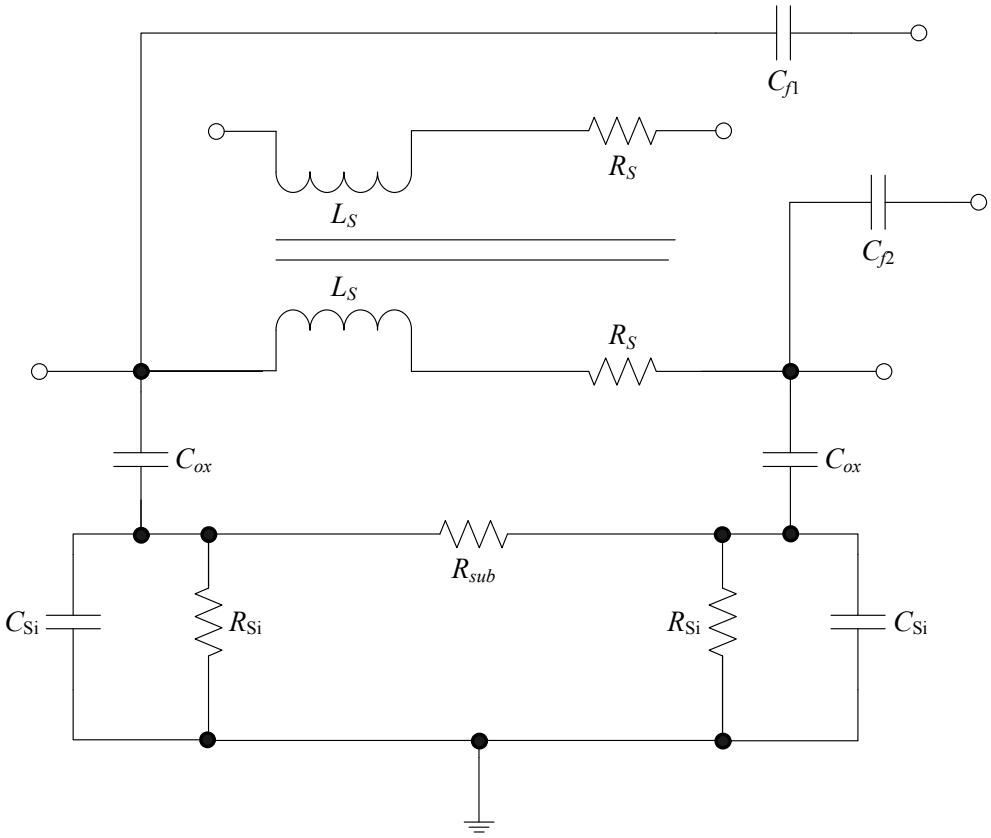


Figure 2.29. An equivalent two-port model for one segment of a spiral inductor [75].

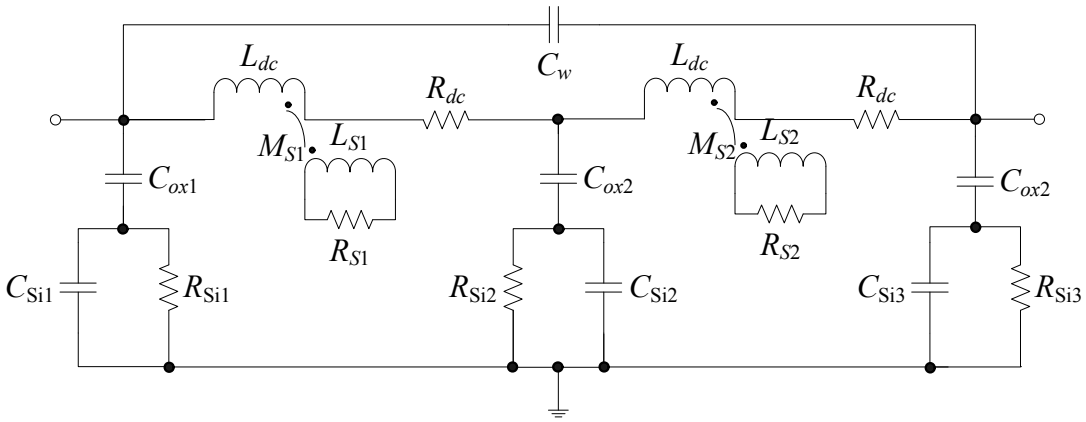


Figure 2.30. A double-π distributed inductor model [76].

2.3.2.4 Calculation of series inductance and parasitics for single-π inductor model

The single-π inductor model of Figure 2.28 is sufficient to accurately model spiral inductors for frequencies below resonance. In this section, series inductance L_S as well as parasitic capacitances and resistances shown in this figure are explained.

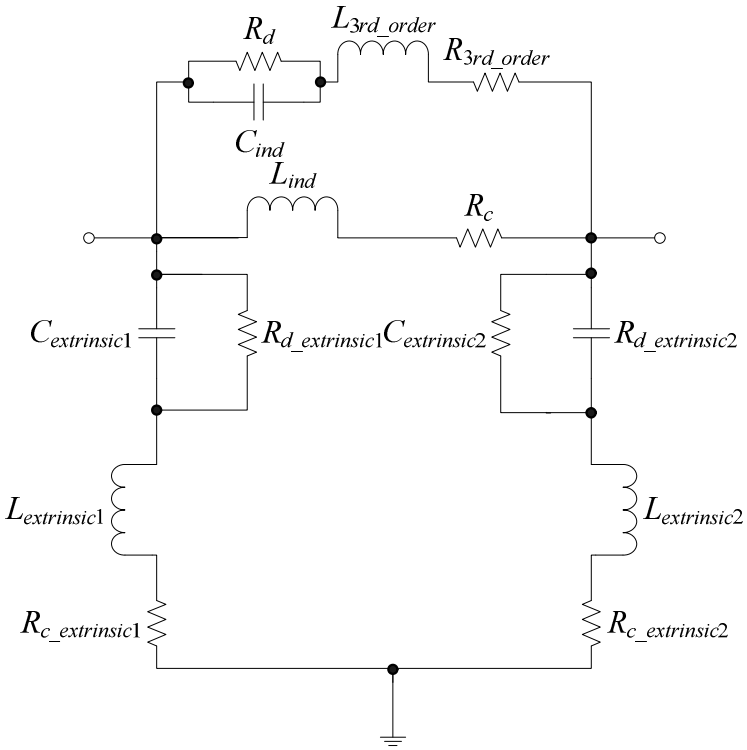


Figure 2.31. A complete third-order inductor model [12].

Series inductance (L_S)

Various equations are commonly used in literature to represent the series inductance of spiral inductors. These include the modified Wheeler equation, expression based on current sheet approximation [72], Bryan equation, as well as the data-fitted monomial expression [77].

The modified Wheeler equation is based on the equation derived by Wheeler in 1928 [72]:

$$L_{mw} = K_1 \mu \frac{n^2 d_{avg}}{1 + K_2 \rho}, \tag{2.29}$$

Here, n is the number of turns, d_{avg} is the average diameter of the spiral and ρ is the fill ratio, all defined in Section 2.3.2.2 . K_1 and K_2 are geometry-dependent coefficients with values defined in Table 2.2 and μ is magnetic permeability of the metal layer.

Table 2.2. Coefficients for the modified Wheeler expression [72].

Layout	K_1	K_2
Square	2.34	2.75
Octagonal	2.33	3.82
Hexagonal	2.25	3.55

Another expression can be obtained by approximating the sides of the spiral by symmetrical current sheets of equivalent current densities as described in [72]:

$$L_{gmd} = \mu \frac{n^2 d_{avg} c_1}{2} \left[\ln \frac{c_2}{\rho} + c_3 \rho + c_4 \rho^2 \right] \tag{2.30}$$

Here, c_1, c_2, c_3 and c_4 are geometry dependent coefficients with values defined in Table 2.3. This expression exhibits a maximum error of 8% for $s \leq 3w$.

Table 2.3. Coefficients for the current sheet expression [72].

Layout	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

Bryan's equation is another popular expression for the square spiral inductance [77]:

$$L = 0.00241 \left(\frac{d_{out} + d_{in}}{4} \right) n^{\frac{5}{3}} \ln \left(\frac{4}{\rho} \right) \tag{2.31}$$

The data-fitted monomial expression is an expression that results in an error smaller than seen in the expressions given above (typically less than 3%). It is based on a data-fitting technique. Inductance in nanohenries (nH) is calculated as [72, 77]:

$$L_{mon} = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}, \tag{2.32}$$

where coefficients β, α_1, α_2, α_3, α_4 and α_5 are once again geometry dependent, as presented in Table 2.4.

Table 2.4. Coefficients for the spiral inductor inductance calculation [72]

Layout	β	α_1 (d_{out})	α_2 (w)	α_3 (d_{avg})	α_4 (n)	α_5 (s)
Square	$1.62 \cdot 10^{-3}$	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	$1.28 \cdot 10^{-3}$	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	$1.33 \cdot 10^{-3}$	-1.21	-0.163	2.43	1.75	-0.049

The monomial expression has been developed by curve fitting over a family of 19000 inductors [72]. It has better accuracy and higher simplicity than the equations described above, making it useful for this thesis.

Parasitic resistance (R_S)

Parasitic resistance is dependent on the frequency of operation. At DC, this value is mostly dependent on the sheet resistance of the material from which the wire is made. At high frequencies, this is overshadowed by the resistance that arises due to formation of eddy currents. It depends on resistivity of metal layer in which the inductor is laid out (ρ), total length of all inductor segments (l), width of the inductor (w) and its effective thickness (t_{eff}) [10]:

$$R_S = \frac{\rho l}{w t_{eff}} \tag{2.33}$$

Effective thickness, t_{eff}, is dependent on the actual thickness of the metal layer, t:

$$t_{eff} = \delta(1 - e^{-t/\delta}), \tag{2.34}$$

where δ is skin depth dependent on frequency f via relation

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{2.35}$$

Parasitic capacitance (C_S)

Parasitic capacitance is the sum of all overlap capacitances created between the spiral and the underpass. If there is only one underpass and it has the same width as the spiral, then the capacitance is equal to [10]

$$C_S = n w^2 \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{2.36}$$

where $t_{oxM1\text{-}M2}$ is the oxide thickness between the spiral and the underpass and ε_{ox} is the dielectric constant of the oxide layer between the two metals.

Oxide and substrate parasitics (C_{ox}, C_{Si} and R_{Si})

Oxide and substrate parasitics are approximately proportional to the area of the inductor spiral ($l \cdot w$), but are also highly dependent on the conductivity of the substrate and the operating frequency. In order to calculate the oxide capacitance C_{ox} and substrate capacitance C_{Si}, the effective thickness (t_{eff}) and effective dielectric constant (ε_{eff}) of either oxide or substrate must be determined. Effective thickness is calculated as [78]

$$t_{eff} = w\left[\frac{w}{t} + 2.42 - 0.44\frac{t}{w} + \left(1 - \frac{t}{w}\right)^6\right]^{-1}, \text{ for } \frac{t}{w} \le 1, \tag{2.37}$$

or

$$t_{eff} = \frac{w}{2\pi}\ln\left(\frac{8t}{w} + \frac{4w}{t}\right), \text{ for } \frac{t}{w} \ge 1 \tag{2.38}$$

for both oxide and substrate. Effective dielectric constant is determined as

$$\varepsilon_{eff} = \frac{1+\varepsilon}{2} + \frac{\varepsilon - 1}{2}\left(1 + \frac{10t}{w}\right)^{-\frac{1}{2}} \tag{2.39}$$

Then,

$$C_{ox} = \frac{wl\varepsilon_0\varepsilon_{effox}}{t_{effox}} \tag{2.40}$$

and

$$C_{\mathrm{Si}} = \frac{wl\varepsilon_0\varepsilon_{eff\mathrm{Si}}}{t_{effox\mathrm{Si}}} \tag{2.41}$$

Similarly, to calculate R_{Si}, effective thickness (t_{eff}) and effective conductivity (σ_{eff}) of substrate are needed. As for the capacitance, effective thickness is given by Equation (2.38), and effective conductivity can be obtained from

$$\sigma_{eff} = \sigma\left[\frac{1}{2} + \frac{1}{2}\left(1 + \frac{10t}{w}\right)^{-\frac{1}{2}}\right], \tag{2.42}$$

where $\sigma = \frac{1}{\rho}$ represents the substrate conductivity.

Therefore,

$$R_{\mathrm{Si}} = \frac{t_{eff\mathrm{Si}}}{\sigma_{eff} wl} \tag{2.43}$$

2.3.2.5 Quality factor and resonance frequency for single-π inductor model

The quality factor, discussed in Section 2.3, is the basic characterisation technique for inductors. For the single-π model, Q-factor can be calculated as [79]

$$Q = \frac{\omega L_S}{R_S} \cdot \frac{R_P}{R_P + \left[\left(\frac{\omega L_S}{R_S}\right)^2 + 1\right] R_S} \cdot \left[1 - (C_P + C_S) \cdot \left(\omega^2 L_S + \frac{R_S^{\,2}}{L_S}\right)\right], \tag{2.44}$$

where

$$R_P = \frac{1}{\omega^2 C_{ox}^{\,2} R_{\mathrm{Si}}} + \frac{R_{\mathrm{Si}} (C_{ox} + C_{\mathrm{Si}})^2}{C_{ox}^{\,2}}, \tag{2.45}$$

$$C_P = C_{ox} \cdot \frac{1 + \omega^2 (C_{ox} + C_{\mathrm{Si}}) C_{\mathrm{Si}} R_{\mathrm{Si}}^{\,2}}{1 + \omega^2 (C_{ox} + C_{\mathrm{Si}})^2 R_{\mathrm{Si}}^{\,2}} \tag{2.46}$$

and $\omega = 2\pi f$. Three different factors can be isolated in Equation (2.44) [28]. The first factor, $F_1 = \omega L_S / R_S$, is the intrinsic (nominal) Q-factor of the overall inductance. Second factor, $F_2 = \frac{R_P}{R_P + \left[(\omega L_S / R_S)^2 + 1\right] R_S}$, models the substrate loss in the semiconducting silicon substrate. The last factor, $F_3 = 1 - (C_P + C_S) \cdot \left(\omega^2 L_S + R_S^{\,2} / L_S\right)$, models the self resonance loss due to total capacitance $C_P + C_S$. This resonant frequency can be isolated by equating the last factor to zero, and solving for ω. This results in the formula for self resonance frequency of the spiral inductor:

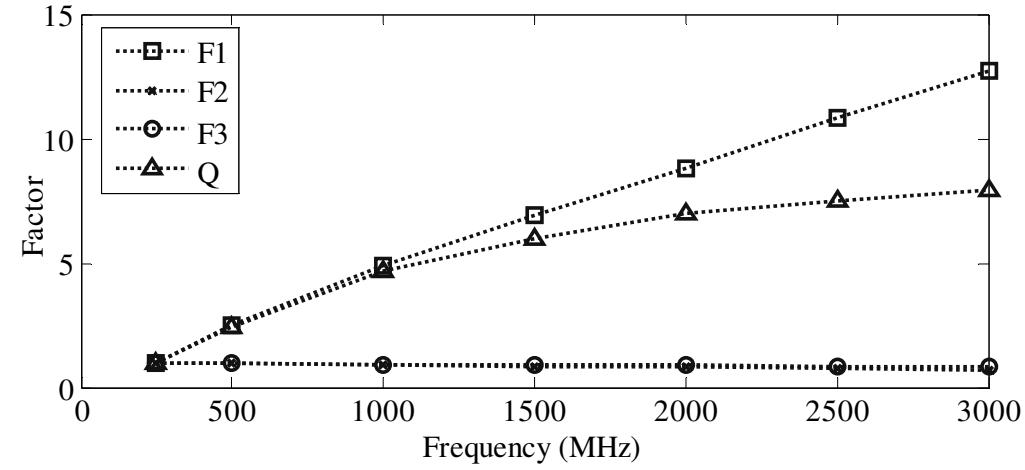
$$\omega_o = \sqrt{\frac{1}{L_S \cdot (C_P + C_S)} - \left(\frac{R_S}{L_S}\right)^2} \tag{2.47}$$

Substrate losses

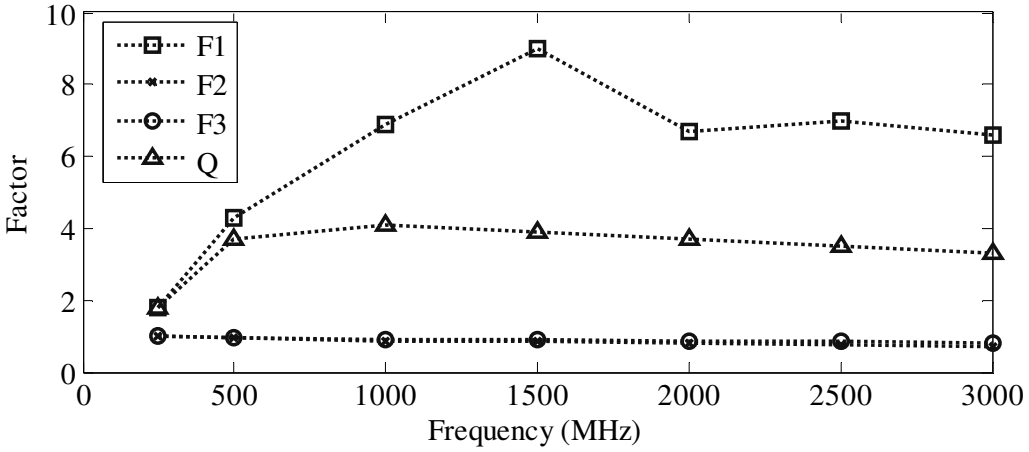
At low frequencies, the loss of metal line (F_1) restricts the performance of inductors [80]. In high frequency ranges, the loss of substrate (F_2) prevails as the restricting factor. F_2 is greatly dependent on the conductivity of the substrate. As conductivity increases at a fixed frequency, the skin depth of the substrate also increases, leading to an increase of eddy currents in the substrate resulting in a decrease of the Q-factor of the inductor. Heavily doped substrates are usually used in a sub-micron process, with substrate resistivity usually

lying in the range of 10 Ω·cm to 30 Ω·cm. As a result, in the traditional (Bi)CMOS process, the performance of spiral inductors is limited by the substrate. The MEMS processes, mentioned earlier in this thesis, strive to rectify this dependence.

Figure 2.32 shows the analysis of factors F_1, F_2 and F_3 defined in (2.44) for 1 nH and 5 nH sample spiral inductors optimised at different frequencies for their highest quality operation. It can be observed that, although the nominal Q-factor (F_1) increases with frequency, F_2 and F_3 decrease in the same range, resulting in the decrease of the overall Q-factor (Q) at frequencies above 1 GHz.



(a)



(b)

Figure 2.32. Analysis of the determining factors of the Q-factor equation for (a) 1 nH inductor and (b) 5 nH inductor.

2.3.2.6 Guidelines for integrating spiral inductors

As detailed in Section 2.3.2, although spiral inductors are a good choice for exclusively on-chip PAs, their use is not as straight forward. They occupy large areas on the chip, suffer from the low quality factors, and are difficult to design for the low tolerance. Capacitors and resistors, on the other hand, do not suffer from these problems.

When designing an integrated capacitor, a designer can simply increase or decrease the area of the component until the required capacitance is obtained. Although capacitance of the parallel plate capacitor does not solely depend on the area of its plates, but also on other factors such as fringing effects, a nearly linear relationship between the two is retained. Similar relationship between the length and total resistance holds for resistors. By modifying the length of a part of the process layer used for fabrication of the resistor, a designer can obtain the wanted value of its resistance. However, this does not apply to the spiral inductors. Contrary to the common sense, one cannot just simply increase the number of turns or width of a single turn to change the inductance. The complicated inductance relationship given in Equation (2.32) or any other can illustrate this interdependency. This complexity of spiral inductor models is one of the reasons why it is a common practice to choose an inductor from a library of inductors supplied with the process rather than to design an inductor for a needed inductance value. If a standard inductor cannot be used in the application of interest, then the iterative process is needed, where one guesses the geometry parameters that could result in the required inductance (and Q-factor) value, calculates inductance, parasitics and Q-factor given the guessed parameters, thereafter repeating this process until one is satisfied with the performance of the inductor. A flow chart of such approach is shown in Figure 2.33.

Reference [81] isolates some general guidelines that can assist in designing a high quality inductor, irrespective of the geometry of the inductor and its model:

1. Where possible, one should use the highest resistivity substrate available. This will reduce the eddy losses that decrease the Q-factor.
2. Placement of inductors should take place on the highest possible metal layers. In this way, substrate parasitics will have a less prominent role because the inductor will be further away from the silicon.

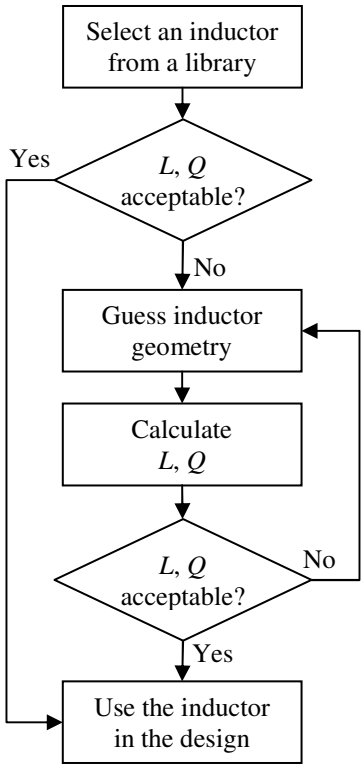


Figure 2.33. A flow chart of conventional spiral inductor design procedure.

3. If necessary, parallel metal layers for the body of the inductor can be used to reduce the sheet resistance.
4. Unconnected metal should be placed at least five turn widths away from inductors. This is another technique that helps reducing eddy current losses.
5. Excessively wide or narrow turn widths should be avoided. Narrow turns have high resistances, and wide turns are vulnerable to current crowding.
6. The narrowest possible spacing between the turns should be maintained. Narrow spacing enhances magnetic coupling between the turns, resulting in higher inductance and Q-factor values.
7. Filling the entire inductor with turns should be avoided. Inner turns are prone to the magnetic field, again resulting in eddy current losses.
8. Placing of unrelated metal plates above or under inductors should be avoided. Ungrounded metal plates will also aid the eddy currents to build up.
9. Placing of junctions beneath the inductor should be avoided. Presence of a junction close to the inductor can produce unwanted coupling of AC signals.
10. Short and narrow inductor leads should be used. The leads will inevitably produce parasitics of their own.

2.4 TECHNOLOGIES FOR POWER AMPLIFIER INTEGRATION

Traditionally, several device technologies have been used for integrating PAs [5, 52, 53]. Initially, gated structures such as MOSFETs, metal-semiconductor field effect transistors (MESFETs), high-electron-mobility-transistors (HEMTs) and pseudomorphic HEMTs (pHEMTs) had found a widespread use. After the introduction of bipolar transistor with a wide-gap emitter, or HBT [82], bipolar transistors emerged as a preferred choice, because of their higher gain and current densities at RF. In the late twentieth century, most of the on chip PA implementations were implemented with HBTs [52]. This resulted in transmitter systems that included at least two ICs in their implementation: a silicon CMOS based front end and a PA fabricated in another technology, which made them bulky and expensive. In the first decade of this century, BiCMOS devices are emerging as an alternative to the two-chip solution because they are able to bridge this integration gap, which as a result reduces the cost of transmitter manufacturing.

Technologies such as gallium-nitride (GaN), aluminium-gallium-nitride (AlGaN), silicon-carbide (SiC), and indium-phosphate (InP), have been struggling for survival in the battle between Si, SiGe and GaAs technologies. The AlGaN/GaN is suitable for both high frequency and high power designs, but together with the SiC technology it has been sidetracked on the road to microwave applications by technical difficulties and high fabrication costs [83]. The InP technology itself does not provide any substantial benefits for the linear PA design [84].

Table 2.5 shows some typical process parameters for the Si BJT, SiGe and GaAs processes [84]. After the inspection of parameters such as cut-off frequency f_T, breakdown voltages and parasitic capacitances, it becomes clear that GaAs presents the best technology for the PA integration. Silicon technology, as expected, offers the worst process parameters. Similar observation is possible by analyzing the PAE, power gain and scattering parameters (*S*-parameters) obtained from the performance measurement study detailed in [84], as summarised in Table 2.6. Measurements were obtained at f = 1.88 GHz with power supply of 3.4 V with quiescent current of about 90 mA for 28 dBm output.

Table 2.5. Process parameters for Si BJT, SiGe HBT and GaAs HBT technologies [84].

	Si BJT	SiGe HBT	GaAs HBT
f_T (GHz)	27	44	46
Forward gain, β	100	200	120
Base-emitter voltage, V_{be} (V)	0.8	0.8	1.33
Early voltage, V_A (V)	36	100	1223
Collector-emitter breakdown voltage, V_{ce} (V)	6.2	6	14.3
Collector-base breakdown voltage, V_{cb} (V)	20	12	26
Emitter-base breakdown voltage, V_{eb} (V)	2	5	6.9
Power density (mW/μm$^{2)}$	2	2	0.9
Thermal conductivity (W/cm-°C)	1.5	1.5	0.49
Base-emitter capacitance, C_{be} (fF)	11	10	2.4
Base-collector capacitance, C_{bc} (fF)	3.6	3.3	1
Possibility of NMOS and PMOS integration	Yes	Yes	No

Table 2.6. Various performance parameters for PAs fabricated in three different technologies (f = 1.88 GHz, V_{CC} =3.4 V and P_{OUT} = 28 dBm) [84].

	Si BJT	SiGe HBT	GaAs HBT
PAE (%)	33.1	35	39.3
Gain (dB)	22.1	21.8	27.1
S_{11} (dB)	-13.8	-16.9	-12.6
S_{12} (dB)	20.2	20.5	27.2

However, it should be noted that the comparison between Si and SiGe technologies is performed from BiCMOS perspective, that is using a BJT in case of pure Si technology, which is not available in the widely used CMOS technologies. Having that in mind and after noting that some SiGe process parameters (e.g. f_T) are comparable to the ones of GaAs technologies, it can be identified that the SiGe BiCMOS performance lies comfortably between the Si CMOS and GaAs HBT technologies and that it is suitable for the PA integration. As such, the SiGe BiCMOS can be considered a CMOS technology with a HBT available for use, allowing for traditional CMOS stages to be incorporated on the same chip, which is, as stated before, considered the main advantage of SiGe. Some additional advantages over the GaAs can also be identified [52]:

- Chip robustness is facilitated by heat-conductive silicon substrate (also seen from Table 2.5),
- Circuit design issues from thermal runaway (Section 2.2.7) are minimized, and
- Reliability at high current densities enables reduction in device size.

Although suitable for experimentation in this thesis, many challenges of high power design on SiGe remain. Nevertheless, new technology trends and ever increasing PA requirements

will always lead to a careful re-evaluation of this powerful technology for commercial use [85].

2.5 RAPID POWER AMPLIFIER DESIGN AND AUTOMATION

The term "rapid power amplifier design" is used to describe a process where many PAs with similar specifications must be designed simultaneously. This section first identifies the need for rapid PA design, followed by the description of several ways to automate this tedious task.

2.5.1 The need for rapid PA design

When wireless transmitters are designed, a set of specifications will normally exist depending on their application. Some of these specifications will directly or indirectly be applicable to the PA itself. These will most certainly include the output power and efficiency described in Sections 2.2.1 and 2.2.3. Additionally, bandwidth and carrier frequency are also of importance and they are dictated by the frequency band in which the transmitter must operate.

Devices with wireless capabilities, such as cordless phones, cellular phones, laptops, personal data assistants (PDAs), as well as many computer peripherals will typically operate in one of the unlicensed frequency bands. Three different ISM bands are available for utilisation in most countries in the world, with transmission channels centred close to 915 MHz, 2.4 GHz and 5 GHz [86]. Two groups of standards are greatly popular for WLANs: Bluetooth and other IEEE 802.11 standards.

Depending on the standard and the frequency band, there will be a number of channels available in each band for use by a transmitting device. For example, for the IEEE 802.11b standard operating at around 2.4 GHz, there are 52 different channels available for transmission, each with a different carrier frequency. If a transmitter is to operate over more than one channel in this band, which will typically arise in situations where two or more of the same devices are present in the same wireless area, then it will either have to contain more than one PA, each optimised for operation in a different channel, or a lone PA will have to be tuneable in some way. In either case, the complexity of the PA system will greatly increase, resulting in a tedious design task.

2.5.2 Automating the rapid PA design

This problem can be resolved by introducing a set of algorithms that will automate a PA design for a given set of specifications. These algorithms should be able to cover the design of several monolithic PA high-efficiency output stages, such as those of the Class E or F (Section 2.2.5). It should also be able to handle the design of an appropriate integrated inductor, as described in Section 2.3. Even in the age of fast personal computers, the speed of execution of the design software still remains important.

There are a number of simple tools addressing some of the given aspects. One of them is a parasitic aware program [22]. It can be used for a PA design optimised for maximum efficiency. However, it only tackles the two-stage Class-E amplifier, with inductor design integrated into the tool. A spiral inductor design tool is described in [26], which can be used to design adequate spiral inductors. These and other available tools can be used in conjunction with commercial synthesis tools, such as MATLAB, Tanner Tools [87] and/or Cadence Virtuoso (see Chapter 3 for description of some of these tools), but to create a really successful design process the designer must be acquainted with many pieces of software instead of only one, which inevitably decreases the speed of design process flow.

Creating a routine that offers comprehensive design coverage, as a part of methodology for design of PAs, therefore, presents a vast research opportunity for this thesis, as stated in the form of a research hypothesis in Section 1.2.

2.6 CONCLUSION

This chapter identified major concepts important for this thesis. After a thorough study of various PA output stages, the switching PA classes (Class E and Class F), were identified as the best choice for integration with wireless transmitters. Although many integrated inductor implementations are possible, the spiral inductor presents the best choice for low-cost integration, removing the need for modification of a standard process and/or outside-chip modelling. The SiGe BiCMOS technology was seen as a very good compromise between the widely popular and inexpensive CMOS on one side, and more expensive GaAs HBT technology, traditionally used in high power design, on the other. As such, it can be used for prototyping the PA devices experimented with in this thesis. Finally, a need for a rapid PA design has been identified, and a method to accomplish this,

incorporated in a software routine that aids PA and spiral inductor design, was proposed to fill in the gap in available knowledge. Chapter 3 follows with the description of the methodology used in this research.

CHAPTER 3 METHODOLOGY

3.1 INTRODUCTION

Chapter 2 provided a review of literature related to the topic of the thesis. This chapter describes methodology used for this research. It starts with the flow of the research process and continues with the description in some detail of the technologies used to simulate the key concepts and prototype the test chip. A part of the chapter deals with various software packages used in the course of the research, such as the software package for conceptual design, CAD packages for simulation and layout, measurement equipment, as well as the software package for algorithm development.

3.2 RESEARCH METHODOLOGY OUTLINE

Due to the fact that the concepts applied in developing a method for rapid PA design had to be transformed into circuits that can be simulated and tested, a major part of this research revolved around designing PAs and spiral inductors, which could be critically evaluated, simulated and finally prototyped.

Design and simulation of various PA stages in CAD tools described later in Section 3.5 ran in parallel with research and development of the set of algorithms for PA automation in MATLAB [16] (Section 3.4). Following successful simulations, a layout, essentially a blueprint for the IC prototype, was developed. The IC is to be used to characterise effects that cannot be characterized otherwise. This includes investigation of the influence of parasitics, which is particularly important for the RF circuits. Also, taking measurements of the fabricated IC presents a good way to get an insight into the quality of operation of on-chip spiral inductors.

Research methodology followed in this thesis is graphically represented by the flow diagram shown in Figure 3.1.

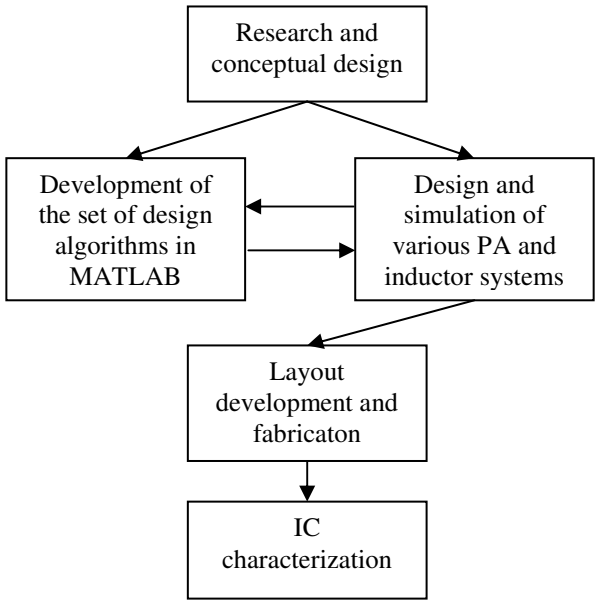


Figure 3.1. Research methodology followed in this thesis.

3.3 THE IC PROCESS

The IC process is significant because of the following reasons:

- All simulations are performed using the SPICE models particular to the IC process.
- Physical layout of the PA and inductor systems are drawn in conformity with the design rules specific to a particular IC process.
- Correct modelling of spiral inductors is process dependent, as described in Section 2.3.2. Spiral inductor part of the PA design routine must be able to interpret the IC process parameters in order to work correctly.

The main process chosen for this thesis is S35 0.35 µm SiGe BiCMOS process from AMS [13]. It is a SiGe BiCMOS process with NPN HBTs, PIP and MIM capacitors and several libraries of standard metal-3 (3M) and thick-metal (TM) spiral inductors. Exact process parameters cannot be disclosed in this thesis due to the non-disclosure agreement (NDA) signed between the author (via University of Pretoria) and AMS. Further process details can be found in [88-90], if available.

Measurements were essential for the works of this thesis. Fabrication of the IC was sponsored by Metal Oxide Semiconductor Implementation Service (MOSIS) [91] as a part of the MOSIS Education Programme (MEP). A grant for a multi-purpose wafer (MPW)

was given to the University of Pretoria. The technology node in which circuits needed to be completed was the 7WL 180 nm process from IBM [14]. Most important features of this process are similar to those of the AMS process except for differences, inter alia, in available capacitors and inductors, and the fact that design rules allow for smaller wire and polysilicon widths and spacing than for the AMS process. An NDA agreement was also signed with IBM; for full process parameters please refer to [92] if available.

3.4 CONCEPTUAL DESIGN AND ALGORITHM DEVELOPMENT

Complete conceptual design and mathematical modelling was done with the aid of MATLAB from Mathworks. This package is a programming language that supports a great number of mathematical functions, and it can be used to speed up tedious hand calculations.

The same package was used to design the first version of the PA design routine. Although this version did not have a graphical user interface (GUI) front-end for the algorithms, the ease of use of MATLAB programming language simplified debugging.

3.5 MODELLING, SIMULATION, AND LAYOUT DESIGN

Modelling and simulation of various PA circuits was performed in Cadence Virtuoso package from Cadence Design Systems. Several tools available in this package were used, and their names and functionality are given in Table 3.1.

Table 3.1. Tools of Cadence Virtuoso package and their functionality.

Tool name	Functionality
Virtuoso Schematic Composer	Schematic level circuit design [93]
Virtuoso Analog Design Environment (ADE) with Spectre and SpectreRF Circuit Simulator	SPICE based simulator [94-96]
Virtuoso Wavescan	Waveform viewer [97]
Virtuoso Layout Editor with Diva/Dracula/Assura DRC and LVS	Layout generation, design checks and layout versus schematic comparison [98]
Spiral Inductor Modeler	Electromagnetic (EM) simulation of spiral inductors [99]

3.5.1 Modelling and simulation

Modelling and simulation were done in Virtuoso Schematic Editor, ADE, Spectre and Spectre RF [93-96]. After being conceptually designed, whether using a design routine that was developed in parallel or otherwise, schematics of each test circuit was drawn in Virtuoso Schematic Editor by instantiating components that have been SPICE modelled and provided by AMS and connecting them by wires. Since pre-designed inductors

available from the vendor were not used here, custom inductor models were used to correctly model spiral inductors. ADE was used to export netlists of created designs, and run analogue (DC operating point, transient, frequency domain, RF) simulations on the exported SPICE netlists using Spectre and Spectre RF. The output of the simulation was then viewed in Wavescan waveform viewer [97] by graphing the resulting waveforms. The waveforms were used to interpret the simulation results.

3.5.2 Layout design and verification

Once satisfied with simulations, the layouts of various PAs were developed in Virtuoso Layout Editor [98]. At this level the transistors, capacitors, inductors and other devices were drawn in accordance with the design rules specified by the IBM process [92]. The design rules check (DRC) module is included here. The layout versus schematic (LVS) module served to investigate the correlation between the given schematic (created in Virtuoso Schematic Editor and simulated in ADE) and layout (created in Virtuoso Layout Editor). The purpose of the comparison was to detect design errors that might have occurred in the process of transforming the schematic into the layout.
Several test circuits were placed on one prototype package.

3.5.3 EM simulation

EM simulation was necessary for simulating spiral inductors. It was done in Virtuoso Spiral Inductor Modeler [99]. The solver for the Spiral Inductor Modeler employs Partial Element Equivalent Circuit (PEEC) algorithm in the generation of macromodels for the spiral components. Electro-static and magneto-static EM solvers are invoked separately to extract the capacitive and inductive parameters of the spiral inductor structure. A process file with information on metal and dielectric layers was required by the modeller and it needed to be manually created.

3.5.4 SPICE model of the HBT

PA simulation, described in Section 3.5.1, is only as accurate as the SPICE model of the transistor used in this simulation.

For the PAs simulated in AMS S35 process, an HBT was used. Traditionally, the Gummel-Poon model was the most popular model for the design of bipolar circuits for a considerable period of time [100]. However, an RF SPICE model, Vertical Bipolar Inter-

Company (VBIC) model for the HBT, available from AMS and accurate up to frequencies of 20 GHz [89], offers several improvements over Gummel-Poon model (particulars of which cannot be disclosed here due to the NDA mentioned earlier). The model used for HBT transistors in IBM 7WL process was also a VBIC model [101].

3.6 MEASUREMENT SETUP AND EQUIPMENT

S-parameters of the fabricated ICs were measured by means of the R&S ZVA 40 Vector Network Analyzer from Rohde and Schwarz [102]. This network analyzer, pictured in Figure 3.2 is capable of measuring two-port parameters up to 40 GHz which is sufficient for the research in this thesis.

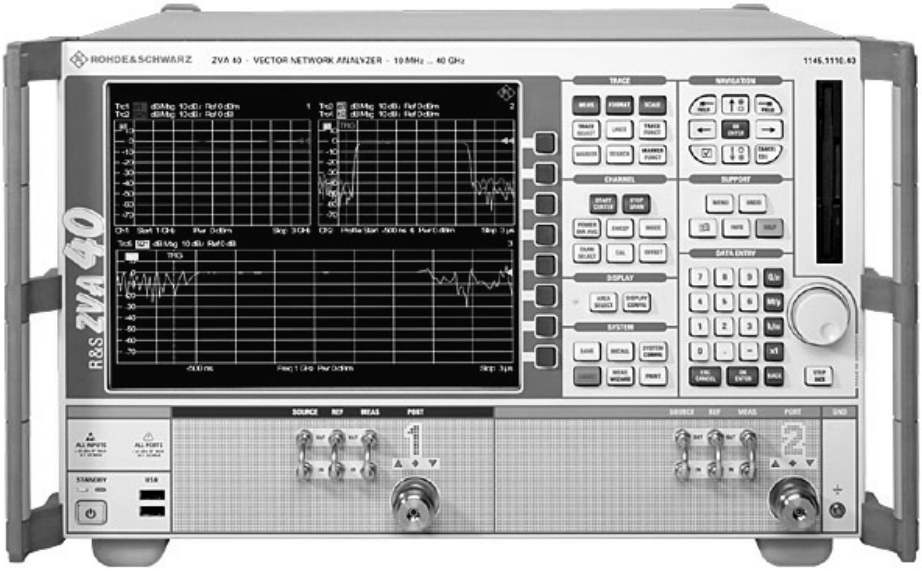


Figure 3.2. R&S ZVA Vector Network Analyzer [102].

3.7 CONCLUSION

Chapter 3 described the design approach to be applied to this thesis. An overview of the design methodology used to complete the research has been given. This was followed by the discussion of the two IC fabrication processes, where simulations were performed in AMS S35 process, and layouts for several good PA configurations were drawn in IBM 7WL process. A description of MATLAB, the tool used for mathematical modelling and algorithm development was given, followed by the presentation of CAD tools (part of Cadence Virtuoso package) to emphasize and justify the need for their use. VBIC model for HBT used for SPICE simulations was described as well, since it was identified as the

model used in simulations for both AMS and IBM processes. Finally, the network analyzer, capable of measuring frequencies up to 40 GHz, was presented. Chapter 4 follows with the details on the system level design routine.

CHAPTER 4 SYSTEM LEVEL DESIGN ROUTINE

4.1 INTRODUCTION

In Chapter 3, the methodology used to carry out the research was described. In this chapter, concepts behind the MATLAB-routine based method for rapid PA design are addressed. The first part of the chapter deals with the method for designing of Class-E PAs. This is followed by a discussion on the method for designing of Class-F PAs. The proposed method for spiral inductor design is described after the discussion on PA design. This chapter also includes several other aspects of importance for this routine, viz. input and output matching as well as full integration of proposed spiral inductors into the complete PA system. The complete MATLAB listings for all developed sub-routines are given in Appendix A.

4.2 METHOD FOR DESIGNING THE CLASS-E POWER AMPLIFIERS

In this section, a novel, routine-based method for designing the Class-E PAs is proposed. It is partially based on equations from the classic paper by Sokal and Sokal [39] (as described in Section 2.2.5.2), but it has been adapted for use in integrated circuits with HBTs. Basic principle of this routine is, however, technology independent.

The PA from Figure 2.9 has been used for this method and is repeated in Figure 4.1 for convenience.

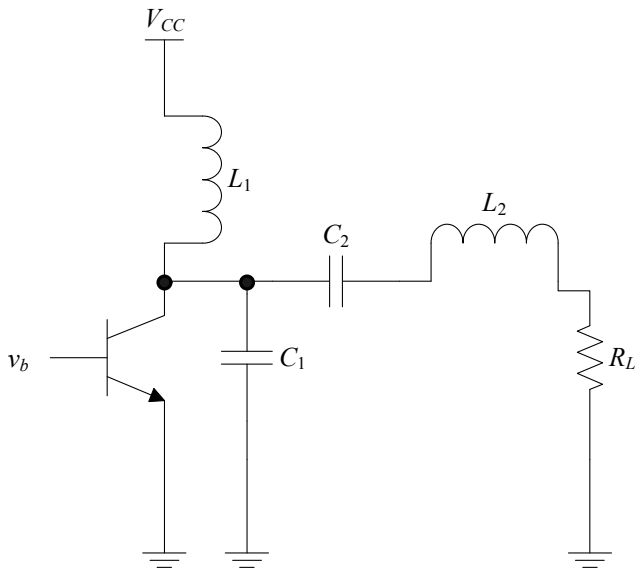


Figure 4.1. Circuit diagram of a single ended Class-E PA [37].

4.2.1 Input parameters

Several parameters are needed as the inputs of the Class-E subroutine:

- *Centre frequency of the channel (f_o).* This quantity, specified in megahertz, is determined by the specifications of the transmitter system the PA is a part of.
- *The loaded quality factor (Q_L).* This is the quality factor of the series resonator created by inductance L_2 and capacitance C_2. It can be chosen freely by the PA designer, but a trade-off must be considered which exists between high efficiency and power (low Q_L) on one side, and total harmonic distortion (THD) of the output signal on the other side (high Q_L). Plausible Q factor is in the range of 5 to 10 [37]. If efficiency is important, a lower Q_L can be chosen and harmonics removed by additional filters at the output of the amplifier [39]. The narrowband output matching network, described in Section 4.4, can serve for this purpose.
- *Output power (P_{out}).* This quantity, specified in miliwatts, is also determined by specifications of the transmitter system. A higher output power is achieved with a lower load resistance (R_L), which places more stringent requirements for the output impedance matching. High output power can also result in the need for a higher supply voltage.
- *Supply voltage (V_{CC}).* This quantity, specified in volts, can be chosen by the designer, but attention must be paid that it does not exceed the value of $BV_{CEO}/3.56$

(see Equation (4.2)), where BV_{CEO} is defined in **Error! Reference source not found.** as collector-emitter breakdown voltage.

Some optional parameters can be specified:

- *Collector-emitter saturation voltage (V_{CEsat}).* This parameter, also specified in volts, is a process-dependent quantity, usually equal to 0.1 or 0.2 V. Since it is approximately equal to 0, its omission will result in minimal discrepancies between the actual and predicted PA values.
- *Maximum and minimum inductance values (L_{max} and L_{min}).* These two quantities, specified in nanohenries, can be included by the designer to limit extremely high or low values of inductors.
- *Collector-emitter breakdown voltage (BV_{CE}).* This quantity, specified in volts, warns the user if the V_{CC} specified is high enough to result in transistor entering breakdown.

Parameters needed for the Class-E PA subroutine are summarized in Table 4.1.

Table 4.1. Input parameters required for the Class-E PA software routine.

Parameter	Unit	Mandatory / Optional
Centre frequency of the channel (f_o)	MHz	Mandatory
Loaded quality factor (Q_L)	-	Mandatory
Output power (P_{out})	mW	Mandatory
Supply voltage (V_{CC})	V	Mandatory
Collector-emitter saturation voltage (V_{CEsat})	V	Optional
Maximum and minimum inductance values (L_{max} and L_{min})	nH	Optional
Collector-emitter breakdown voltage (BV_{CE})	V	Optional

4.2.2 Subroutine outputs

The following quantities are outputs of the Class-E software subroutine:

1. Optimum load resistance, R_L (Ω);
2. Shunt capacitor, C_1 (pF);
3. Series capacitor, C_2 (pF) and series inductor, L_2 (nH);
4. Feed inductor, L_1 (RFC);
5. Shunt capacitor, C_p (pF);
6. DC and maximum currents, I_{DC} and i_{max} (mA);
7. Maximum collector voltage, v_{max} (V); and
8. Loaded quality factor, Q_L, which places inductances within the maximum and minimum values.

4.2.3 Description and flow diagram of the Class-E subroutine

This subroutine is carried out in a linear fashion. It utilizes Equations (2.16) through (2.19) to calculate R_L, L_2, C_2 and C_1. The DC current is calculated by [30]

$$I_{DC} = \frac{V_{CC}}{1.734R_L} \tag{4.1}$$

The maximum transistor voltage and current are given by

$$v_{max} = 3.56V_{CC} \tag{4.2}$$

and

$$i_{max} = 2.86I_{DC} \tag{4.3}$$

The capacitor C_1 must include the output capacitance of the transistor used for amplification.

Flow diagram of the Class-E design subroutine is given in Figure 4.2. Complete MATLAB code listing for the subroutine is given in Figure A.3 and Figure A.4.

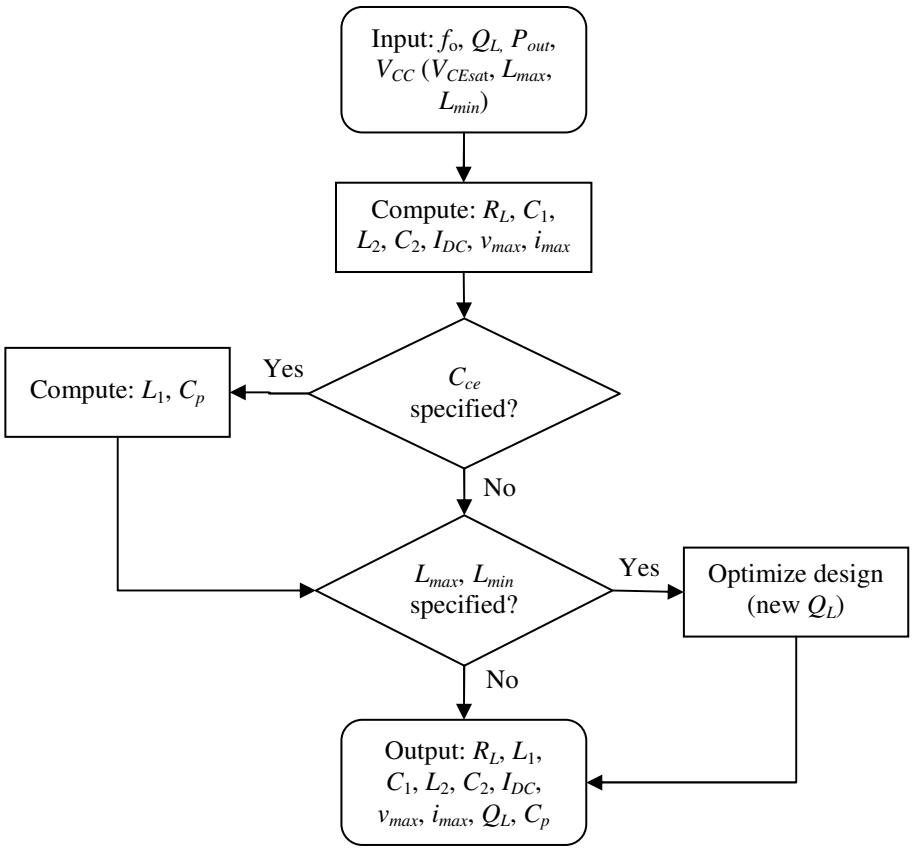


Figure 4.2. Flow diagram of the Class-E PA design subroutine.

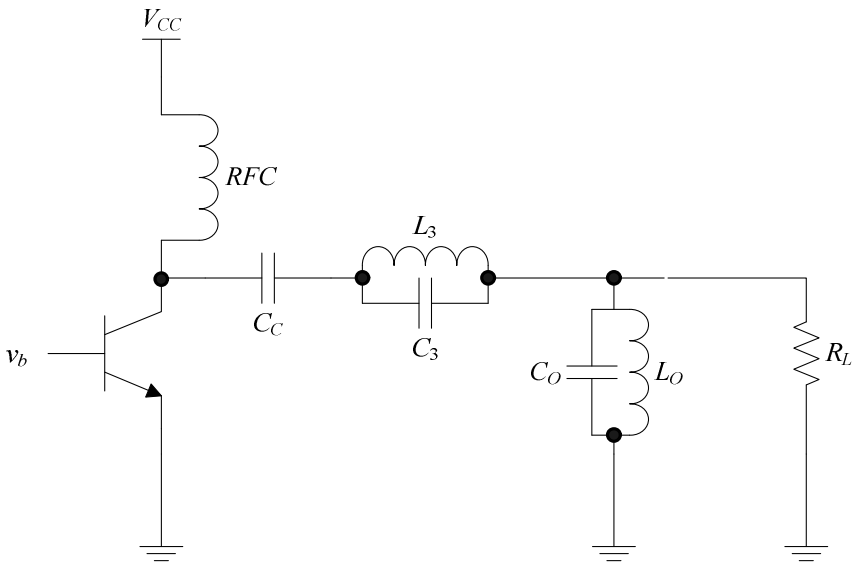
4.3 METHOD FOR DESIGNING THE CLASS-F POWER AMPLIFIERS

This section extends the concepts of the routine-based method for designing the Class-E PAs from the previous section onto the design of the Class-F PAs. In Section 2.2.5.3 it was discussed that the efficiency of integrated Class-F PAs depends on the number of harmonic resonators used. In this section, a method for designing two different Class-F PA configurations are discussed: the third-harmonic peaking Class-F circuit (shown in Figure 2.13 and repeated in Figure 4.3(a) for convenience) and Class-F PA with resonators up to the fifth harmonic (Figure 4.3(b)). Theoretical efficiencies for the two circuits are 81.7% and 90.5% respectively [43]. The former is included because of its particularly simple output filter, whilst the latter is included because it can deliver relatively high efficiency while still keeping the output filter reasonably simple. Including a greater number of resonators further increases the complexity of the circuit and is not deemed feasible here.

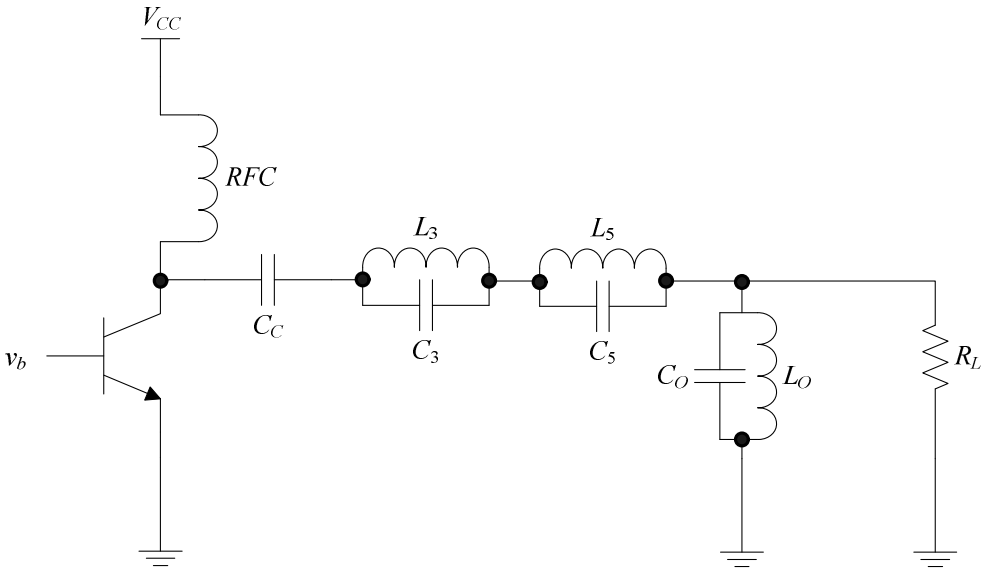
4.3.1 Input parameters

As in the case of the Class-E design, several input parameters are needed for the Class-F subroutine to complete successfully:

- *Centre frequency of the channel (f_o).* Again, this is determined by the specifications of the transmitter system of which the PA is a part. It is specified in megahertz.
- *Output power (P_{out}).* This quantity, similar to the one in the Class-E part of the routine, is specified in miliwatts and is also determined by the specifications of transmitter system.
- *Supply voltage (V_{CC}).* This quantity, specified in volts, can be chosen by the designer, but attention must be paid that the value of BV_{CEO}/δ_V (see Equation (4.8)) is not exceeded.
- *Inductance values for nominal resonant tank (L_O), third-harmonic resonant tank (L_3) and fifth-harmonic resonant tank (L_5).* In case of Class-F PA, there is no trade-off between the filtering inductance values to some other quantity, and these values can be chosen freely. Resonant capacitors are calculated based on the corresponding inductance values. Fifth-harmonic resonant tank inductor is only needed if the fifth-harmonic resonator is used.



(a)



(b)

Figure 4.3. Class-F PA circuits: (a) third-harmonic peaking circuit and (b) circuit with resonators up to the fifth harmonic.

- *Collector-emitter breakdown voltage (BV_{CE}).* This quantity, specified in volts, is the only optional parameter and it is used in order for the program to warn the user if V_{CC} specified is high enough to send the transistor into breakdown.

Parameters needed for the Class-E PA part of the routine are summarized in Table 4.2.

Table 4.2. Input parameters required for the Class-F PA software routine.

Parameter	Unit	Mandatory / Optional
Centre frequency of the channel (f_O)	MHz	Mandatory
Output power (P_{out})	mW	Mandatory
Supply voltage (V_{CC})	V	Mandatory
Filtering inductances (L_0, L_3 and L_5)	nH	Mandatory
Collector-emitter breakdown voltage (BV_{CE})	V	Optional

4.3.2 Subroutine outputs

The following quantities are outputs of the Class-F software subroutine:

1. Optimum load resistance, R_L (Ω);
2. Nominal frequency resonant capacitor, C_O (pF);
3. Third- and fifth-harmonic frequency resonant capacitors, C_3 and C_5 (pF);
4. DC current, peak collector current and output peak current, I_{DC}, i_{Cm} and I_{om} (mA); and
5. Peak collector voltage and peak output voltage, v_{Cm} (V) and V_{om} (V).

4.3.3 Description and flow diagram of the Class-F subroutine

In the case of the Class-F subroutine, voltage and current coefficients are needed in order to shape current and voltage waveforms to deliver maximum power and efficiency to the load, as discussed in Section 2.2.5.3. All required coefficients are tabulated in Table 4.3 for the two Class-F PA configurations.

Table 4.3. Maximum-efficiency waveform coefficients [43].

Coefficient	Value (Resonators up to third-harmonic)	Values (Resonators up to fifth-harmonic)
γ_V	1.1547	1.2071
δ_V	2	2
γ_I	1.4142	1.5
δ_I	2.1863	3

Similarly to the case of the Class-E PA, design is performed for the optimum load resistance [43]:

$$R_L = \frac{\gamma_V{}^2 V_{CC}{}^2}{2P_{out}} \tag{4.4}$$

DC current needed for correct waveform shaping is given by

$$I_{DC} = \frac{\gamma_V V_{CC}}{\gamma_I R_L} \tag{4.5}$$

Maximum output voltage and current can be calculated by Equations (2.22) and (2.23) from Section 2.2.5.3. Peaks of the collector voltage and current waveforms are given by

$$v_{Cm} = \delta_V V_{CC} \tag{4.6}$$

and

$$i_{Cm} = \delta_I I_{DC} \tag{4.7}$$

Resonant capacitors (C_O, C_3 and C_5) can be calculated by once again manipulating Equation (2.14):

$$C_i = \frac{1}{(2\pi f)^2 L_i}, \tag{4.8}$$

where $i = O$, 3 or 5.

Flow diagram of the Class-F PA design subroutine is given in Figure 4.4. Complete MATLAB code listing for the routine is given in Figure A.5 and Figure A.6.

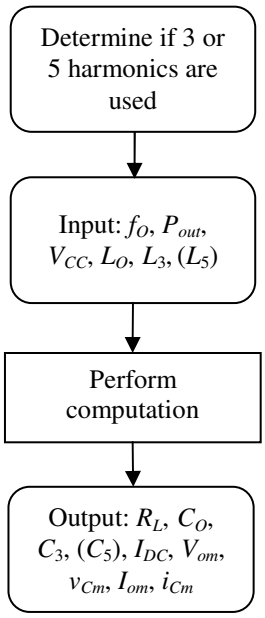


Figure 4.4. Flow diagram of the Class-F PA design subroutine.

4.4 METHOD FOR OUTPUT MATCHING

Output matching for a PA was discussed in Section 2.2.4. The PA design routine utilizes both wideband and narrowband matching, and choice of output network depends on the specific application.

4.4.1 Input parameters

The following input parameters are needed for the output matching part of the routine to complete successfully:

- *Source impedance of the matching network (R_S).* This impedance is equivalent to the optimum load resistance of the PA and it is specified in ohms.
- *Load impedance of the matching network (R_L).* This impedance is equivalent to the impedance of the antenna. It is specified in ohms and it is usually equal to 50 Ω.
- *Centre frequency of the matching network (f_O).* In PA applications, this is the centre frequency of the channel. The matching network will only be operating correctly at the centre frequency. This quantity is specified in megahertz.
- *Bandwidth of the matching network (B).* This parameter, also specified in megahertz, is needed for narrowband matching networks (T and Π networks).

Since most antennas have 50 Ω impedances, the load impedance can be assumed known and it should be specified only if it differs from the default value.

4.4.2 Subroutine outputs

Inductance (L_i) and capacitance (C_i) parameters of five different matching networks, where i = 1 or 2, are the outputs of this part of the PA design routine. These matching networks are shown in Figure 4.5(a)-(e) [33].

4.4.3 Description of the matching network subroutine

The matching network subroutine executes in linear fashion, using a predetermined set of equations.

4.4.3.1 High-pass L network

The high pass L network is shown in Figure 4.5(a). The matching inductor L_1 is determined by [33]

$$L_1 = \frac{1}{2\pi f_O}\sqrt{\frac{R_S{}^2 R_L}{R_L - R_S}} \tag{4.9}$$

and the matching capacitor is determined by

$$C_1 = \frac{1}{2\pi f_O}\left(\frac{R_L{}^2 + (2\pi f_O L_1)^2}{R_L(2\pi f_O L_1)}\right) \tag{4.10}$$

4.4.3.2 T networks

Calculations for T networks of Figure 4.5(a) and (c) are based on the method described in [103]. Using this method, two L networks separated by virtual resistance R_V are designed, as shown in Figure 4.6. In this figure, X_{S1} and X_{P1} are reactances of the first L network, and X_{S2} and X_{P2} are reactances of the second L network. The two L networks are then combined into a single T network by removing the virtual resistance.

The virtual resistance is found from

$$R_V = R_{small}(Q^2 + 1)\,, \tag{4.11}$$

where R_{small} = min(R_S, R_L), and $Q = f_O/B$ is the Q-factor of the matching network. Series reactance X_{S1} is then

$$X_{S1} = QR_S \tag{4.12}$$

and parallel reactance X_{P1} is

$$X_{P1} = \frac{R_V}{Q} \tag{4.13}$$

For the second L network, a separate Q-factor needs to be calculated:

$$Q_2 = \sqrt{\frac{R_V}{R_L} - 1} \tag{4.14}$$

and X_{S2} and X_{P2} are then

$$X_{S2} = Q_2 R_L \tag{4.15}$$

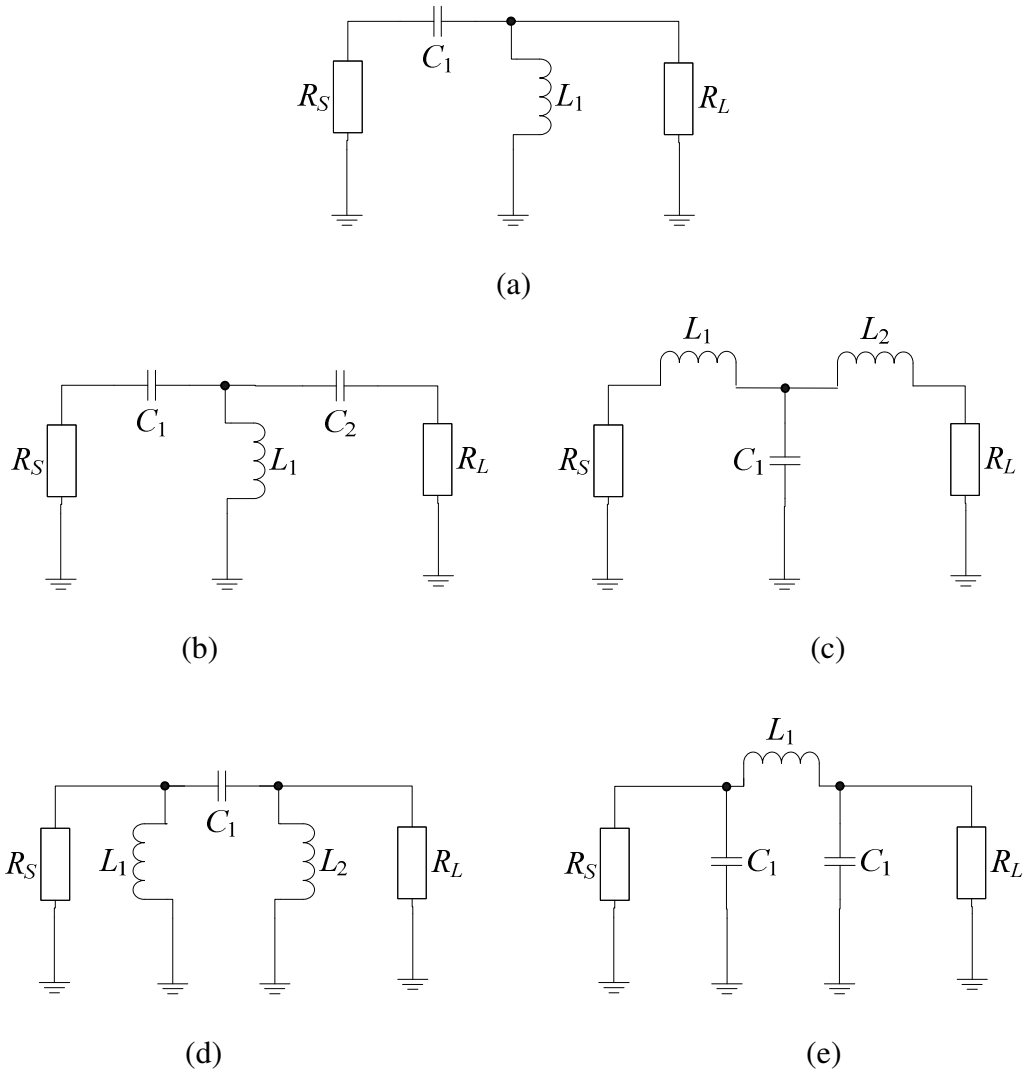


Figure 4.5. Five matching networks that are output of the matching network PA design subroutine: (a) wideband high-pass L network, (b) narrowband capacitor-inductor-capacitor T network, (c) narrowband inductor-capacitor-inductor T network, (d) narrowband inductor-capacitor-inductor Π network and (e) narrowband capacitor-inductor-capacitor Π network.

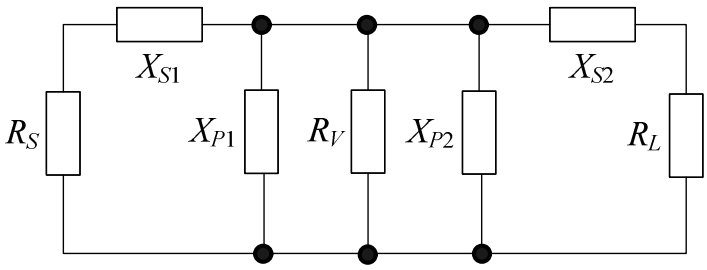


Figure 4.6. Two L networks separated by virtual resistance forming a T network.

and

$$X_{P2} = \frac{R_V}{Q_2} \tag{4.16}$$

After all the reactances have been calculated, virtual resistance is removed and X_{P1} and X_{P2} are combined in parallel to get final reactance X_P:

$$X_P = \frac{X_{P1} X_{P2}}{X_{P1} + X_{P2}} \tag{4.17}$$

Definitions for reactances of capacitors and inductors can be used to obtain actual values of inductors and capacitors needed:

$$L_i = \frac{X_{Li}}{2\pi f} \tag{4.18}$$

and

$$C_i = \frac{1}{2\pi f X_{Ci}}, \tag{4.19}$$

where L_i and C_i are inductors and capacitors in the matching network.

4.4.3.3 Π networks

Similar procedure can be applied to the Π networks Figure 4.5(d) and (e), with the difference that in this case serial reactances X_{S1} and X_{S2}, instead of parallel reactances X_{P1} and X_{P2}, are separated by a virtual resistor. Virtual resistance is given by

$$R_V = \frac{R_{high}}{Q^2 + 1}, \tag{4.20}$$

where $R_{high} = \max(X_S, X_L)$. X_{S2} and X_{P2} are then

$$X_{S2} = QR_V \tag{4.21}$$

and

$$X_{P2} = \frac{R_L}{Q} \tag{4.22}$$

Q-factor of the first L network is

$$Q_1 = \sqrt{\frac{R_S}{R_V} - 1} \tag{4.23}$$

and X_{S1} and X_{P1} are then

$$X_{S1} = Q_1 R_V \tag{4.24}$$

and

$$X_{P1} = \frac{R_P}{Q_1} \tag{4.25}$$

After all reactances have been calculated and virtual resistance removed, X_{S1} and X_{S2} are simply added, and inductors and capacitors are obtained from Equations (4.18) and (4.19).

Complete code listing for this part of the routine is given Figure A.31.

4.5 METHOD FOR DESIGNING SPIRAL INDUCTORS

As discussed in Chapter 2, the inductor is the most important passive component of any PA. Spiral integrated inductor presents a viable option for practical implementations of PAs designed with the aid of the PA design routine described in this chapter. This is because of the deterministic models that can be used to accurately predict the inductance value and Q-factors of any inductive structure on chip, given the process parameters and geometry of that inductive structure. However, an iterative procedure is used in practice, where one "guesses" inductor geometry that will result in an inductor with the performance close to the performance needed for a good power amplification (as illustrated in the flowchart in Figure 2.33). In this section, an improvement to the iterative procedure is proposed. A new non-iterative routine can find an inductor of the specified value, with the highest possible Q-factor, occupying a limited area, and using predetermined technology layers.

Concepts are developed for the single square spiral inductor of Figure 2.27 (a). The drawing of this geometry is repeated in Figure 4.7 for convenience.

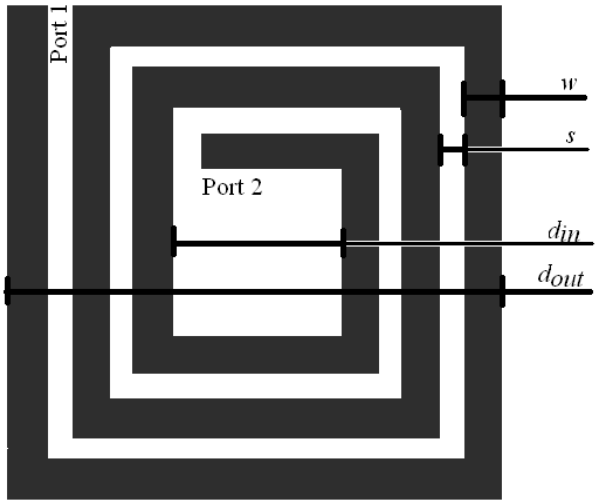


Figure 4.7. Integrated square spiral inductor.

4.5.1 Input parameters

The main idea behind this routine is to synthesize the square inductor geometry resulting in the highest Q-factor for specified inductance given some design constraints. Alternatively, inductances and Q-factor values of various square inductors can be calculated if the geometry parameters of such inductors are given.

For accurate inductor modelling, two sets of parameters are needed: geometry and process parameters, together with the frequency of operation of the inductor. For the highest Q-factor, higher layers of the metal should be used for the inductor spiral. Other general guidelines for the inductor design from Section 2.3.2.6 should be followed where possible.

Three subsections that follow give a detailed description of parameters needed for the spiral inductor design.

4.5.1.1 Geometry parameters

If the geometry of a device is specified and the inductance and Q-factor are to be determined (analysis), the following input geometry parameters are necessary:

- Outer diameter, d_{out} (μm);
- Inner diameter, d_{in} (μm);
- Turn width, w (μm); and
- Number of turns, n.

If the inductance is specified, and geometry resulting in the highest Q-factor is required (synthesis), only constraints for the geometry should be specified (all in micrometer):

- Minimum value of inner diameter, $d_{in(min)}$;
- Maximum value of outer diameter, $d_{out(max)}$;
- Minimum value for turn spacing, s_{min}; and
- Minimum turn width, w_{min}.

In the latter case, tolerance (in percentage) for the acceptable inductance values, as well as grid resolution (in micrometer), are needed for successful program completion.

Table 4.4 summarizes the geometry input parameters.

Table 4.4. Geometry parameters for the spiral inductor design.

Parameter	Units	Geometry / inductance known
Outer diameter (d_{out})	µm	Geometry
Inner diameter (d_{in})	µm	Geometry
Turn width (w)	µm	Geometry
Number of turns (n)	-	Geometry
Minimum value of the inner diameter	µm	Inductance
Maximum value of the outer diameter	µm	Inductance
Minimum value for turn spacing (s)	µm	Inductance
Minimum turn width	µm	Inductance
Inductance value tolerance	%	Inductance
Grid resolution	µm	Inductance

4.5.1.2 Process parameters

The inductance value of a high-Q structure is predominantly determined by its geometry. However, the silicon substrate introduces process-dependent parasitics, which are dependent on process parameters. They decrease the Q-factor and add shift to the inductance value. The following substrate parameters need to be specified:

- Thickness of the metal in which the inductor spiral is laid out, t (nm);
- Resistivity of the metal used for the spiral, ρ (Ω·m);
- Permeability of the metal used for the spiral, μ (H/m);
- Thickness of the oxide between the two top metals, t_m (nm);
- Relative permittivity of the oxide between the two top metals, ε_{rm};
- Thickness of the oxide between the substrate and the top metal, t_{sm} (nm);
- Relative permittivity of the oxide between the substrate and the top metal, ε_{rs};
- Thickness of the silicon substrate, t_{Si} (µm);

- Relative permittivity of the silicon substrate, ε_{rSi}; and
- Resistivity of the silicon substrate, ρ_{Si} (Ω·m).

The process parameters are summarized in Table 4.5. AMS S35 process parameters are used later in Chapter 5 for verification by means of simulations.

Table 4.5. Process parameters for the spiral inductor design.

Parameter	Unit
Thickness of metal in which the inductor spiral is laid out	nm
Resistivity of metal used for the spiral (ρ)	Ω·m
Permeability of metal used for the spiral (μ)	H/m
Thickness of oxide between the two top metals (t_m)	nm
Relative permittivity of oxide between the two top metals (ε_{rm})	-
Thickness of oxide between substrate and top metal (t_{sm})	nm
Relative permittivity of oxide between substrate and top metal (ε_{rm})	-
Thickness of the silicon substrate (t_{Si})	µm
Relative permittivity of the silicon substrate (ε_{rSi})	-
Resistivity of the silicon substrate (ρ_{Si})	Ω·m

4.5.1.3 Operating frequency (f_O)

If the inductor is a part of a PA design (this does not need to be the case), the operating frequency is usually the centre frequency of the channel. In other scenarios, operating frequency can be understood as the frequency at which the Q-factor will be highest for a particular geometry.

4.5.2 Subroutine outputs

The inductor design subroutine has both numerical outputs and outputs in the form of text and data files.

4.5.2.1 Numerical outputs

The following quantities are numerical outputs of the inductor design software subroutine:

1. Effective inductance value of the inductor at the operating frequency, L_S (nH);
2. Nominal inductance value of the inductor ($Q \rightarrow \infty$), L_{inf} (nH);
3. Q-factor of the inductor at the operating frequency, Q;
4. Resonant frequency of the inductor, f_r (GHz);
5. Width of the spiral (µm);
6. Spacing between the turns of the spiral (µm);
7. Input diameter of the spiral (µm);
8. Output diameter of the spiral (µm); and

9. Number of turns of the spiral.

4.5.2.2 Text and data file outputs

If required, this subroutine can export the netlist and layout of the designed inductor structure.

The SPICE netlist of the inductor structure, complete with the inductance value and parasititcs calculated for a single-π inductor model, as described in Section 4.5.3 that follows, is saved with a .spc extension. It can be used in SPICE simulations without the need for one to draw the schematic of the inductor with its parasitics in the schematic editor. The netlist is exported in T-Spice format, recognised by most simulators including Cadence Virtuoso.

Layout of the inductor can be exported into Caltech intermediate form (CIF) file or graphic data system (GDS) II file. Both formats contain mask geometry information of the inductor [104, 105]. The GDS II format is the stream format and it is more popular of the two. The stream file is saved with a .gds extension. The CIF file is a text based and it is saved with a .cif extension. Either of the files can be imported into layout software to eliminate the need for one to draw any inductor layout structures.

4.5.3 Description and flow diagrams of inductor design subroutine

The inductor design subroutine consists of two parts. The first part calculates inductance for a given geometry, whereas the second finds geometry that gives the highest Q-factor for a specified inductance.

The first part of the subroutine is a set of calculations that utilizes equations for the single-π inductor model (Section 2.3.2.3). Nominal inductance is calculated by means of the data-fitted monomial equation as specified by Equation (2.32), where coefficients are specified in Table 2.4. Parasitics are calculated utilizing Equations (2.33 – 2.43). Q-factor and resonance frequency are calculated with Equations (2.44 – 2.47). The resulting inductance can be calculated from [89]

$$L_{eff} = \frac{\mathrm{Im}(Z)}{2\pi f_o}, \tag{4.28}$$

where Z is the total impedance of the single-π modelled inductor with its one port grounded.

The second part is a search algorithm that looks into a range of possible geometries and identifies geometry that will result in the required inductance within certain tolerance. While more than one geometry will result in the correct inductance at a given frequency, but each of these geometries will have a different Q-factor. The geometry that gives the highest Q-factor is chosen by the algorithm as its output. The same set of equations (Equations (2.32 – 2.47), (4.28)) is used in the search algorithm. Accuracy of the algorithm depends on the tolerance for the required inductance values and on the search grid resolution. Higher tolerance of the inductance value will result in less accurate inductance values, but there will be a greater probability that inductor geometry resulting in the particular inductance will be found with lower grid resolution. This probability can be increased by increasing the grid resolution, but with the increased grid resolution, the time of execution and memory requirements of the search algorithm will also increase. It is up to users to decide which combination of inductance tolerance and grid resolution will be appropriate for a specific application.

The flow diagram of the inductor design software subroutine is given in Figure 4.8. The search algorithm used to find the geometry when inductance is specified is given in Figure 4.9 [106, 107]. The complete MATLAB code listing for this subroutine, with reference to algorithms for netlist, CIF and GDS file extraction, are given in Figure A.25.

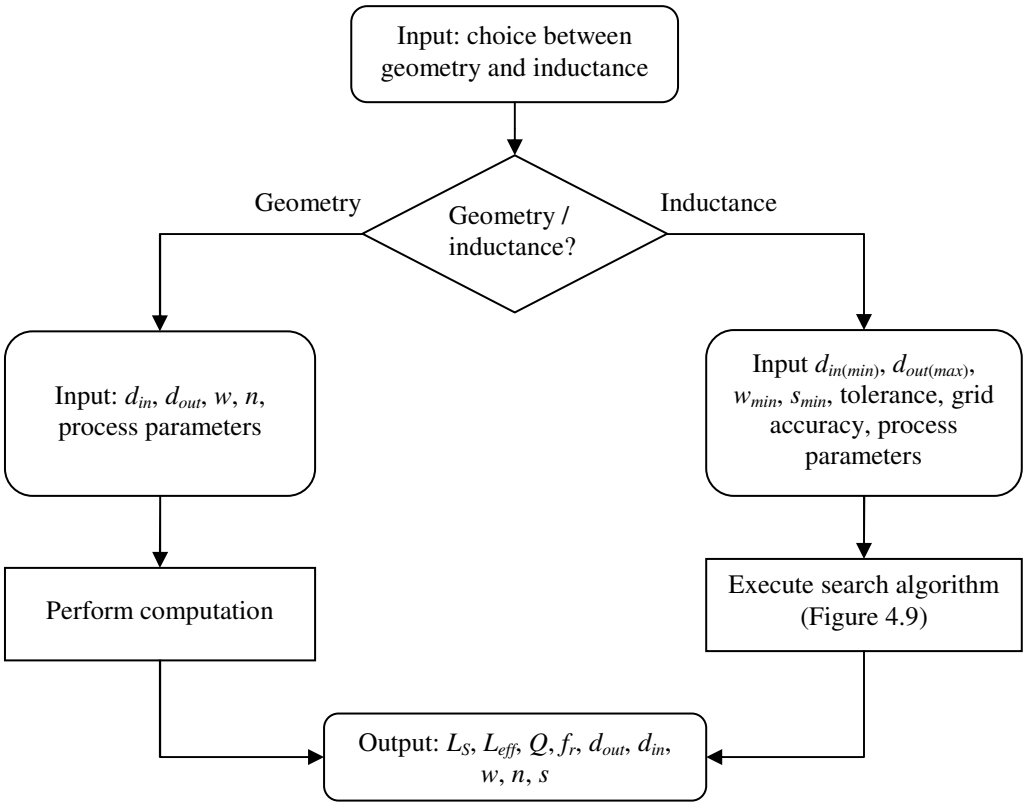


Figure 4.8. Flow diagram of the inductor design subroutine.

4.6 MATCHING AND BIASING AT THE INPUT SIDE OF THE POWER AMPLIFIER

Driving HBTs at large signal levels applicable to PAs present a challenge for performing input impedance matching, because its input impedance behaviour at different power levels and other operating conditions is highly nonlinear [30]. Therefore, the design of the input matching network only becomes possible after extensive simulations have been performed on a specific PA configuration designed with the use of the routine. Various simulations can be used to predict the input impedance and its behaviour under likely operating conditions, and this information can be used in the design of the input matching network. In certain cases, it may even be possible to omit the input matching, if the output impedance of the preceding amplifier stage itself presents a good match.

If large-signal *S*-parameters of the output stage can be found, then method involving two-port networks described in [108] can be utilized to find the input impedance of the stage. Figure 4.9 shows an amplifier as a two-port network. With reference to this figure, reflection coefficient as seen looking towards load is

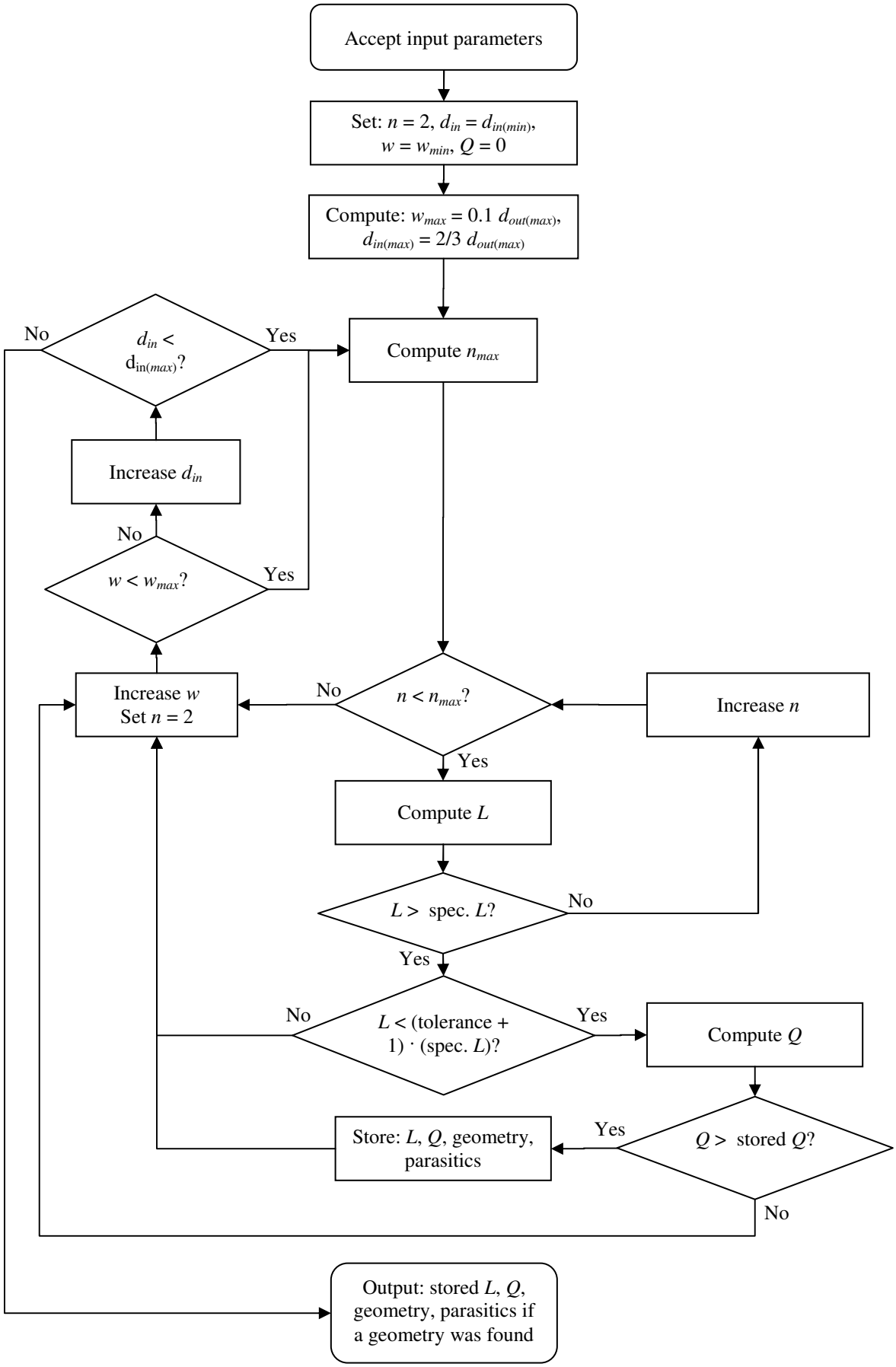


Figure 4.9. Flow diagram of the inductance search algorithm.

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{4.27}$$

where Z_L is the impedance of the load and Z_0 is the characteristic impedance reference used when obtaining the *S*-parameters. Input reflection coefficient of the amplifier in terms of *S*-parameters is

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.28}$$

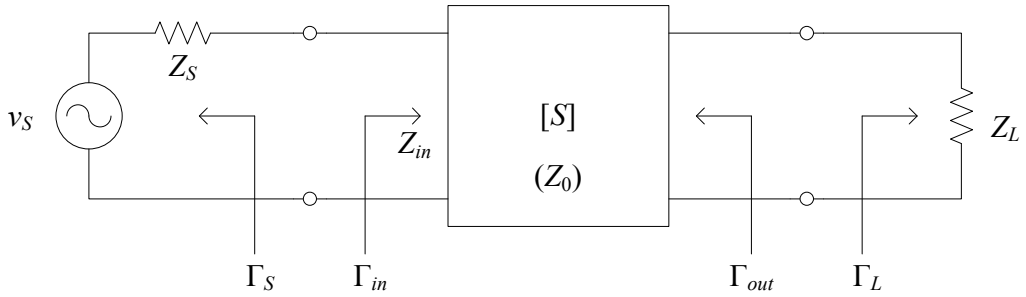


Figure 4.9. A two-port network with the source and load reflection coefficients [108].

For perfect matching at the output amplifier (which will generally be the case) with $Z_0 = Z_L$, Γ_{in} will be equal to S_{11}. Finally,

$$Z_{in} = Z_0 \frac{1 + \Gamma_{in}}{1 - \Gamma_{in}} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{4.29}$$

Matching networks described in Section 4.4.3 can be used to perform the matching. Reactance of Z_{in} is handled either by absorbing it into the matching network, or by resonating it out with equal and opposite reactance [103]. Finally, after the matching is performed, the stability of the amplifier should be ensured [108].

Challenges similar to the ones that arise when doing input impedance matching can be seen with trying to achieve biasing at the input of the PA. It is difficult to predict the exact optimum quiescent point for a PA analytically, so it is found by means of simulations. The DC level of the input drive signal is swept in the region that is identified to contain the optimum bias point, and the correct value is identified. Only once the optimum quiescent point is found, an active or passive biasing network can be utilized.

4.7 COMPLETE SYSTEM INTEGRATION

Methods for designing different PA blocks described in Sections 4.2 to 4.5 are combined into one stand-alone routine [109-111]. This routine can be used to perform the complete Class-E or Class-F stage design, including the output impedance matching and design of all inductors needed in the PA. Quantities, such as operating frequency, needed for more than one sub-routine, are only entered once, which is a distinct advantage of using one complete routine for the design instead of using each of the subroutines separately. Output quantities are displayed sequentially, and they combine most of the separate methods.

4.7.1 Input parameters

All input parameters of the complete routine are summarized in Table 4.6. This table also includes the section number in which the detailed description of each parameter is given.

Table 4.6. Summary of input parameters for the complete PA design routine.

Parameter	Unit	Mandatory / Optional	Section
Centre frequency of the channel (f_o)	MHz	Mandatory	4.2.1, 4.3.1, 4.4.1, 4.5.1.3
Loaded quality factor (Q_L)	-	Mandatory (Class E)	4.2.1
Output power (P_{out})	mW	Mandatory	4.2.1, 4.3.1
Supply voltage (V_{CC})	V	Mandatory	4.2.1, 4.3.1
Collector-emitter saturation voltage (V_{CEsat})	V	Optional (Class E)	4.2.1
Maximum and minimum inductance values (L_{max} and L_{min})	nH	Optional (Class E)	4.2.1
Collector-emitter breakdown voltage (B_{VCE})	V	Optional	4.2.1, 4.3.1
Filtering inductances (L_0, L_3 and L_5)	nH	Mandatory (Class F)	4.3.1
Bandwidth of the matching network (B)	MHz	Mandatory	4.4.1
Minimum value of the inner diameter	µm	Mandatory	4.5.1.1
Maximum value of the outer diameter	µm	Mandatory	4.5.1.1
Minimum value for turn spacing	µm	Mandatory	4.5.1.1
Minimum turn width	µm	Mandatory	4.5.1.1
Inductance value tolerance	%	Mandatory	4.5.1.1
Grid resolution	µm	Mandatory	4.5.1.1
Thickness of metal in which the inductor spiral is laid out	nm	Mandatory	4.5.1.2
Resistivity of metal used for the spiral (ρ)	Ω·m	Mandatory	4.5.1.2
Permeability of metal used for the spiral (μ)	H/m	Mandatory	4.5.1.2
Thickness of oxide between the two top metals (t_m)	nm	Mandatory	4.5.1.2
Relative permittivity of oxide between the two top metals (ε_{rm})	-	Mandatory	4.5.1.2
Thickness of oxide between the substrate and the top metal (t_{sm})	nm	Mandatory	4.5.1.2
Relative permittivity of oxide between the substrate and the top metal (ε_{rm})	-	Mandatory	4.5.1.2
Thickness of the silicon substrate (t_{Si})	µm	Mandatory	4.5.1.2
Relative permittivity of the silicon substrate (ε_{rSi})	-	Mandatory	4.5.1.2
Resistivity of the silicon substrate (ρ_{Si})	Ω·m	Mandatory	4.5.1.2

4.7.2 Routine outputs

Output parameters combine most of the output parameters calculated by separate subroutines. They are summarized in Table 4.7. As in the case of input parameters, the

number of the section in which the parameter is described is also included in the table. For each inductor required by the PA, all relevant inductance parameters are also displayed.

4.7.3 Description and flow diagram of the PA design routine

At the beginning of the execution of the routine, users can chose to perform the design of either a Class-E or a Class-F PA. Depending on the choice, either the Class-E subroutine, described in Section 4.2, or Class-F, described in Section 4.3 is executed. Following this, the users have a choice to perform the output impedance matching to a standard impedance by invoking a subroutine described in Section 4.4. After this, users can choose to design spiral inductors for all inductors (including matching inductors), needed for full PA design. Both 3-metal and thick-metal inductors are designed for each inductor, allowing users to choose the geometry they consider better for a particular application. The inductor search algorithm described in Section 4.5 is used for the inductor design. CIF and GDS II files are not exported here because of a large amount of inductors designed. If needed, the inductor design subroutine can be invoked separately in order to export these files. However, the user is left with the choice to export the netlist of the complete PA system. The netlist includes the matching network and the subcircuits for all spiral inductors, provided that options for impedance matching and spiral inductor design have been selected.

Execution of the complete PA routine is summarized graphically in the flow chart in Figure 4.11. The MATLAB code listing or the main routine invoking all subroutines is given in Figure A.1.

Table 4.7. Output parameters of the PA design routine.

Parameter	Unit	Remark	Section
Optimum load resistance (R_L)	Ω	-	4.2.2, 4.3.2
DC current (I_{DC})	mA	-	4.2.2, 4.3.2
Maximum current (I_{max})	mA	-	4.2.2, 4.3.2
Maximum collector voltage (V_{max})	V	-	4.2.2, 4.3.2
Shunt capacitor (C_1)	pF	Class E	4.2.2
Series capacitor (C_2)	pF	Class E	4.2.2
Inductor (L_2)	nH	Class E	4.2.2
Feed inductor (L_1)	nH or RFC	Class E (Optional)	4.2.2
Shunt capacitor (C_p)	pF	Class E (Optional)	4.2.2
Loaded quality factor which will place inductances within the maximum and minimum values (Q_L)	-	Class E (Optional)	4.2.2
Nominal frequency resonant capacitor (C_0)	pF	Class F	4.3.2
Third-harmonic frequency resonant capacitor (C_3)	pF	Class F	4.3.2
Fifth-harmonic frequency resonant capacitor (C_5)	pF	Class F (Optional)	4.3.2
Output peak current (I_{om})	mA	Class F	4.3.2
Peak output voltage (V_{om})	V	Class F	4.3.2
Matching network inductors and capacitors	nH or pF	L, T and Π networks	4.4.2
Effective inductance value of inductor at operating frequency (L_S)	nH	For each inductor	4.5.2.1
Nominal inductance value of the inductor (L_{inf})	nH	For each inductor	4.5.2.1
Q-factor of the inductor at the operating frequency (Q)	-	For each inductor	4.5.2.1
Resonant frequency of the inductor (f_r)	GHz	For each inductor	4.5.2.1
Width of the spiral	mm	For each inductor	4.5.2.1
Spacing between the turns of the spiral	mm	For each inductor	4.5.2.1
Input diameter of the spiral	mm	For each inductor	4.5.2.1
Output diameter of the spiral	mm	For each inductor	4.5.2.1
Number of turns of the spiral	-	For each inductor	4.5.2.1

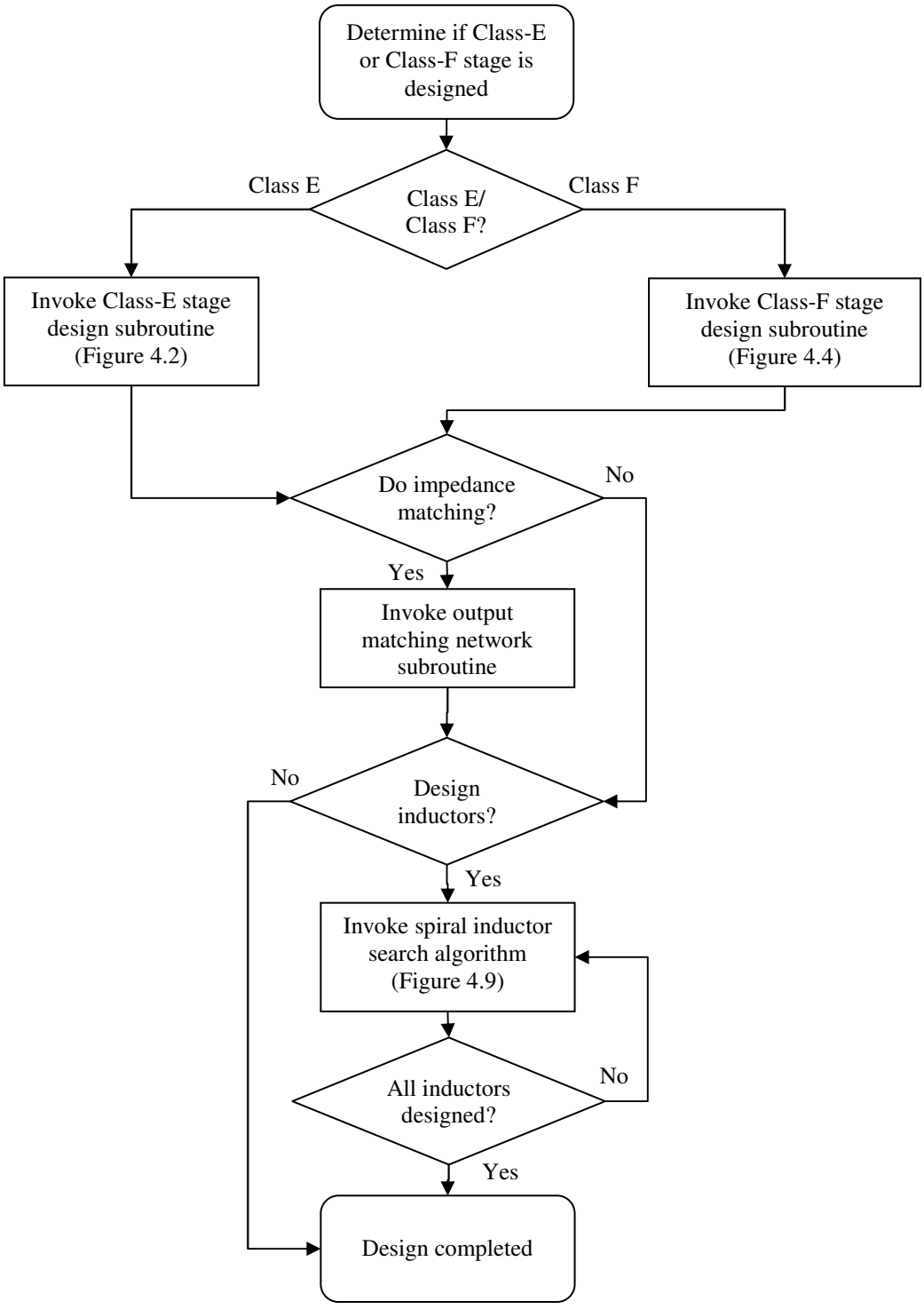


Figure 4.11. Flow chart of the complete PA design routine.

4.8 CONCLUSION

In this chapter, various design methods constituting the PA system level design routine were described. The Class-E and Class-F output stage design subroutines were identified as the starting point in the design of a complete PA system. The output impedance

matching integrated well with the output stage method, and the user could chose between a broadband L-matching network, and narrowband T or Π-matching networks. The search algorithm for spiral inductors was presented as a way to integrate inductors with quality factors as optimal as possible into the PA output stage and the output matching network. For completeness, a separate conventional subroutine that calculates inductance of any square inductor geometry was also revisited in this chapter. Inductor design subroutines were accompanied by SPICE netlist and mask geometry information (CIF and GDS II files) extractors. It has also been discussed that input impedance matching and biasing are not covered by the system level design routine, because of the highly nonlinear and nondeterministic input impedance characteristic of the PA. As an alternative, a method for impedance matching involving *S*-parameter simulation of the complete PA system (excluding input matching and biasing) was proposed and described. Simulation was suggested as a good starting point for the design of the biasing network for the PA as well. In Chapter 5, the design routine developed in this chapter will be used to design several PA systems.

CHAPTER 5 FULL CIRCUIT DESIGN AND SIMULATION

5.1 INTRODUCTION

In Chapter 4, a system level design routine for the PA design has been developed. In Chapter 5, this routine is used to design spiral inductors and PAs, which are then simulated in order to verify the correctness of the routine. Two distinct topics are dealt with in this chapter. The first one aims to demonstrate the correctness of the spiral inductor model used in the routine and the effectiveness of the inductance search algorithm. The second one shows how the system routine is used in the design of the Class-E and Class-F PA systems supported with resonator design and impedance matching. For inductors, the routine is verified by conducting EM simulations of inductors with inductance and Q-factor values predicted by this routine. For the full PA design, the routine is verified by SPICE and RF SPICE simulations of designed circuits. All circuit-level simulations described in this chapter have been performed in S35 0.35 µm SiGe BiCMOS process from AMS, described in Section 3.3.

5.2 VERIFICATION OF THE SPIRAL INDUCTOR MODEL AND THE INDUCTANCE SEARCH ALGORITHM

As discussed earlier in this thesis, an accurate spiral inductor modelling is paramount for a good PA design. This is why it was important to verify accuracy of the spiral inductor model used in the inductor search algorithm (Section 4.5).

The inductance search algorithm was used to design ten 3M and ten TM inductors fabricated over a standard resistivity substrate at common frequencies of 1, 2, 2.4 and 5 GHz. The smallest inductor value designed for was 0.5 nH, followed by nine inductors in increments of 0.5 nH. Table 5.1 and Table 5.2 show geometric parameters, LF inductance values and the Q-factor of each designed 3M and TM inductor respectively. To verify the predicted values, EM simulation on the designed inductors was performed by means of the EM simulator described in Section 3.5.3. Process files needed for EM simulations for both 3M and TM inductors are given in Figures B.1 and B.2 in Appendix B. The inductance and Q-factor values resulting from EM simulations are also shown in Table 5.1 and Table 5.2.

The comparisons of inductances and Q-factors of all forty inductors designed in this manner are shown graphically in Figures 5.4 through 5.19. This set of figures shows a very good correspondence between two ways of obtaining data in case of inductance values. This shows that inductance values obtained using the inductor model in the inductor design part of the PA design routine accurately predicts actual inductance values.

Good correspondence between the two in terms of Q-factor values exists for 3M inductors, whereas in the case of TM inductors, the graphs of calculated and EM simulated values take similar shape, with simulated Q-factors being larger than those of the calculated Q-factors. This discrepancy can be explained: as the impedance of parasitic elements in the RL model of the spiral (with oxide and substrate effects ignored) approaches that of inductive reactance near the peak frequency, the model yields a pessimistic estimate of the actual Q-factor of the spiral [101]. 3M inductors lie closer to the substrate and have larger resistances than TM inductors, so this effect is less prominent. The fact that the Q-factor is underestimated rather than overestimated can be used to an advantage, since the TM inductors designed by the inductor calculator will perform better than predicted, which will be acceptable in many cases.

Table 5.1. Metal-3 inductors designed with inductance search algorithm.

Frequency (GHz)	Nominal inductance (nH)	Calculated LF inductance (nH)	Calculated Q	EM inductance (nH)	EM Q	d_{out} (μm)	d_{in} (μm)	w (μm)	s (μm)	n
1	0.5	0.50	3.37	0.50	3.00	220	30	47	1	2
1	1	1.00	4.63	0.94	4.15	291	93	49	1	2
1	1.5	1.48	5.22	1.40	4.75	347	149	49	1	2
1	2	1.95	5.47	1.90	5.11	397	199	49	1	2
1	2.5	2.39	5.50	2.33	2.33	441	243	49	1	2
1	3	2.83	5.39	2.75	5.27	483	285	49	1	2
1	3.5	3.29	5.10	3.22	3.22	500	326	43	1	2
1	4	3.67	4.80	3.52	4.52	426	164	43	1	3
1	4.5	4.12	4.66	3.97	4.56	427	189	39	1	3
1	5	4.55	4.60	4.52	4.41	431	211	36	1	3
2	0.5	0.49	5.79	0.45	4.29	210	32	55	1	2
2	1	0.97	7.16	0.91	5.92	288	90	49	1	2
2	1.5	1.41	6.89	1.32	6.11	339	141	49	1	2
2	2	1.86	6.24	1.73	6.23	349	191	39	1	2
2	2.5	2.32	5.64	2.26	5.68	363	233	32	1	2
2	3	2.76	5.12	2.72	5.27	384	270	28	1	2
2	3.5	3.21	4.81	3.01	5.33	276	152	20	1	3
2	4	3.65	4.53	3.45	5.19	283	171	18	1	3
2	4.5	4.06	4.27	3.86	4.98	294	188	17	1	3
2	5	4.51	4.05	4.35	4.76	241	123	14	1	4
2.4	0.5	0.49	6.72	0.45	4.94	216	30	46	1	2
2.4	1	0.95	7.63	0.90	6.38	286	88	49	1	2
2.4	1.5	1.39	6.95	1.34	6.34	316	142	43	1	2
2.4	2	1.86	6.18	1.82	6.25	320	190	32	1	2
2.4	2.5	2.30	5.51	2.26	5.47	339	229	27	1	2
2.4	3	2.76	5.04	2.71	5.32	249	131	19	1	3
2.4	3.5	3.17	4.69	3.12	4.89	262	150	18	1	3
2.4	4	3.61	4.39	3.59	4.74	262	168	15	1	3
2.4	4.5	4.03	4.12	4.03	4.60	220	110	13	1	4
2.4	5	4.47	3.91	4.50	4.55	216	122	11	1	4
5	0.5	0.47	9.48	0.41	6.05	200	30	42	1	2
5	1	0.92	8.22	0.88	6.93	209	95	28	1	2
5	1.5	1.36	6.76	1.34	5.88	222	140	20	1	2
5	2	1.81	5.71	1.80	5.48	169	87	13	1	3
5	2.5	2.22	5.03	2.20	5.15	176	106	11	1	3
5	3	2.60	4.46	2.59	4.45	186	122	10	1	3
5	3.5	2.97	4.02	2.96	4.03	160	82	9	1	4
5	4	3.46	3.70	3.52	4.43	148	94	6	1	4
5	4.5	3.98	3.43	4.07	4.30	141	103	4	1	4
5	5	4.29	3.27	4.42	4.24	106	38	4	1	7

Table 5.2. Thick-metal inductors designed with inductance search algorithm.

Frequency (GHz)	Nominal inductance (nH)	Calculated LF inductance (nH)	Calculated Q	EM inductance (nH)	EM Q	d_{out} (μm)	d_{in} (μm)	w (μm)	s (μm)	n
1	0.5	0.50	7.43	0.38	4.71	216	30	48	2	2
1	1	0.99	10.1	0.93	8.13	299	95	50	2	2
1	1.5	1.47	11.1	1.39	9.96	355	151	50	2	2
1	2	1.95	11.5	1.84	11.1	406	202	50	2	2
1	2.5	2.39	11.4	2.30	11.7	451	247	50	2	2
1	3	2.81	10.9	2.70	12.0	493	289	50	2	2
1	3.5	3.29	10.3	3.20	11.6	499	331	41	2	2
1	4	3.71	9.78	3.49	9.62	403	173	37	2	3
1	4.5	4.17	9.49	3.95	9.89	409	197	34	2	3
1	5	4.60	9.21	4.40	9.99	418	218	32	2	3
2	0.5	0.49	11.4	0.43	9.17	222	30	47	2	2
2	1	0.96	13.0	0.88	13.4	295	91	50	2	2
2	1.5	1.42	11.9	1.35	14.6	316	148	41	2	2
2	2	1.88	10.8	1.82	14.2	324	196	31	2	2
2	2.5	2.33	9.80	2.27	13.8	348	236	37	2	2
2	3	2.79	9.08	2.66	11.6	268	134	21	2	3
2	3.5	3.21	8.55	3.10	11.6	276	154	19	2	3
2	4	3.64	8.05	3.54	11.6	283	173	17	2	3
2	4.5	4.09	7.59	3.96	11.4	294	190	16	2	3
2	5	4.49	7.25	4.39	10.3	240	124	13	2	4
2.4	0.5	0.49	12.4	0.43	10.7	219	31	46	2	2
2.4	1	0.94	13.0	0.86	14.4	286	90	48	2	2
2.4	1.5	1.41	11.6	1.36	15.3	289	149	34	2	2
2.4	2	1.88	10.3	1.83	14.7	302	194	26	2	2
2.4	2.5	2.34	9.25	2.24	11.8	229	113	18	2	3
2.4	3	2.78	8.61	2.69	12.0	238	134	16	2	3
2.4	3.5	3.18	8.01	3.08	12.0	256	152	16	2	3
2.4	4	3.63	7.47	3.56	11.7	256	170	13	2	3
2.4	4.5	4.54	7.04	4.00	10.6	213	113	11	2	4
2.4	5	4.46	6.67	4.36	10.6	223	123	11	2	4
5	0.5	0.47	14.4	0.41	17.3	200	32	41	2	2
5	1	0.93	12.1	0.89	18.9	199	99	24	2	2
5	1.5	1.38	9.83	1.35	17.0	215	143	17	2	2
5	2	1.82	9.37	1.74	14.0	163	89	11	2	3
5	2.5	2.26	7.31	2.18	13.5	170	108	9	2	3
5	3	2.70	6.74	2.62	10.6	123	47	6	2	5
5	3.5	3.09	6.23	3.04	12.0	182	138	6	2	3
5	4	3.42	5.88	3.32	10.4	137	61	6	2	5
5	4.5	3.79	5.44	3.70	10.8	163	103	6	2	4
5	5	4.07	5.02	3.98	9.65	149	73	6	2	5

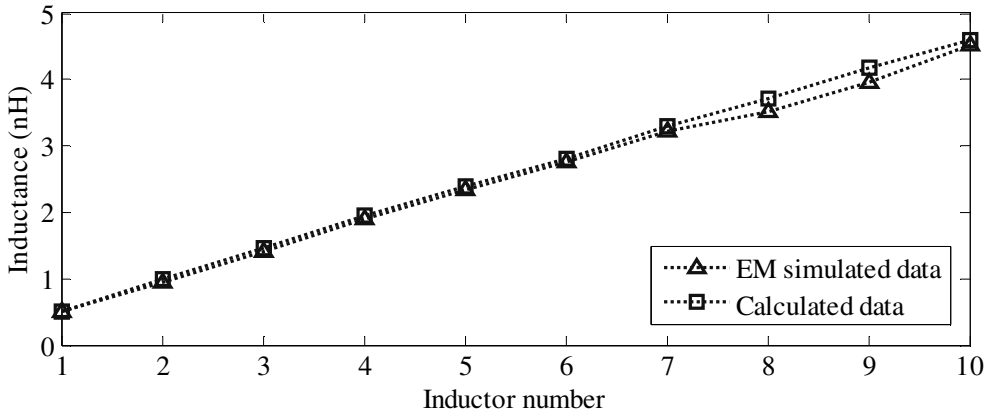


Figure 5.1. Inductance of 1 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

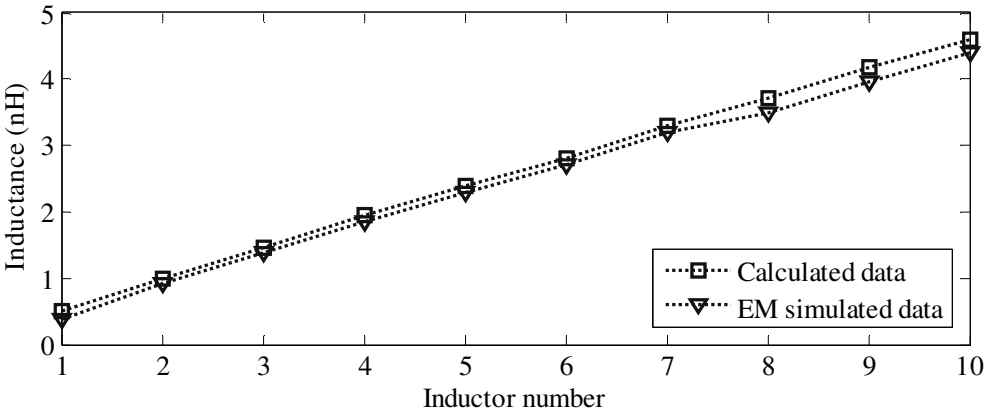


Figure 5.2. Inductance of 1 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

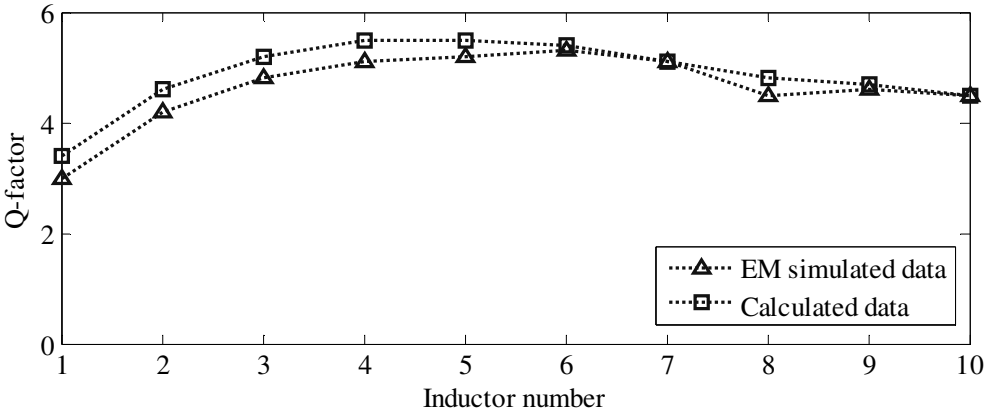


Figure 5.3. Q-factor of 1 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

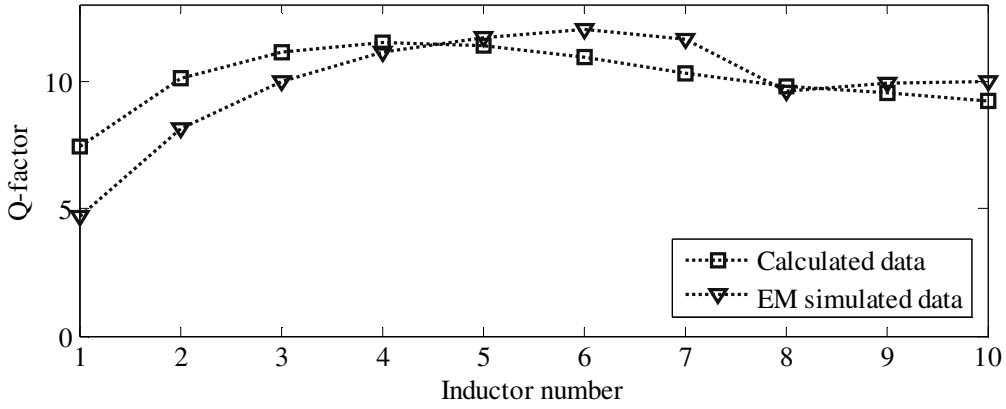


Figure 5.4. Q-factor of 1 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

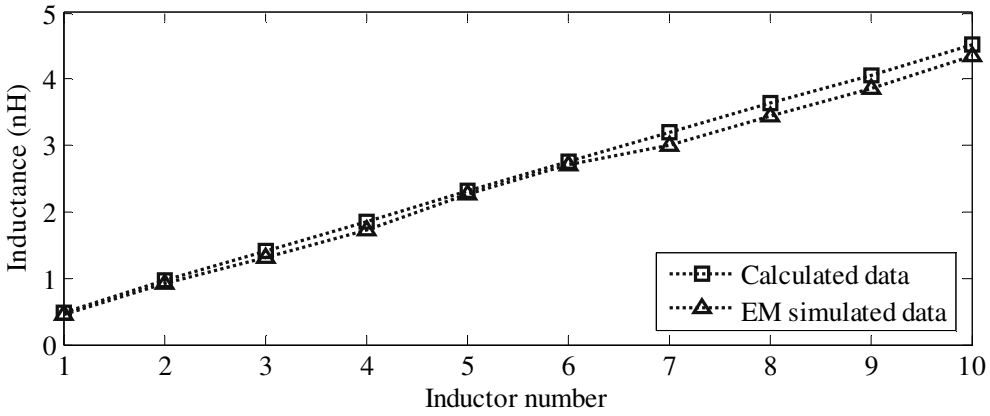


Figure 5.5. Inductance of 2 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

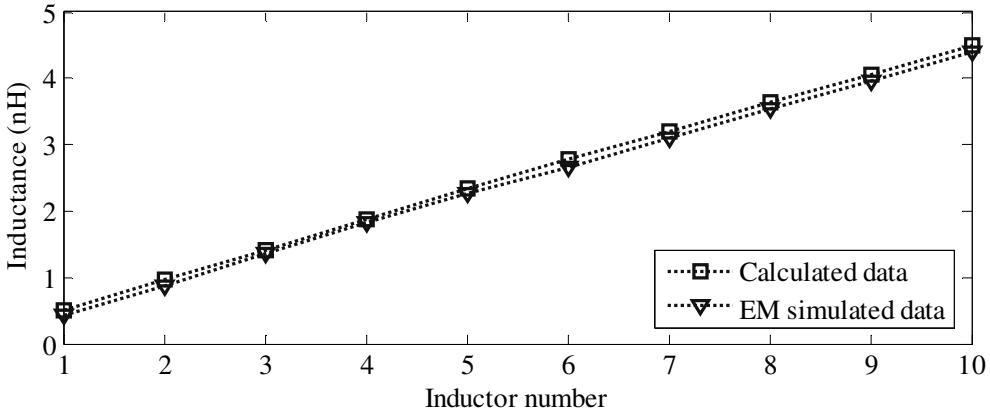


Figure 5.6. Inductance of 2 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

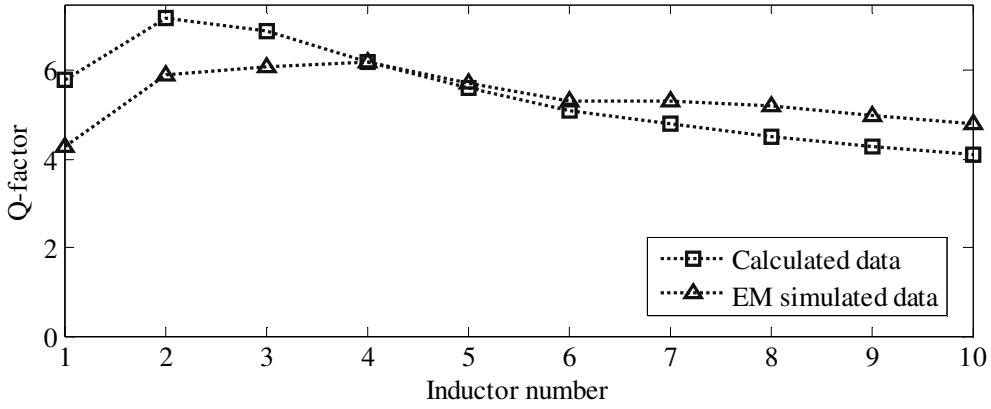


Figure 5.7. Q-factor of 2 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

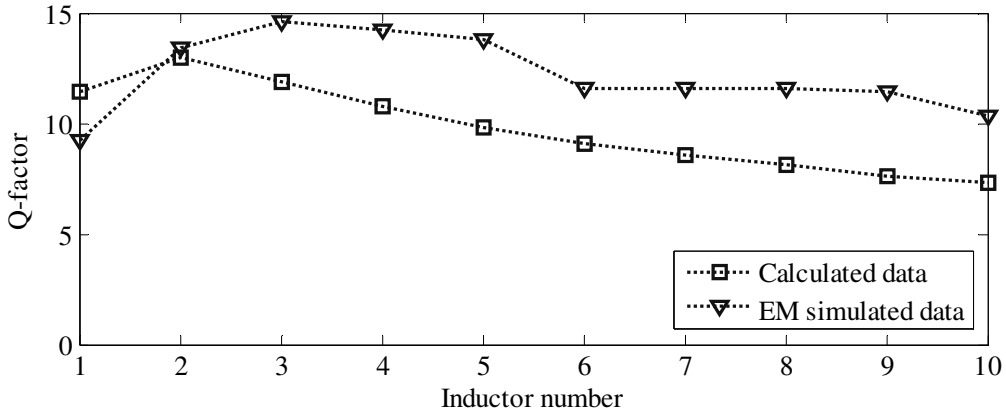


Figure 5.8. Q-factor of 2 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

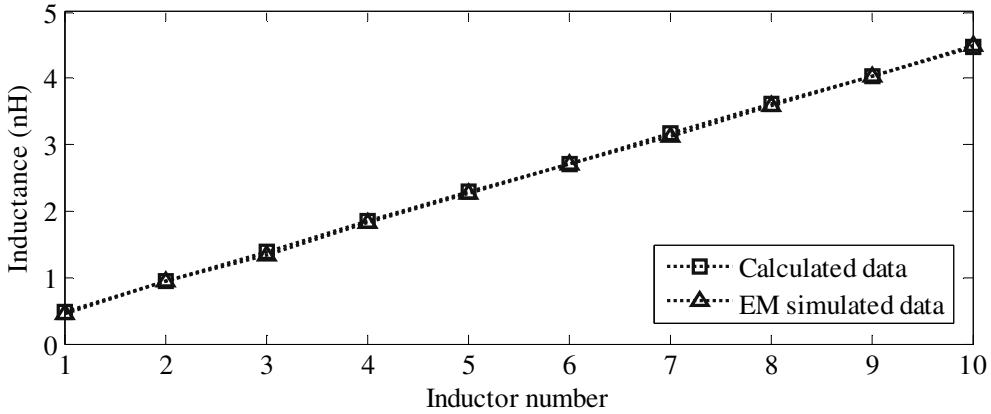


Figure 5.9. Inductance of 2.4 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

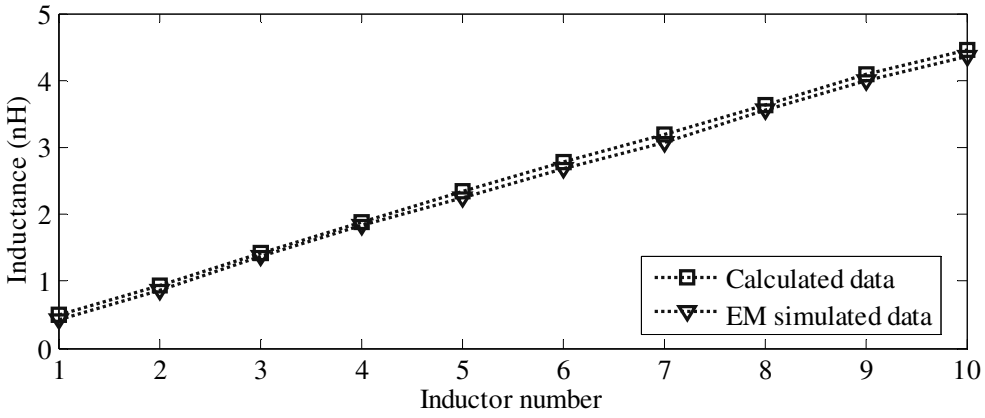


Figure 5.10. Inductance of 2.4 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

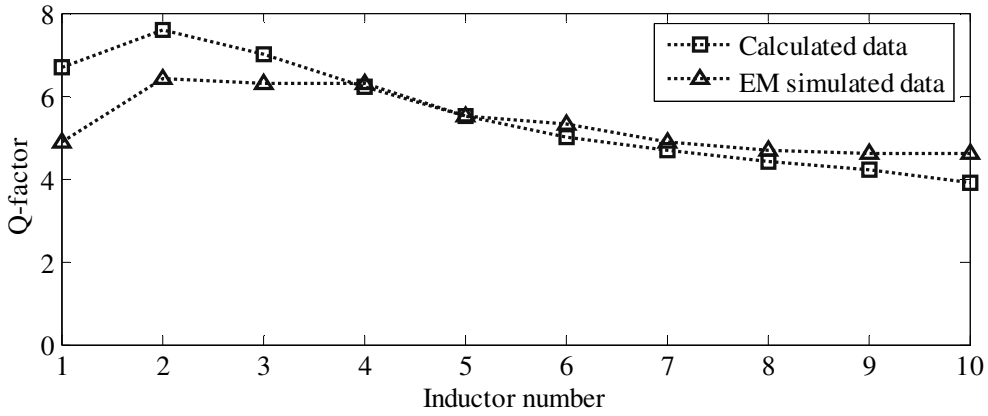


Figure 5.11. Q-factor of 2.4 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

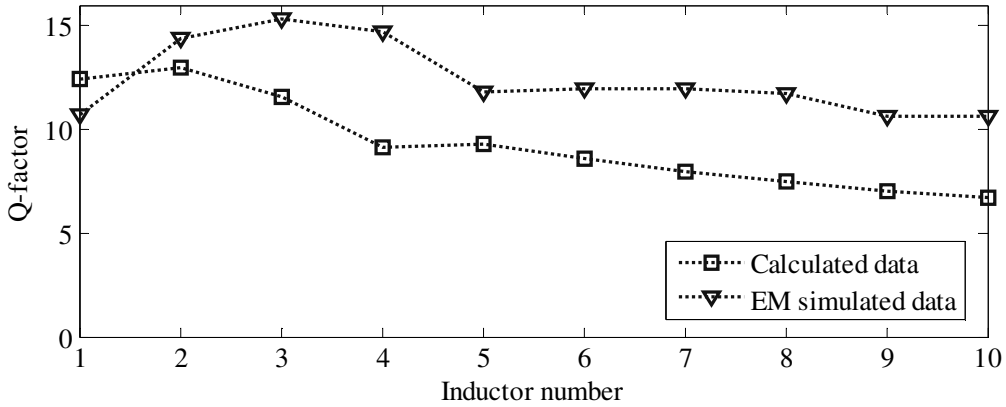


Figure 5.12. Q-factor of 2.4 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

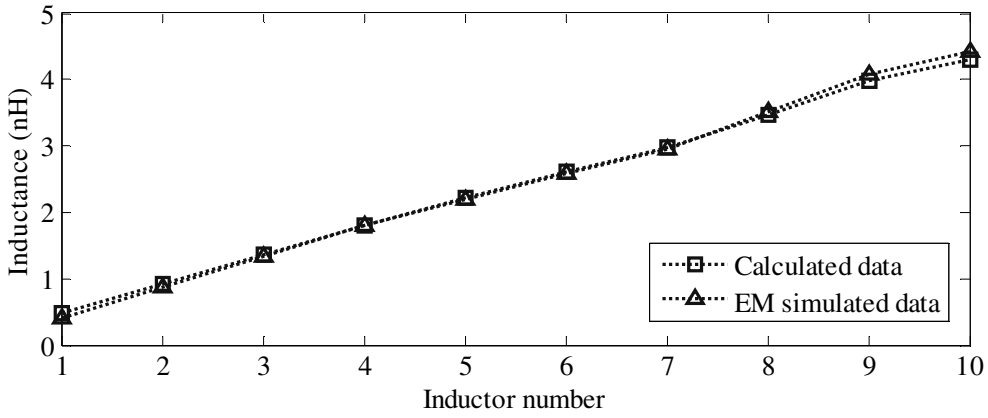


Figure 5.13. Inductance of 5 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

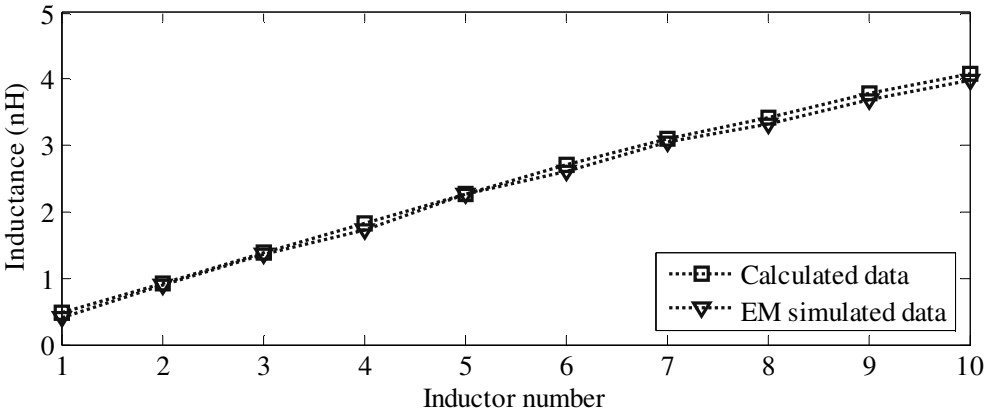


Figure 5.14. Inductance of 5 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

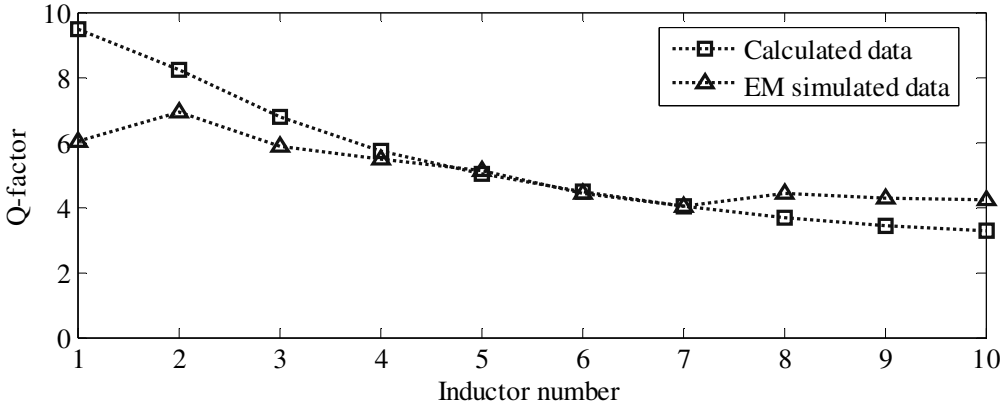


Figure 5.15. Q-factor of 5 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

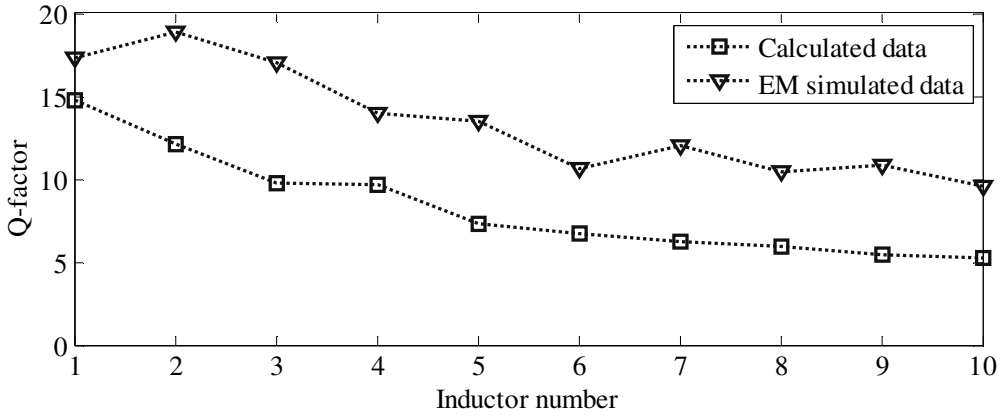


Figure 5.16. Q-factor of 5 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

5.3 VERIFICATION OF THE FULL SYSTEM INTEGRATION ROUTINE

In order to verify the completeness of the full system integration routine, the routine was used to design two Class-E and two Class-F PAs intended for the 2.4 GHz ISM band. Basic simulations were performed on each of four configurations to determine a better one for each Class-E and Class-F PA. Chosen configurations were then designed and simulated further, to include biasing and matching networks, to make the full PA systems layout-ready. Each of the Class-E and Class-F stages is treated in a separate section.

5.3.1 Lower power Class-E configuration

5.3.1.1 Design

The first designed configuration was the lower power Class-E configuration. Aimed output power was 25 mW, or 14 dBm, with the loaded quality factor of 5. HS HBT npn254 transistor with total emitter length of 96 μm was chosen for the design to obtain maximum available gain. The supply voltage of 0.5 V was taken as a safe operating voltage. It was assumed that it would be possible to connect 100 nH RFC externally to the IC. Matching bandwidth of 500 MHz was taken as reasonable should Π or T-network be implemented in the design. The chosen design parameters, as well as component values calculated by the design routine, are shown in Table 5.3.

Table 5.3. Chosen and calculated parameters for the design of the lower power Class-E PA.

Parameter	Value	Unit
Centre frequency (f_o)	2.4	GHz
Loaded quality factor (Q_L)	5	-
Aimed output power (P_{out})	25	mW
Supply voltage (V_{CC})	0.5	V
Matching bandwidth (BW)	500	MHz
RFC (L_1)	100	nH
Required load resistance (R_L)	5.77	Ω
Series inductance (L_2)	1.91	nH
Series capacitance (C_2)	3.42	pF
Shunt capacitance (C_1)	2.11	pF
DC current (I_{DC})	49.97	mA
Peak collector voltage (v_{Cp})	1.78	V
Peak collector current (i_{sp})	143	mA
L-network matching inductance (L_M)	1.2	nH
L-network matching capacitance (C_M)	4.15	pF
Ind-cap-ind T-network matching inductance 1 (L_{M1})	1.837	nH
Ind-cap-ind T-network matching capacitance 1 (C_{M1})	2.932	pF
Ind-cap-ind T-network matching inductance 2 (L_{M2})	4.417	nH
Cap-ind-cap T-network matching capacitance 1 (C_{M1})	2.964	pF
Cap-ind-cap T-network matching inductance 1 (L_{M1})	1.500	nH
Cap-ind-cap T-network matching capacitance 2 (C_{M2})	0.996	pF
Ind-cap-ind Π-network matching inductance 1 (L_{M1})	0.287	nH
Ind-cap-ind Π-network matching capacitance 1 (C_{M1})	5.200	pF
Ind-cap-ind Π-network matching inductance 2 (L_{M2})	0.691	nH
Cap-ind-cap Π-network matching capacitance 1 (C_{M1})	15.309	pF
Cap-ind-cap Π-network matching inductance 1 (L_{M1})	0.846	nH
Cap-ind-cap Π-network matching capacitance 2 (C_{M2})	6.366	nH

To complete the design, L-network matching was chosen and 3M inductors were selected for the implementation of inductors L_2 (named M30191N) and L_M (named M30120N). Table 5.4 shows geometry and Q-factors for the two inductors found by the inductance search algorithm. The exported netlist of the whole PA design is shown in Figure 5.17.

Table 5.4. Computed 3M inductor parameters for the lower power Class-E design.

Parameter	Value (M30191N)	Value (M30120N)	Unit
Inductance at 2.4 GHz (L_S)	1.92	1.20	nH
Inductance at DC (L_{SLF})	1.78	1.12	nH
Q-factor (Q)	6.18	7.31	-
Resonant frequency (f_R)	8.19	8.59	GHz
Turn width (w)	33.0	50.0	µm
Turn spacing (s)	2.00	2.00	µm
Inner diameter (d_{in})	186	110	µm
Outer diameter (d_{out})	322	314	µm
Number of turns (n)	2	2	-

```
.SUBCKT L2 L1 L2 GND
CS L1 L2 77.10fF
LS N4 L1 1.78n
RS N4 L2 2.59
Csi1 N2 GND 78.38fF
Csi2 N3 GND 78.38fF
Cox1 L1 N2 355.85fF
Cox2 L2 N3 355.85fF
Rsi1 N2 GND 269.76
Rsi2 N3 GND 269.76
.ENDS

.SUBCKT LM L1 L2 GND
CS L1 L2 177.00fF
LS N4 L1 1.12n
RS N4 L2 1.50
Csi1 N2 GND 75.61fF
Csi2 N3 GND 75.61fF
Cox1 L1 N2 448.95fF
Cox2 L2 N3 448.95fF
Rsi1 N2 GND 279.04
Rsi2 N3 GND 279.04
.ENDS

.SUBCKT class-E-1 bias supply Gnd
LRFC_2 supply N_2 100.00n
XL2_1 N_5 N_M1 Gnd L2
RResistor_1 N_M2 Gnd 50.00 TC=0.0, 0.0
Xnpn254_1 N_2 bias Gnd Gnd npn254 area=96
CCapacitor_1 N_2 Gnd 2.11p
CCapacitor_2 N_2 N_5 3.42p
XLM_1 Gnd N_M2 Gnd LM
CCapacitor_M N_M1 N_M2 4.15p
.ENDS
```

Figure 5.17. Exported netlist of the lower power Class-E design.

5.3.1.2 Simulation

Figure 5.18 shows the circuit diagram of the PA system, with ideal sources used for power supply and drive voltages.

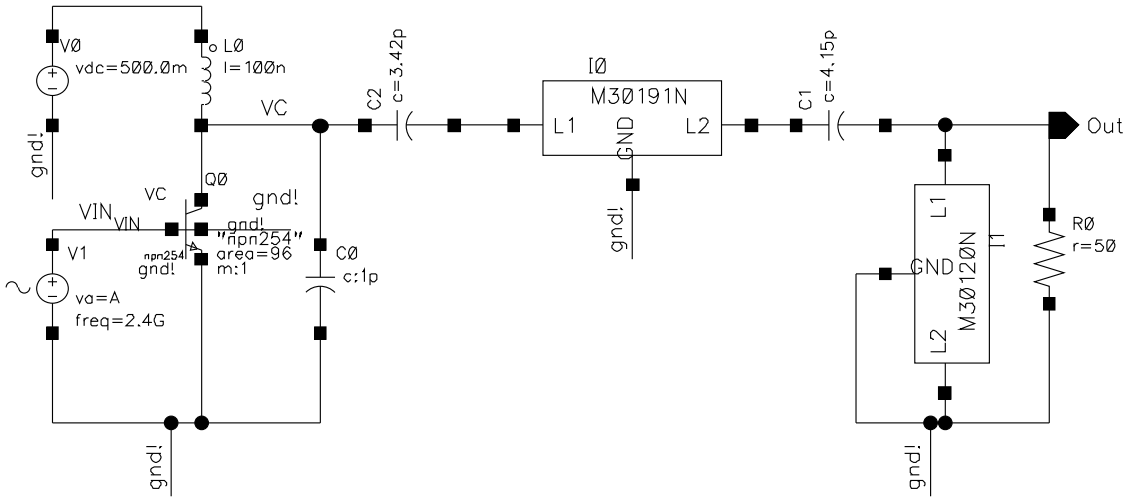


Figure 5.18. Circuit diagram of the lower power Class-E PA design.

The frequency domain simulation of the PA including the collector voltage waveform and output voltage waveform is shown in Figure 5.19. Biasing point of the drive voltage was

determined by sweeping the DC voltage across the base of the transistor. The biasing voltage was swept around typical V_{BE} voltage of the HBT, so that near-to-Class-B biasing could be established with maximum output voltage. The results of the sweep pertaining to the output voltage waveform are shown in Figure 5.20. From this figure it was clear that the biasing voltage of about 0.88 V gave best results. The time domain simulation of all relevant voltage and current waveforms after the optimum biasing point was established is shown in Figure 5.21 and Figure 5.22.

From Figure 5.21 and Figure 5.22, it can be seen that the peak-to-peak output voltage over 50 Ω load is 1.21 V and the DC current consumption is 34.0 mA. This results in collector efficiency of the stage of 21 % with output power of only 3.64 mW (5.61 dBm). As expected, the output specification of the stage was not reached, due to nonideal inductors and the fact that the HBT does not act as an ideal switch. The same set of simulations was performed on the same system using ideal inductors, resulting in an output power of 7.84 dBm, and showing that 2.23 dBm decrease in output power can be directly attributed to low quality inductors.

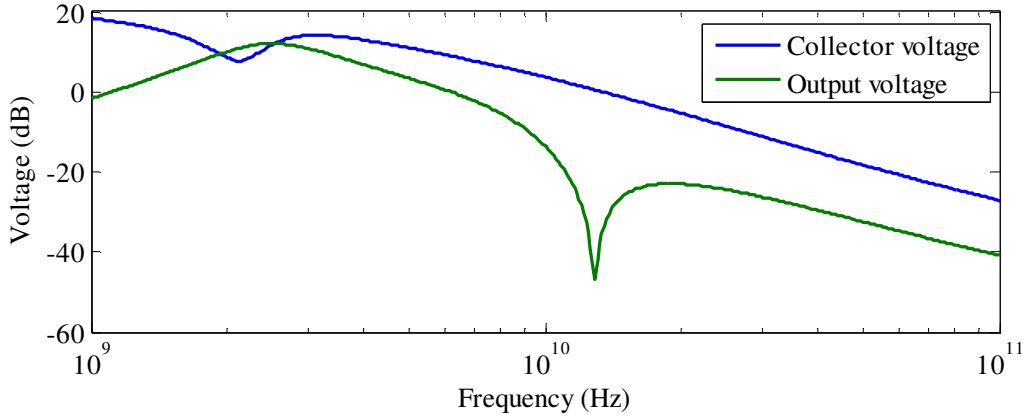


Figure 5.19. Frequency response of the lower power Class-E design.

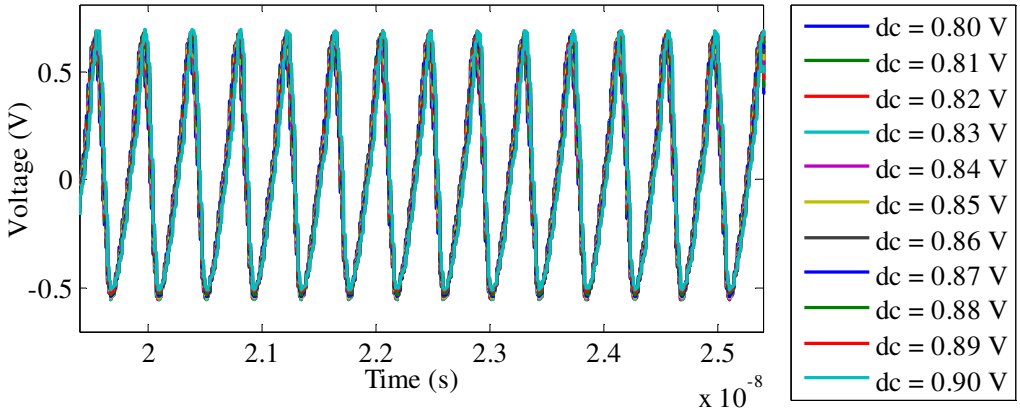
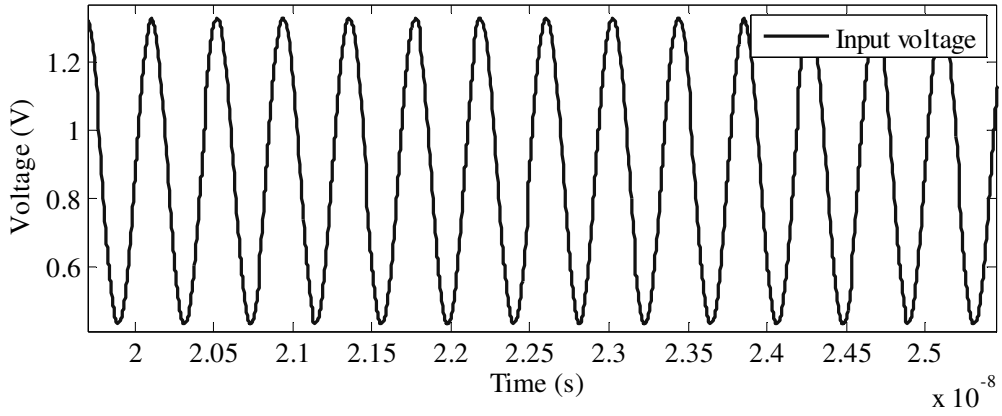
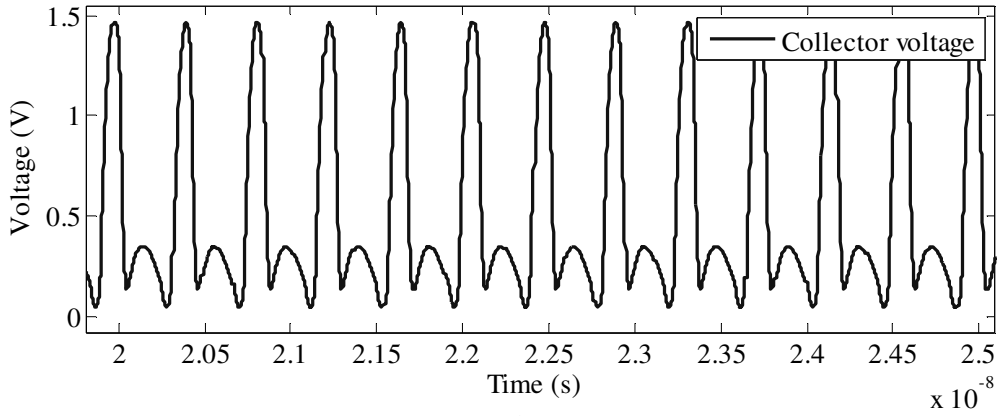


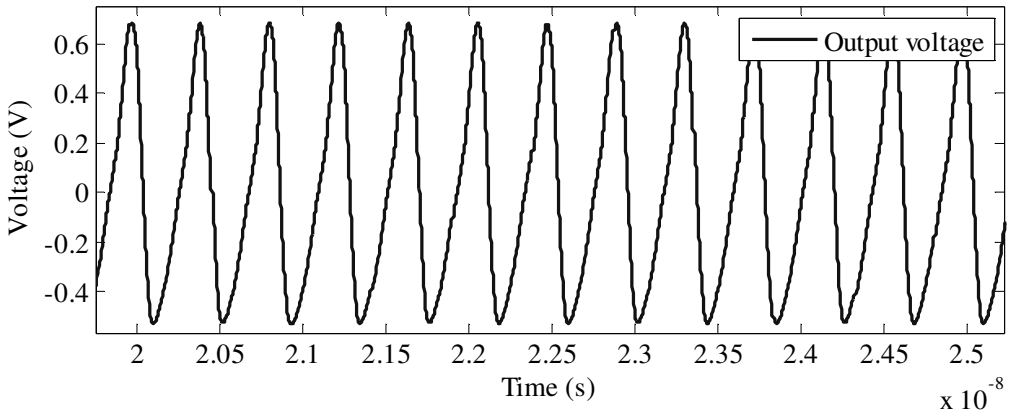
Figure 5.20. DC sweep of the input biasing voltage of the lower power Class-E design with output voltage waveform as the output.



(a)



(b)



(c)

Figure 5.21. Transient response of (a) input voltage, (b) collector voltage and (c) output voltage waveforms of the lower power Class-E design.

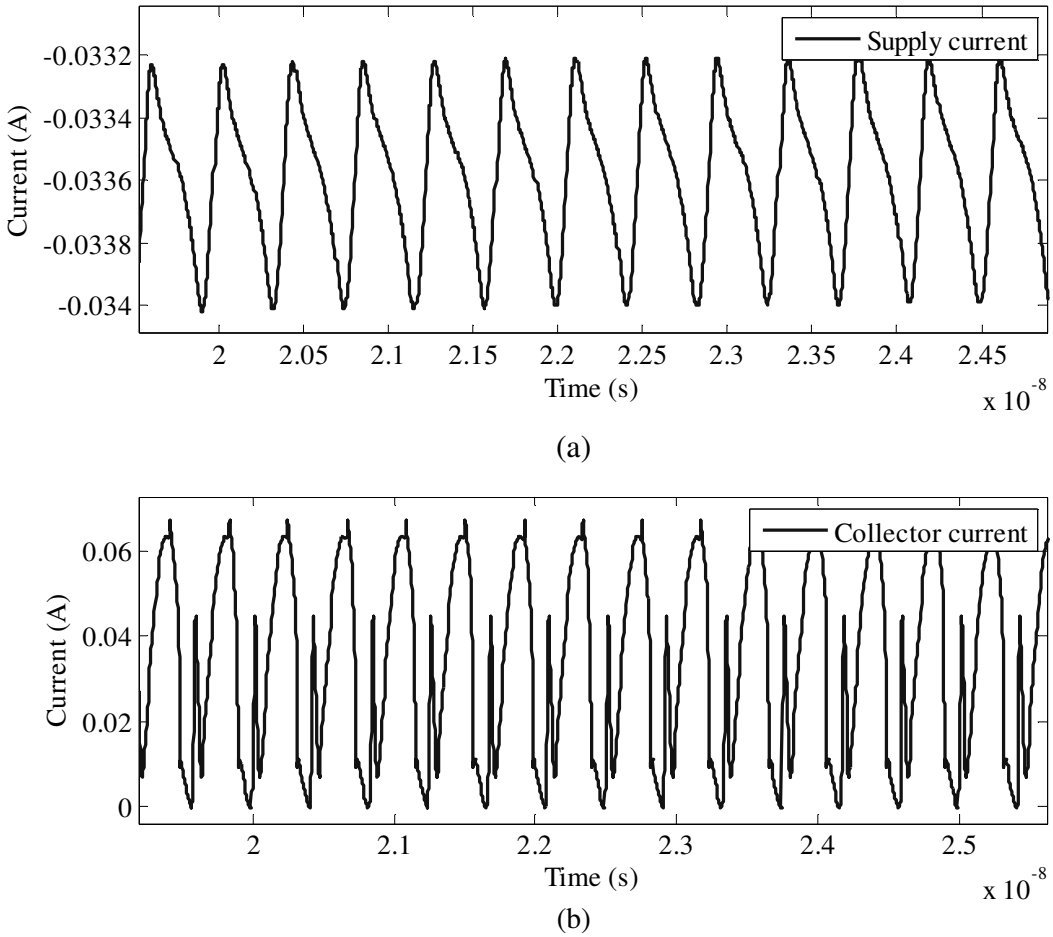


Figure 5.22. Transient response of (a) supply current and (b) collector current waveforms of the lower power Class-E design.

5.3.2 Higher power Class-E configuration

5.3.2.1 Design

The second designed configuration was the higher power Class-E configuration. Aimed output power was 50 mW, or 17 dBm, again with the loaded quality factor of 5. HV HBT npn254h5 transistor with total emitter length of 96 μm was chosen for this design. Although its frequency response at 2.4 GHz frequency is somewhat inferior to that of its HS counterpart, its inclusion allowed for the higher supply voltage of 1 V to be used. External RFC of 100 nH was used again, and the matching bandwidth of 1 GHz was observed to result in reasonable component values for the Π or T network. The chosen design parameters, as well as component values calculated by the design routine, are shown in Table 5.5.

Table 5.5. Chosen and calculated parameters for the design of the higher power Class-E PA.

Parameter	Value	Unit
Centre frequency (f_o)	2.4	GHz
Loaded quality factor (Q_L)	5	-
Aimed output power (P_{out})	50	mW
Supply voltage (V_{CC})	1	V
Matching bandwidth (BW)	1	GHz
RFC (L_1)	100	nH
Required load resistance (R_L)	11.5	Ω
Series inductance (L_2)	3.83	nH
Series capacitance (C_2)	1.71	pF
Shunt capacitance (C_1)	1.05	pF
DC current (I_{DC})	49.97	mA
Peak collector voltage (v_{Cp})	3.56	V
Peak collector current (i_{sp})	143	mA
L-network matching inductance (L_M)	1.82	nH
L-network matching capacitance (C_M)	3.15	pF
Ind-cap-ind T-network matching inductance 1 (L_{M1})	1.837	nH
Ind-cap-ind T-network matching capacitance 1 (C_{M1})	2.676	pF
Ind-cap-ind T-network matching inductance 2 (L_{M2})	2.482	nH
Cap-ind-cap T-network matching capacitance 1 (C_{M1})	2.394	pF
Cap-ind-cap T-network matching inductance 1 (L_{M1})	1.643	nH
Cap-ind-cap T-network matching capacitance 2 (C_{M2})	1.172	pF
Ind-cap-ind Π-network matching inductance 1 (L_{M1})	1.022	nH
Ind-cap-ind Π-network matching capacitance 1 (C_{M1})	2.848	pF
Ind-cap-ind Π-network matching inductance 2 (L_{M2})	1.382	nH
Cap-ind-cap Π-network matching capacitance 1 (C_{M1})	4.301	pF
Cap-ind-cap Π-network matching inductance 1 (L_{M1})	1.544	nH
Cap-ind-cap Π-network matching capacitance 2 (C_{M2})	3.183	nH

To complete the design, the capacitor-inductor-capacitor Π-network matching was chosen and TM-inductors were selected for the implementation of inductors L_2 (named M40383N) and L_{M1} (named M40154N). Table 5.6 shows the geometry and Q-factors for the two inductors as found by the inductance search algorithm. The exported netlist of the whole PA design is shown in Figure 5.23.

Table 5.6. Computed TM-inductor parameters for the higher power Class-E design.

Parameter	Value (M40383N)	Value (M40154N)	Unit
Inductance at 2.4 GHz (L_S)	3.83	1.55	nH
Inductance at DC (L_{SLF})	3.47	1.45	nH
Q-factor (Q)	7.66	11.5	-
Resonant frequency (f_R)	7.46	9.39	GHz
Turn width (w)	14.0	34.0	µm
Turn spacing (s)	2.00	2.00	µm
Inner diameter (d_{in})	164	110	µm
Outer diameter (d_{out})	256	314	µm
Number of turns (n)	2	2	-

```
.SUBCKT L2 L1 L2 GND
CS L1 L2 20.82fF
LS N4 L1 3.47n
RS N4 L2 3.81
Csi1 N2 GND 79.47fF
Csi2 N3 GND 79.47fF
Cox1 L1 N2 165.21fF
Cox2 L2 N3 165.21fF
Rsi1 N2 GND 266.94
Rsi2 N3 GND 266.94
.ENDS

.SUBCKT LM6 L1 L2 GND
CS L1 L2 81.84fF
LS N4 L1 1.45n
RS N4 L2 1.15
Csi1 N2 GND 70.03fF
Csi2 N3 GND 70.03fF
Cox1 L1 N2 236.82fF
Cox2 L2 N3 236.82fF
Rsi1 N2 GND 301.87
Rsi2 N3 GND 301.87
.ENDS

.SUBCKT Class-E-2 bias supply Gnd
LRFC_2 supply N_2 100.00n
XL2_1 N_5 N_M1 Gnd L2
RResistor_1 N_M2 Gnd 50.00 TC=0.0, 0.0
Xnpn254_1 N_2 bias Gnd Gnd npn254h5 area=96
CCapacitor_1 N_2 Gnd 1.05p
CCapacitor_2 N_2 N_5 1.71p
CCapacitor_M1 Gnd N_M1 4.30p
CCapacitor_M2 Gnd N_M2 3.18p
XLM6_1 N_M1 N_M2 Gnd LM6
.ENDS
```

Figure 5.23. Exported netlist of the higher power Class-E design.

5.3.2.2 Simulation

Figure 5.24 shows the circuit diagram of the PA system, with ideal sources used for the power supply and drive voltages.

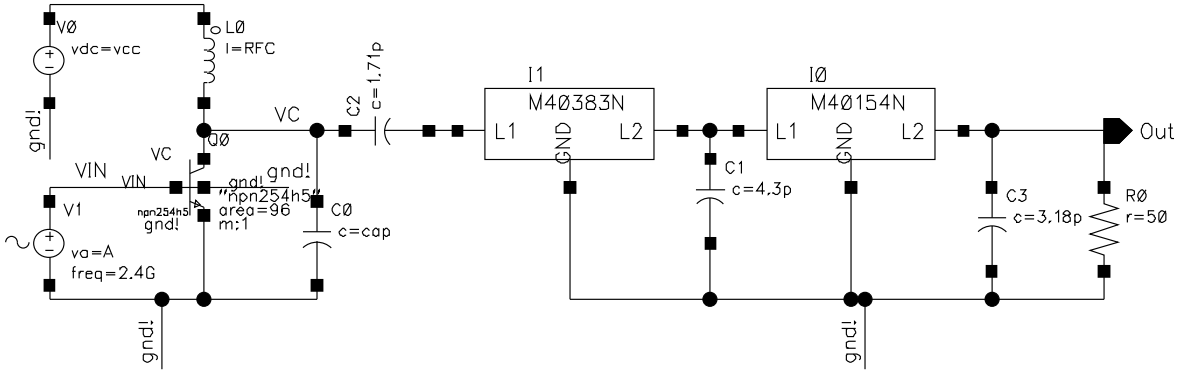


Figure 5.24. Circuit diagram of the higher power Class-E PA design.

Frequency domain simulation of the PA, including the collector voltage and output voltage waveforms, is shown in Figure 5.25. The biasing point of the drive voltage was determined by sweeping the DC voltage across the base of the transistor. The biasing voltage was swept around the typical V_{BE} voltage of the HBT, so that near-to-Class-B biasing could be

established with the maximum output power. The results of the sweep pertaining to the output voltage waveforms are shown in Figure 5.26. From this figure it was established that the biasing voltage of about 0.82 V gave best results. The time domain simulation of all relevant voltage and current waveforms after establishing optimum biasing point is shown in Figure 5.27 and Figure 5.28.

From Figure 5.27 and Figure 5.28, the peak-to-peak output voltage over 50 Ω load is 1.92 V and the DC current consumption is 39.0 mA. This results in collector efficiency of the stage of 23.5 % with output power of 9.2 mW (9.6 dBm). Once again, the output specification of the stage was not reached but much better output power than that for the lower power stage has been realized with roughly the same collector efficiency. If the same set of simulations is performed on the same system using ideal inductors, the resulting output power is 12.1 dBm, which proves that the 2.5 dBm decrease in output power can be directly attributed to spiral inductors.

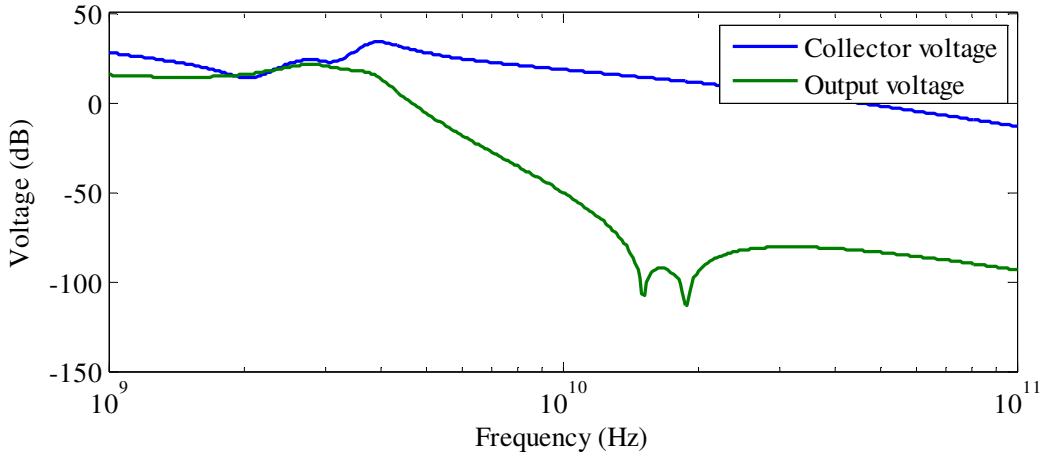


Figure 5.25. Frequency response of the higher power Class-E design.

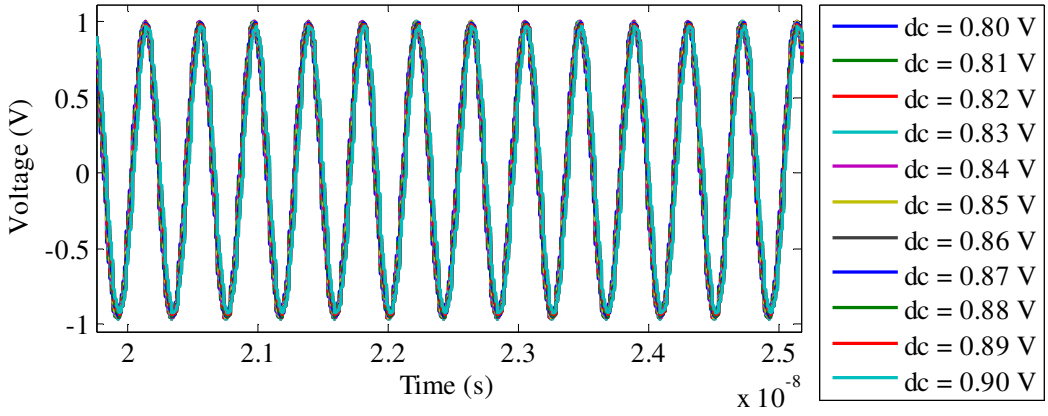


Figure 5.26. DC sweep of the input biasing voltage of the higher power Class-E design with output voltage waveform as output.

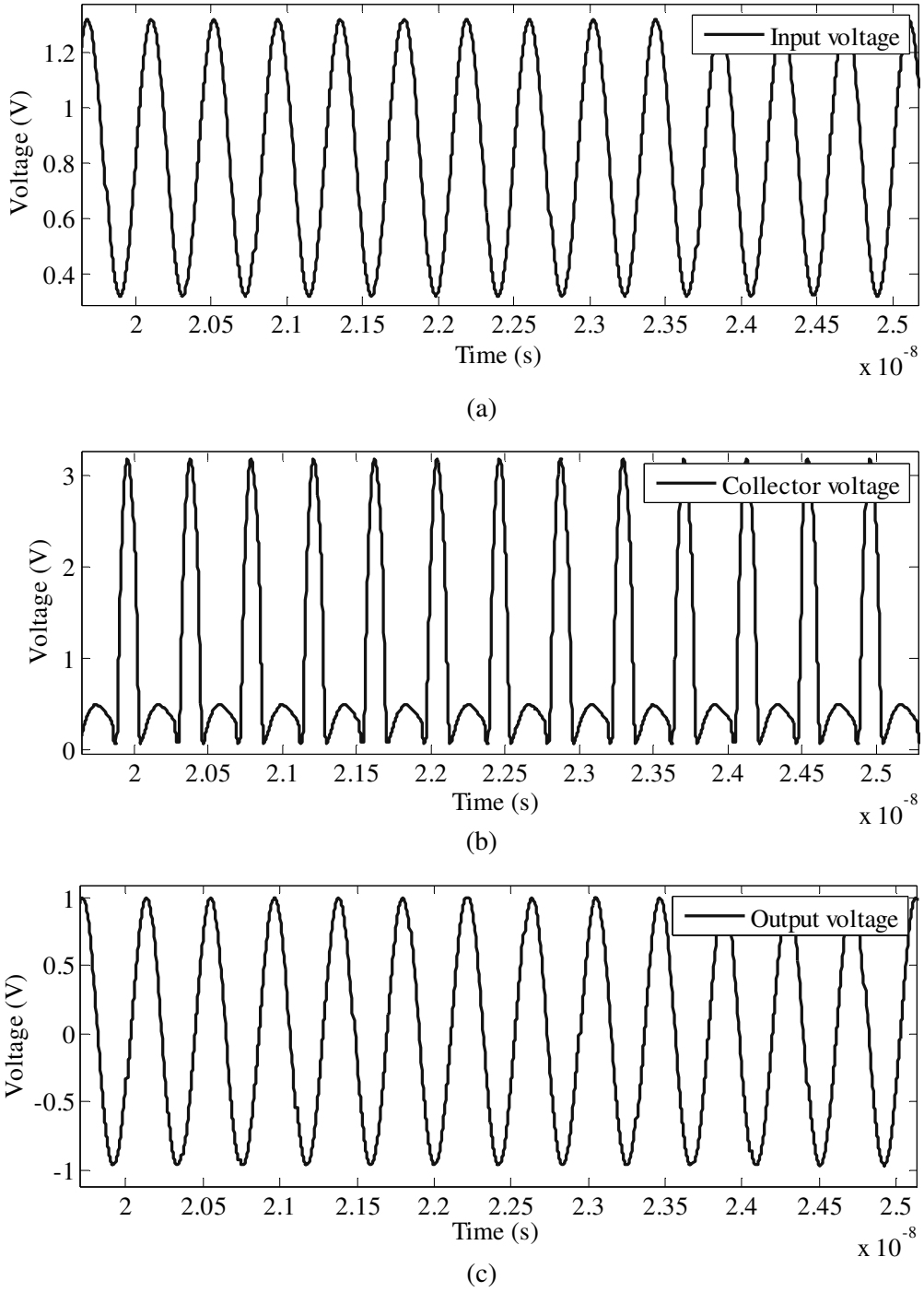


Figure 5.27. Transient response of (a) input voltage, (b) collector voltage and (c) output voltage waveforms of the higher power Class-E design.

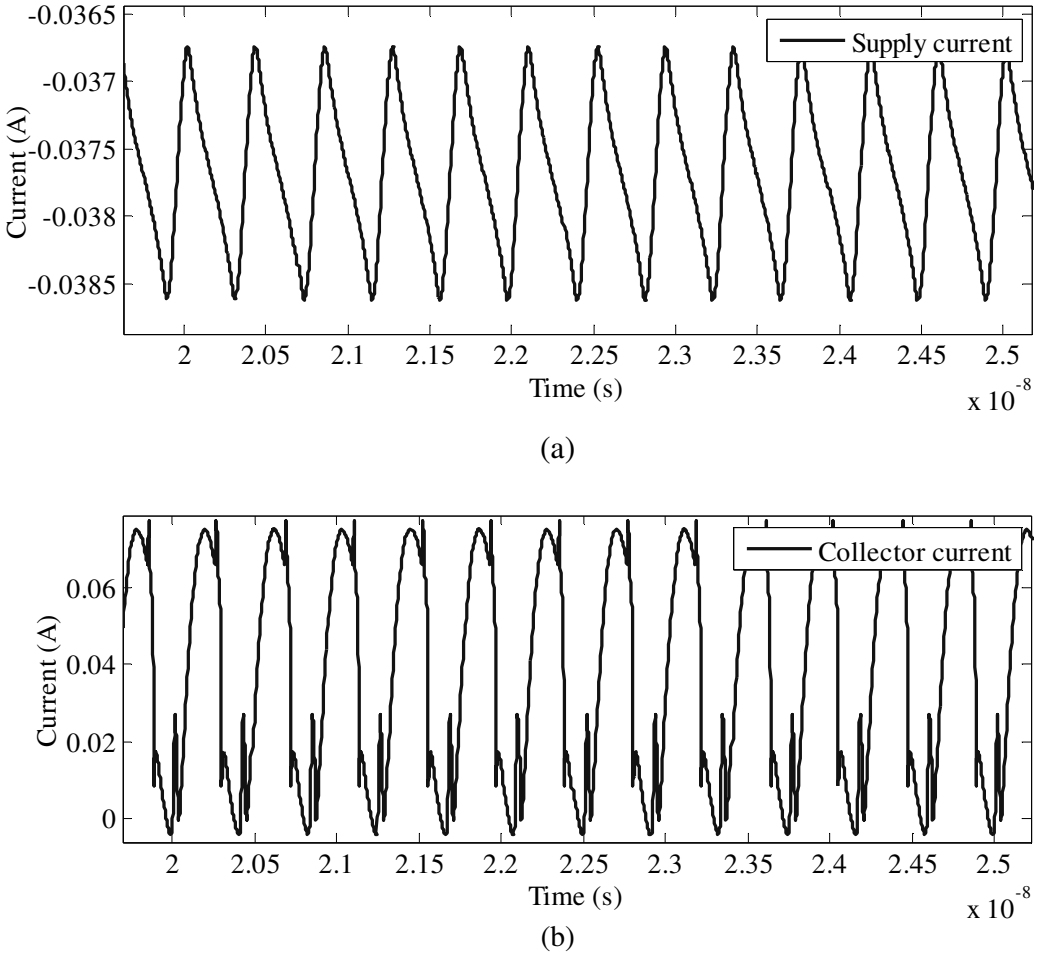


Figure 5.28. Transient response of (a) supply current and (b) collector current waveforms of the higher power Class-E design.

5.3.3 Lower power Class-F configuration

5.3.3.1 Design

The third designed configuration was the lower power Class-F configuration. The aimed output power was 13.5 mW, or 11.3 dBm. This particular power output was chosen so as to obtain an optimum load impedance for maximum power of roughly 50 Ω at DC supply of 1 V. For the maximum available gain, the HS HBT npn254 transistor with total emitter length of 96 μm was chosen. It was again assumed that it would be possible to connect 100 nH RFC externally to the IC. The third harmonic peaking circuit was the topology of choice, with 1 nH and 0.5 nH inductors chosen as filtering inductances for the base- and third-harmonic filters respectively. The chosen design parameters, as well as component values calculated by the design routine, are shown in Table 5.7.

Table 5.7. Chosen and calculated parameters for the design of the lower power Class-F PA.

Parameter	Value	Unit
Centre frequency (f_o)	2.4	GHz
Aimed output power (P_{out})	13.5	mW
Supply voltage (V_{CC})	1	V
RFC (L_1)	100	nH
Required load resistance (R_L)	49.4	Ω
Base filter inductance (L_O)	1.00	nH
Base filter capacitance (C_O)	4.40	pF
Third-harmonic filter inductance (L_3)	0.50	nH
Third-harmonic filter capacitance (C_3)	0.98	pF
DC current (I_{DC})	16.5	mA
Peak collector voltage (v_{Cp})	2.00	V
Peak collector current (i_{sp})	48.1	mA

In order to complete the design the 3M inductors were selected for the implementation of inductors L_O (named M30100N) and L_3 (named M30050N). Table 5.8 shows the geometry and Q-factors for the two inductors as found by the inductance search algorithm. The exported netlist of the whole PA design is shown in Figure 5.29.

Table 5.8. Computed 3M inductor parameters for the lower power Class-F design.

Parameter	Value (M30100N)	Value (M300500N)	Unit
Inductance at 2.4 GHz (L_S)	1.00	0.50	nH
Inductance at DC (L_{SLF})	0.95	0.49	nH
Q-factor (Q)	7.52	6.67	-
Resonant frequency (f_R)	9.51	14.7	GHz
Turn width (w)	50.0	470	µm
Turn spacing (s)	2.00	2.00	µm
Inner diameter (d_{in})	89.0	30.0	µm
Outer diameter (d_{out})	293	222	µm
Number of turns (n)	2	2	-

```
.SUBCKT L0 L1 L2 GND
CS L1 L2 177.00fF
LS N4 L1 0.95n
RS N4 L2 1.37
Csi1 N2 GND 68.94fF
Csi2 N3 GND 68.94fF
Cox1 L1 N2 409.33fF
Cox2 L2 N3 409.33fF
Rsi1 N2 GND 306.05
Rsi2 N3 GND 306.05
.ENDS

.SUBCKT L3 L1 L2 GND
CS L1 L2 156.40fF
LS N4 L1 0.49n
RS N4 L2 1.01
Csi1 N2 GND 47.11fF
Csi2 N3 GND 47.11fF
Cox1 L1 N2 268.66fF
Cox2 L2 N3 268.66fF
Rsi1 N2 GND 448.03
Rsi2 N3 GND 448.03
.ENDS

.SUBCKT class-F-1 bias supply Gnd
LRFC_2 supply N_1 100.00n
CCapacitor_3 N_1 N_4 1.00p
XL0_1 N_2 Gnd Gnd L0
CCapacitor_1 N_2 Gnd
XL3_1 N_4 N_2 Gnd L3
CCapacitor_2 N_4 N_2 0.98p
RResistor_1 N_2 Gnd 49.38 TC=0.0, 0.0
Xnpn254_1 N_1 bias Gnd Gnd npn254 area=96
.ENDS
```

Figure 5.29. Exported netlist of the lower power Class-F design.

5.3.3.2 Simulation

Figure 5.30 shows the circuit diagram of the PA system, with ideal sources used for power supply and drive voltages.

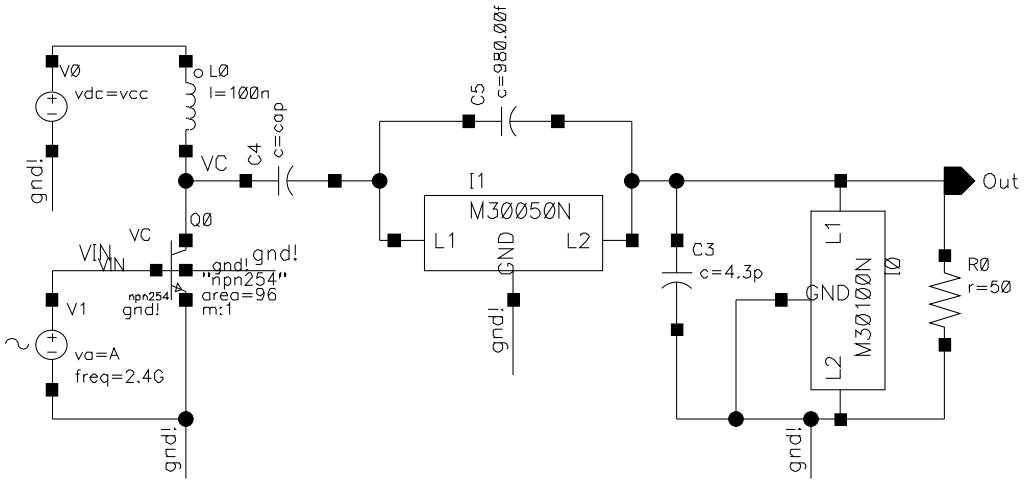


Figure 5.30. Circuit diagram of the lower power Class-F PA design.

The frequency domain simulation of the PA, including the collector voltage waveform and output voltage waveform is shown in Figure 5.31. Biasing point of the drive voltage was

determined by sweeping the DC voltage across the base of the transistor. The biasing voltage was swept just above the V_{BE} voltage of the HBT, so that a near-to-Class-B biasing could be established with maximum output voltage. The results of the sweep pertaining to the output voltage waveform are shown in Figure 5.32. From this figure it was recognized that the biasing voltage of about 0.97 V gives best results. The time domain simulation of all relevant voltage and current waveforms after establishing optimum biasing point is shown in Figure 5.33 and Figure 5.34.

Figure 5.33 and Figure 5.34 show that the peak-to-peak output voltage over 50 Ω load is 1.87 V and the DC current consumption is 64.0 mA. This results in collector efficiency of the stage of 13.7 % with an output power of only 8.74 mW (9.4 dBm) and evident harmonic distortion. From the same set of simulations performed on the same system using ideal inductors, the resulting output power was 11.2 dBm, showing that the 1.8 dBm decrease in output power can be directly attributed to the low quality inductors.

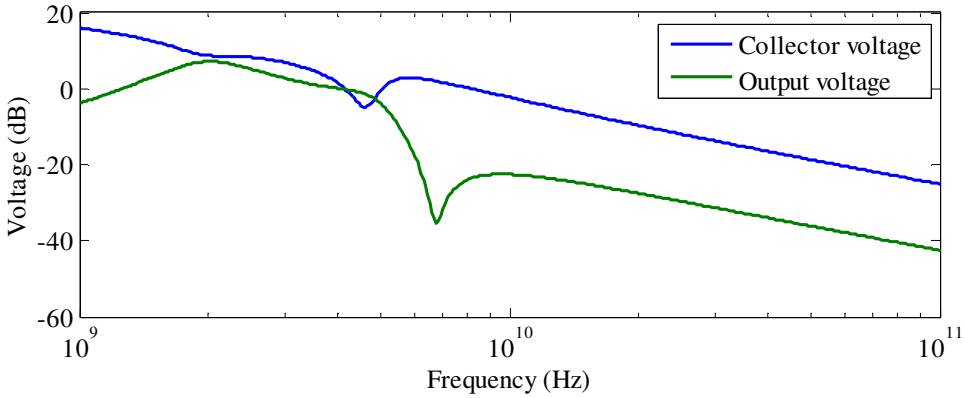


Figure 5.31. Frequency response of the lower power Class-F design.

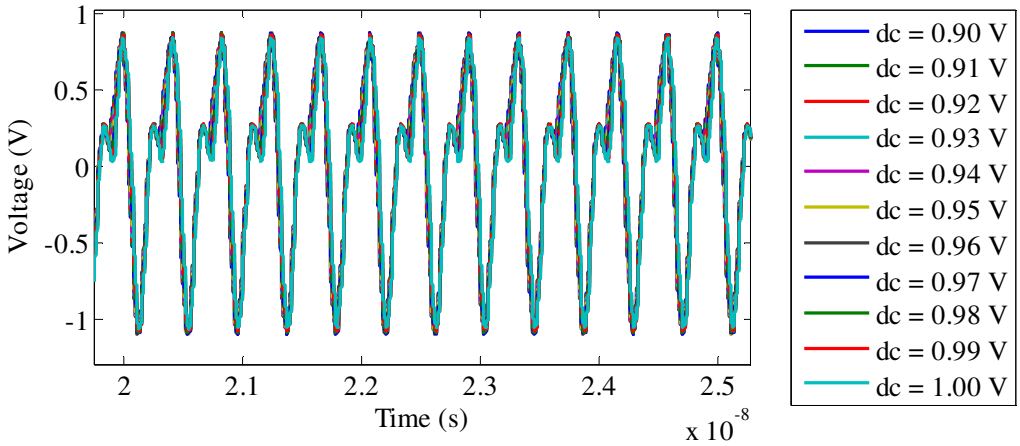


Figure 5.32. DC sweep of the input biasing voltage of the lower power Class-F design with output voltage waveform as output.

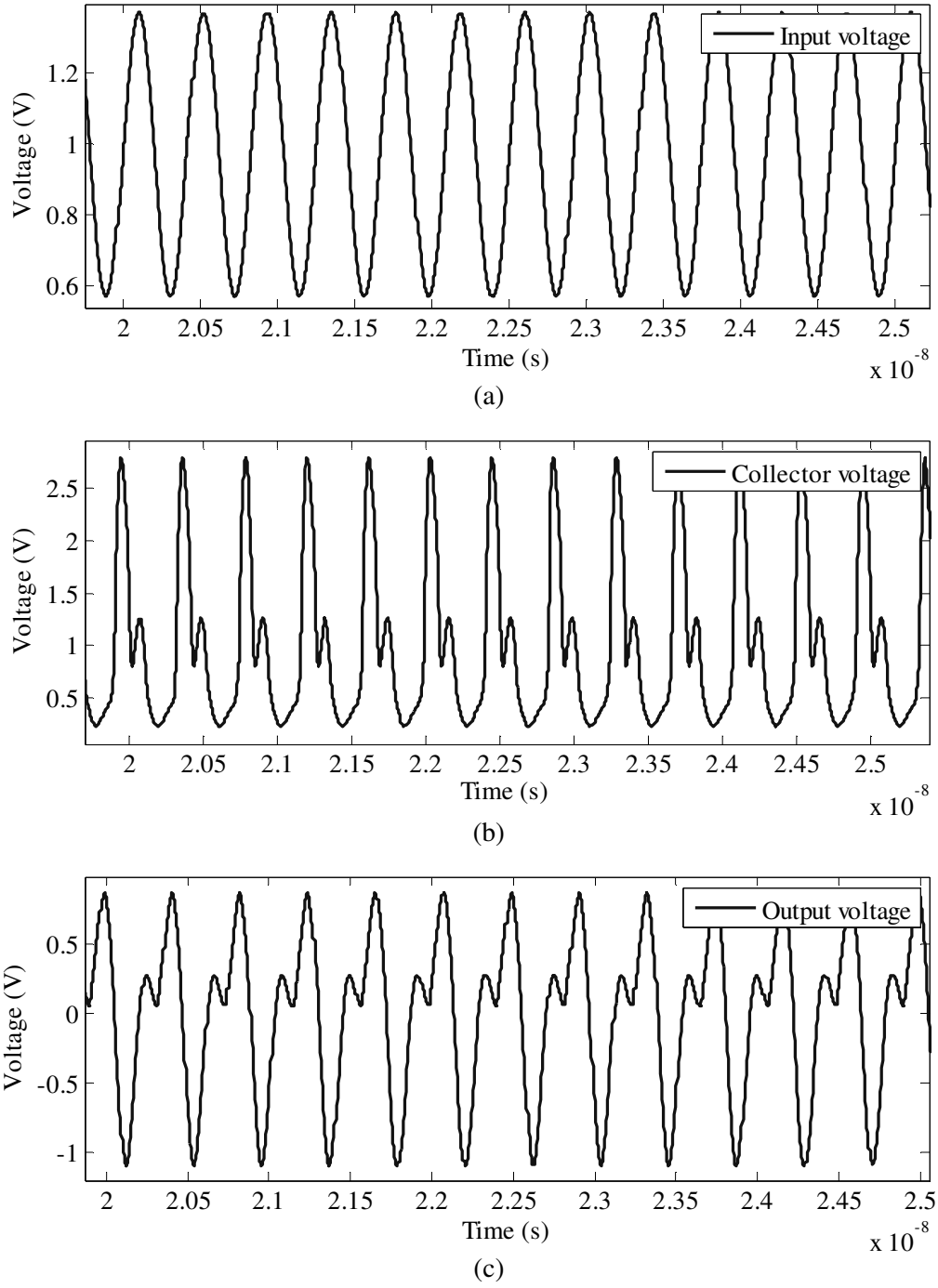


Figure 5.33. Transient response of (a) input voltage, (b) collector voltage and (c) output voltage waveforms of the lower power Class-F design.

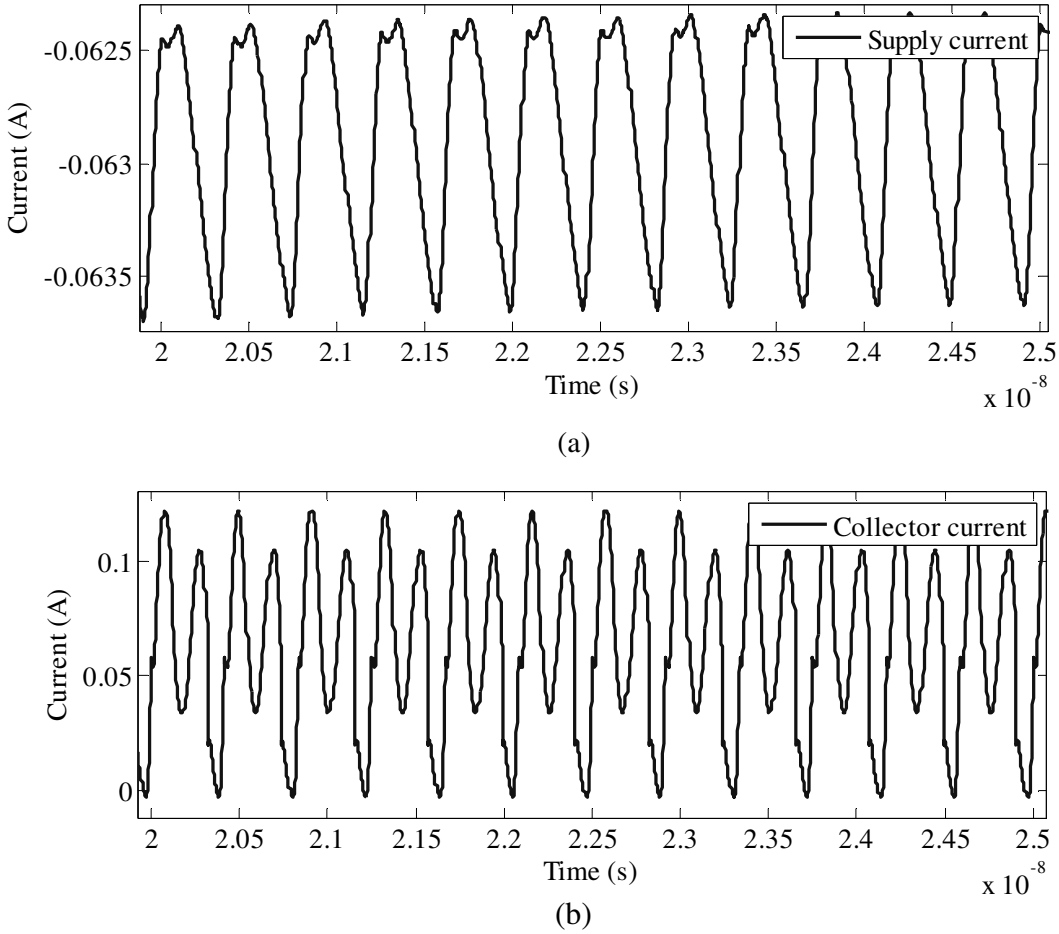


Figure 5.34. Transient response of (a) supply current and (b) collector current waveforms of the lower power Class-F design.

5.3.4 Higher power Class-F configuration

5.3.4.1 Design

The final designed configuration was the higher power Class-F configuration. Aimed output power was 50 mW, or 17.0 dBm. DC supply of 1.5 V was used in conjunction with HV HBT npn254h5 transistor with total emitter length of 96 µm. It was once again assumed that it would be possible to connect a 100 nH RFC externally to the IC. The Class-F output stage with resonators of up to the fifth harmonics was the topology of choice, with 1 nH inductors as filtering inductances for the base filter and 0.5 nH for the third and fifth harmonic filters respectively. Matching networks with 500 MHz bandwidth were considered for output matching. The chosen design parameters, as well as component values calculated by the design routine, are shown in Table 5.9.

Table 5.9. Chosen and calculated parameters for the design of the higher power Class-F PA.

Parameter	Value	Unit
Centre frequency (f_o)	2.4	GHz
Aimed output power (P_{out})	50	mW
Supply voltage (V_{CC})	1.5	V
RFC (L_1)	100	nH
Required load resistance (R_L)	32.8	Ω
Base filter inductance (L_O)	1.00	nH
Base filter capacitance (C_O)	4.40	pF
Third-harmonic filter inductance (L_3)	0.50	nH
Third-harmonic filter capacitance (C_3)	0.98	pF
Fifth-harmonic filter inductance (L_5)	0.50	nH
Fifth-harmonic filter capacitance (C_5)	0.35	pF
DC current (I_{DC})	36.8	mA
Peak collector voltage (v_{Cp})	3.00	V
Peak collector current (i_{sp})	110	mA
L-network matching inductance (L_M)	4.58	nH
L-network matching capacitance (C_M)	2.79	pF
Ind-cap-ind T-network matching inductance 1 (L_{M1})	10.43	nH
Ind-cap-ind T-network matching capacitance 1 (C_{M1})	0.272	pF
Ind-cap-ind T-network matching inductance 2 (L_{M2})	12.74	nH
Cap-ind-cap T-network matching capacitance 1 (C_{M1})	0.421	pF
Cap-ind-cap T-network matching inductance 1 (L_{M1})	6.048	nH
Cap-ind-cap T-network matching capacitance 2 (C_{M2})	0.345	pF
Ind-cap-ind Π-network matching inductance 1 (L_{M1})	0.566	nH
Ind-cap-ind Π-network matching capacitance 1 (C_{M1})	3.698	pF
Ind-cap-ind Π-network matching inductance 2 (L_{M2})	0.691	nH
Cap-ind-cap Π-network matching capacitance 1 (C_{M1})	7.772	pF
Cap-ind-cap Π-network matching inductance 1 (L_{M1})	1.192	nH
Cap-ind-cap Π-network matching capacitance 2 (C_{M2})	6.366	nH

In order to complete the design the TM inductors were selected for the implementation of inductors L_O (named M40100N), L_3 and L_5 (named M40050N) as well as L_{M1} (named M40119N). Table 5.10 shows the geometry and Q-factors for the two inductors as found by the inductance search algorithm. The exported netlist of the whole PA design is shown in Figure 5.35.

Table 5.10. Computed TM inductor parameters for the higher power Class-F design.

Parameter	Value (M40100N)	Value (M400500N)	Value (M40119N)	Unit
Inductance at 2.4 GHz (L_S)	1.00	0.50	1.19	nH
Inductance at DC (L_{SLF})	0.94	0.49	1.13	nH
Q-factor (Q)	13.0	12.4	12.5	-
Resonant frequency (f_R)	9.82	15.0	9.68	GHz
Turn width (w)	48.0	46.0	42.0	µm
Turn spacing (s)	2.00	2.00	2.00	µm
Inner diameter (d_{in})	90.0	31.0	115	µm
Outer diameter (d_{out})	286	219	287	µm
Number of turns (n)	2	2	2	-

```
.SUBCKT L0 L1 L2 GND
CS L1 L2 163.12fF
LS N4 L1 0.94n
RS N4 L2 0.72
Csi1 N2 GND 67.01fF
Csi2 N3 GND 67.01fF
Cox1 L1 N2 279.59fF
Cox2 L2 N3 279.59fF
Rsi1 N2 GND 314.94
Rsi2 N3 GND 314.94
.ENDS

.SUBCKT L3 L1 L2 GND
CS L1 L2 149.81fF
LS N4 L1 0.49n
RS N4 L2 0.53
Csi1 N2 GND 46.40fF
Csi2 N3 GND 46.40fF
Cox1 L1 N2 188.59fF
Cox2 L2 N3 188.59fF
Rsi1 N2 GND 454.91
Rsi2 N3 GND 454.91
.ENDS

.SUBCKT L5 L1 L2 GND
CS L1 L2 149.81fF
LS N4 L1 0.49n
RS N4 L2 0.53
Csi1 N2 GND 46.40fF
Csi2 N3 GND 46.40fF
Cox1 L1 N2 188.59fF
Cox2 L2 N3 188.59fF
Rsi1 N2 GND 454.91
Rsi2 N3 GND 454.91
.ENDS

.SUBCKT LM6 L1 L2 GND
CS L1 L2 124.89fF
LS N4 L1 1.13n
RS N4 L2 0.87
Csi1 N2 GND 67.98fF
Csi2 N3 GND 67.98fF
Cox1 L1 N2 261.28fF
Cox2 L2 N3 261.28fF
Rsi1 N2 GND 310.66
Rsi2 N3 GND 310.66
.ENDS

.SUBCKT Class-F-2 bias supply Gnd
LRFC_2 supply N_1 100.00n
CCapacitor_3 N_1 N_4 1.00p
XL0 N_M1 Gnd Gnd L0
CCapacitor_1 N_M1 Gnd 4.40p
XL3 N_4 N_3 Gnd L3
CCapacitor_2 N_4 N_3 0.98p
XL5 N_3 N_M1 Gnd L5
CCapacitor_4 N_3 N_M1 0.35p
RResistor_1 N_M2 Gnd 50.00 TC=0.0, 0.0
Xnpn254h5_1 N_1 bias Gnd Gnd npn254 area=96
CCapacitor_M1 Gnd N_M1 7.77p
CCapacitor_M2 Gnd N_M2 6.37p
XLM6_1 N_M2 N_M1 Gnd LM6
.ENDS
```

Figure 5.35. Exported netlist of the higher power Class-F design.

5.3.4.2 Simulation

Figure 5.36 shows the circuit diagram of the PA system, with ideal sources used for power supply and drive voltages.

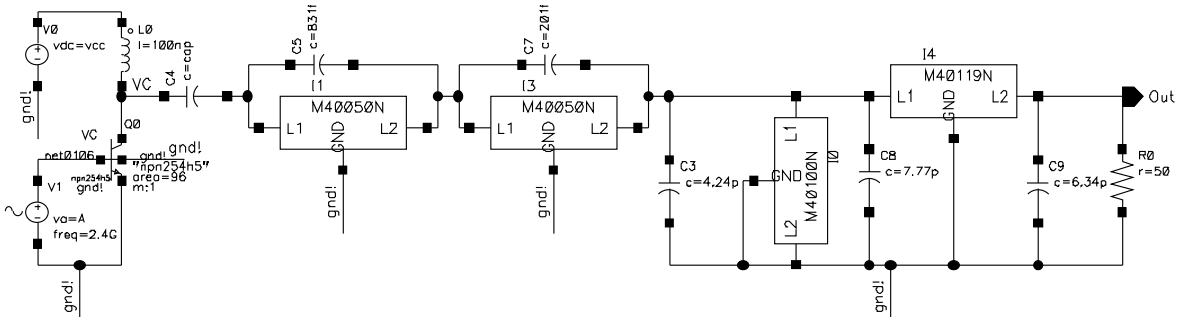


Figure 5.36. Circuit diagram of the higher power Class-F PA design.

Frequency domain simulation of the PA including the collector voltage waveform and output voltage waveform is shown in Figure 5.37. The biasing point of the drive voltage was determined by sweeping the DC voltage across the base of the transistor. The biasing voltage was swept just above the V_{BE} voltage of the HBT, so that a near-to-Class-B biasing could be established with maximum output voltage. The biasing voltage was swept around the V_{BE} voltage of the HBT. The results of the sweep pertaining to the output voltage waveform are shown in Figure 5.38. From this figure it was decided that the biasing voltage of about 0.8 V gave best results. The time domain simulation of all relevant voltage and current waveforms after an optimum biasing point was established is shown in Figure 5.39 and Figure 5.40.

From Figure 5.39 and Figure 5.40 the peak-to-peak output voltage over 50 Ω load is 2.22 V and the DC current consumption is 41.0 mA. This results in collector efficiency of the stage of 20.0 % with output power of 12.3 mW (10.9 dBm) and no evident harmonic distortion. When the same set of simulations was performed on the same system but using ideal inductors, the resulting output power was 13.9 dBm, showing that the 3 dBm decrease in output power can be directly attributed to low quality inductors.

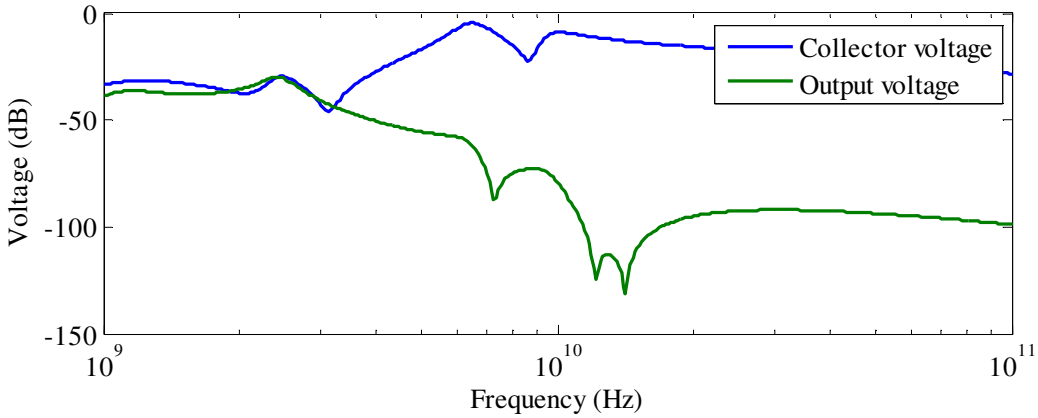


Figure 5.37. Frequency response of the higher power Class-F design.

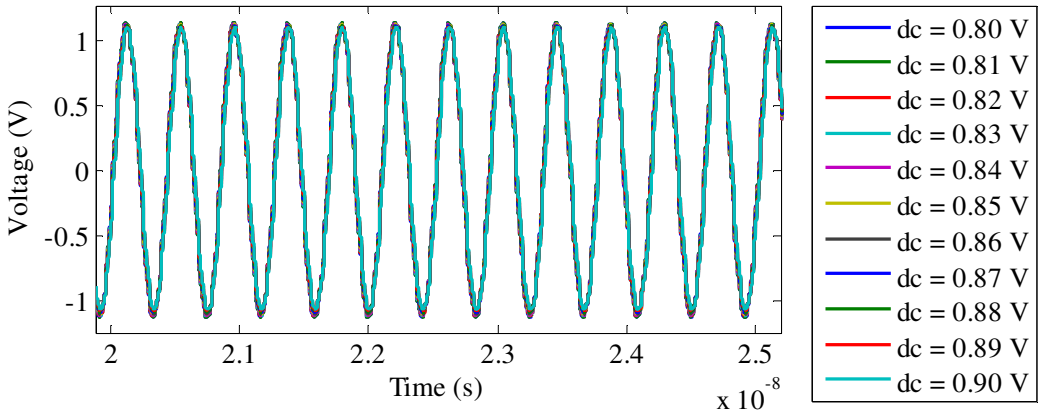
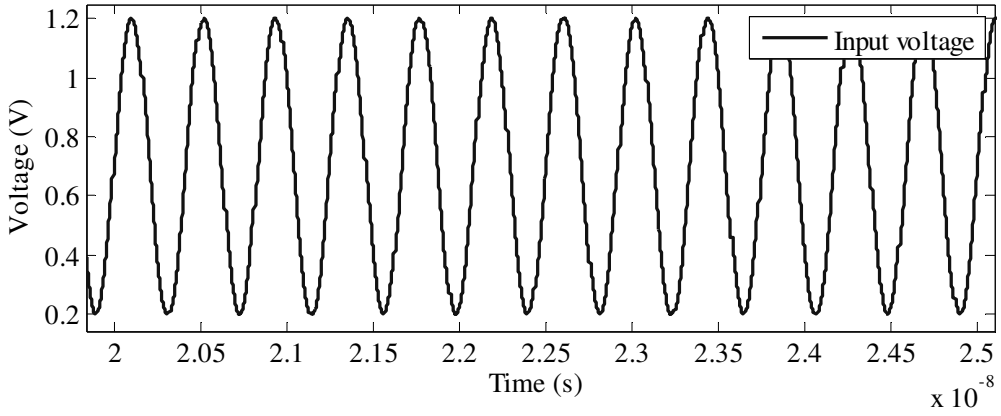
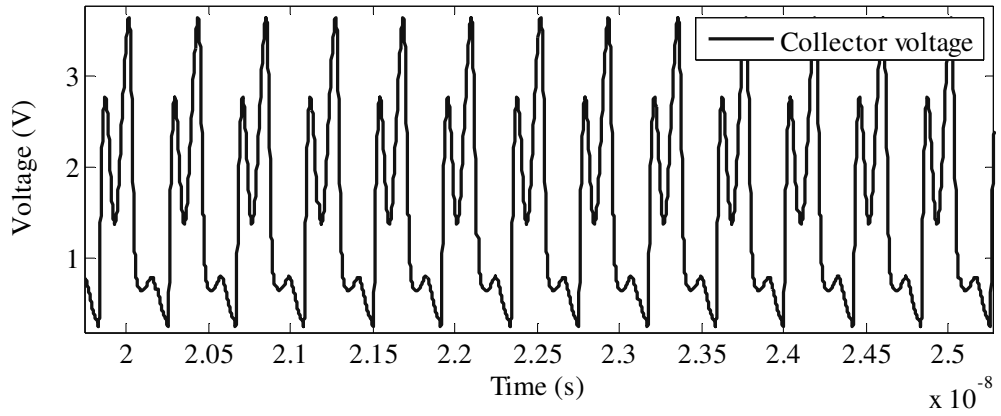


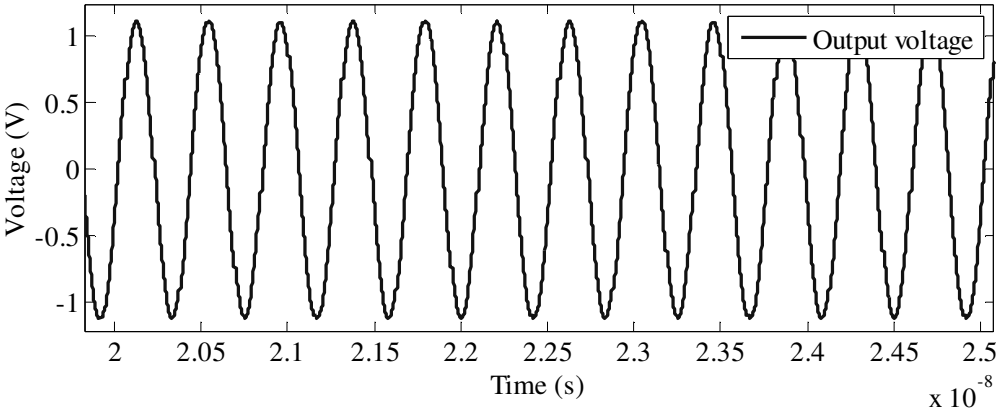
Figure 5.38. DC sweep of the input biasing voltage of the higher power Class-F design with output voltage waveform as the output.



(a)



(b)



(c)

Figure 5.39. Transient response of (a) input voltage, (b) collector voltage and (c) output voltage waveforms of the higher power Class-F design.

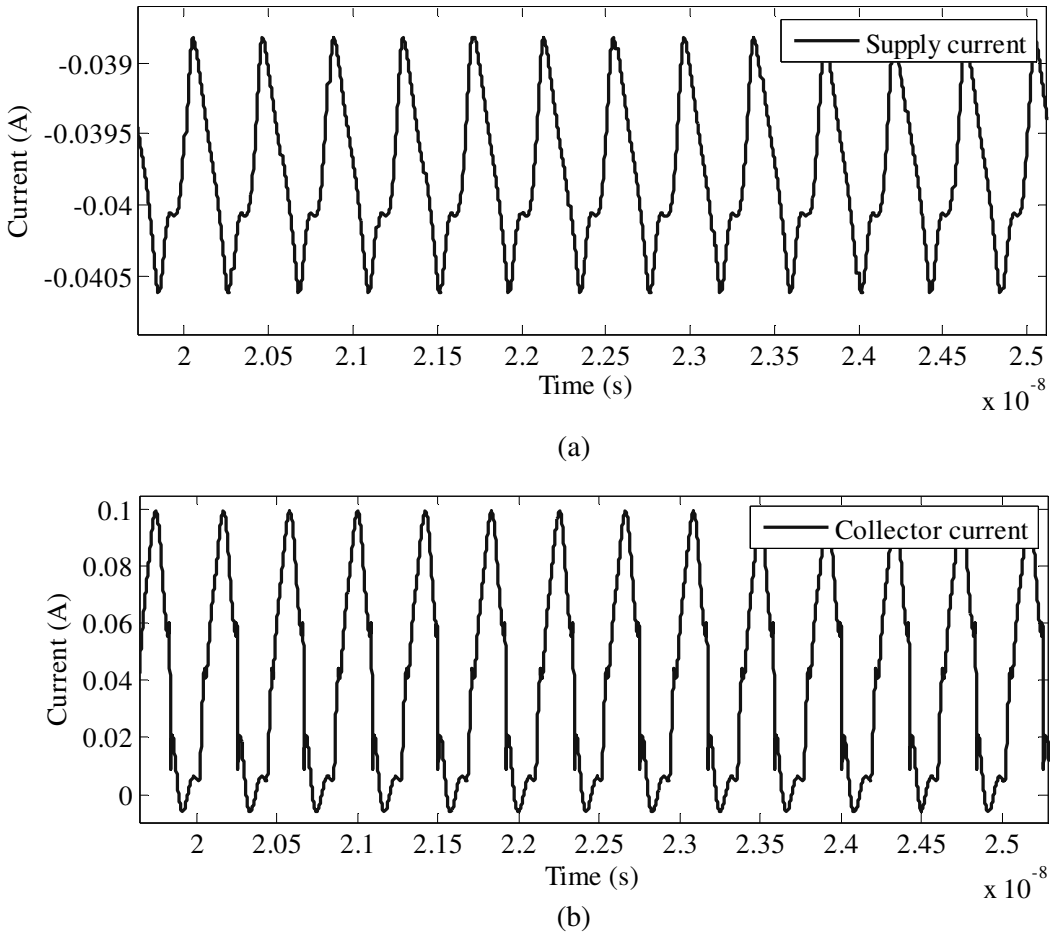


Figure 5.40. Transient response of (a) supply current and (b) collector current waveforms of the higher power Class-F design.

5.3.5 Choice of better Class-E and Class-F configuration

From the analyses in Sections 5.3.1 through 5.3.4, it is evident that both in case of Class-E and Class-F amplifiers, the configuration identified as the "higher power" configuration gives better quality amplification. In both cases, the output power, collector efficiency and harmonic distortion of the output signal are evidently better than those for their "lower power" counterparts.

In neither case the designed output power was reached, which was due to the loss of gain and output power capability of the HBT at the design frequency of 2.4 GHz. Further loss of output power was experienced due to the implementation of modelled spiral inductors. Both loss mechanisms were considered acceptable within the scope of this thesis.

5.4 FURTHER DESIGN OF THE CLASS-E AMPLIFIER

An active biasing network similar to the one described in [33] was designed from first principles in order to provide the bias of 0.82 V for the Class-E amplifier described in Section 5.3.2. The *S*-parameter based input impedance matching, described in Section 4.6 was implemented for this PA to match the assumed input source impedance of 50 Ω to the input port (base) of the PA. A simple L matching network was used here. The schematic showing the complete PA, including biasing and input impedance matching, with matching inductors also implemented using spiral inductors, is shown in Figure 5.41. All RFCs and decoupling capacitors were considered to be implemented off-chip.

Temperature sweep from -20 to 120 °C on the output voltage waveform is shown in Figure 5.42. From this figure, it is seen that there is no deterioration of output voltage waveform (and therefore no gain decrease) as temperature increases and therefore emitter and/or base ballasting are not needed. Harmonic content of the same waveform at room temperature (27 °C) is shown in Figure 5.43. From this figure, the THD is only 2.14 %.

Also at room temperature, the PA draws 55 mA from 1 V voltage supply, whilst exhibiting output power of 6.3 mW, resulting in collector efficiency of 11.3 %. For 1 mW input power level, the PAE is 9.6 %.

The *S*-parameters of the PA modelled as two port network (where ground represents the second port) are shown in Figure 5.44 to Figure 5.47 [110]. From these figures, it is evident that input and output port of this PA are well matched, and that in the forward direction, the system acts as an amplifier, whilst in the reverse direction, the system acts as an attenuator, as expected.

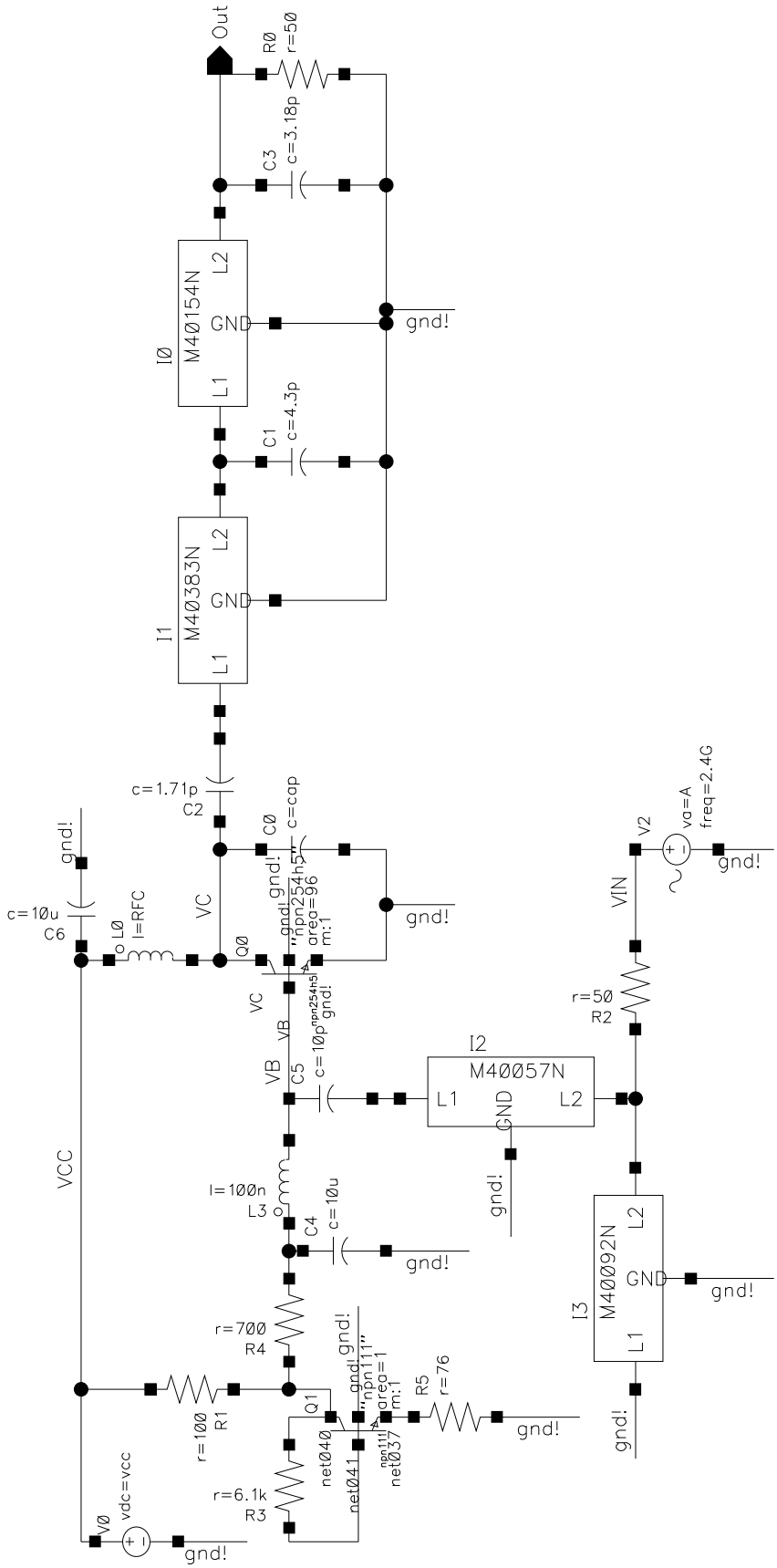


Figure 5.41. Designed Class-E PA with biasing and matching networks.

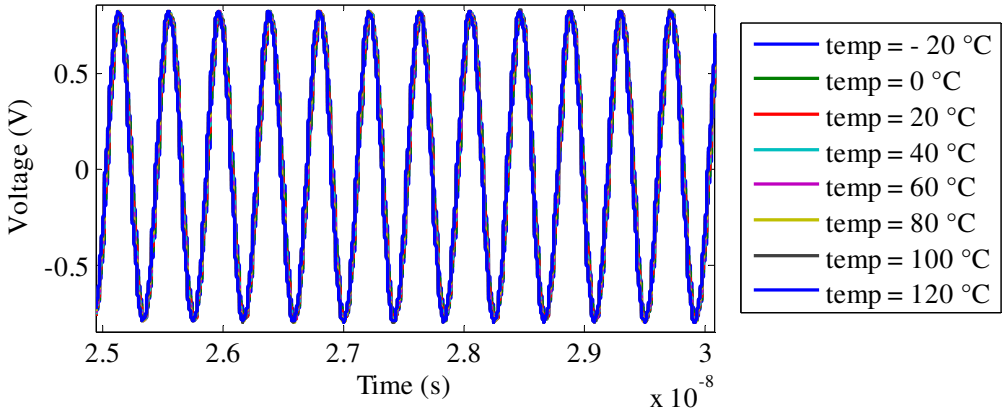


Figure 5.42. Temperature-swept output voltage waveform of the full Class-E PA.

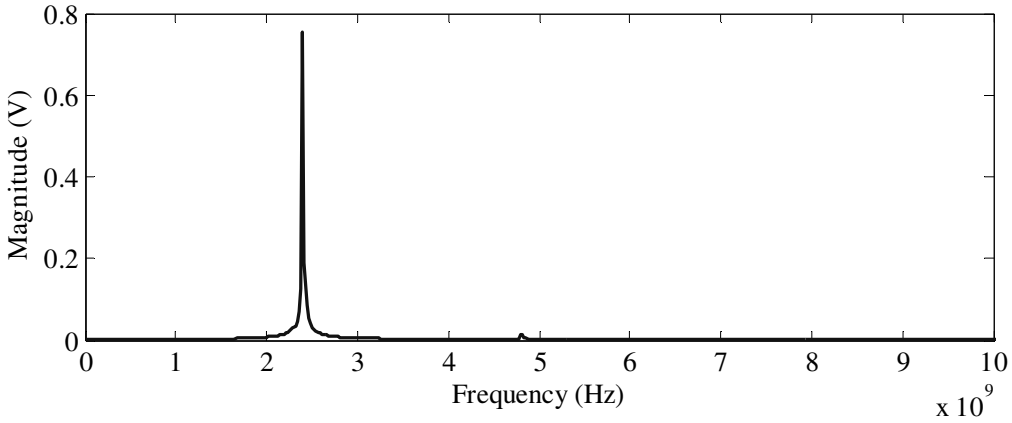


Figure 5.43. Harmonics of the output voltage waveform of the designed Class-E PA system.

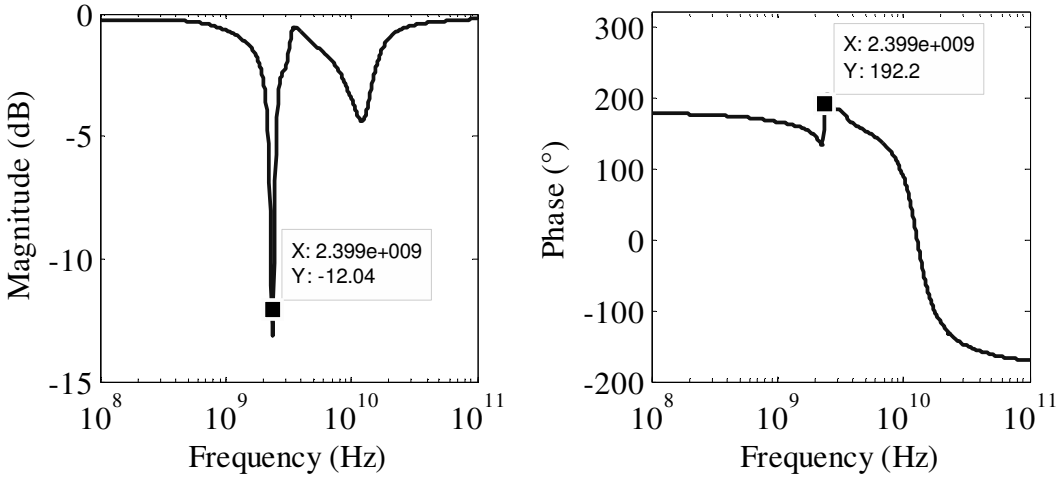


Figure 5.44. Input port voltage reflection coefficient (S_{11}) of the designed Class-E PA system.

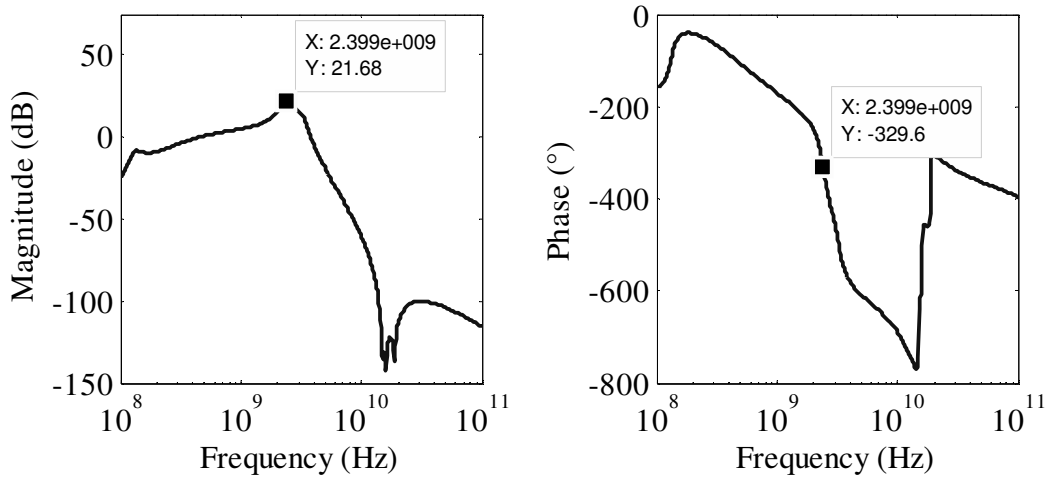


Figure 5.45. Forward voltage gain (S_{21}) of the designed Class-E PA system.

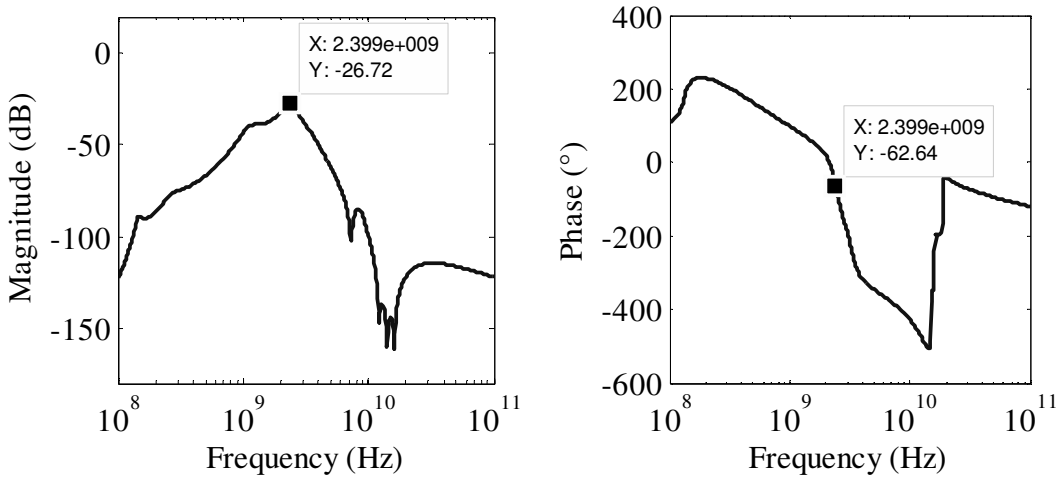


Figure 5.46. Reverse voltage gain (S_{12}) of the designed Class-E PA system.

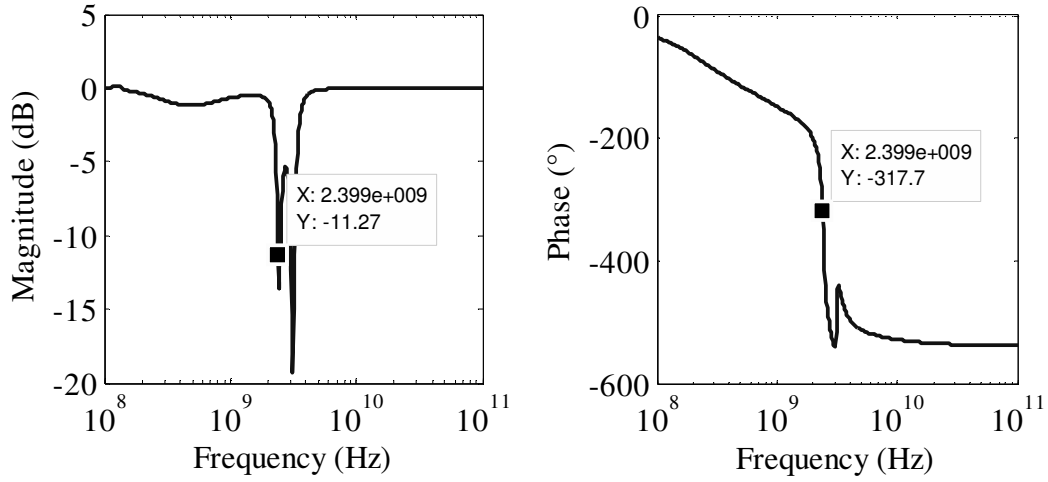


Figure 5.47. Output port voltage reflection coefficient (S_{22}) of the designed Class-E PA system.

5.5 FURTHER DESIGN OF THE CLASS-F AMPLIFIER

As in the case of Class-E amplifier, an active biasing network was designed to provide a bias of 0.8 V for the Class-F amplifier described in Section 5.3.4. An *S*-parameter based input impedance matching was implemented on this PA as well to match the assumed input source impedance of 50 Ω to the input port (base) of the PA. The schematic showing a complete PA, including biasing and input impedance matching, with matching inductors also implemented using spiral inductors, is shown in Figure 5.48. Again, all RFCs and decoupling capacitors were considered to be implemented off-chip.

Temperature sweep from -20 to 120 °C on the output voltage waveform is shown in Figure 5.49. From this figure, it is seen that there is no deterioration of the output voltage waveform (and therefore no gain decrease) as temperature increases and therefore emitter and/or base ballasting are not needed. The harmonic content of the same waveform at room temperature (27 °C) is shown in Figure 5.50. From this figure, the THD is only 0.59 %.

Also at room temperature, the PA draws 35 mA from a 1.5 V voltage supply, whilst exhibiting the output power of 5.3 mW, resulting in collector efficiency of 10.0 %. For 1 mW input power level, the PAE is 8.2 %.

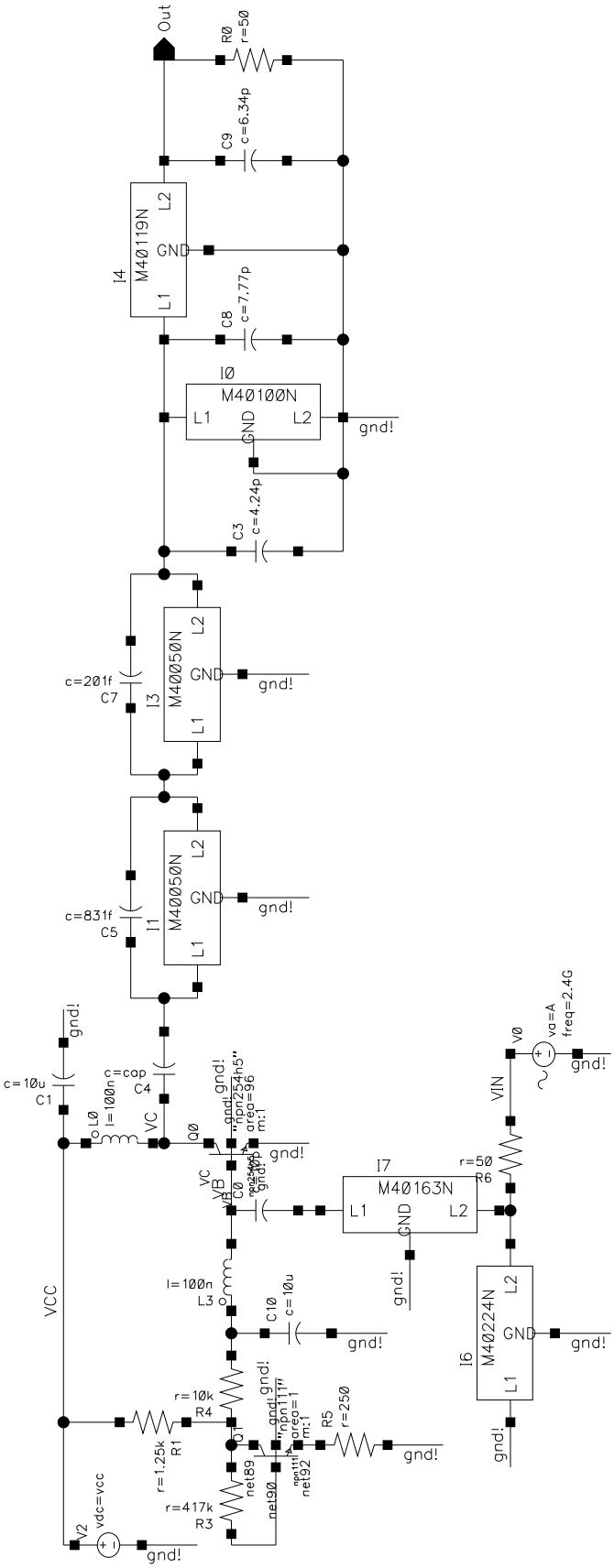


Figure 5.48. Designed Class-F PA with biasing and matching networks.

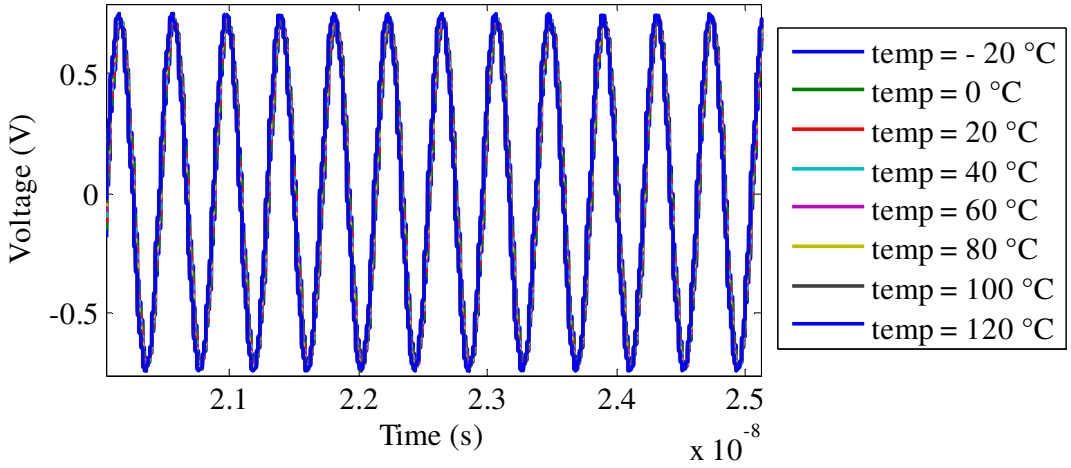


Figure 5.49. Temperature-swept output voltage waveform of the full Class-F PA.

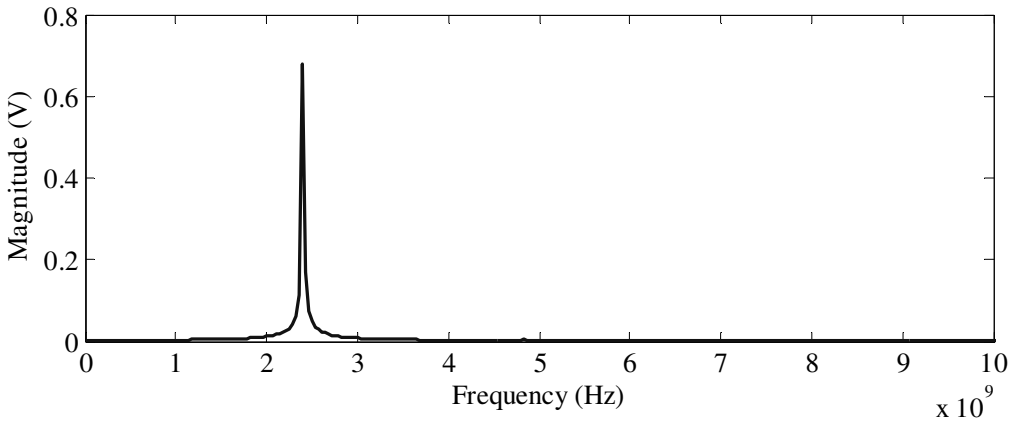


Figure 5.50. Harmonics of the output voltage waveform of the designed Class-F PA system.

The *S*-parameters of the PA modelled as a two port network are shown in Figure 5.51 to Figure 5.54 [110]. From these figures, it is evident that input and output ports of this PA are well matched, and that in the forward direction, the system acts as an amplifier, while in the reverse direction, the system acts as an attenuator, as expected.

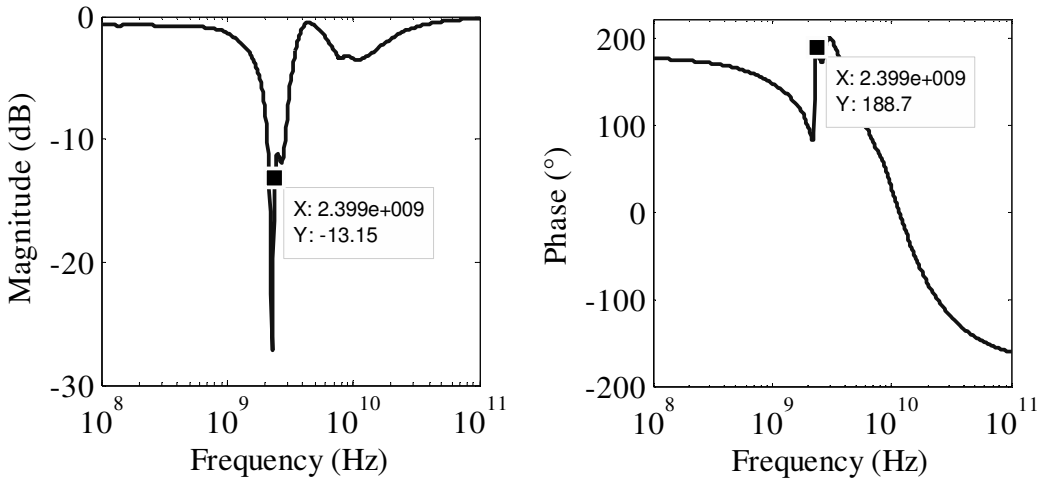


Figure 5.51. The input port voltage reflection coefficient (S_{11}) of the designed Class-F PA system.

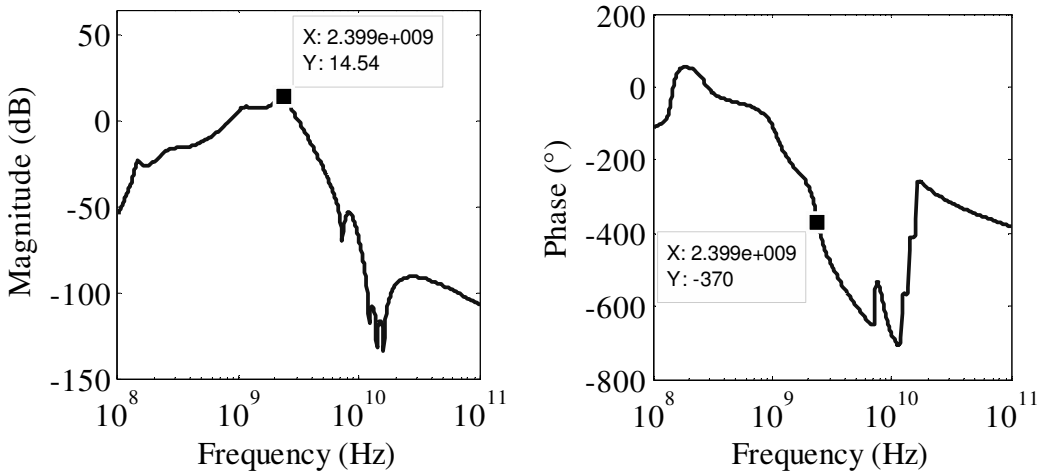


Figure 5.52. The forward voltage gain (S_{21}) of the designed Class-F PA system.

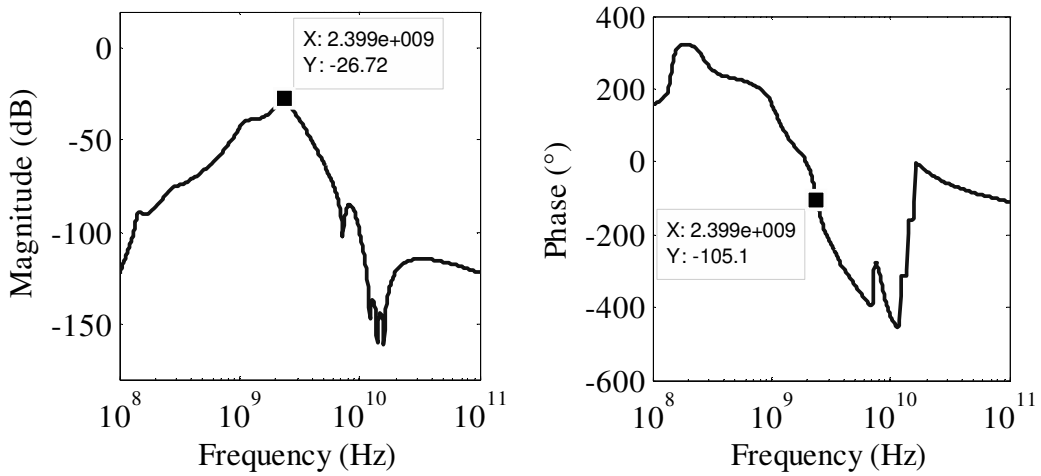


Figure 5.53. The reverse voltage gain (S_{12}) of the designed Class-F PA system.

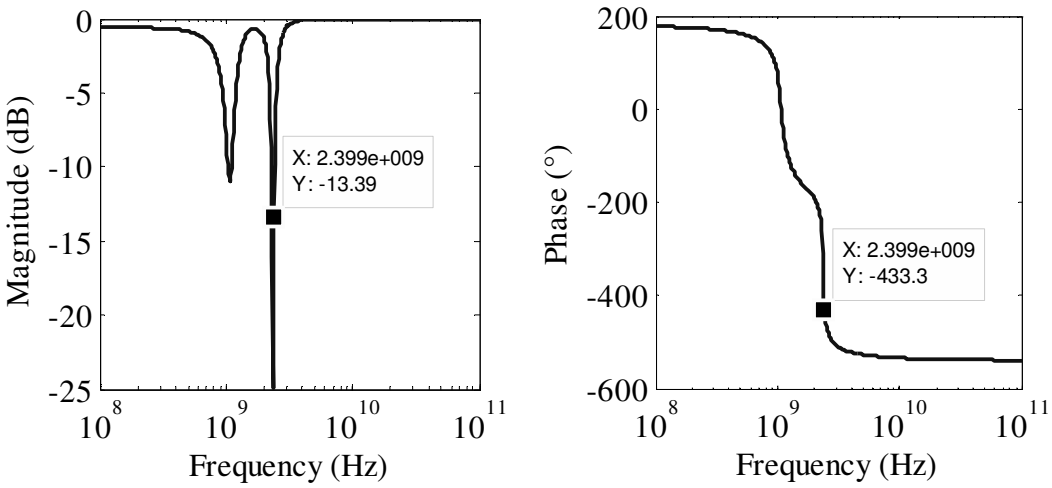


Figure 5.54. Output port voltage reflection coefficient (S_{22}) of the designed Class-F PA system.

5.6 CONCLUSION

In this chapter, the two integral parts of the system level routine for the design of PAs were shown. The inductor model and inductance search algorithm were verified by means of EM simulations. The model and EM simulation corresponded well and it has been established that spiral inductors can be used with monolithic PAs if their inductance and Q-factor are predicted by the inductance search algorithm. Furthermore, the streamlined use of the complete PA design routine was demonstrated by designing one Class-E and one Class-F output stage complete with input and output matching as well as biasing with minimum optimisation effort. While the results were short of the goal parameters of the two amplifiers, particularly the output power, the importance of the routine has been confirmed. Chapter 6 follows with measurement results.

CHAPTER 6 LAYOUT, FABRICATION AND MEASUREMENT RESULTS

6.1 INTRODUCTION

In Chapter 5, the inductor modelling and spiral inductor search algorithm was verified by means of EM simulations. Furthermore, a full circuit design and simulations in the AMS S35 (0.35 µm BiCMOS) process for the PAs designed with the full system integration routine were presented. In this chapter, several inductors were identified to correspond with the inductors provided and measured by the AMS in order to establish the accuracy of inductor modelling experimentally. Additionally, layouts for the designs described in Sections 5.3.2 and 5.3.4 have been drawn. Due to constraints described in Section 3.3, fabrication in AMS process was not possible, so layouts are drawn in IBM 7WL (180 nm BiCMOS) process. This also offers a proof that the research outputs are technology independent. The IC measurements were performed on a custom designed PCB.

6.1.1 Inductor measurements

As a starting point, the square spiral inductor structures given by AMS in [89] have been analyzed and square spiral inductors identified. These included eleven layer-three inductors for the three-metal AMS process (3M) and fourteen thick-layer (TM) inductors for the AMS thick-metal process. The spiral inductor part of the routine, as developed in Chapter 4, was then employed to calculate inductances and Q-factors of the same inductors at the same respective frequencies. Furthermore, EM simulations were performed for completeness.

Comparison of the inductance and Q-factor values predicted by the inductor model and simulated by means of EM simulations against those measured by AMS cannot be given in this version of the thesis due to obligations to the signed NDA. In summary, the measurement results show that inductance values are correctly predicted (within 3.7 %) by the inductor models used for the inductance search algorithm. As far as Q-factors are concerned, situation differs for the 3M and TM inductors, where more accurate predictions are accomplished for the 3M inductors than for the TM (3.9 % vs. 34 %), the phenomenon that has previously been described in Section 5.2.

6.2 FULL SYSTEM INTEGRATION MEASUREMENTS

One Class-E PA and one Class-F PA were submitted for fabrication.

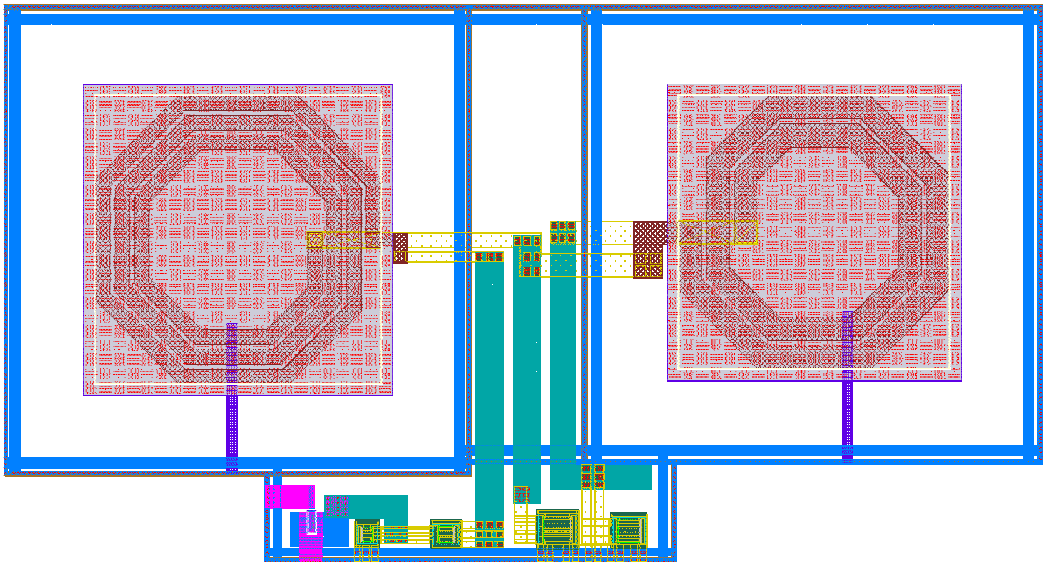
6.2.1 Circuit layouts

Due to the process differences, some considerations had to be taken into account in performing the layouts of the circuits described in Sections 5.3.2 and 5.3.4.

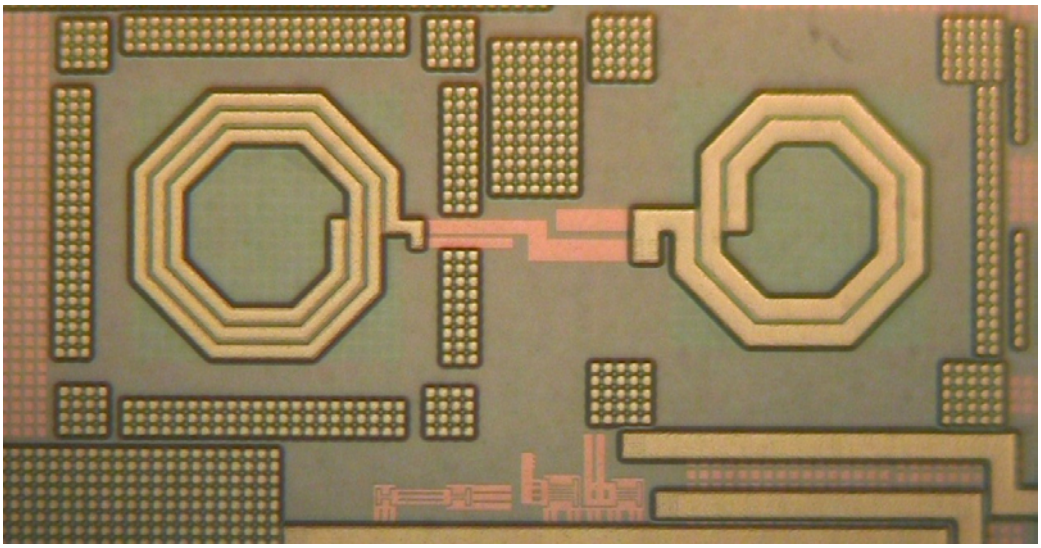
- HBTs in AMS process have larger total emitter area than HBTs in IBM process. This should result in a poorer frequency (*S*-parameter) response of the IBM transistor to the one in the AMS process, and the total output power delivered to the load of the IC will inevitably be lower.

- Inductors available in the IBM process are octagonal spiral inductors. In order to utilize them properly, the spiral inductor design algorithm described in Section 4.5 had to be modified to cater for octagonal geometries. Also, the IBM process offered two types of ground planes: trench isolation TI (TI) and metal 1 (M1). Inductors without a ground plane were not supported by the process therefore TI ground plane was implemented to decrease the spiral-to-substrate capacitance and lower turn-to-turn coupling.

The layouts and photographs of the Class-E and Class-F PAs are shown in Figure 6.1 and Figure 6.2 respectively. The total chip area occupied without the bondpad openings was 1130 × 600 μm^2 for the Class-E configuration and 950 × 950 μm^2 for Class-F configuration. Figure 6.3 shows the Class-E and Class-F PAs within the MPW.

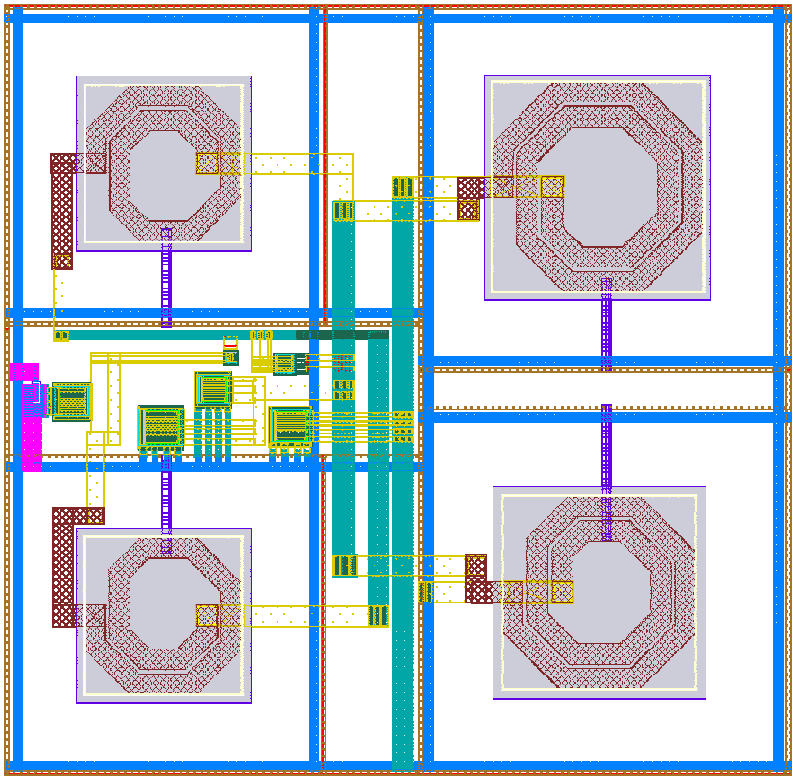


(a)

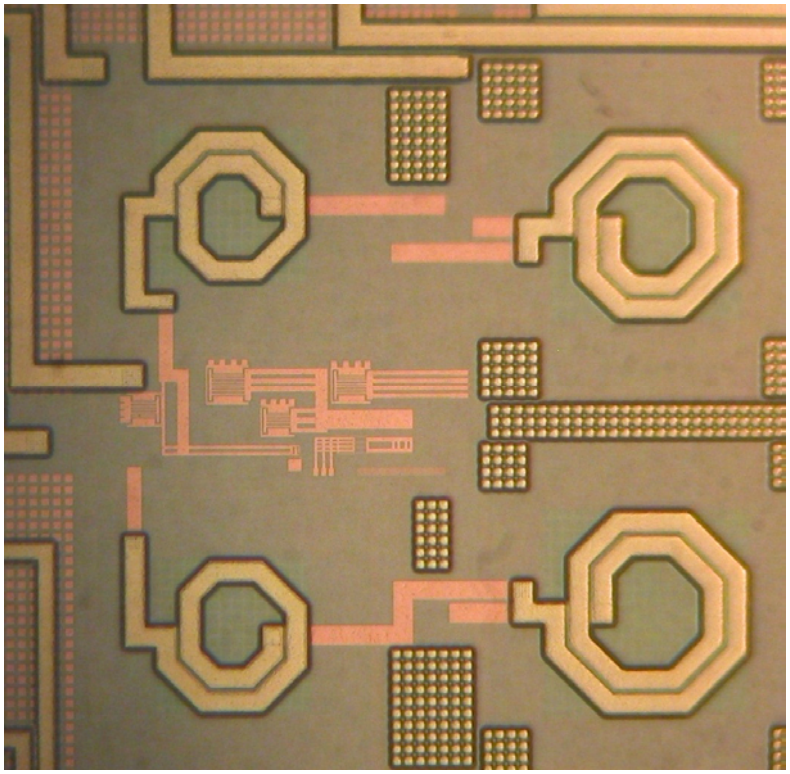


(b)

Figure 6.1. The (a) layout and (b) photo of the Class-E PA.

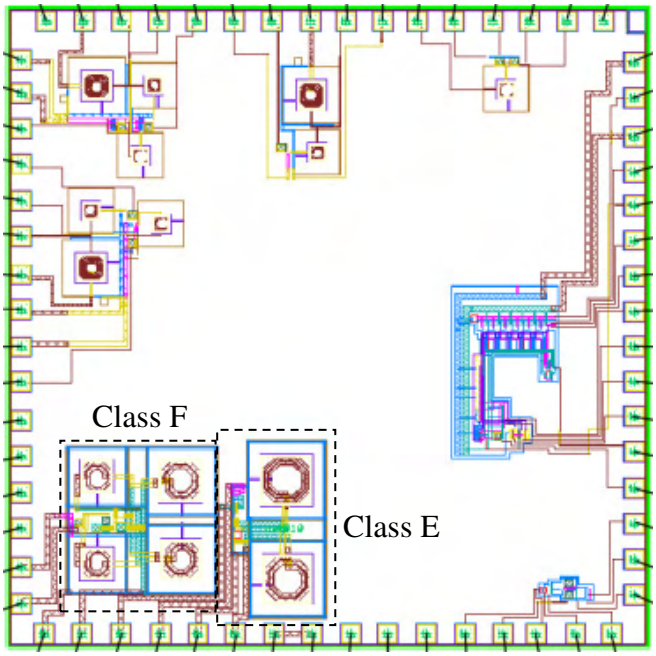


(a)

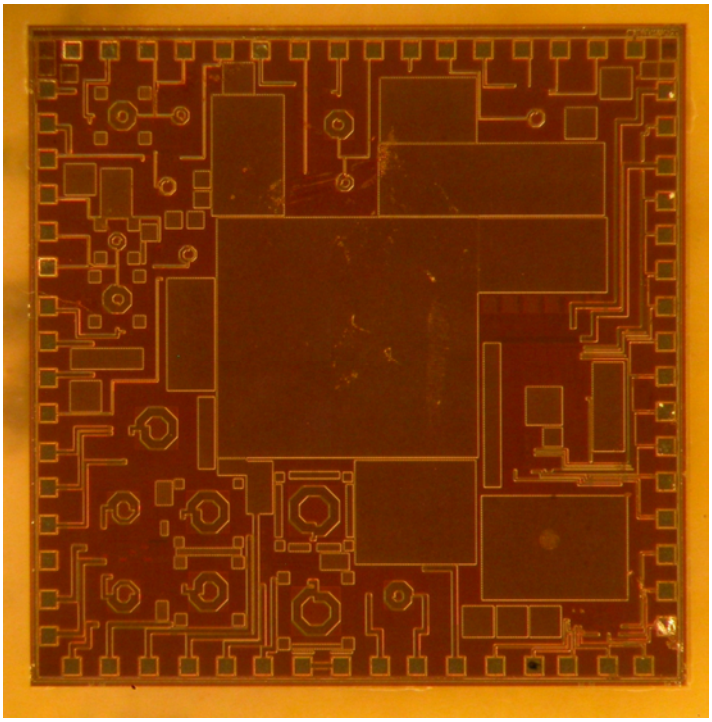


(b)

Figure 6.2. The (a) layout and (b) photo of the Class-F PA.



(a)



(b)

Figure 6.3. Class-E and Class-F PAs within the MPW: (a) layout and (b) photo.

6.2.2 Packaging

The two PA configurations fabricated formed a part of a joint MPW run with two other research projects on the same chip. Therefore, the IC packaging has been chosen by group decision. The dies were packaged using quad flat no-lead (QFN) packages and soldered

onto a PCB for testing purposes. A 64 pin QFN package, shown in Figure 6.4 has been used. The typical bond wire inductance is between 1 and 2 nH.

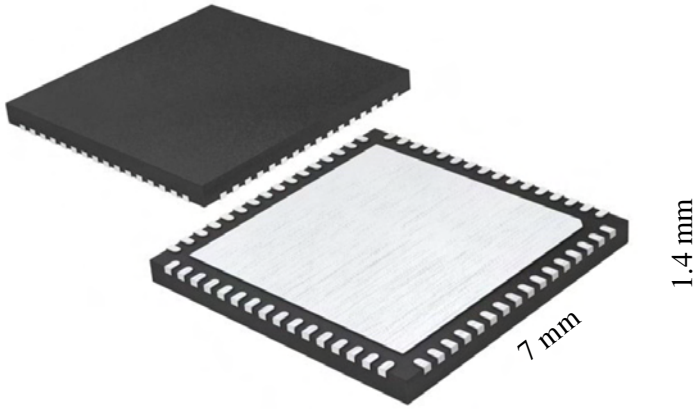


Figure 6.4. The 64-pin QFN package.

Figure 6.5 shows a PA (Class-E or Class-F) in relation to bondpad and bondwire capacitances (modelled as 57 pF), bondwire inductances (modelled as 1 nH), RFC inductance (~1.8 nH at 50 mA current [112]) and resistance (30 Ω) and 50 Ω antenna.

6.2.3 Package simulations

Two techniques, *S*-parameters and power sweep, were identified as suitable measurement techniques for the fabricated system. Measurements were performed with the aid of the network analyzer described in Section 3.6. Although traditionally switch-mode PAs are analyzed by probing of the transient response waveforms, as done in Chapter 4, this method is impractical for packaged ICs. Power sweep, in addition to *S*-parameter measurements, allows for the investigation of output power capability and presents a good practical alternative to waveform probing. Nonlinear measurement techniques, such as THD, were not deemed paramount in this case due to switch-mode nature of Class-E and Class-F PAs.

The choice of biasing voltage (near-to-class-B) enabled the highest output power, as discussed in Chapter 5. Off-chip input matching was omitted for the simplicity of the measurement setup. Although this approach results in the apparent lower PAE, this was acceptable for measurement purposes.

Figure 6.6 and Figure 6.7 show the simulated output *S*-parameters for the packaged Class-E and Class-F configurations respectively. From these figures, a slight phase shift

can be seen for the Class-F PA, whilst larger shift is seen in the case of the Class-E PA. These shifts are attributed to packaging parasitics. Power sweeps for frequencies where highest gain occurs for both Class-E and Class-F configurations are shown in Figure 6.8 and Figure 6.9, respectively.

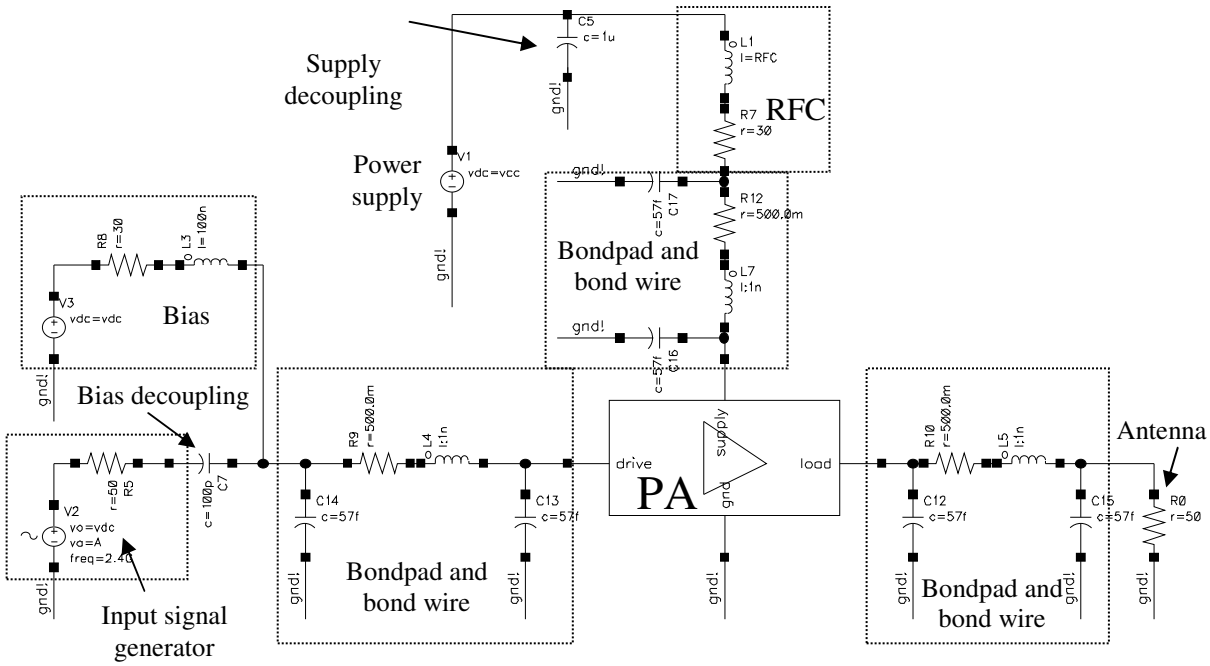


Figure 6.5. The PA in relation to bondpad and bondwire capacitances, bondwire inductances, RFC inductance and resistance, and the antenna.

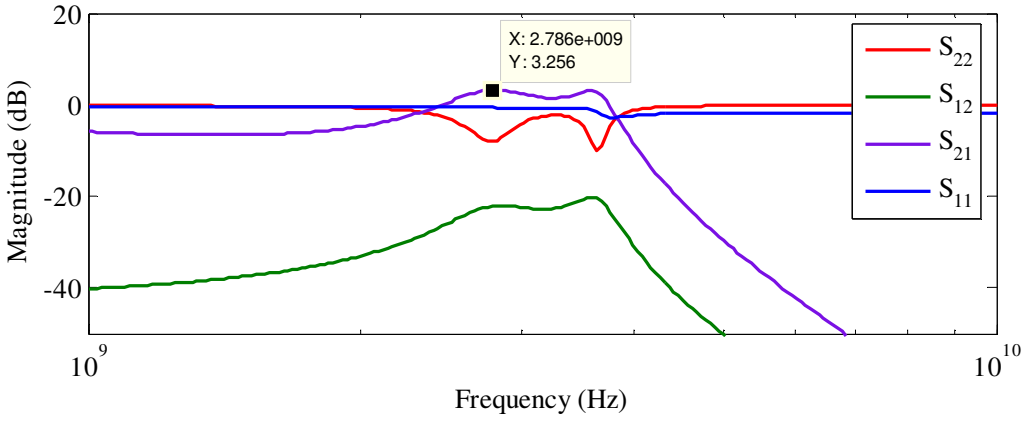


Figure 6.6. The simulated *S*-parameter response of the fabricated Class-E PA.

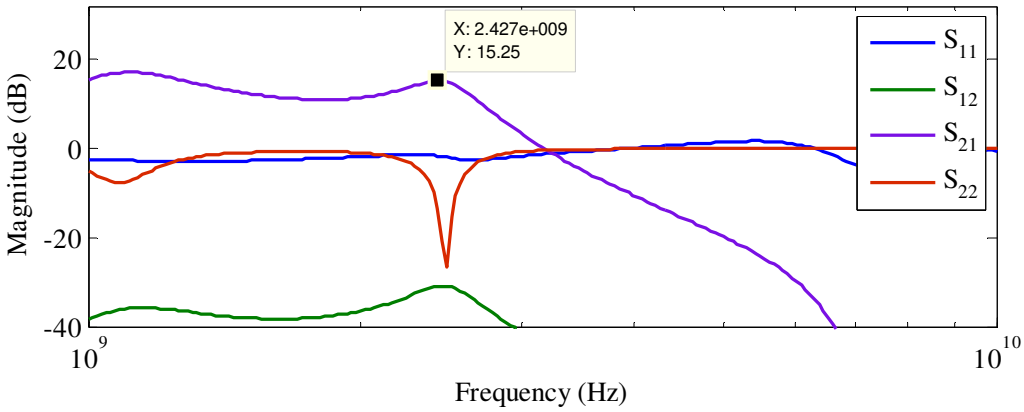


Figure 6.7. The simulated *S*-parameter response of the fabricated Class-F PA.

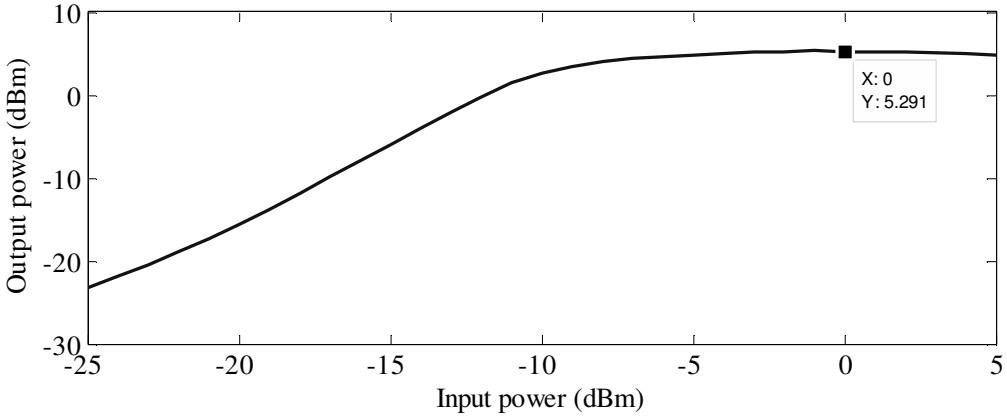


Figure 6.8. The simulated power sweep response of the fabricated Class-E PA.

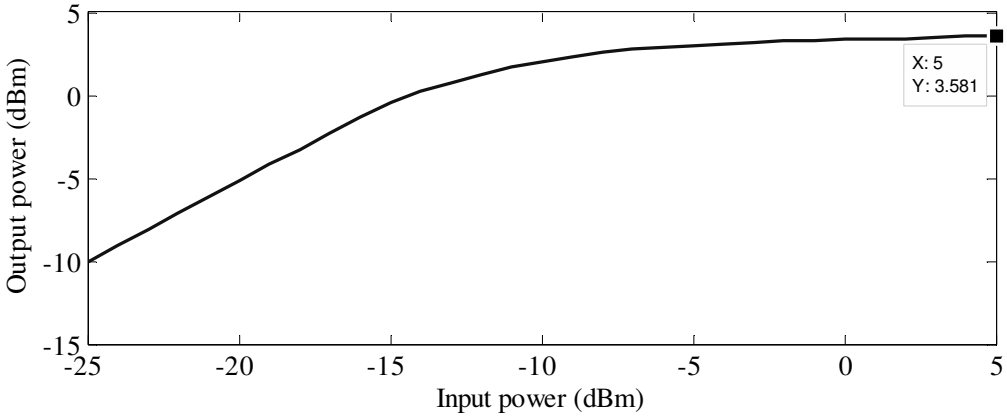


Figure 6.9. The simulated power sweep response of the fabricated Class-F PA.

6.2.4 The PCB design

A 4 layer RF PCB to be used for testing has been designed by a third party. Due to space constraints, the SubMiniature version A (SMA) connectors [113] had to be placed far away from the IC which brought additional mismatch at the output. The high quality RF chokes

have been used with the inductance of 1.8 nH at 50 mA current. The photograph of the populated PCB is shown in Figure 6.10.

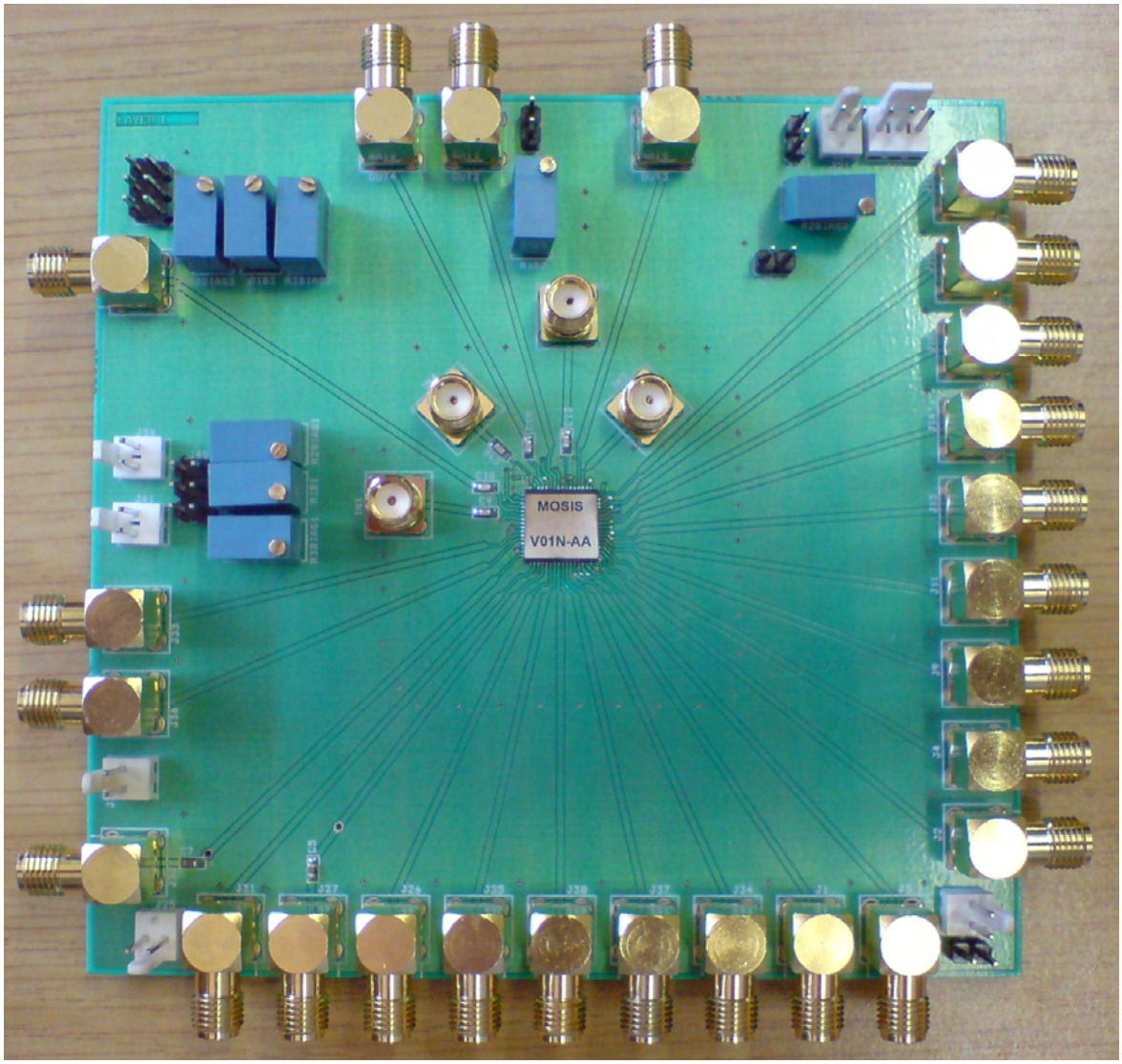


Figure 6.10. The photograph of the populated PCB.

6.2.5 Measurement results

The measurement setup was designed in such a way as to resemble the simulation setup as close as possible. However, due to mismatches and imperfections of the PCB, track and connector attenuation had to be measured at the frequencies of interest and compensated for when presenting the results. The measured *S*-parameters of Class-E PA are shown in Figure 6.11.

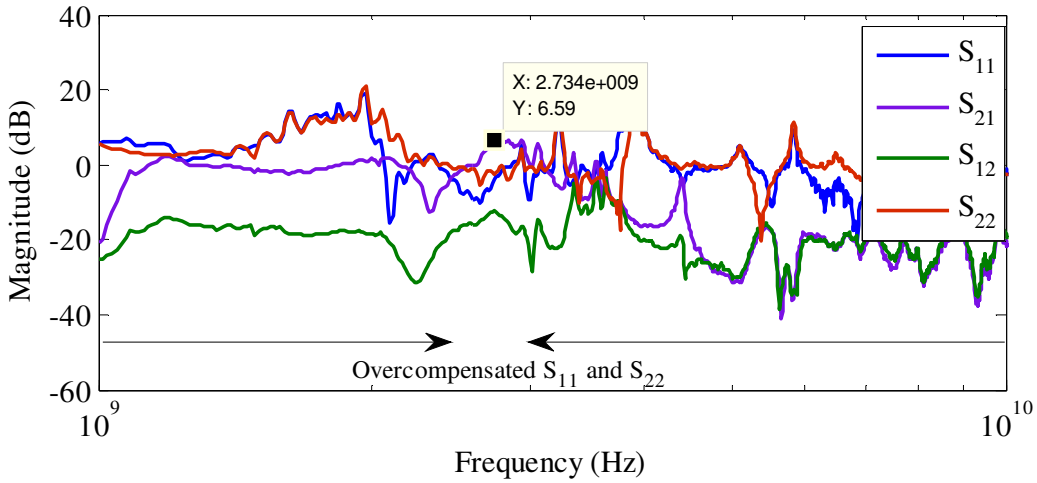


Figure 6.11. The measured *S*-parameter response of the fabricated Class-E PA.

Sound correspondence can be seen between *S*-parameters in the Figure 6.6 and Figure 6.11, which shows that the fabricated PA behaves as predicted by simulations that included package modelling. A slightly greater magnitude of the forward gain (S_{21}) is seen in the measured results, which is due to the better-than-predicted behaviour of the bond-wires and RFCs. However, some mismatch can be seen at the output (S_{22}), likely due to the inductive behaviour of the SMA connectors. Since no input matching has been done, the flat response of S_{11} can be ignored in this analysis. Positive magnitude of S_{11} and S_{22} below and above the frequency of interest is attributed to the overcompensation of the PCB mismatch.

The measured *S*-parameters of Class-F PA are shown in Figure 6.12.

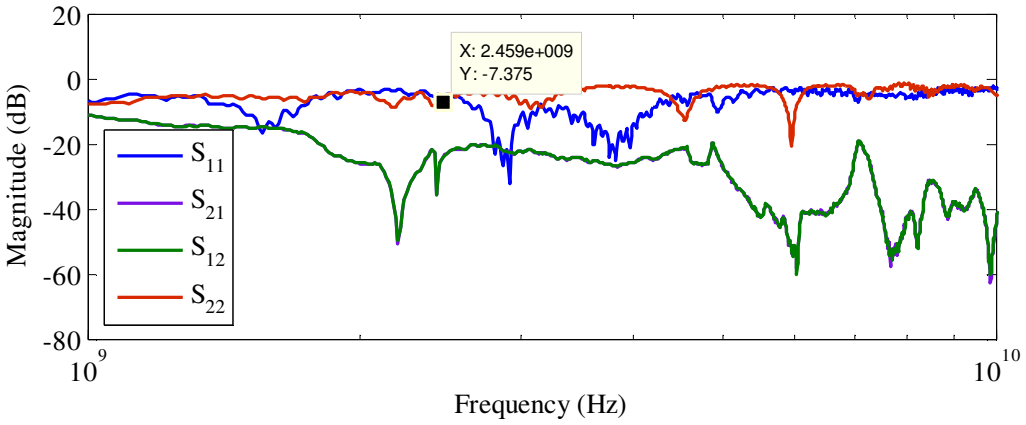


Figure 6.12. The measured *S*-parameter response of the fabricated Class-F PA.

From Figure 6.12, it can be seen that S_{21} and S_{12} lie on top of each other. This shows that the Class-F PA is not operational, most likely due to a short circuit or an open circuit on

the inside of the package or on the PCB (since the PA circuit on silicon itself passed LVS and DRC checks). Such an error was not possible to prove or disprove visually or with the available equipment. However, the trace of S_{22} shows a dip to -7.3 dB close to 2.4 GHz, which confirms the presence of the PA's output matching. It was also established that the PA draws several tens of mA from the voltage supply, which pinpoints the problem towards the input or output connection rather than to a problem with the active device.

The measured power sweep for the Class-E system is shown in Figure 6.13. Power sweep was not performed for the Class-F configuration, due to the problems encountered during *S*-parameter measurements.

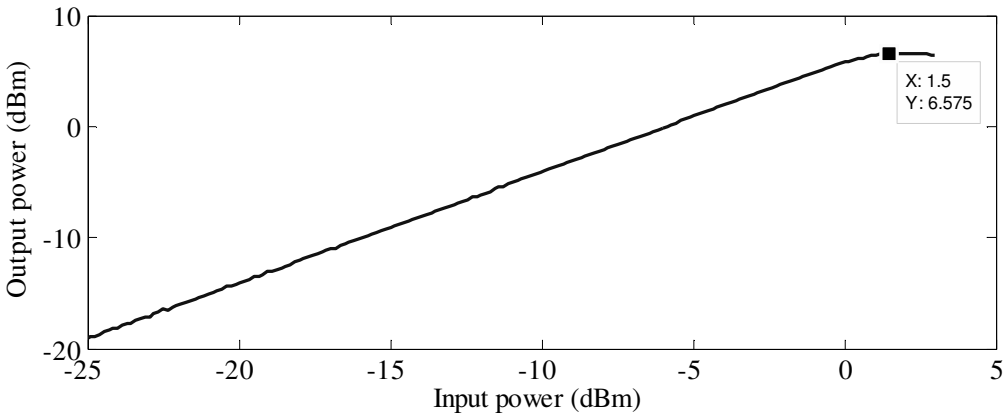


Figure 6.13. The measured power sweep response of the fabricated Class-E PA.

Analysis of Figure 6.13 in conjunction with Figure 6.8 shows a rough correspondence between measured and simulated results. Some difference is seen in the gradient of the output-vs.-input power (power gain) curve, which is attributed to biasing and matching conditions differing due to nonlinearities on the PCB. Measured maximum output power differs from simulated maximum output power by only 1.5 dBm, with both simulated and measured powers reaching more than 5 dBm. This difference is attributed to bond-wire and package parasitics, a discrepancy that was also seen in the case of *S*-parameter measurements.

6.3 CONCLUSION

This chapter presented experimental means of verifying the core software routines presented in this thesis. The spiral inductor design routine was analyzed by means of measured data provided by the AMS, while in order to characterize the routine for the full system integration, layouts of the PA circuits were submitted for fabrication. Fabrication

was however achieved using a technology node from IBM, due to a fabrication grant to the University, yet also served to confirm the versatility of the algorithms. The packaging and PCB design were also discussed. Measured results have been compared against simulated waveforms in terms of *S*-parameters as well as power sweep.

CHAPTER 7 CONCLUSIONS AND IMPLICATIONS

7.1 INTRODUCTION

Chapter 1 and Chapter 2 dealt with the initial research question and hypothesis and a comprehensive literature review in order to establish a foundation for its answer. The research question dealt with looking for a method that can be employed to speed up the design on PAs and their passives for a range of wireless applications while retaining the high quality of amplification. Chapter 3 focused on the methodology of the research procedure and specified the process essentials and tools that were used. Chapter 4 highlighted design routine that lead to Chapter 5, which documented the simulation results supporting the research hypothesis. The layouts of two PAs submitted for fabrication as well as measurement results and their analyses were described in Chapter 6.

The goal of this chapter is to make critical evaluation conclusion of all the research and data gathered in this thesis, and summarize this in a final, concluding section that emphasizes the theories and hypothesis. This is backed up with suggestions for future research on this topic.

7.2 CONCLUSIONS ABOUT THE RESEARCH PROBLEM

In Section 1.2 it was hypothesized that the equations describing the PA and inductor models can be used as a starting point in the development of a set of algorithms which should allow the best possible PA to be found and designed for a given set of specifications such as the PA bandwidth, centre frequency and class of operation. It was is also hypothesized that another set of algorithms can be used to determine geometry of a spiral inductor that gives the highest possible Q-factor, using process parameters for a particular process.

The hypothesis was proven by applying a developed routine to successfully synthesize a number of inductors for the AMS S35 process as well as to design a number of switch-mode PAs utilising the same spiral inductors.

The accuracy of the single-π model used for describing the inductor, the main passive component of any PA, has been verified by comparison between the results based on modelling and results based on EM simulations performed in Cadence Virtuoso Spiral Inductor Modeler, allowing the characterisation of a large number of inductor geometries. This also allowed for verification of the developed spiral inductor search algorithm, due to the fact that 3M and TM inductors designed by the inductor search algorithm could now be verified by EM simulations. Experimentally, a number of square planar spiral 3M and TM inductors were identified to have been characterized by the AMS. The comparison was made between the results obtained by calculations based on modelling and experimental results given by AMS; and it was established that the model analyzes the inductance value of inductors with an average relative error of 3.6 %. With Q-factors taken in evaluation, it has been established that average relative errors differ, with error being as low as 3.9 % for 3M inductors and as high as 34 % for TM inductors. The latter discrepancy has been explained by the fact that for inductor structures with less prominent influence of substrate parasitic, the simplistic assumption of the series RL circuit for the spiral itself yields a pessimistic Q-factor estimate.

This research also shows that with the correct design method which includes optimisation for operation at correct frequency, quality factors in excess of 10 can be obtained for square spiral inductors without resorting to any of techniques described in Sections 2.3.1.2, 2.3.1.3 or 2.3.1.5.

Sections 2.2.5.2 and 2.2.5.3, theorize that in high power and low voltage supply applications, antenna resistances reaching values of less than 10 Ω would be needed for an optimum PA performance. This research proved this practical and provided algorithms that automate impedance matching from designed to standard antenna impedances (50 Ω).

The largest contribution of this research was a set of *algorithms for designing the switch-mode PAs*. Simulations were used to determine that for the complete routine-driven PA system design, that includes output matching and utilisation of real (spiral) inductors, the switch-mode power amplifiers for 50 Ω load at 2.4 GHz centre frequency can be designed applying the streamlined method of this research for the power output of about 6 dB less than aimed. This power loss was expected, and it can be attributed to the non-ideal

properties of the driving transistor and Q-factor limitations of integrated inductors, all of which was described in detail in the literature review in Chapter 2.

Additional algorithms, such as one for the SPICE netlist extraction and the spiral inductor layout extraction into industry accepted CIF and GDS II formats were found beneficial for the ease of manipulation with designed PAs as well as the inductor structures. This presents a step forward towards designing a compact EDA tool.

The layouts of two full PA configurations (one Class-E and one Class-F) implementing spiral inductors have been fabricated in the IBM 7WL SiGe BiCMOS process for the purpose of obtaining the measured results. Although the first designs were completed in the AMS S35 process, this allowed for confirmation of the theorized fact that while all results presented in this thesis were obtained for a single fabrication process, the principles devised in this research are technology independent and that they can be used with different BiCMOS processes, as long as process parameters are made available before carrying out the design. Naturally, in the BiCMOS process, the active device chosen is an HBT; but the choice of the active device is arbitrary and depends on the application, with the recommendation that wide transistor structures should be used to physically support high currents; meaning that a CMOS process with NMOS as driving transistor can be used should the need arise (for an example of a CMOS implementation related to this thesis please see [107]). Upon fabrication, the aspects that cannot be covered in simulations, such as the influence of parasitics, have been investigated. It was established that, at least in the case of Class-E amplifier, they corresponded well with the simulations that included packaging parasitics.

All algorithms presented in this research were devised in MATLAB. Flow diagrams of all design algorithms were presented in Chapter 4, while the complete listings of the MATLAB routines utilising them are given in Appendix A.

7.3 IMPLICATIONS FOR THE THEORY

This research leaves two major implications to the existing theory.

- In Chapter 2 it was seen that although the theory of switch-mode PAs is well developed, streamlined approach is generally not employed when designing PAs. Classic design models, some even dating back to 1975 (Sokal), have been interrelated into a set of algorithms that will enable rapid PA design.

- The existing theory involving monolithic spiral inductor design was expanded by means of addition of the spiral inductor design algorithm. Although spiral inductor design algorithms were intended to expand the existing body of knowledge for designing PAs, they implicitly expand the theory of any application that requires integrated inductors, such as LNAs, DC to DC converters or VCOs.

7.4 IMPLICATIONS FOR FUTURE RESEARCH

Suggestions for the improvement and expansion of the concepts derived in this work for future research are given below.

- The method devised in this research analyzes only one type of spiral inductors, viz. square spiral single-layered inductors (with the exception of octagonal inductors briefly tackled in Chapter 6). Various spiral inductor configurations have been researched in Section 2.3.2, and the routine could be expanded to include different spiral inductor options, such as spirals of different geometries (e.g. hexagonal or circular), or tapered or multi-layered spirals.

- In modelling the spiral inductors, it has been assumed that there was no ground plane between the spiral and the substrate. The IBM 7WL process developers offer inductors with two types of ground planes in their standard library [101], which result in two different sets of Q-factors. The modelling of inductors could be expanded to cater for different ground planes available in different processes.

- It was observed that in certain cases, the calculated Q-factor had been underestimated. The inductor design algorithms could be improved by replacing the simple single-π inductor model with one of the more advanced models, all described in Section 2.3.2.3. This, however, would require more input parameters to the routine, and the inductance search algorithm would take longer to converge.

- The method looks into only two types of switch-mode PAs, i.e. Class-E and Class-F. It could be expanded to include inverse classes, such as Class F^{-1}, or hybrid classes, such and Class EF into the list of PA configurations available for the design.

- An attempt could be made to streamline the design of classic (i.e. non switch-mode) PAs.

- The method devised here deals only with output impedance matching. Therefore, in Section 4.6, a cut-and-try method grounded on simulation-based *S*-parameters analysis is proposed in case an input impedance matching is needed to complete the design. The theory could be expanded to devise algorithms for input impedance matching as well, which would make the system design routine more complete.

- As stated earlier in this chapter, although spiral inductor design algorithms were intended for the use with PAs, they could also be used as a starting point for devising algorithms for other devices that make use of inductors, for example for an LNA described in [18]. If such algorithms are combined with the PA algorithms presented in this work, a complete RF amplifier EDA software package could be obtained.

- As stipulated in Chapter 2, as frequency of operation increases beyond about 20 GHz (microwave as opposed to RF frequencies), it becomes possible to utilise transmission lines instead of passive components for the PA design as well as for the matching. The transmission line theory could be researched in order to expand the algorithms of this thesis for the use in millimetre-wave applications [114, 115].

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APPENDIX A MATLAB CODE

A.1 INTRODUCTION

Appendix A lists the MATLAB code for all sub-routines of the program for the complete PA design integration. The sub-routines are listed in order in which they first appear in the MATLAB code, starting with the main PA design program.

A.2 MAIN PA DESIGN PROGRAM

Figure A.1 and Figure A.2 show the MATLAB code for the main subroutine of the PA design program (paprog.m).

```
try
    clear all; %Clear all variables from workspace
    fprintf('Welcome to PA Design Program v2.0.0\n\n');
    choice = 0;
    inductor = zeros(1,10); %declare array size 10
    while (choice ~= 1 && choice ~= 2)
        choice = input('Please enter 1 for Class-E Amplifier design or 2 for Class-F
Amplifier design: ');
        if (choice ~= 1 && choice ~= 2)
            fprintf('Wrong entry. Please try again.\n');
        end
    end
    if (choice == 1)
        classE; %Class-E PA design program
    end
    if (choice == 2)
        classF; %Class-F PA design program
    end
    %Impedance matching
    wo = 2*pi*fo; %Calc. radian frequency
    cmat = input('\nDo you want to perform the impedance matching to 50 ohm antenna
impedance (y/n)? ', 's');
    if cmat == 'y' || cmat == 'Y';
        %impedance
        BW = input('\nPlease enter the matching bandwidth (MHz): '); %Input bandwidth
        BW = BW * 1e6;
        RS = RL; %Source resistance
        RL = 50; %Load resistance
        QL = fo/BW; %Quality factor
        calcMatch;
    end%if
    %cnet - flag - if selected, matching will be performed
    cnet = input('\nDo you want to export the netlist of the PA (y/n)? ', 's');
fprintf('\n');
    if cmat == 'y' || cmat == 'Y';
        %cind - flag - if selected, spiral inductors will be found
cind = input('\nDo you want to attempt to find inductor(s) for the PA (y/n)? ', 's');
    end

    if (cind == 'y' || cind == 'Y') || (cnet == 'y' || cnet == 'Y');
        %Overrides any inductor values if needed
        overrideInductors;
    end
```

Figure A.1. MATLAB code of the main subroutine of the PA design program.

```
    fprintf('\n');
    if cind == 'y' || cind == 'Y';
        %Find inductors
        %Define constants
        b = 1.62e-3;
        a1 = -1.21;
        a2 = -0.147;
        a3 = 2.40;
        a4 = 1.78;
        a5 = -0.030;
        f = fo;
        omega = wo;
        %Setup the inductance search algorithm search paramters
        indSetup;
        if cnet == 'y' || cnet == 'Y';
            %Name of the PA used for netlist extraction
            paName = input('\nPlease enter the PA name (press "s" to skip): ', 's');
            if paName(1) == 's' || paName(1) == 'S';
                %Default PA name
                paName = 'MyPA';
            end%if
            RFC = 1;
            fileName = strcat(paName, '_net.spc');
            fid = fopen(fileName, 'w');
        end
        fprintf('\nINDUCTORS\n');
            %Find the inductors designed by the PA program
            findInductors;
        end
        %Export the netlist
        exportPA;
    catch
        fprintf('MATLAB returns: \n%s\nError occurred while running the program.
    Please try running the program again.\n\n', lasterr);
    end%try
```

Figure A.2. MATLAB code of the main subroutine of the PA design program (continued).

A.3 CLASS-E DESIGN SUBROUTINE

Figure A.3 and Figure A.4 show the MATLAB code for the Class-E design subroutine (ClassE.m).

```
%Enter PA design parameters
fo = input('Please enter the frequency of operation, fo (MHz): ');
if (fo <= 0)
    fo = 1e9; %Frequency
else
    fo = fo * 1e6;
end
w = 2*pi*fo; %Radian frequency
QL = input('Please enter the loaded quality factor, QL: ');
if (QL < 1)
    QL = 10; %Loaded quality factor
end
Po = input('Please enter the required output power, Po (mW): ');
if (Po <= 0)
    Po = 0.01; %Output power
else
    Po = Po/1000;
end
Vcc = input('Please enter the value of the regulated power supply (Vcc/Vdd): ');
if (Vcc <= 0)
    Vcc = 1; %Power supply
end
VCEsat = input('Please enter VCEsat/VDSsat (-1 to skip): ');
if (VCEsat <= 0)
    VCEsat = 0; %Saturation VCE voltage
end

Lmax = input('Please enter the highest allowed inductance (nH) (-1 to skip): ');
if (Lmax <= 0)
    Lmax = 0; %Maximum inductance
else
    Lmax = Lmax * 1e-9;
end
Lmin = input('Please enter the lowest allowed inductance (nH) (-1 to skip): ');
if (Lmin <= 0)
    Lmin = 0; %Minimum inductance
else
    Lmin = Lmin * 1e-9;
end

BVCE = input('Please enter collector-emiiter breakdown voltage (V) (-1 to skip): ');
if (BVCE <= 0)
    BVCE = 0; %Breakdown voltage
end

%Calculate
vcp = 3.56 * Vcc;
if (vcp > BVCE && BVCE > 0)
    NVcc = BVCE / 3.56;
    fprintf('Warning: Vcc should not exceed %.2f or the transistor will go into
breakdown!\n', NVcc);
end
RL = 0.577*(Vcc - VCEsat)^2/Po; %Load resistance
L2 = QL*RL/w; %Series inductance
C1 = 1/(w*RL*5.447); %Parallel capacitance
C2 = C1*(5.447/QL)*(1+1.42/(QL - 2.08)); %Series Capacitance

Idc = Vcc / (1.734*RL); %DC current consumption
isp = 2.86 * Idc; %Maximum collector current dissipation

%Q-factor adjustment
if (Lmax ~= 0)
    if (L2 > Lmax)
```

Figure A.3. MATLAB code for the Class-E design subroutine.

```
        QLB = w*Lmax/RL;
        if (QLB > 1)
        L2 = Lmax;
            C2 = C1*(5.447/QLB)*(1+1.42/(QLB - 2.08));
            fprintf('New QL = %.2f \n', floor(100 * QLB + 0.5) / 100);
        else
            fprintf('Cannot find QL greater than 1 to keep L2 <= Lmax\n');
        end
    end
end

if (Lmin ~= 0)
    if (L2 < Lmin)
        QLB = w*Lmin/RL;
        L2 = Lmin;
        C2 = C1*(5.447/QLB)*(1+1.42/(QLB - 2.08));
        fprintf('New QL = %.2f \n', floor(100 * QLB + 0.5) / 100);
    end
end

%Display calculated values
fprintf('\nRESULTS:\n');
fprintf('RL = %.2f Ohm \n', floor(100 * RL + 0.5) / 100);
fprintf('L2 = %.2f nH \n', floor(1e11 * L2 + 0.5) / 100);
fprintf('C2 = %.3f pF \n', floor(1e14 * C2 + 0.5) / 100);
fprintf('C1 = %.3f pF \n', floor(1e14 * C1 + 0.5) / 100);
fprintf('Idc = %.2f mA \n', floor(1e5 * Idc + 0.5) /100);
fprintf('vcp = %.2f V \n', floor(1e2 * vcp + 0.5) / 100);
fprintf('isp = %.2f mA \n', floor(1e5 * isp + 0.5) / 100);

Lfeed = 0;
```

Figure A.4. MATLAB code for the Class-E design subroutine (continued).

A.4 CLASS-F DESIGN SUBROUTINE

Figure A.5 and Figure A.6 show the MATLAB code for the Class-F design subroutine (ClassF.m).

```
%Enter PA design parameters
harmonics = 0;
%Choose between the 3 and 5 harmonic designs
while (harmonics ~= 1 && harmonics ~= 2)
    harmonics = input('Please enter 1 for 3-harmonic design or 2 for 5-harmonic design:
');
    if (harmonics ~= 1 && harmonics ~= 2)
       fprintf('Wrong entry. Please try again.\n');
    end
end
fo = input('Please enter the frequency of operation, fo (MHz): ');
if (fo <= 0)
    fo = 1e9; %Frequency of operation
else
    fo = fo * 1e6;
end
w = 2*pi*fo;
Po = input('Please enter the required output power, Po (mW): ');
if (Po <= 0)
    Po = 0.01; %Output power
else
    Po = Po/1000;
end
Vcc = input('Please enter the value of the regulated power supply (Vcc/Vdd): ');
if (Vcc <= 0)
    Vcc = 1; %Voltage supply
end
BVCE = input('Please enter collector-emiiter breakdown voltage (V) (-1 to skip): ');
if (BVCE <= 0)
    BVCE = 0; %Collector-emitter breakdown voltage
end
L0 = input('Please enter the inductance for the base filter (nH): ');
if (L0 <= 0)
    L0 = 1e-9; %Base filter inductance
else
    L0 = L0 * 1e-9;
end
L3 = input('Please enter the inductance for the third harmonic filter (nH): ');
if (L3 <= 0)
    L3 = 1e-9; %Third harmonic filter inductance
else
    L3 = L3 * 1e-9;
end
if harmonics == 2;
    L5 = input('Please enter the inductance for the fifth harmonic filter (nH): ');
    if (L5 <= 0)
        L5 = 1e-9; %Fifth harminic filter inductance
    else
        L5 = L5 * 1e-9;
    end
else
    L5 = 0;
end

if harmonics == 1
    %third harmonic peaking circuit coefficients
    dV = 2;
    gV = 1.1547;
    dI = 2.91;
    gI = 1.4142;
else
    %5 resonators circuit coefficients
    dV = 2;
```

Figure A.5. MATLAB code for the Class-F design subroutine.

```
    gV = 1.2071;
    dI = 3;
gI = 1.5;
end

%Calculate optimum resistance and waveforms
RL = gV^2*Vcc^2/(2*Po);
Vom = gV*Vcc;
vCm = dV*Vcc;
Idc = gV*Vcc/(gI*RL);
iCm = dI*Idc;
A = 2*acos(Idc/(Idc-iCm));

%Calculate Filters
%base
C0 = 1/((2*pi*fo)^2*L0);
%3rd harmonic
C3 = 1/((2*pi*3*fo)^2*L3);
if harmonics == 2;
    C5 = 1/((2*pi*5*fo)^2*L3);
end
%Display calculated values
fprintf('\nRESULTS:\n');
fprintf('RL = %.2f Ohm \n', floor(100 * RL + 0.5) / 100);
fprintf('L0 = %.2f nH \n', floor(1e11 * L0 + 0.5) / 100);
fprintf('C0 = %.3f pF \n', floor(1e14 * C0 + 0.5) / 100);
fprintf('L3 = %.2f nH \n', floor(1e11 * L3 + 0.5) / 100);
fprintf('C3 = %.3f pF \n', floor(1e14 * C3 + 0.5) / 100);
if harmonics == 2;
    fprintf('L5 = %.2f nH \n', floor(1e11 * L5 + 0.5) / 100);
    fprintf('C5 = %.3f pF \n', floor(1e14 * C5 + 0.5) / 100);
end
fprintf('Idc = %.2f mA \n', floor(1e5 * Idc + 0.5) /100);
fprintf('vCm = %.2f V \n', floor(1e2 * vCm + 0.5) / 100);
fprintf('Vom = %.2f V \n', floor(1e2 * Vom + 0.5) / 100);
fprintf('iCm = %.2f mA \n', floor(1e5 * iCm + 0.5) / 100);

if (vCm > BVCE && BVCE > 0)
    NVcc = BVCE / dV;
    fprintf('Warning: Vcc should not exceed %.2f or the transistor will go into
breakdown!\n', NVcc);
end
```

Figure A.6. MATLAB code for the Class-F design subroutine (continued).

A.5 IMPEDANCE MATCHING

Figure A.7 and Figure A.8 show the MATLAB code for the impedance matching subroutine (calcMatch.m).

```
%L network
LM = 1/wo * (RL^2*RS / (RL - RS))^(1/2);
CM = 1/wo * (RL^2 + (wo*LM)^2) / (RL^2 * wo * LM);

%Results for L network
fprintf('\nL network: \n');
fprintf('LM = %.3f nH\n', floor(1e11 * LM + 0.5) / 100);
fprintf('CM = %.3f pF\n', floor(1e14 * CM + 0.5) / 100);
```

Figure A.7. MATLAB code for the impedance matching subroutine.

```
%T networks
Rsmall = RS;
if RL < Rsmall
    Rsmall = RL;
end
R = Rsmall*(QL^2 + 1);
XS1 = QL*RS;
XP1 = R/QL;

Q2 = (R/RL - 1)^(1/2);
XP2 = R/Q2;
XS2 = Q2*RL;

CT1 = XP1*XP2/(XP1+XP2);
CT2 = XP1*XP2/abs(XP1-XP2);

LM1 = XS1/wo;
LM2 = XS2/wo;
LM3 = CT1/wo;

CM1 = 1/(CT1*wo);
CM2 = 1/(XS1*wo);
CM3 = 1/(XS2*wo);

%Results for T network
fprintf('\nind-cap-ind T network: \n');
fprintf('L1 = %.3f nH\n', floor(1e12 * XS1/wo + 0.5) / 1000);
fprintf('C1 = %.3f pF\n', floor(1e15 * 1/(CT1*wo) + 0.5) / 1000);
fprintf('L2 = %.3f nH\n', floor(1e12 * XS2/wo + 0.5) / 1000);

fprintf('cap-ind-cap T network: \n');
fprintf('C1 = %.3f pF\n', floor(1e15 * 1/(XS1*wo) + 0.5) / 1000);
fprintf('L1 = %.3f nH\n', floor(1e12 * CT1/wo + 0.5) / 1000);
fprintf('C2 = %.3f pF\n', floor(1e15 * 1/(XS2*wo) + 0.5) / 1000);

%Pi network
RH = RS;
if RL > RH
    RH = RL;
end
R = RH/(QL^2 + 1);
XS2 = QL*R;
XP2 = RL/QL;

Qi = (RS/R - 1)^(1/2);
XP1 = RS/Q2;
XS1 = Qi*R;

CT1 = XS1 + XS2;
CT2 = abs(XS1-XS2);

LM4 = XP1/wo;
LM5 = XP2/wo;
LM6 = CT1/wo;

CM4 = 1/(CT1*wo);
CM5 = 1/(XP1*wo);
CM6 = 1/(XP2*wo);
%Results for Pi network
fprintf('\nind-cap-ind Pi network: \n');
fprintf('L1 = %.3f nH\n', floor(1e12 * XP1/wo + 0.5) / 1000);
fprintf('C1 = %.3f pF\n', floor(1e15 * 1/(CT1*wo) + 0.5) / 1000);
fprintf('L2 = %.3f nH\n', floor(1e12 * XP2/wo + 0.5) / 1000);

fprintf('cap-ind-cap Pi network: \n');
fprintf('C1 = %.3f pF\n', floor(1e15 * 1/(XP1*wo) + 0.5) / 1000);
fprintf('L1 = %.3f nH\n', floor(1e12 * CT1/wo + 0.5) / 1000);
fprintf('C2 = %.3f pF\n', floor(1e15 * 1/(XP2*wo) + 0.5) / 1000);
```

Figure A.8. MATLAB code for the impedance matching subroutine (continued).

A.6 INDUCTANCE VALUE OVERRIDE

Figure A.9 and Figure A.10 show the MATLAB code for the inductance values override subroutine (overrideInductors.m). Any inductance value calculated by the PA design program can be overridden by this subroutine manually if needed.

```
%Overrides any inductance values calculated by PA design program
cov = input('Do you want to override any of the inductance values (y/n)? ', 's');
if cov == 'y' || cov == 'Y';
    if choice == 1;
        fprintf('Old L2 = %.2f nH. ', L2*1e9);
        iL2 = input ('New L2 (-1 to skip): ');
        if iL2 > 0;
            L2 = iL2/1e9;
        end
        fprintf('Old Lfeed = %.2f nH. ', Lfeed*1e9);
        iLfeed = input ('New Lfeed (-1 to skip): ');
        if iLfeed > 0;
            Lfeed = iLfeed/1e9;
        end
    elseif choice == 2;
        fprintf('Old Lfeed = 100.00 nH. ');
        iLfeed = input ('New Lfeed (-1 to skip): ');
        if iLfeed > 0;
            Lfeed = iLfeed/1e9;
        else
            Lfeed = 1e-7;
        end
        fprintf('Old L0 = %.2f nH. ', L0*1e9);
        iL0 = input ('New L0 (-1 to skip): ');
        if iL0 > 0;
            L0 = iL0/1e9;
        end
        fprintf('Old L3 = %.2f nH. ', L3*1e9);
        iL3 = input ('New L3 (-1 to skip): ');
        if iL3 > 0;
            L3 = iL3/1e9;
        end
        if harmonics == 2;
           fprintf('Old L5 = %.2f nH. ', L5*1e9);
           iL5 = input ('New L5 (-1 to skip): ');
            if iL5 > 0;
                L5 = iL5/1e9;
            end
        end
    end
    if cmn == 1;
        fprintf('Old LM = %.2f nH. ', LM*1e9);
        iLM = input ('New LM (-1 to skip): ');
        if iLM > 0;
            LM = iLM/1e9;
        end
    elseif cmn == 2;
        fprintf('Old LM1 = %.2f nH. ', LM1*1e9);
        iLM1 = input ('New LM1 (-1 to skip): ');
        if iLM1 > 0;
            LM1 = iLM1/1e9;
        end
        fprintf('Old LM2 = %.2f nH. ', LM2*1e9);
        iLM2 = input ('New LM2 (-1 to skip): ');
        if iLM2 > 0;
            LM2 = iLM2/1e9;
        end
   elseif cmn == 3;
        fprintf('Old LM3 = %.2f nH. ', LM3*1e9);
        iLM3 = input ('New LM3 (-1 to skip): ');
        if iLM3 > 0;
```

Figure A.9. MATLAB code for the inductance values override subroutine.

```
            LM3 = iLM3/1e9;
        end
    elseif cmn == 4;
        fprintf('Old LM4 = %.2f nH. ', LM4*1e9);
        iLM4 = input ('New LM4 (-1 to skip): ');
        if iLM4 > 0;
            LM4 = iLM4/1e9;
        end
        fprintf('Old LM5 = %.2f nH. ', LM5*1e9);
        iLM5 = input ('New LM5 (-1 to skip): ');
        if iLM5 > 0;
            LM5 = iLM5/1e9;
        end
    elseif cmn == 5;
        fprintf('Old LM6 = %.2f nH. ', LM6*1e9);
        iLM6 = input ('New LM6 (-1 to skip): ');
        if iLM6 > 0;
            LM6 = iLM6/1e9;
        end
    end
else
    %fix feed for Class-F amplifier
    if choice == 2;
        Lfeed = 1e-7;
    end
end
```

Figure A.10. MATLAB code for the inductance values override subroutine (continued).

A.7 SETUP OF INDUCTANCE SEARCH ALGORITHM PARAMETERS

Figure A.11 shows the MATLAB code for the setup of inductance search algorithm parameters (indSetup.m).

```
%Setup the inductance search algorithm search parameters
tolerance = input('Please enter the tolerance for the inductance value (%) (-1 to
skip): ');
if (tolerance <= 0)
    tolerance = 0.01;
else
    tolerance = tolerance/100;
end
resolution = input('Please enter the search grid resolution (um) (-1 to skip): ');
if (resolution <= 0)
    resolution = 1;
end
%Setup the geometry parameters
cminpar = input('Do you want to change any of the default geometry parameters (y/n)? ',
's');
if cminpar == 'y' || cminpar == 'Y'
  dinmin = input('\nPlease enter the minimum value for din (um) (-1 to skip): ');
  if (dinmin < 30)
    dinmin = 30;
    fprintf('Using the default value of %.0f um for minimum din.\n', dinmin);
  end%if
  doutmax = input('Please enter the maximum value for dout (um) (-1 to skip): ');
  if (doutmax <= 0)
    doutmax = 500;
    fprintf('Using the default value of %.0f um for maximum dout.\n', doutmax);
  end%if
  smin = input('Please enter the minimum value for turn spacing s (um) (-1 to skip):
');
  if (smin <= 0)
    smin = 2;
    fprintf('Using the default value of %.0f um for s.\n', smin);
  end%if
  wmin = input('Please enter the minimum turn width w (um) (-1 to skip): ');
  if (wmin <= 0)
    wmin = 2;
    fprintf('Using the default value of %.0f um for w.\n', wmin);
  end%if
else
    %Default parameters
  dinmin = 30;
  doutmax = 500;
  smin = 2;
  wmin = 2;
  fprintf('Using the default values of %.1f, %.1f, %.1f and %.1f for dinmin, doutmax, s
and wmin respectively.\n', dinmin, doutmax, smin, wmin);
end%if
```

Figure A.11. MATLAB code for the setup of inductance search algorithm parameters.

A.8 SEARCH FOR REQUIRED INDUCTORS

Figure A.12 and Figure A.13 show the MATLAB code for the subroutine that searches for inductor geometries of all inductors needed by PA design program (findInductors.m).

```
%Enter inductor process parameters
entProcParam;
if choice == 1;
    Ls = L2*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'L2';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
    if Lfeed ~= 0;
        Ls = Lfeed*1e9;
        fprintf('\nInductor value: %.3f nH',Ls);
        indSearch; %Inductance search algorithm
        if cnet == 'y' || cnet == 'Y';
            inductorName = 'Lfeed';
            exportSubckt; %Exports the spiral inductor subcircuit
        end
    end
elseif choice == 2;
    Ls = L0*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'L0';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
    if L3 ~= L0;
        Ls = L3*1e9;
        fprintf('\nInductor value: %.3f nH',Ls);
        indSearch; %Inductance search algorithm
    end
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'L3';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
    if harmonics == 2;
        if L5 ~= L3;
            Ls = L5*1e9;
            fprintf('\nInductor value: %.3f nH',Ls);
            indSearch; %Inductance search algorithm
        end
        if cnet == 'y' || cnet == 'Y';
            inductorName = 'L5';
            exportSubckt; %Exports the spiral inductor subcircuit
        end
    end
end
if cmn == 1;
    Ls = LM*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'LM';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
end
if cmn == 2;
    Ls = LM1*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'LM1';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
```

Figure A.12. MATLAB code for search for geometries of all needed inductors.

```
    Ls = LM2*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'LM2';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
end
if cmn == 3;
    Ls = LM3*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'LM3';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
end
if cmn == 4;
    Ls = LM4*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'LM4';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
    Ls = LM5*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'LM5';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
end
if cmn == 5;
    Ls = LM6*1e9;
    fprintf('\nInductor value: %.3f nH',Ls);
    indSearch; %Inductance search algorithm
    if cnet == 'y' || cnet == 'Y';
        inductorName = 'LM6';
        exportSubckt; %Exports the spiral inductor subcircuit
    end
end
```

Figure A.13. MATLAB code for search for geometries of all needed inductors (continued).

A.9 PA NETLIST EXPORT

Figure A.14 through to Figure A.16 show the MATLAB code for the subroutine that exports the netlists of designed Class-E or Class-F PA (exportPA.m).

```
%This procedure exports the netlist of Class-E or Class-F PA
if (cnet == 'y' || cnet == 'Y')
    cModel = 0;
    %Input the transistor choice
    while cModel ~= 1 && cModel ~= 2 && cModel ~= 3;
        fprintf('\n');
        cModel = input('Please enter 1 for HBT, 2 RF NMOS or 3 for any other
transistor: ');
    end
    if cModel == 1;
       modelName = input('Please enter the model name (e.g. npn254h5): ', 's');
       if modelName(1) == 's' || modelName(1) == 'S';
            modelName = 'npn254';
       end
        wEmitters = input('Please enter the total emitter width (um) (-1 to skip): ');
        if wEmitters < 0;
            wEmitters = 1;
        end
        transistor = strcat(['X',modelName,'_1 N_1 bias Gnd Gnd ',modelName,' area=',
num2str(wEmitters)]);
    elseif cModel == 2;
        lnmos = input('Please enter the NMOS length (um): ');
        wnmos = input('Please enter the NMOS width (um): ');
        ng = input('Please enter the number of NMOS fingers: ');
        addparam = input('Please type in any additional SPICE parameters in format
PARAM=param ("s" to skip): ', 's');
        if lnmos < 0;
            lnmos = 1;
        end
        if wnmos < 0;
            wnmos = 100;
        end
        if ng < 0;
            ng = 10;
        end
        if addparam(1) == 's'
            addparam = ' ';
        end
        transistor = strcat (['Xnmosrf_1 N_1 bias Gnd Gnd nmosrf l=',num2str(lnmos),'u
wtot=',num2str(wnmos),'u ng=',num2str(ng),' ',addparam]);
    else
        transistor = input('Please type the SPICE command for your transistor: ','s');
    end
end
%Export the netlist
if (cnet == 'y' || cnet == 'Y') && (cind ~= 'y' && cind ~= 'Y') && choice == 1;
        paName = input('\nPlease enter the PA name (press "s" to skip): ', 's');
        if paName(1) == 's' || paName(1) == 'S';
            paName = 'MyPA';
        end%if
        if Lfeed == 0;
            RFC = 100;
        else
            RFC = Lfeed*1e9;
        end
        fileName = strcat(paName, '_net.spc');
        fid = fopen(fileName, 'w');
        fprintf(fid, '.SUBCKT %s bias supply Gnd\n', paName);
        fprintf(fid, 'LRFC_2 supply N_1 %.2fn\n', RFC);
        if cmn == 0;
          fprintf(fid, 'LInductor_2 N_5 N_3 %.2fn\n', floor(1e11 * L2 + 0.5) / 100);
          fprintf(fid, 'RResistor_1 N_3 Gnd %.2f TC=0.0, 0.0\n', floor(100 * RL + 0.5)
/ 100);
```

Figure A.14. MATLAB code for the subroutine used for netlist export.

```
        else
          fprintf(fid, 'LInductor_2 N_5 N_M1 %.2fn\n', floor(1e11 * L2 + 0.5) / 100);
          fprintf(fid, 'RResistor_1 N_M2 Gnd %.2f TC=0.0, 0.0\n', 50);
        end
        fprintf(fid, transistor);
        fprintf(fid, '\n');
        if Lfeed == 0;
          fprintf(fid, 'CCapacitor_1 N_1 Gnd %.2fp\n', floor(1e14 * C1 + 0.5) / 100);
        else
          fprintf(fid, 'CCapacitor_1 N_1 Gnd %.2fp\n', floor(1e14 * Cp + 0.5) / 100);
        end
        fprintf(fid, 'CCapacitor_2 N_1 N_5 %.2fp\n', floor(1e14 * C2 + 0.5) / 100);
        matchIdeal; %Export matching inductors
        fprintf(fid, '.ENDS\n');
        fclose(fid);
        fprintf('File %s created successfully.\n\n', fileName);
    end

    if (cnet == 'y' || cnet == 'Y') && (cind == 'y' || cind == 'Y') && choice == 1;
        fprintf(fid, '.SUBCKT %s bias supply Gnd\n', paName);
        if Lfeed == 0;
          RFC = 100;
          fprintf(fid, 'LRFC_2 supply N_1 %.2fn\n', RFC);
        else
          fprintf(fid, 'XLfeed_1 supply N_1 Gnd Lfeed\n');
        end
        if cmn == 0;
          fprintf(fid, 'XL2_1 N_5 N_3 Gnd L2\n');
          fprintf(fid, 'RResistor_1 N_3 Gnd %.2f TC=0.0, 0.0\n', floor(100 * RL + 0.5)
/ 100);
        else
          fprintf(fid, 'XL2_1 N_5 N_M1 Gnd L2\n');
          fprintf(fid, 'RResistor_1 N_M2 Gnd %.2f TC=0.0, 0.0\n', 50);
        end
        fprintf(fid, transistor);
        fprintf(fid, '\n');
        fprintf(fid, 'CCapacitor_1 N_1 Gnd %.2fp\n', floor(1e14 * C1 + 0.5) / 100);
        fprintf(fid, 'CCapacitor_2 N_1 N_5 %.2fp\n', floor(1e14 * C2 + 0.5) / 100);
        matchSpiral; %Export matching inductors
        fprintf(fid, '.ENDS\n');
        fclose(fid);
        fprintf('File %s created successfully.\n\n', fileName);
    end

  if (cnet == 'y' || cnet == 'Y') && (cind ~= 'y' && cind ~= 'Y') && choice == 2;
        paName = input('\nPlease enter the PA name (press "s" to skip): ', 's');
        if paName(1) == 's' || paName(1) == 'S';
          paName = 'MyPA';
        end%if
        fileName = strcat(paName, '_net.spc');
        fid = fopen(fileName, 'w');
        RFC = Lfeed*1e9;
        fprintf(fid, '.SUBCKT %s bias supply Gnd\n', paName);
        fprintf(fid, 'LRFC_2 supply N_1 %.2fn\n', RFC);
        fprintf(fid, 'CCapacitor_3 N_1 N_4 %.2fp\n', 1);
        if cmn == 0;
          fprintf(fid, 'LInductor_2 N_2 Gnd %.2fn\n', floor(1e11 * L0 + 0.5) / 100);
          fprintf(fid, 'CCapacitor_1 N_2 Gnd %.2fp\n', floor(1e14 * C0 + 0.5) / 100);
          if harmonics == 1;
            fprintf(fid, 'LInductor_1 N_4 N_2 %.2fn\n', floor(1e11 * L3 + 0.5) / 100);
            fprintf(fid, 'CCapacitor_2 N_4 N_2 %.2fp\n', floor(1e14 * C3 + 0.5) / 100);
          end
          if harmonics == 2;
            fprintf(fid, 'LInductor_1 N_4 N_3 %.2fn\n', floor(1e11 * L3 + 0.5) / 100);
            fprintf(fid, 'CCapacitor_2 N_4 N_3 %.2fp\n', floor(1e14 * C3 + 0.5) / 100);
            fprintf(fid, 'LInductor_3 N_3 N_2 %.2fn\n', floor(1e11 * L5 + 0.5) / 100);
            fprintf(fid, 'CCapacitor_4 N_3 N_2 %.2fp\n', floor(1e14 * C5 + 0.5) / 100);
          end
          fprintf(fid, 'RResistor_1 N_2 Gnd %.2f TC=0.0, 0.0\n', floor(100 * RL + 0.5)
/ 100);
```

Figure A.15. MATLAB code for the subroutine used for netlist export (continued).

```
        else
          fprintf(fid, 'LInductor_2 N_M1 Gnd %.2fn\n', floor(1e11 * L0 + 0.5) / 100);
          fprintf(fid, 'CCapacitor_1 N_M1 Gnd %.2fp\n', floor(1e14 * C0 + 0.5) / 100);
          if harmonics == 1;
            fprintf(fid, 'LInductor_1 N_4 N_M1 %.2fn\n', floor(1e11 * L3 + 0.5) / 100);
            fprintf(fid, 'CCapacitor_2 N_4 N_M1 %.2fp\n', floor(1e14 * C3 + 0.5) /
100);
          end
          if harmonics == 2;
            fprintf(fid, 'LInductor_1 N_4 N_3 %.2fn\n', floor(1e11 * L3 + 0.5) / 100);
            fprintf(fid, 'CCapacitor_2 N_4 N_3 %.2fp\n', floor(1e14 * C3 + 0.5) / 100);
            fprintf(fid, 'LInductor_3 N_3 N_M1 %.2fn\n', floor(1e11 * L5 + 0.5) / 100);
            fprintf(fid, 'CCapacitor_4 N_3 N_M1 %.2fp\n', floor(1e14 * C5 + 0.5) /
100);
          end
          fprintf(fid, 'RResistor_1 N_M2 Gnd %.2f TC=0.0, 0.0\n', 50);
        end

        fprintf(fid, transistor);
        fprintf(fid, '\n');
        matchIdeal; %Export matching inductors
        fprintf(fid, '.ENDS\n');
        fclose(fid);
        fprintf('File %s created successfully.\n\n', fileName);
    end

    if (cnet == 'y' || cnet == 'Y') && (cind == 'y' || cind == 'Y') && choice == 2;
        fprintf(fid, '.SUBCKT %s bias supply Gnd\n', paName);
        RFC = Lfeed*1e9;
        fprintf(fid, 'LRFC_2 supply N_1 %.2fn\n', RFC);
        fprintf(fid, 'CCapacitor_3 N_1 N_4 %.2fp\n', 1);
        if cmn == 0;
          fprintf(fid, 'XL0_1 N_2 Gnd Gnd L0\n');
          fprintf(fid, 'CCapacitor_1 N_2 Gnd\n');
          if harmonics == 1;
            fprintf(fid, 'XL3_1 N_4 N_2 Gnd L3\n');
            fprintf(fid, 'CCapacitor_2 N_4 N_2 %.2fp\n', floor(1e14 * C3 + 0.5) / 100);
          end
          if harmonics == 2;
            fprintf(fid, 'XL3_1 N_4 N_3 Gnd L3\n');
            fprintf(fid, 'CCapacitor_2 N_4 N_3 %.2fp\n', floor(1e14 * C3 + 0.5) / 100);
            fprintf(fid, 'XL5_1 N_3 N_2 Gnd L5\n');
            fprintf(fid, 'CCapacitor_4 N_3 N_2 %.2fp\n', floor(1e14 * C5 + 0.5) / 100);
          end
          fprintf(fid, 'RResistor_1 N_2 Gnd %.2f TC=0.0, 0.0\n', floor(100 * RL + 0.5)
/ 100);
        else
          fprintf(fid, 'XL0_1 N_M1 Gnd Gnd L0\n');
          fprintf(fid, 'CCapacitor_1 N_M1 Gnd %.2fp\n', floor(1e14 * C0 + 0.5) / 100);
          if harmonics == 1;
            fprintf(fid, 'XL3_1 N_4 N_M1 Gnd L3\n');
            fprintf(fid, 'CCapacitor_2 N_4 N_M1 %.2fp\n', floor(1e14 * C3 + 0.5) /
100);
          end
          if harmonics == 2;
            fprintf(fid, 'XL3_1 N_4 N_3 Gnd L3\n');
            fprintf(fid, 'CCapacitor_2 N_4 N_3 %.2fp\n', floor(1e14 * C3 + 0.5) / 100);
            fprintf(fid, 'XL5_1 N_3 N_M1 Gnd L5\n');
            fprintf(fid, 'CCapacitor_4 N_3 N_M1 %.2fp\n', floor(1e14 * C5 + 0.5) /
100);
          end
          fprintf(fid, 'RResistor_1 N_M2 Gnd %.2f TC=0.0, 0.0\n', 50);
        end
        fprintf(fid, transistor);
        fprintf(fid, '\n');
        matchSpiral; %Export matching inductors
        fprintf(fid, '.ENDS\n');
        fclose(fid);
        fprintf('File %s created successfully.\n\n', fileName);
    end
```

Figure A.16. MATLAB code for the subroutine used for netlist export (continued).

A.10 ENTERING PROCESS PARAMETERS

Figure A.17 and Figure A.18 show the MATLAB code for the subroutine that allows for entering process parameters (entProcParam.m).

```
%Enter process parameters
%Change default process parameters - any process can be used
%Enter default process parameters here
TM3default = 1000;
rhodefault = 2.82e-8;
MAldefault = 1.257e-6;
ToxM2M3default = 1000;
E = 8.85e-12;
EroxM2M3default = 4;
ToxM3Sdefault = 5000;
EroxM3Sdefault = 4;
TSidefault = 1000;
ErSidefault = 11.7;
rhoSidefault = 0.2;

ctech = input('Do you want to change any of the default process parameters (y/n)? ',
's');
if ctech == 'y' || ctech == 'Y'
    fprintf('\nPlease enter the thickness of the top metal (nm) (-1 to skip): \nOld
value: %.0f  -->  ', TM3default);
    TM3 = input('New value: ');
    if (TM3 <= 0)
      TM3 = TM3default * 1e-9;
    else
      TM3 = TM3 * 1e-9;
    end%if
    fprintf('Please enter rho (ohm.m) (-1 to skip): \nOld value: %.2e  -->  ',
rhodefault);
    rho = input('New value: ');
    if (rho <=0)
      rho = rhodefault;
    end%if
    fprintf('Please enter MAl (H/m) (-1 to skip): \nOld value: %.2e -->  ',
MAldefault);
    MAl = input('New value: ');
    if (MAl <= 0)
      MAl = MAldefault;
    end%if
    delta = sqrt(rho / (pi * MAl * f));
    teff = delta*(1-exp(-TM3/delta));
    fprintf('Please enter thickness of the oxide between top two metals (nm) (-1 to
skip): \nOld value: %.0f  -->  ', ToxM2M3default);
    ToxM2M3 = input('New value: ');
    if (ToxM2M3 <= 0)
      ToxM2M3 = ToxM2M3default * 1e-9;
    else
      ToxM2M3 = ToxM2M3 * 1e-9;
    end%if
    fprintf('Please enter Er of the oxide between top two metals (-1 to skip): \nOld
value: %.2f  -->  ', EroxM2M3default);
    EroxM2M3 = input('New value: ');
    if (EroxM2M3 <= 0)
      EroxM2M3 = EroxM2M3default;
    end%if
    EoxM2M3 = E * EroxM2M3;
    fprintf('Please enter thickness of the oxide between the substrate and the top
metal (nm) (-1 to skip): \nOld value: %.0f  -->  ', ToxM3Sdefault);
    ToxM3S = input('New value: ');
    if (ToxM3S <= 0)
      ToxM3S = ToxM3Sdefault * 1e-9;
    else
      ToxM3S = ToxM3S * 1e-9;
```

Figure A.17. MATLAB code for the subroutine used for entering process parameters.

```
    end%if
    fprintf('Please enter Er of the oxide between the substrate and the top metal (-1
to skip): \nOld value: %.2f  -->  ', EroxM3Sdefault);
    EroxM3S = input('New value: ');
    if (EroxM3S <= 0)
      EroxM3S = EroxM3Sdefault;
    end%if
    fprintf('Please enter TSi (um) (-1 to skip): \nOld value: %.0f  -->  ',TSidefault);
    TSi = input('New value: ');
    if (TSi <= 0)
      TSi = TSidefault * 1e-6;
    else
      TSi = TSi*1e-6;
    end%if
    fprintf('Please enter ErSi (-1 to skip): \nOld value: %.2f  -->  ', ErSidefault);
    ErSi = input('New value: ');
    if (ErSi <= 0)
      ErSi = ErSidefault;
    end%if
    %Rsi
    fprintf('Please enter rhoSi (ohm.m) (-1 to skip): \nOld value: %.2f  -->  ',
rhoSidefault);
    rhoSi = input('New value: ');
    if (rhoSi <= 0)
      rhoSi = rhoSidefault;
    end%if
else
    %If the parameters are not changed, use default parameters
    TM3 = TM3default * 1e-9;
    ToxM3S = ToxM3Sdefault * 1e-9;
    rho = rhodefault;
    MAl = MAldefault;
    delta = sqrt(rho / (pi * MAl * f));
    teff = delta*(1-exp(-TM3/delta));
    ToxM2M3 = ToxM2M3default * 1e-9;
    EroxM2M3 = EroxM2M3default;
    EoxM2M3 = E * EroxM2M3;
    EroxM3S = EroxM3Sdefault;
    TSi = TSidefault * 1e-6;
    ErSi = ErSidefault;
    rhoSi = rhoSidefault;
end%if
fprintf('\n');
```

Figure A.18. MATLAB code for the subroutine used for entering process parameters (continued).

A.11 INDUCTANCE SEARCH ALGORITHM

Figure A.19 and Figure A.20 show the MATLAB code for the inductance search algorithm (indSearch.m).

```
%This procedure searches for the inductance geometry with the highest
%quality factor given the inductance
%Initialize all storage variables to zero
  Qstored = 0;
  fostored = 0;
  Lcstored =0;
  Rsstored = 0;
  RSistored = 0;
  CSistored = 0;
  Coxstored = 0;
  Csstored = 0;
  wstored = 0;
  sstored = 0;
  dinstored = 0;
  doutstored = 0;
  nstored = 0;
  fprintf('\nLooking for the geometry with highest quality factor Q...\n\n');
  %Initialize geometry parameters to default minimum/maximum values
  Lc = 0;
  dout = 0;
  s = smin;
  din = dinmin;
  w = wmin;
  n = 2;
  %Inductance search algorithm
  while (din < 2*doutmax/3)
      s = smin;
          w = wmin;
          while (w <= doutmax/10)
              n = 2;
              dout = 0;
              while (dout < doutmax)
                  dout = din + 2*n*w + 2*(n-1)*s;
                  if (dout > doutmax)
                    break
                  end%if
                  davg = (din + dout) / 2;
                  Lc = b * dout^a1 * w^a2 * davg^a3 * n^a4 * s^a5;
                  calcParasitics; %Procedure to calculate parasitics
                  Lcc = Lc/1e9;
                  Lzz = Lz*1e9;
                  if (Lzz > Ls)
                      if (Lzz < (1 + tolerance) * Ls)
                          %Calculate Q-factor
                          Rp = 1/(omega^2*Cox^2*RSi) + RSi*(Cox + CSi)^2/Cox^2;
                          Cp = Cox*(1 + omega^2*(Cox + CSi)*CSi*RSi^2)/(1 +
omega^2*(Cox + CSi)^2*RSi^2);
                          Q = omega*Lcc/Rs*Rp/(Rp + ((omega*Lcc/Rs)^2 + 1)*Rs)*(1 - (Cp
+ Cs)*(omega^2*Lcc + Rs^2/Lcc));
                          fo = 1/(2*pi)*sqrt(1/(Lcc*(Cp + Cs)) - (Rs/Lcc)^2);
                          if (Q > Qstored)
                            Qstored = Q;
                            fostored = fo;
                            Lclfstored = Lc;
                            Lcstored = Lzz;
                            Rsstored = Rs;
                            RSistored = RSi;
                            CSistored = CSi;
                            Coxstored = Cox;
                            Csstored = Cs;
                            wstored = w;
                            sstored = s;
```

Figure A.19. MATLAB code for the inductance search algorithm.

```
                            dinstored = din;
                            doutstored = dout;
                            nstored = n;
                        end%if
                    end%if
                    Lc = 0;
                    n = 1;
                    break
                end%if
                n = n + 1;
            end%while
            w = w + resolution;
        end%while
    %end%while
    din = din + resolution;
  end%while
  %==== OUTPUT PARAMS ====%
  if Qstored < 1
      fprintf('Could not find a geometry for %.2f nH\nlimited to dinmin and doutmax
with Q greater than 1 at %.2f MHz.\n', Ls, f/1e6)
  end%if
  if Qstored >=1
    fprintf('Ls = %.2f nH \n', Lcstored);
    fprintf('Lslf = %.2f nH \n', Lclfstored);
    fprintf('Q = %.2f \n', floor(100 * Qstored + 0.5) / 100);
    fprintf('fo = %.2f GHz\n', floor(fostored/1e7 + 0.5) / 100);
    fprintf('w = %.2f um\n', floor(100*wstored + 0.5) / 100);
    fprintf('s = %.2f um\n', floor(100*sstored + 0.5) / 100);
    fprintf('din = %.2f um\n', floor(100*dinstored + 0.5) / 100);
    fprintf('dout = %.2f um\n', floor(100*doutstored + 0.5) / 100);
    fprintf('n = %d\n', floor(100*nstored + 0.5) / 100);
  end%if
```

Figure A.20. MATLAB code for the inductance search algorithm (continued).

A.12 EXPORT OF THE SPIRAL INDUCTOR SUBCIRCUIT

Figure A.21 shows the MATLAB code for the export of the netlist of the spiral inductor as a part of the complete PA netlist (exportSubckt.m).

```
%Exports the spiral inductor subcircuit
try
   fprintf(fid, '.SUBCKT %s L1 L2 GND\n', inductorName);
    fprintf(fid, 'CS L1 L2 %.2ffF\n', floor(1e17 * Csstored + 0.5) / 100);
    fprintf(fid, 'LS N4 L1 %.2fn\n', floor(100 * Lclfstored + 0.5) / 100);
    fprintf(fid, 'RS N4 L2 %.2f\n', floor(100 * Rsstored + 0.5) / 100);
    fprintf(fid, 'Csi1 N2 GND %.2ffF\n', floor(1e17 * CSistored + 0.5) / 100);
    fprintf(fid, 'Csi2 N3 GND %.2ffF\n', floor(1e17 * CSistored + 0.5) / 100);
    fprintf(fid, 'Cox1 L1 N2 %.2ffF\n', floor(1e17 * Coxstored + 0.5) / 100);
    fprintf(fid, 'Cox2 L2 N3 %.2ffF\n', floor(1e17 * Coxstored + 0.5) / 100);
    fprintf(fid, 'Rsi1 N2 GND %.2f\n', floor(100 * RSistored + 0.5) / 100);
    fprintf(fid, 'Rsi2 N3 GND %.2f\n', floor(100 * RSistored + 0.5) / 100);
    fprintf(fid, '.ENDS\n\n');
catch
    fprintf('MATLAB reports:\n%s\n', lasterr);
    fprintf('Netlist export failed.\n');
end%try
```

Figure A.21. MATLAB code for the export of the spiral inductor subcircuit.

A.13 EXPORT OF THE PART OF NETLIST INVOLVING MATCHING

Figure A.22 shows the MATLAB code for the export of the part of netlist that involves matching when ideal inductors are used (matchIdeal.m). Figure A.23 shows the MATLAB

code for the export of the part of netlist that involves matching when spiral inductors are used (matchSpiral.m).

```
if cmn == 1;
    fprintf(fid, 'LInductor_M Gnd N_M2 %.2fn\n', floor(1e11 * LM + 0.5) / 100);
    fprintf(fid, 'CCapacitor_M N_M1 N_M2 %.2fp\n', floor(1e14 * CM + 0.5) / 100);
elseif cmn == 2;
    fprintf(fid, 'LInductor_M1 N_M1 N_M %.2fn\n', floor(1e12 * LM1 + 0.5) / 1000);
    fprintf(fid, 'LInductor_M2 N_M N_M2 %.2fn\n', floor(1e12 * LM2 + 0.5) / 1000);
    fprintf(fid, 'CCapacitor_M1 Gnd N_M %.2fp\n', floor(1e15 * CM1 + 0.5) / 1000);
elseif cmn == 3
    fprintf(fid, 'CCapacitor_M1 N_M1 N_M %.2fp\n', floor(1e15 * CM2 + 0.5) / 1000);
    fprintf(fid, 'CCapacitor_M2 N_M N_M2 %.2fp\n', floor(1e15 * CM3 + 0.5) / 1000);
    fprintf(fid, 'LInductor_M1 Gnd N_M %.2fn\n', floor(1e12 * LM3 + 0.5) / 1000);
elseif cmn == 4;
    fprintf(fid, 'LInductor_M1 Gnd N_M1 %.2fn\n', floor(1e12 * LM4 + 0.5) / 1000);
    fprintf(fid, 'LInductor_M2 Gnd N_M2 %.2fn\n', floor(1e12 * LM5 + 0.5) / 1000);
    fprintf(fid, 'CCapacitor_M1 N_M2 N_M1 %.2fp\n', floor(1e15 * CM4 + 0.5) / 1000);
elseif cmn == 5;
    fprintf(fid, 'CCapacitor_M1 Gnd N_M1 %.2fp\n', floor(1e15 * CM5 + 0.5) / 1000);
    fprintf(fid, 'CCapacitor_M2 Gnd N_M2 %.2fp\n', floor(1e15 * CM6 + 0.5) / 1000);
    fprintf(fid, 'LInductor_M1 N_M2 N_M1 %.2fn\n', floor(1e12 * LM6 + 0.5) / 1000);
end
```

Figure A.22. MATLAB code for the export of the part of the netlist that involves matching when ideal inductors are used.

```
if cmn == 1;
    fprintf(fid, 'XLM_1 Gnd N_M2 Gnd LM\n');
    fprintf(fid, 'CCapacitor_M N_M1 N_M2 %.2fp\n', floor(1e14 * CM + 0.5) / 100);
elseif cmn == 2;
    fprintf(fid, 'XLM1_1 N_M1 N_M Gnd LM1\n');
    fprintf(fid, 'XLM2_1 N_M N_M2 Gnd LM2\n');
    fprintf(fid, 'CCapacitor_M1 Gnd N_M %.2fp\n', floor(1e15 * CM1 + 0.5) / 1000);
elseif cmn == 3
    fprintf(fid, 'CCapacitor_M1 N_M1 N_M %.2fp\n', floor(1e15 * CM2 + 0.5) / 1000);
    fprintf(fid, 'CCapacitor_M2 N_M N_M2 %.2fp\n', floor(1e15 * CM3 + 0.5) / 1000);
    fprintf(fid, 'XLM3_1 Gnd N_M Gnd LM3\n');
elseif cmn == 4;
    fprintf(fid, 'XLM4_1 Gnd N_M1 Gnd LM4\n');
    fprintf(fid, 'XLM5_1 Gnd N_M2 Gnd LM5\n');
    fprintf(fid, 'CCapacitor_M1 N_M1 N_M2 %.2fp\n', floor(1e15 * CM4 + 0.5) / 1000);
elseif cmn == 5;
    fprintf(fid, 'CCapacitor_M1 Gnd N_M1 %.2fp\n', floor(1e15 * CM5 + 0.5) / 1000);
    fprintf(fid, 'CCapacitor_M2 Gnd N_M2 %.2fp\n', floor(1e15 * CM6 + 0.5) / 1000);
    fprintf(fid, 'XLM6_1 N_M1 N_M2 Gnd LM6\n');
end
```

Figure A.23. MATLAB code for the export of the part of the netlist that involves matching when spiral inductors are used.

A.14 CALCULATING PARASITICS OF ANY DESIGNED SPIRAL INDUCTOR

Figure A.24 shows the MATLAB code for the subroutine that calculates the parasitics of any designed spiral inductor (calcParasitics.m).

```
%This procedure calculates the parasitics of spiral inductors
ell = 4*n*(din+w) + (2*n)*(2*n-1) * (w+s);
Rs = rho * ell / (w * teff);
ws = w / 1e6;
ells = ell / 1e6;
Cs = n * ws * ws * EoxM2M3 / ToxM2M3;
if (ToxM3S <= ws)
   ToxM1Seff = ws * (ws/ToxM3S + 2.42 - 0.44*ToxM3S/ws + (1 - ToxM3S/ws)^6)^(-1);
else
   ToxM1Seff = ws/(2*pi) * log(8*ToxM3S/ws + 4*ws/ToxM3S);
end%if
EoxM1Seff = E *((EroxM3S + 1)/2 + (EroxM3S - 1)/2*(1 + 10*ToxM3S/ws)^(-1/2));
Cox = ells * ws * EoxM1Seff / ToxM1Seff / 2;
TSieffC = ws/(2*pi) * log(8*TSi/ws + 4*ws/TSi);
ESieff = E *((ErSi + 1)/2 + (ErSi - 1)/2*(1 + 10*TSi/ws)^(-1/2));
CSi = ells * ws * ESieff / TSieffC / 2;
sigmaeff = 1/rhoSi * (1/2 + 1/2*(1 + 10*TSi/ws)^(-1/2));
RSi = 2 * TSieffC / (ells * ws * sigmaeff);

%Effective Ls
%Complex number calculations
% i = sqrt(-1)
ZSi = 1/(i*omega*CSi);
Zox = 1/(i*omega*Cox);
Zs = 1/(i*omega*Cs);
Lss = Lc / 1e9;
ZLs = i*omega*Lss;
ZA = Zox + ZSi * RSi / (ZSi + RSi);
ZB = Zs * ( ZLs + Rs) / (Zs + ZLs + Rs);
Z = ZA * ZB / (ZA + ZB);
R = real(Z);
Lz = imag(Z) / omega;
```

Figure A.24. MATLAB code for the subroutine that calculates the parasitics of any designed spiral inductor.

A.15 DESIGN OF SPIRAL INDUCTORS AS A MAIN ROUTINE

Figure A.25 shows the MATLAB code for the routine for Design of Spiral Inductors (indcalc2.m).

```
%This program finds a geometry for given inductance or calculates the inductance for
%given geometry. GDS and CIF file extraction is included as well as netlist
%extraction.
try
    clear all; %Clear all variables from the workspace
    %Define constants
    b = 1.62e-3;
    a1 = -1.21;
    a2 = -0.147;
    a3 = 2.40;
    a4 = 1.78;
    a5 = -0.030;
    fprintf('\nWelcome to Inductor Calculator v2.2 for Matlab. Please follow the
prompts.\n');
    choice = input('\nPlease enter 1 to specify geometry or 2 to specify inductance:
');
    if choice == 1 || choice == 2
      if choice == 2 %If choice is 2, program finds a geometry for given inductance
          Ls = input('Please enter the wanted inductance value (Ls) (nH): '); %Wanted
inductance
          indSetup;
          fprintf('\n');
          f = input('Please enter the operating frequency (MHz): ')*1e6; %Frequency
          omega = (2*pi*f); %Radian frequency
          entProcParam; %Call the procedure for entering process parameters
          indSearch; %Inductance search algorithm
      end%if
      if choice == 1
          indGeom;
      end%if
      %Export the netlist
      cnet = input('\nDo you want to export the netlist of this inductor into a SPC
file (y/n)? ', 's');
      if cnet == 'y' || cnet == 'Y';
        exportNetlist;
      end%if
      %Export the layout
      cwcif = input('\nDo you want to export the layout of this inductor into a CIF or
GDS file (c - CIF, g - GDS, n - none)? ', 's');
      if cwcif == 'c' || cwcif == 'C';
        writecif; %Export layout into a text (CIF) file
      elseif cwcif == 'g' || cwcif == 'G';
        convertGDS; %Export layout into a stream (GDS) file
      end
      fprintf('\n');
    else
      fprintf('Wrong choice. Please run the program again.\n\n');
    end%if
catch
    fprintf('MATLAB returns: \n%s\nError occurred while running the program. Please try
running the program again.\n\n', lasterr);
end%try
```

Figure A.25. MATLAB code for the routine for design of spiral inductors.

A.16 DESIGN OF INDUCTORS WITH KNOWN GEOMETRY

Figure A.26 shows the MATLAB code for the subroutine that allows for design of spiral inductors with known geometry (indGeom.m).

```
%This procedure calculates the inductance and quality factor values for any
%given square inductor geometry
%Input geometry parameters
dout = input('Please enter the dout diameter (dout) (um): ');
din = input('Please enter the din diameter (din) (um): ');
w = input('Please enter the turn width (w) (um): ');
n = input('Please enter the number of turns: ');
ratio = floor(100*(din / dout) + 0.5)/100;
%Perform basic checks
nmin = (dout/2 - din/2 + 1)/(w + 1);
while (nmin < 2) || (n > nmin) || (n < 2)
    if (nmin <2)
        fprintf('Given geometry results in n smaller than 2. Please re-enter the
geometry: \n');
    end%if
    if (n > nmin)
        fprintf('The number of turns (n) is too small for the chosen geometry. Please
re-enter the geometry: \n');
    end%if
    if (n < 2)
        fprintf('Cannot use less than two turns. Please choose n as 2 or greater.
Please re-enter the geometry: \n');
    end%if
    dout = input('Please enter the dout diameter (dout) (um): ');
    din = input('Please enter the din diameter (din) (um): ');
    w = input('Please enter the turn width (w) (um): ');
    n = input('Please enter the number of turns: ');
    ratio = floor(100*(din / dout) + 0.5)/100;
    nmin = (dout/2 - din/2 + 1)/(w + 1);
end%while
%Enter operating frequency
f = input('Please enter the operating frequency (MHz): ')*1e6;
omega = (2*pi*f); %Radian frequency
s = (dout / 2 - din / 2 - n * w) / (n - 1); %Pitch between the turns of the spiral
davg = (din + dout) / 2; %Average diameter
Lc = b * dout^a1 * w^a2 * davg^a3 * n^a4 * s^a5; %Inductance
entProcParam; %Call the procedure for entering process parameters
calcParasitics; %Call the procedure that calculates parasitics and Q factor
Lcc = Lc/1e9;
Lzz = Lz*1e9;
%Calculate Q-factor
Rp = 1/(omega^2*Cox^2*RSi) + RSi*(Cox + CSi)^2/Cox^2;
Cp = Cox*(1 + omega^2*(Cox + CSi)*CSi*RSi^2)/(1 + omega^2*(Cox + CSi)^2*RSi^2);
Q = omega*Lcc/Rs*Rp/(Rp + ((omega*Lcc/Rs)^2 + 1)*Rs)*(1 - (Cp + Cs)*(omega^2*Lcc +
Rs^2/Lcc));
fo = 1/(2*pi)*sqrt(1/(Lcc*(Cp + Cs)) - (Rs/Lcc)^2);
%Outputs
fprintf('Ls = %.2f nH \n', Lzz);
fprintf('Lslf = %.2f nH \n', Lc);
fprintf('Q = %.2f \n', floor(100 * Q + 0.5) / 100);
fprintf('fo = %.2f GHz\n', floor(fo/1e7 + 0.5) / 100);
fprintf('w = %.2f um\n', floor(100*w + 0.5) / 100);
fprintf('s = %.2f um\n', floor(100*s + 0.5) / 100);
fprintf('din = %.2f um\n', floor(100*din + 0.5) / 100);
fprintf('dout = %.2f um\n', floor(100*dout + 0.5) / 100);
fprintf('n = %d\n', floor(100*n + 0.5) / 100);
%Store the parasitic parameters for netlist extraction
Lcstored = Lzz;
Lclfstored = Lc;
Rsstored = Rs;
RSistored = RSi;
CSistored = CSi;
Coxstored = Cox;
Csstored = Cs;
nstored = n;
doutstored = dout;
wstored = w;
sstored = s;
```

Figure A.26. MATLAB code subroutine for design of spiral inductors with known geometry.

A.17 EXPORT OF THE STAND-ALONE NETLIST OF A SPIRAL INDUCTOR

Figure A.27 shows the MATLAB code for the subroutine that exports the stand-alone netlist of a designed spiral inductor (exportNetlist.m).

```
%This procedure exports the netlist of a spiral inductor
try
    inductorName = input('Please enter the inductor name (press "s" to skip): ', 's');
    if inductorName(1) == 's' || inductorName(1) == 'S';
        inductorName = 'MyInductor';
    end%if
    fileName = strcat(inductorName, '_net.spc');
    fid = fopen(fileName, 'w')    ;
    fprintf(fid, '*SUBCKT gen. by Inductor Calculator v2.2\n');
    fprintf(fid, '.SUBCKT %s L1 L2 GND\n', inductorName);
    fprintf(fid, 'CS L1 L2 %.2ffF\n', floor(1e17 * Csstored + 0.5) / 100);
    fprintf(fid, 'LS N4 L1 %.2fn\n', floor(100 * Lclfstored + 0.5) / 100);
    fprintf(fid, 'RS N4 L2 %.2f\n', floor(100 * Rsstored + 0.5) / 100);
    fprintf(fid, 'Csi1 N2 GND %.2ffF\n', floor(1e17 * CSistored + 0.5) / 100);
    fprintf(fid, 'Csi2 N3 GND %.2ffF\n', floor(1e17 * CSistored + 0.5) / 100);
    fprintf(fid, 'Cox1 L1 N2 %.2ffF\n', floor(1e17 * Coxstored + 0.5) / 100);
    fprintf(fid, 'Cox2 L2 N3 %.2ffF\n', floor(1e17 * Coxstored + 0.5) / 100);
    fprintf(fid, 'Rsi1 N2 GND %.2f\n', floor(100 * RSistored + 0.5) / 100);
    fprintf(fid, 'Rsi2 N3 GND %.2f\n', floor(100 * RSistored + 0.5) / 100);
    fprintf(fid, '.ENDS\n\n');
    fclose(fid);
    fprintf('File %s created successfully.\n', fileName);
catch
    fprintf('MATLAB reports:\n%s\n', lasterr);
    fprintf('Netlist export failed.\n');
end%try
```

Figure A.27. MATLAB code for the subroutine that exports the stand-alone netlist of a spiral inductor.

A.18 EXTRACTION OF INDUCTOR LAYOUT INTO A CIF FILE

Figure A.28 though Figure A.30 show the MATLAB code for the subroutine for extraction of the layout of a designed inductor into a CIF file (writecif.m).

```
%This procedure exports the layout of an inductor into a text based (CIF)
%file
try
    ccif = input('Do you want to change any CIF paramaters (y/n)? ', 's');
    if ccif == 'y' || ccif == 'Y'
        %Change default CIF parameters
        scaling = input('Please enter CIF scaling factor (-1 to skip): ');
        if scaling <= 0;
            scaling = 2000;
        end%if
        viaSpacing = input('Please enter via spacing (-1 to skip): ');
        if viaSpacing <= 0;
            viaSpacing = 1;
        end%if
        viaWidth = input('Please enter via width (-1 to skip): ');
        if viaWidth <= 0;
            viaWidth = 0.5;
```

Figure A.28. MATLAB code for the subroutine for inductor extraction into a CIF file.

```
        end%if
    else
       %Default CIF parameters
        scaling = 2000;
        viaSpacing = 1;
        viaWidth = 0.5;
    end%if
    %Calculate usable parameters
    dout2 = round(doutstored*scaling);
    zero = 0;
    w2 = round(wstored * scaling);
    s2 = round(sstored * scaling);
    n = nstored;
    spacing = viaSpacing * scaling;
    width = viaWidth * scaling;
    %Specify the inductor name and open the file
    cellName = input('Please enter the cell (inductor) name (press "s" to skip): ',
's');
    if cellName(1) == 's' || cellName(1) == 'S';
        cellName = 'mycell';
    end%if
    fileName = strcat(cellName, '_lay.cif');
    fid = fopen (fileName, 'w');
    %Print into the file
    %PRINT THE HEADER
    fprintf(fid,'(CIF written by the Inductance Calculator MATLAB version);\n');
    fprintf(fid,'(Version: 2.10);\n');
    fprintf(fid,'(DATE: %s);\n',date);
    fprintf(fid,'(FABCELL: %s  %d x %d Microns);\n',cellName, dout, dout);
    fprintf(fid,'(L-Edit Layer NTUB = CIF Layer NTUB);\n');
    fprintf(fid,'(L-Edit Layer DIFF = CIF Layer DIFF);\n');
    fprintf(fid,'(L-Edit Layer PPLUS = CIF Layer PPLUS);\n');
    fprintf(fid,'(L-Edit Layer CONT = CIF Layer CONT);\n');
    fprintf(fid,'(L-Edit Layer MET1 = CIF Layer MET1);\n');
    fprintf(fid,'(L-Edit Layer MET2 = CIF Layer MET2);\n');
    fprintf(fid,'(L-Edit Layer VIA2 = CIF Layer VIA2);\n');
    fprintf(fid,'(L-Edit Layer MET3 = CIF Layer MET3);\n');
    fprintf(fid,'(L-Edit Layer VIA3 = CIF Layer VIA3);\n');
    fprintf(fid,'(L-Edit Layer MET4 = CIF Layer MET4);\n');
    fprintf(fid,'(L-Edit Layer FIMP = CIF Layer FIMP);\n');
    fprintf(fid,'(L-Edit Layer TEXT = CIF Layer TEXT);\n');
    fprintf(fid,'(L-Edit Layer SFCDEF = CIF Layer SFCDEF);\n');
    fprintf(fid,'(SCALING: 1 CIF Unit = 1/%d Microns);\n',scaling);
    fprintf(fid,'DS 1 2 40;\n');
    fprintf(fid,'9 %s;\n', cellName);
    fprintf(fid,'94 P1 %d,0 TEXT;\n', w2/2);
    fprintf(fid,'94 P2 %d,0 TEXT;\n', dout2 - (n-0.5)*w2 - (n-1)*s2);
    fprintf(fid,'94 %s %d,%d SFCDEF;\n', cellName, dout2/2, dout2/2);

    %PRINT LOWER METAL
    fprintf(fid,'L MET2;\n');
    fprintf(fid,'B %d %d %d,%d;\n',w2, w2*(n + 1) + s2*n, dout2 - n*w2 - (n - 1)*s2 +
w2/2, (w2*(n + 1) + s2*n)/2);

    %PRINT VIAS
    fprintf(fid,'L VIA2;\n');
    x = floor(w2 / (spacing + width));
```

Figure A.29. MATLAB code for the subroutine for inductor extraction into a CIF file (continued).

```
    y = floor((2*w2 + s2) / (spacing + width));
    for i=0:x-1;
        for j=0:y-1;
            fprintf(fid,'B %d %d %d,%d; \n', width, width, dout2 - n*w2 - (n - 1)*s2 +
(spacing + width)*(i + 0.5), (n-1)*w2 + (n-1)*s2 + (spacing + width)*(j + 0.5) );
        end%for
    end%for

    %PRINT HIGHER METAL
    fprintf(fid,'L MET3;\n');
    fprintf(fid,'P ');
    %inner points
    %first turn
    fprintf(fid,'%d,%d\n', w2, zero);
    fprintf(fid,'%d,%d\n', w2, dout2 - w2);
    fprintf(fid,'%d,%d\n', dout2 - w2, dout2 - w2);
    fprintf(fid,'%d,%d\n', dout2 - w2, w2);
    %inner turns
    for turn = 2:n-1;
        fprintf(fid,'%d,%d\n', turn*w2 + (turn-1)*s2, (turn-1)*w2 + (turn-2)*s2);
        fprintf(fid,'%d,%d\n', turn*w2 + (turn-1)*s2, dout2 - (turn-1)*s2 - turn*w2);
        fprintf(fid,'%d,%d\n', dout2 - (turn-1)*s2 - turn*w2, dout2 - (turn-1)*s2 -
turn*w2);
        fprintf(fid,'%d,%d\n', dout2 - (turn-1)*s2 - turn*w2, turn*w2 + (turn-1)*s2);
    end%for
    %last turn
    turn = n;
    fprintf(fid,'%d,%d\n', turn*w2 + (turn-1)*s2, (turn-1)*w2 + (turn-2)*s2);
    fprintf(fid,'%d,%d\n', turn*w2 + (turn-1)*s2, dout2 - (turn-1)*s2 - turn*w2);
    fprintf(fid,'%d,%d\n', dout2 - (turn-1)*s2 - turn*w2, dout2 - (turn-1)*s2 -
turn*w2);
    fprintf(fid,'%d,%d\n', dout2 - (turn-1)*s2 - turn*w2, (turn-1)*w2 + (turn-1)*s2);
    fprintf(fid,'%d,%d\n', dout2 - (turn-1)*s2 - (turn-1)*w2, (turn-1)*w2 + (turn-
1)*s2);
    fprintf(fid,'%d,%d\n', dout2 - (turn-1)*s2 - (turn-1)*w2, dout2 - (turn-1)*w2 -
(turn-1)*s2);
    fprintf(fid,'%d,%d\n', (turn-1)*w2 + (turn-1)*s2, dout2 - (turn-1)*w2 - (turn-
1)*s2);
    fprintf(fid,'%d,%d\n', (turn-1)*w2 + (turn-1)*s2, (turn-2)*w2 + (turn-2)*s2);
    %inner turns
    for turn = n-1:-1:2;
        fprintf(fid,'%d,%d\n', dout2 - (turn-1)*s2 - (turn-1)*w2, (turn-1)*w2 + (turn-
1)*s2);
        fprintf(fid,'%d,%d\n', dout2 - (turn-1)*s2 - (turn-1)*w2, dout2 - (turn-1)*w2 -
(turn-1)*s2);
        fprintf(fid,'%d,%d\n', (turn-1)*s2 + (turn-1)*w2, dout2 - (turn-1)*w2 - (turn-
1)*s2);
        fprintf(fid,'%d,%d\n', (turn-1)*s2 + (turn-1)*w2, (turn-2)*w2 + (turn-2)*s2);
    end%for
    %first turn
    fprintf(fid,'%d,%d\n', dout2, zero);
    fprintf(fid,'%d,%d\n', dout2, dout2);
    fprintf(fid,'%d,%d\n', zero, dout2);
    fprintf(fid,'%d,%d;\n', zero, zero);

    %PRINT FOOTER
    fprintf(fid,'DF;\n');
    fprintf(fid,'C 1;\n');
    fprintf(fid,'E');

    %Close the file
    fclose(fid);
    fprintf('File %s created successfully.\n', fileName');
catch
    fprintf('MATLAB returns:\n%s\n',lasterr);
    fprintf('Could not export to the file.\n');
end%try
```

Figure A.30. MATLAB code for the subroutine for inductor extraction into a CIF file (continued).

A.19 EXTRACTION OF INDUCTOR LAYOUT INTO A GDSII FILE

Extraction of inductor layout into stream (GDSII file) required tedious number format and number-to-string conversions and string manipulation. The routine (convertGDS.m) and its subroutines (str2hex.m, coordinatesSpiral.m, coordinatesUnderpass.m, coordinatesVia.m, coordinatesP1.m, coordinatesP2.m and coordinatesName.m) total to about 500 lines making it impractically long to be included in this appendix. The complete MATLAB code can be purchased from Business Enterprises at the University of Pretoria. For details, please see Appendix C.

A.20 MATCHING AS A MAIN ROUTINE

Figure A.31 shows the MATLAB code for the routine that performs matching between any two real impedances (match.m).

```
%Calculates the match between real source and load given the frequency of
%operation and bandwidth (for narrowband networks)
clear all;

RS = input('Please enter the value for the source resistance RS (ohm): ');
RL = input('Please enter the value for the load resistance RL (ohm): ');
fo = input('Please enter the operating frequency (MHz): ');
BW = input('Please enter the bandwidth (MHz): ');

fo = fo * 1e6;
BW = BW * 1e6;
wo = 2*pi*fo;
QL = fo/BW;

calcMatch;
```

Figure A.31. MATLAB code for the routine that performs matching between any two real impedances.

APPENDIX B PROCESS FILES FOR EM SIMULATIONS

B.1 INTRODUCTION

Appendix B gives the process files required for running the EM simulations of the designed square spiral inductors as stipulated in Section 5.2.

B.2 PROCESS FILE FOR 3M AMS S35 TECHNOLOGY

Figure B.1 shows the process file for 3M variation of the AMS S35 technology. Layer thicknesses are not disclosed to the reader due to the NDA between the author (via University of Pretoria) and AMS.

```
processType CMOS
numLayers 9

layer 0
        name tab
        type ground
        thickness 0.1e-6
        epsr 1
        rho 1.7857e-8
layer 1
        name substrate
        type dielectric
        thickness 725e-6
        epsr 11.7
        rho 0.19
layer 2
        name sio2
        type dielectric
        thickness 1e-6
        epsr 4.0
        rho 1e10
layer 3
        name metal1
        type metal
        thickness 1e-6
        epsr 4
        rho 1e10
        rhom 2.82e-8
layer 4
        name sio2
        type dielectric
        thickness 1e-6
        epsr 4
        rho 1e10
layer 5
        name metal2
        type metal
        thickness 1e-6
        epsr 4
        rho 1e10
        rhom 2.82e-8
layer 6
        name sio2
        type dielectric
        thickness 1e-6
        epsr 4
        rho 1e10
layer 7
        name metal3
        type metal
        thickness 1e-6
        epsr 4
        rho 1e10
        rhom 2.82e-8
layer 8
        name sio2
        type dielectric
        thickness 1e-6
        epsr 4
        rho 1e10
```

Figure B.1. Process file for 3M variation of the AMS S35 technology.

B.3 PROCESS FILE FOR TM AMS S35 TECHNOLOGY

Figure B.2 shows the process file for TM variation of the AMS S35 technology. Layer thicknesses are not disclosed to the reader due to the NDA between the author and AMS.

```
processType CMOS
numLayers 11

layer 0
        name tab
        type ground
        thickness 0.1e-6
        epsr 1
        rho 1.7857e-8
layer 1
        name substrate
        type dielectric
        thickness 725e-6
        epsr 11.7
        rho 0.19
layer 2
        name sio2
        type dielectric
        thickness 1e-6
        epsr 4.0
        rho 1e10
layer 3
        name metal1
        type metal
        thickness 1e-6
        epsr 4
        rho 1e10
        rhom 2.82e-8
layer 4
        name sio2
        type dielectric
        thickness 1e-6
        epsr 4
        rho 1e10
layer 5
        name metal2
        type metal
        thickness 1e-6
        epsr 4
        rho 1e10
        rhom 2.82e-8
layer 6
        name sio2
        type dielectric
        thickness 1e-6
        epsr 4
        rho 1e10
layer 7
        name metal3
        type metal
        thickness 1e-6
        epsr 4
        rho 1e10
        rhom 2.82e-8
layer 8
        name sio2
        type dielectric
        thickness 1e-6
        epsr 4
        rho 1e10
layer 9
        name metal4
        type metal
        thickness 1e-6
        epsr 4
        rho 1e10
        rhom 2.82e-8
layer 10
        name sio2
        type dielectric
        thickness 1e-6
        epsr 3.9
        rho 1e10
```

Figure B.2. Process file for TM variation of the AMS S35 technology.

APPENDIX C DESIGN METHOD – BE AT UP (PTY) LTD

The resulting design method was implemented as a MATLAB script, and extended to the national and international scientific community via Business Enterprises at the University of Pretoria (BE at UP (Pty) ltd). The extension is offered via an online page: http://www.be.up.co.za/pa-inductance-calculator/. A screen capture (accessed: 24 February 2011) of this page can be seen in Figure C.1.

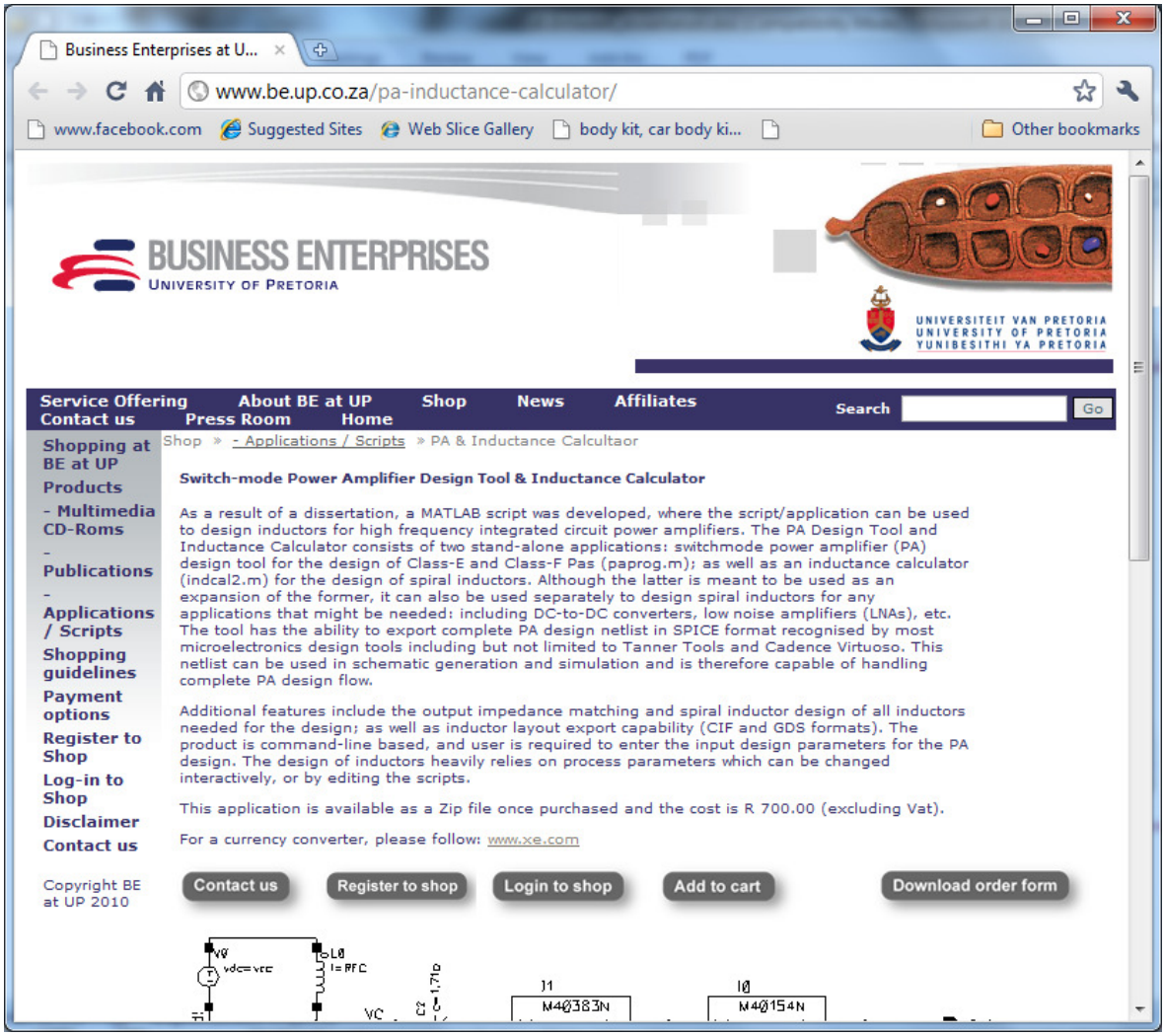

Figure C.1. An offering to the scientific community: Switch-mode Power Amplifier Design Tool & Inductance Calculator.