# CHAPTER 6 LAYOUT, FABRICATION AND MEASUREMENT RESULTS

## 6.1 INTRODUCTION

In Chapter 5, the inductor modelling and spiral inductor search algorithm was verified by means of EM simulations. Furthermore, a full circuit design and simulations in the AMS S35 (0.35 μm BiCMOS) process for the PAs designed with the full system integration routine were presented. In this chapter, several inductors were identified to correspond with the inductors provided and measured by the AMS in order to establish the accuracy of inductor modelling experimentally. Additionally, layouts for the designs described in Sections 5.3.2 and 5.3.4 have been drawn. Due to constraints described in Section 3.3, fabrication in AMS process was not possible, so layouts are drawn in IBM 7WL (180 nm BiCMOS) process. This also offers a proof that the research outputs are technology independent. The IC measurements were performed on a custom designed PCB.

### 6.1.1 Inductor measurements

As a starting point, the square spiral inductor structures given by AMS in [89] have been analyzed and square spiral inductors identified. These included eleven layer-three inductors for the three-metal AMS process (3M) and fourteen thick-layer (TM) inductors for the AMS thick-metal process. The spiral inductor part of the routine, as developed in Chapter 4, was then employed to calculate inductances and Q-factors of the same inductors at the same respective frequencies. Furthermore, EM simulations were performed for completeness.

Comparison of the inductance and Q-factor values predicted by the inductor model and simulated by means of EM simulations against those measured by AMS cannot be given in this version of the thesis due to obligations to the signed NDA. In summary, the measurement results show that inductance values are correctly predicted (within 3.7 %) by the inductor models used for the inductance search algorithm. As far as Q-factors are concerned, situation differs for the 3M and TM inductors, where more accurate predictions are accomplished for the 3M inductors than for the TM (3.9 % vs. 34 %), the phenomenon that has previously been described in Section 5.2.

## 6.2 FULL SYSTEM INTEGRATION MEASUREMENTS

One Class-E PA and one Class-F PA were submitted for fabrication.

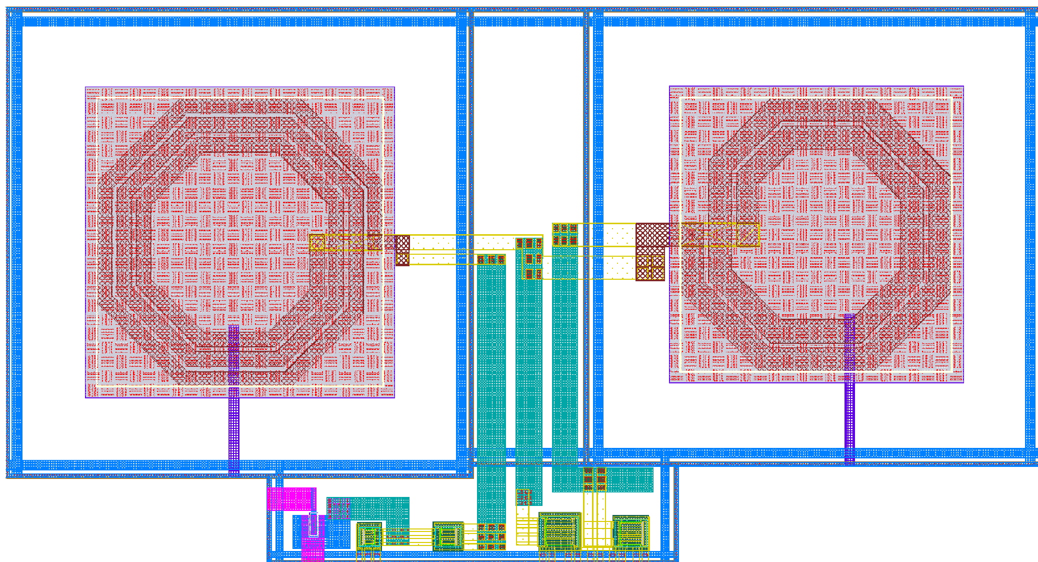
### 6.2.1 Circuit layouts

Due to the process differences, some considerations had to be taken into account in performing the layouts of the circuits described in Sections 5.3.2 and 5.3.4.

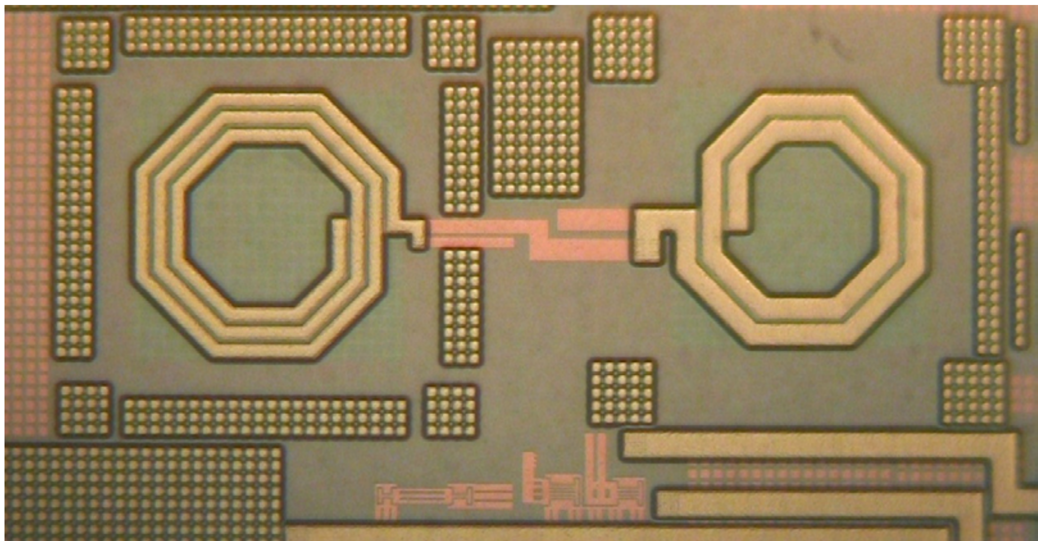
- HBTs in AMS process have larger total emitter area than HBTs in IBM process. This should result in a poorer frequency (*S*-parameter) response of the IBM transistor to the one in the AMS process, and the total output power delivered to the load of the IC will inevitably be lower.

- Inductors available in the IBM process are octagonal spiral inductors. In order to utilize them properly, the spiral inductor design algorithm described in Section 4.5 had to be modified to cater for octagonal geometries. Also, the IBM process offered two types of ground planes: trench isolation TI (TI) and metal 1 (M1). Inductors without a ground plane were not supported by the process therefore TI ground plane was implemented to decrease the spiral-to-substrate capacitance and lower turn-to-turn coupling.

The layouts and photographs of the Class-E and Class-F PAs are shown in Figure 6.1 and Figure 6.2 respectively. The total chip area occupied without the bondpad openings was $1130 \times 600$ $\mu m^2$ for the Class-E configuration and $950 \times 950$ $\mu m^2$ for Class-F configuration. Figure 6.3 shows the Class-E and Class-F PAs within the MPW.

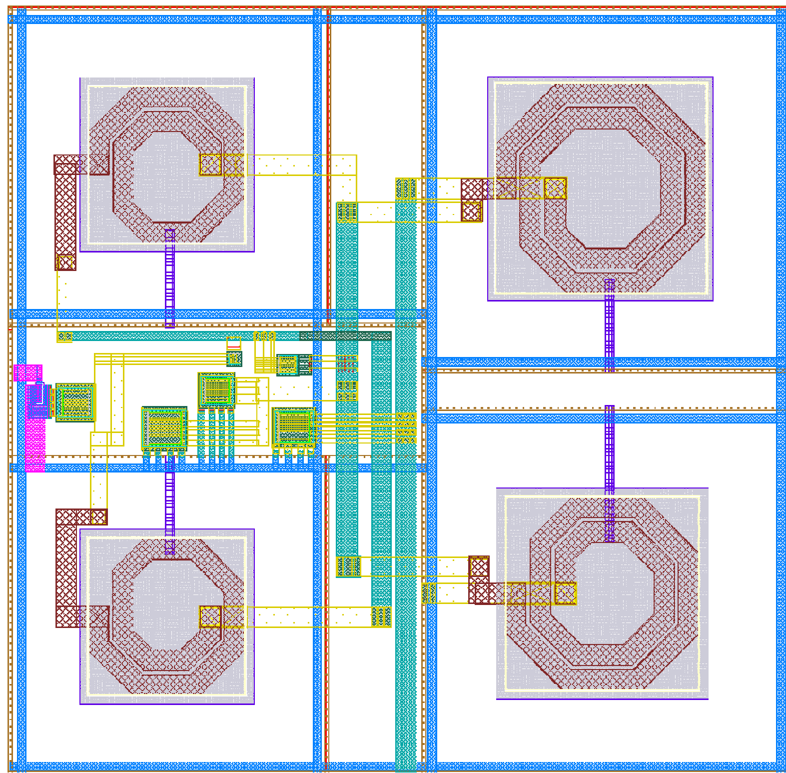


(a)

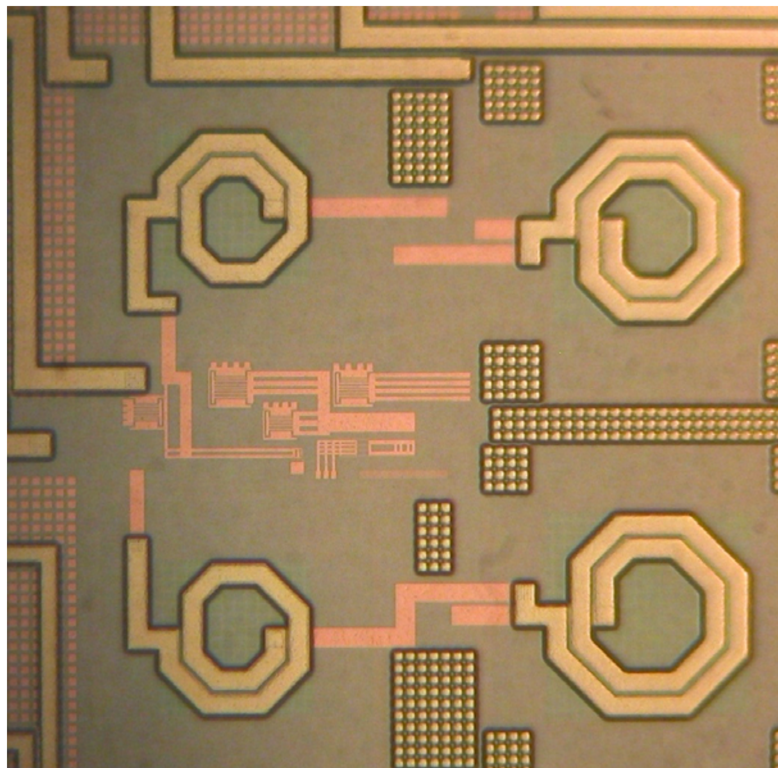


(b)

**Figure 6.1. The (a) layout and (b) photo of the Class-E PA.**

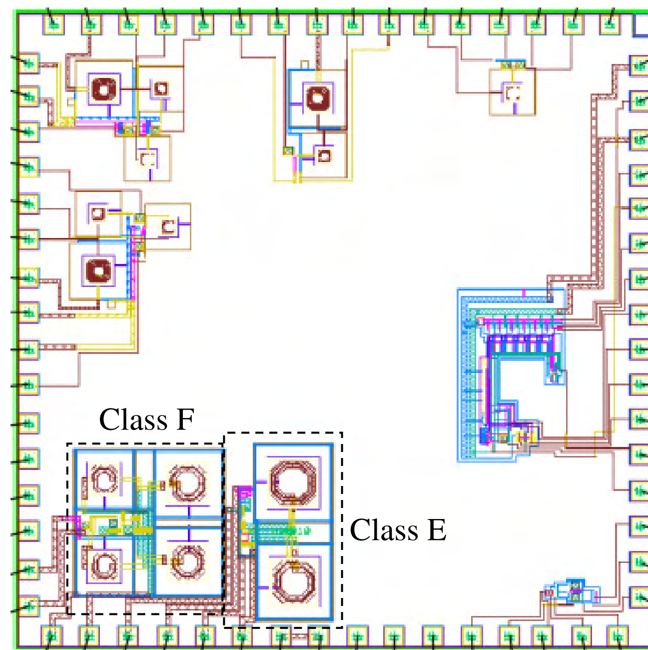


(a)

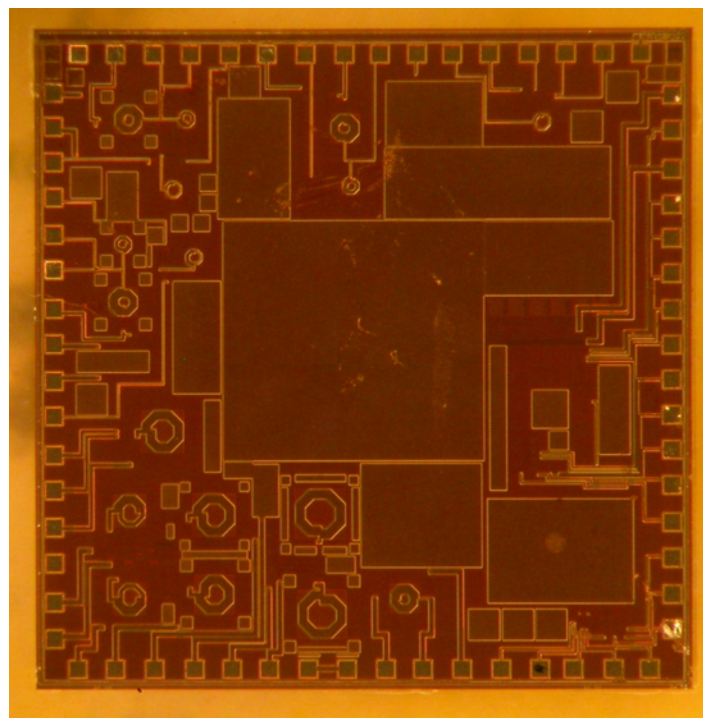


(b)

**Figure 6.2. The (a) layout and (b) photo of the Class-F PA.**




(a)



(b)

**Figure 6.3. Class-E and Class-F PAs within the MPW: (a) layout and (b) photo.**

### 6.2.2 Packaging

The two PA configurations fabricated formed a part of a joint MPW run with two other research projects on the same chip. Therefore, the IC packaging has been chosen by group decision. The dies were packaged using quad flat no-lead (QFN) packages and soldered

onto a PCB for testing purposes. A 64 pin QFN package, shown in Figure 6.4 has been used. The typical bond wire inductance is between 1 and 2 nH.

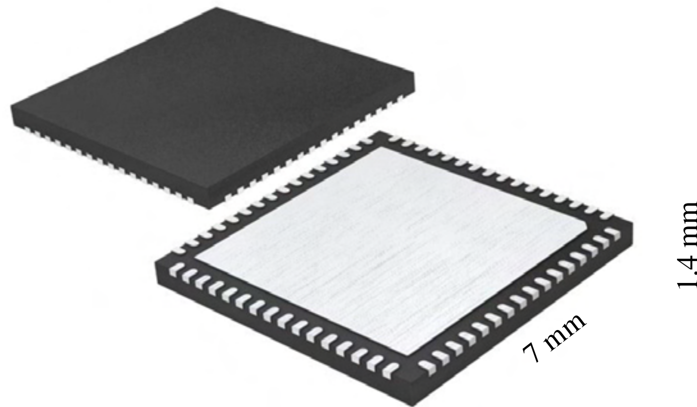



**Figure 6.4. The 64-pin QFN package.**

Figure 6.5 shows a PA (Class-E or Class-F) in relation to bondpad and bondwire capacitances (modelled as 57 pF), bondwire inductances (modelled as 1 nH), RFC inductance (~1.8 nH at 50 mA current [112]) and resistance (30 Ω) and 50 Ω antenna.

### 6.2.3 Package simulations

Two techniques, *S*-parameters and power sweep, were identified as suitable measurement techniques for the fabricated system. Measurements were performed with the aid of the network analyzer described in Section 3.6. Although traditionally switch-mode PAs are analyzed by probing of the transient response waveforms, as done in Chapter 4, this method is impractical for packaged ICs. Power sweep, in addition to *S*-parameter measurements, allows for the investigation of output power capability and presents a good practical alternative to waveform probing. Nonlinear measurement techniques, such as THD, were not deemed paramount in this case due to switch-mode nature of Class-E and Class-F PAs.

The choice of biasing voltage (near-to-class-B) enabled the highest output power, as discussed in Chapter 5. Off-chip input matching was omitted for the simplicity of the measurement setup. Although this approach results in the apparent lower PAE, this was acceptable for measurement purposes.

Figure 6.6 and Figure 6.7 show the simulated output *S*-parameters for the packaged Class-E and Class-F configurations respectively. From these figures, a slight phase shift

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can be seen for the Class-F PA, whilst larger shift is seen in the case of the Class-E PA. These shifts are attributed to packaging parasitics. Power sweeps for frequencies where highest gain occurs for both Class-E and Class-F configurations are shown in Figure 6.8 and Figure 6.9, respectively.

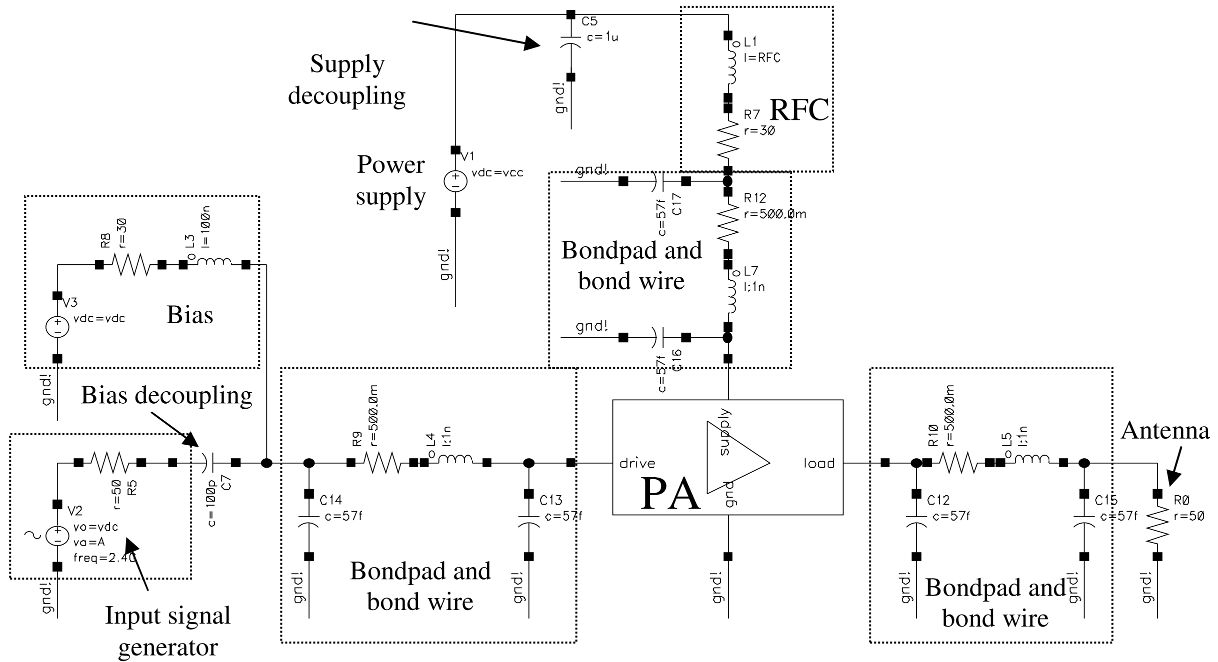


**Figure 6.5. The PA in relation to bondpad and bondwire capacitances, bondwire inductances, RFC inductance and resistance, and the antenna.**

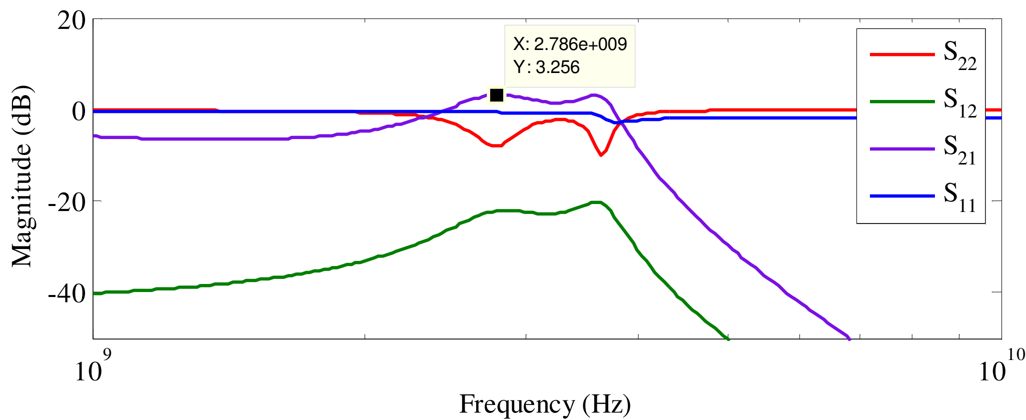


**Figure 6.6. The simulated *S*-parameter response of the fabricated Class-E PA.**

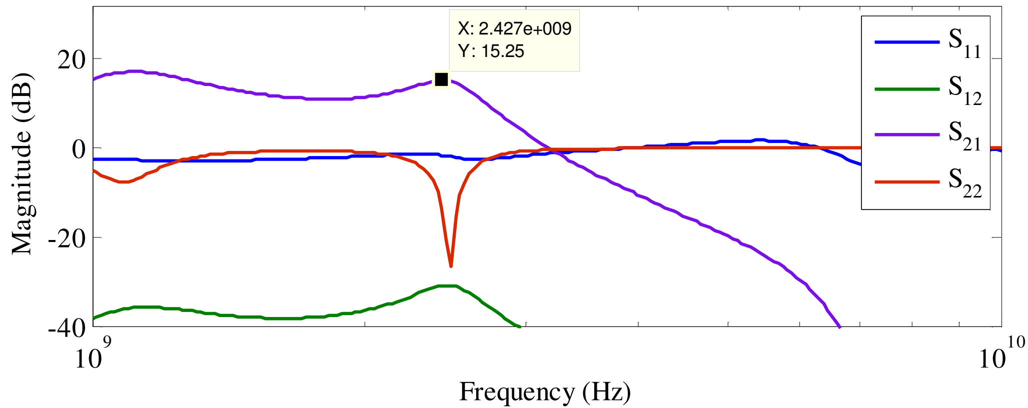


**Figure 6.7. The simulated *S*-parameter response of the fabricated Class-F PA.**

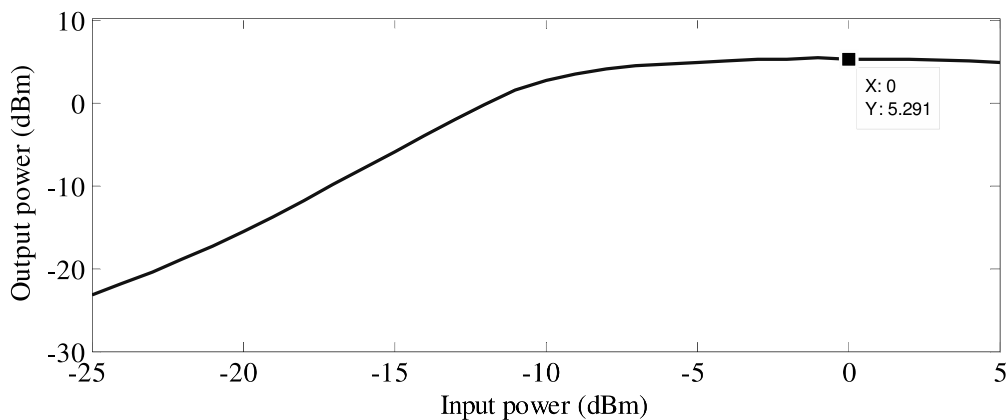


**Figure 6.8. The simulated power sweep response of the fabricated Class-E PA.**

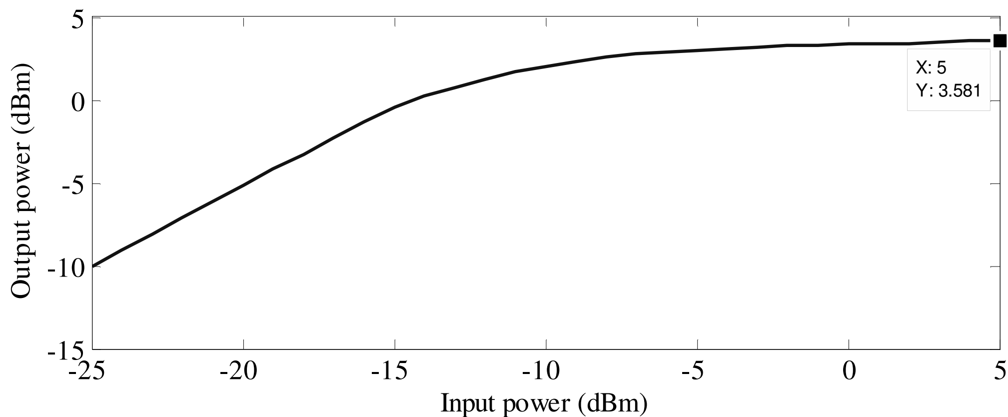


**Figure 6.9. The simulated power sweep response of the fabricated Class-F PA.**

### 6.2.4 The PCB design

A 4 layer RF PCB to be used for testing has been designed by a third party. Due to space constraints, the SubMiniature version A (SMA) connectors [113] had to be placed far away from the IC which brought additional mismatch at the output. The high quality RF chokes

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have been used with the inductance of 1.8 nH at 50 mA current. The photograph of the populated PCB is shown in Figure 6.10.

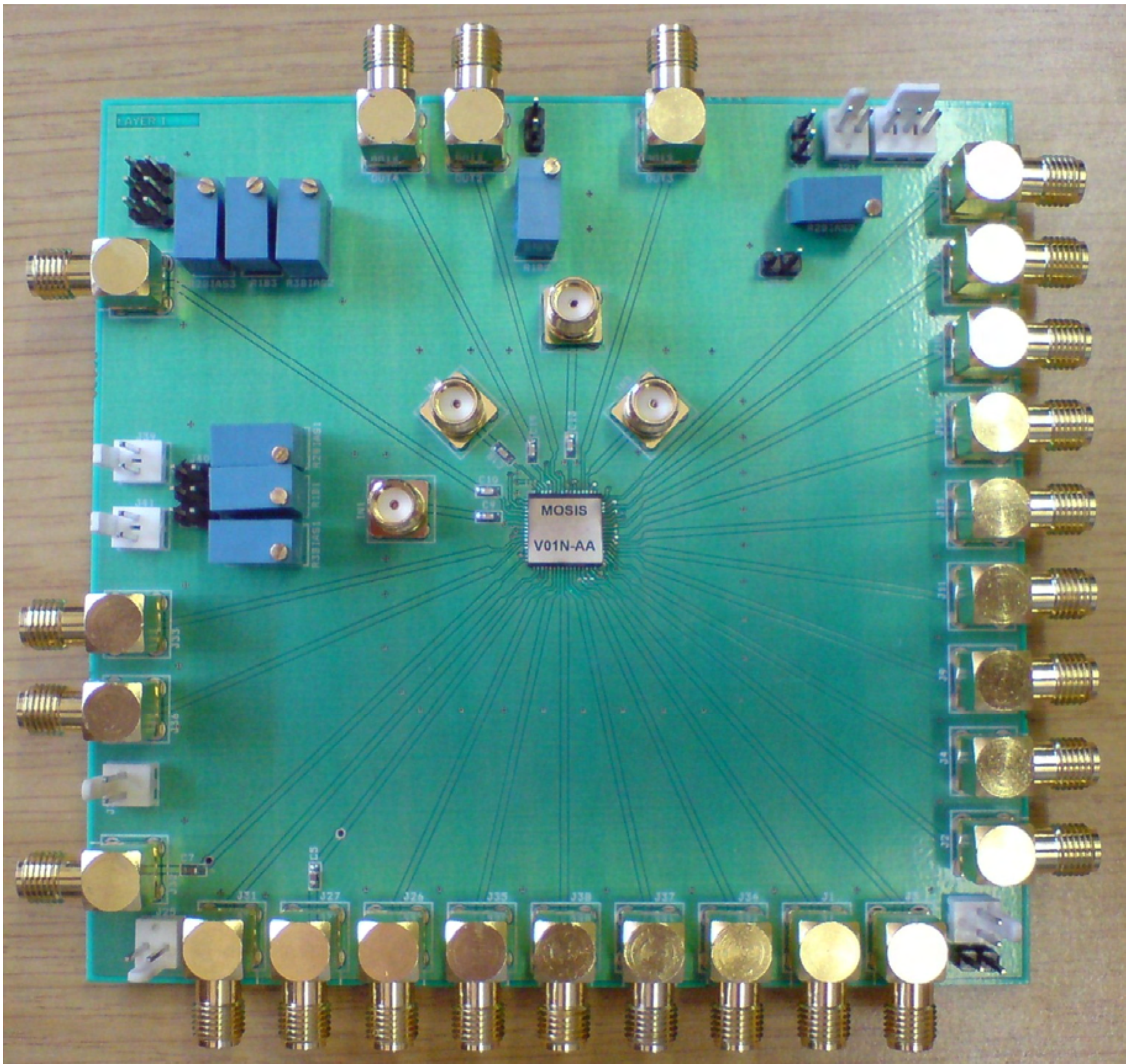


**Figure 6.10. The photograph of the populated PCB.**

### 6.2.5 Measurement results

The measurement setup was designed in such a way as to resemble the simulation setup as close as possible. However, due to mismatches and imperfections of the PCB, track and connector attenuation had to be measured at the frequencies of interest and compensated for when presenting the results. The measured *S*-parameters of Class-E PA are shown in Figure 6.11.

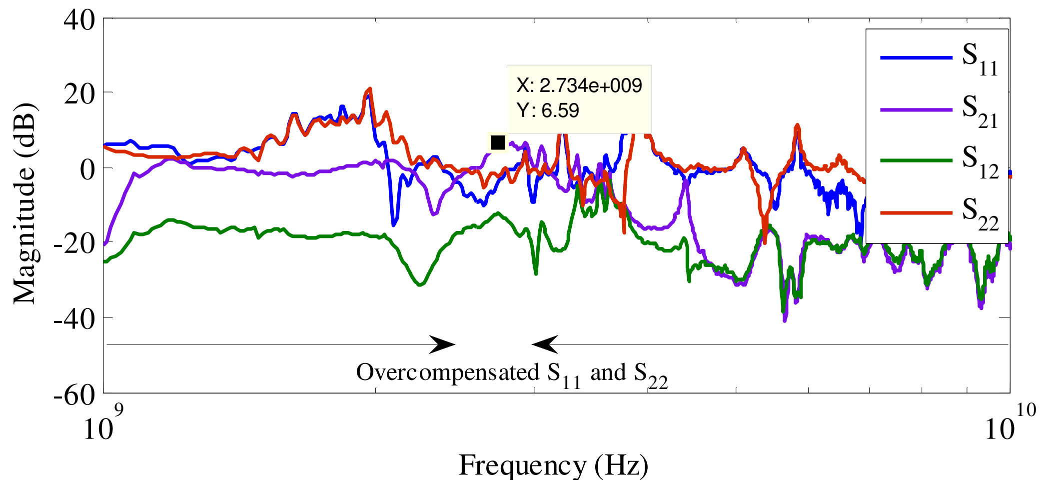


**Figure 6.11. The measured *S*-parameter response of the fabricated Class-E PA.**

Sound correspondence can be seen between *S*-parameters in the Figure 6.6 and Figure 6.11, which shows that the fabricated PA behaves as predicted by simulations that included package modelling. A slightly greater magnitude of the forward gain ($S_{21}$) is seen in the measured results, which is due to the better-than-predicted behaviour of the bond-wires and RFCs. However, some mismatch can be seen at the output ($S_{22}$), likely due to the inductive behaviour of the SMA connectors. Since no input matching has been done, the flat response of $S_{11}$ can be ignored in this analysis. Positive magnitude of $S_{11}$ and $S_{22}$ below and above the frequency of interest is attributed to the overcompensation of the PCB mismatch.

The measured *S*-parameters of Class-F PA are shown in Figure 6.12.

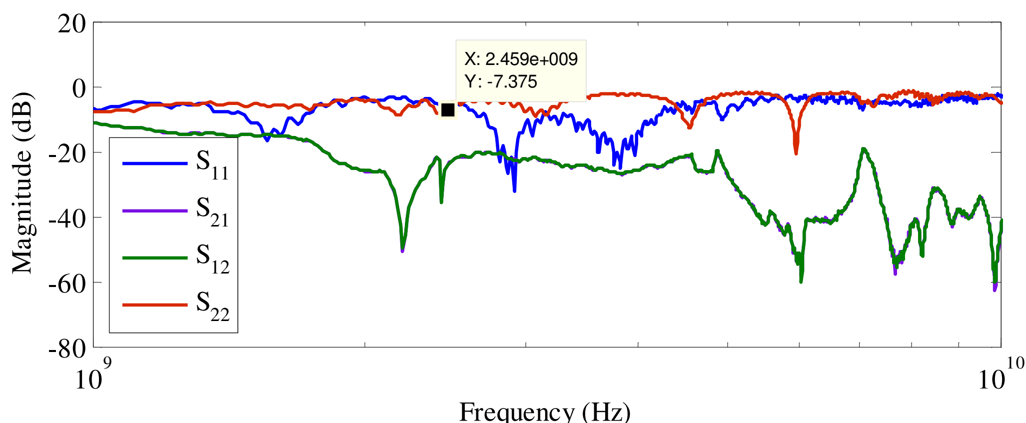


**Figure 6.12. The measured *S*-parameter response of the fabricated Class-F PA.**

From Figure 6.12, it can be seen that $S_{21}$ and $S_{12}$ lie on top of each other. This shows that the Class-F PA is not operational, most likely due to a short circuit or an open circuit on

the inside of the package or on the PCB (since the PA circuit on silicon itself passed LVS and DRC checks). Such an error was not possible to prove or disprove visually or with the available equipment. However, the trace of $S_{22}$ shows a dip to -7.3 dB close to 2.4 GHz, which confirms the presence of the PA's output matching. It was also established that the PA draws several tens of mA from the voltage supply, which pinpoints the problem towards the input or output connection rather than to a problem with the active device.

The measured power sweep for the Class-E system is shown in Figure 6.13. Power sweep was not performed for the Class-F configuration, due to the problems encountered during *S*-parameter measurements.

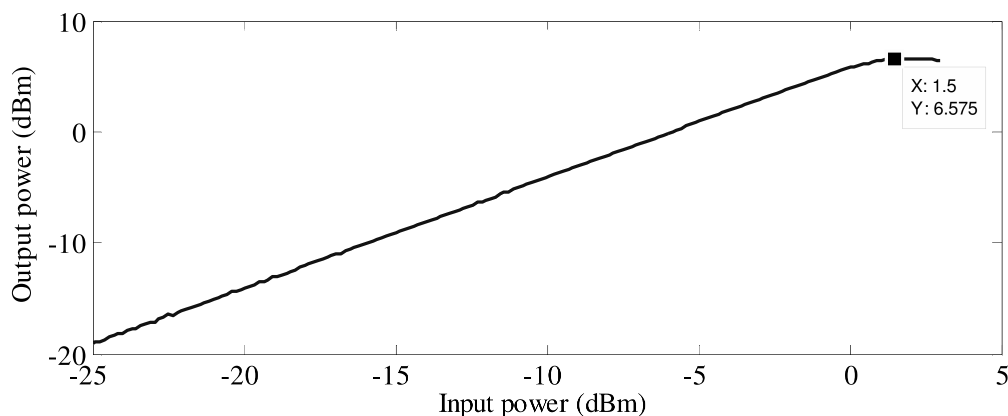


**Figure 6.13. The measured power sweep response of the fabricated Class-E PA.**

Analysis of Figure 6.13 in conjunction with Figure 6.8 shows a rough correspondence between measured and simulated results. Some difference is seen in the gradient of the output-vs.-input power (power gain) curve, which is attributed to biasing and matching conditions differing due to nonlinearities on the PCB. Measured maximum output power differs from simulated maximum output power by only 1.5 dBm, with both simulated and measured powers reaching more than 5 dBm. This difference is attributed to bond-wire and package parasitics, a discrepancy that was also seen in the case of *S*-parameter measurements.

## 6.3 CONCLUSION

This chapter presented experimental means of verifying the core software routines presented in this thesis. The spiral inductor design routine was analyzed by means of measured data provided by the AMS, while in order to characterize the routine for the full system integration, layouts of the PA circuits were submitted for fabrication. Fabrication

was however achieved using a technology node from IBM, due to a fabrication grant to the University, yet also served to confirm the versatility of the algorithms. The packaging and PCB design were also discussed. Measured results have been compared against simulated waveforms in terms of *S*-parameters as well as power sweep.