CHAPTER 5 FULL CIRCUIT DESIGN AND SIMULATION

5.1 INTRODUCTION

In Chapter 4, a system level design routine for the PA design has been developed. In Chapter 5, this routine is used to design spiral inductors and PAs, which are then simulated in order to verify the correctness of the routine. Two distinct topics are dealt with in this chapter. The first one aims to demonstrate the correctness of the spiral inductor model used in the routine and the effectiveness of the inductance search algorithm. The second one shows how the system routine is used in the design of the Class-E and Class-F PA systems supported with resonator design and impedance matching. For inductors, the routine is verified by conducting EM simulations of inductors with inductance and Q-factor values predicted by this routine. For the full PA design, the routine is verified by SPICE and RF SPICE simulations of designed circuits. All circuit-level simulations described in this chapter have been performed in S35 0.35 µm SiGe BiCMOS process from AMS, described in Section 3.3.

5.2 VERIFICATION OF THE SPIRAL INDUCTOR MODEL AND THE INDUCTANCE SEARCH ALGORITHM

As discussed earlier in this thesis, an accurate spiral inductor modelling is paramount for a good PA design. This is why it was important to verify accuracy of the spiral inductor model used in the inductor search algorithm (Section 4.5).

The inductance search algorithm was used to design ten 3M and ten TM inductors fabricated over a standard resistivity substrate at common frequencies of 1, 2, 2.4 and 5 GHz. The smallest inductor value designed for was 0.5 nH, followed by nine inductors in increments of 0.5 nH. Table 5.1 and Table 5.2 show geometric parameters, LF inductance values and the Q-factor of each designed 3M and TM inductor respectively. To verify the predicted values, EM simulation on the designed inductors was performed by means of the EM simulator described in Section 3.5.3. Process files needed for EM simulations for both 3M and TM inductors are given in Figures B.1 and B.2 in Appendix B. The inductance and Q-factor values resulting from EM simulations are also shown in Table 5.1 and Table 5.2.

The comparisons of inductances and Q-factors of all forty inductors designed in this manner are shown graphically in Figures 5.4 through 5.19. This set of figures shows a very good correspondence between two ways of obtaining data in case of inductance values. This shows that inductance values obtained using the inductor model in the inductor design part of the PA design routine accurately predicts actual inductance values.

Good correspondence between the two in terms of Q-factor values exists for 3M inductors, whereas in the case of TM inductors, the graphs of calculated and EM simulated values take similar shape, with simulated Q-factors being larger than those of the calculated Q-factors. This discrepancy can be explained: as the impedance of parasitic elements in the RL model of the spiral (with oxide and substrate effects ignored) approaches that of inductive reactance near the peak frequency, the model yields a pessimistic estimate of the actual Q-factor of the spiral [101]. 3M inductors lie closer to the substrate and have larger resistances than TM inductors, so this effect is less prominent. The fact that the Q-factor is underestimated rather than overestimated can be used to an advantage, since the TM inductors designed by the inductor calculator will perform better than predicted, which will be acceptable in many cases.

Table 5.1. Metal-3 inductors designed with inductance search algorithm.

Frequency (GHz)	Nominal inductance (nH)	Calculated LF inductance (nH)	Calculated Q	EM inductance (nH)	EM Q	d_{out} (μm)	d_{in} (μm)	w (μm)	s (μm)	n
1	0.5	0.50	3.37	0.50	3.00	220	30	47	1	2
1	1	1.00	4.63	0.94	4.15	291	93	49	1	2
1	1.5	1.48	5.22	1.40	4.75	347	149	49	1	2
1	2	1.95	5.47	1.90	5.11	397	199	49	1	2
1	2.5	2.39	5.50	2.33	2.33	441	243	49	1	2
1	3	2.83	5.39	2.75	5.27	483	285	49	1	2
1	3.5	3.29	5.10	3.22	3.22	500	326	43	1	2
1	4	3.67	4.80	3.52	4.52	426	164	43	1	3
1	4.5	4.12	4.66	3.97	4.56	427	189	39	1	3
1	5	4.55	4.60	4.52	4.41	431	211	36	1	3
2	0.5	0.49	5.79	0.45	4.29	210	32	55	1	2
2	1	0.97	7.16	0.91	5.92	288	90	49	1	2
2	1.5	1.41	6.89	1.32	6.11	339	141	49	1	2
2	2	1.86	6.24	1.73	6.23	349	191	39	1	2
2	2.5	2.32	5.64	2.26	5.68	363	233	32	1	2
2	3	2.76	5.12	2.72	5.27	384	270	28	1	2
2	3.5	3.21	4.81	3.01	5.33	276	152	20	1	3
2	4	3.65	4.53	3.45	5.19	283	171	18	1	3
2	4.5	4.06	4.27	3.86	4.98	294	188	17	1	3
2	5	4.51	4.05	4.35	4.76	241	123	14	1	4
2.4	0.5	0.49	6.72	0.45	4.94	216	30	46	1	2
2.4	1	0.95	7.63	0.90	6.38	286	88	49	1	2
2.4	1.5	1.39	6.95	1.34	6.34	316	142	43	1	2
2.4	2	1.86	6.18	1.82	6.25	320	190	32	1	2
2.4	2.5	2.30	5.51	2.26	5.47	339	229	27	1	2
2.4	3	2.76	5.04	2.71	5.32	249	131	19	1	3
2.4	3.5	3.17	4.69	3.12	4.89	262	150	18	1	3
2.4	4	3.61	4.39	3.59	4.74	262	168	15	1	3
2.4	4.5	4.03	4.12	4.03	4.60	220	110	13	1	4
2.4	5	4.47	3.91	4.50	4.55	216	122	11	1	4
5	0.5	0.47	9.48	0.41	6.05	200	30	42	1	2
5	1	0.92	8.22	0.88	6.93	209	95	28	1	2
5	1.5	1.36	6.76	1.34	5.88	222	140	20	1	2
5	2	1.81	5.71	1.80	5.48	169	87	13	1	3
5	2.5	2.22	5.03	2.20	5.15	176	106	11	1	3
5	3	2.60	4.46	2.59	4.45	186	122	10	1	3
5	3.5	2.97	4.02	2.96	4.03	160	82	9	1	4
5	4	3.46	3.70	3.52	4.43	148	94	6	1	4
5	4.5	3.98	3.43	4.07	4.30	141	103	4	1	4
5	5	4.29	3.27	4.42	4.24	106	38	4	1	7

Table 5.2. Thick-metal inductors designed with inductance search algorithm.

Frequency (GHz)	Nominal inductance (nH)	Calculated LF inductance (nH)	Calculated Q	EM inductance (nH)	EM Q	d_{out} (μm)	d_{in} (μm)	w (μm)	s (μm)	n
1	0.5	0.50	7.43	0.38	4.71	216	30	48	2	2
1	1	0.99	10.1	0.93	8.13	299	95	50	2	2
1	1.5	1.47	11.1	1.39	9.96	355	151	50	2	2
1	2	1.95	11.5	1.84	11.1	406	202	50	2	2
1	2.5	2.39	11.4	2.30	11.7	451	247	50	2	2
1	3	2.81	10.9	2.70	12.0	493	289	50	2	2
1	3.5	3.29	10.3	3.20	11.6	499	331	41	2	2
1	4	3.71	9.78	3.49	9.62	403	173	37	2	3
1	4.5	4.17	9.49	3.95	9.89	409	197	34	2	3
1	5	4.60	9.21	4.40	9.99	418	218	32	2	3
2	0.5	0.49	11.4	0.43	9.17	222	30	47	2	2
2	1	0.96	13.0	0.88	13.4	295	91	50	2	2
2	1.5	1.42	11.9	1.35	14.6	316	148	41	2	2
2	2	1.88	10.8	1.82	14.2	324	196	31	2	2
2	2.5	2.33	9.80	2.27	13.8	348	236	37	2	2
2	3	2.79	9.08	2.66	11.6	268	134	21	2	3
2	3.5	3.21	8.55	3.10	11.6	276	154	19	2	3
2	4	3.64	8.05	3.54	11.6	283	173	17	2	3
2	4.5	4.09	7.59	3.96	11.4	294	190	16	2	3
2	5	4.49	7.25	4.39	10.3	240	124	13	2	4
2.4	0.5	0.49	12.4	0.43	10.7	219	31	46	2	2
2.4	1	0.94	13.0	0.86	14.4	286	90	48	2	2
2.4	1.5	1.41	11.6	1.36	15.3	289	149	34	2	2
2.4	2	1.88	10.3	1.83	14.7	302	194	26	2	2
2.4	2.5	2.34	9.25	2.24	11.8	229	113	18	2	3
2.4	3	2.78	8.61	2.69	12.0	238	134	16	2	3
2.4	3.5	3.18	8.01	3.08	12.0	256	152	16	2	3
2.4	4	3.63	7.47	3.56	11.7	256	170	13	2	3
2.4	4.5	4.54	7.04	4.00	10.6	213	113	11	2	4
2.4	5	4.46	6.67	4.36	10.6	223	123	11	2	4
5	0.5	0.47	14.4	0.41	17.3	200	32	41	2	2
5	1	0.93	12.1	0.89	18.9	199	99	24	2	2
5	1.5	1.38	9.83	1.35	17.0	215	143	17	2	2
5	2	1.82	9.37	1.74	14.0	163	89	11	2	3
5	2.5	2.26	7.31	2.18	13.5	170	108	9	2	3
5	3	2.70	6.74	2.62	10.6	123	47	6	2	5
5	3.5	3.09	6.23	3.04	12.0	182	138	6	2	3
5	4	3.42	5.88	3.32	10.4	137	61	6	2	5
5	4.5	3.79	5.44	3.70	10.8	163	103	6	2	4
5	5	4.07	5.02	3.98	9.65	149	73	6	2	5

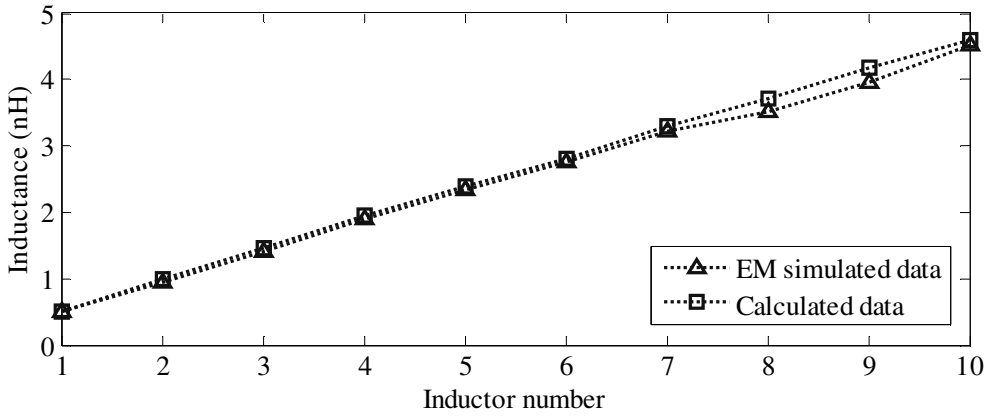


Figure 5.1. Inductance of 1 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

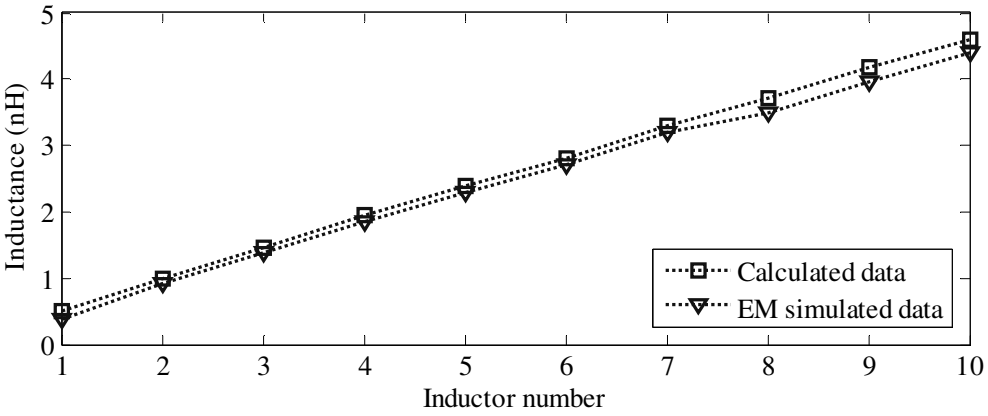


Figure 5.2. Inductance of 1 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

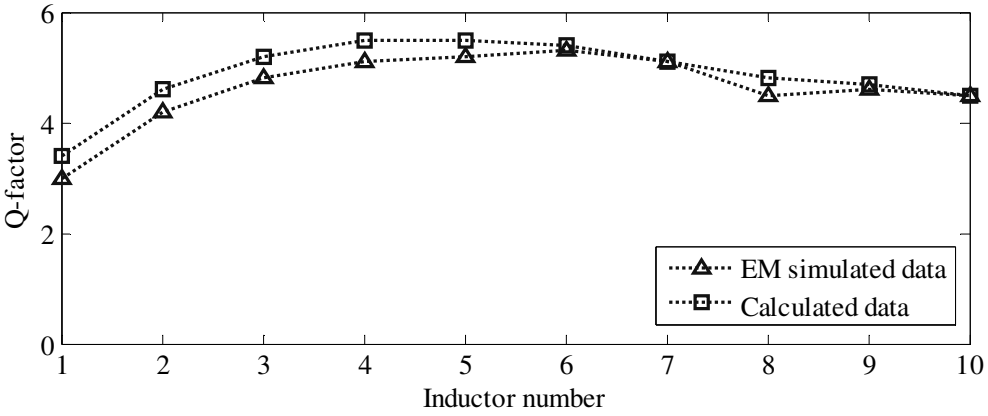


Figure 5.3. Q-factor of 1 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

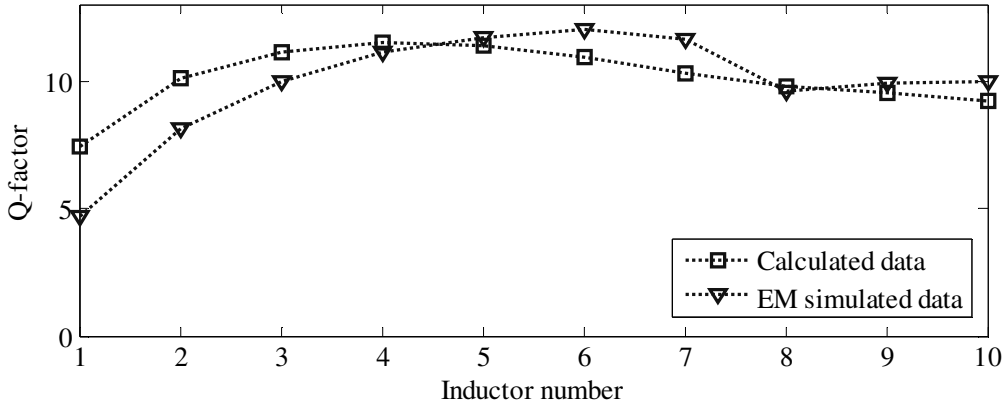


Figure 5.4. Q-factor of 1 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

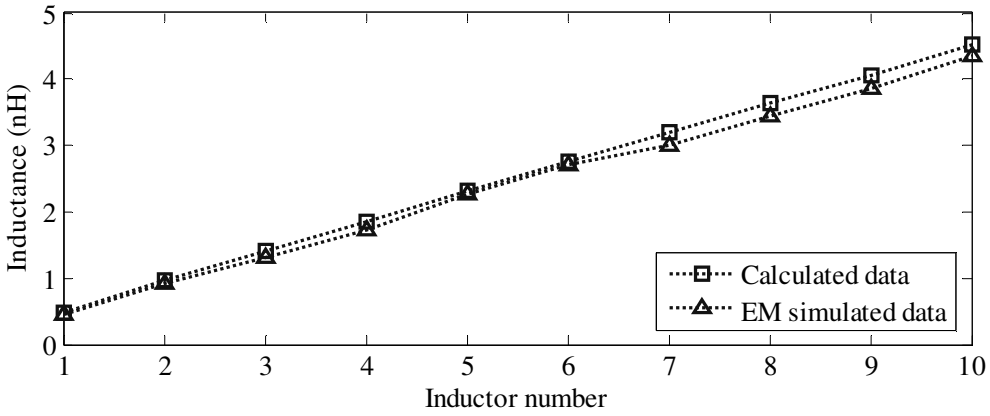


Figure 5.5. Inductance of 2 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

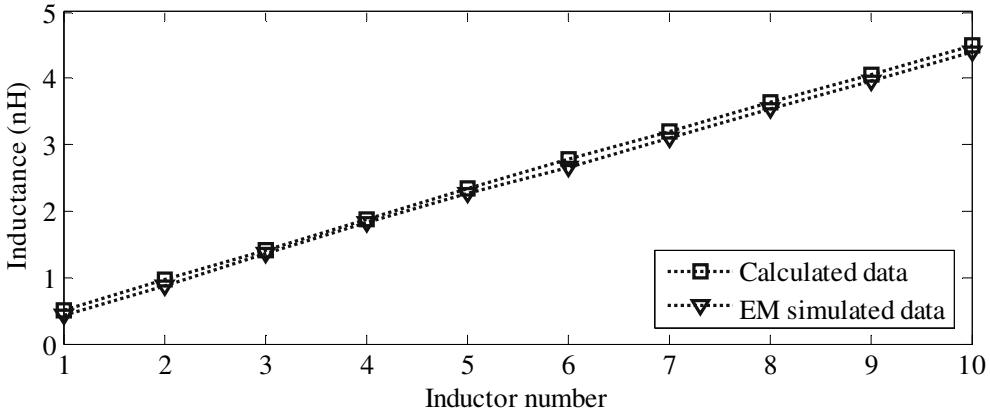


Figure 5.6. Inductance of 2 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

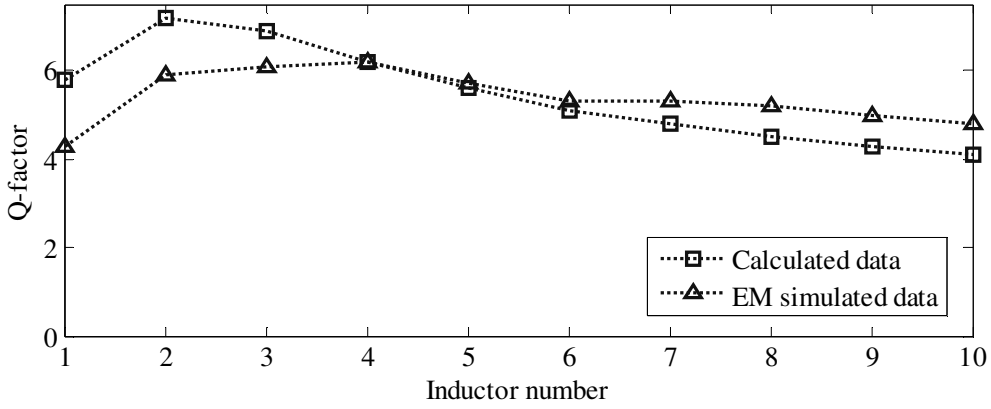


Figure 5.7. Q-factor of 2 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

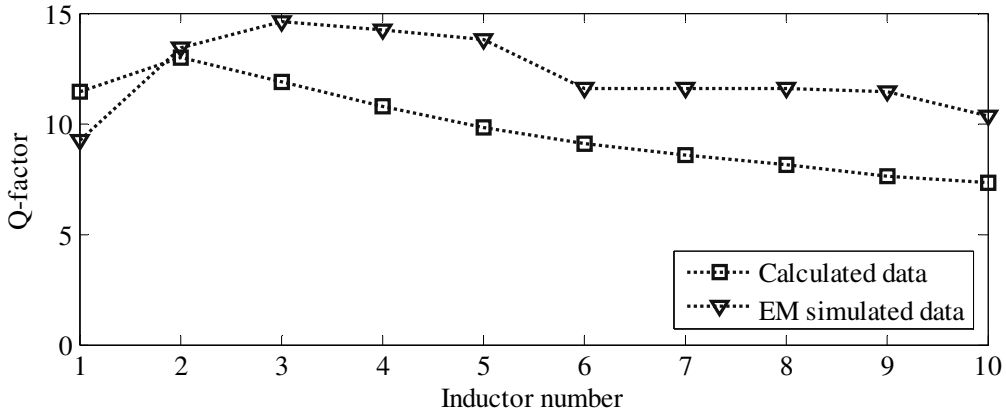


Figure 5.8. Q-factor of 2 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

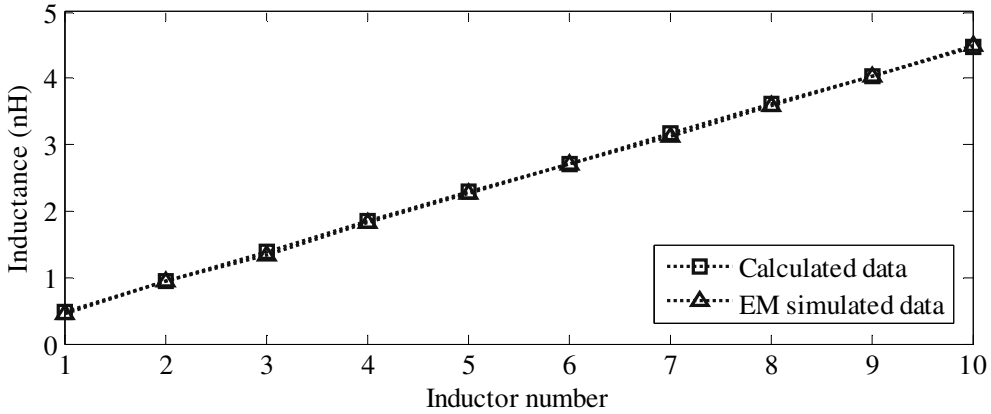


Figure 5.9. Inductance of 2.4 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

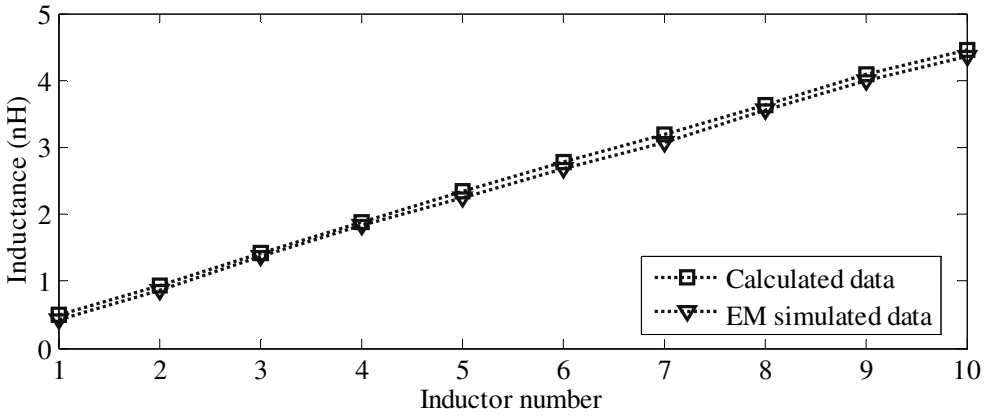


Figure 5.10. Inductance of 2.4 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

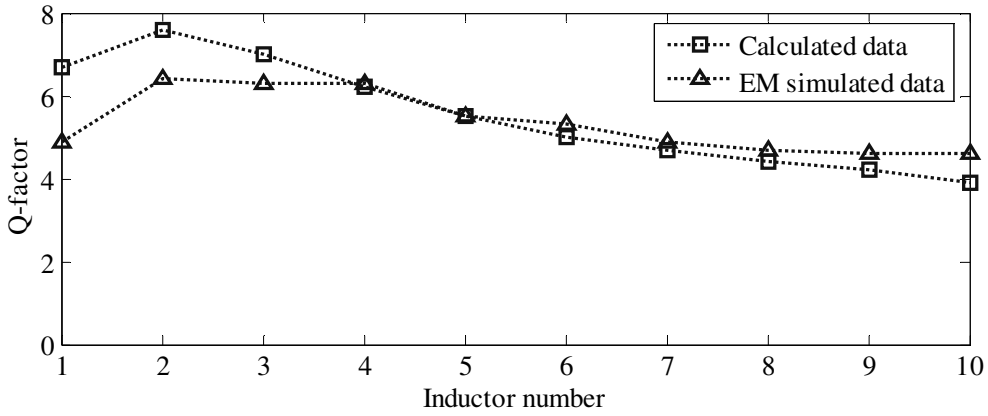


Figure 5.11. Q-factor of 2.4 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

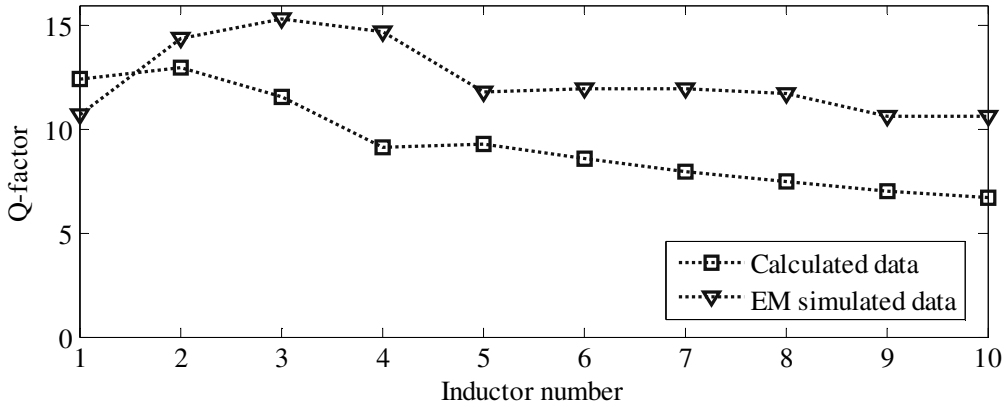


Figure 5.12. Q-factor of 2.4 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

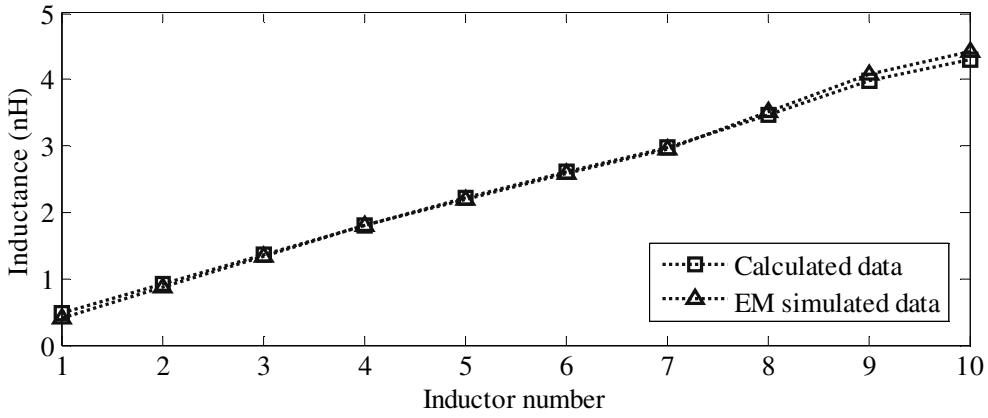


Figure 5.13. Inductance of 5 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

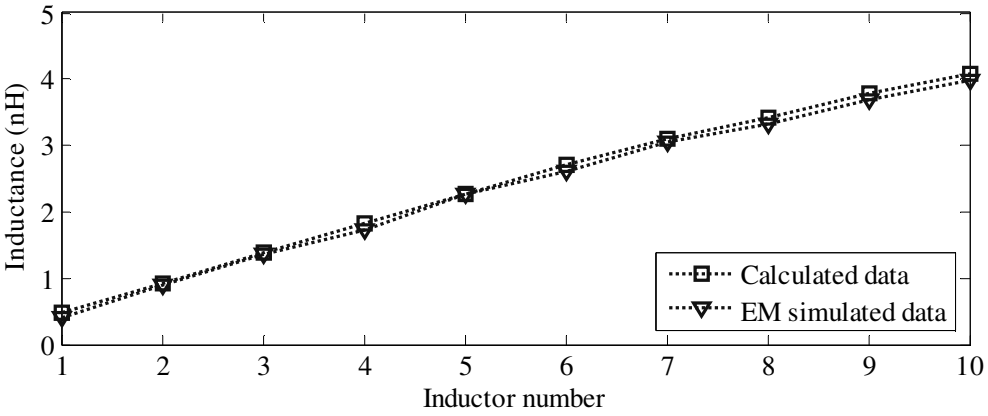


Figure 5.14. Inductance of 5 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

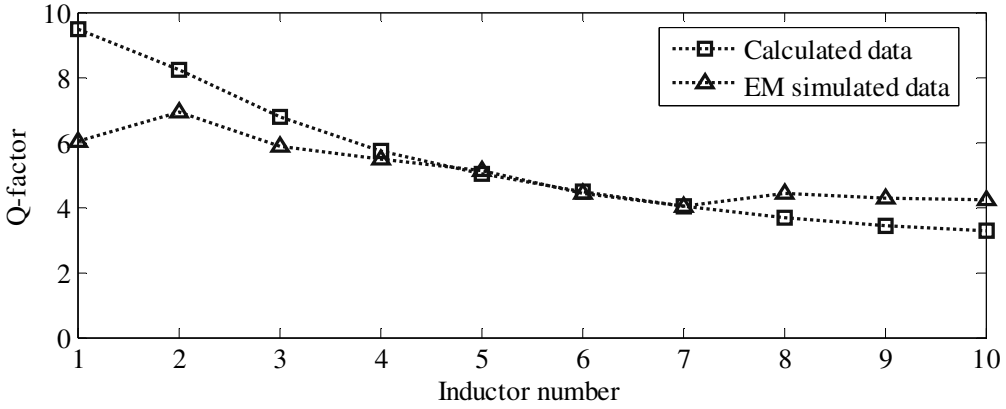


Figure 5.15. Q-factor of 5 GHz 3M inductors designed with inductance search algorithm and simulated by means of EM simulation.

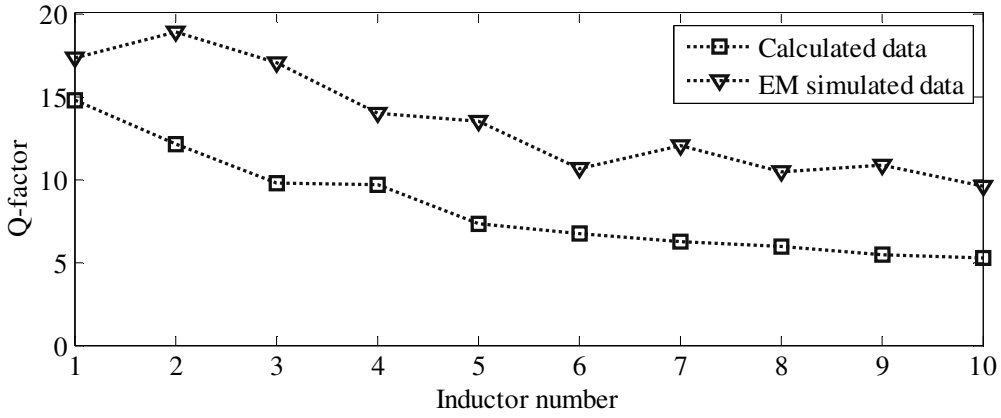


Figure 5.16. Q-factor of 5 GHz TM inductors designed with inductance search algorithm and simulated by means of EM simulation.

5.3 VERIFICATION OF THE FULL SYSTEM INTEGRATION ROUTINE

In order to verify the completeness of the full system integration routine, the routine was used to design two Class-E and two Class-F PAs intended for the 2.4 GHz ISM band. Basic simulations were performed on each of four configurations to determine a better one for each Class-E and Class-F PA. Chosen configurations were then designed and simulated further, to include biasing and matching networks, to make the full PA systems layout-ready. Each of the Class-E and Class-F stages is treated in a separate section.

5.3.1 Lower power Class-E configuration

5.3.1.1 Design

The first designed configuration was the lower power Class-E configuration. Aimed output power was 25 mW, or 14 dBm, with the loaded quality factor of 5. HS HBT npn254 transistor with total emitter length of 96 μm was chosen for the design to obtain maximum available gain. The supply voltage of 0.5 V was taken as a safe operating voltage. It was assumed that it would be possible to connect 100 nH RFC externally to the IC. Matching bandwidth of 500 MHz was taken as reasonable should Π or T-network be implemented in the design. The chosen design parameters, as well as component values calculated by the design routine, are shown in Table 5.3.

Table 5.3. Chosen and calculated parameters for the design of the lower power Class-E PA.

Parameter	Value	Unit
Centre frequency (f_o)	2.4	GHz
Loaded quality factor (Q_L)	5	-
Aimed output power (P_{out})	25	mW
Supply voltage (V_{CC})	0.5	V
Matching bandwidth (BW)	500	MHz
RFC (L_1)	100	nH
Required load resistance (R_L)	5.77	Ω
Series inductance (L_2)	1.91	nH
Series capacitance (C_2)	3.42	pF
Shunt capacitance (C_1)	2.11	pF
DC current (I_{DC})	49.97	mA
Peak collector voltage (v_{Cp})	1.78	V
Peak collector current (i_{sp})	143	mA
L-network matching inductance (L_M)	1.2	nH
L-network matching capacitance (C_M)	4.15	pF
Ind-cap-ind T-network matching inductance 1 (L_{M1})	1.837	nH
Ind-cap-ind T-network matching capacitance 1 (C_{M1})	2.932	pF
Ind-cap-ind T-network matching inductance 2 (L_{M2})	4.417	nH
Cap-ind-cap T-network matching capacitance 1 (C_{M1})	2.964	pF
Cap-ind-cap T-network matching inductance 1 (L_{M1})	1.500	nH
Cap-ind-cap T-network matching capacitance 2 (C_{M2})	0.996	pF
Ind-cap-ind Π-network matching inductance 1 (L_{M1})	0.287	nH
Ind-cap-ind Π-network matching capacitance 1 (C_{M1})	5.200	pF
Ind-cap-ind Π-network matching inductance 2 (L_{M2})	0.691	nH
Cap-ind-cap Π-network matching capacitance 1 (C_{M1})	15.309	pF
Cap-ind-cap Π-network matching inductance 1 (L_{M1})	0.846	nH
Cap-ind-cap Π-network matching capacitance 2 (C_{M2})	6.366	nH

To complete the design, L-network matching was chosen and 3M inductors were selected for the implementation of inductors L_2 (named M30191N) and L_M (named M30120N). Table 5.4 shows geometry and Q-factors for the two inductors found by the inductance search algorithm. The exported netlist of the whole PA design is shown in Figure 5.17.

Table 5.4. Computed 3M inductor parameters for the lower power Class-E design.

Parameter	Value (M30191N)	Value (M30120N)	Unit
Inductance at 2.4 GHz (L_S)	1.92	1.20	nH
Inductance at DC (L_{SLF})	1.78	1.12	nH
Q-factor (Q)	6.18	7.31	-
Resonant frequency (f_R)	8.19	8.59	GHz
Turn width (w)	33.0	50.0	µm
Turn spacing (s)	2.00	2.00	µm
Inner diameter (d_{in})	186	110	µm
Outer diameter (d_{out})	322	314	µm
Number of turns (n)	2	2	-

```
.SUBCKT L2 L1 L2 GND
CS L1 L2 77.10fF
LS N4 L1 1.78n
RS N4 L2 2.59
Csi1 N2 GND 78.38fF
Csi2 N3 GND 78.38fF
Cox1 L1 N2 355.85fF
Cox2 L2 N3 355.85fF
Rsi1 N2 GND 269.76
Rsi2 N3 GND 269.76
.ENDS

.SUBCKT LM L1 L2 GND
CS L1 L2 177.00fF
LS N4 L1 1.12n
RS N4 L2 1.50
Csi1 N2 GND 75.61fF
Csi2 N3 GND 75.61fF
Cox1 L1 N2 448.95fF
Cox2 L2 N3 448.95fF
Rsi1 N2 GND 279.04
Rsi2 N3 GND 279.04
.ENDS

.SUBCKT class-E-1 bias supply Gnd
LRFC_2 supply N_2 100.00n
XL2_1 N_5 N_M1 Gnd L2
RResistor_1 N_M2 Gnd 50.00 TC=0.0, 0.0
Xnpn254_1 N_2 bias Gnd Gnd npn254 area=96
CCapacitor_1 N_2 Gnd 2.11p
CCapacitor_2 N_2 N_5 3.42p
XLM_1 Gnd N_M2 Gnd LM
CCapacitor_M N_M1 N_M2 4.15p
.ENDS
```

Figure 5.17. Exported netlist of the lower power Class-E design.

5.3.1.2 Simulation

Figure 5.18 shows the circuit diagram of the PA system, with ideal sources used for power supply and drive voltages.

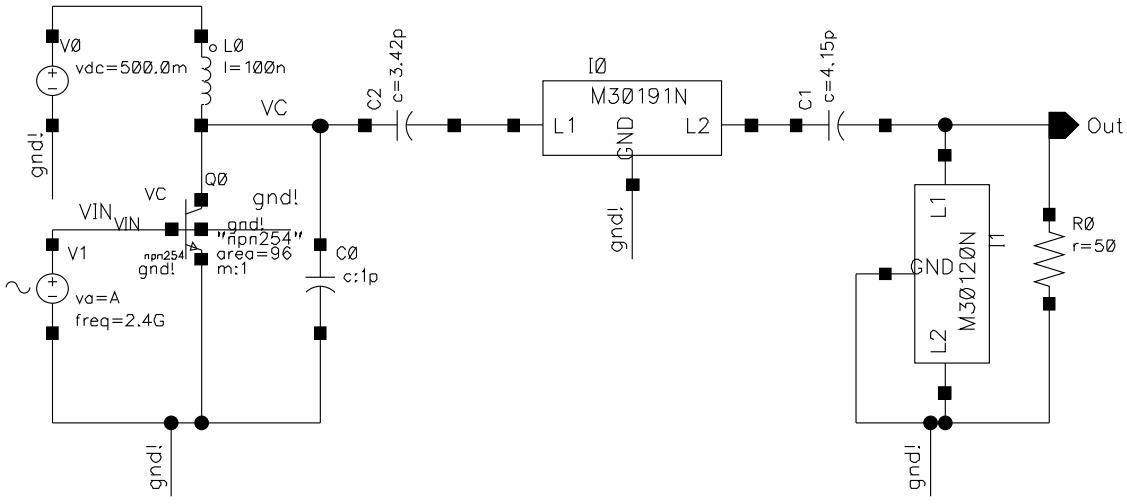


Figure 5.18. Circuit diagram of the lower power Class-E PA design.

The frequency domain simulation of the PA including the collector voltage waveform and output voltage waveform is shown in Figure 5.19. Biasing point of the drive voltage was

determined by sweeping the DC voltage across the base of the transistor. The biasing voltage was swept around typical V_{BE} voltage of the HBT, so that near-to-Class-B biasing could be established with maximum output voltage. The results of the sweep pertaining to the output voltage waveform are shown in Figure 5.20. From this figure it was clear that the biasing voltage of about 0.88 V gave best results. The time domain simulation of all relevant voltage and current waveforms after the optimum biasing point was established is shown in Figure 5.21 and Figure 5.22.

From Figure 5.21 and Figure 5.22, it can be seen that the peak-to-peak output voltage over 50 Ω load is 1.21 V and the DC current consumption is 34.0 mA. This results in collector efficiency of the stage of 21 % with output power of only 3.64 mW (5.61 dBm). As expected, the output specification of the stage was not reached, due to nonideal inductors and the fact that the HBT does not act as an ideal switch. The same set of simulations was performed on the same system using ideal inductors, resulting in an output power of 7.84 dBm, and showing that 2.23 dBm decrease in output power can be directly attributed to low quality inductors.

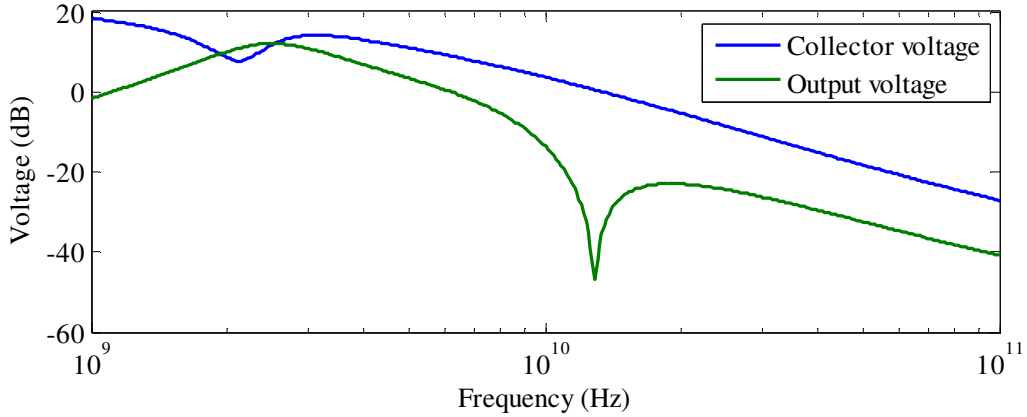


Figure 5.19. Frequency response of the lower power Class-E design.

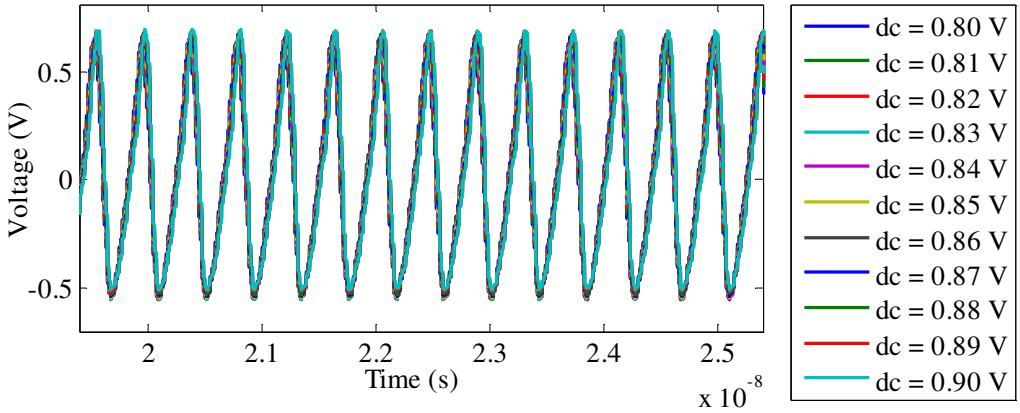
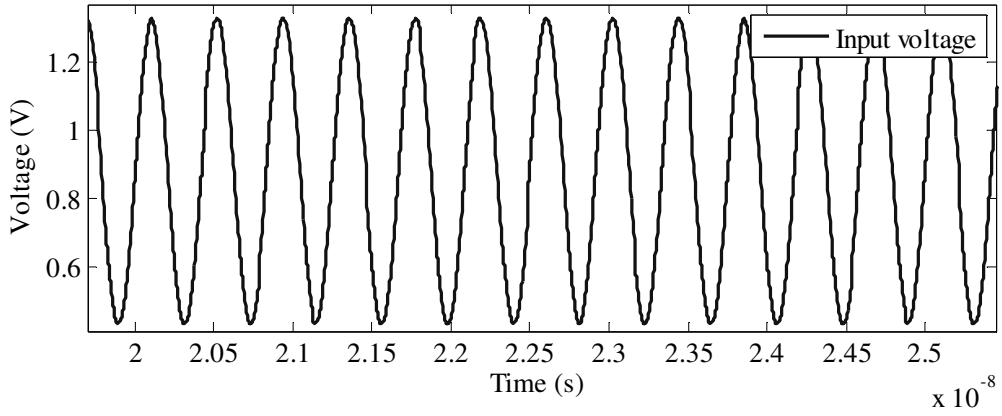
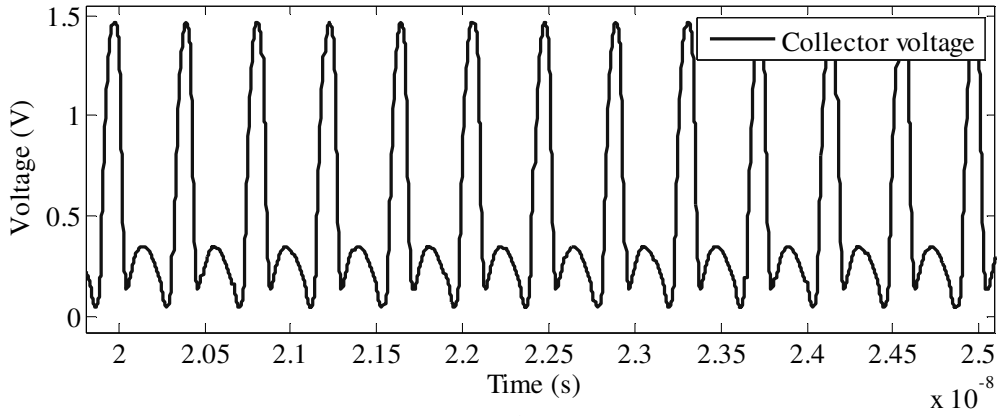


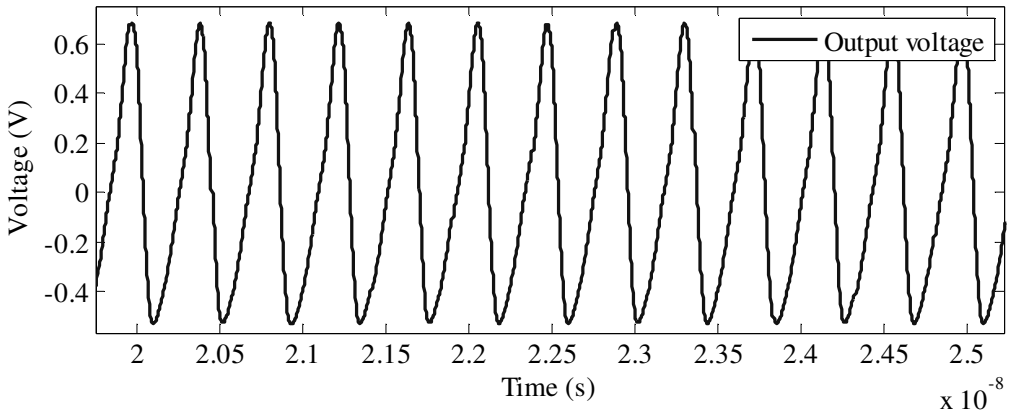
Figure 5.20. DC sweep of the input biasing voltage of the lower power Class-E design with output voltage waveform as the output.



(a)



(b)



(c)

Figure 5.21. Transient response of (a) input voltage, (b) collector voltage and (c) output voltage waveforms of the lower power Class-E design.

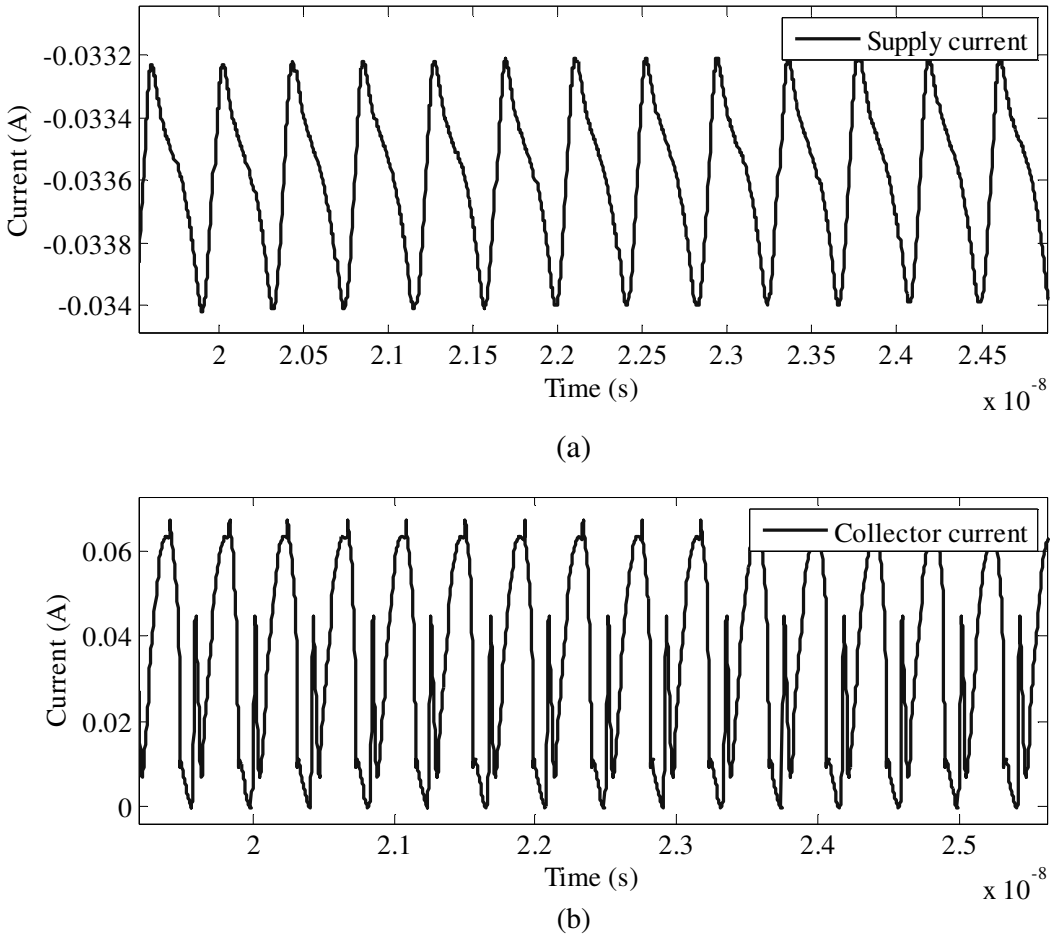


Figure 5.22. Transient response of (a) supply current and (b) collector current waveforms of the lower power Class-E design.

5.3.2 Higher power Class-E configuration

5.3.2.1 Design

The second designed configuration was the higher power Class-E configuration. Aimed output power was 50 mW, or 17 dBm, again with the loaded quality factor of 5. HV HBT npn254h5 transistor with total emitter length of 96 μm was chosen for this design. Although its frequency response at 2.4 GHz frequency is somewhat inferior to that of its HS counterpart, its inclusion allowed for the higher supply voltage of 1 V to be used. External RFC of 100 nH was used again, and the matching bandwidth of 1 GHz was observed to result in reasonable component values for the Π or T network. The chosen design parameters, as well as component values calculated by the design routine, are shown in Table 5.5.

Table 5.5. Chosen and calculated parameters for the design of the higher power Class-E PA.

Parameter	Value	Unit
Centre frequency (f_o)	2.4	GHz
Loaded quality factor (Q_L)	5	-
Aimed output power (P_{out})	50	mW
Supply voltage (V_{CC})	1	V
Matching bandwidth (BW)	1	GHz
RFC (L_1)	100	nH
Required load resistance (R_L)	11.5	Ω
Series inductance (L_2)	3.83	nH
Series capacitance (C_2)	1.71	pF
Shunt capacitance (C_1)	1.05	pF
DC current (I_{DC})	49.97	mA
Peak collector voltage (v_{Cp})	3.56	V
Peak collector current (i_{sp})	143	mA
L-network matching inductance (L_M)	1.82	nH
L-network matching capacitance (C_M)	3.15	pF
Ind-cap-ind T-network matching inductance 1 (L_{M1})	1.837	nH
Ind-cap-ind T-network matching capacitance 1 (C_{M1})	2.676	pF
Ind-cap-ind T-network matching inductance 2 (L_{M2})	2.482	nH
Cap-ind-cap T-network matching capacitance 1 (C_{M1})	2.394	pF
Cap-ind-cap T-network matching inductance 1 (L_{M1})	1.643	nH
Cap-ind-cap T-network matching capacitance 2 (C_{M2})	1.172	pF
Ind-cap-ind Π-network matching inductance 1 (L_{M1})	1.022	nH
Ind-cap-ind Π-network matching capacitance 1 (C_{M1})	2.848	pF
Ind-cap-ind Π-network matching inductance 2 (L_{M2})	1.382	nH
Cap-ind-cap Π-network matching capacitance 1 (C_{M1})	4.301	pF
Cap-ind-cap Π-network matching inductance 1 (L_{M1})	1.544	nH
Cap-ind-cap Π-network matching capacitance 2 (C_{M2})	3.183	nH

To complete the design, the capacitor-inductor-capacitor Π-network matching was chosen and TM-inductors were selected for the implementation of inductors L_2 (named M40383N) and L_{M1} (named M40154N). Table 5.6 shows the geometry and Q-factors for the two inductors as found by the inductance search algorithm. The exported netlist of the whole PA design is shown in Figure 5.23.

Table 5.6. Computed TM-inductor parameters for the higher power Class-E design.

Parameter	Value (M40383N)	Value (M40154N)	Unit
Inductance at 2.4 GHz (L_S)	3.83	1.55	nH
Inductance at DC (L_{SLF})	3.47	1.45	nH
Q-factor (Q)	7.66	11.5	-
Resonant frequency (f_R)	7.46	9.39	GHz
Turn width (w)	14.0	34.0	µm
Turn spacing (s)	2.00	2.00	µm
Inner diameter (d_{in})	164	110	µm
Outer diameter (d_{out})	256	314	µm
Number of turns (n)	2	2	-

```
.SUBCKT L2 L1 L2 GND
CS L1 L2 20.82fF
LS N4 L1 3.47n
RS N4 L2 3.81
Csi1 N2 GND 79.47fF
Csi2 N3 GND 79.47fF
Cox1 L1 N2 165.21fF
Cox2 L2 N3 165.21fF
Rsi1 N2 GND 266.94
Rsi2 N3 GND 266.94
.ENDS

.SUBCKT LM6 L1 L2 GND
CS L1 L2 81.84fF
LS N4 L1 1.45n
RS N4 L2 1.15
Csi1 N2 GND 70.03fF
Csi2 N3 GND 70.03fF
Cox1 L1 N2 236.82fF
Cox2 L2 N3 236.82fF
Rsi1 N2 GND 301.87
Rsi2 N3 GND 301.87
.ENDS

.SUBCKT Class-E-2 bias supply Gnd
LRFC_2 supply N_2 100.00n
XL2_1 N_5 N_M1 Gnd L2
RResistor_1 N_M2 Gnd 50.00 TC=0.0, 0.0
Xnpn254_1 N_2 bias Gnd Gnd npn254h5 area=96
CCapacitor_1 N_2 Gnd 1.05p
CCapacitor_2 N_2 N_5 1.71p
CCapacitor_M1 Gnd N_M1 4.30p
CCapacitor_M2 Gnd N_M2 3.18p
XLM6_1 N_M1 N_M2 Gnd LM6
.ENDS
```

Figure 5.23. Exported netlist of the higher power Class-E design.

5.3.2.2 Simulation

Figure 5.24 shows the circuit diagram of the PA system, with ideal sources used for the power supply and drive voltages.

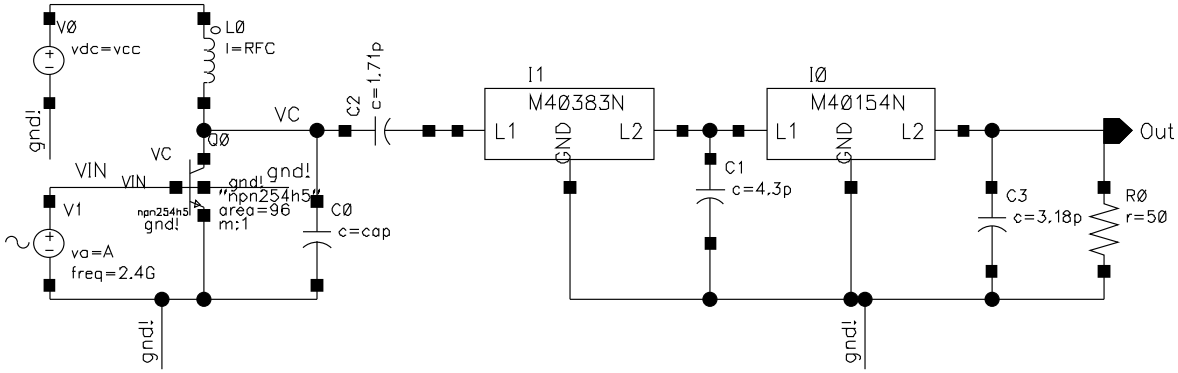


Figure 5.24. Circuit diagram of the higher power Class-E PA design.

Frequency domain simulation of the PA, including the collector voltage and output voltage waveforms, is shown in Figure 5.25. The biasing point of the drive voltage was determined by sweeping the DC voltage across the base of the transistor. The biasing voltage was swept around the typical V_{BE} voltage of the HBT, so that near-to-Class-B biasing could be

established with the maximum output power. The results of the sweep pertaining to the output voltage waveforms are shown in Figure 5.26. From this figure it was established that the biasing voltage of about 0.82 V gave best results. The time domain simulation of all relevant voltage and current waveforms after establishing optimum biasing point is shown in Figure 5.27 and Figure 5.28.

From Figure 5.27 and Figure 5.28, the peak-to-peak output voltage over 50 Ω load is 1.92 V and the DC current consumption is 39.0 mA. This results in collector efficiency of the stage of 23.5 % with output power of 9.2 mW (9.6 dBm). Once again, the output specification of the stage was not reached but much better output power than that for the lower power stage has been realized with roughly the same collector efficiency. If the same set of simulations is performed on the same system using ideal inductors, the resulting output power is 12.1 dBm, which proves that the 2.5 dBm decrease in output power can be directly attributed to spiral inductors.

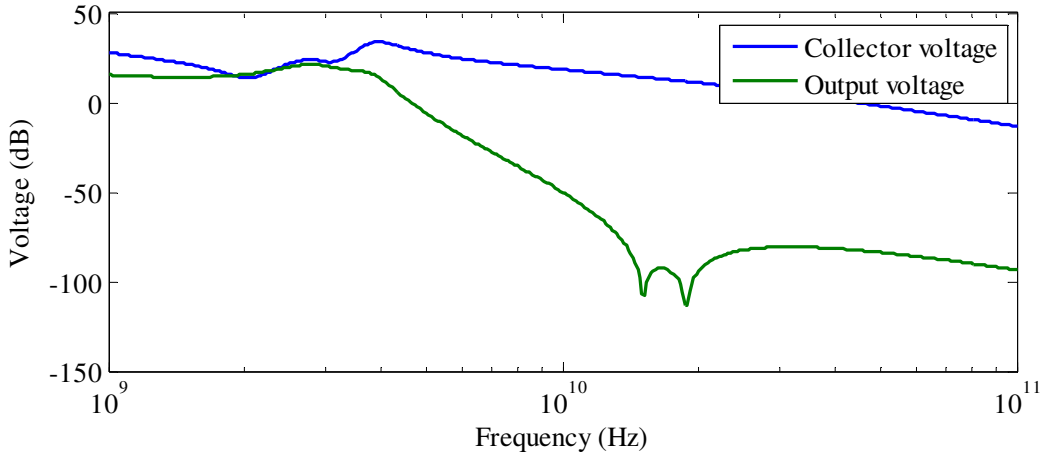


Figure 5.25. Frequency response of the higher power Class-E design.

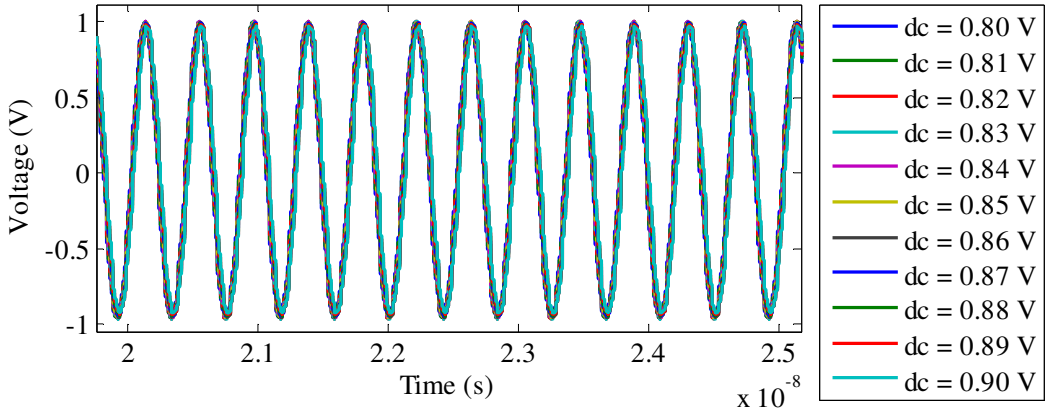


Figure 5.26. DC sweep of the input biasing voltage of the higher power Class-E design with output voltage waveform as output.

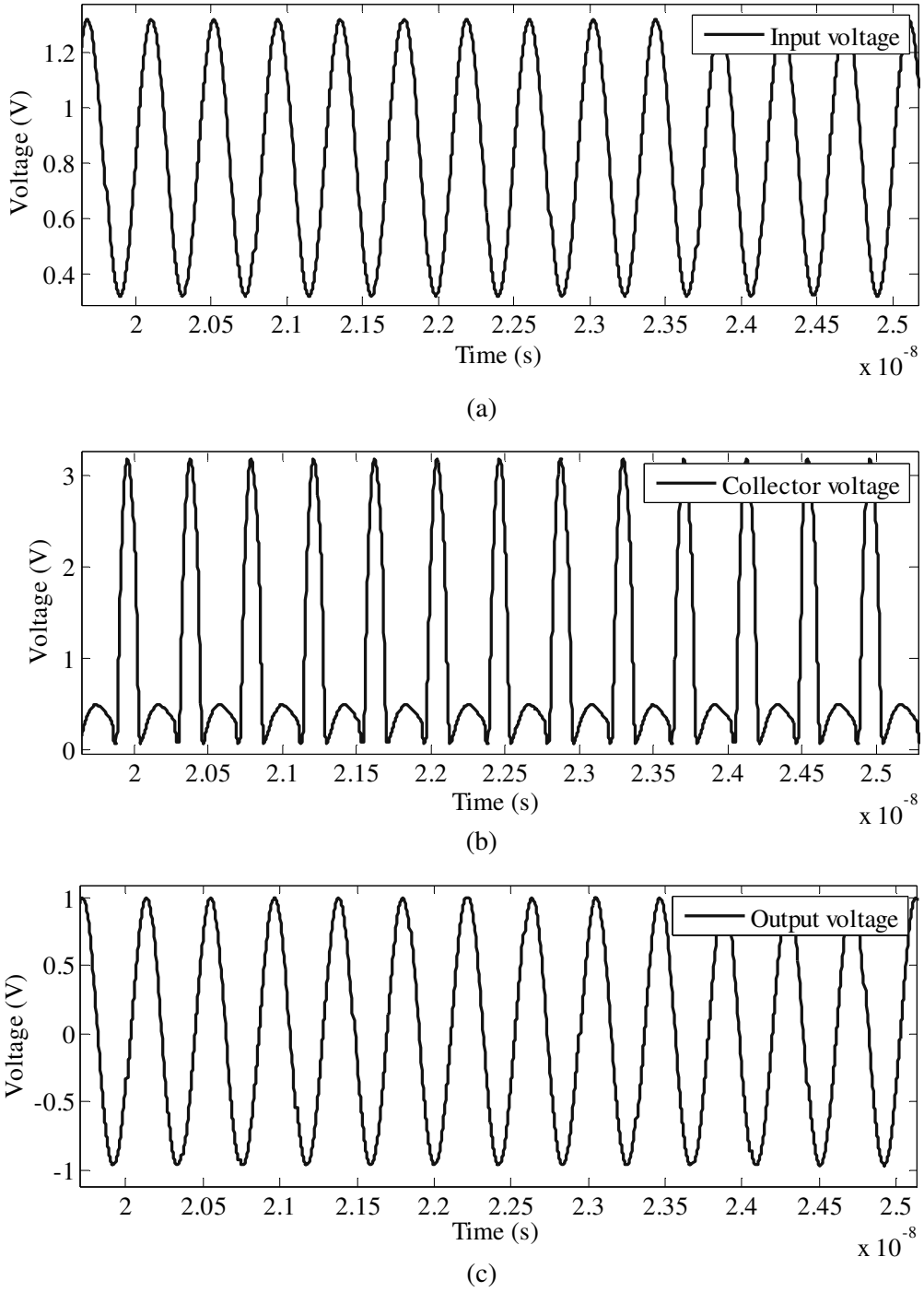


Figure 5.27. Transient response of (a) input voltage, (b) collector voltage and (c) output voltage waveforms of the higher power Class-E design.

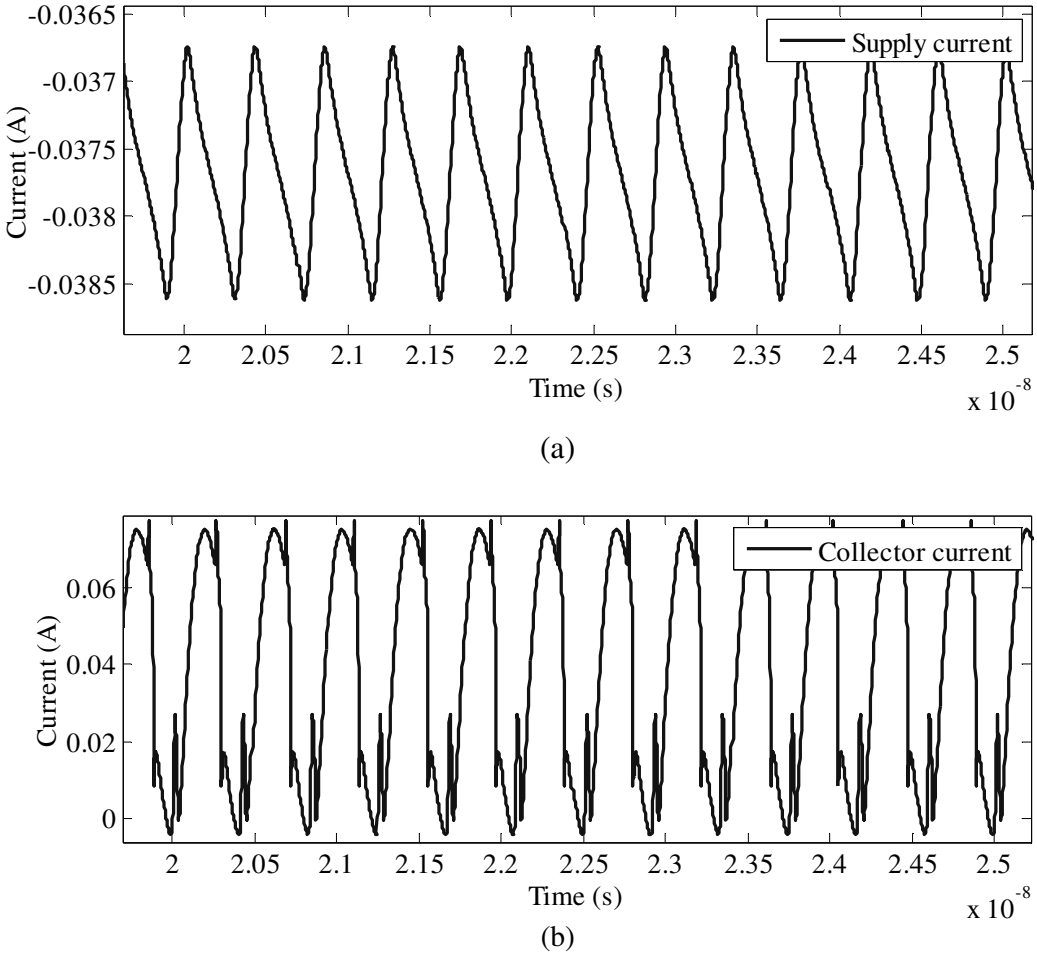


Figure 5.28. Transient response of (a) supply current and (b) collector current waveforms of the higher power Class-E design.

5.3.3 Lower power Class-F configuration

5.3.3.1 Design

The third designed configuration was the lower power Class-F configuration. The aimed output power was 13.5 mW, or 11.3 dBm. This particular power output was chosen so as to obtain an optimum load impedance for maximum power of roughly 50 Ω at DC supply of 1 V. For the maximum available gain, the HS HBT npn254 transistor with total emitter length of 96 μm was chosen. It was again assumed that it would be possible to connect 100 nH RFC externally to the IC. The third harmonic peaking circuit was the topology of choice, with 1 nH and 0.5 nH inductors chosen as filtering inductances for the base- and third-harmonic filters respectively. The chosen design parameters, as well as component values calculated by the design routine, are shown in Table 5.7.

Table 5.7. Chosen and calculated parameters for the design of the lower power Class-F PA.

Parameter	Value	Unit
Centre frequency (f_o)	2.4	GHz
Aimed output power (P_{out})	13.5	mW
Supply voltage (V_{CC})	1	V
RFC (L_1)	100	nH
Required load resistance (R_L)	49.4	Ω
Base filter inductance (L_O)	1.00	nH
Base filter capacitance (C_O)	4.40	pF
Third-harmonic filter inductance (L_3)	0.50	nH
Third-harmonic filter capacitance (C_3)	0.98	pF
DC current (I_{DC})	16.5	mA
Peak collector voltage (v_{Cp})	2.00	V
Peak collector current (i_{sp})	48.1	mA

In order to complete the design the 3M inductors were selected for the implementation of inductors L_O (named M30100N) and L_3 (named M30050N). Table 5.8 shows the geometry and Q-factors for the two inductors as found by the inductance search algorithm. The exported netlist of the whole PA design is shown in Figure 5.29.

Table 5.8. Computed 3M inductor parameters for the lower power Class-F design.

Parameter	Value (M30100N)	Value (M300500N)	Unit
Inductance at 2.4 GHz (L_S)	1.00	0.50	nH
Inductance at DC (L_{SLF})	0.95	0.49	nH
Q-factor (Q)	7.52	6.67	-
Resonant frequency (f_R)	9.51	14.7	GHz
Turn width (w)	50.0	470	µm
Turn spacing (s)	2.00	2.00	µm
Inner diameter (d_{in})	89.0	30.0	µm
Outer diameter (d_{out})	293	222	µm
Number of turns (n)	2	2	-

```
.SUBCKT L0 L1 L2 GND
CS L1 L2 177.00fF
LS N4 L1 0.95n
RS N4 L2 1.37
Csi1 N2 GND 68.94fF
Csi2 N3 GND 68.94fF
Cox1 L1 N2 409.33fF
Cox2 L2 N3 409.33fF
Rsi1 N2 GND 306.05
Rsi2 N3 GND 306.05
.ENDS

.SUBCKT L3 L1 L2 GND
CS L1 L2 156.40fF
LS N4 L1 0.49n
RS N4 L2 1.01
Csi1 N2 GND 47.11fF
Csi2 N3 GND 47.11fF
Cox1 L1 N2 268.66fF
Cox2 L2 N3 268.66fF
Rsi1 N2 GND 448.03
Rsi2 N3 GND 448.03
.ENDS

.SUBCKT class-F-1 bias supply Gnd
LRFC_2 supply N_1 100.00n
CCapacitor_3 N_1 N_4 1.00p
XL0_1 N_2 Gnd Gnd L0
CCapacitor_1 N_2 Gnd
XL3_1 N_4 N_2 Gnd L3
CCapacitor_2 N_4 N_2 0.98p
RResistor_1 N_2 Gnd 49.38 TC=0.0, 0.0
Xnpn254_1 N_1 bias Gnd Gnd npn254 area=96
.ENDS
```

Figure 5.29. Exported netlist of the lower power Class-F design.

5.3.3.2 Simulation

Figure 5.30 shows the circuit diagram of the PA system, with ideal sources used for power supply and drive voltages.

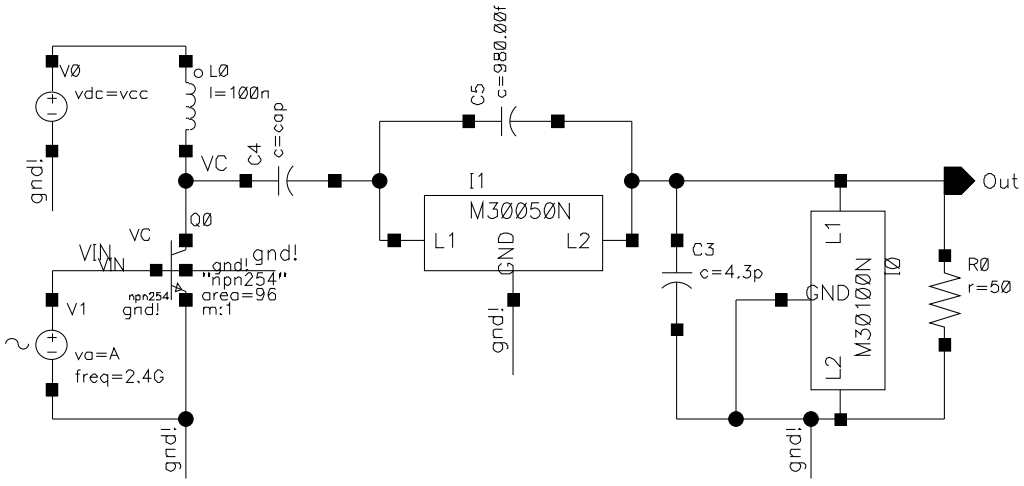


Figure 5.30. Circuit diagram of the lower power Class-F PA design.

The frequency domain simulation of the PA, including the collector voltage waveform and output voltage waveform is shown in Figure 5.31. Biasing point of the drive voltage was

determined by sweeping the DC voltage across the base of the transistor. The biasing voltage was swept just above the V_{BE} voltage of the HBT, so that a near-to-Class-B biasing could be established with maximum output voltage. The results of the sweep pertaining to the output voltage waveform are shown in Figure 5.32. From this figure it was recognized that the biasing voltage of about 0.97 V gives best results. The time domain simulation of all relevant voltage and current waveforms after establishing optimum biasing point is shown in Figure 5.33 and Figure 5.34.

Figure 5.33 and Figure 5.34 show that the peak-to-peak output voltage over 50 Ω load is 1.87 V and the DC current consumption is 64.0 mA. This results in collector efficiency of the stage of 13.7 % with an output power of only 8.74 mW (9.4 dBm) and evident harmonic distortion. From the same set of simulations performed on the same system using ideal inductors, the resulting output power was 11.2 dBm, showing that the 1.8 dBm decrease in output power can be directly attributed to the low quality inductors.

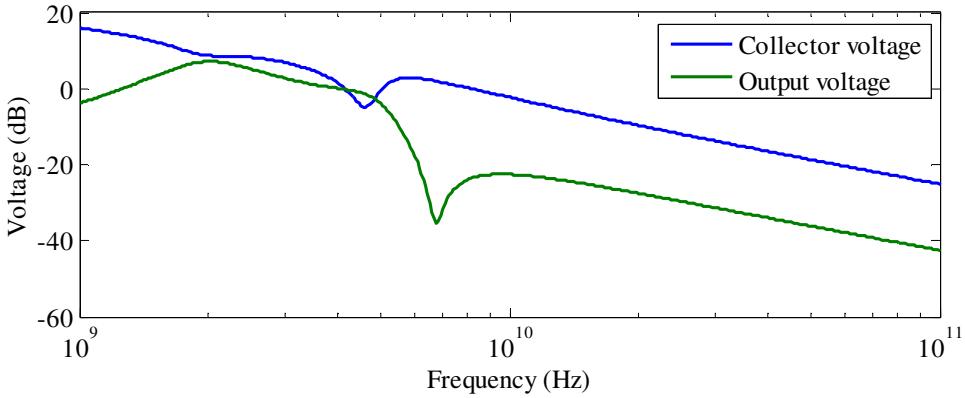


Figure 5.31. Frequency response of the lower power Class-F design.

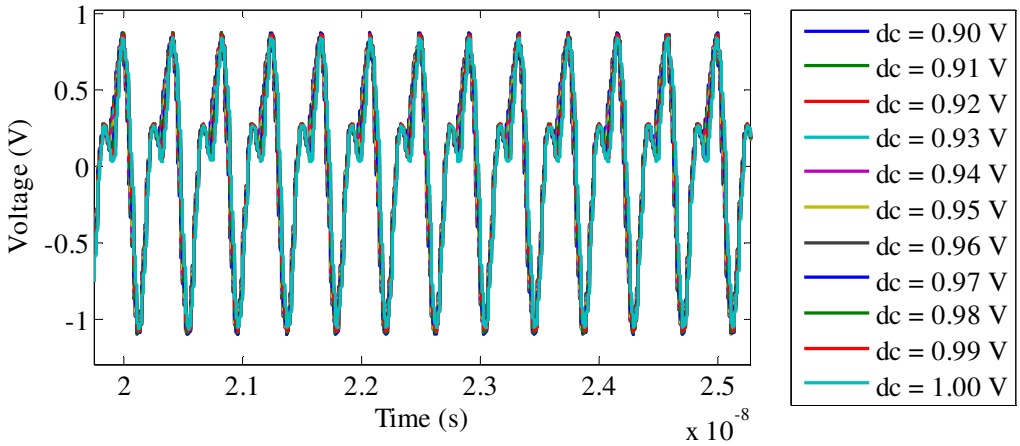


Figure 5.32. DC sweep of the input biasing voltage of the lower power Class-F design with output voltage waveform as output.

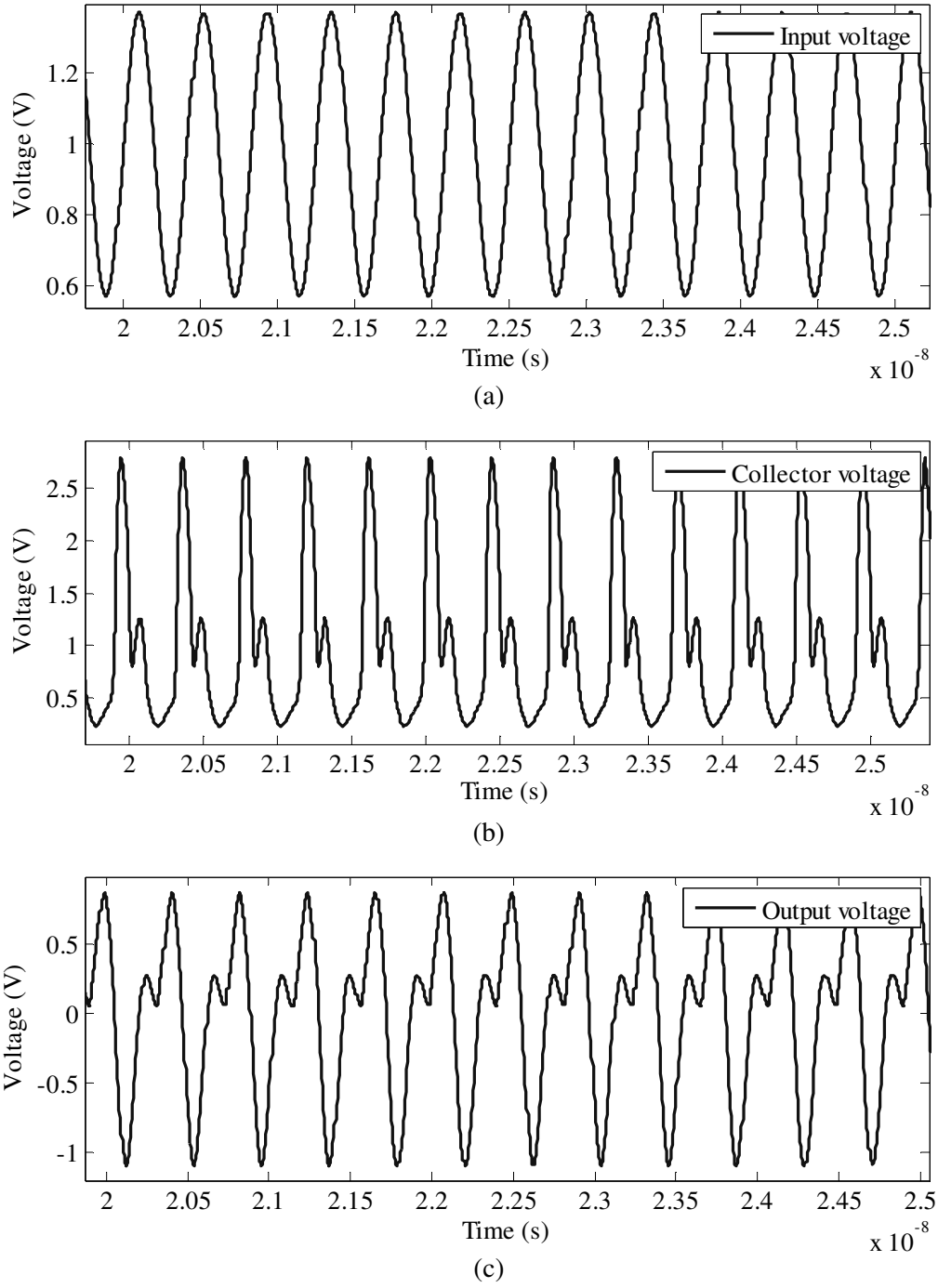


Figure 5.33. Transient response of (a) input voltage, (b) collector voltage and (c) output voltage waveforms of the lower power Class-F design.

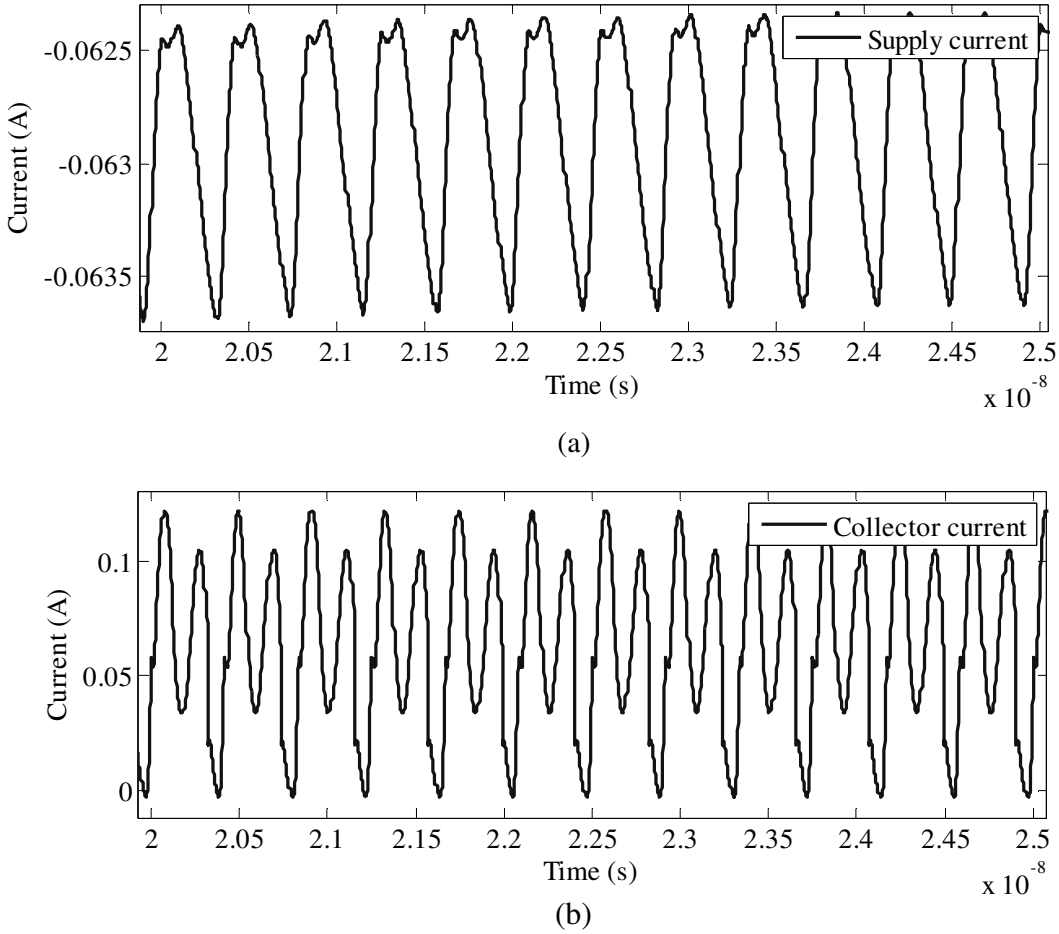


Figure 5.34. Transient response of (a) supply current and (b) collector current waveforms of the lower power Class-F design.

5.3.4 Higher power Class-F configuration

5.3.4.1 Design

The final designed configuration was the higher power Class-F configuration. Aimed output power was 50 mW, or 17.0 dBm. DC supply of 1.5 V was used in conjunction with HV HBT npn254h5 transistor with total emitter length of 96 µm. It was once again assumed that it would be possible to connect a 100 nH RFC externally to the IC. The Class-F output stage with resonators of up to the fifth harmonics was the topology of choice, with 1 nH inductors as filtering inductances for the base filter and 0.5 nH for the third and fifth harmonic filters respectively. Matching networks with 500 MHz bandwidth were considered for output matching. The chosen design parameters, as well as component values calculated by the design routine, are shown in Table 5.9.

Table 5.9. Chosen and calculated parameters for the design of the higher power Class-F PA.

Parameter	Value	Unit
Centre frequency (f_o)	2.4	GHz
Aimed output power (P_{out})	50	mW
Supply voltage (V_{CC})	1.5	V
RFC (L_1)	100	nH
Required load resistance (R_L)	32.8	Ω
Base filter inductance (L_O)	1.00	nH
Base filter capacitance (C_O)	4.40	pF
Third-harmonic filter inductance (L_3)	0.50	nH
Third-harmonic filter capacitance (C_3)	0.98	pF
Fifth-harmonic filter inductance (L_5)	0.50	nH
Fifth-harmonic filter capacitance (C_5)	0.35	pF
DC current (I_{DC})	36.8	mA
Peak collector voltage (v_{Cp})	3.00	V
Peak collector current (i_{sp})	110	mA
L-network matching inductance (L_M)	4.58	nH
L-network matching capacitance (C_M)	2.79	pF
Ind-cap-ind T-network matching inductance 1 (L_{M1})	10.43	nH
Ind-cap-ind T-network matching capacitance 1 (C_{M1})	0.272	pF
Ind-cap-ind T-network matching inductance 2 (L_{M2})	12.74	nH
Cap-ind-cap T-network matching capacitance 1 (C_{M1})	0.421	pF
Cap-ind-cap T-network matching inductance 1 (L_{M1})	6.048	nH
Cap-ind-cap T-network matching capacitance 2 (C_{M2})	0.345	pF
Ind-cap-ind Π-network matching inductance 1 (L_{M1})	0.566	nH
Ind-cap-ind Π-network matching capacitance 1 (C_{M1})	3.698	pF
Ind-cap-ind Π-network matching inductance 2 (L_{M2})	0.691	nH
Cap-ind-cap Π-network matching capacitance 1 (C_{M1})	7.772	pF
Cap-ind-cap Π-network matching inductance 1 (L_{M1})	1.192	nH
Cap-ind-cap Π-network matching capacitance 2 (C_{M2})	6.366	nH

In order to complete the design the TM inductors were selected for the implementation of inductors L_O (named M40100N), L_3 and L_5 (named M40050N) as well as L_{M1} (named M40119N). Table 5.10 shows the geometry and Q-factors for the two inductors as found by the inductance search algorithm. The exported netlist of the whole PA design is shown in Figure 5.35.

Table 5.10. Computed TM inductor parameters for the higher power Class-F design.

Parameter	Value (M40100N)	Value (M400500N)	Value (M40119N)	Unit
Inductance at 2.4 GHz (L_S)	1.00	0.50	1.19	nH
Inductance at DC (L_{SLF})	0.94	0.49	1.13	nH
Q-factor (Q)	13.0	12.4	12.5	-
Resonant frequency (f_R)	9.82	15.0	9.68	GHz
Turn width (w)	48.0	46.0	42.0	µm
Turn spacing (s)	2.00	2.00	2.00	µm
Inner diameter (d_{in})	90.0	31.0	115	µm
Outer diameter (d_{out})	286	219	287	µm
Number of turns (n)	2	2	2	-

```
.SUBCKT L0 L1 L2 GND
CS L1 L2 163.12fF
LS N4 L1 0.94n
RS N4 L2 0.72
Csi1 N2 GND 67.01fF
Csi2 N3 GND 67.01fF
Cox1 L1 N2 279.59fF
Cox2 L2 N3 279.59fF
Rsi1 N2 GND 314.94
Rsi2 N3 GND 314.94
.ENDS

.SUBCKT L3 L1 L2 GND
CS L1 L2 149.81fF
LS N4 L1 0.49n
RS N4 L2 0.53
Csi1 N2 GND 46.40fF
Csi2 N3 GND 46.40fF
Cox1 L1 N2 188.59fF
Cox2 L2 N3 188.59fF
Rsi1 N2 GND 454.91
Rsi2 N3 GND 454.91
.ENDS

.SUBCKT L5 L1 L2 GND
CS L1 L2 149.81fF
LS N4 L1 0.49n
RS N4 L2 0.53
Csi1 N2 GND 46.40fF
Csi2 N3 GND 46.40fF
Cox1 L1 N2 188.59fF
Cox2 L2 N3 188.59fF
Rsi1 N2 GND 454.91
Rsi2 N3 GND 454.91
.ENDS

.SUBCKT LM6 L1 L2 GND
CS L1 L2 124.89fF
LS N4 L1 1.13n
RS N4 L2 0.87
Csi1 N2 GND 67.98fF
Csi2 N3 GND 67.98fF
Cox1 L1 N2 261.28fF
Cox2 L2 N3 261.28fF
Rsi1 N2 GND 310.66
Rsi2 N3 GND 310.66
.ENDS

.SUBCKT Class-F-2 bias supply Gnd
LRFC_2 supply N_1 100.00n
CCapacitor_3 N_1 N_4 1.00p
XL0 N_M1 Gnd Gnd L0
CCapacitor_1 N_M1 Gnd 4.40p
XL3 N_4 N_3 Gnd L3
CCapacitor_2 N_4 N_3 0.98p
XL5 N_3 N_M1 Gnd L5
CCapacitor_4 N_3 N_M1 0.35p
RResistor_1 N_M2 Gnd 50.00 TC=0.0, 0.0
Xnpn254h5_1 N_1 bias Gnd Gnd npn254 area=96
CCapacitor_M1 Gnd N_M1 7.77p
CCapacitor_M2 Gnd N_M2 6.37p
XLM6_1 N_M2 N_M1 Gnd LM6
.ENDS
```

Figure 5.35. Exported netlist of the higher power Class-F design.

5.3.4.2 Simulation

Figure 5.36 shows the circuit diagram of the PA system, with ideal sources used for power supply and drive voltages.

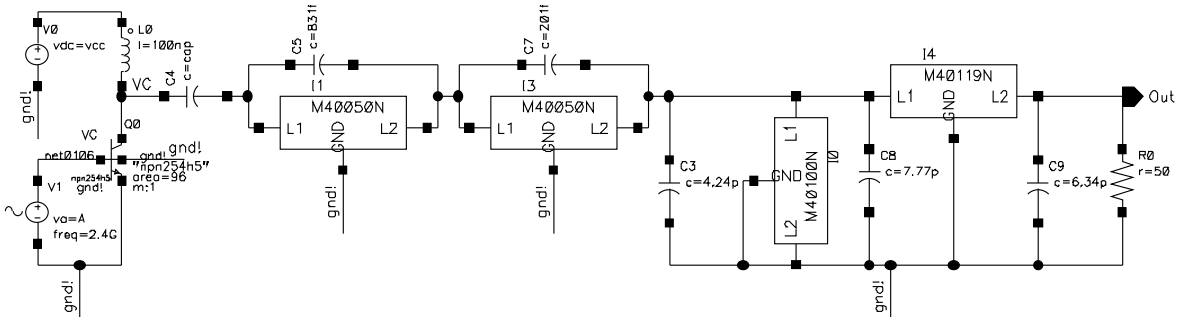


Figure 5.36. Circuit diagram of the higher power Class-F PA design.

Frequency domain simulation of the PA including the collector voltage waveform and output voltage waveform is shown in Figure 5.37. The biasing point of the drive voltage was determined by sweeping the DC voltage across the base of the transistor. The biasing voltage was swept just above the V_{BE} voltage of the HBT, so that a near-to-Class-B biasing could be established with maximum output voltage. The biasing voltage was swept around the V_{BE} voltage of the HBT. The results of the sweep pertaining to the output voltage waveform are shown in Figure 5.38. From this figure it was decided that the biasing voltage of about 0.8 V gave best results. The time domain simulation of all relevant voltage and current waveforms after an optimum biasing point was established is shown in Figure 5.39 and Figure 5.40.

From Figure 5.39 and Figure 5.40 the peak-to-peak output voltage over 50 Ω load is 2.22 V and the DC current consumption is 41.0 mA. This results in collector efficiency of the stage of 20.0 % with output power of 12.3 mW (10.9 dBm) and no evident harmonic distortion. When the same set of simulations was performed on the same system but using ideal inductors, the resulting output power was 13.9 dBm, showing that the 3 dBm decrease in output power can be directly attributed to low quality inductors.

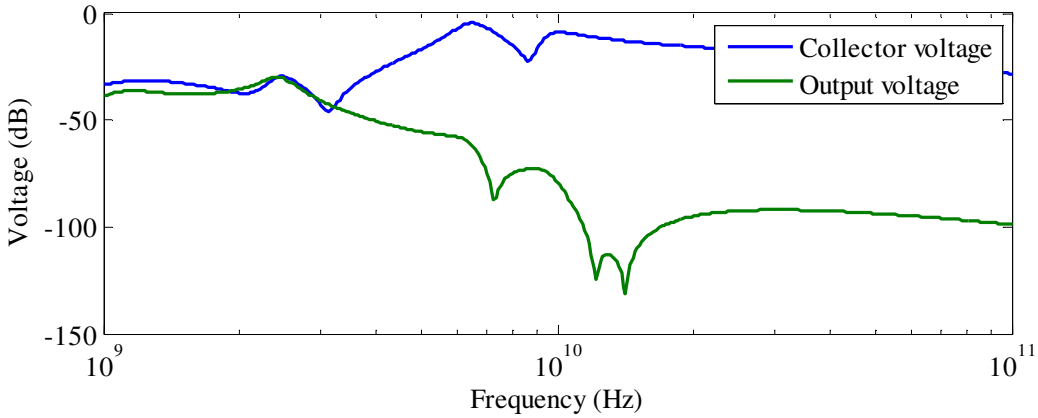


Figure 5.37. Frequency response of the higher power Class-F design.

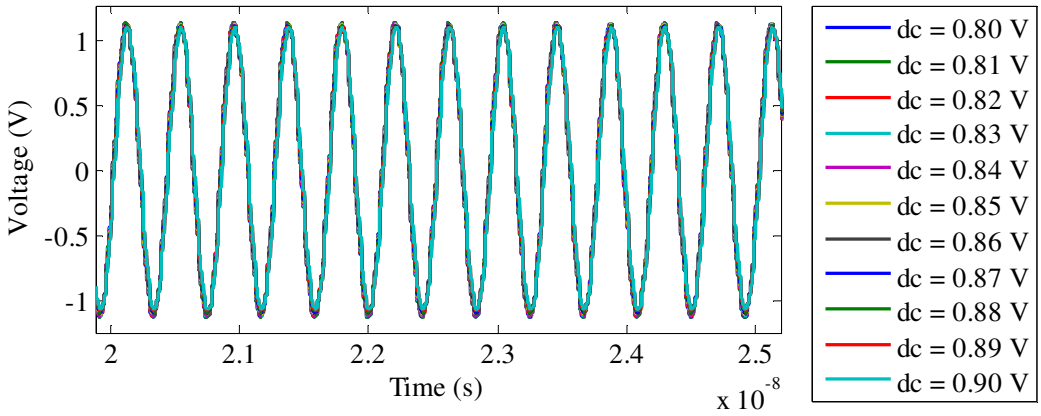
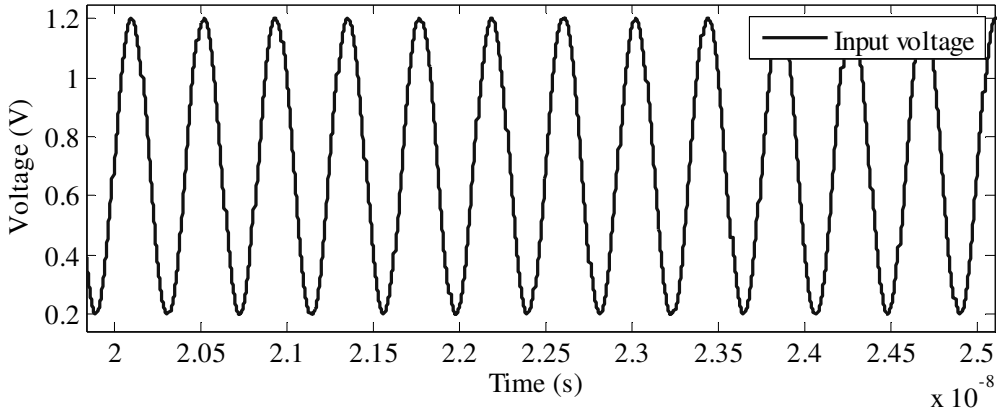
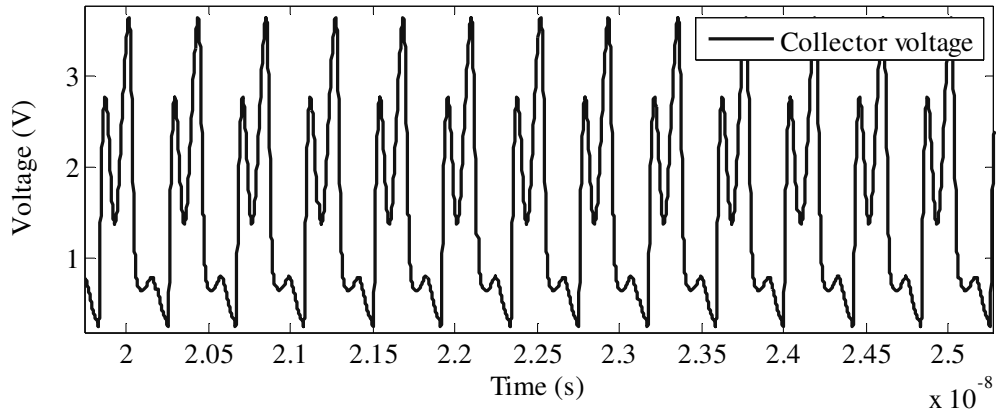


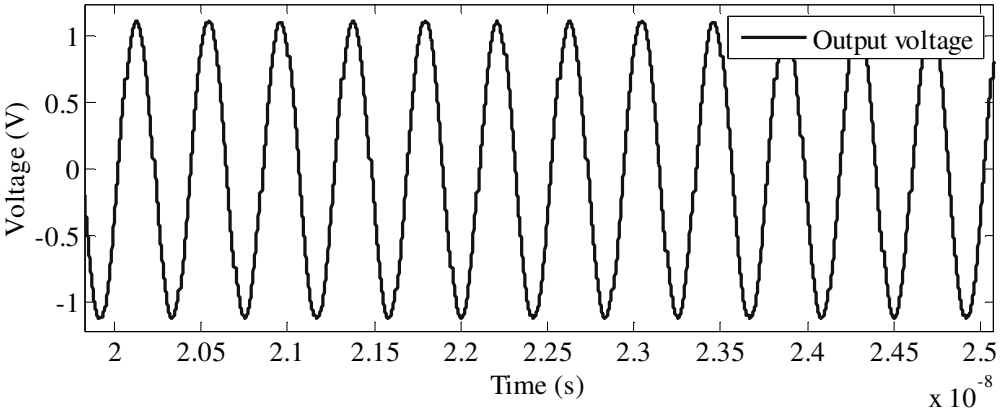
Figure 5.38. DC sweep of the input biasing voltage of the higher power Class-F design with output voltage waveform as the output.



(a)



(b)



(c)

Figure 5.39. Transient response of (a) input voltage, (b) collector voltage and (c) output voltage waveforms of the higher power Class-F design.

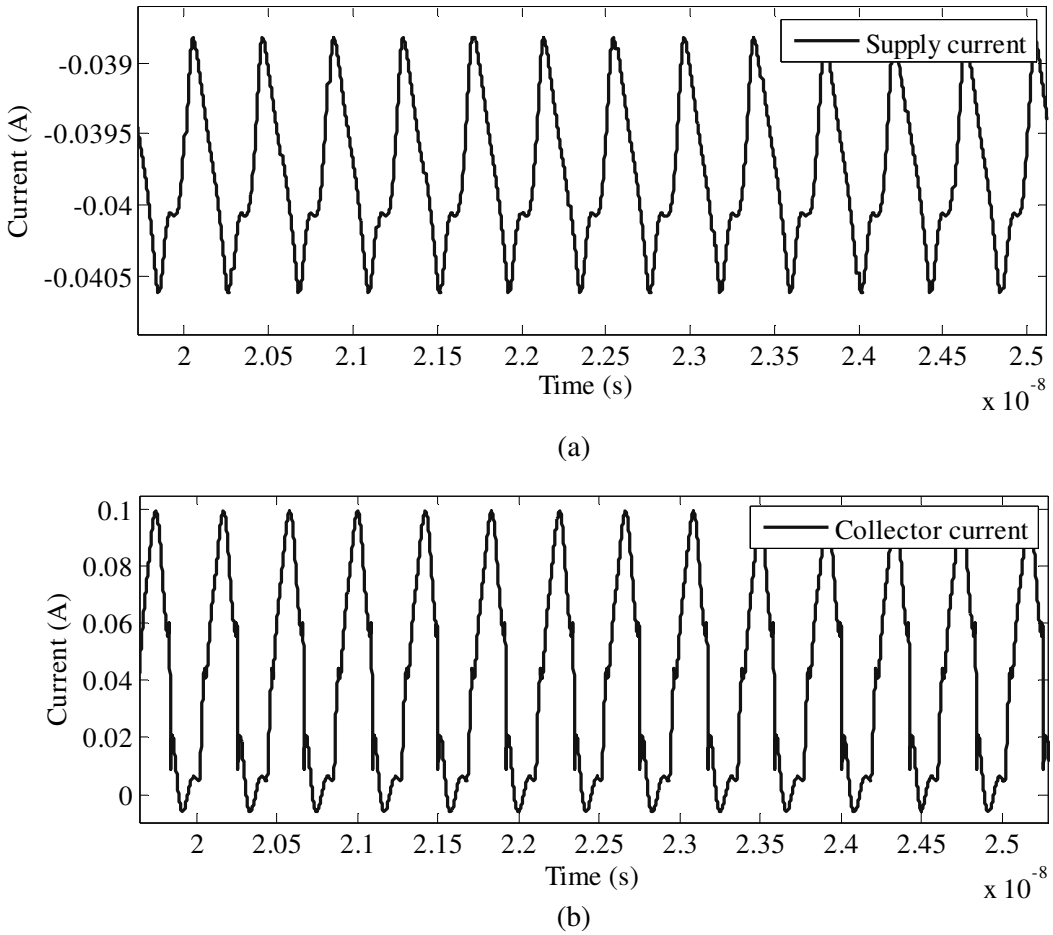


Figure 5.40. Transient response of (a) supply current and (b) collector current waveforms of the higher power Class-F design.

5.3.5 Choice of better Class-E and Class-F configuration

From the analyses in Sections 5.3.1 through 5.3.4, it is evident that both in case of Class-E and Class-F amplifiers, the configuration identified as the "higher power" configuration gives better quality amplification. In both cases, the output power, collector efficiency and harmonic distortion of the output signal are evidently better than those for their "lower power" counterparts.

In neither case the designed output power was reached, which was due to the loss of gain and output power capability of the HBT at the design frequency of 2.4 GHz. Further loss of output power was experienced due to the implementation of modelled spiral inductors. Both loss mechanisms were considered acceptable within the scope of this thesis.

5.4 FURTHER DESIGN OF THE CLASS-E AMPLIFIER

An active biasing network similar to the one described in [33] was designed from first principles in order to provide the bias of 0.82 V for the Class-E amplifier described in Section 5.3.2. The *S*-parameter based input impedance matching, described in Section 4.6 was implemented for this PA to match the assumed input source impedance of 50 Ω to the input port (base) of the PA. A simple L matching network was used here. The schematic showing the complete PA, including biasing and input impedance matching, with matching inductors also implemented using spiral inductors, is shown in Figure 5.41. All RFCs and decoupling capacitors were considered to be implemented off-chip.

Temperature sweep from -20 to 120 °C on the output voltage waveform is shown in Figure 5.42. From this figure, it is seen that there is no deterioration of output voltage waveform (and therefore no gain decrease) as temperature increases and therefore emitter and/or base ballasting are not needed. Harmonic content of the same waveform at room temperature (27 °C) is shown in Figure 5.43. From this figure, the THD is only 2.14 %.

Also at room temperature, the PA draws 55 mA from 1 V voltage supply, whilst exhibiting output power of 6.3 mW, resulting in collector efficiency of 11.3 %. For 1 mW input power level, the PAE is 9.6 %.

The *S*-parameters of the PA modelled as two port network (where ground represents the second port) are shown in Figure 5.44 to Figure 5.47 [110]. From these figures, it is evident that input and output port of this PA are well matched, and that in the forward direction, the system acts as an amplifier, whilst in the reverse direction, the system acts as an attenuator, as expected.

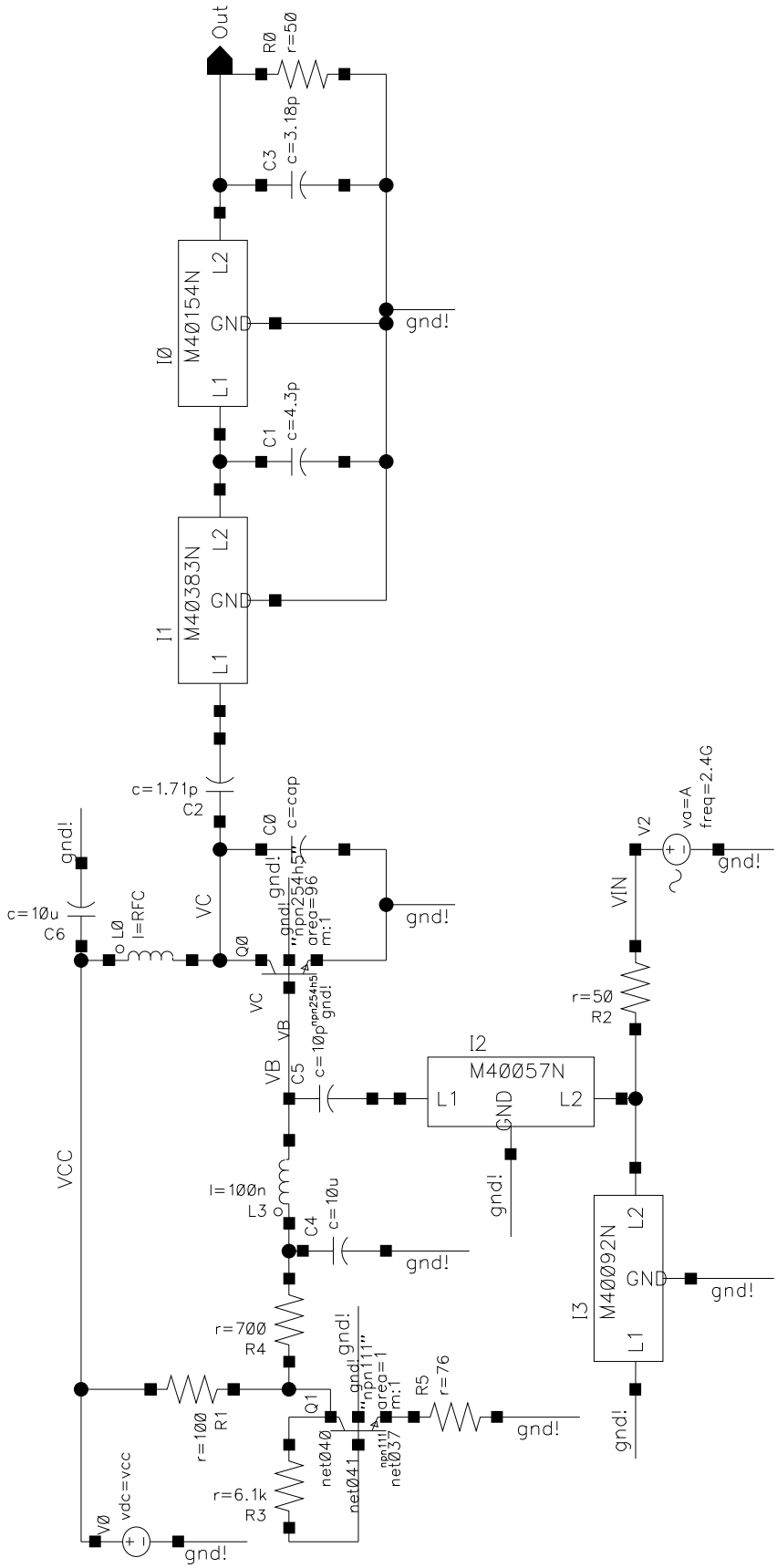


Figure 5.41. Designed Class-E PA with biasing and matching networks.

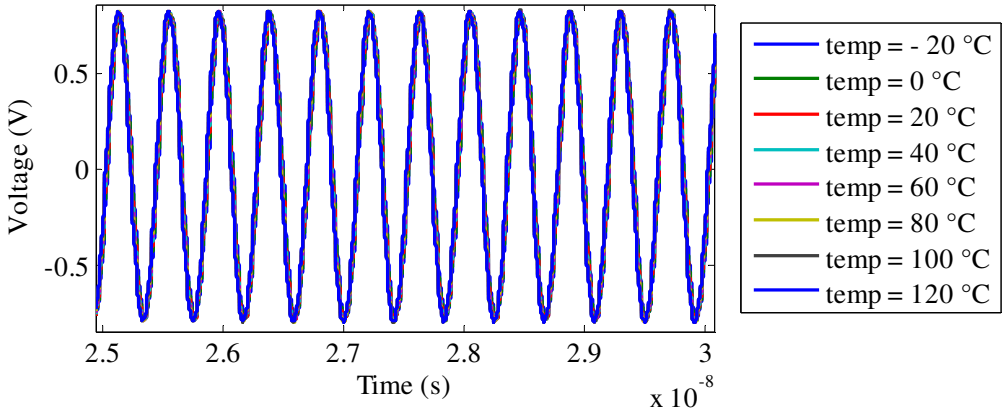


Figure 5.42. Temperature-swept output voltage waveform of the full Class-E PA.

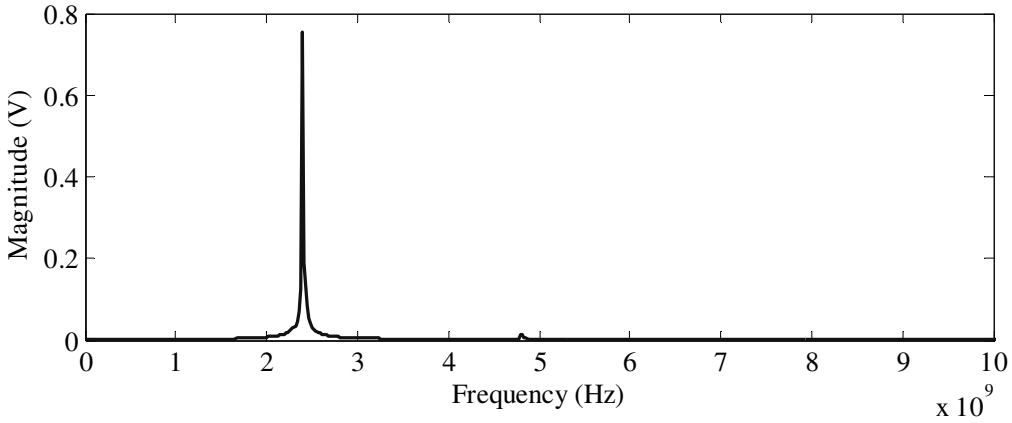


Figure 5.43. Harmonics of the output voltage waveform of the designed Class-E PA system.

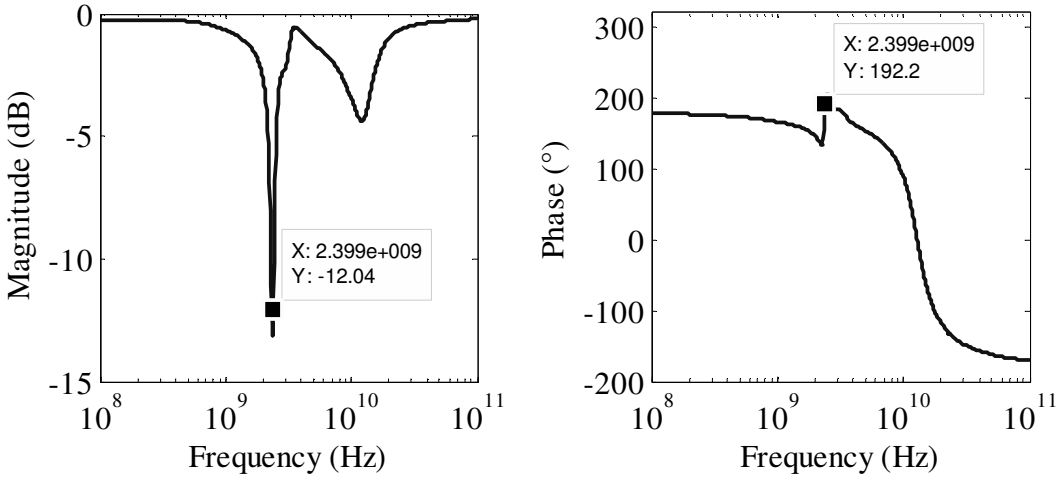


Figure 5.44. Input port voltage reflection coefficient (S_{11}) of the designed Class-E PA system.

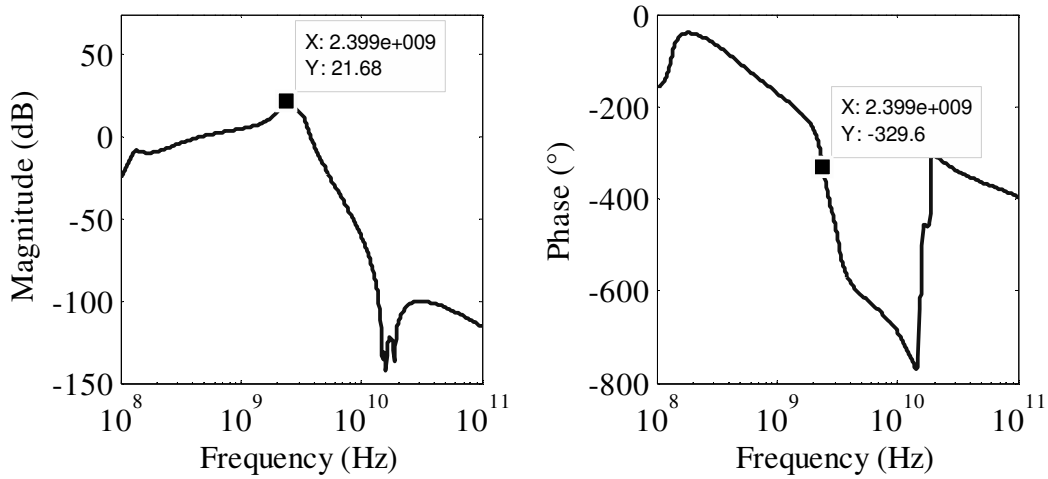


Figure 5.45. Forward voltage gain (S_{21}) of the designed Class-E PA system.

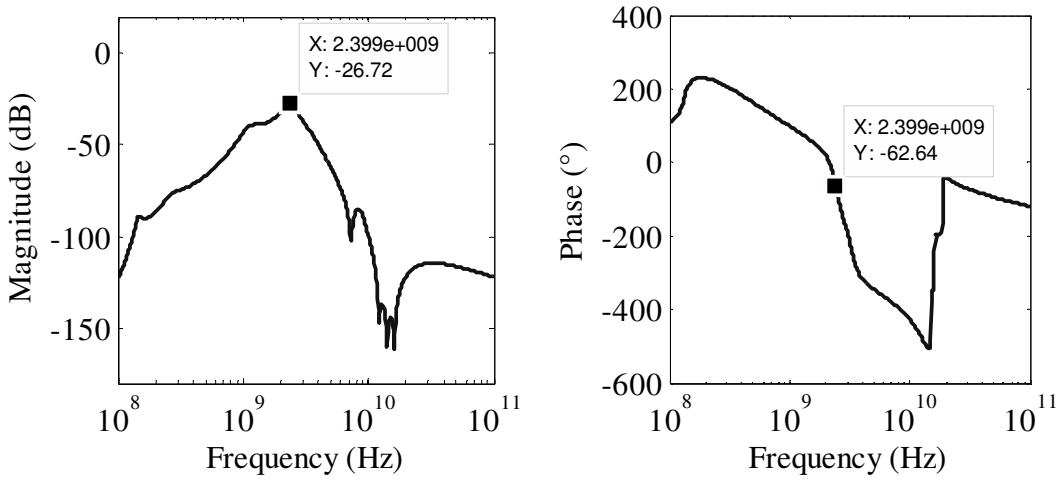


Figure 5.46. Reverse voltage gain (S_{12}) of the designed Class-E PA system.

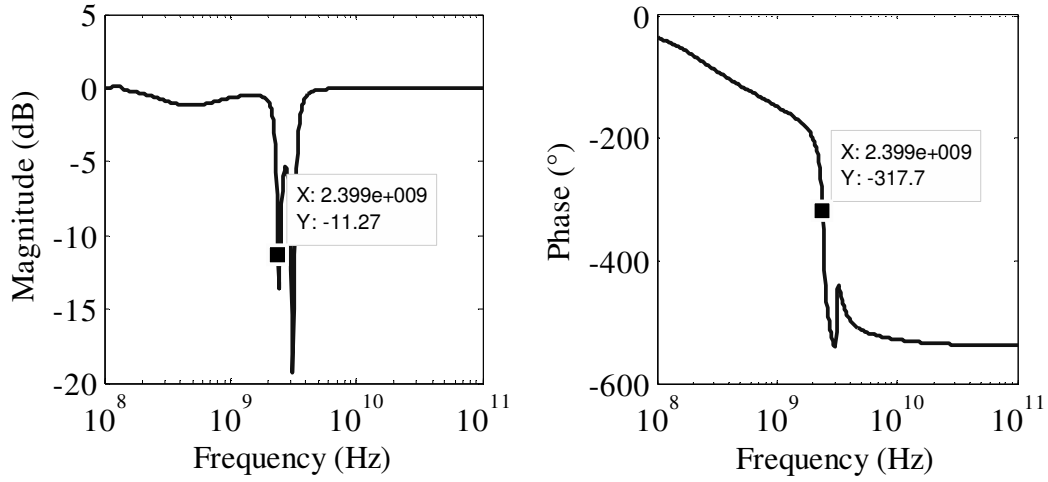


Figure 5.47. Output port voltage reflection coefficient (S_{22}) of the designed Class-E PA system.

5.5 FURTHER DESIGN OF THE CLASS-F AMPLIFIER

As in the case of Class-E amplifier, an active biasing network was designed to provide a bias of 0.8 V for the Class-F amplifier described in Section 5.3.4. An *S*-parameter based input impedance matching was implemented on this PA as well to match the assumed input source impedance of 50 Ω to the input port (base) of the PA. The schematic showing a complete PA, including biasing and input impedance matching, with matching inductors also implemented using spiral inductors, is shown in Figure 5.48. Again, all RFCs and decoupling capacitors were considered to be implemented off-chip.

Temperature sweep from -20 to 120 °C on the output voltage waveform is shown in Figure 5.49. From this figure, it is seen that there is no deterioration of the output voltage waveform (and therefore no gain decrease) as temperature increases and therefore emitter and/or base ballasting are not needed. The harmonic content of the same waveform at room temperature (27 °C) is shown in Figure 5.50. From this figure, the THD is only 0.59 %.

Also at room temperature, the PA draws 35 mA from a 1.5 V voltage supply, whilst exhibiting the output power of 5.3 mW, resulting in collector efficiency of 10.0 %. For 1 mW input power level, the PAE is 8.2 %.

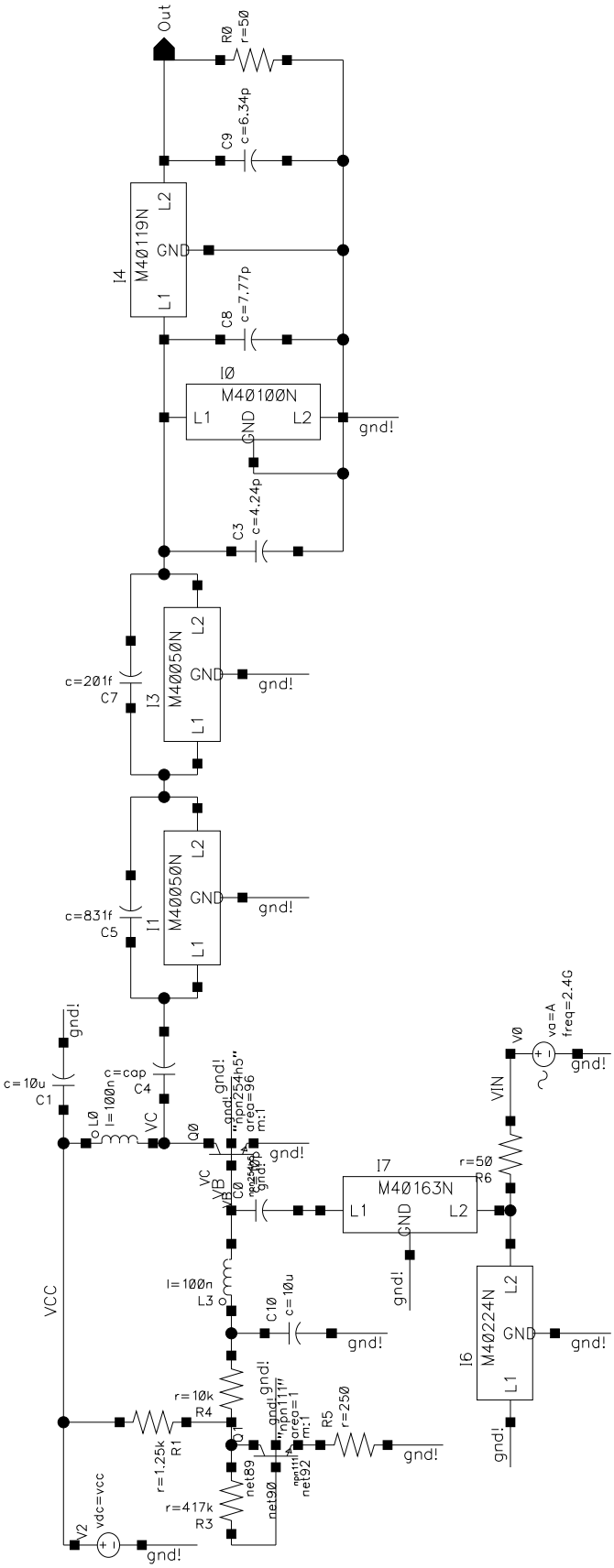


Figure 5.48. Designed Class-F PA with biasing and matching networks.

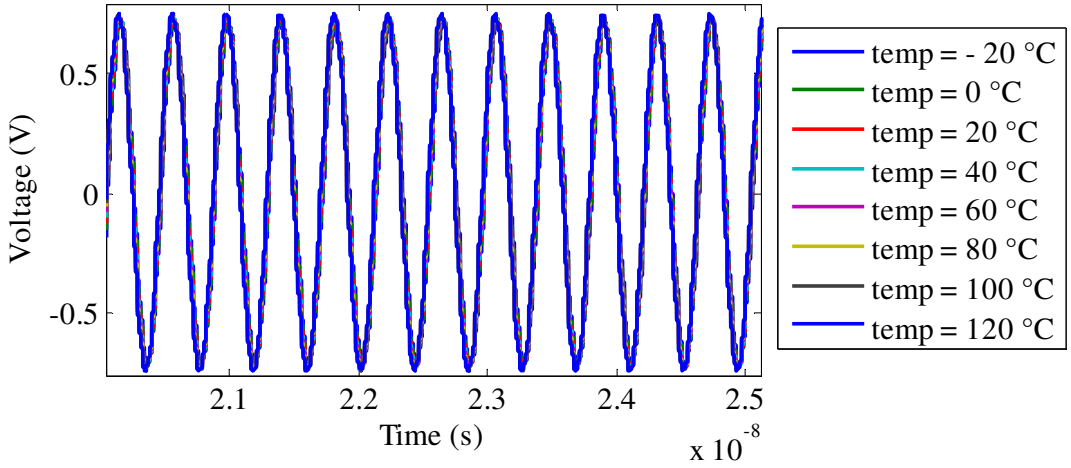


Figure 5.49. Temperature-swept output voltage waveform of the full Class-F PA.

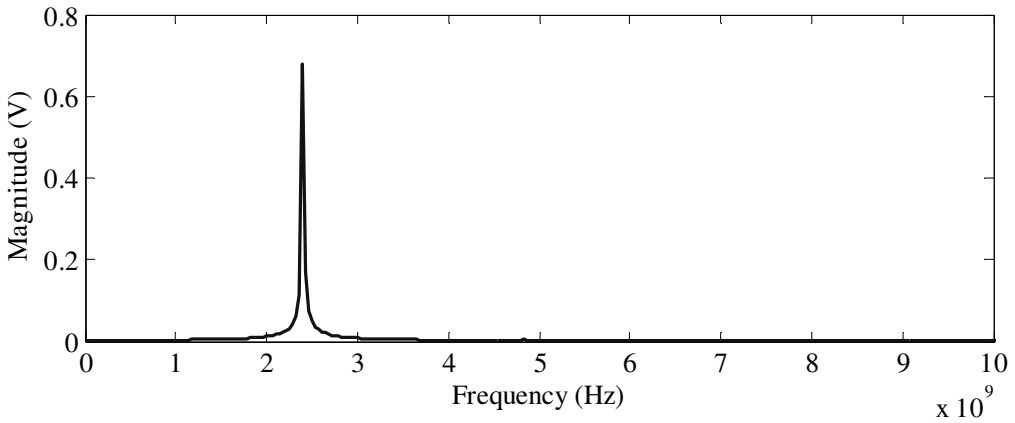


Figure 5.50. Harmonics of the output voltage waveform of the designed Class-F PA system.

The *S*-parameters of the PA modelled as a two port network are shown in Figure 5.51 to Figure 5.54 [110]. From these figures, it is evident that input and output ports of this PA are well matched, and that in the forward direction, the system acts as an amplifier, while in the reverse direction, the system acts as an attenuator, as expected.

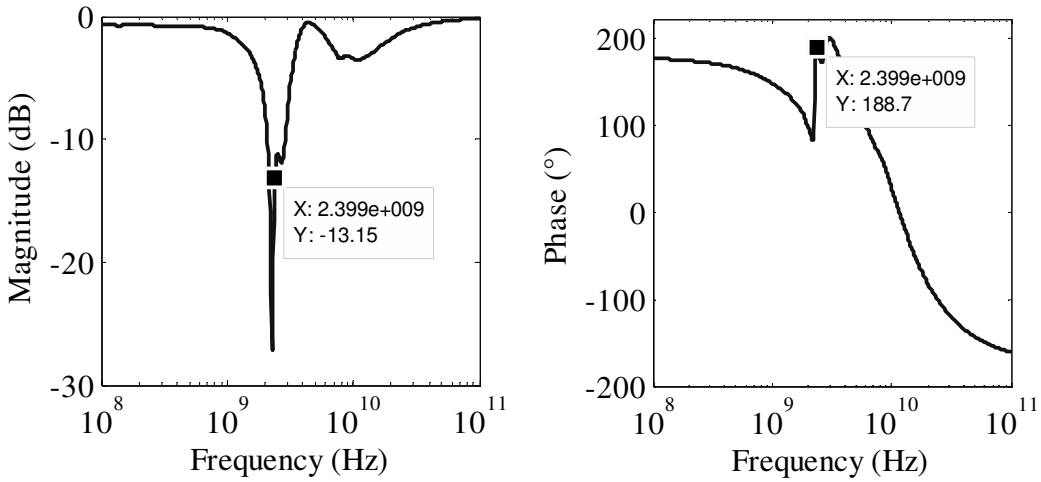


Figure 5.51. The input port voltage reflection coefficient (S_{11}) of the designed Class-F PA system.

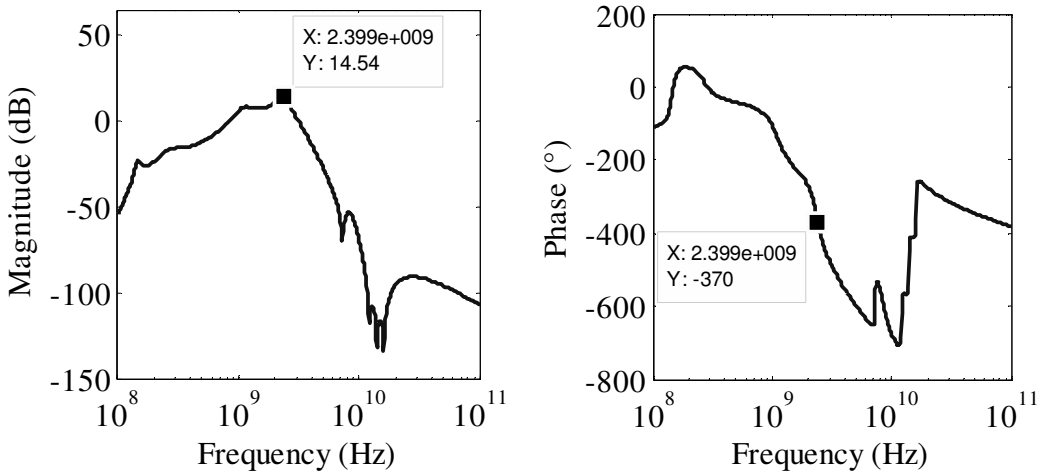


Figure 5.52. The forward voltage gain (S_{21}) of the designed Class-F PA system.

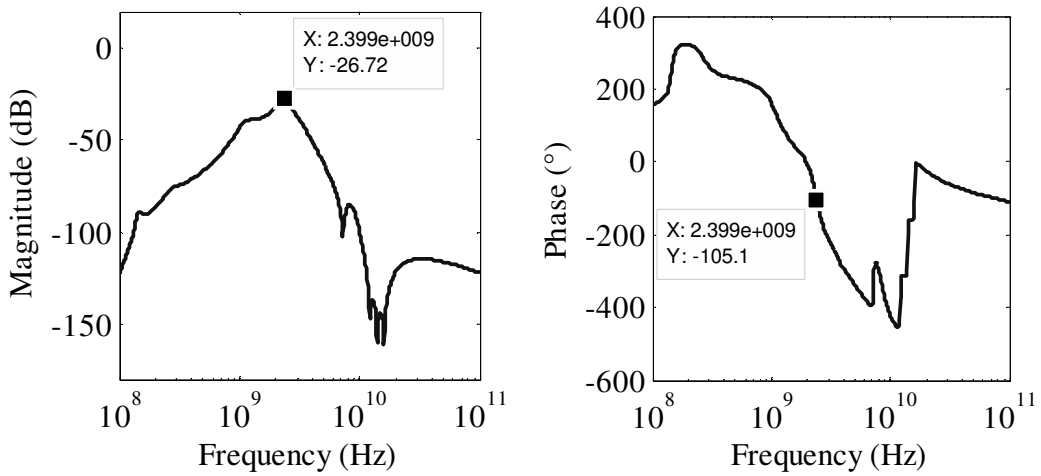


Figure 5.53. The reverse voltage gain (S_{12}) of the designed Class-F PA system.

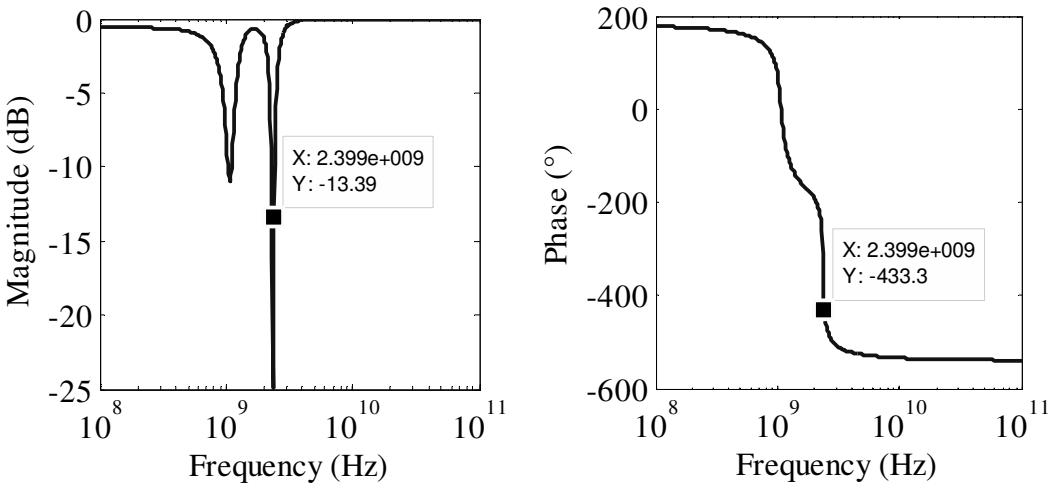


Figure 5.54. Output port voltage reflection coefficient (S_{22}) of the designed Class-F PA system.

5.6 CONCLUSION

In this chapter, the two integral parts of the system level routine for the design of PAs were shown. The inductor model and inductance search algorithm were verified by means of EM simulations. The model and EM simulation corresponded well and it has been established that spiral inductors can be used with monolithic PAs if their inductance and Q-factor are predicted by the inductance search algorithm. Furthermore, the streamlined use of the complete PA design routine was demonstrated by designing one Class-E and one Class-F output stage complete with input and output matching as well as biasing with minimum optimisation effort. While the results were short of the goal parameters of the two amplifiers, particularly the output power, the importance of the routine has been confirmed. Chapter 6 follows with measurement results.