CHAPTER 3 METHODOLOGY

3.1 INTRODUCTION

Chapter 2 provided a review of literature related to the topic of the thesis. This chapter describes methodology used for this research. It starts with the flow of the research process and continues with the description in some detail of the technologies used to simulate the key concepts and prototype the test chip. A part of the chapter deals with various software packages used in the course of the research, such as the software package for conceptual design, CAD packages for simulation and layout, measurement equipment, as well as the software package for algorithm development.

3.2 RESEARCH METHODOLOGY OUTLINE

Due to the fact that the concepts applied in developing a method for rapid PA design had to be transformed into circuits that can be simulated and tested, a major part of this research revolved around designing PAs and spiral inductors, which could be critically evaluated, simulated and finally prototyped.

Design and simulation of various PA stages in CAD tools described later in Section 3.5 ran in parallel with research and development of the set of algorithms for PA automation in MATLAB [16] (Section 3.4). Following successful simulations, a layout, essentially a blueprint for the IC prototype, was developed. The IC is to be used to characterise effects that cannot be characterized otherwise. This includes investigation of the influence of parasitics, which is particularly important for the RF circuits. Also, taking measurements of the fabricated IC presents a good way to get an insight into the quality of operation of on-chip spiral inductors.

Research methodology followed in this thesis is graphically represented by the flow diagram shown in Figure 3.1.

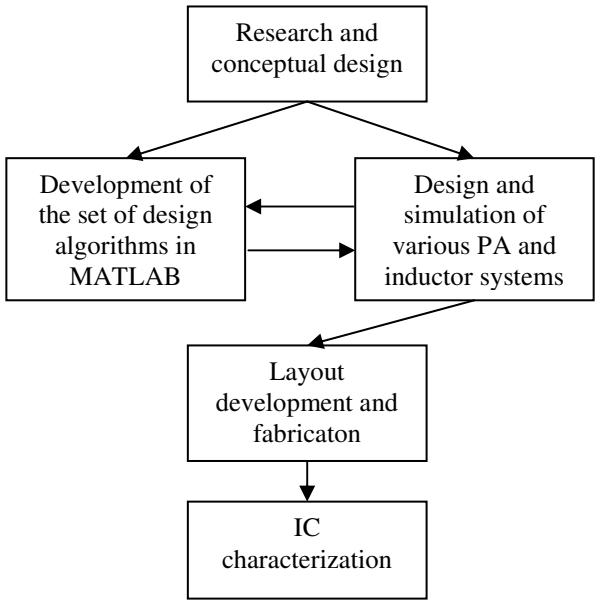


Figure 3.1. Research methodology followed in this thesis.

3.3 THE IC PROCESS

The IC process is significant because of the following reasons:

- All simulations are performed using the SPICE models particular to the IC process.
- Physical layout of the PA and inductor systems are drawn in conformity with the design rules specific to a particular IC process.
- Correct modelling of spiral inductors is process dependent, as described in Section 2.3.2. Spiral inductor part of the PA design routine must be able to interpret the IC process parameters in order to work correctly.

The main process chosen for this thesis is S35 0.35 µm SiGe BiCMOS process from AMS [13]. It is a SiGe BiCMOS process with NPN HBTs, PIP and MIM capacitors and several libraries of standard metal-3 (3M) and thick-metal (TM) spiral inductors. Exact process parameters cannot be disclosed in this thesis due to the non-disclosure agreement (NDA) signed between the author (via University of Pretoria) and AMS. Further process details can be found in [88-90], if available.

Measurements were essential for the works of this thesis. Fabrication of the IC was sponsored by Metal Oxide Semiconductor Implementation Service (MOSIS) [91] as a part of the MOSIS Education Programme (MEP). A grant for a multi-purpose wafer (MPW)

was given to the University of Pretoria. The technology node in which circuits needed to be completed was the 7WL 180 nm process from IBM [14]. Most important features of this process are similar to those of the AMS process except for differences, inter alia, in available capacitors and inductors, and the fact that design rules allow for smaller wire and polysilicon widths and spacing than for the AMS process. An NDA agreement was also signed with IBM; for full process parameters please refer to [92] if available.

3.4 CONCEPTUAL DESIGN AND ALGORITHM DEVELOPMENT

Complete conceptual design and mathematical modelling was done with the aid of MATLAB from Mathworks. This package is a programming language that supports a great number of mathematical functions, and it can be used to speed up tedious hand calculations.

The same package was used to design the first version of the PA design routine. Although this version did not have a graphical user interface (GUI) front-end for the algorithms, the ease of use of MATLAB programming language simplified debugging.

3.5 MODELLING, SIMULATION, AND LAYOUT DESIGN

Modelling and simulation of various PA circuits was performed in Cadence Virtuoso package from Cadence Design Systems. Several tools available in this package were used, and their names and functionality are given in Table 3.1.

Table 3.1. Tools of Cadence Virtuoso package and their functionality.

Tool name	Functionality
Virtuoso Schematic Composer	Schematic level circuit design [93]
Virtuoso Analog Design Environment (ADE) with Spectre and SpectreRF Circuit Simulator	SPICE based simulator [94-96]
Virtuoso Wavescan	Waveform viewer [97]
Virtuoso Layout Editor with Diva/Dracula/Assura DRC and LVS	Layout generation, design checks and layout versus schematic comparison [98]
Spiral Inductor Modeler	Electromagnetic (EM) simulation of spiral inductors [99]

3.5.1 Modelling and simulation

Modelling and simulation were done in Virtuoso Schematic Editor, ADE, Spectre and Spectre RF [93-96]. After being conceptually designed, whether using a design routine that was developed in parallel or otherwise, schematics of each test circuit was drawn in Virtuoso Schematic Editor by instantiating components that have been SPICE modelled and provided by AMS and connecting them by wires. Since pre-designed inductors

available from the vendor were not used here, custom inductor models were used to correctly model spiral inductors. ADE was used to export netlists of created designs, and run analogue (DC operating point, transient, frequency domain, RF) simulations on the exported SPICE netlists using Spectre and Spectre RF. The output of the simulation was then viewed in Wavescan waveform viewer [97] by graphing the resulting waveforms. The waveforms were used to interpret the simulation results.

3.5.2 Layout design and verification

Once satisfied with simulations, the layouts of various PAs were developed in Virtuoso Layout Editor [98]. At this level the transistors, capacitors, inductors and other devices were drawn in accordance with the design rules specified by the IBM process [92]. The design rules check (DRC) module is included here. The layout versus schematic (LVS) module served to investigate the correlation between the given schematic (created in Virtuoso Schematic Editor and simulated in ADE) and layout (created in Virtuoso Layout Editor). The purpose of the comparison was to detect design errors that might have occurred in the process of transforming the schematic into the layout.
Several test circuits were placed on one prototype package.

3.5.3 EM simulation

EM simulation was necessary for simulating spiral inductors. It was done in Virtuoso Spiral Inductor Modeler [99]. The solver for the Spiral Inductor Modeler employs Partial Element Equivalent Circuit (PEEC) algorithm in the generation of macromodels for the spiral components. Electro-static and magneto-static EM solvers are invoked separately to extract the capacitive and inductive parameters of the spiral inductor structure. A process file with information on metal and dielectric layers was required by the modeller and it needed to be manually created.

3.5.4 SPICE model of the HBT

PA simulation, described in Section 3.5.1, is only as accurate as the SPICE model of the transistor used in this simulation.

For the PAs simulated in AMS S35 process, an HBT was used. Traditionally, the Gummel-Poon model was the most popular model for the design of bipolar circuits for a considerable period of time [100]. However, an RF SPICE model, Vertical Bipolar Inter-

Company (VBIC) model for the HBT, available from AMS and accurate up to frequencies of 20 GHz [89], offers several improvements over Gummel-Poon model (particulars of which cannot be disclosed here due to the NDA mentioned earlier). The model used for HBT transistors in IBM 7WL process was also a VBIC model [101].

3.6 MEASUREMENT SETUP AND EQUIPMENT

S-parameters of the fabricated ICs were measured by means of the R&S ZVA 40 Vector Network Analyzer from Rohde and Schwarz [102]. This network analyzer, pictured in Figure 3.2 is capable of measuring two-port parameters up to 40 GHz which is sufficient for the research in this thesis.

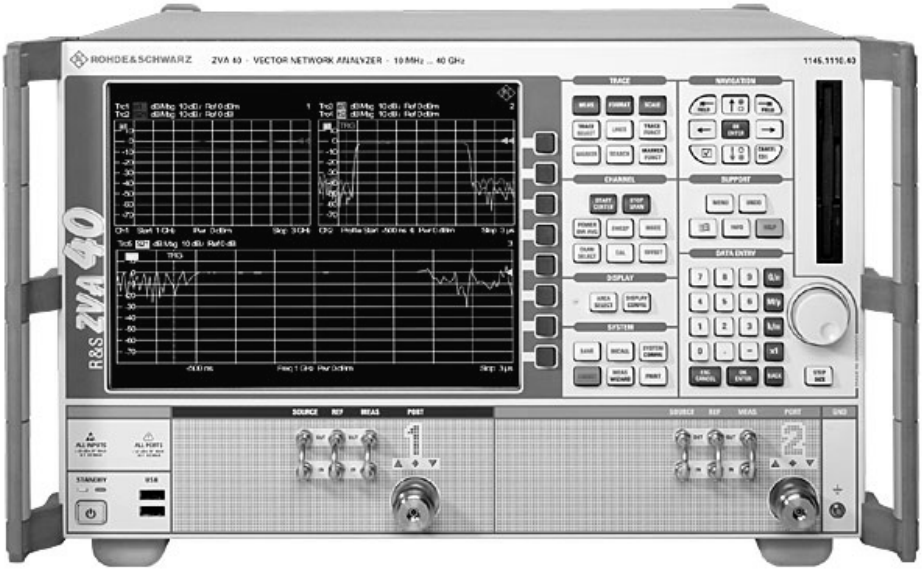


Figure 3.2. R&S ZVA Vector Network Analyzer [102].

3.7 CONCLUSION

Chapter 3 described the design approach to be applied to this thesis. An overview of the design methodology used to complete the research has been given. This was followed by the discussion of the two IC fabrication processes, where simulations were performed in AMS S35 process, and layouts for several good PA configurations were drawn in IBM 7WL process. A description of MATLAB, the tool used for mathematical modelling and algorithm development was given, followed by the presentation of CAD tools (part of Cadence Virtuoso package) to emphasize and justify the need for their use. VBIC model for HBT used for SPICE simulations was described as well, since it was identified as the

model used in simulations for both AMS and IBM processes. Finally, the network analyzer, capable of measuring frequencies up to 40 GHz, was presented. Chapter 4 follows with the details on the system level design routine.

CHAPTER 4 SYSTEM LEVEL DESIGN ROUTINE

4.1 INTRODUCTION

In Chapter 3, the methodology used to carry out the research was described. In this chapter, concepts behind the MATLAB-routine based method for rapid PA design are addressed. The first part of the chapter deals with the method for designing of Class-E PAs. This is followed by a discussion on the method for designing of Class-F PAs. The proposed method for spiral inductor design is described after the discussion on PA design. This chapter also includes several other aspects of importance for this routine, viz. input and output matching as well as full integration of proposed spiral inductors into the complete PA system. The complete MATLAB listings for all developed sub-routines are given in Appendix A.

4.2 METHOD FOR DESIGNING THE CLASS-E POWER AMPLIFIERS

In this section, a novel, routine-based method for designing the Class-E PAs is proposed. It is partially based on equations from the classic paper by Sokal and Sokal [39] (as described in Section 2.2.5.2), but it has been adapted for use in integrated circuits with HBTs. Basic principle of this routine is, however, technology independent.

The PA from Figure 2.9 has been used for this method and is repeated in Figure 4.1 for convenience.

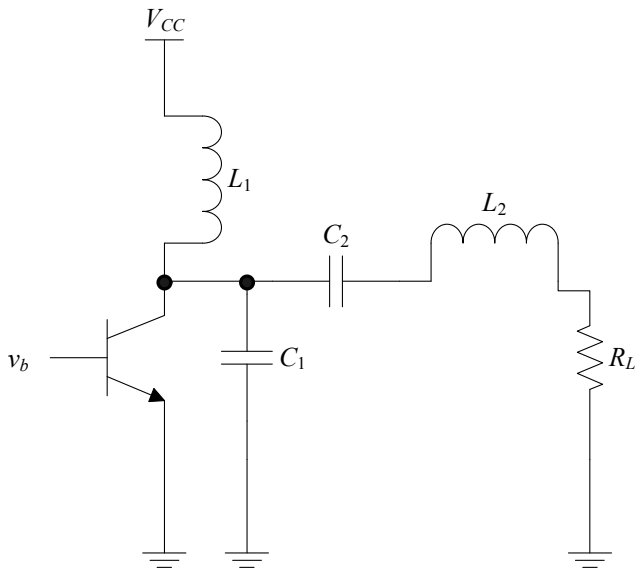


Figure 4.1. Circuit diagram of a single ended Class-E PA [37].

4.2.1 Input parameters

Several parameters are needed as the inputs of the Class-E subroutine:

- *Centre frequency of the channel (f_o).* This quantity, specified in megahertz, is determined by the specifications of the transmitter system the PA is a part of.
- *The loaded quality factor (Q_L).* This is the quality factor of the series resonator created by inductance L_2 and capacitance C_2. It can be chosen freely by the PA designer, but a trade-off must be considered which exists between high efficiency and power (low Q_L) on one side, and total harmonic distortion (THD) of the output signal on the other side (high Q_L). Plausible Q factor is in the range of 5 to 10 [37]. If efficiency is important, a lower Q_L can be chosen and harmonics removed by additional filters at the output of the amplifier [39]. The narrowband output matching network, described in Section 4.4, can serve for this purpose.
- *Output power (P_{out}).* This quantity, specified in miliwatts, is also determined by specifications of the transmitter system. A higher output power is achieved with a lower load resistance (R_L), which places more stringent requirements for the output impedance matching. High output power can also result in the need for a higher supply voltage.
- *Supply voltage (V_{CC}).* This quantity, specified in volts, can be chosen by the designer, but attention must be paid that it does not exceed the value of $BV_{CEO}/3.56$

(see Equation (4.2)), where BV_{CEO} is defined in **Error! Reference source not found.** as collector-emitter breakdown voltage.

Some optional parameters can be specified:

- *Collector-emitter saturation voltage (V_{CEsat}).* This parameter, also specified in volts, is a process-dependent quantity, usually equal to 0.1 or 0.2 V. Since it is approximately equal to 0, its omission will result in minimal discrepancies between the actual and predicted PA values.
- *Maximum and minimum inductance values (L_{max} and L_{min}).* These two quantities, specified in nanohenries, can be included by the designer to limit extremely high or low values of inductors.
- *Collector-emitter breakdown voltage (BV_{CE}).* This quantity, specified in volts, warns the user if the V_{CC} specified is high enough to result in transistor entering breakdown.

Parameters needed for the Class-E PA subroutine are summarized in Table 4.1.

Table 4.1. Input parameters required for the Class-E PA software routine.

Parameter	Unit	Mandatory / Optional
Centre frequency of the channel (f_o)	MHz	Mandatory
Loaded quality factor (Q_L)	-	Mandatory
Output power (P_{out})	mW	Mandatory
Supply voltage (V_{CC})	V	Mandatory
Collector-emitter saturation voltage (V_{CEsat})	V	Optional
Maximum and minimum inductance values (L_{max} and L_{min})	nH	Optional
Collector-emitter breakdown voltage (BV_{CE})	V	Optional

4.2.2 Subroutine outputs

The following quantities are outputs of the Class-E software subroutine:

1. Optimum load resistance, R_L (Ω);
2. Shunt capacitor, C_1 (pF);
3. Series capacitor, C_2 (pF) and series inductor, L_2 (nH);
4. Feed inductor, L_1 (RFC);
5. Shunt capacitor, C_p (pF);
6. DC and maximum currents, I_{DC} and i_{max} (mA);
7. Maximum collector voltage, v_{max} (V); and
8. Loaded quality factor, Q_L, which places inductances within the maximum and minimum values.

4.2.3 Description and flow diagram of the Class-E subroutine

This subroutine is carried out in a linear fashion. It utilizes Equations (2.16) through (2.19) to calculate R_L, L_2, C_2 and C_1. The DC current is calculated by [30]

$$I_{DC} = \frac{V_{CC}}{1.734R_L} \tag{4.1}$$

The maximum transistor voltage and current are given by

$$v_{max} = 3.56V_{CC} \tag{4.2}$$

and

$$i_{max} = 2.86I_{DC} \tag{4.3}$$

The capacitor C_1 must include the output capacitance of the transistor used for amplification.

Flow diagram of the Class-E design subroutine is given in Figure 4.2. Complete MATLAB code listing for the subroutine is given in Figure A.3 and Figure A.4.

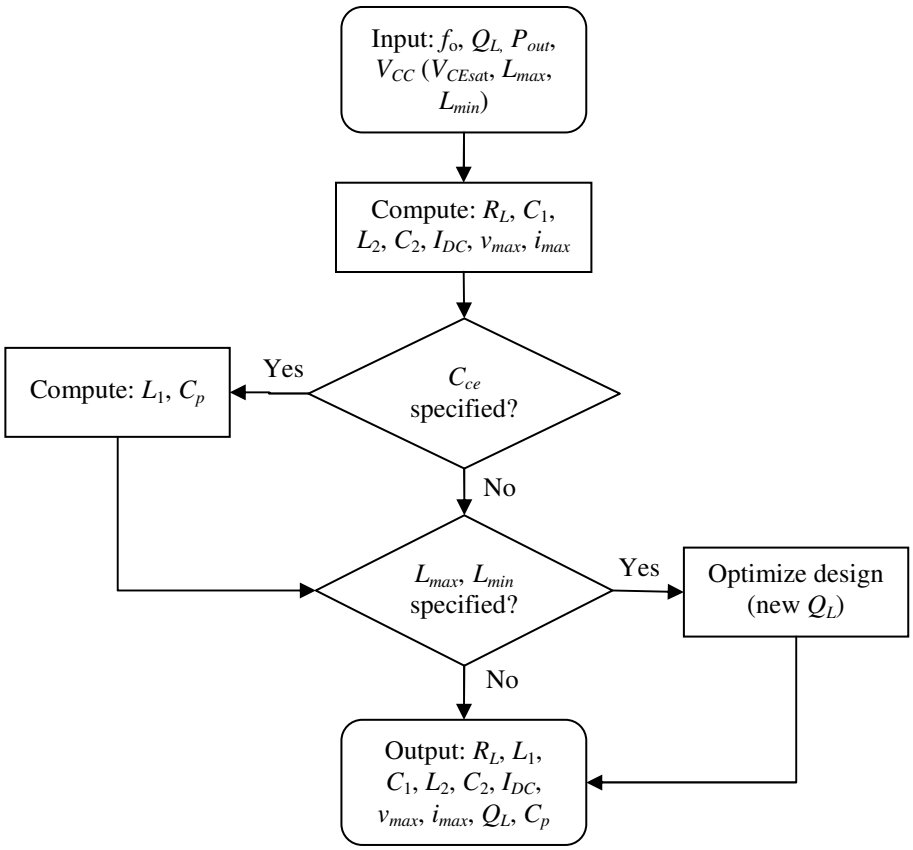


Figure 4.2. Flow diagram of the Class-E PA design subroutine.

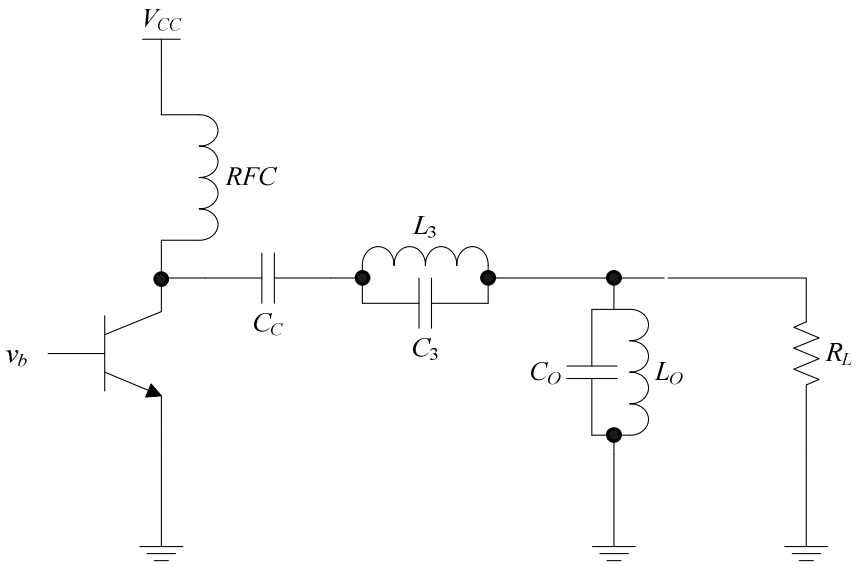
4.3 METHOD FOR DESIGNING THE CLASS-F POWER AMPLIFIERS

This section extends the concepts of the routine-based method for designing the Class-E PAs from the previous section onto the design of the Class-F PAs. In Section 2.2.5.3 it was discussed that the efficiency of integrated Class-F PAs depends on the number of harmonic resonators used. In this section, a method for designing two different Class-F PA configurations are discussed: the third-harmonic peaking Class-F circuit (shown in Figure 2.13 and repeated in Figure 4.3(a) for convenience) and Class-F PA with resonators up to the fifth harmonic (Figure 4.3(b)). Theoretical efficiencies for the two circuits are 81.7% and 90.5% respectively [43]. The former is included because of its particularly simple output filter, whilst the latter is included because it can deliver relatively high efficiency while still keeping the output filter reasonably simple. Including a greater number of resonators further increases the complexity of the circuit and is not deemed feasible here.

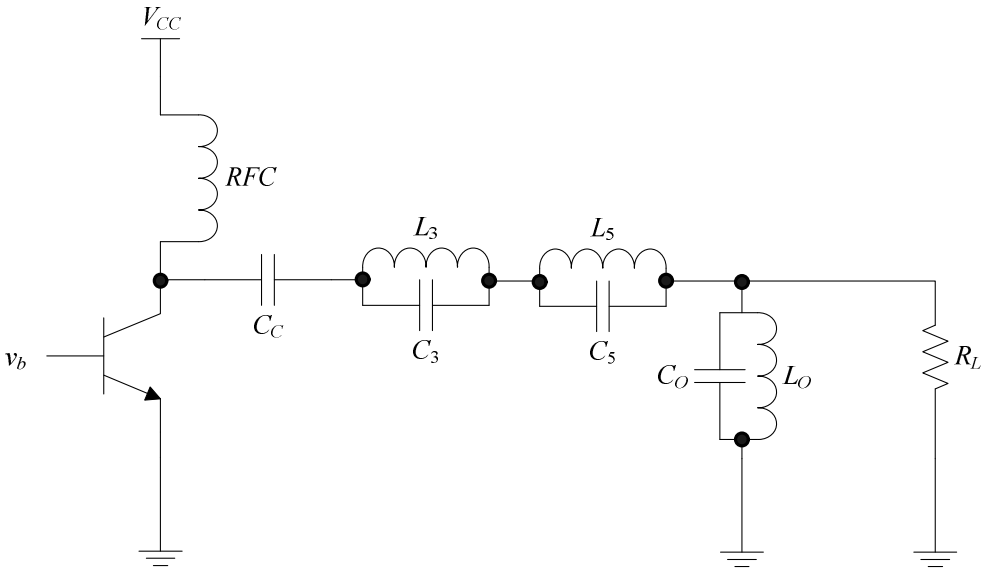
4.3.1 Input parameters

As in the case of the Class-E design, several input parameters are needed for the Class-F subroutine to complete successfully:

- *Centre frequency of the channel (f_o).* Again, this is determined by the specifications of the transmitter system of which the PA is a part. It is specified in megahertz.
- *Output power (P_{out}).* This quantity, similar to the one in the Class-E part of the routine, is specified in miliwatts and is also determined by the specifications of transmitter system.
- *Supply voltage (V_{CC}).* This quantity, specified in volts, can be chosen by the designer, but attention must be paid that the value of BV_{CEO}/δ_V (see Equation (4.8)) is not exceeded.
- *Inductance values for nominal resonant tank (L_O), third-harmonic resonant tank (L_3) and fifth-harmonic resonant tank (L_5).* In case of Class-F PA, there is no trade-off between the filtering inductance values to some other quantity, and these values can be chosen freely. Resonant capacitors are calculated based on the corresponding inductance values. Fifth-harmonic resonant tank inductor is only needed if the fifth-harmonic resonator is used.



(a)



(b)

Figure 4.3. Class-F PA circuits: (a) third-harmonic peaking circuit and (b) circuit with resonators up to the fifth harmonic.

- *Collector-emitter breakdown voltage (BV_{CE}).* This quantity, specified in volts, is the only optional parameter and it is used in order for the program to warn the user if V_{CC} specified is high enough to send the transistor into breakdown.

Parameters needed for the Class-E PA part of the routine are summarized in Table 4.2.

Table 4.2. Input parameters required for the Class-F PA software routine.

Parameter	Unit	Mandatory / Optional
Centre frequency of the channel (f_O)	MHz	Mandatory
Output power (P_{out})	mW	Mandatory
Supply voltage (V_{CC})	V	Mandatory
Filtering inductances (L_0, L_3 and L_5)	nH	Mandatory
Collector-emitter breakdown voltage (BV_{CE})	V	Optional

4.3.2 Subroutine outputs

The following quantities are outputs of the Class-F software subroutine:

1. Optimum load resistance, R_L (Ω);
2. Nominal frequency resonant capacitor, C_O (pF);
3. Third- and fifth-harmonic frequency resonant capacitors, C_3 and C_5 (pF);
4. DC current, peak collector current and output peak current, I_{DC}, i_{Cm} and I_{om} (mA); and
5. Peak collector voltage and peak output voltage, v_{Cm} (V) and V_{om} (V).

4.3.3 Description and flow diagram of the Class-F subroutine

In the case of the Class-F subroutine, voltage and current coefficients are needed in order to shape current and voltage waveforms to deliver maximum power and efficiency to the load, as discussed in Section 2.2.5.3. All required coefficients are tabulated in Table 4.3 for the two Class-F PA configurations.

Table 4.3. Maximum-efficiency waveform coefficients [43].

Coefficient	Value (Resonators up to third-harmonic)	Values (Resonators up to fifth-harmonic)
γ_V	1.1547	1.2071
δ_V	2	2
γ_I	1.4142	1.5
δ_I	2.1863	3

Similarly to the case of the Class-E PA, design is performed for the optimum load resistance [43]:

$$R_L = \frac{\gamma_V{}^2 V_{CC}{}^2}{2P_{out}} \tag{4.4}$$

DC current needed for correct waveform shaping is given by

$$I_{DC} = \frac{\gamma_V V_{CC}}{\gamma_I R_L} \tag{4.5}$$

Maximum output voltage and current can be calculated by Equations (2.22) and (2.23) from Section 2.2.5.3. Peaks of the collector voltage and current waveforms are given by

$$v_{Cm} = \delta_V V_{CC} \tag{4.6}$$

and

$$i_{Cm} = \delta_I I_{DC} \tag{4.7}$$

Resonant capacitors (C_O, C_3 and C_5) can be calculated by once again manipulating Equation (2.14):

$$C_i = \frac{1}{(2\pi f)^2 L_i}, \tag{4.8}$$

where $i = O$, 3 or 5.

Flow diagram of the Class-F PA design subroutine is given in Figure 4.4. Complete MATLAB code listing for the routine is given in Figure A.5 and Figure A.6.

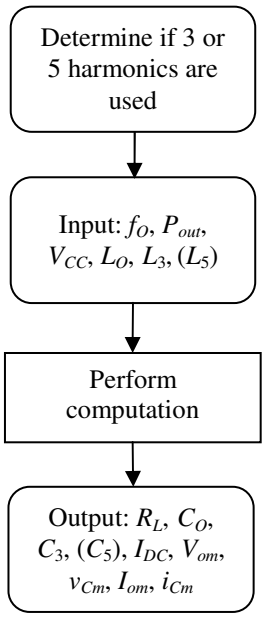


Figure 4.4. Flow diagram of the Class-F PA design subroutine.

4.4 METHOD FOR OUTPUT MATCHING

Output matching for a PA was discussed in Section 2.2.4. The PA design routine utilizes both wideband and narrowband matching, and choice of output network depends on the specific application.

4.4.1 Input parameters

The following input parameters are needed for the output matching part of the routine to complete successfully:

- *Source impedance of the matching network (R_S).* This impedance is equivalent to the optimum load resistance of the PA and it is specified in ohms.
- *Load impedance of the matching network (R_L).* This impedance is equivalent to the impedance of the antenna. It is specified in ohms and it is usually equal to 50 Ω.
- *Centre frequency of the matching network (f_O).* In PA applications, this is the centre frequency of the channel. The matching network will only be operating correctly at the centre frequency. This quantity is specified in megahertz.
- *Bandwidth of the matching network (B).* This parameter, also specified in megahertz, is needed for narrowband matching networks (T and Π networks).

Since most antennas have 50 Ω impedances, the load impedance can be assumed known and it should be specified only if it differs from the default value.

4.4.2 Subroutine outputs

Inductance (L_i) and capacitance (C_i) parameters of five different matching networks, where i = 1 or 2, are the outputs of this part of the PA design routine. These matching networks are shown in Figure 4.5(a)-(e) [33].

4.4.3 Description of the matching network subroutine

The matching network subroutine executes in linear fashion, using a predetermined set of equations.

4.4.3.1 High-pass L network

The high pass L network is shown in Figure 4.5(a). The matching inductor L_1 is determined by [33]

$$L_1 = \frac{1}{2\pi f_O}\sqrt{\frac{R_S{}^2 R_L}{R_L - R_S}} \tag{4.9}$$

and the matching capacitor is determined by

$$C_1 = \frac{1}{2\pi f_O}\left(\frac{R_L{}^2 + (2\pi f_O L_1)^2}{R_L(2\pi f_O L_1)}\right) \tag{4.10}$$

4.4.3.2 T networks

Calculations for T networks of Figure 4.5(a) and (c) are based on the method described in [103]. Using this method, two L networks separated by virtual resistance R_V are designed, as shown in Figure 4.6. In this figure, X_{S1} and X_{P1} are reactances of the first L network, and X_{S2} and X_{P2} are reactances of the second L network. The two L networks are then combined into a single T network by removing the virtual resistance.

The virtual resistance is found from

$$R_V = R_{small}(Q^2 + 1)\,, \tag{4.11}$$

where R_{small} = min(R_S, R_L), and $Q = f_O/B$ is the Q-factor of the matching network. Series reactance X_{S1} is then

$$X_{S1} = QR_S \tag{4.12}$$

and parallel reactance X_{P1} is

$$X_{P1} = \frac{R_V}{Q} \tag{4.13}$$

For the second L network, a separate Q-factor needs to be calculated:

$$Q_2 = \sqrt{\frac{R_V}{R_L} - 1} \tag{4.14}$$

and X_{S2} and X_{P2} are then

$$X_{S2} = Q_2 R_L \tag{4.15}$$

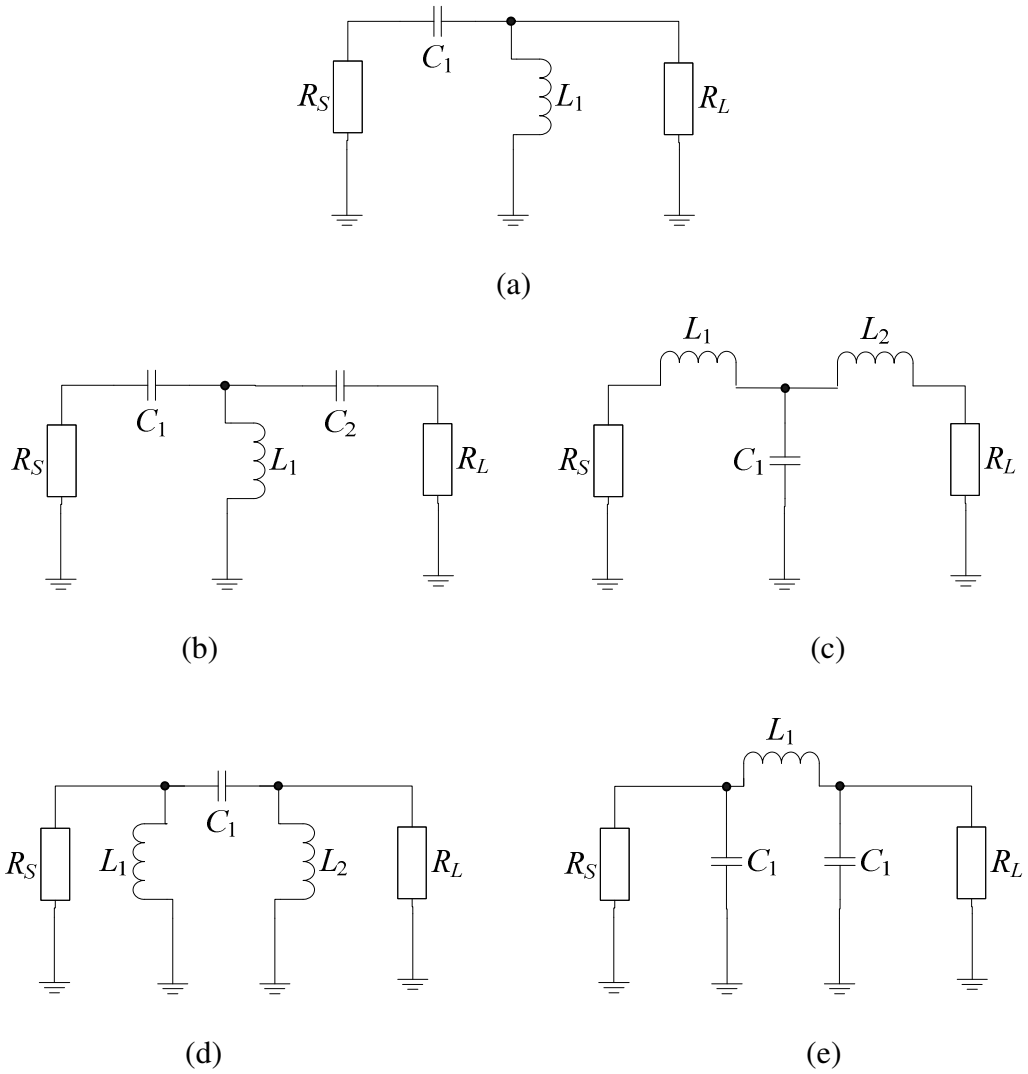


Figure 4.5. Five matching networks that are output of the matching network PA design subroutine: (a) wideband high-pass L network, (b) narrowband capacitor-inductor-capacitor T network, (c) narrowband inductor-capacitor-inductor T network, (d) narrowband inductor-capacitor-inductor Π network and (e) narrowband capacitor-inductor-capacitor Π network.

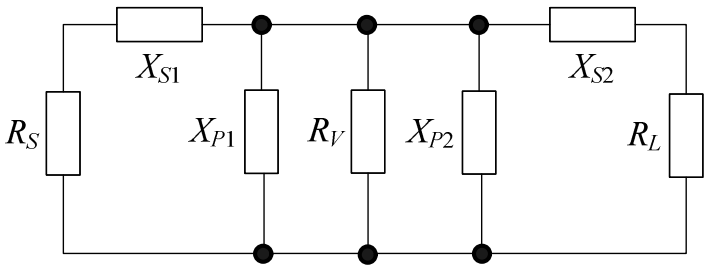


Figure 4.6. Two L networks separated by virtual resistance forming a T network.

and

$$X_{P2} = \frac{R_V}{Q_2} \tag{4.16}$$

After all the reactances have been calculated, virtual resistance is removed and X_{P1} and X_{P2} are combined in parallel to get final reactance X_P:

$$X_P = \frac{X_{P1} X_{P2}}{X_{P1} + X_{P2}} \tag{4.17}$$

Definitions for reactances of capacitors and inductors can be used to obtain actual values of inductors and capacitors needed:

$$L_i = \frac{X_{Li}}{2\pi f} \tag{4.18}$$

and

$$C_i = \frac{1}{2\pi f X_{Ci}}, \tag{4.19}$$

where L_i and C_i are inductors and capacitors in the matching network.

4.4.3.3 Π networks

Similar procedure can be applied to the Π networks Figure 4.5(d) and (e), with the difference that in this case serial reactances X_{S1} and X_{S2}, instead of parallel reactances X_{P1} and X_{P2}, are separated by a virtual resistor. Virtual resistance is given by

$$R_V = \frac{R_{high}}{Q^2 + 1}, \tag{4.20}$$

where $R_{high} = \max(X_S, X_L)$. X_{S2} and X_{P2} are then

$$X_{S2} = QR_V \tag{4.21}$$

and

$$X_{P2} = \frac{R_L}{Q} \tag{4.22}$$

Q-factor of the first L network is

$$Q_1 = \sqrt{\frac{R_S}{R_V} - 1} \tag{4.23}$$

and X_{S1} and X_{P1} are then

$$X_{S1} = Q_1 R_V \tag{4.24}$$

and

$$X_{P1} = \frac{R_P}{Q_1} \tag{4.25}$$

After all reactances have been calculated and virtual resistance removed, X_{S1} and X_{S2} are simply added, and inductors and capacitors are obtained from Equations (4.18) and (4.19).

Complete code listing for this part of the routine is given Figure A.31.

4.5 METHOD FOR DESIGNING SPIRAL INDUCTORS

As discussed in Chapter 2, the inductor is the most important passive component of any PA. Spiral integrated inductor presents a viable option for practical implementations of PAs designed with the aid of the PA design routine described in this chapter. This is because of the deterministic models that can be used to accurately predict the inductance value and Q-factors of any inductive structure on chip, given the process parameters and geometry of that inductive structure. However, an iterative procedure is used in practice, where one "guesses" inductor geometry that will result in an inductor with the performance close to the performance needed for a good power amplification (as illustrated in the flowchart in Figure 2.33). In this section, an improvement to the iterative procedure is proposed. A new non-iterative routine can find an inductor of the specified value, with the highest possible Q-factor, occupying a limited area, and using predetermined technology layers.

Concepts are developed for the single square spiral inductor of Figure 2.27 (a). The drawing of this geometry is repeated in Figure 4.7 for convenience.

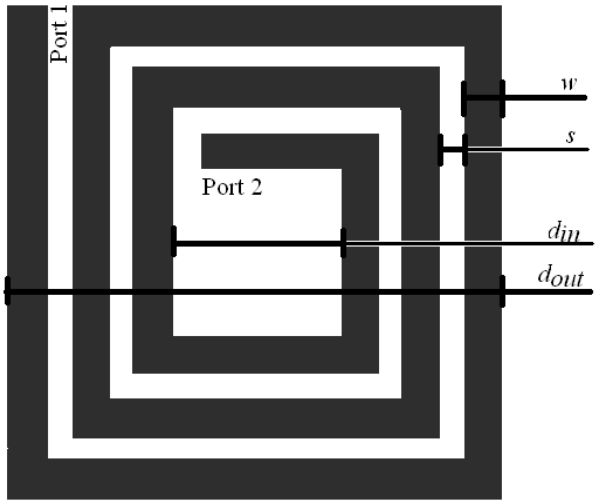


Figure 4.7. Integrated square spiral inductor.

4.5.1 Input parameters

The main idea behind this routine is to synthesize the square inductor geometry resulting in the highest Q-factor for specified inductance given some design constraints. Alternatively, inductances and Q-factor values of various square inductors can be calculated if the geometry parameters of such inductors are given.

For accurate inductor modelling, two sets of parameters are needed: geometry and process parameters, together with the frequency of operation of the inductor. For the highest Q-factor, higher layers of the metal should be used for the inductor spiral. Other general guidelines for the inductor design from Section 2.3.2.6 should be followed where possible.

Three subsections that follow give a detailed description of parameters needed for the spiral inductor design.

4.5.1.1 Geometry parameters

If the geometry of a device is specified and the inductance and Q-factor are to be determined (analysis), the following input geometry parameters are necessary:

- Outer diameter, d_{out} (μm);
- Inner diameter, d_{in} (μm);
- Turn width, w (μm); and
- Number of turns, n.

If the inductance is specified, and geometry resulting in the highest Q-factor is required (synthesis), only constraints for the geometry should be specified (all in micrometer):

- Minimum value of inner diameter, $d_{in(min)}$;
- Maximum value of outer diameter, $d_{out(max)}$;
- Minimum value for turn spacing, s_{min}; and
- Minimum turn width, w_{min}.

In the latter case, tolerance (in percentage) for the acceptable inductance values, as well as grid resolution (in micrometer), are needed for successful program completion.

Table 4.4 summarizes the geometry input parameters.

Table 4.4. Geometry parameters for the spiral inductor design.

Parameter	Units	Geometry / inductance known
Outer diameter (d_{out})	µm	Geometry
Inner diameter (d_{in})	µm	Geometry
Turn width (w)	µm	Geometry
Number of turns (n)	-	Geometry
Minimum value of the inner diameter	µm	Inductance
Maximum value of the outer diameter	µm	Inductance
Minimum value for turn spacing (s)	µm	Inductance
Minimum turn width	µm	Inductance
Inductance value tolerance	%	Inductance
Grid resolution	µm	Inductance

4.5.1.2 Process parameters

The inductance value of a high-Q structure is predominantly determined by its geometry. However, the silicon substrate introduces process-dependent parasitics, which are dependent on process parameters. They decrease the Q-factor and add shift to the inductance value. The following substrate parameters need to be specified:

- Thickness of the metal in which the inductor spiral is laid out, t (nm);
- Resistivity of the metal used for the spiral, ρ (Ω·m);
- Permeability of the metal used for the spiral, μ (H/m);
- Thickness of the oxide between the two top metals, t_m (nm);
- Relative permittivity of the oxide between the two top metals, ε_{rm};
- Thickness of the oxide between the substrate and the top metal, t_{sm} (nm);
- Relative permittivity of the oxide between the substrate and the top metal, ε_{rs};
- Thickness of the silicon substrate, t_{Si} (µm);

- Relative permittivity of the silicon substrate, ε_{rSi}; and
- Resistivity of the silicon substrate, ρ_{Si} (Ω·m).

The process parameters are summarized in Table 4.5. AMS S35 process parameters are used later in Chapter 5 for verification by means of simulations.

Table 4.5. Process parameters for the spiral inductor design.

Parameter	Unit
Thickness of metal in which the inductor spiral is laid out	nm
Resistivity of metal used for the spiral (ρ)	Ω·m
Permeability of metal used for the spiral (μ)	H/m
Thickness of oxide between the two top metals (t_m)	nm
Relative permittivity of oxide between the two top metals (ε_{rm})	-
Thickness of oxide between substrate and top metal (t_{sm})	nm
Relative permittivity of oxide between substrate and top metal (ε_{rm})	-
Thickness of the silicon substrate (t_{Si})	µm
Relative permittivity of the silicon substrate (ε_{rSi})	-
Resistivity of the silicon substrate (ρ_{Si})	Ω·m

4.5.1.3 Operating frequency (f_O)

If the inductor is a part of a PA design (this does not need to be the case), the operating frequency is usually the centre frequency of the channel. In other scenarios, operating frequency can be understood as the frequency at which the Q-factor will be highest for a particular geometry.

4.5.2 Subroutine outputs

The inductor design subroutine has both numerical outputs and outputs in the form of text and data files.

4.5.2.1 Numerical outputs

The following quantities are numerical outputs of the inductor design software subroutine:

1. Effective inductance value of the inductor at the operating frequency, L_S (nH);
2. Nominal inductance value of the inductor ($Q \rightarrow \infty$), L_{inf} (nH);
3. Q-factor of the inductor at the operating frequency, Q;
4. Resonant frequency of the inductor, f_r (GHz);
5. Width of the spiral (µm);
6. Spacing between the turns of the spiral (µm);
7. Input diameter of the spiral (µm);
8. Output diameter of the spiral (µm); and

9. Number of turns of the spiral.

4.5.2.2 Text and data file outputs

If required, this subroutine can export the netlist and layout of the designed inductor structure.

The SPICE netlist of the inductor structure, complete with the inductance value and parasititcs calculated for a single-π inductor model, as described in Section 4.5.3 that follows, is saved with a .spc extension. It can be used in SPICE simulations without the need for one to draw the schematic of the inductor with its parasitics in the schematic editor. The netlist is exported in T-Spice format, recognised by most simulators including Cadence Virtuoso.

Layout of the inductor can be exported into Caltech intermediate form (CIF) file or graphic data system (GDS) II file. Both formats contain mask geometry information of the inductor [104, 105]. The GDS II format is the stream format and it is more popular of the two. The stream file is saved with a .gds extension. The CIF file is a text based and it is saved with a .cif extension. Either of the files can be imported into layout software to eliminate the need for one to draw any inductor layout structures.

4.5.3 Description and flow diagrams of inductor design subroutine

The inductor design subroutine consists of two parts. The first part calculates inductance for a given geometry, whereas the second finds geometry that gives the highest Q-factor for a specified inductance.

The first part of the subroutine is a set of calculations that utilizes equations for the single-π inductor model (Section 2.3.2.3). Nominal inductance is calculated by means of the data-fitted monomial equation as specified by Equation (2.32), where coefficients are specified in Table 2.4. Parasitics are calculated utilizing Equations (2.33 – 2.43). Q-factor and resonance frequency are calculated with Equations (2.44 – 2.47). The resulting inductance can be calculated from [89]

$$L_{eff} = \frac{\mathrm{Im}(Z)}{2\pi f_o}, \tag{4.28}$$

where Z is the total impedance of the single-π modelled inductor with its one port grounded.

The second part is a search algorithm that looks into a range of possible geometries and identifies geometry that will result in the required inductance within certain tolerance. While more than one geometry will result in the correct inductance at a given frequency, but each of these geometries will have a different Q-factor. The geometry that gives the highest Q-factor is chosen by the algorithm as its output. The same set of equations (Equations (2.32 – 2.47), (4.28)) is used in the search algorithm. Accuracy of the algorithm depends on the tolerance for the required inductance values and on the search grid resolution. Higher tolerance of the inductance value will result in less accurate inductance values, but there will be a greater probability that inductor geometry resulting in the particular inductance will be found with lower grid resolution. This probability can be increased by increasing the grid resolution, but with the increased grid resolution, the time of execution and memory requirements of the search algorithm will also increase. It is up to users to decide which combination of inductance tolerance and grid resolution will be appropriate for a specific application.

The flow diagram of the inductor design software subroutine is given in Figure 4.8. The search algorithm used to find the geometry when inductance is specified is given in Figure 4.9 [106, 107]. The complete MATLAB code listing for this subroutine, with reference to algorithms for netlist, CIF and GDS file extraction, are given in Figure A.25.

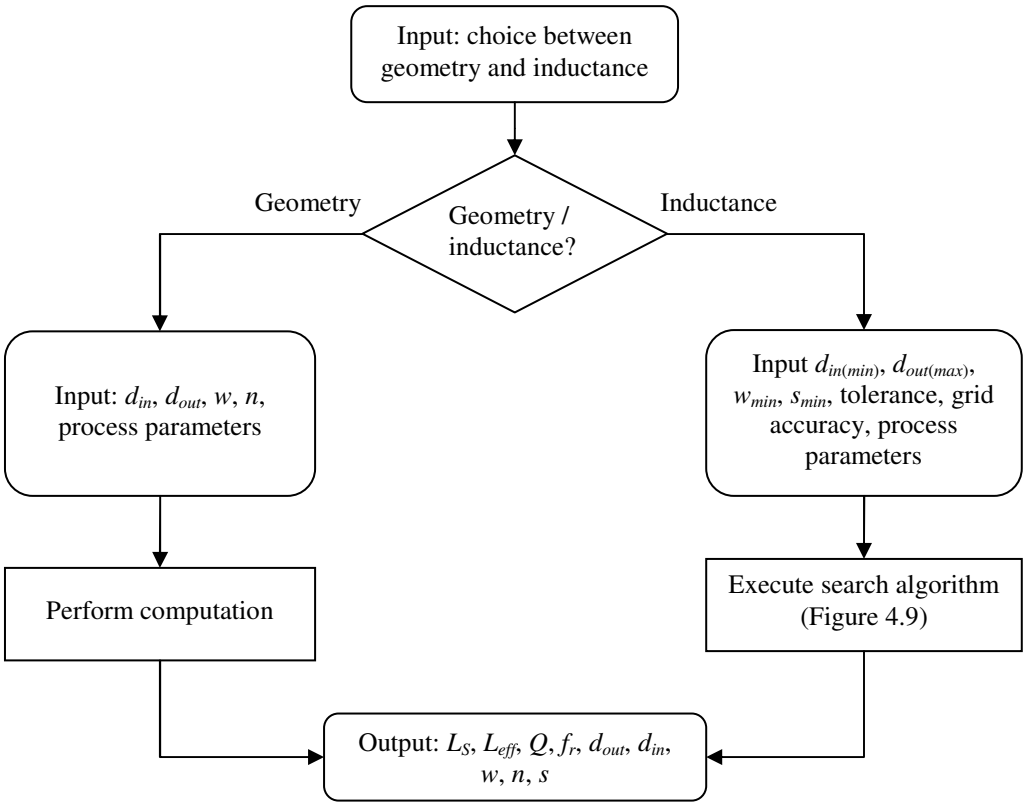


Figure 4.8. Flow diagram of the inductor design subroutine.

4.6 MATCHING AND BIASING AT THE INPUT SIDE OF THE POWER AMPLIFIER

Driving HBTs at large signal levels applicable to PAs present a challenge for performing input impedance matching, because its input impedance behaviour at different power levels and other operating conditions is highly nonlinear [30]. Therefore, the design of the input matching network only becomes possible after extensive simulations have been performed on a specific PA configuration designed with the use of the routine. Various simulations can be used to predict the input impedance and its behaviour under likely operating conditions, and this information can be used in the design of the input matching network. In certain cases, it may even be possible to omit the input matching, if the output impedance of the preceding amplifier stage itself presents a good match.

If large-signal *S*-parameters of the output stage can be found, then method involving two-port networks described in [108] can be utilized to find the input impedance of the stage. Figure 4.9 shows an amplifier as a two-port network. With reference to this figure, reflection coefficient as seen looking towards load is

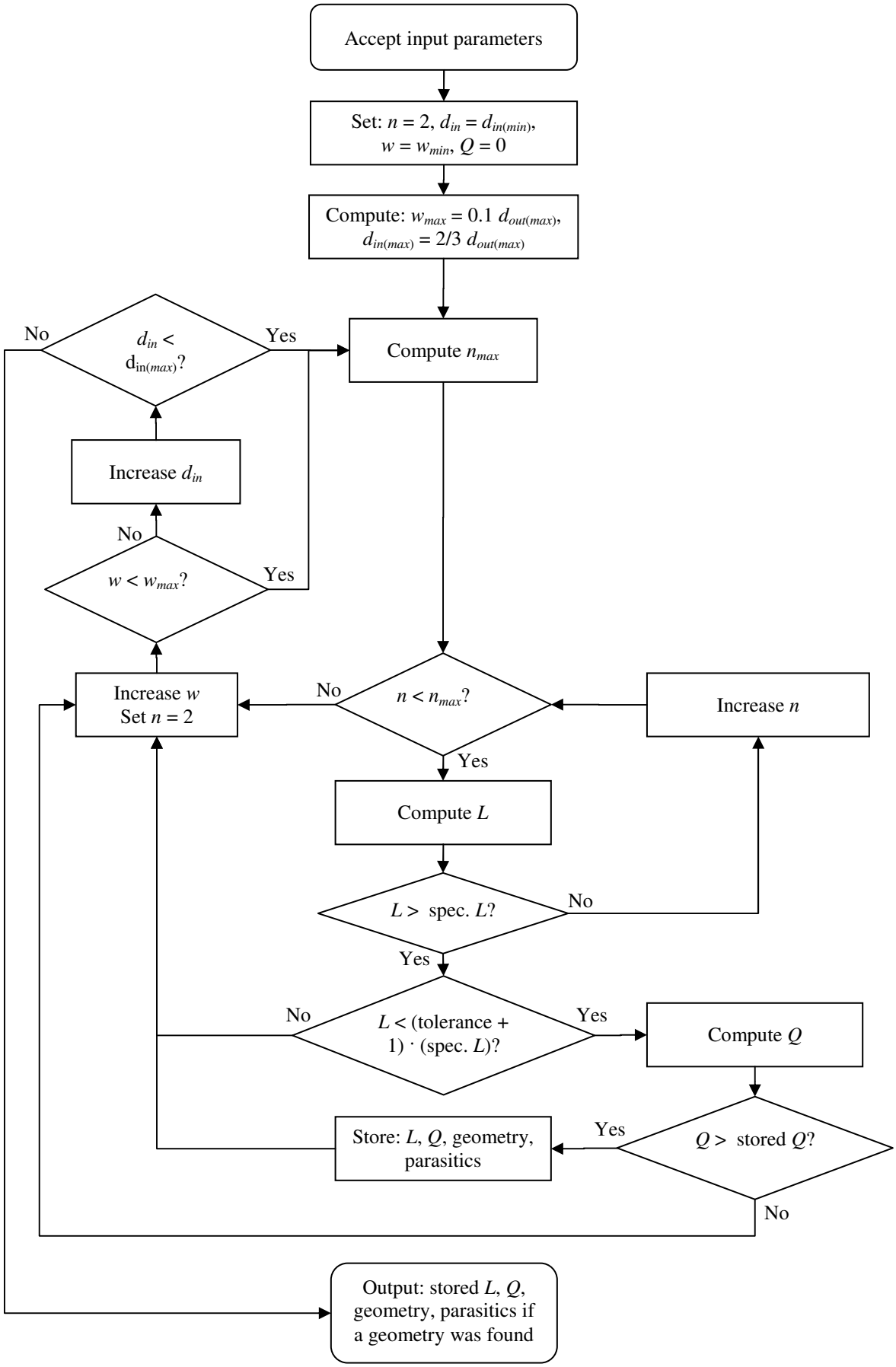


Figure 4.9. Flow diagram of the inductance search algorithm.

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{4.27}$$

where Z_L is the impedance of the load and Z_0 is the characteristic impedance reference used when obtaining the *S*-parameters. Input reflection coefficient of the amplifier in terms of *S*-parameters is

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.28}$$

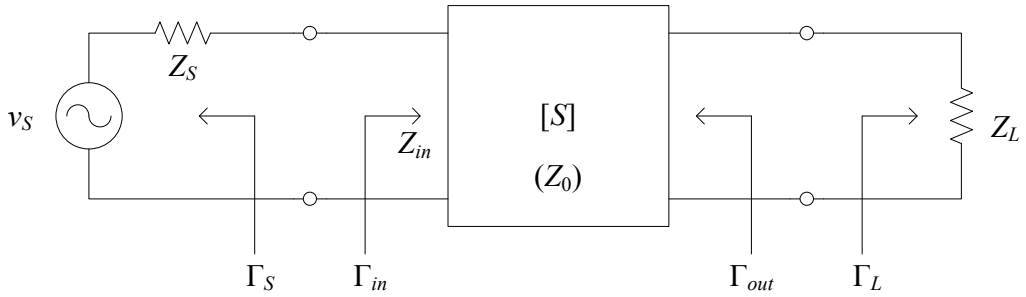


Figure 4.9. A two-port network with the source and load reflection coefficients [108].

For perfect matching at the output amplifier (which will generally be the case) with $Z_0 = Z_L$, Γ_{in} will be equal to S_{11}. Finally,

$$Z_{in} = Z_0 \frac{1 + \Gamma_{in}}{1 - \Gamma_{in}} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{4.29}$$

Matching networks described in Section 4.4.3 can be used to perform the matching. Reactance of Z_{in} is handled either by absorbing it into the matching network, or by resonating it out with equal and opposite reactance [103]. Finally, after the matching is performed, the stability of the amplifier should be ensured [108].

Challenges similar to the ones that arise when doing input impedance matching can be seen with trying to achieve biasing at the input of the PA. It is difficult to predict the exact optimum quiescent point for a PA analytically, so it is found by means of simulations. The DC level of the input drive signal is swept in the region that is identified to contain the optimum bias point, and the correct value is identified. Only once the optimum quiescent point is found, an active or passive biasing network can be utilized.

4.7 COMPLETE SYSTEM INTEGRATION

Methods for designing different PA blocks described in Sections 4.2 to 4.5 are combined into one stand-alone routine [109-111]. This routine can be used to perform the complete Class-E or Class-F stage design, including the output impedance matching and design of all inductors needed in the PA. Quantities, such as operating frequency, needed for more than one sub-routine, are only entered once, which is a distinct advantage of using one complete routine for the design instead of using each of the subroutines separately. Output quantities are displayed sequentially, and they combine most of the separate methods.

4.7.1 Input parameters

All input parameters of the complete routine are summarized in Table 4.6. This table also includes the section number in which the detailed description of each parameter is given.

Table 4.6. Summary of input parameters for the complete PA design routine.

Parameter	Unit	Mandatory / Optional	Section
Centre frequency of the channel (f_o)	MHz	Mandatory	4.2.1, 4.3.1, 4.4.1, 4.5.1.3
Loaded quality factor (Q_L)	-	Mandatory (Class E)	4.2.1
Output power (P_{out})	mW	Mandatory	4.2.1, 4.3.1
Supply voltage (V_{CC})	V	Mandatory	4.2.1, 4.3.1
Collector-emitter saturation voltage (V_{CEsat})	V	Optional (Class E)	4.2.1
Maximum and minimum inductance values (L_{max} and L_{min})	nH	Optional (Class E)	4.2.1
Collector-emitter breakdown voltage (B_{VCE})	V	Optional	4.2.1, 4.3.1
Filtering inductances (L_0, L_3 and L_5)	nH	Mandatory (Class F)	4.3.1
Bandwidth of the matching network (B)	MHz	Mandatory	4.4.1
Minimum value of the inner diameter	µm	Mandatory	4.5.1.1
Maximum value of the outer diameter	µm	Mandatory	4.5.1.1
Minimum value for turn spacing	µm	Mandatory	4.5.1.1
Minimum turn width	µm	Mandatory	4.5.1.1
Inductance value tolerance	%	Mandatory	4.5.1.1
Grid resolution	µm	Mandatory	4.5.1.1
Thickness of metal in which the inductor spiral is laid out	nm	Mandatory	4.5.1.2
Resistivity of metal used for the spiral (ρ)	Ω·m	Mandatory	4.5.1.2
Permeability of metal used for the spiral (μ)	H/m	Mandatory	4.5.1.2
Thickness of oxide between the two top metals (t_m)	nm	Mandatory	4.5.1.2
Relative permittivity of oxide between the two top metals (ε_{rm})	-	Mandatory	4.5.1.2
Thickness of oxide between the substrate and the top metal (t_{sm})	nm	Mandatory	4.5.1.2
Relative permittivity of oxide between the substrate and the top metal (ε_{rm})	-	Mandatory	4.5.1.2
Thickness of the silicon substrate (t_{Si})	µm	Mandatory	4.5.1.2
Relative permittivity of the silicon substrate (ε_{rSi})	-	Mandatory	4.5.1.2
Resistivity of the silicon substrate (ρ_{Si})	Ω·m	Mandatory	4.5.1.2

4.7.2 Routine outputs

Output parameters combine most of the output parameters calculated by separate subroutines. They are summarized in Table 4.7. As in the case of input parameters, the

number of the section in which the parameter is described is also included in the table. For each inductor required by the PA, all relevant inductance parameters are also displayed.

4.7.3 Description and flow diagram of the PA design routine

At the beginning of the execution of the routine, users can chose to perform the design of either a Class-E or a Class-F PA. Depending on the choice, either the Class-E subroutine, described in Section 4.2, or Class-F, described in Section 4.3 is executed. Following this, the users have a choice to perform the output impedance matching to a standard impedance by invoking a subroutine described in Section 4.4. After this, users can choose to design spiral inductors for all inductors (including matching inductors), needed for full PA design. Both 3-metal and thick-metal inductors are designed for each inductor, allowing users to choose the geometry they consider better for a particular application. The inductor search algorithm described in Section 4.5 is used for the inductor design. CIF and GDS II files are not exported here because of a large amount of inductors designed. If needed, the inductor design subroutine can be invoked separately in order to export these files. However, the user is left with the choice to export the netlist of the complete PA system. The netlist includes the matching network and the subcircuits for all spiral inductors, provided that options for impedance matching and spiral inductor design have been selected.

Execution of the complete PA routine is summarized graphically in the flow chart in Figure 4.11. The MATLAB code listing or the main routine invoking all subroutines is given in Figure A.1.

Table 4.7. Output parameters of the PA design routine.

Parameter	Unit	Remark	Section
Optimum load resistance (R_L)	Ω	-	4.2.2, 4.3.2
DC current (I_{DC})	mA	-	4.2.2, 4.3.2
Maximum current (I_{max})	mA	-	4.2.2, 4.3.2
Maximum collector voltage (V_{max})	V	-	4.2.2, 4.3.2
Shunt capacitor (C_1)	pF	Class E	4.2.2
Series capacitor (C_2)	pF	Class E	4.2.2
Inductor (L_2)	nH	Class E	4.2.2
Feed inductor (L_1)	nH or RFC	Class E (Optional)	4.2.2
Shunt capacitor (C_p)	pF	Class E (Optional)	4.2.2
Loaded quality factor which will place inductances within the maximum and minimum values (Q_L)	-	Class E (Optional)	4.2.2
Nominal frequency resonant capacitor (C_0)	pF	Class F	4.3.2
Third-harmonic frequency resonant capacitor (C_3)	pF	Class F	4.3.2
Fifth-harmonic frequency resonant capacitor (C_5)	pF	Class F (Optional)	4.3.2
Output peak current (I_{om})	mA	Class F	4.3.2
Peak output voltage (V_{om})	V	Class F	4.3.2
Matching network inductors and capacitors	nH or pF	L, T and Π networks	4.4.2
Effective inductance value of inductor at operating frequency (L_S)	nH	For each inductor	4.5.2.1
Nominal inductance value of the inductor (L_{inf})	nH	For each inductor	4.5.2.1
Q-factor of the inductor at the operating frequency (Q)	-	For each inductor	4.5.2.1
Resonant frequency of the inductor (f_r)	GHz	For each inductor	4.5.2.1
Width of the spiral	mm	For each inductor	4.5.2.1
Spacing between the turns of the spiral	mm	For each inductor	4.5.2.1
Input diameter of the spiral	mm	For each inductor	4.5.2.1
Output diameter of the spiral	mm	For each inductor	4.5.2.1
Number of turns of the spiral	-	For each inductor	4.5.2.1

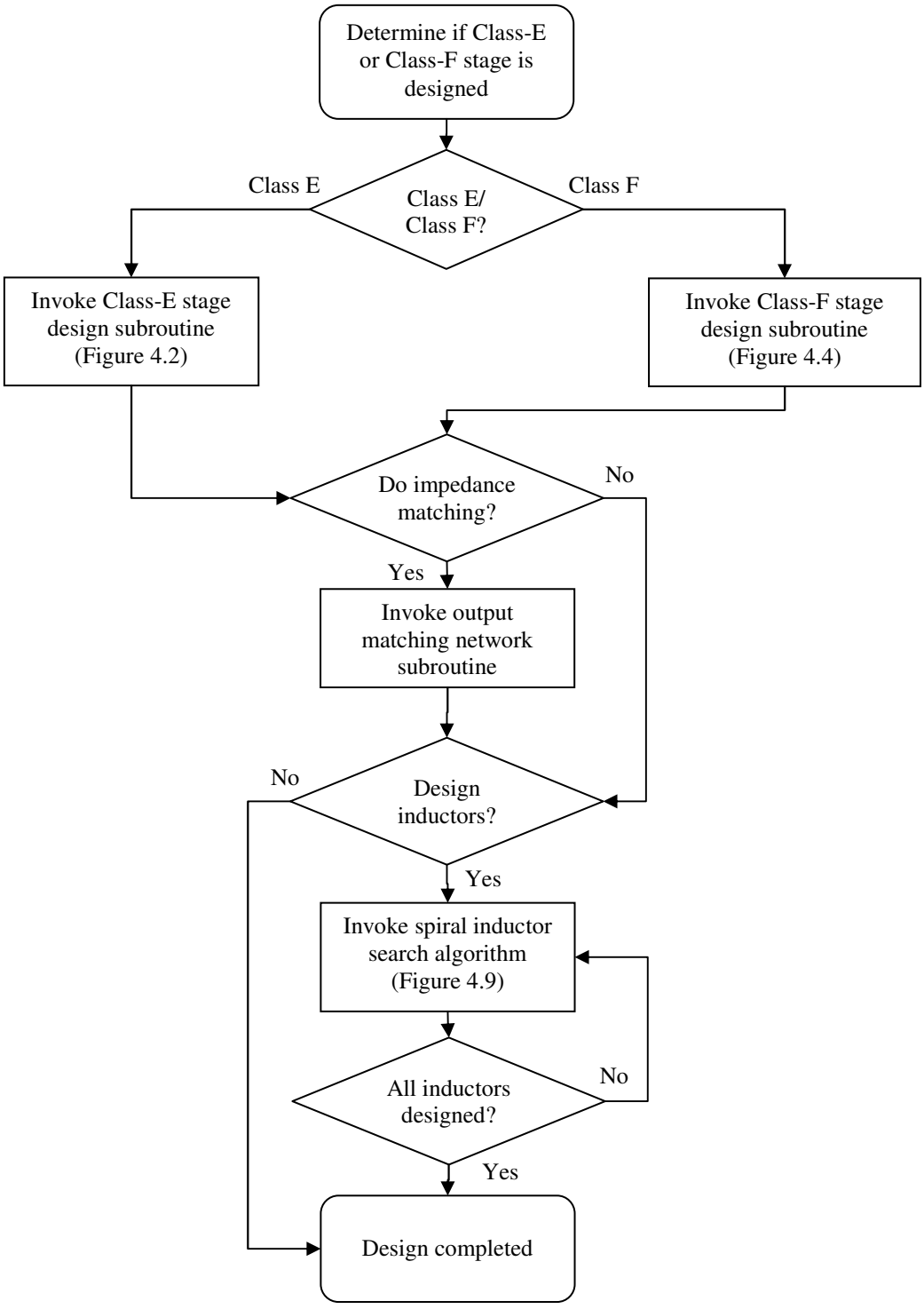


Figure 4.11. Flow chart of the complete PA design routine.

4.8 CONCLUSION

In this chapter, various design methods constituting the PA system level design routine were described. The Class-E and Class-F output stage design subroutines were identified as the starting point in the design of a complete PA system. The output impedance

matching integrated well with the output stage method, and the user could chose between a broadband L-matching network, and narrowband T or Π-matching networks. The search algorithm for spiral inductors was presented as a way to integrate inductors with quality factors as optimal as possible into the PA output stage and the output matching network. For completeness, a separate conventional subroutine that calculates inductance of any square inductor geometry was also revisited in this chapter. Inductor design subroutines were accompanied by SPICE netlist and mask geometry information (CIF and GDS II files) extractors. It has also been discussed that input impedance matching and biasing are not covered by the system level design routine, because of the highly nonlinear and nondeterministic input impedance characteristic of the PA. As an alternative, a method for impedance matching involving *S*-parameter simulation of the complete PA system (excluding input matching and biasing) was proposed and described. Simulation was suggested as a good starting point for the design of the biasing network for the PA as well. In Chapter 5, the design routine developed in this chapter will be used to design several PA systems.