

CHAPTER 1 INTRODUCTION

1.1 BACKGROUND TO THE RESEARCH

In the recent mobile telecommunication history, a number of wireless modulation schemes have found commercial use. Transmitter devices employing these schemes all demand a power amplifier (PA) for their successful operation. Figure 1.1 shows the PA as a part of a simple telecommunication system [1]. Bulky and high-power off-the-shelf component-based PAs are being replaced by radio-frequency (RF) integrated circuit (RFIC) PAs [2], operating from low-voltage power supplies [3]. This trend is evident in a wide spectrum of analogue and digital applications, starting from short distance (cordless phones, Bluetooth, wireless local area networks (WLANs)), to medium (RF identification (RFID)) and long distance applications (cellular phones, third generation (3G) devices) [4]. The PA remains a bottleneck in the full integration of wireless transceivers, especially if integration is done in pure silicon complementary metal-oxide semiconductor (CMOS) processes. For this reason, most commercial wireless devices use an external PA to drive an antenna. This external device is usually fabricated in technologies superior to the silicon (Si) CMOS, such as gallium-arsenide (GaAs) heterojunction bipolar transistor (HBT) technology [5].

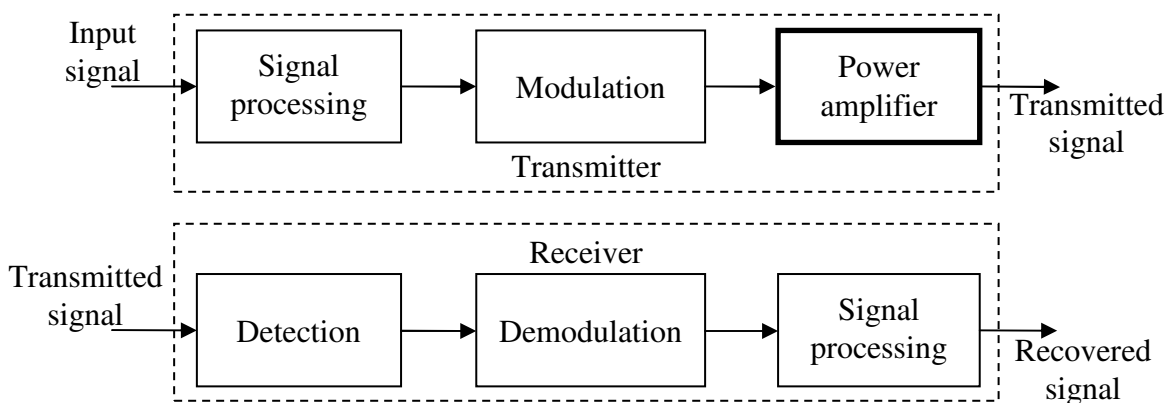


Figure 1.1. PA as a part of a simple telecommunication system [1].

Nevertheless, it is not always possible to separate a PA from the rest of the system, so that designers often have to be satisfied with a simple PA design in a pure CMOS process, or alternatively, a hybrid processes such as silicon-germanium (SiGe) bipolar-CMOS (BiCMOS) process [6].

In many RF modulation schemes, such as the direct sequence spread spectrum (DSSS) technique, it is necessary to design several PAs in order to ensure operation over different channels of the same band. For example, for a system based on DSSS [7], transmission is possible over a number of channels in Industrial, Scientific and Medical (ISM) band; their centre frequencies ranging from 2.4000 GHz to 2.4835 GHz. If a correct design methodology is not employed, designing of all PAs for all channels can be quite time consuming.

Basic PA is designed around one or more active devices, either metal-oxide semiconductor field-effect transistors (MOSFETs), bipolar junction transistors (BJTs) or HBTs. Several PA output stages are commonly used in telecommunications, with Class E and Class F widely used [8].

Irrespective of the output stage, and additional to the active devices, a number of passive components (inductors and capacitors) must be included. At the schematic design level this does not present a problem, because ideal capacitors and inductors can be used for the first design. However, translating of the design onto the layout level (where layout refers to actual drawing of components on a silicon wafer) becomes more intricate. Here, designing of an inductor poses a special problem, because of a great number of inductor options [9].

Even with a proper integrated inductor topology selected, the more affordable electronic design automation (EDA) software packages do not have built-in procedures for integrated inductor netlist extraction, but designers have to rely on inductors, if any, provided in High Performance Interface Tool Kits (HIT-kits). Furthermore, the built-in netlist extractors usually interpret an inductor as simply a long piece of metal or wire (which short-circuits the nodes placed at the two ends of an inductor), thus making the extracted netlists incorrect. Although there are a few models of integrated inductors described in literature [10-12], they are often not used by designers who are either satisfied by simulations at the schematic level or replace actual inductors with ideal inductors in order to proceed with the post-layout simulations. Drawbacks of such an approach might not be apparent at low frequencies, but they become particularly important in the design of PAs at RF, due to the fact that even small differences between actual and designed values of inductance can strongly affect the centre frequency, gain or efficiency of the amplifier. Often, these

mismatches can only be seen after the fabrication of the chip is completed, thus introducing additional unnecessary chip fabrication iterations.

1.2 RESEARCH PROBLEM AND HYPOTHESIS

In the description in Section 1.1, the following research problem can be identified:

What kind of methodology can be employed to speed up the design of power amplifiers together with their passives (inductors) for a range of wireless applications, at the same time taking care that high quality of amplification is maintained?

To answer the research question, the following hypothesis is formulated:

If the performance of a power amplifier system is related to optimising its subsystems, then implementing a methodology that uses software algorithms to perform the optimization will produce better quality power amplifiers.

To test the hypothesis, various PA and inductor options were investigated and those of Class E, and Class F identified as most commonly used topologies in RF design, because of their predisposition for high efficiencies and high power. Inductors were modelled as monolithic spiral inductors. Equations describing the PA and inductor models were used as a starting point when developing a method that allows that for a given a set of specifications such as PA bandwidth, centre frequency and class of operation, the best possible PA is found and designed. It is speculated, inter alia, that this method can be coined as a software routine. The same routine determines a geometry of a spiral inductor that gives the highest possible Q (quality) factor, using process parameters for a particular process. In parallel with the development of the software routine, a number of PAs were designed in the SiGe S35 (0.35 μm BiCMOS) process from Austriamicrosystems (AMS) [13] and simulated in order to verify the correctness of developed algorithms. Finally, the layouts of designed systems were prepared and then sent for fabrication to an auxiliary process from IBM¹ (IBM 7WL) process [14], in order to investigate aspects that cannot be

¹ IBM is the short name for International Business Machines.

covered in simulations, such as influence of parasitics, as well as correctness of the quality factor and inductance values of spiral inductors.

1.3 JUSTIFICATION FOR THE RESEARCH

Computer-aided design (CAD) is not uncommon in circuit design. Conceptual design is usually performed in a mathematical package, which can be followed by schematic design in a schematic editor. Performance of the circuit is normally simulated in SPICE² [15] based simulators. However, there are often various missing links, and the designer needs to resort to hand design to complete the design cycle. Being a common example of this problem, the design of PAs leaves an opportunity for a software routine to be developed that will aid this task.

1.4 METHODOLOGY

Various PA concepts were explored in depth to identify a few commonly used simple PA models to be used as a starting point for automating a PA design. A number of PAs based on these models were designed from the first principles in MATLAB from Mathworks [16], and then simulated with the aid of a Cadence Virtuoso circuit design and simulation package from Cadence Design Systems [17]. Knowledge gained from the design and simulation was at the same time used to design a program in MATLAB that automates this design. Layouts for several good circuits were drawn (in Virtuoso Layout Editor which is also a part of Cadence Virtuoso), and then the IC was sent for fabrication in the 180 nm BiCMOS process.

The detailed methodology followed in this thesis is described in Chapter 3.

1.5 DEFINITIONS

Definitions adopted by researchers are often not uniform; therefore the key and controversial terms have been defined to establish positions taken in PhD research.

As it will be explained in detail in Section 2.2.5, the PAs are grouped in classes, for example *Class A*, *Class E*. etc. If the letter naming the class follows the keyword *Class* without a dash (*Class A*), the keyword-letter combination is used as a noun. If a hyphen is

² SPICE stands for simulation program with integrated-circuit emphasis.

used, the combination is an adjective (*Class-A amplifier*). The keyword *Class* is capitalized in most cases, in order to point out that it is part of the name of the particular PA.

1.6 DELIMITATIONS OF SCOPE AND KEY ASSUMPTIONS

Although concepts developed in this thesis can be transferred to a vast number of fabrication technologies, due to the time and financial constraints for obtaining prototypes, the use of only two (SiGe BiCMOS) technologies was possible. Application of the developed methodology to other technologies is proposed, but testing of this idea was only possible from conceptual perspective.

1.7 CONTRIBUTION OF THE RESEARCH

A new method for the design of the full PA systems has been proposed for the use in the low-gigahertz integrated applications. A detailed list of the resulting contributions to the body of knowledge is given here.

- Inductors have been identified as being traditionally difficult to integrate due to low quality factors and their indeterministic behaviour. Main contribution of this research is engineering of an inductor design process. This inductance search algorithm finds the highest quality factor configuration of a single-layer square spiral inductor within a certain tolerance using formulae for inductance and inductor parasitics of traditional single- π inductor model. This algorithm in effect contributes towards enhancing conventional PA design and is a major improvement over the common trial-and-error methods used by current designers.
- An algorithm for calculating inductance, parasitics and Q-factor of the existing square geometries, has also been developed, so that the feature for the quick analysis of existing inductor structures can be retained.
- This research also shows that in fact, with the correct design methodology, which includes optimisation for operation at correct frequency, quality factors in excess of 10 can be obtained for on-chip inductors without modification to the process or flow of fabrication.

- Several inductors have been designed using the above mentioned algorithm and comparisons made with the experimental results for the AMS S35 process provided by the AMS foundry. Correspondence is established between designed, experimental and EM simulation results. EM simulations enabled qualification of inductors other than those with experimental results available. Average relative errors of 3.7 % for inductance and 21 % for the Q factor at its peak frequency were obtained for both metal-3 and thick-metal inductor options available.
- Although intended for the use with PAs, the spiral inductor design algorithms can contribute in any other application that might require integrated inductors, for example the low-noise amplifiers (LNAs) [18], DC to DC converters [19] or voltage-controlled oscillators (VCOs) [20].
- Further contribution of this research is a set of algorithms for the complete design of the switching-mode (Class-E and Class-F) PAs. These algorithms make use of the classic design equations so that the values of the parasitic components can be calculated given input parameters, including the required output power, centre frequency, supply voltage, and choice of class of operation (Class E or Class F). These design equations are brought forward from the existing body of knowledge and combined into a single routine which makes them easier to handle during the design process.
- In high power and low voltage supply applications, antenna resistances reaching values of less than 10 Ω would be needed. To overcome this impracticality this thesis provides algorithms that automate impedance matching from optimum to standard antenna impedances (50 Ω).
- Simulations showed that, for the complete PA system design, output matching and real (spiral) inductors, switch-mode PAs for 50 Ω load at 2.4 GHz centre frequency can be designed using the streamlined method of this research for the power output of about 6 dB less than aimed. This power loss was expected, and it can be attributed to non-ideal properties of the driving transistor and Q-factor limitations of the integrated inductors.

- While these results were obtained for only two fabrication processes, it has been found that principles devised in this thesis are technology independent and can be used with a range of CMOS and BiCMOS processes.
- Additional algorithms, such as the one for the SPICE netlist extraction and spiral inductor layout extraction (CIF and GDSII formats), were found extremely beneficial for the completeness of the design flow and integration into a compact EDA tool.

Table 1.1 shows some PA and spiral inductor designs found in literature and their design methods, while focusing on strengths and weaknesses of each employed method. This table also shows where and how the research presented in this thesis extends the existing body of knowledge by overcoming the identified weaknesses.

Table 1.1. Comparison of the PA design methods found in literature with the one proposed in this thesis.

Ref	Impact factor ¹	Topic	Strengths	Weaknesses
[21]	2.043	Class-E PA design	<ul style="list-style-type: none"> • Single ended Class-E PA design is performed while taking the advantages of the BiCMOS process over inferior CMOS processes. • Design is optimised for high efficiency. 	<ul style="list-style-type: none"> • Simulation-driven cut-and-try approach for the PA design is used. • Although the bond wire used for the resonant tank of the PA exhibits high Q-factor, such an approach cannot be extended to wider set of applications since the range of inductance values obtainable by bond wires is limited.
[22]	2.043	Two-stage Class-E design optimization tool	<ul style="list-style-type: none"> • Template-driven simulation-based methodology coined as software tool is presented. • The effects of parasitics for both active (transistors) and passive devices (inductors) are included. 	<ul style="list-style-type: none"> • The tool seems to be too detailed for the goal that it accomplishes: the design of only one topology, viz. two-stage Class-E PA.
[23]	2.043	Class-E PA in 65 nm CMOS	<ul style="list-style-type: none"> • The design employs a differential topology. • Finite DC feed inductance reduces high-voltage stress. 	<ul style="list-style-type: none"> • No design methodology for inductors is presented. • Although available switch-mode topologies are well researched, a repeatable design method is not speculated.
[24]	1.140	Class-F PA for low-voltage supplies	<ul style="list-style-type: none"> • Class-F PA utilizes a simple single-ended topology with input and output harmonic terminations. • High gain and high efficiency are accomplished. • Analysis of the spiral inductor model leads to inductor width that maximises the Q-factor. 	<ul style="list-style-type: none"> • No design methodology for inductors presented • A repeatable PA design method is not speculated.
[25]	1.436	Optimizing the design of spiral inductors	<ul style="list-style-type: none"> • It is identified that the width is dependent on the spiral length 	<ul style="list-style-type: none"> • Spiral length depends on input and output diameters making optimisation method impractical.

¹ ISI Web of Knowledge - Journal Citation Reports (Published by Thomson Reuters)

Table 1.1 (Continued). Comparison of the PA design methods found in literature with the one proposed in this thesis.

Ref	Impact factor	Topic	Strengths	Weaknesses
[26]	2.730	Analysis and synthesis of spiral inductors	<ul style="list-style-type: none"> • Advanced inductor modelling. • Full web-based inductor tool employs a search algorithm to synthesize inductors. • Both synthesis and analysis are performed. 	<ul style="list-style-type: none"> • Although designs have been optimised for different parameters, little discussion pertaining Q-factors has been carried out.
[27]	2.730	Inductor layout design optimisation	<ul style="list-style-type: none"> • The method looks into the effects of core diameter, turn spacing and turn width on the overall performance of inductors. 	<ul style="list-style-type: none"> • Multiple fabrication runs and wafer testing are necessary to optimise inductor designs.
[28]	2.730	Enhancement of the inductor Q-factor with low temperature annealing	<ul style="list-style-type: none"> • Although the substrate resistance is decreased which also decreases the Q-factor of the inductor, resistance of the spiral is decreased, resulting in overall inductor Q-factor increase. 	<ul style="list-style-type: none"> • Substrate resistance decrease apart from decreasing inductor Q-factor, could be influential on other components of a PA.
[29]	2.302	Q-factor improvement by means of deep-trench-mesh substrate	<ul style="list-style-type: none"> • Decreased capacitive coupling and resistive losses lead to Q-factor improvements up to 28 % in 0.35 μm BiCMOS process. 	<ul style="list-style-type: none"> • Cut-and-try method is used to optimise inductor designs. • Deep-trench-mesh might not be available in all technologies.
This work	-	Design methodology for switch-mode PA design	<ul style="list-style-type: none"> • Fully streamlined PA design method is presented for two-most common high-power high-frequency stages (Class F, Class E). • Matching and inductor design are presented. • Theory is fully backed up by means of simulations and experimental results (where applicable). • All geometry parameters are taken into consideration and total geometry search is performed. 	<ul style="list-style-type: none"> • The method only includes the design of the output stage.
This work	-	Optimisation of Q-factors of spiral inductors for square geometries	<ul style="list-style-type: none"> • Search is governed by inductance and Q-factor. • Technology independent. • Simulation/model oriented (no fabrication is needed for test runs). 	<ul style="list-style-type: none"> • No post-processing has been attempted.

1.8 PUBLICATIONS LEADING FROM THIS RESEARCH

The following journal articles have been published as part of research activities of the author:

- Božanić, M., Sinha, S., and Müller, A., 2010. Streamlined Design of SiGe Based Power Amplifiers. *Romanian Journal of Information Science and Technology (RJIST)*, Vol. 13, No. 1, pp. 22-32.
- Božanić, M. and Sinha, S., 2009. Design Approach to CMOS Based Class-E and Class-F Power Amplifier. *SAIEE Africa Research Journal*, Vol. 100, No. 3, pp. 79-86.
- Božanić, M. and Sinha, S., 2008. Software Aided Design of a CMOS Based Power Amplifier Deploying a Passive Inductor. *SAIEE Africa Research Journal*, Vol. 99, No. 1, pp. 18-24.

The following peer-reviewed international conference articles have been published and presented by the author:

- Božanić, M., Sinha, S., Müller, A. and du Plessis, M., 2009. Design Flow for A SiGe BiCMOS Based Power Amplifier, *Proceedings: IEEE International Semiconductor Conference (CAS) 2009*, 12-14 October, Sinaia, pp. 311-314.
- Božanić M. and Sinha, S., 2009. Design Flow for CMOS Based Class-E and Class-F Power Amplifiers, *Proceedings: IEEE AFRICON 2009*, 23-26 September, Nairobi, pp. 1-6.
- Božanić M. and Sinha, S., 2009. Design methodology for SiGe-based Class E power amplifier, *Proceedings: South African Conference on Semi and Superconductor Technology (SACSST)*, 8-9 April, Stellenbosch, pp. 31-36.
- Božanić, M. and Sinha, S., 2007. Design methodology for a CMOS based power amplifier deploying a passive inductor, *Proceedings: IEEE AFRICON 2007*, 26-28 September, Windhoek, pp. 1-7.

The following article was submitted to an ISI-listed peer-reviewed journal:

- Božanić, M. and Sinha, S., 2011. Switch-Mode Power Amplifier Design Method, submitted for publication in *Microwave and Optical Technology Letters*.

Program developed during the course of this research has also been commercialized (Appendix C).

1.9 OUTLINE OF THIS THESIS

Chapter 1 includes introduction to the thesis and a brief background for the research. The research question and hypothesis are clearly stated and justification for the research and its contributions are provided.

Chapter 2 provides the review of body of knowledge related to the context of this research. A brief discussion on PAs is given, followed by the more detailed discussion on the Class-A, Class-B, Class-C, Class-E and Class-F amplifiers, as well as on some hybrid classes. This is followed by a detailed discussion on inductors for PA applications, with special attention paid to the spiral inductor, its modelling, and techniques for increased quality factor integrated inductor design. Subsequently, some fabrication processes have been discussed in brief, with a more detailed discussion on the SiGe BiCMOS process and its relation to the silicon CMOS and GaAs HBT processes. The chapter concludes with the discussion on the importance of the rapid PA design.

Chapter 3 describes the methodology applied for the successful completion of the research presented in this thesis. It includes the research methodology outline, details on the software packages and design suites used for both research and development, background to the design process as well as description of the HBT SPICE model.

Chapter 4 describes concepts behind the MATLAB-routine based method for a rapid PA design. Flow diagrams of algorithms for the design of the Class-E and Class-F output stages, spiral inductor design, output impedance matching, as well as the flow diagram of the routine for the full PA system design are given here. For the complete program listings, the reader is referred to Appendix A. For the commercial version of the program, the reader is referred to Appendix C.

Chapter 5 describes the circuit level design and simulation of various PA systems used for testing of the first (MATLAB) version of the PA design routine. Circuit diagrams and simulation test benches and results constitute the bulk of this chapter. Inductor model and

inductance search algorithm are verified by means of EM simulations, as well as by comparison to the measured results. The streamlined use of the complete PA design routine is demonstrated by designing one Class-E and one Class-F output stage complete with input and output matching as well as biasing with minimum optimisation effort. For the technology files needed for completion of EM simulations, the reader is referred to Appendix B.

Chapter 6 presents layouts and photographs of the PA circuits submitted for fabrication as well the experimental results. The packaging and circuit board design issues are also discussed.

Chapter 7 concludes this thesis and gives suggestions for future research.

1.10 CONCLUSION

Chapter 1 laid the core foundations for this thesis. The research problem, viz. the need for a method to perform the tedious design of PAs and spiral inductors, has been formulated as a hypothesis, followed by the introduction to the research background. Solution to the research problem was proposed in the form of set of algorithms (initially developed in MATLAB) that will cover many aspects of a switch-mode PA design. Algorithms will additionally be able to handle modelling and design of the most important component of a PA – the passive inductor.

This chapter also briefly dealt with justification for the research and methodology used to carry out the research as well its contributions and research outputs to date. Finally, the outline of the thesis has been given. Chapter 2 follows with the review of literature.