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LC-LADDER AND CAPACITIVE SHUNT-SHUNT FEEDBACK LNA MODELLING FOR WIDEBAND HBT RECEIVERS

by

Marnus Weststrate

Submitted in partial fulfilment of the requirements for the degree

Philosophiae Doctor (Electronic Engineering)

in the

Department of Electrical, Electronic and Computer Engineering

Faculty of Engineering, Built Environment and Information Technology

UNIVERSITY OF PRETORIA

July 2011

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SUMMARY

LC-LADDER AND CAPACITIVE SHUNT-SHUNT FEEDBACK LNA MODELLING FOR WIDEBAND HBT RECEIVERS

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Keywords: Low noise amplifier, wideband, ladder filters, capacitive feedback, noise generators, impedance matching, mathematical model, noise optimization, performance trade-offs, mm-wave, SiGe Heterojunction Bipolar Transistor (HBT)

Although the majority of wireless receiver subsystems have moved to digital signal processing over the last decade, the low noise amplifier (LNA) remains a crucial analogue subsystem in any design being the dominant subsystem in determining the noise figure (NF) and dynamic range of the receiver as a whole.

In this research a novel LNA configuration, namely the LC-ladder and capacitive shunt-shunt feedback topology, was proposed for use in the implementation of very wideband LNAs. This was done after a thorough theoretical investigation of LNA configurations available in the body of knowledge from which it became apparent that for the most part narrowband LNA configurations are applied to wideband applications with suboptimal results, and also that the wideband configurations that exist have certain shortcomings.

A mathematical model was derived to describe the new configuration and consists of equations for the input impedance, input return loss, gain and NF, as well as an approximation of the worst case IIP3. Compact design equations were also derived from

this model and a design strategy was given which allows for electronic design automation of a LNA using this configuration. A process for simultaneously optimizing the circuit for minimum NF and maximum gain was deduced from this model and different means of improving the linearity of the LNA were given. This proposed design process was used successfully throughout this research.

The accuracy of the mathematical model has been verified using simulations. Two versions of the LNA were also fabricated and the measured results compared well with these simulations. The good correlation found between the calculated, simulated and measured results prove the accuracy of the model, and some comments on how the accuracy of the model could be improved even further are provided as well.

The simulated results of a LNA designed for the 1 GHz to 18 GHz band in the IBM 8HP process show a gain of 21.4 dB and a minimum NF of only 1.7 dB, increasing to 3.3 dB at the upper corner frequency while maintaining an input return loss below -10 dB. After steps were taken to improve the linearity, the IIP3 of the LNA is -14.5 dBm with only a small degradation in NF now 2.15 dB at the minimum. The power consumption of the respective LNAs are 12.75 mW and 23.25 mW and each LNA occupies a chip area of only 0.43 mm^2.

Measured results of the LNA fabricated in the IBM 7WL process had a gain of 10 dB compared to an expected simulated gain of 20 dB, however significant path loss was introduced by the IC package and PCB parasitics. The S_{11} tracked the simulated response very well and remained below -10 dB over the feasible frequency range. Reliable noise figure measurements could not be obtained. The measured P_{1dB} compression point is -22 dBm.

A 60 GHz LNA was also designed using this topology in a SiGe process with f_T of 200 GHz. A simulated NF of 5.2 dB was achieved for a gain of 14.2 dB and an input return loss below -15 dB using three amplifier stages. The IIP3 of the LNA is -8.4 dBm and the power consumption 25.5 mW. Although these are acceptable results in the mm-wave range it was however found that the wideband nature of this configuration is redundant in the unlicensed 60 GHz band and results are often inconsistent with the design theory due to second order effects.

The wideband results however prove that the LC-ladder and capacitive shunt-shunt feedback topology is a viable means for especially implementing LNAs that require a very wide operating frequency range and also very low NF over that range.

OPSOMMING

LC-LEER EN KAPASITIEWE SJUNT-SJUNT-TERUGVOER LRV-MODELLERING VIR WYEBAND-HBT-ONTVANGERS

deur

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Graad: Philosophiae Doctor (Elektroniese Ingenieurswese)

Sleutelwoorde: Laeruis-versterker, wyeband, LC-leerfilters, kapasitiewe terugvoer, ruisbronne, impedansieaanpassing, wiskundige model, ruisoptimering, verrigtings-kompromieë, mm-golf, SiGe Heterovoegvlak- Bipolêre Transistor (HBT).

Alhoewel die meeste draadlose ontvangersubstelsels oor die laaste dekade na syfer-seinprosessering verskuif het, bly die laeruis-versterker (LRV) steeds ’n noodsaaklike analoogsubstelsel in enige ontwerp, aangesien dit die substelsel is met die grootste impak op die ruissyfer van die ontvanger as geheel.

In hierdie navorsing word ’n nuwe LRV-topologie, naamlik die LC-leer en kapasitiewe sjunt-sjunt-terugvoertopologie, voorgestel vir gebruik in uiters wyeband-LRVs. Dit is gedoen na ’n deeglike teoretiese ondersoek van huidige LRVs in die literatuur. Hieruit het dit duidelik geword dat smalband-LRV-topologië oor die algemeen vir wyeband-toepassings gebruik word, wat lei tot suboptimale resultate, en ook dat die wyeband-topologië wat wel bestaan, bepaalde tekortkominge het.

’n Wiskundige model is afgelei om hierdie nuwe topologie te beskryf en bestaan uit vergelykings vir die inset-impedansie, die inset-weerkaatsingsverlies, die spanningswins en die ruissyfer, asook ’n benadering vir die ergste IIP3-geval. Kompakte ontwerpvergelykings is ook van die model afgelei en ’n ontwerpstrategie geskik vir

elektroniese ontwerpsoutomatisasie van LRVs met hierdie topologie is voorgestel. ‘n Proses vir die optimering van die versterker om die ruissyfer te minimeer is afgelei van die model en verskillende metodes om die lineariteit van die LRV te verbeter, is bespreek. Die voorgestelde ontwerpproses is deurgaans suksesvol toegepas tydens hierdie navorsing.

Die akkuraatheid van die wiskundige model is bevestig deur simulasies. Twee weergawes van die LRV is vervaardig en die gemete resultate vergelyk goed met die simulasies. Die goeie korrellasie tussen die berekende, simulasie- en gemete resultate bewys die akkuraatheid van die model. Opmerkings oor moontlike verbeterings aan die model om die akkuraatheid selfs verder te verbeter, is ook gemaak.

Die simulasieresultate van ’n LRV wat ontwerp is vir die 1 GHz- tot 18 GHz-band in die IBM 8HP-proses wys ’n wins van 21.4 dB en ’n minimum ruissyfer van slegs 1.7 dB, wat vermeerder tot 3.3 dB by die boonste afsny-frekwensie, terwyl die inset-weerkaatsingsverlies onder -10 dB bly. Nadat stappe gedoen is om die lineariteit te verbeter, is die IIP3 van die LRV -14.5 dBm met slegs ’n klein verswakking in ruis, waar die minimumruissyfer nou 2.15 dB is. Die LRVs se drywingsverbruik is onderskeidelik 12.75 mW en 23.25 mW en elke LRV beslaan ’n oppervlak van slegs 0.43 mm^2.

Gemete resultate van die LRV wat in the IBM 7WL-proses vervaardig is, toon ’n wins van 10 dB teenoor ’n verwagte gesimuleerde wins van 20 dB. Merkwaardige verliese is egter teenwoordig as gevolg van die geïntegreerde stroombaanpakkie en die toets-etsbord. Die gemete S_{11} volg die simulasies egter besonder goed en bly onder -10 dB oor die totale moontlike frekwensiebereik soos gevind in die simulasies. ’n Betroubare ruissyfermeting kon nie geneem word nie. Die gemete P_{1dB}-winssaamperspunt is -22 dBm.

Verder is ’n 60 GHz LRV ontwerp met hierdie topologie in ’n SiGe-proses met ’n f_T van 200 GHz. ’n Gesimuleerde ruissyfer van 5.2 dB is behaal met ’n wins van 14.2 dB en insetweerkaastingsverlies laer as -15 dB deur drie versterkerstadiums te gebruik. Die IIP3 van die LRV is -8.4 dBm met ’n drywingsverbruik van 25.5 mW. Alhoewel die resultate aanvaarbaar is in die mm-golflengteband, is so ’n wyeband-implementasie oorbodig in die ongelisensieerde 60 GHz-band en is gevind dat die resultate ook dikwels nie ooreenstem met die ontwerpsteorie nie as gevolg van tweede-orde-effekte.

Die wyeband-resultate bewys egter dat die LC-leer en kapasitiewe sjunt-sjunt-terugvoertopologie goeie potensiaal inhou vir LRV implementasies, wat veral ’n uiters wye bandwydte nodig het, asook ’n baie lae ruissyfer oor daardie band.

ACKNOWLEDGMENT

First and foremost I thank God for the grace of giving me the ability to complete this work and I trust that He will use my qualification for the glory of His name.

This research would not have been possible if it was not for my supervisor Prof. Saurabh Sinha who has over time been my teacher, mentor and friend. For not only offering me the opportunity to continue my postgraduate studies at the Carl and Emily Fuchs Institute for Microelectronics (CEFIM), but also securing funding for the research, and the invaluable guidance, advice and review of my work many thanks. Your availability, dedication to the betterment of your students, and effort towards providing quality feedback in as short a time as possible does not go unnoticed and was a key factor in the success of my research.

It has also been a pleasure working alongside my friends and colleagues Marius Goosen and Mladen Božanić towards the submission or our circuits on a combined MPW run. The teamwork is much appreciated. Also special thanks to Marius with whom I was able to discuss my work throughout the past few years leading up to this thesis which served as a catalyst in finding solutions to many problems.

I would also like to thank Jannes Venter for the Cadence support he provides at CEFIM and the great amount of time spent towards configuring a Cadence server compatible with the IBM HIT-kits. Our informal conversations on circuit design and layout have also been invaluable.

Thanks also to my other colleagues and friends at CEFIM, namely Wayne Maclean, Christo Janse van Rensburg, Johan Schoeman and Wynand Lambrechts for making the time spent on this research fun. And thanks to Johan and Wynand for reviewing the Afrikaans version of my summary. I also thank Professor Monuko du Plessis for his sound directing of the activities at CEFIM and Tilla Nel for ensuring that the admin runs so smoothly.

Finally I thank my other friends and family for the support they have given me, and in particular my mother for teaching me how to learn and strive for excellence from a young age, and my father for imparting his interest and experience in circuit design to me and for the countless discussions to the benefit of my research.

This research has been funded by ARMSCOR (the Armaments Corporation of South Africa Ltd.) under the direction of Rob Calitz and Knowledge Ramolefe for which I am truly grateful. The funds were administered by the Council for Scientific and Industrial Research (CSIR), South Africa.

I would also like to thank the Defence, Peace, Safety and Security (DPSS) business unit at the CSIR as well as Grintek Ewation for availing their laboratories for the experimental testing of the low noise amplifier.

I thank Denel Dynamics, a division of Denel (Pty) Ltd., for both extending my bursary to include my postgraduate studies and allowing me the time to complete this research.

I thank MOSIS for accepting my research proposal and granting the free IBM 7WL MPW production run that was used to fabricate the LNA.

I also thank the National Research Foundation (NRF) of South Africa for contributing toward travel expenses for conferences where this work was presented, as well as IMT-Bucharest in Romania for paying my local expenses in Romania through their bilateral agreement with CEFIM on two accounts. I thank also the Federal Ministry for Education and Research (BMBF), Germany, for paying my local expenses for a long term exchange at the Technical University of Dresden (TUD), and my colleagues at TUD for the pleasure of working with them.

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LIST OF ABBREVIATIONS

ADE	Analog Design Environment
ARJ	Africa Research Journal
BEOL	Back end of line
BGA	Ball grid array
BiCMOS	Bipolar and CMOS
BJT	Bipolar junction transistor
CMOS	Complementary metal oxide semiconductor
CSIR	Council for scientific and industrial research
DC	Direct current
DPSS	Defence, peace, safety and security
DUT	Device under test
EDA	Electronic design automation
ENR	Excess noise ratio
ESR	Equivalent series resistance
FET	Field effect transistor
FOM	Figure of merit
GaAs	Gallium arsenide
GBP	Gain-bandwidth product
HA	Hyper abrupt
HBT	Heterojunction bipolar transistor
HICUM	High current model
HIT-kit	High performance interface tool kit
IC	Integrated circuit
IF	Impact factor
IIP3	Third order input intermodulation product
InP	Indium phosphate
I/O	Input / output
IMN	Input matching network
ISI	Institute for Scientific Information
LNA	Low noise amplifier
LVS	Layout versus schematic
MDS	Minimum detectable signal

MIM	Metal-insulator-metal
MOS	Metal-oxide-semiconductor
MOSIS	MOS implementation service
MEP	MOSIS educational program
MPW	Multi-project wafer
NDA	Non-disclosure agreement
NF	Noise figure
PA	Power amplifier
PCB	Printed circuit board
PDK	Process design kit
PSD	Power spectral density
QFN	Quad flat no-lead (package)
RF	Radio frequency
SHF	Super high frequency
SiGe	Silicon-germanium
SPICE	Simulation program with integrated circuit emphasis
UWB	Ultra-wideband
VBIC	Vertical bipolar inter-company model

CHAPTER 1: INTRODUCTION

The research question addressed in this thesis is whether a combined LC-ladder and capacitive shunt-shunt feedback matching network can be used successfully in wideband low noise amplifier (LNA) implementations, especially with improved performance compared to current LNA implementations in literature.

1.1 BACKGROUND TO THE RESEARCH

In wireless receiver modules the first subsystem is usually a LNA designed to provide sufficient amplification for subsequent stages while adding as little noise as possible. The ability of a design to meet this objective is quantified in the noise factor of the amplifier which is defined as the ratio of the signal-to-noise ratio at the output of the amplifier to the signal-to-noise ratio at the input. It is well known that the first amplification stage dominates the total noise figure (NF) of the system [**1**] and thus the noise optimization of this first stage is critical. In general the important characteristics of low noise amplifiers are: low noise figure, good input matching, sufficient flat gain over a required frequency band, good linearity and reasonable power consumption.

As applications move to higher frequencies new design challenges are introduced. At high frequencies with wide frequency bands the noise performance of silicon bipolar junction transistors (BJT) are no longer satisfactory. Traditionally III-V compounds such as GaAs or InP were used in high speed applications as they are capable of achieving high unity gain frequencies, albeit at a much higher fabrication cost than that of silicon processes [**2**]. III-V compound devices require high supply current to achieve this high speed performance though, which makes their usage less desirable. Although the optimal noise performance and fabrication cost of GaAs and InP devices are comparable to that of silicon-germanium (SiGe) processes, the SiGe heterojunction bipolar transistors (HBT) have higher associated gain in amplifiers designed for minimum noise figure [**3**].

The increased availability of SiGe processes has positioned it as an important alternative to III-V compounds and has led to the use of SiGe HBTs in many high frequency applications. One of the major reasons for the success of SiGe HBTs in wireless applications is its very low noise capability [**4**] due to very high beta as well as a small base spreading resistance due to aggressive lateral and vertical scaling. In addition, HBTs

are high speed devices with unity gain frequencies above 200 GHz in certain processes making it an attractive choice for amplifier design at high frequencies. Since the SiGe fabrication process is an extension of the CMOS fabrication process to which extra processing steps are added it is also possible to integrate digital logic with efficient radio frequency (RF) circuits on the same die.

It has been shown that the input impedance matching plays an important role in achieving minimum noise figure and that an optimal source impedance exists for achieving the best noise performance [**5**]. This impedance is usually different than for maximum power transfer. LNA design entails achieving a low noise figure and usually optimal noise matching for a first amplifier stage. The obvious trade-off between minimum noise and maximum available gain has sparked much research interest into achieving a simultaneous optimal noise and power match. A traditional approach is the use of shunt-shunt feedback to modify the amplifier input impedance achieving such a simultaneous match [**6**], [**7**]. This also provides wide band operation. Emitter scaling is also a very common method used to modify the optimal source resistance of a transistor which could then be set equal to the characteristic impedance of the system [**8**], [**9**] achieving a simultaneous match in narrowband applications.

The LNA configurations mentioned above often employ inductive input matching or emitter degeneration. Through process scaling and lower inductor values required at high frequencies, the use of on-chip passive inductors have become common in integrated RF applications; however, these on-chip inductors suffer from low quality factor (Q-factor) due to the high permittivity of silicon dioxide which has a relative permittivity of 3.9. Although active inductors increase the noise figure of an amplifier they offer an important alternative for achieving a high Q-factor and reducing chip size and have been used in low noise amplifiers with good results [**10**].

At present narrowband techniques are often applied directly to wideband LNA implementations and as such good performance over the entire frequency band is often not achieved. This emphasizes the need for novel wideband LNA topologies capable of achieving good and relatively constant performance over the entire band of interest.

1.2 HYPOTHESIS AND RESEARCH QUESTIONS

Use of the LC-ladder input matching network has been shown as an effective means of achieving an arbitrary wide conjugate input impedance match and has been implemented in conjunction with the emitter degeneration technique [**11**]. This configuration has the shortcoming of introducing a pole at the lower frequency end, and this in turn requires an inductive load to equalize the voltage gain with the result that the final LNA requires four area consuming inductors. Due to the nature of the matching network a given lower corner frequency also fixes the collector current limiting the design decisions.

The shunt-shunt capacitive feedback technique has been shown capable of synthesizing an equivalent series RC network and used effectively in the design of a LNA for the ultra-wideband (UWB) [**12**]. This is however a narrowband configuration and is not ideal for wideband implementation.

From the above, the following hypothesis was formulated:

> *If a fourth order LC-ladder filter can be used to realize input matching over an arbitrary frequency band, and a shunt-shunt capacitive feedback common-emitter configuration can be modelled as an equivalent series RC circuit, then a combination of these two circuits can be used as a wideband LNA overcoming selected shortcomings of current LNAs in literature.*

To prove the hypothesis the following research questions must be addressed:

- Can it be proven through mathematical modelling that the proposed configuration is capable of wideband matching and low noise operation?
- Does this configuration avoid introducing a pole at the lower corner frequency?
- Can the inductor count be reduced compared to the LC-ladder and inductive emitter degeneration configuration?
- Does this configuration decouple the collector current from the lower corner frequency value?

1.3 JUSTIFICATION FOR THE RESEARCH

The goal of most wireless communication systems is achieving a high data rate. Even with the vast improvements allowed by the coding schemes employed in wireless communications today the signal-to-noise ratio remains a fundamental limiting factor of data throughput. Since the LNA is the determining factor in the noise figure of a system any improvement in noise figure is of great importance. Good linearity, which also limits the data rate, should however be maintained as the high power consumption required to compensate for poor linearity is undesirable, especially in battery-powered devices.

Table 1.1 lists the specifications of some related work found in literature indicating the state-of-the-art LNA performance. The simulated and measured results of designs done in this research using the proposed LC-ladder and capacitive shunt-shunt feedback configuration are also shown. For the same input matching and gain specification a lower NF and power consumption is achieved compared to most of the listed LNAs at the cost of reduced IIP3. This makes the proposed configuration especially suited to applications were low noise is very important and linearity only a secondary concern. Furthermore it is suited to very wideband designs such as the designed LNA operating from 0.8 to 18 GHz [**13**].

The desired specifications of the LNA that was designed in this research were defined towards the implementation of a receiver that is able to operate at multiple 800 MHz bands over the 1 GHz to 18 GHz range. A configuration capable of achieving such a wide band can however also be used for software defined radio (SDR) applications [**14**], [**15**] in general, or applied directly to smaller application specific sub-bands.

Since there is an abundance of bandwidth available in the unlicensed part of the mm-wave frequency band (57-64 GHz) which can be leveraged against power consumption in mobile devices [**16**], the investigation of a design at these frequencies is also warranted.

Although this research was done towards bipolar transistor LNA implementations the simple high frequency small-signal transistor model was used in the derivation of the mathematical model with r_π neglected in the frequency range of operation. The described techniques can therefore also be easily applied to field effect transistors (FET) with the only required change being the substitution of the appropriate equivalent noise source equations and transconductance equation for FETs.

Table 1.1. Simulated and measured results of the LNAs designed for this research using the proposed topology compared to state-of-the-art measured LNA results from literature.

Ref.	Impact factor (IF)	5 year IF	Technique	Technology / f_T	BW [GHz]	S_{11} [dB]	S_{21} [dB]	NF [dB]	IIP3 [dBm]	P [mW]	Area [mm^2]
This work	-	-	LC-ladder & capacitive-feedback (simulated)	0.13 µm (8HP) / 200 GHz	1-18	< -10	21.4	1.7-3.6	-22.6 @ 4.2 GHz	12.75	-
This work	-	-	LC-ladder & capacitive-feedback (optimized for linearity) (simulated)	0.13 µm (8HP) / 200 GHz	1-18	< -9.8	20	2.2-3.9	-14.5 @ 4.2 GHz	23.25	-
This work	-	-	LC-ladder & capacitive-feedback (simulated)	0.18 µm (7WL) / 60 GHz	3-14	< -10	20.7	2.8-4.3	-22.5 @ 6.5 GHz	14.22	0.4272
This work	-	-	LC-ladder & capacitive-feedback (optimized for linearity) (simulated)	0.18 µm (7WL) / 60 GHz	3-14	< -9.7	20.1	2.9-4.8	-19.0 @ 6.5 GHz	33.3	0.4272
This work	-	-	LC-ladder & capacitive-feedback (optimized for linearity) (measured)	0.18 µm (7WL) / 60 GHz	3-6	< -9.7	11†	N/A‡	-22.0 (P_{1dB})	33.3	0.4272
[**17**]	3.4661[1]	4.037	Inductive emitter degeneration	0.6 µm CMOS	1.5	< -10	22	3.5	-9.3 @ 1.5 GHz	30	-
[**11**]	3.4661[1]	4.037	LC-ladder & inductive-emitter degeneration	0.18 µm (Jazz semicond.)	3-10	< -9	21	2.5-4.5	-5.5 @ 3.4 GHz	30	1.35*
[**6**]	Proc.	Proc.	Frequency controlled shunt-shunt feedback	0.18 µm CMOS	3-10	< -13	8	3.5-4.4	-	18.5	-
[**18**]	2.7111[1]	3.187	Resistive feedback	0.18 µm / 150 GHz	3–10	< -10	20	3.4-4.7	-17 @ 3.5 GHz	42.5	0.18
[**19**]	3.4661[1]	4.037	Inductive emitter degeneration	0.18 µm CMOS	3-10	< -10	9.3	4-7	-6.7 @ 6 GHz	9	1.1*
[**20**]	Proc.	Proc.	Emitter degeneration with added BE-capacitance	0.18 µm / 120 GHz	0.1-13	< -7.2	20.3	1.8-3.1	2.1 @ 6 GHz	26	0.72
[**12**]	2.7111[1]	3.187	Shunt-shunt capacitive-feedback	0.35 µm SiGe BiCMOS	3-14	< -9	23	2.5-5.8	-17 @ 5 GHz	25.8	0.2223
[**21**]	1.13[2]	-	Parallel LC resonators & emitter degeneration	0.13 µm CMOS	6.8-8.8	< -10	29.5	4.0-5.2	-8.5 @ 7.7 GHz	15	0.4
[**9**]	2.3021[1]	2.533	Inductive emitter degeneration	0.13 µm (8HP) / 200 GHz	28-40	< -10	23.5	2.3-3.2	-19.5 @ 35 GHz	11	0.09
[**22**]	Proc.	Proc.	Multiple resistive feedback paths	0.35 µm (Jazz semicond.)	3-10	< -10	21	4.0-4.9	-	-	-
[**23**]	Proc.	Proc.	Diff. emitter-coupled pair with emitter followers	0.8 µm	3.1-10.6	< -7	19.9	2.1-2.9	-17.5 @ 7 GHz	77	0.14*
[**24**]	Proc.	Proc.	Three stage with CE and resistive feedback	0.18 µm / 120 GHz	5.2-15.8	< -10	19.1	4.2-5.2	-6.47 @ 13 GHz	116	0.0954*

1. ISI web of knowledge
2. https://www.researchgate.net/journal/1549-7747_Circuits_and_Systems_II:_Express_Briefs,_IEEE_Transactions_on

† From 3 GHz to 10 GHz
‡ NF measurement was not feasible due to the low gain
* Including bond pads

1.4 RESEARCH METHODOLOGY

Various LNA configurations were investigated in a thorough literature study to find the most appropriate option for wideband implementations. The shortcomings of many configurations were subsequently identified and narrowband configurations were deemed unsuitable for the design. A new LNA topology which is a combination of the LC-ladder input matching network (IMN) and capacitive feedback topology was then proposed to overcome many of these shortcomings [**25**].

A complete mathematical model which characterizes this configuration was subsequently derived and MATLAB was used to model the LNA performance. The derivation was done using an RF analogue approach. This mathematical model was also used to define compact design equations for a first order design and a process for optimizing the circuit for minimum NF was determined.

The design equations were used in the design of wideband LNAs using two different IBM SiGe BiCMOS processes, namely the 0.18 µm 7WL process and the 0.13 µm 8HP process with f_T of 60 GHz and 200 GHz respectively. Selected process parameters are discussed in Chapter 3. The calculated results were verified through simulations using Cadence Virtuoso and the high performance interface tool kits (HIT-kits) supplied by IBM.

Finally, after the LNA was optimized further using simulations it was submitted for fabrication in the IBM 7WL 0.18 µm SiGe BiCMOS process. The dies were packaged in quad flat no-lead (QFN) packages and soldered onto a test printed circuit board (PCB). The noise figure, gain, input reflection coefficient and P_{1dB} of one prototype was measured using a Rohde & Schwarz ZVA40 Vector Network Analyzer and an Agilent E4440A PSA spectrum analyzer.

To verify the accuracy of the initial calculated results and subsequent simulations, the measured performance was compared to results of simulations which included the package parasitics.

1.5 DELIMITATIONS OF SCOPE AND KEY ASSUMPTIONS

In the derivation of the mathematical model of the LNA the simple high frequency small-signal transistor model was used to derive equations that could be easily interpreted. Inductors were also viewed simply as a series inductance and parasitic resistance. This is however sufficient for a first order design and in fact agrees well with simulations done using complex transistor models despite the simplicity of this approach.

In the circuit simulations parameterized cells (p-cells) were used which include the device parasitics present in the circuit. The interconnect capacitance was however not included in simulation and may cause slight deviations in the expected performance.

During the experimental testing the characteristics of only a single prototype was measured due to the shortcomings of the test PCB discussed in Section 6.7. Therefore the presented results merely offers a proof of concept, but more rigorous testing should be performed to fully characterize the LNA performance based on a larger sample.

The noise figure was measured at room temperature and not at 290 °K as specified in the definition of NF [**1**].

1.6 CONTRIBUTION TO THE FIELD

A new LNA configuration, namely the LC-ladder and capacitive shunt-shunt feedback topology, has been proposed for use in wideband applications up to 20 GHz. A detailed list of the resulting contributions to the body of knowledge is given here.

- This configuration has been demonstrated successfully through the design and simulation of a 1-18 GHz LNA achieving a simulated 21.4 dB gain and S_{11} < -10 dB with a minimum NF of 1.7 dB increasing to a maximum of 3.6 dB at the upper corner frequency. The power consumption of this LNA is only 12.7 mW and it occupies a chip area of 0.43 mm^2 including three on-chip inductors.

- A second LNA with improved linearity from -22.6 dBm IIP3 to -14.5 dBm is also presented and achieves 20 dB gain with a minimum and maximum NF of 2.2 dB and 3.9 dB respectively, and power consumption of 23.3 mW.

- This proposed technique followed a thorough literature study on existing LNA configurations which were analyzed to find the performance and shortcomings of each as now given and compared in Chapter 2.

    - It became apparent that there is a need for wideband LNA configurations that can be applied directly to wideband implementations – as is the case with the proposed configuration which is a true wideband topology – instead of, as is often done [**12**], [**20**], adapting more well known narrowband techniques to wideband applications leading to undesirable and, as proven in this work, to a large extent unnecessary trade-offs between input matching, noise and gain performance.

    - Many wideband configurations that do exist do not optimize all LNA performance measures simultaneously, as in [**6**] for instance where high NF and low gain negates the advantages of a wideband conjugate match. It has been shown that minimizing NF and maximizing gain in the LC-ladder and capacitive shunt-shunt feedback topology can always be obtained simultaneously.

    - A large number of on-chip inductors (three being typical in narrowband and four in wideband implementations [**9**], [**6**], [**11**]) usually characterizes topologies in the body of knowledge. The LC-ladder and capacitive feedback topology however requires only a maximum of three inductors when operating close to the limits of the technology node where the first stage output pole could fall within the band of interest. When this is not the case, the first amplifier stage produces constant gain with frequency and the number of on-chip inductors could be reduced to only two.

    - In some cases a pole is introduced in the frequency response by the IMN, which could be at the lower corner frequency [**11**] requiring an inductive load to equalize the voltage gain, this however is not the case with the proposed technique in which there is no such intrinsic pole introduce by the IMN.

- A Monte Carlo analysis and temperature sweep showed that this is a very robust configuration, especially when the feedback techniques proposed to improve linearity are applied.

    - The gain of the LNA varies by only 2.4 dB on average and between 18.8 dB and 21.4 dB in the mid-band. Although S_{11} also varies by 2 dB it remains within specification over most of the operating bandwidth, and NF varies by as little as 0.3 dB over most of the band with the maximum NF in extreme cases being 4.25 dB.

    - A sweep over the military specification temperature range revealed only a 2.5 dB variation in gain and a 2 dB variation in NF from -55 °C to 125 °C.

- A first order mathematical model has been derived to characterize the proposed topology, and this model has also been used to derive compact design equations for such a LNA. The most novel contribution in this model is the derivation of the NF equation, in which the individual noise source powers occur as individual terms in the equation from which the dominant contribution could be determined, and strategies for optimization deduced. This allowed for a more focussed procedure for noise optimization.

- The model is suitable for use in electronic design automation (EDA) software that determines component values for a LNA based on a specified frequency range, gain and maximum NF. Preliminary MATLAB source code for such software used successfully throughout this research is given in Appendix A; and as such the design-for-design of this configuration has also been done. At the moment only a complete derivation for IIP3 is lacking and suggestions regarding this have been made for future work. Implementation of such EDA software will also ensure the repeatability of this novel design procedure and effectively archive it for future use.

- Some limitations of this topology have been identified and were also demonstrated in a 60 GHz LNA design where the wideband nature of the configuration proved redundant and the design theory did not meet with the expected results due to second order effects.

- It was noted that this topology can be used to push a transistor of a given technology node to its limits and then allows for trading gain, NF, bandwidth and power consumption during the design process. This trade-off has been quantified in the noise figure versus bandwidth trade-off equation which forms part of the model.
- The accuracy of the model has been verified through simulations in Cadence Virtuoso using the IBM HIT-kits, and LNAs of two versions of this topology have been submitted for fabrication. The measured performance from these LNAs conform well to the expected results from simulations when the shortcomings of the PCB and test procedure are taken into account which further validates this topology as a candidate for wideband LNA implementations.

1.7 PUBLICATIONS LEADING FROM THIS RESEARCH

The following peer reviewed conference articles have been published and presented by the author as part of his research activities:

- M. Weststrate and S. Sinha, "Noise optimization of a wideband capacitive shunt-shunt feedback LNA design suitable for software-defined radio," *Proc. of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Hammamet, 13-16 December 2009.
- M. Weststrate, S. Sinha and D. Neculoiu, "Limitations of a LC-ladder and Capacitive Feedback LNA and Scaling to mm-Wave Frequencies," *Proc. of the IEEE CAS 2009 (International Semiconductor Conference)*, Sinaia, pp. 315-318, 12-14 October 2009.
- M. Weststrate and S. Sinha, "Analysis of a Low Noise Amplifier with LC-Ladder Matching and Capacitive Shunt-Shunt Feedback," *Proc. of IEEE Africon 2009*, Nairobi, 23-25 September 2009.
- M. Weststrate and S. Sinha, "Mathematical Analysis of Input Matching Techniques With Application in Wide-band LNA Design," *Proc. of the South African Conference on Semi- and Superconductor Technology (SACSST)*, Stellenbosch, pp. 128-132, 8-9 April 2009.
- D. Foty, S. Sinha, M. Weststrate, C. Coetzee, A.H. Uys, and E. Sibanda, "mm-Wave Radio Communications Systems: The Quest Continues," *Proc. of the 3rd International Radio Electronics Forum (IREF) on "Applied Radio Electronics. The State and Prospects of Development,"* Kharkov, pp. 14-17, 22-24 October 2008 (Invited Paper).

Presentations were also given by the author at both the 9th and 10th European high current model (HICUM) workshop. At the workshop held in Würzburg, Germany on 23 October 2009 the presentation entitled *Design and Simulation of Wideband LNAs up to 60 GHz* was given and at the workshop in Dresden, Germany on 24 September 2010 a presentation entitled *Sensitivity of LNA performance characteristics to individual HICUM parameters*.

The following peer reviewed journal articles submitted by the author as part of his research activities have been published. All journals except the ARJ are accredited by the Institute for Scientific Information (ISI). The ARJ is, however, a fully peer-reviewed accredited journal – Dept. of Higher Education and Training (DoHET), Ministry of Education, South Africa:

- M. Weststrate and S. Sinha, "Mathematical Modelling of the LC-Ladder and Capacitive Shunt-Shunt Feedback LNA Topology," *SAIEE Africa Research Journal (ARJ)*, vol. 100, pp. 72-78, September 2009.
- M. Weststrate, S. Sinha and D. Neculoiu, "Design Trade-offs and Limitations of a LC-Ladder and Capacitive Feedback LNA and its Application at mm-Wave Frequencies," *Romanian Journal of Information Science and Technology (ROMJIST)*, vol. 13, no. 1, pp. 98-107, 2010.
- M. Weststrate and S. Sinha, "Wideband LNA design using the LC-Ladder and Capacitive Shunt-Shunt Feedback Topology," *Microwave and Optical Technology Letters, accepted for publication in July 2011*.

The following article by the author has also been submitted and conditionally accepted in an ISI accredited peer reviewed journal:

- M. Weststrate, A. Mukherjee, S. Sinha and M. Schröter, "Sensitivity of narrow- and wideband LNA performance characteristics to individual HICUM parameters," submitted to the *International Journal of Electronics, submitted in March 2011, resubmitted in May 2011*.

1.8 OUTLINE OF THE THESIS

Chapter 1 serves as an introduction to the thesis providing a brief background to the research resented. The hypothesis is stated and the justification for the research is

provided. A summary of the research methodology as well as the contribution of the research to the body of knowledge is also given with a list of publications leading from this research.

Chapter 2 provides a review of the literature pertaining to this research topic. A brief general discussion on the noise sources in transistors is given, followed by the effects of these sources in HBT amplifier circuits, as well as the characteristics of HBTs making them suitable for low noise design. A general discussion on input matching techniques is presented after which various matching schemes found in present literature are discussed with comments on the advantages and disadvantages of each. These include the well known inductive emitter degeneration technique which by way of emitter scaling used to adjust the optimal noise resistance can achieve a simultaneous optimal noise and conjugate input match. Also some techniques using feedback to adjust the input impedance and topologies with more complex input matching networks. The discussion involves a comparison of the gain, noise and linearity of these configurations. Subsequently the use of on-chip inductors, as well as the trade-offs and characteristics of active inductors are presented. This chapter concludes with the proposal of a new LNA topology combining the LC-ladder and capacitive feedback approach to provide wideband matching and good noise performance.

Chapter 3 describes the SiGe transistor processes used in the wideband LNA designs intended to verify the soundness of the mathematical model, and also the transistor models used in simulations.

Chapter 4 discusses the derivation of the mathematical model of the proposed amplifier configuration. Equations for input matching, gain and noise figure are derived and these are also rewritten to provide compact design equations. An approximation for the linearity and quantification of certain design trade-offs are also presented. Finally the design steps are given in a way that can potentially be used in a software package to automate the design process.

Chapter 5 describes the design and simulation of three different amplifiers. The first is a design for the 1 GHz to 18 GHz range using the IBM 8HP 0.13 µm process. The second is a design at 60 GHz using the same process and finally the amplifier to be fabricated using the IBM 7WL 0.18 µm process is presented over the 3 GHz to 14 GHz frequency band.

The layouts of the circuits that were fabricated are presented in Chapter 6 with some discussion as well as the packaging choices and its limitations. The schematic of a test PCB for the biasing and measurement of the packaged devices is also given.

The measurement setup and test procedures are discussed in Chapter 7. The experimental results are also presented with some comments on its comparison with the expected results from simulations.

The conclusion, critical evaluation of the work and potential areas for future research are provided in Chapter 8.

CHAPTER 2: LITERATURE REVIEW

2.1 INTRODUCTION

The objective in LNA design is to achieve sufficient gain over a required frequency band while maintaining a very low noise figure. This is crucial for the first amplification stage since it dominates the NF of the system as a whole as shown in

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A1}G_{A2}} + \frac{F_4 - 1}{G_{A1}G_{A2}G_{A3}} + \cdots, \tag{2.1}$$

where F is the noise factor, G_A the associated gain and the subscripts indicate successive amplifier stages [**1**]. The linearity of the amplifier as well as power consumption are also important specifications and thus limitations that the design must contend with. This chapter provides a review of the literature pertaining to low noise amplifier design and achieving these design objectives.

The increased availability of silicon-germanium (SiGe) processes has led to the use of SiGe HBT in many high frequency applications. One of the major reasons for the success of the SiGe HBTs in wireless applications is its low noise capability [**4**] and high speed, which also makes it attractive for low noise amplifier design; thus the use of HBTs is elaborated. Inductors are also important in RF design and the availability of on-chip inductors have allowed for complete integration of RF circuits. However, passive on-chip inductors are costly in terms of chip area and suffer from a low Q-factor and thus various inductor types and optimization techniques are briefly discussed, as well as the possibility of employing active inductors to avoid these shortcomings at the cost of higher noise.

The first part of this chapter discusses the noise sources present in transistors, followed by the effect of these sources in HBT amplifier circuits. The characteristics of HBTs making them suitable for low noise design are discussed, as well as important linearity considerations. Various input matching techniques are then presented, including a detailed discussion of the very common use of emitter scaling to adjust the optimal noise resistance for a simultaneous optimal noise and power input match.

2.2 NOISE IN AMPLIFIER CIRCUITS

There are five types of well known noise sources present in circuits with active and passive devices. These are [**26**]: Thermal noise, shot noise, Flicker or 1/*f* noise, burst noise and avalanche noise.

Thermal noise occurs due to the random thermal motion of electrons. For a given circuit component with a resistance *R* the average thermal noise voltage is given by

$$\overline{v^2} = 4kTR\Delta f \ , \tag{2.2a}$$

and the equivalent noise current by

$$\overline{i^2} = \frac{4kT}{R}\Delta f \ , \tag{2.2b}$$

where k = 13.8E-24 J/K is Boltzmann's constant, Δf is the amplifier noise bandwidth and T is absolute temperature. Since the standard definition of noise figure is at T = 290 °K [**1**] this will be the assumed temperature throughout this thesis unless otherwise stated. Since the thermal noise spectrum is frequency independent within the noise bandwidth it contributes to amplifier white noise. The thermal noise voltage or current is minimized for very small or very large values of *R* respectively.

Shot noise is associated with direct current (DC) flow through a p-n junction and is always present in diodes, MOSFETs and bipolar transistors. In a forward biased p-n junction the forward current exists as a result of holes and electrons gaining enough energy to cross the electric field present in the depletion region. Thus the passage of each carrier across the junction is a random event occurring when a specific carrier has sufficient energy and velocity directed toward the junction and the apparent steady forward current is in fact composed of a large number of random independent current pulses [**26**]. The fluctuations that occur in this current are called shot noise and is usually specified in terms of its mean-square variation about the average value as

$$\overline{i^2} = 2qI_D\Delta f \ , \tag{2.3}$$

where q is the electron charge, I_D the average forward current and Δf the amplifier noise bandwidth. The spectrum of shot noise is also frequency independent and thus contributes to white noise.

Flicker noise and burst noise are both frequency dependent and occur at lower frequencies. Flicker noise is caused mainly by traps associated with contamination and crystal defects which capture and release carriers in a random fashion. The time constants associated with this process give rise to a noise signal with energy concentrated at low frequencies [**26**]. Burst noise is not fully understood but does show some relation to the presence of heavy-metal ion contamination. Since the dependence of the noise spectral density on frequency for flicker noise is $1/f$ (pink noise) and that of burst noise $1/f^2$ (brown noise) above a cut-off frequency, these noise sources are not important in super high frequency (SHF) circuits, with the exception of voltage controlled oscillators where flicker noise can be up-converted as phase noise [**4**].

Avalanche noise occurs in reverse biased p-n junctions where electrons in the depletion region acquire sufficient energy to create electron-hole pairs by colliding with silicon atoms. This creates large noise spikes and generally dominates all other noise sources when present. The noise magnitude is proportional to the DC flow [**26**]. This source of noise can be minimized by ensuring the reverse bias voltage is small enough to limit the occurrence of avalanche breakdown.

In summary, for high frequency amplifier circuits, assuming reverse bias is sufficiently low such that avalanche breakdown becomes negligible, the noise sources to contend with are thermal noise and shot noise.

2.3 NOISE IN HBT AMPLIFIERS

The LNA noise figure is tied to the physical noise sources in the transistor which are, for SiGe HBTs, the shot noise associated with the base and collector DC as well as the thermal noise of the base resistance (r_b) [**4**].

Although many virtual resistors such as the output resistance of a transistor are included in the complete transistor model shown in Figure 2.1, these resistances, being virtual, do not contribute to the transistor thermal noise. The actual resistances present in a transistor are the base, emitter and collector series resistances which exist due to the resistivity of the

p- and n-material. In SiGe HBTs the emitter and collector resistances can usually be neglected since the emitter resistance is very small and the collector resistance thermal noise is reduced by the gain of the transistor when referred back to the input. This makes the base resistance the most important contributor of thermal noise. Since this noise is applied at the base of the transistor it is not reduced by the amplifier voltage gain and forms a major limitation on minimum NF.

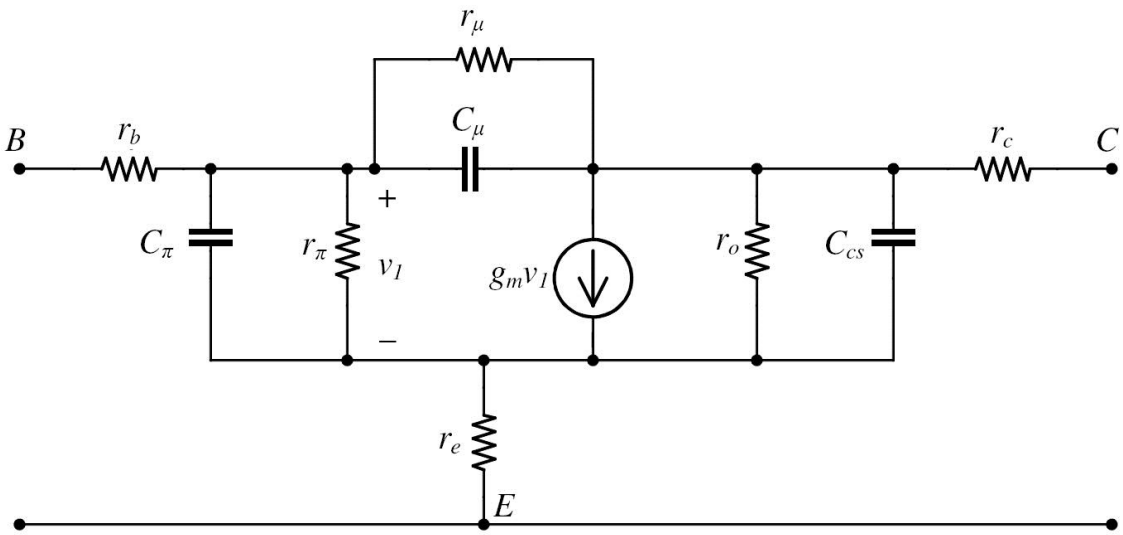

Figure 2.1. Complete bipolar transistor small-signal equivalent circuit.

As discussed in Section 2.2 shot noise is generated by DC flowing in forward [**26**] biased p-n junctions. In bipolar transistors both the base and collector currents introduce shot noise at the base-emitter junction. From the base majority carrier holes cross the base-emitter junction to form the base current and majority carrier electrons in the emitter cross the junction to form the collector current in *npn*-transistors. At the reverse biased collector-base junction the electric field causes a drift process which simply transports the electrons from the base into the collector without adding additional shot noise. The base transit time (τ_F) of the electrons across the base changes the correlation between the base and collector current noise in the common emitter configuration [**4**], however it is feasible to neglect this transit time (effectively assuming the noise is generated in the BC-junction) at frequencies much lower than $f_T/2$ [**8**]. In such cases the correlation admittance seen by the equivalent input noise voltage and current generators is only due to the collector current noise component (see (2.9) and (2.10) in Section 2.3.1) and equal to Y_{11} of the amplifier two-port.

2.3.1 Common-emitter amplifier noise and gain parameters

SHF LNAs are often implemented as narrowband amplifiers using active devices characterised by *S*-parameters and tuned with distributed passive structures. An alternative design technique is a RF analogue approach combining lumped passive devices with the transistor model to achieve the desired functionality [**27**].

The noise optimization methods of these approaches differ significantly. With the lumped element method the equivalent circuit of the transistor with the noise sources described in the previous section are considered with the elements comprising the matching networks and their noise sources in order to define an overall equation for the noise figure indicating which component values could be optimized. With a distributed design the minimum NF of a transistor (NF_{min}) is quantified and the deviation of the source impedance from the optimal noise match determines the final NF of the system. The following discussion assumes the latter approach.

Starting with the equations for a two-port's noise parameters in terms of the power spectral density (PSD) of the equivalent noise current and voltage as well as their correlation as given in [**5**], it can be shown that when written in terms of the intrinsic transistor parameters, the noise parameters of a common emitter amplifier are given by equations (2.4) through (2.7) [**4**].

$$R_n = r_b + \frac{1}{2g_m} \tag{2.4}$$

$$G_{s,opt} = \sqrt{\frac{g_m}{2R_n}\frac{1}{\beta} + \frac{(\omega C_i)^2}{2g_m R_n}\left(1 - \frac{1}{2g_m R_n}\right)} \tag{2.5}$$

$$B_{s,opt} = -\frac{\omega C_i}{2g_m R_n} \tag{2.6}$$

$$NF_{\min} = 1 + \frac{1}{\beta} + \sqrt{\frac{2g_m R_n}{\beta} + \frac{2R_n(\omega C_i)^2}{g_m}\left(1 - \frac{1}{2g_m R_n}\right)} \tag{2.7}$$

R_n is the noise resistance, $G_{s,opt} + jB_{s,opt}$ is the optimal source admittance and NF_{min} the minimum noise figure achieved when optimal noise input matching is used. Equation (2.7) can also be written in the more practically useful form [**8**]

$$NF_{\min} = 1 + \frac{n}{\beta_0} + \frac{f}{f_T}\sqrt{\frac{2I_C}{V_T}(r_E + r_B)\left(\frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{\beta_0 f^2}}, \tag{2.8}$$

where n is the collector current ideality factor, approximately equal to one, except under high current injection bias when its value can exceed 1.2. Equation (2.8) shows that the absolute minimum attainable noise figure is fixed for a specific process through the first and second terms. The third term indicates that NF_{min} is frequency dependent. It is apparent that at a given collector current the noise is primarily a function of four key parameters: the series resistances (r_b and r_e), the unity gain frequency (f_T), and the transistor common-emitter current gain (β) [**28**].

The two terms inside the second square root term become equal at $f = f_T / \sqrt{\beta}$ which defines the transition of NF_{min} from a white noise behaviour to becoming frequency dependent. Below this frequency NF_{min} is proportional to $\sqrt{r_b / \beta}$ which together with the second term indicate the need for high β and low r_b. Above this corner frequency NF_{min} increases with a slope proportional to $\sqrt{r_b} / f_T$ also making high f_T critical for achieving good noise performance. In this case β becomes irrelevant as long as it is sufficiently large (> ~50-100) [**28**].

When examined in terms of the physical noise sources in the transistor it can be seen that higher β reduces the base current (I_B) and the referred collector current shot noise which decreases the PSD of the equivalent input noise current (S_i) significantly as given by [**29**]

$$S_{i_n} = 2qI_B + \frac{2qI_C}{\beta^2}. \tag{2.9}$$

The frequency dependence of the noise current arises from the roll-off of β with frequency above $f_b = f_T / \sqrt{\beta}$ [**26**]. Lowering r_b causes a drop in the PSD of the equivalent input noise voltage (S_v) given by [**29**]

$$S_{v_n} \approx 4kT\left(r_b + \frac{1}{2g_m}\right). \tag{2.10}$$

The dependence of NF on I_C is apparent from both (2.9) and (2.10) through g_m.

The associated gain (G_a) of an amplifier is the power gain that can be achieved when the input of an amplifier is noise matched in order to minimize NF. It has been shown that the associated gain for HBT amplifiers is given by [**29**], [**30**]

$$G_a = \frac{1}{\omega^2 C_{bc} C_i r_b}\sqrt{\frac{g_m r_b + ½}{2}\frac{g_m^2}{\beta} + \frac{(\omega C_i)^2}{2} g_m r_b}\ . \tag{2.11}$$

It can be seen that increasing f_T by decreasing the input capacitance (C_i) serves to increase the gain in addition to improving noise performance. An increased β however decreases the associated gain since G_a is inversely proportional to the square-root of β. This is an important limitation since at low frequencies increasing β is the only means of reducing noise figure [**4**]. Although the base-collector capacitance (C_{bc}) does not impact NF_{min} directly, it does affect G_a which indicates that, in addition to large f_T, a large f_{max} is also desirable and is defined as [**31**]

$$f_{\max} = \sqrt{\frac{f_T}{8\pi r_b C_{bc}}}\ . \tag{2.12}$$

Finally it is seen that G_a increases with I_C through g_m indicating the need for a certain amount of I_C to have sufficient associated gain [**30**]. Equation (2.8) however shows that the NF also increases with g_m which implies a trade-off between NF and associated gain. To better quantify this trade-off the noise measure (M) which includes both the noise factor and associated gain in a single parameter is often used as a figure of merit (FOM) and is defined as [**28**]

$$M = \frac{F-1}{1-\frac{1}{G_a}}. \tag{2.13}$$

2.3.2 Low noise capability of HBTs

The intrinsic properties of SiGe HBTs make them especially well suited for low noise design. The additional freedom offered by band-gap engineering allows SiGe HBTs to simultaneously achieve high β, a high f_T and low r_b all of which are important for noise performance as described in the preceding section. This is in contrast to Si BJTs where these requirements often result in limiting constraints where for example decreasing r_b by increasing the base doping causes a drop in β [**30**]. Through the addition of germanium to the base of the transistor the band-gap energy of the base material is reduced which allows for much higher doping while maintaining good emitter injection efficiency.

A review of four generations of IBM technology [**28**] reveals the improvements in noise performance through both scaling and structural enhancements. Vertical scaling of the base and collector has resulted in a rise in f_T from 47 GHz in 0.25 µm technology to more than 200 GHz and even above 350 GHz in some 0.13 µm processes. With the reduction of base width using a higher Ge mole fraction to maintain a constant total Ge content in the base also increases β [**4**]. As a result of lateral scaling which reduced the minimum emitter area, f_T vs. I_C characteristics have been shifted toward lower currents allowing successive generations to achieve higher f_T at any given I_C value. This is especially desirable since SiGe HBTs typically have the best noise performance at less than 20 % of the peak f_T or f_{max} current density and high-current-density performance may be traded for improved noise at lower current densities [**28**].

Lateral scaling has also reduced the contribution of the sheet resistance of the intrinsic base to the overall r_b as it is inversely proportional to the emitter width. Although r_b could be further reduced by higher doping of the extrinsic base this is seldom done in traditional structures since the higher doping tends to diffuse toward the collector pedestal which increases C_{bc} and thus reduces f_{max} and the power gain. A key improvement in this regard has been the introduction of the raised base structure which is illustrated in Figure 2.2. The raised base decouples r_b and C_{bc} allowing extremely high extrinsic base doping for very low r_b without risk of a trade-off against C_{bc} [**28**].

The improvement of f_T has led to a 2.5 dB reduction in NF_{min} at 26 GHz and reduction of r_b has contributed another 1 dB drop. This gives a total NF improvement of 3.5 dB from the 0.5 µm to the 0.13 µm processes. At 15 GHz NF_{min} remains below 1 dB when I_C is varied

from 5 to 40 mA. The associated power gain is more than 10 dB with the highest value of 13 dB at 40 mA and continuing to rise beyond the maximum current used in the study [**28**].

These results show that HBTs are a good choice for high frequency and low noise applications.

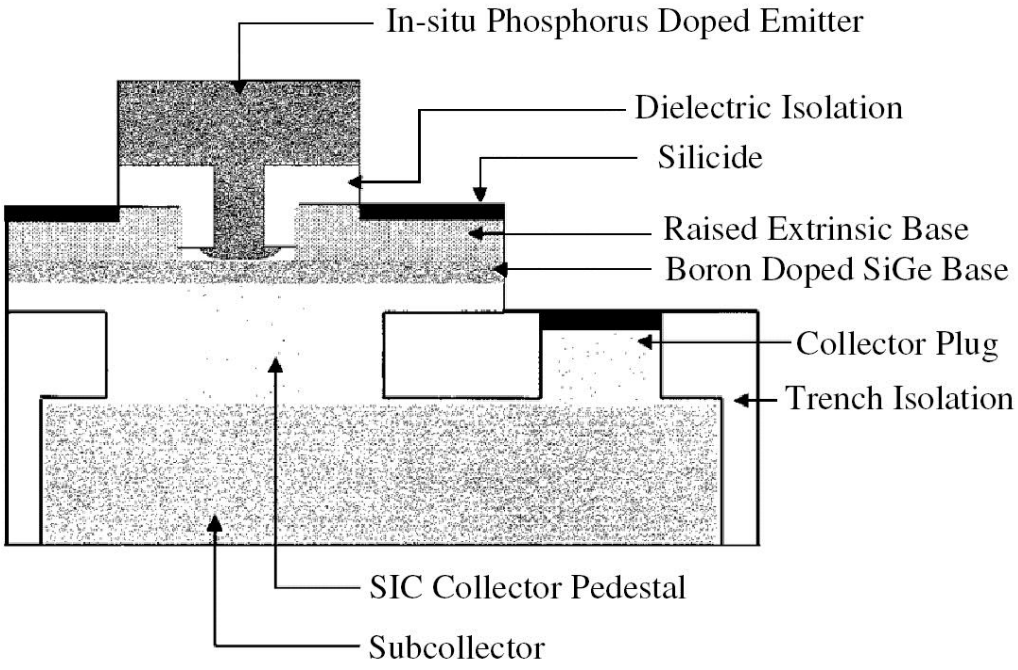

Figure 2.2. Cross section of a raised extrinsic base SiGe HBT [32**].**

2.3.3 Design for minimum transistor noise figure

It was shown in Section 2.3.1 that there is a minimum attainable noise figure for transistors in a given technology. The transistor deviates from this minimum noise figure through its dependence on the collector current through g_m, as well as an increase with frequency at higher frequencies as β starts to roll-off. From (2.7) it can be shown that NF_{min} first decreases with increasing I_C and then increases with I_C monotonically, if the dependence of C_i on I_C for bipolar transistors is observed [**4**]. This is shown in Figure 2.3 and indicates the absolute minimum noise figure that can be attained for this specific transistor by selection of a suitable I_C. Since the power gain is also dependent on I_C the associated gain was traded-off with a smaller NF which occurs at a f_T smaller than the maximum f_T for the device; typically at less than 20 % of the value for peak f_T in SiGe HBTs [**28**].

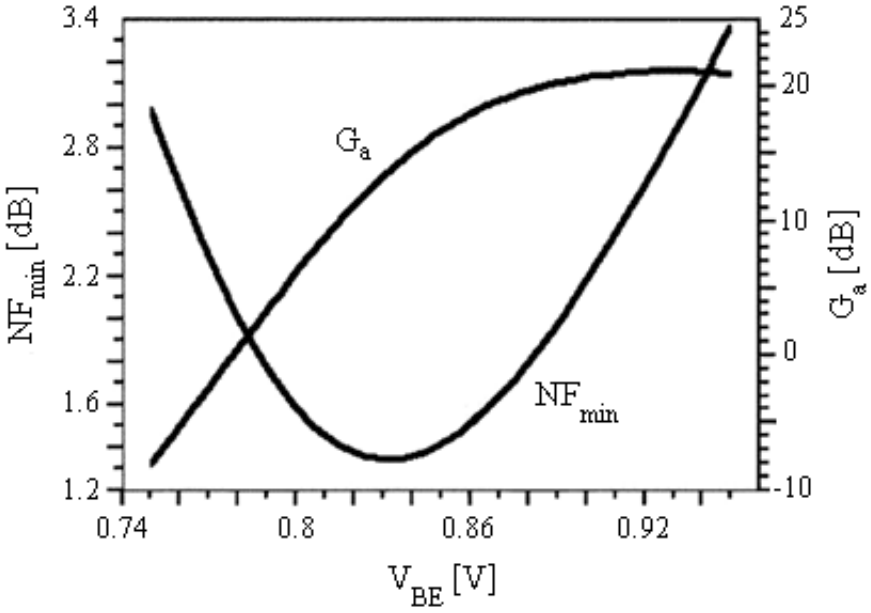

Figure 2.3. Typical minimum NF and current gain vs. VBE characteristic [4].

In selecting an amplifier topology for a multi-stage amplifier the FOM defined in Section 2.3.1 can be used as it captures both noise and available gain characteristics. The noise measure for identical SiGe HBTs in a common-emitter, common-base and cascode configuration was measured [**33**] at the minimum-noise bias and resulted in noise measures: M_{CE}=3.75, M_{CB}=3.40 and M_{casc}=3.47. These results show that for a simultaneous optimal noise and power match a common base amplifier stage would result in the best noise figure, however such a simultaneous match is not feasible for CB-amplifiers and thus a cascode configuration should be used instead [**33**]. Cascode amplifiers have the further advantage of good reverse isolation which simplifies the matching network design and also better frequency response due to reduced Miller multiplication of C_μ in the first transistor.

2.4 LINEARITY OF HBT AMPLIFIERS

The linearity of an amplifier can be quantified by either the 1 dB gain compression point (P_{1dB}) or the third order input intermodulation product (IIP3). P_{1dB} is the input power resulting in a 1 dB drop in the first harmonic power gain due to the output power present in the second and higher order harmonics. The IIP3 is the two tone input power resulting in the first and third harmonic output power becoming equal. It is usually necessary to extrapolate this value since it typically occurs at an input power larger than the onset of

gain compression and it can in fact be shown that P_{1dB} is typically 9.6 dB lower than IIP3 [**34**].

Five sources of non-linearity can be identified in bipolar transistor amplifiers. The collector current transported from the emitter (I_{CE}) is a nonlinear function of V_{BE}. The hole injection into the emitter (I_{BE}) is also a nonlinear function of V_{BE}. The avalanche multiplication current (I_{CB}) is a strong nonlinear function of both V_{BE} and V_{CB}. Finally, C_{BE} and C_{BC} are both nonlinear junction capacitance [**35**], [**36**].

In [**37**] a Volterra-series based approach was used which completely distinguishes individual nonlinearities and is practical in circuits operating in weak nonlinearity such as LNAs. It was found that in HBT amplifiers the nonlinearity is dominated by the $I_{CE} - V_{CE}$ nonlinearity for small collector currents, by the nonlinearity due to avalanche multiplication for 5 mA < I_C < 25 mA, and by the C_{CB} nonlinearity for collector currents above 25 mA.

The $I_{CE} - V_{CE}$ nonlinearity improves with higher collector current. Increasing J_C reduces the net charge density on the collector side of the CB junction which reduces $M - 1$ and thus also improves the avalanche multiplication nonlinearity. Therefore an improvement of IIP3 with collector current is seen until the C_{CB} nonlinearity starts to dominate after which the overall IIP3 is independent of collector current. It was also shown that an optimal V_{CE} exists for maximizing IIP3 for a given I_C [**37**]. This was found to be due mainly to the feedback provided by C_{BC} and the avalanche current.

Since the avalanche multiplication nonlinearity improves with higher J_C, and typical operating currents result in amplifiers operating where this nonlinearity dominates it is also clear why reducing the emitter area usually improves linearity.

Feedback is a well know method for improving linearity by either using local feedback in every amplifier stage or overall feedback between the input and output of the LNA. An improvement in IIP3 of $(1 + A\beta)^{3/2}$ is typically found when feedback is employed, where A is the forward gain and β the feedback gain of the amplifier [**38**].

The C_{BC} and avalanche nonlinearities can be reduced using the cascode instead of common-emitter configuration. With the cascode configuration V_{CB}, the voltage drop over the nonlinear C_{BC}, is greatly reduced, which also reduces the avalanche multiplication [**35**].

LNAs are often implemented as multi-stage amplifiers to achieve sufficient gain. In such cases the overall IIP3 is dominated by the IIP3 of the last amplifier stage, which is reduced by the gain of the preceding stages to find the overall IIP3. Therefore in multi-stage amplifiers the first stage should be optimized for minimum noise as it dominates the overall NF, and the final stage should be optimized for linearity [**39**].

2.5 INPUT MATCHING

Input matching is important in RF applications and even more so in LNA design. Not only is a conjugate match desirable to achieve maximum power transfer, but the final NF of the amplifier is also affected by the input matching network. The noise parameters of a two-port amplifier are the minimum noise figure NF_{min}, the optimal noise admittance $Y_{s,opt}$ and the noise resistance R_n [**5**] which were defined in Section 2.3.1. For an arbitrary source admittance Y_s the noise figure of an amplifier stage is given by

$$NF = NF_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{s,opt}\right|^2, \tag{2.14}$$

where G_s is the real part of Y_s and the other parameters are as defined in Section 2.3.1. The noise figure is minimized when $Y_s = Y_{s,opt}$ and R_n determines the sensitivity of the noise figure to deviations of Y_s from $Y_{s,opt}$. In general, the optimum Y_s for noise matching differs from the optimum source admittance for a conjugate match [**30**].

Various input matching techniques are presented in the following sub-sections followed by a discussion on the trade-offs of the performance measures that are involved [**25**].

2.5.1 Traditional input matching techniques

A number of traditional matching techniques with various tradeoffs exist to achieve both narrowband and wideband input matching. The simplest of these is a resistive match [**40**] where a 50 Ω shunt resistance (assuming a 50 Ω system) is used at the transistor base. Since the transistor input resistance is much larger than 50 Ω this results in a conjugate

match independent of frequency. The disadvantage of a resistive match is the increased voltage noise from the resistor usually leading to an unacceptably high NF. For this reason a resistive match is seldom used in practice.

Resistive shunt-shunt feedback can also be employed with much improved noise performance compared to a simple shunt resistor to ground, but the minimum NF is still not attained [**40**]. Since this configuration uses feedback, stability considerations also become important.

A third alternative is to use a common-base amplifier as the input stage [**40**]. The input impedance of a common-base amplifier is $1/g_m$ and, although sensitive to variations in temperature, a 50 Ω termination can be achieved by selecting I_C such that g_m = 0.02 S. However, this configuration still suffers from a high NF due to the collector current of the transistor not being optimized for low noise in the case of bipolar transistors; also since the common-base amplifier is a current buffer, any noise currents of subsequent stages are referred directly back to the input without reduction [**26**].

Of all traditional input matching techniques inductive emitter degeneration achieves the best noise performance [**17**] and was first introduced in [**41**] to generate the real part of the input impedance required for matching. It has further been shown that simultaneous optimal noise and conjugate matching is possible [**8**] by scaling the transistor emitter length. This technique is described in detail in Section 2.5.3.

2.5.2 Impedance matching in the super high frequency range

When designing amplifiers using the common-emitter or cascode configuration in the SHF range (3 GHz – 30 GHz), also referred to as the centimetre wave range, the transistor is operated far beyond the beta cut-off frequency f_β defined as f_T/β_0 where f_T is the transistor unity gain frequency and β_0 the DC current gain. Since the current gain rolls of at approximately -20 dB/decade above f_β it is found that

$$\begin{aligned}\beta_{RF} &= \frac{\beta_0}{1+\beta_0 \dfrac{C_\pi + C_\mu}{g_m} j\omega} \\ &= \frac{\beta_0}{1+\beta_0 \dfrac{1}{2\pi f_T} j\omega} \\ &\approx -j\frac{\omega_T}{\omega}\end{aligned} \tag{2.15}$$

for sufficiently high ω [**35**] where $\beta_0\omega/\omega_T >> 1$.

For the case where $\omega >> \omega_T/\beta$ one also finds that the impedance of the parasitic base-emitter capacitance (C_π) becomes small compared to the equivalent input resistance (r_π) as proved in (2.16).

$$\begin{gathered}When \quad \omega = \tfrac{\omega_T}{\beta} + \omega' \\ \left|y_{C_\pi}\right| = \omega C_\pi = \tfrac{\omega_T C_\pi}{\beta} + \omega' C_\pi \\ with \quad \omega_T \approx \tfrac{g_m}{C_\pi} \quad and \quad r_\pi = \tfrac{\beta}{g_m} \\ \left|y_{C_\pi}\right| = \tfrac{1}{r_\pi} + \omega' C_\pi \\ \therefore \quad \left|y_{C_\pi}\right| >> y_{r_\pi} = \tfrac{1}{r_\pi} \quad if \quad \omega' C_\pi >> 0 \\ \therefore \quad \tfrac{\omega_T C_\pi}{\beta} + \omega' C_\pi >> \tfrac{\omega_T C_\pi}{\beta} \\ or \quad \omega >> \tfrac{\omega_T}{\beta}\end{gathered} \tag{2.16}$$

This results in the base-emitter impedance (Z_π) being dominated by C_π and thus $Z_\pi \approx 1/(j\omega C_\pi)$.

Input matching is generally performed by generating an equivalent input resistance using either inductive series-series feedback in the emitter (L_E) of the transistor or shunt-shunt feedback between the collector and base terminals. This, together with a series inductor (L_B) at the base, results in an equivalent series RLC circuit seen at the input of the amplifier. The input impedance of such a RLC circuit is

$$Z_{IN} \approx sL_{IN} + R_{IN} + \frac{1}{sC_\pi}. \tag{2.17}$$

The frequency response of S_{11} is then [**12**]

$$S_{11} = \frac{Z_{IN} - R_S}{Z_{IN} + R_S} \approx \frac{s^2 + \frac{1}{C_{IN} L_{IN}}}{s^2 + s\frac{R_{IN} + R_S}{L_{IN}} + \frac{1}{C_{IN} L_{IN}}} \equiv \frac{s^2 + \omega_0^2}{s^2 + s\frac{\omega_0}{Q_{IN}} + \omega_0^2} \tag{2.18}$$

where $R_{IN} = R_s$ has been assumed, ω_0 is the resonant frequency of the RLC circuit and Q_{IN} the quality factor. Since S_{11} has a standard notch transfer function and it is required that $|S_{11}| < -10$ dB over the operating frequency range the Q-factor of the circuit is governed by [**12**]

$$\Delta f_{10dB} = \frac{\omega_0}{6\pi Q_{IN}} \approx \frac{R_{IN} + R_s}{6\pi L_{IN}}. \tag{2.19}$$

It follows that there is a limit on the maximum value of L_{IN} where $R_{IN} = R_s$ is fixed. This alludes to a limit on the bandwidth that can be achieved with this technique in practice and it will be shown that this implementation is indeed better suited to narrowband applications.

Two implementations based on this technique exist: the well known inductive emitter degeneration technique [**8**] as well as a relatively new topology employing capacitive shunt-shunt feedback [**12**].

2.5.3 Inductive emitter degeneration

Figure 2.4 shows the equivalent series RLC-circuit resulting from an emitter degenerative inductor (L_E). At high frequencies (with β defined as in (2.15)) β-multiplication of the emitter inductor results in the equivalent impedance

$$Z_{eq} = j\omega L_E (1 - j\frac{\omega_T}{\omega}) = j\omega L_E + \omega_T L_E \tag{2.20}$$

at the base of the transistor together with the base-emitter capacitance. With an additional series inductor at the base L_B+L_E can be chosen to resonate with C_π at the required centre

frequency, providing a real input impedance of $\omega_T L_E$ which can be chosen as 50 Ω providing conjugate matching for a 50 Ω source impedance.

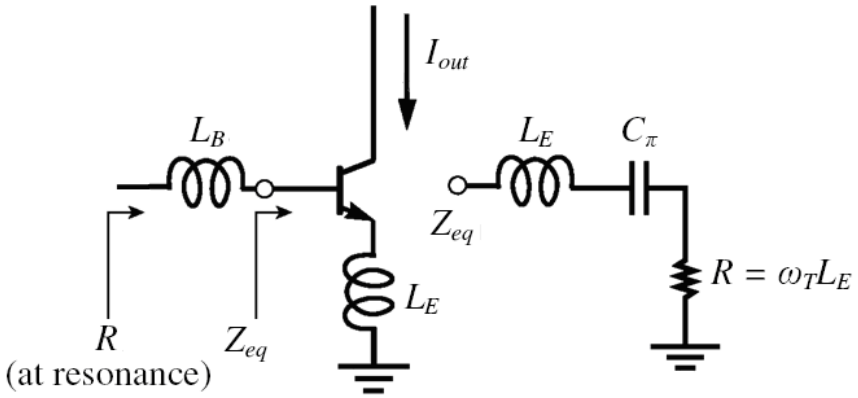

Figure 2.4. High frequency equivalent circuit at the base of an inductively degenerated common-emitter amplifier [11**].**

It has also been shown that simultaneous optimal noise and conjugate matching is possible [**8**] since $R_{s,opt}$ scales inversely with the transistor emitter length and the base inductor reduces the imaginary part of $Z_{s,opt}$ to zero resulting in an optimal noise match being achieved. Such a simultaneous conjugate and optimal noise match also results in the maximum attainable FOM.

Since the technique requires changing the optimal source impedance without increasing the minimum transistor noise figure, the effect of scaling the emitter length on NF should be investigated. The base resistance for a traditional silicon bipolar transistor is given by [**42**]

$$r_b = \frac{\sqrt{\rho_s \rho_c}}{2l_e} + \frac{\rho_s W_{eb}}{2l_e} + \frac{\rho_s w_e}{12 l_e}, \tag{2.22}$$

where ρ_s and ρ_c are the base and contact sheet resistances respectively, W_{eb} is the gap width between the base and emitter, w_e is the lateral emitter width and l_e is the emitter length. If the well known equation for the collector current of a bipolar transistor [**26**] is written in the form

$$I_C = J_S (w_e l_e) \exp\left(V_{BE} \Big/ nV_T \right), \tag{2.23}$$

where J_S is the saturation current density, n the ideality factor (approximately 1 in the process used for this research) and V_{BE} and V_T the base emitter voltage and thermal voltage respectively, and substituted into (2.8) together with (2.22) it can be shown that the minimum noise figure is independent of emitter length. This can also be shown for (2.7) when noted that C_i is dependent on I_C. This allows scaling of the emitter length without affecting noise figure while the emitter width is always kept at the minimum for a specific process since it has a large impact on the minimum noise figure. The dependence of NF_{min} on w_e is mostly due to the increased r_b with increased emitter width as seen in (2.22). Although the structure of SiGe HBTs is significantly more complicated and therefore not accurately described by (2.22) [**43**] the same qualitative result can still be obtained through such emitter scaling [**9**].

It was first suggested in [**8**] that the emitter length of a bipolar transistor could be scaled in order to change the optimal source impedance as both R_n and $R_{s,opt}$ scale with the inverse of emitter length as seen by substituting (2.22) into either (2.4) or (2.5), the latter resulting in the definition for $R_{s,opt}$ as a function of l_e as [**35**]

$$R_{s,opt} = \frac{\omega_T}{\omega}\frac{1}{l_e}\sqrt{\frac{2(r_b \cdot l_e)}{J_C \cdot w_e}V_T}\ , \tag{2.24}$$

where w_e is the emitter width, J_C is the collector current density and V_T the thermal voltage.

The following design steps were proposed:

1) Use simulations to find the collector current density J_C that minimizes NF_{min} and is set through V_{BE} as

$$J_C = J_S \exp\left(V_{BE}/nV_T\right). \tag{2.25}$$

2) Adjust the emitter length such that the optimum source resistance R_{opt} equals the characteristic impedance of the system (usually 50 Ω).

3) Add an emitter inductor L_E to match the real part of the input impedance. If lossless, L_E only changes X_{opt} but does not affect R_{opt}.

4) Add a base inductor L_B to cancel the transistor's input reactance and simultaneously transform the optimum noise reactance to 0 Ω.

The final circuit is then as shown in Figure 2.4.

This technique was used successfully in the design of low noise amplifiers at 1.9, 2.4 and 5.8 GHz [**8**] and also in a 52 GHz cascade LNA using SiGe HBTs [**33**]. It was found that the independence of NF_{min} on emitter length in practice is true for length-to-width ratios (l_E/w_E) larger than ten [**8**]. Furthermore when the finite Q-factor of the passive on-chip inductors, typically 7 to 10, was incorporated into the simulations the noise figure was degraded by 0.7–1.4 dB. This emphasizes the need for high Q-factor passive on-chip inductors.

More recent work done on this matching technique [**9**] points out the three key assumptions in the method discussed thus far:

1) NF_{min} is not a function of the emitter length at the optimal current density.

2) Inductor L_E does not affect R_{opt}, but only changes R_{in}.

3) The magnitudes of the optimal noise reactance and input reactance are always the same ($X_{in} = -X_{opt}$).

It was found that these assumptions do not hold well at mm-wave frequencies (the Ka-band was investigated in [**9**]) mostly due to the collector-base feedback capacitance C_μ. Since the Ku-band is also above 10 GHz it was important to investigate the effect of C_μ on the design of Ku-band amplifiers.

In the design steps above the real part of the input impedance is matched using an emitter inductor. As illustrated by Figure 2.4 an emitter degenerative inductor creates a series RLC-circuit at the input of the transistor which was shown to be

$$Z_{in} = \frac{g_m L_E}{C_\pi} + j\omega L_E + \frac{1}{j\omega C_\pi} = \underbrace{\omega_T L_E}_{R_{eff}} + j\omega L_E + \frac{1}{j\omega C_\pi} \tag{2.26}$$

neglecting C_μ. In this case the emitter inductor does not change R_{opt} but only X_{opt}. However, the input impedance and optimal source impedance changes substantially when C_μ is considered as shown in Figure 2.5, and for a cascode amplifier using the Miller approximation [**9**]

$$j\omega C_M = \frac{\omega^2 g_m L_E C_\mu}{1+(\omega g_m L_E)^2} + j\omega C_\mu \cdot \frac{2+(\omega g_m L_E)^2}{1+(\omega g_m L_E)^2} \tag{2.27}$$

From the real part of (2.27) it can be seen that L_E and C_μ generate a noiseless shunt conductance. The effect of this shunt conductance is illustrated in [**9**]. It can be seen that the optimal noise matching resistance does change with L_E through C_M (the Miller capacitance resulting from C_μ), and thus the L_E required for R_{in} = R_{opt} and X_{in} = –X_{opt} is no longer the same. This means that R_{opt} = R_{in} = 50 Ω is no longer the optimal value for simultaneous noise and conjugate match since X_{opt} is no longer equal to –X_{in} at that L_E value. Since the conductance of C_M is noiseless the value of L_E does not affect NF_{min}.

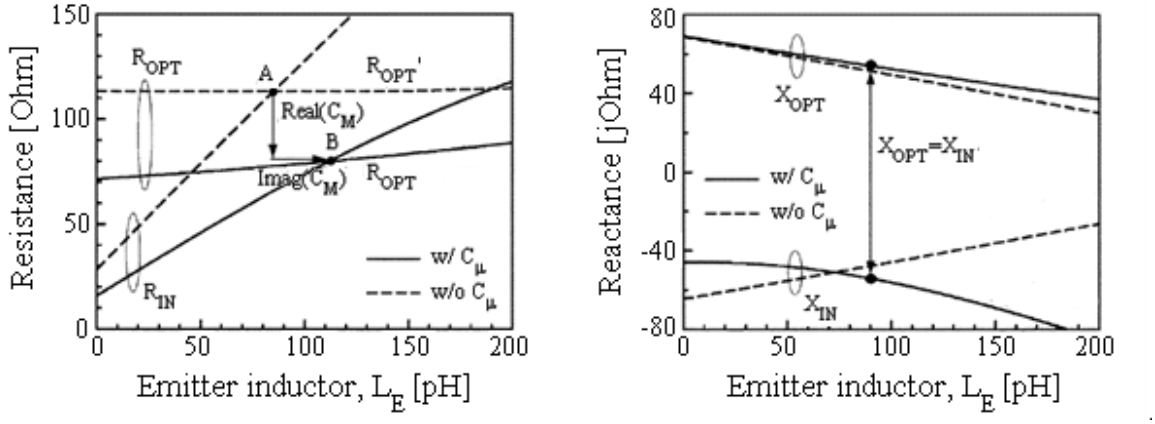

Figure 2.5. Simulated input and optimal noise resistance and reactance with and without Cμ [9].

To find the closest possible power match while still matching for optimum noise figure it is suggested [**9**] to minimize the reflection coefficient

$$\left|\Gamma_{opt-in}\right| = \left|\frac{Z_{opt} - Z_{in}^*}{Z_{opt} + Z_{in}^*}\right| \tag{2.28}$$

by adjusting the value of L_E. It is then possible to match for minimum noise figure at the resonance frequency with a single base inductor. At frequencies where the base inductor parasitic capacitances become important R_{opt} should be chosen larger than the characteristic impedance when adjusting the emitter length to compensate.

It has also been shown [**44**], and this was confirmed in [**9**], that there is some dependence of NF_{min} on l_E in SHF circuits and thus its effect should be taken into account for Ku-band designs. Assuming an optimal noise and power match condition with emitter and base inductors as described in Section 2.3.3 new forms of analytical equations were derived for the transistor IIP3, gain and NF and is shown as functions of collector current and emitter length in Figure 2.6 [**44**].

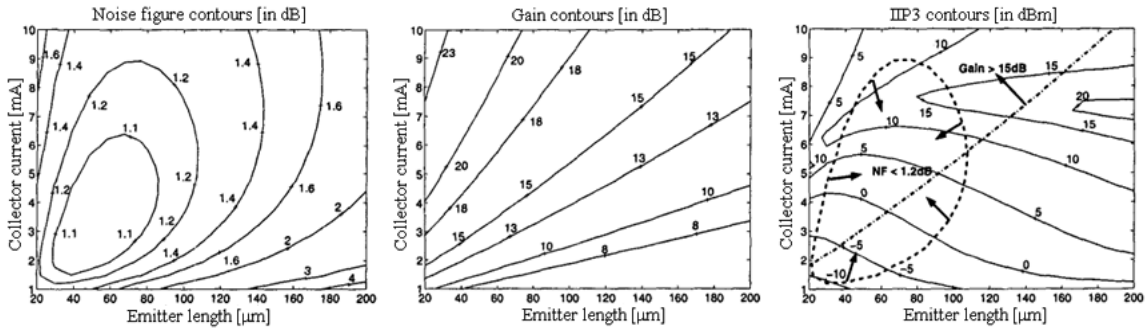

Figure 2.6. Noise figure, gain and IIP3 contours as a function of emitter length and collector current for an input impedance matched LNA at 2 GHz [44**].**

These equations/graphs can be used to design for a given NF, gain and IIP3 as indicated in the right most graph of Figure 2.6. The limit on NF and gain is drawn on the IIP3 plot to indicate the design space. In this specific design it was found that the IIP3 is 0 dBm at the optimum noise figure design point, however an IIP3 of 15 dBm was achievable with only a 0.15 dB increase in noise figure which is clearly the better design point. This shows the importance of considering all amplifier characteristics in choosing the operating point of a transistor. It is also important to note that fabrication tolerances in the emitter length will affect the amplifier performance.

Figure 2.7 shows the dependence of R_{opt} on emitter length and collector current with the plot of NF_{min} [**9**]. This is a further design constraint. To simplify the design of the first amplifier stage the gain may be regarded as less important since the required amplifier gain will be provided by subsequent stages. Power consumption places an upper limit on the

collector current, however for a substantial improvement of other amplifier characteristics slightly higher power consumption may be justified.

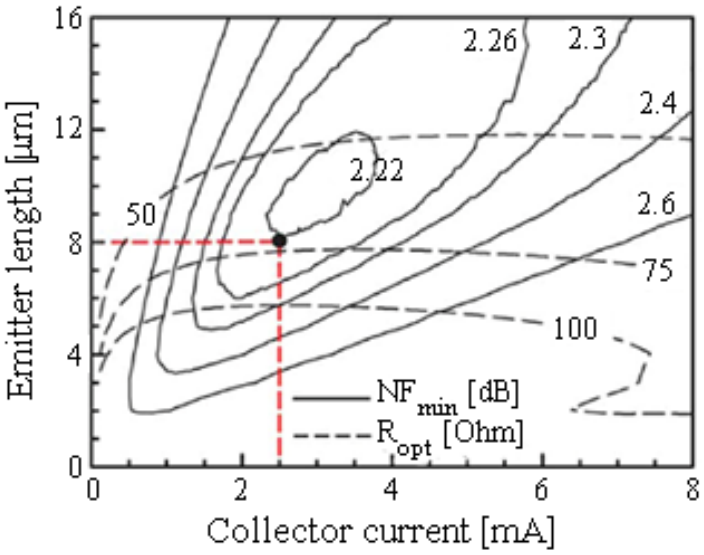

Figure 2.7. Simulated minimum NF and optimal noise resistance contour as a function of emitter length and collector current without emitter degeneration [9].

Form the above discussion it is clear that the selection of emitter length provides an important extra degree of freedom in the design of low noise amplifiers which may be easily overlooked as device dimensions do not form part of the traditional design parameters as is the case with MOSFETs.

The ability to match for optimum noise figure while achieving near optimal power matching makes this matching technique very attractive. However, a major disadvantage is that matching occurs only at resonance. In wideband applications this means that gain will degrade rapidly for frequencies away from the resonant frequency. The low Q-factor of the equivalent RLC circuit required for the S_{11} specification also severely degrades the NF as shown later in Section 2.6.1. Finally it was shown that the collector-base feedback capacitance and Miller effect neglected in the design equations modify the input impedance and thus the performance of implemented circuits differ from theoretical expectations.

2.5.4 Capacitive shunt-shunt feedback technique

An alternative method for generating an equivalent input RLC circuit which requires only one inductor, as opposed to the emitter degeneration technique which requires two area

consuming inductors, has been proposed which uses capacitive shunt-shunt feedback between the collector and base terminals as shown in Figure 2.8 [**12**].

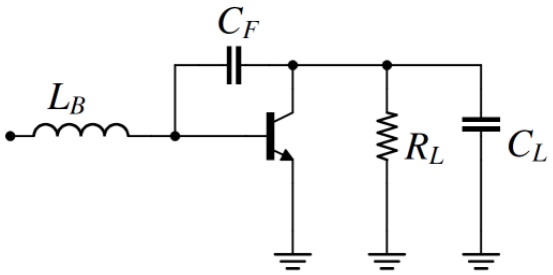

Figure 2.8. Circuit diagram of a capacitive shunt-shunt feedback circuit used to produce an equivalent input RLC circuit [12**].**

Using small-signal analysis the Miller impedance at the base of the transistor resulting from the feedback capacitor and load reactance can be written as

$$Z_M = \frac{1}{j\omega \underbrace{C_{BC}(1+g_m R_L)}_{C_M}} + \underbrace{\frac{R_L}{1+g_m R_L}\left(1+\frac{C_L}{C_{BC}}\right)}_{R_M}. \tag{2.29}$$

In this equation g_m is the transistor transconductance, C_{BC} the total base-collector capacitance comprised of the base-collector capacitance, C_μ, and an intentionally added capacitance, C_F, in parallel with C_μ where necessary. R_L and C_L are the respective parallel connected load resistance and capacitance as shown in Figure 2.8.

Thus the Miller impedance can be represented as an equivalent series resistor (R_M) and capacitor (C_M). This series combination can be converted to an equivalent parallel combination and can be combined with C_π which is also in parallel. Finally this total impedance can be converted back to a series RC circuit which forms the input impedance. The two components are then given by [**12**]

$$R_{IN} = \frac{R_L}{1+g_m R_L}\left(1+\frac{C_L}{C_{BC}}\right)\left(\frac{C_M}{C_\pi + C_M}\right)^2 \approx 50\,\Omega \tag{2.30a}$$

$$C_{IN} = C_\pi + (1+g_m R_L)(C_\mu + C_F) \tag{2.30b}$$

A base inductor is then used to set the resonant frequency of the circuit with C_{IN} similar to the emitter degeneration case.

A combination of inductive degeneration and capacitive feedback has also been used in with a cascode configuration [**45**]. The use of C_F provided an additional degree of freedom allowing improved linearity without degrading the NF.

2.5.5 LC-ladder input matching network with emitter degeneration

Both the emitter degeneration and capacitive feedback techniques are narrowband amplifiers due to the equivalent series RLC circuit at the input which is tuned to a centre frequency. The bandwidth is determined, and ultimately limited by the Q-factor of this RLC circuit.

As an alternative to using a low Q-factor series RLC circuit for input matching, a fourth-order doubly terminated bandpass filter has been used to produce a uniform input impedance over an arbitrary bandwidth through proper selection of the reactive elements [**11**]. This is illustrated in Figure 2.9. Inspection of the filter circuit reveals that the series RLC circuit required for the filter can be generated using the equivalent input circuit of the transistor, and thus a wideband 50 Ω input match can be achieved.

The values of the reactive elements are determined based on the upper (f_H) and lower (f_L) corner frequencies of the matched bandwidth by [**11**]

$$L_1 \approx \frac{R_S}{2\pi f_L} \quad and \quad C_2 \approx \frac{1}{2\pi f_L R_S} \tag{2.31a}$$

$$L_2 \approx \frac{R_S}{2\pi f_H} \quad and \quad C_1 \approx \frac{1}{2\pi f_H R_S} \tag{2.31b}$$

Two disadvantages of this configuration can however be identified. The series capacitance, C_2, (as in Figure 2.9) is the constant base-emitter capacitance of the transistor. From (2.31) the value of this C_π is then dependent on ω_L through

$$C_\pi = C_2 = \frac{1}{\omega_L Z_0}. \tag{2.32}$$

This can be substituted into the well know equation for ω_T

$$\omega_T = \frac{g_m}{(C_\pi + C_\mu)} \approx \frac{I_C}{V_T C_\pi} = \frac{I_C}{V_T C_2} \tag{2.33}$$

resulting in I_C being restricted to [**11**]

$$I_C = \frac{\omega_T V_T}{\omega_L Z_0}. \tag{2.34}$$

This prohibits the arbitrary selection of collector current to optimize NF or power consumption.

A further disadvantage is the pole introduced at the lower corner of the matched bandwidth by the input matching network. The current flowing into the matching network can be approximated as the source voltage divided by $2R_S$ over the matched bandwidth. The transistor output current is proportional to the base-emitter voltage which is the voltage over the series capacitor in the equivalent filter circuit since both the inductance and resistive parts are generated by the base and emitter inductors. The voltage over C_2 is given by [**11**]

$$v_\pi = \frac{v_s}{2R_S} \cdot \frac{1}{j\omega C_2} \tag{2.35}$$

which becomes

$$v_\pi = v_s \frac{f_L}{2f} \tag{2.36}$$

with the substitution of (2.31a) indicating a pole at the lower cut-off frequency. It is possible to compensate for this pole by using an inductive load.

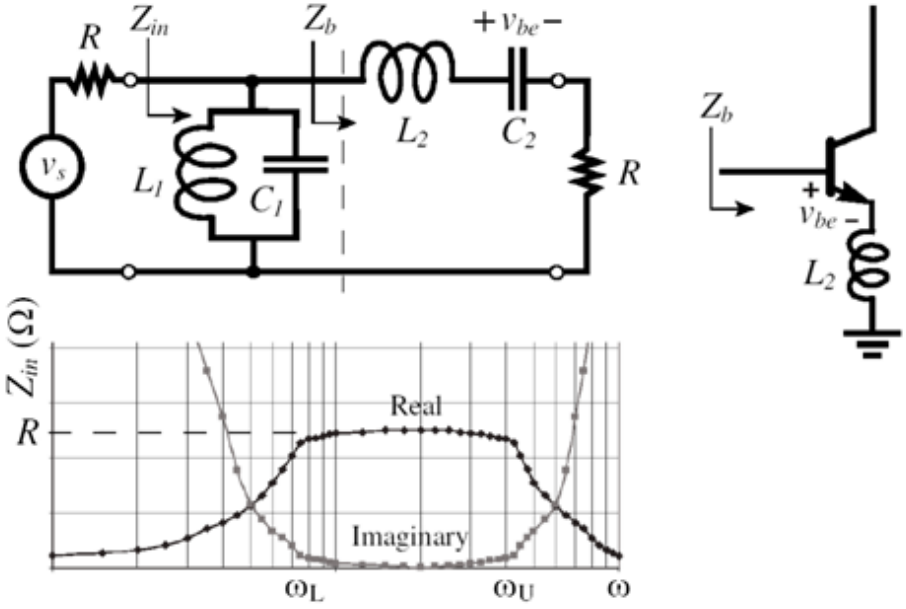

Figure 2.9. Band-pass resistor-terminated ladder filter, its input impedance vs. frequency and similarity with common-emitter amplifier degenerated with an inductor [11].

2.5.6 Wideband matching using shunt-shunt feedback

Feedback is often implemented in amplifier design as a means to linearize the gain, extend the amplifier bandwidth and also for input matching as described in Sections 2.5.3 and 2.5.4. A combination of series-series feedback in the emitter and shunt-shunt feedback between the base and collector has been used in [**6**] to achieve wideband matching as illustrated in Figure 2.10.

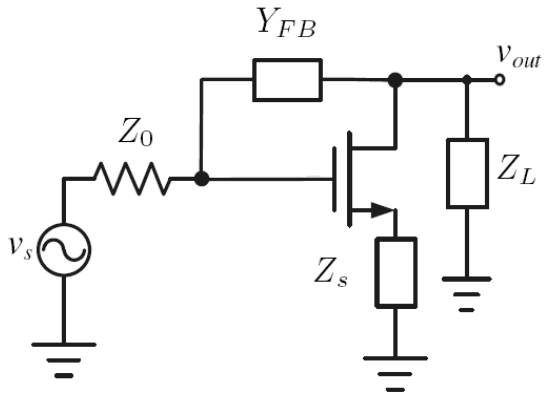

Figure 2.10. An emitter degenerated shunt-shunt feedback amplifier [6].

This configuration has been used to generate a combination of negative feedback and a controlled amount positive feedback at the high frequency end of the amplifier to achieve a

flat gain over the entire ultra wideband (3.1-10.6 GHz). Using the Miller effect a simultaneous wideband noise and power match was also achieved. The shunt-shunt feedback network is shown in Figure 2.11. The inductor L_d compensates for the typical gain roll-off of the transistor. The feedback network was designed to consist of a resistive component providing negative feedback over most of the amplifier bandwidth. A frequency dependent component (an inductor) was added to provide positive feedback at the higher frequency end, thereby compensating for the remaining gain roll-off of the transistor. A graphic design method to aid the design of the feedback network has been proposed [**7**].

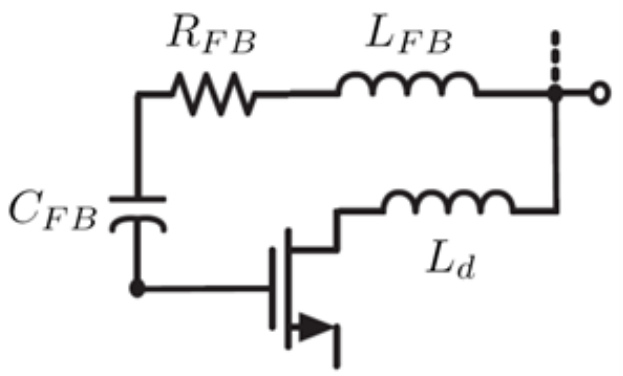

Figure 2.11. Shunt-shunt feedback network achieving a wideband flat gain response [6**].**

To perform input matching the Miller theorem was used to convert the feedback impedance to a shunt impedance at the input. The equivalent input impedance could be modelled as a parallel capacitor and resistor combination. This is due to the decreased effective inductance as the Miller effect decreases with the gain roll-off resulting in a capacitive reactance. This reactance was matched using a series inductor, which was also used to set the input impedance to the system's characteristic impedance as described earlier. The pad capacitance together with the inductor was used to absorb the input capacitance over a wide bandwidth resulting in an approximate wideband real input impedance. Thus a simultaneous noise and power match was achieved [**6**].

2.6 PERFORMANCE MEASURE TRADE-OFFS

Although all the matching techniques discussed in the previous section can be used to achieve good input matching, observations can be made regarding the trade-offs of NF, gain and linearity for the various configurations and are discussed next.

2.6.1 Noise figure

As mentioned earlier the matched bandwidth of the input impedance when using a narrowband matching technique is extended by lowering the Q-factor of the equivalent input RLC circuit. This however is in conflict with the goal of achieving high gain at ω_0 and it can also be shown that the collector current contribution to the NF is inversely proportional to the square of the Q-factor [**11**].

For a low-Q input RLC circuit $s^2 L_B C_{IN} \approx 0$ holds over the band of interest [**12**] and hence the NF contribution due to the collector current is given by

$$\begin{aligned} n_{ic} &\approx \frac{g_m}{2} Z_0 \left(\frac{\omega_0}{\omega_T} \right)^2 \\ &\approx \frac{R_S}{2g_m} \cdot (C_\pi + C_\mu)^2 \cdot \omega_0^2 \end{aligned} \tag{2.37}$$

which, when noting that $Q_{IN} = 1/\omega C_\pi R_S$, neglecting C_μ becomes

$$n_{ic} \approx \frac{1}{2g_m R_S Q_{IN}^2}. \tag{2.38}$$

This clearly indicates the trade-off between the NF and the input matched bandwidth.

In reality the base current also contributes to the NF and its contribution increases with Q_{IN} [**12**]. This means that an optimal Q_{IN} exists for achieving a minimum NF and can be set through proper transistor sizing. In addition it is well known that an I_C exists which results in minimum NF since collector current initially decreases with I_C while NF increases with I_B.

This allows use of the LNA optimization technique first formulated in [**17**] which has been adapted for use with bipolar transistor amplifiers in [**12**]; however the optimization is still restricted by the Q-factor requirement of the input matching.

Clearly it is desirable to decouple the input matching bandwidth from the input Q-factor to allow the Q-factor to be optimized for NF. The wideband LC-ladder matching network achieves this since the matched bandwidth is instead determined by the ladder filter

elements as in (2.31a) and (2.31b). The only remaining constraint on the input capacitance then results from ω_L through (2.32).

2.6.2 Linearity

While NF places a lower limit on the dynamic range of a LNA the IIP3 determines the upper limit. IIP3 is especially important in wideband LNAs where many signals stronger than the signal of interest may exist at surrounding frequencies compared to the narrowband case where out of band interference is filtered.

In the narrowband case it can be shown that the IIP3 is inversely proportional to the square of f_T [**11**]. This shows that maximizing f_T in order to minimize NF lowers (worsens) the IIP3 of the amplifier indicating a design trade-off.

In the wideband case, such as in Figure 2.9, the IIP3 can be defined as [**11**]

$$V_{IIP3_{LNA}} \approx 4\sqrt{2}V_T \cdot \left(1+\left(\frac{I_C \omega L_E}{V_T}\right)^2\right)^{3/4} \tag{2.39}$$

showing that the IIP3 improves with frequency in contrast to the NF, and the linearity can be improved by increasing the feedback through L_E. It was shown in [**45**] that feedback through an additional C_F also improves the IIP3 at the cost of gain. To maintain constant gain the collector current can be increased and the emitter area modified to maintain a constant J_C.

2.6.3 Gain

Although the first stage of a LNA typically focuses on achieving a low NF since a further amplifier stage can provide additional gain, the gain of the first stage remains important as it serves to reduce the noise of a second stage when referred to the input. In addition it is desirable to use a single stage LNA wherever possible to reduce physical size and power consumption.

As discussed, the magnitude of the current gain at the frequency range of interest for the applicable transistor process is given by $\beta = \omega_T/\omega$ and subsequently the power gain also increases with ω_T [**35**]. This satisfies intuitively why IIP3 would decrease with increased

f_T, which is a result of the higher gain. Increasing f_T however requires increased J_C which degrades the NF and thus NF must often be sacrificed to achieve a required gain specification.

A disadvantage of the techniques using capacitive feedback is that the gain is reduced further by the additional feedback. This will result in less reduction of the NF of a second amplification stage when referred to the input. The resulting higher input referred noise will then worsen the NF. This indicates the importance of considering all relevant design constraints in selecting the best amplifier topology.

2.7 ON-CHIP PASSIVE INDUCTORS

As the demand for RF ICs grew and devices started operating at higher frequencies requiring smaller inductor values, the use of on-chip inductors have come into widespread use. Although passive on-chip inductors allow for complete integration of RF applications, it comes at the cost of very large chip area and in many applications for example LNAs completely dominate the required chip area. These inductors also suffer from a low Q-factor (usually in the range of 7 to 15) which, to a large extent, is due to the poor permittivity of the silicon substrate and metal resistance. Higher substrate loss at high frequencies causes a further roll-off of the already low Q-factor as frequency increases.

Three main types of inductors can be integrated on chip [**46**]. Microstrip transmission line inductors are created by high-impedance transmission lines. However this technique is only available at very high frequencies such as the 60 GHz band where wavelength becomes comparable to the chip area. Even in these cases the transmission lines are costly in chip area and the narrow width of the lines introduce extra losses. With coplanar waveguide inductors both the centre conductor and the ground metal are in the top metal layer. Most of the electromagnetic field concentrates at the slot region minimizing the substrate loss. Although this inductor type exhibits the highest Q-factor it requires a very large chip area due to the ground metal also present on the metal layer. Finally, line inductors offer the highest inductance for a given chip area and are often implemented as spiral inductors. The smaller chip area tends to increase the Q-factor, however the magnetic field penetrates the lossy substrate and thus only moderate Q-factors can be achieved.

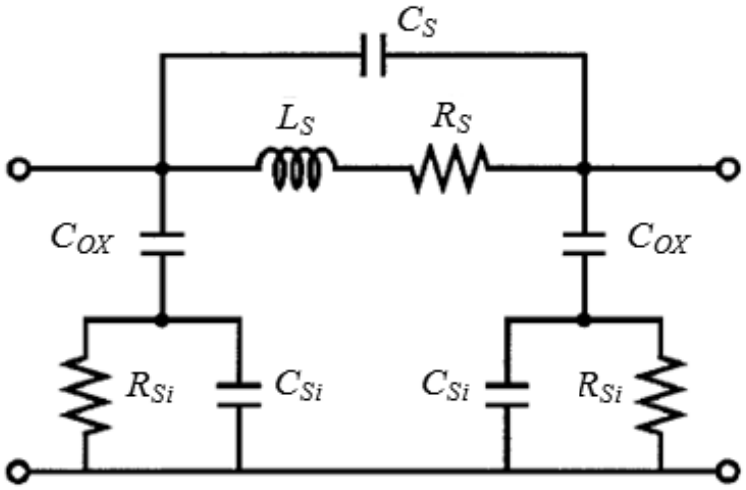

Figure 2.12. Lumped physical model of a spiral inductor on silicon [47**].**

A physical model which is commonly used to represent an on-chip spiral inductor and which also shows the introduced parasitic elements is illustrated in Figure 2.12 [**47**]. The series inductance is the desired component and results from the self inductance of the metal wire as well as the mutual inductance between the turns. The series resistance is due to the resistivity of the metal which is the dominant cause of low Q-factor at lower frequencies. The series capacitance results from the capacitive coupling between the spirals and the underpass of the inductor. The oxide capacitance between the inductor and the substrate as well as the capacitance and resistance of the silicon substrate are modelled as shunt components at the input and output of the inductor model.

The large number of parasitic elements involved in spiral inductor layout emphasizes the need for techniques to reduce these effects. The series resistance is a major contributor to low Q-factor and can be reduced by increasing the conductor thickness [**48**]. However, a disadvantage of this is that the inductance is inversely proportional to the metal thickness; and the skin effect becomes more pronounced as the thickness is increased which serves to increase the resistance in the higher RF range. The eddy current effect occurs when a conductor is subjected to time-varying magnetic fields and also contributes to the series resistance. These eddy currents manifest themselves as skin and proximity effects, where the skin effect causes the current in a conductor to induce eddy currents in the conductor itself and the proximity effect occurs when eddy currents are induced in a nearby conductor. In both cases the eddy currents serve to reduce the current flow and thus add to the series resistance. The eddy current effect is much less in the parallel turns of a planar spiral inductor, compared to the coupling between the conductors of stacked on-chip

inductors which is one reason for even further reduced Q-factor in stacked passive inductors [**47**].

Substrate loss is another major limitation of integrated inductors due to the high permittivity of silicon dioxide (ε_r = 3.9) and is the dominant factor in determining the self-resonant frequency. The relatively high conductivity of the doped substrate has further negative impact on performance. Since the inductor dimensions are usually comparable to the substrate thickness and much larger than the oxide thickness, the substrate capacitance and resistance are approximately proportional to the area of the inductor [**47**]. The substrate type however is also important in determining the substrate capacitance and resistance and this model is only valid for uniform substrate doping. It has been shown that higher doping result in higher capacitance and thus a lower self-resonant frequency [**48**].

Very thorough equations for the derivation of these parasitic effects are available [**47**] and are not repeated here. Losses can be minimized by proper selection of the conductor width, spacing and metal thickness for given substrate parameters. It may also be desirable to optimize for either low metal resistance at lower frequencies or lower substrate capacitance at high frequencies. The optimization of an inductor is crucial to achieve good performance, and computer optimization of the layout can achieve up to 50 % improvement in the Q-factor over un-optimized designs [**48**]. Such optimization software has been developed and is discussed in [**49**].

2.8 ACTIVE INDUCTORS

Active inductors provide a useful alternative to low Q-factor passive on-chip inductors. The parasitic elements of the active devices still limit the attainable Q-factor, however Q-factors in the high tens up to 100 are usually attainable using bipolar transistors. The main disadvantages of active inductors are increased power consumption, increased electrical noise from the active devices and limited dynamic range [**50**]. The noise introduced can be as much as 100 times larger than for a passive inductor [**51**]. This means the use of active inductors should be carefully considered as the increased noise makes it unsuitable for most low noise applications. Increased power consumption is also undesirable in most integrated applications, especially in portable devices.

Apart from the high Q-factor active inductors have the further advantage of offering a significant reduction in chip area compared to using on-chip passive spiral inductors. A three inductor LNA design has been reported where a 25 % reduction in chip area from 0.83 mm^2 to 0.6 mm^2 was achieved by implementing an active load inductance while doubling the amplifier's power consumption from 18.3 mW to 40.8 mW [**10**]. Although its use as a load inductance reduces the effect on the NF, the doubling of power consumption should be weighed carefully against the need for higher integration density in a specific application.

Many active inductor circuits employ a gyrator approach. An ideal gyrator is a linear two-port network that neither stores nor dissipates energy described by the volt-ampere characteristic [**50**]

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & g \\ -g & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{2.21}$$

where g is a designable transconductance parameter known as the gyration ratio. This implies that two voltage controlled current sources are required as shown in Figure 2.13. With the gyrator terminated in a capacitive load, the driving point input impedance is given by

$$Z_{in} = s\frac{C}{g^2}. \tag{2.22}$$

This is equivalent to an inductor $L = C/g^2$ and for an ideal lossless gyrator the Q-factor is infinitely large.

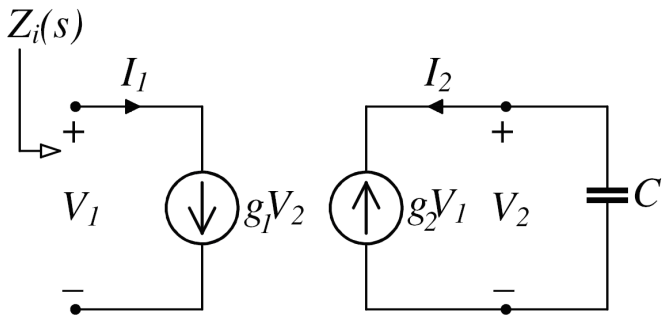

Figure 2.13. Two-port equivalent of an ideal gyrator terminated in a capacitive load resulting in an inductive input impedance [50**].**

In practical gyrator circuits both transconductance amplifiers will introduce parasitic elements. Not only will they have finite input and output resistances but also parasitic input and output shunt capacitances, as well as a feedback capacitance. In HBT amplifiers the input capacitance is derived from the depletion and diffusion components of the base-emitter junction capacitance and also from Miller multiplication of the base-collector junction capacitance [**50**] which can be quite large. The output capacitance in bipolar circuits is due to the collector-substrate capacitance which, depending on the amount of Miller multiplication, may not be a dominant energy storage element [**50**]. When the load capacitance value is calculated the parasitic capacitances at the port should be taken into account as this will serve to increase the effective capacitance. The input and feedback capacitances pose bigger problems which are discussed next.

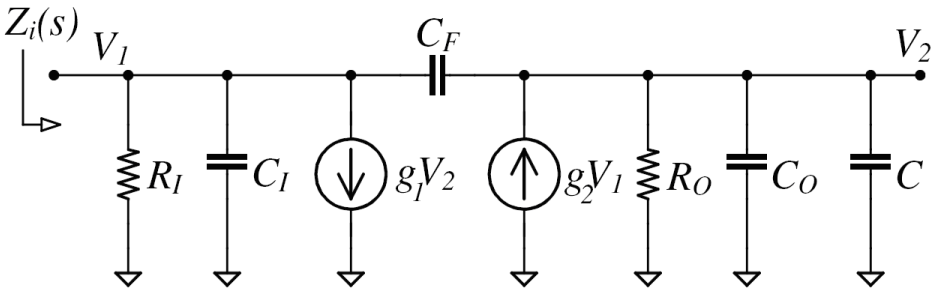

Figure 2.14. Linearized high frequency two-port equivalent circuit of an active inductor [50**].**

The active inductor gyrator circuit can be represented by the equivalent circuit in Figure 2.14. The input impedance of this circuit is [**50**]

$$Z_i(s) = \frac{R_e + sL_e}{1 + \left(\frac{2\zeta}{\omega_n}\right)s + \left(\frac{s}{\omega_n}\right)^2}. \tag{2.23}$$

At low frequencies the effective inductance L_e and series resistance R_e are given by

$$L_e \approx \frac{C_O + C_F + C}{g_1 g_2}, \tag{2.24}$$

and

$$R_e = \frac{1}{g_1 g_2 R_O}, \tag{2.25}$$

resulting in a finite Q-factor. Furthermore the denominator indicates undamped resonance at a frequency ω_n which is given by [**50**]

$$\omega_n = \sqrt{\frac{1}{L_e\left[C_I + \frac{C_F(C_O+C)}{C_O+C_F+C}\right]}}. \tag{2.26}$$

Thus the inductance produced at the input port effectively resonates with the net shunt input capacitance which limits the useful operating range of the active inductor. To ensure the stability of the circuit, g_2 (refer to Figure 2.14) should be larger or equal to g_1. If $g_2 \approx g_1$ and R_O is large, the damping factor (ζ) is given by

$$\zeta \approx \frac{\omega_n L_e}{2R_I}, \tag{2.27}$$

which shows that increasing the input resistance serves to increase the damping factor thereby circumventing potential oscillation problems [**50**].

Figure 2.15 shows a practical implementation of an active inductor with its equivalent circuit. The parallel capacitance is due to the input capacitance of transistor Q_1. The inductance is determined by the transconductance of the transistors and also by the base-emitter capacitance of transistor Q_2, which acts as the capacitive load for the gyrator circuit. This means that the inductor value could be increased by adding additional parallel capacitance between the base and emitter of this transistor; however this comes at the cost of bandwidth [**52**].

The ratio g_m/g_{ds} has also been identified as an indicator of active inductor performance, as the limited g_{ds} of FETs unavoidably raises the series resistance and degrades the inductor Q-factor [**52**]. Therefore using bipolar transistors improves the performance of the active inductor since the g_m/g_{ds} ratio can be in the order of thousands. The limitations of bipolar transistors include finite β, however this has little influence for β values above 100. The base-spreading resistance has a much greater impact on performance and should be kept to a minimum which can be done by using an appropriate transistor structure, usually with

multiple base contacts and a long stripe-shaped emitter region [**52**]. Another major advantage of using bipolar active inductors is its low power consumption compared to its FET counterpart. Only a fraction of the operating current is required to achieve similar performance [**52**].

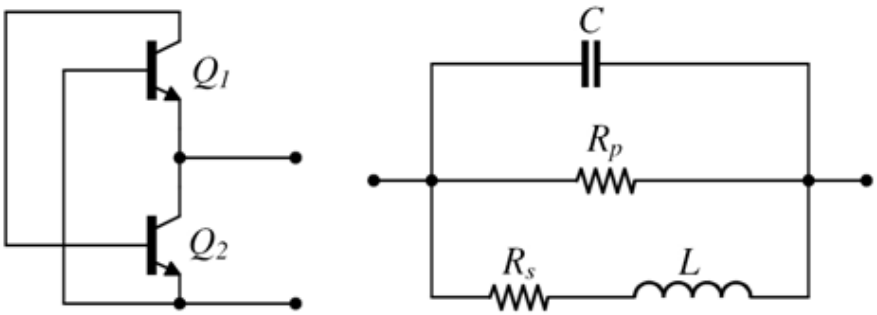

Figure 2.15. A two transistor active inductor configuration and its equivalent circuit representation [52**].**

A Q-factor enhancing method has been proposed [**52**] for this topology where a resistance is added in series with the base of the feedback transistor. The series resistor adds additional negative resistance to the circuit which serves to reduce losses at certain frequencies [**53**], [**54**]. This is especially useful in FET circuits since their lower gain and drain-source resistance reduces the Q-factor. However this is a narrowband technique and thus less suitable for wideband applications, indicating the need for bipolar transistors with inherent high gain in wideband designs.

2.9 CONCLUSION

The critical role of the LNA in a wireless receiver module makes LNA optimization an ongoing research topic where significant improvements are still being made. Since the input matching network is the determining factor in the NF for a given transistor technology, this has been identified as an area that would benefit from further research.

Both emitter scaling and shunt-shunt feedback can be used to achieve a simultaneous noise and power match, but the emitter scaling technique only provides an optimal match at resonance. Furthermore, due to the low Q-factor of the equivalent input circuit standard emitter degeneration configurations are not ideal for achieving a wideband low NF. This suggests that a wideband approach such as the LC-ladder input matching technique is the better choice in wideband LNA design.

The feedback offered by C_F in the capacitive shunt-shunt feedback configuration has proven to be an effective means of both generating an equivalent input RLC circuit, as well as improving linearity without degrading the NF. This technique also requires one less inductor compared to emitter degeneration, resulting in a smaller physical amplifier size.

Based on the findings in this chapter using a LC-ladder matched amplifier with capacitive shunt-shunt feedback a wideband conjugate match could be achieved. The matching bandwidth is decoupled from the Q-factor of the equivalent input circuit by the LC-ladder and C_2 is no longer restricted to the value of C_π due to the Miller capacitance resulting from C_F, thus overcoming many of the shortcomings identified in existing LNA configurations [**25**]. To the author's knowledge such a configuration has not been implemented.

Although geometry scaling and higher operating frequencies have enabled the use of on-chip inductors, allowing for the complete integration of RF circuits on chip, they remain an important limitation in such designs due to low Q-factor. The large parasitic resistance is especially important where NF is considered. At mm-wave frequencies using microstrip transmission lines are the most feasible implementation for inductors. In the SHF range the use of spiral line inductors offers the highest inductance per chip area and should be used and optimized as discussed in [**49**].

Active inductors are an alternative to passive on-chip inductors which achieves very high Q-factors and reduces chip area. This however comes at the cost of both higher noise and higher power consumption making them unsuitable for LNA input matching networks. Depending on the amount of noise reduction offered by the gain of preceding amplifier stages the use of active inductors as load inductors may be feasible.

To improve the linearity of the LNA local and/or overall feedback can be implemented and the cascode configuration can be used to reduce V_{CB}.

CHAPTER 3: SiGe MONOLITHIC TECHNOLOGIES

3.1 INTRODUCTION

This chapter describes the two integrated circuit processes that were used in the verification of the designed LNAs. Full details of the process design kits (PDKs) cannot be disclosed due to a non-disclosure agreement (NDA) with the foundry; only those details already available in the public domain are given here. Two models commonly used in the simulation of bipolar transistors are also briefly discussed.

The process that was initially selected for the implementation of the LNA is the IBM 8HP[1] 0.13 µm SiGe BiCMOS process available through MOSIS[2]. The process offers HBTs with unity gain frequencies of 200 GHz thus still providing high gain in the Ku-band as well as the low noise characteristics inherent to HBTs as described in Chapter 2, making it ideal for this LNA implementation.

A second IBM process was however used for fabrication of the LNA due to the availability of a run sponsored by MOSIS in the 7WL[3] 0.18 µm SiGe BiCMOS process. This process has an f_T of only 60 GHz. Simulations were nonetheless done using both processes and are discussed in Chapter 5 and as such a summary of the specifications of both processes are given in the following subsections.

Unless otherwise noted all data relating to the 8HP process was taken from [**55**], [**56**] and data for the 7WL process from [**57**], [**58**]. The maximum power supply voltage for the 8HP process is 1.5 V and for the 7WL process 1.8 V.

3.2 HETEROJUNCTION BIPOLAR TRANSISTORS

Both the 8HP and 7WL technologies offer high performance and high breakdown vertical NPN bipolar transistor variations. Selected electrical parameters of the high performance HBTs are summarized in Table 3.1.

[1] www.mosis.com/ibm/8hp/
[2] MOSIS is a multi-project wafer (MPW) IC fabrication service provider
[3] www.mosis.com/ibm/7wl/

Table 3.1. High performance HBT electrical parameters.

Parameter	Units	8HP Minimum	8HP Nominal	7WL Minimum	7WL Nominal
β	-	100	600	140	220
f_T (peak)	GHz	180	200	54	60
f_{max}	GHz	-	280	-	280
BV_{CE0}	V	1.5	1.77	2.8	3.3

3.3 HBT MODELS

Two high frequency transistor models commonly used in circuit simulation namely the vertical bipolar inter-company model (VBIC) and the high current model (HICUM) are discussed next.

3.3.1 VBIC – vertical bipolar inter-company model

For BJT simulation the VBIC transistor model included in the 8HP/7WL design kits was used by importing the appropriate model libraries into Spectre RF. The VBIC model is an extended Gummel-Poon model which has been created to overcome the deficiencies of the classic Gummel-Poon model. The large-signal equivalent circuit is shown in Figure 3.1.

The model provides built-in support for the following features [**59**]:

- Parasitic vertical PNP to substrate
- Weak avalanche multiplication (impact ionization)
- Thermal network (dV_{be}/dT)
- Fixed oxide capacitances for the emitter-base and collector-base junctions
- Quasi-saturation modelling
- Improved Early effect modelling (compared to the standard Gummel-Poon model)

The modelling of reverse base-emitter junction breakdown is not included as it is not supported by the VBIC equations. The NPN model in the 8HP process currently also support only one emitter stripe in either a c-b-e-b-c or c-b-e configuration. The 7WL process supports multiple emitters.

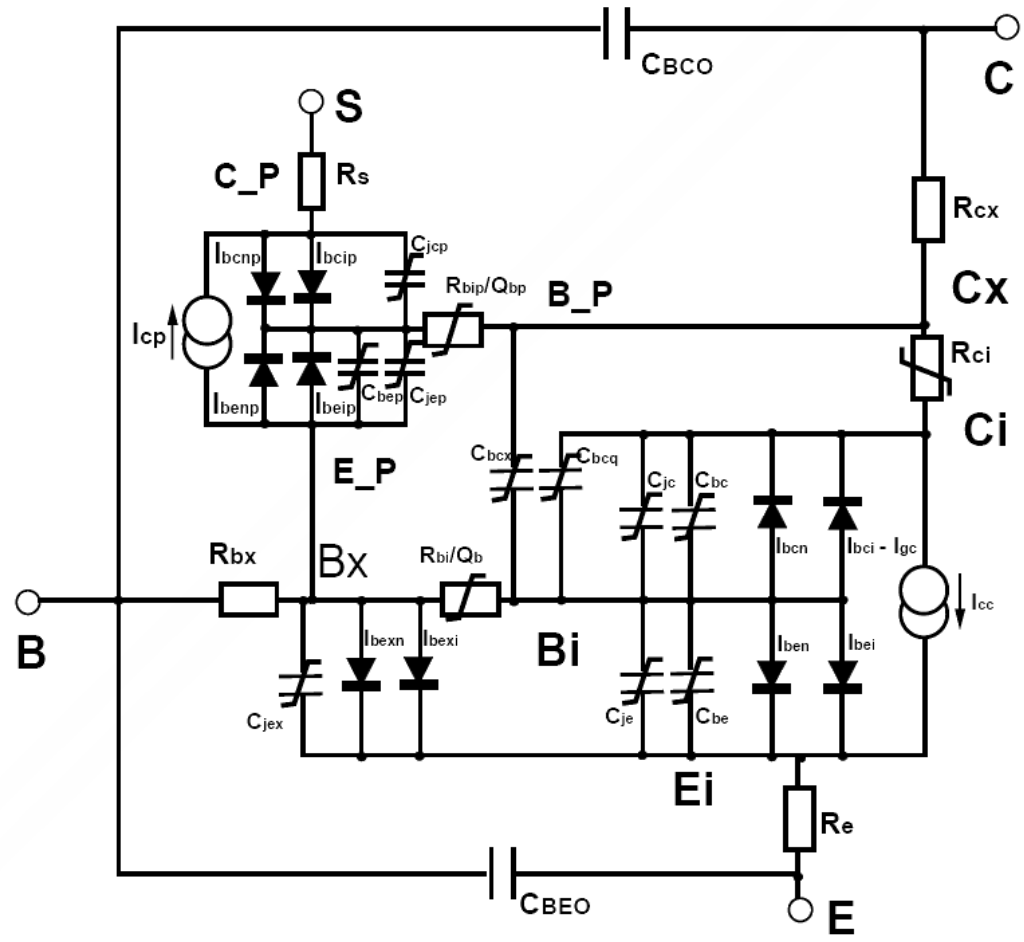

Figure 3.1. Equivalent large-signal circuit of the VBIC transistor model [59**].**

3.3.2 HICUM – high current model

Although simulations using the HICUM parameters were not done in this study it is referenced in the suggestions for future work and thus described here. The HICUM targets the design of bipolar transistor circuits at high-frequencies and high-current densities using Si, SiGe or III-V based processes.

HICUM is a semi-physical compact bipolar transistor model. Semi-physical means that for arbitrary transistor configurations, defined by emitter size as well as the number and location of base, emitter and collector contacts, a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data (sheet resistances and capacitances per unit area or length etc.) [**60**]. The large-signal equivalent circuit for HICUM/LEVEL2 is shown in Figure 3.2.

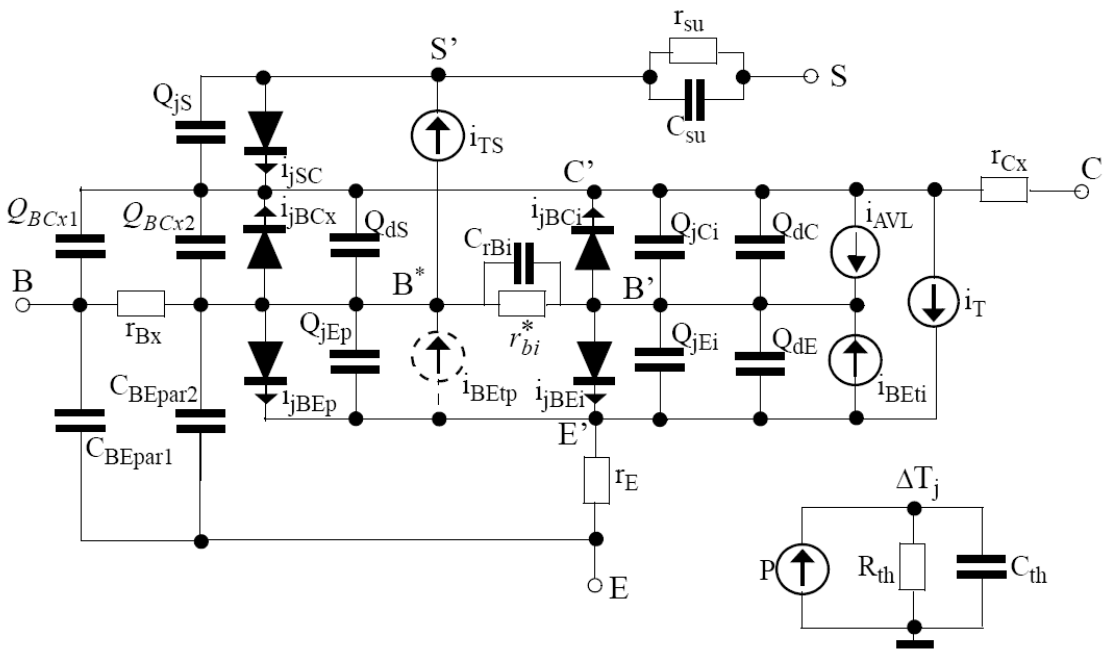

Figure 3.2. Large-signal HICUM/LEVEL 2 equivalent circuit [60**].**

The important physical and electrical effects taken into account by HICUM/LEVEL2 are [**60**]:

- High-current effects (including quasi-saturation).
- Distributed high-frequency model for the external base-collector region.
- Emitter periphery injection and associated charge storage.
- Emitter current crowding (through a bias dependent internal base resistance).
- Two- and three-dimensional collector current spreading.
- Parasitic (bias independent) capacitances between base-emitter and base-collector terminal.
- Vertical non-quasi-static (NQS) effects for transfer current and minority charge.
- Temperature dependence and self-heating.
- Weak avalanche breakdown at the base-collector junction.
- Tunnelling in the base-emitter junction.
- Parasitic substrate transistor.
- Band-gap differences (occurring in HBTs).
- Lateral (geometry) scalability.

3.4 METAL AND INTERCONNECT LAYERS

Both the 8HP and 7WL processes offer a maximum of seven metal layers. The first five layers of the 8HP process are copper interconnects with two analogue metal aluminium layers. In the 7WL process the first and sixth metal layers are copper and the other layers aluminium. In addition to these layers there is a special metal layer used to create metal resistors and an additional aluminium layer used to form the top plate of metal-insulator-metal capacitors.

3.5 8HP AND 7WL RESISTORS

The 8HP technology provides four types of resistors and the 7WL technology six, realized on different process layers. For a given sheet and contact resistance of the layer in question the resistance is calculated as

$$R = \left(R_S \frac{L}{W} \right) + \left(2 \frac{R_{end}}{W} \right), \tag{3.1}$$

where:

- R_S = Sheet resistance (Ω/sq)
- R_{end} = End contact resistance (Ω-μm)
- L = Design length from contact to contact
- W = Design width of the mask

Only square and rectangle geometries are supported. Since dog-bone and L-shapes are not supported this places a limit on the minimum dimensions which is larger than the general minimum feature rules.

3.6 CAPACITORS

The 8HP and 7WL processes provide three types of capacitors:

- MOS Varactors (thin or thick oxide MOS capacitor)
- HA varactors (hyper abrupt junction diode varactors)
- Single aluminium metal-insulator-metal (MIM) capacitors

Since the LNA does not require variable capacitance MIM capacitors were used. The 7WL process also has a dual MIM option effectively doubling the capacitance per area.

The nominal capacitance value of a single MIM capacitor can be calculated as

$$C = (C_A \cdot L \cdot W) + (C_P \cdot 2 \cdot (L + W)), \tag{3.2}$$

where L is the design length and W the design width. The capacitance per area and periphery capacitances are indicated by C_A and C_P respectively. The simulation model includes the parasitic capacitance from the bottom plate of the MIM capacitor to the substrate. This parasitic capacitance depends on the BEOL metallization option (nlev = 5, 6 or 7) and can also be calculated using (3.2) with the appropriate capacitance values.

3.7 INDUCTORS AND TRANSMISSION LINES

The 8HP process supports single layer inductors on the top metal layer. In the 7WL process single layer inductors as well as series or parallel stacked inductors on the two top metal layers are available, however only single layer inductors were used in the this implementation.

At the frequency of interest the inductance and quality factor vary considerably with frequency due to both the turn-to-turn parasitic capacitance and the conductive substrate. The peak Q-factor and corresponding frequency is lower than an equivalent inductor realized in a semi-insulating substrate process such as GaAs. Depending on the inductor design the Q-factor peaks may vary from 500 MHz to 15 GHz with higher frequency peaks occurring for lower values of inductance.

3.7.1 Inductor and RF-line layout considerations

To ensure enough resistance between the spiral and the substrate contacts surrounding it for decoupling, all contacts must be placed at least 80 µm from the spiral. If not the simulation results obtained with the ideal AC ground connection are no longer valid. This rule is also applicable to RF-lines.

Metal areas adjacent to the spiral connected to AC ground will add capacitance in parallel with the inductance lowering the self resonance frequency and large planes or closed loops

of metal will support eddy and loop currents that will lower the peak Q-factor. Apart from other metal layers the bonding pads will also affect inductor performance and C4 solder ball contacts should be spaced at least 110 µm from the spiral and wire bond pads at least 83 µm away to ensure a maximized Q-factor and self resonance frequency.

3.8 BOND PADS

The 8HP and 7WL processes support both wire bond pads as well as C4 pads for ball grid arrays. Wire bond pads were used in the implementation. The typical pad capacitance of the 8HP process is approximately 30 fF and that of the 7WL process approximately 35 fF.

3.9 CONCLUSION

This chapter provided an overview of the IBM 8HP and 7WL IC processes used in the simulation of the proposed circuits. The 7WL process was also used to fabricate a LNA to obtain experimental results as discussed in Chapters 5 through 7.

CHAPTER 4: MATHEMATICAL MODELLING

4.1 INTRODUCTION

The literature study presented in Chapter 2 concluded that a LC-ladder matched amplifier with capacitive shunt-shunt feedback could be a feasible means of implementing a wideband LNA that overcomes many of the shortcomings in existing LNA topologies. To characterise the performance of such a LNA extensive mathematical modelling of this proposed configuration was performed in order to quantify the performance measures important in LNA design [**61**], [**62**]. A RF analogue approach was used and the model consists of equations for input impedance, input return loss (S_{11}), forward gain (S_{21}) and NF, as well as an approximation of the IIP3 of the LNA. From this model compact design equations were also derived. The above derivations are presented in this chapter. All mathematical modelling for the research has been done using MATLAB[4].

The simple high frequency small-signal transistor model was used in the derivation and proved to be sufficient for a first order design when calculations were compared to simulation results. In the noise analysis only base resistance thermal noise, and base- and collector current shot noise were considered since flicker noise is negligible above 1 GHz and it was assumed that the base-collector voltage would be small enough to limit avalanche noise. Finally, inductors were modelled consisting of a series inductance and frequency dependent series resistance derived from the inductor Q-factor which was assumed constant over frequency within the band of interest.

4.2 INPUT MATCHING

Since it remains common practice to use a 50 Ω characteristic impedance in RF circuit and antenna design it is required that the LNA have a 50 Ω input impedance (or at least S_{11} < -10 dB) over the entire frequency band. To achieve this wideband operation a fourth order LC-ladder filter is used which allows the realization of an arbitrary wide matched bandwidth [**11**]. This is combined with the capacitive shunt-shunt feedback technique [**12**], [**45**] which is used to synthesize the resistance and capacitance of the series RLC part of the LC-ladder circuit. The circuit diagram of this configuration is shown in Figure 4.1.

[4] www.mathworks.com

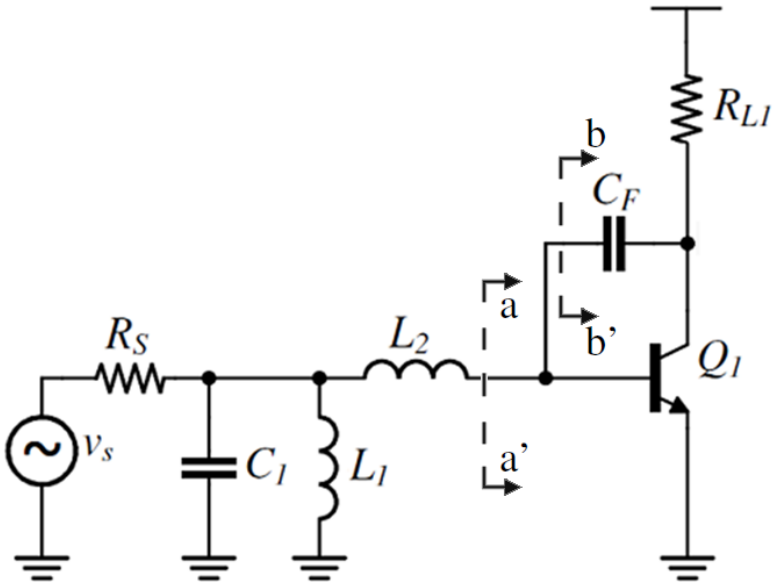

Figure 4.1. Schematic of the LC-ladder and capacitive shunt-shunt feedback input matching topology.

4.2.1 LC-ladder network

The LC-ladder consists of four reactive elements shown in Figure 4.2 where C_2 and L_1 determine the lower corner frequency of the matched band and C_1 and L_2 the upper corner frequency. The design of such a network was discussed in Section 2.5.5 and is repeated here for convenience. The appropriate values for these components are given by [**11**]

$$L_1 \approx \frac{R_S}{2\pi f_L} \quad and \quad C_2 \approx \frac{1}{2\pi f_L R_S} \tag{4.1a}$$

$$L_2 \approx \frac{R_S}{2\pi f_H} \quad and \quad C_1 \approx \frac{1}{2\pi f_H R_S} \tag{4.1b}$$

where R_S is the source resistance and f_L and f_H the lower and upper corner frequencies of the matched bandwidth respectively.

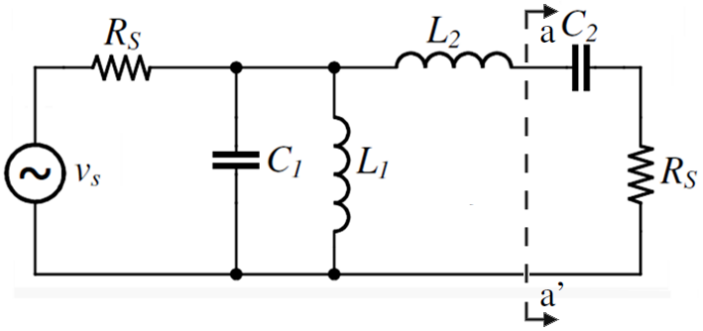

Figure 4.2. Schematic of a fourth order LC-ladder filter [11].

A benefit of using this configuration is that it takes advantage of what would in many cases be regarded as unwanted parasitic components and incorporates them into the matching network. The shunt capacitor C_1 can be implemented as the pad capacitance and in fact often requires an additional MIM capacitor in parallel to attain the required capacitance, thus there is no limitation due to the input pad. The shunt inductor L_1 can in turn be used as the DC bias choke, thus saving one extra on-chip inductor or the need for using an off-chip choke.

The series inductor L_2 is usually relatively small and implemented as a spiral inductor or transmission line depending on the frequency band. The series capacitor C_2 as well as the 50 Ω load resistance is derived from the transistor input impedance as seen when comparing the schematics in Figure 4.1 and Figure 4.2 along the line a-a'.

4.2.2 Capacitive feedback Miller impedance

The use of capacitive feedback to generate a series RC circuit for matching purposes was introduced in [**12**] as discussed in Section 2.5.4. The equations they provide can be verified using the small-signal circuit looking into the feedback capacitor C_F, and neglecting r_b. This is shown in Figure 4.3, where line b-b' has reference to Figure 4.1.

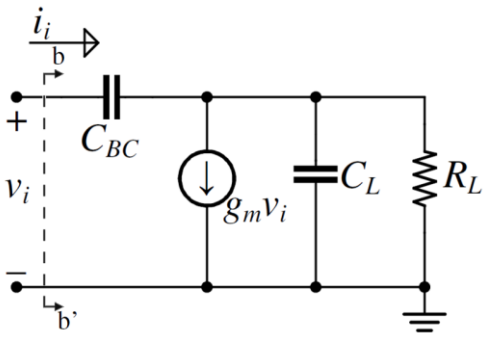

Figure 4.3. Small-signal equivalent of the capacitive feedback circuit when looking into the feedback capacitor.

The input voltage can be written in terms of the input current as

$$v_i = (i_i - g_m v_i)\left(R_L \left\| \frac{1}{j\omega C_L}\right.\right) + i_i \frac{1}{j\omega C_{BC}}. \tag{4.2}$$

Solving for v_i/i_i results in

$$\begin{aligned}\frac{v_i}{i_i} &= \frac{\dfrac{R_L}{1+j\omega R_L C_L} + \dfrac{1}{j\omega C_{BC}}}{1+g_m\left(\dfrac{R_L}{1+j\omega R_L C_L}\right)}, \\ &= \frac{R_L + \dfrac{1+j\omega R_L C_L}{j\omega C_{BC}}}{1+g_m R_L + j\omega R_L C_L}\end{aligned} \tag{4.3}$$

which when applying the approximation $(1 + g_m R_L) >> |\omega R_L C_L|$ in the denominator, which is usually the case, becomes

$$Z_M = \underbrace{\frac{1}{j\omega C_{BC}(1+g_m R_L)}}_{C_M} + \underbrace{\frac{R_L}{1+g_m R_L}\left(1+\frac{C_L}{C_{BC}}\right)}_{R_M}. \tag{4.4}$$

The resulting equivalent circuit at the input of the transistor is thus as shown in Figure 4.4.

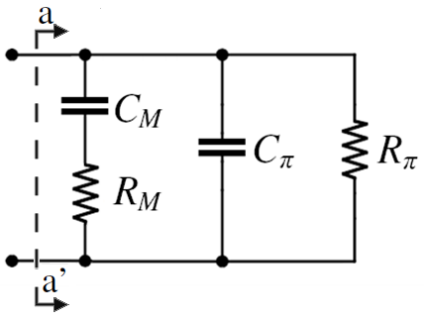

Figure 4.4. Equivalent circuit at the base of the transistor.

Using a successive series-to-parallel and then parallel-to-series transformation of R_M, while combining C_M and C_π, and neglecting R_π which is much larger than R_M results in

$$R_{M,p} = \frac{1}{\omega^2 C_M^2 R_M} \quad and \quad R_{IN} = \frac{1}{\omega^2 (C_\pi + C_M)^2 R_{M,p}}, \qquad (4.5)$$
$$\Rightarrow \quad R_{IN} = \frac{C_M^2}{(C_\pi + C_M)^2} R_M$$

and thus the input impedance is defined as the series combination of

$$\begin{aligned} C_{IN} &= C_\pi + C_M \\ &= C_\pi + (1 + g_m R_L)(C_\mu + C_F) \end{aligned} \qquad (4.6)$$

and

$$\begin{aligned} R_{IN} &= \frac{R_L}{(1 + g_m R_L)} \left(1 + \frac{C_L}{C_{BC}}\right) \left(\frac{C_M}{C_\pi + C_M}\right)^2 \\ &\approx \frac{1}{g_m} \left(1 + \frac{C_L}{C_{BC}}\right) \end{aligned} . \qquad (4.7)$$

Although the conversions in (4.5) use the *Q*-factor of the capacitor which may change with frequency, conversion first to parallel and then back to series causes the *Q*-factor to cancel and thus the matching remains constant with frequency. The simplification in (4.7) also shows that the result of the conversion only has a small influence on the equivalent resistance since C_M is usually much larger than C_π.

4.2.3 Input reflection coefficient

With this configuration based on LC-ladder filter theory it is possible, by designing for R_{IN} = 50 Ω and $C_{IN} = C_2$, to obtain a 50 Ω input impedance over an arbitrary frequency band. The input reflection coefficient from the definition of S_{11} is then

$$S_{11} = \frac{Z_{IN} - R_S}{Z_{IN} + R_S}, \qquad (4.8a)$$

where Z_{IN} is defined as

$$Z_{IN} = j\omega L_1 \left\| \frac{1}{j\omega C_1} \right\| \left(j\omega L_2 + \frac{1}{j\omega C_{IN}} + R_{IN} \right). \qquad (4.8b)$$

4.2.4 Comparison to the inductively degenerated LC-ladder technique

The LC-ladder matching technique combined with an emitter degenerated transistor as discussed in Section 2.5.5 had the disadvantage of introducing a pole at the lower corner frequency of the matched bandwidth, causing a -20 dB per decade roll-off in the base-emitter voltage as shown in (2.36) which has to be corrected by using an inductive load.

Since the emitter inductor is used to synthesize the series resistance, v_{be} is the voltage being evoked by the input current across the capacitor in the equivalent series RLC circuit which is the base-emitter capacitance C_π. The roll-off is due to the decreasing impedance of the capacitor with frequency.

In contrast, this roll-off is not present when combining the LC-ladder with capacitive feedback. In this case v_{be} is the voltage evoked across the input impedance of the transistor which includes both the capacitor and the resistor in the equivalent RLC circuit. When the current flowing into the transistor is approximated as $v_S/(2R_S)$ over the band of interest as before, the voltage over the v_{be} junction now becomes

$$\begin{aligned} v_{be} &= \frac{v_s}{2R_s}\left(R_s + \frac{1}{j\omega C_2}\right) \\ &= \frac{v_s}{2}\left(\frac{j\omega R_s C_2 + 1}{j\omega R_s C_2}\right) \\ &= \frac{v_s}{2}\left(\frac{j\frac{\omega}{\omega_L} + 1}{j\frac{\omega}{\omega_L}}\right) \end{aligned} \quad . \tag{4.9}$$

Thus the base-emitter voltage is a decreasing function at -20 dB per decade from infinity to a corner at -6 dB at the lower cut-off frequency, from where the zero results in a constant voltage drop over the base-emitter junction with frequency.

4.3 GAIN EQUATIONS

4.3.1 Input matching network gain

To determine the gain of the input matching network a Norton and Thévenin equivalent transformation can be used to move the source voltage in series with the rest of the RLC circuit at the transistor input. To this end the impedances

$$Z_1 = R_{L1} + j\omega L_1 \tag{4.10a}$$

$$Z_2 = R_{L2} + j\omega L_2 \tag{4.10b}$$

were defined where L_1 and L_2 are the inductors in the LC-ladder network, and R_{L1} and R_{L2} the associated parasitic series resistance; as well as

$$Z_s = \frac{1}{\frac{1}{R_s} + \frac{1}{R_{L1} + j\omega L_1} + j\omega C_1} \tag{4.11}$$

which is the parallel combination of R_S, L_1 and C_1.

A Norton equivalent transformation of v_s and R_S to find i_s and then a Thévenin transformation with i_s and Z_S results in the series source voltage

$$v_{s,eq} = \frac{Z_s}{R_s} v_s \tag{4.12}$$

and source impedance of Z_S. The voltage gain of the input matching network can then be defined as

$$A_{v,in} = \frac{Z_s}{R_s} \cdot \frac{Z_{T,IN}}{Z_s + Z_2 + Z_{T,IN}}, \tag{4.13}$$

where $Z_{T,IN}$ is the impedance at the base of the transistor derived from (4.6) and (4.7) as

$$Z_{T,IN} = R_{IN} + \frac{1}{j\omega C_{IN}}. \tag{4.14}$$

4.3.2 First stage gain

Since the first amplifier stage is a common-emitter configuration without emitter feedback the voltage gain is defined as

$$A_{v,1} = G_{M1} \cdot Z_{L1} \tag{4.15}$$

with G_{M1} the transconductance gain and Z_{L1} the load impedance. From inspection of Figure 4.1 the transconductance and load impedance are given respectively by

$$G_{M1} = g_m - j\omega C_{BC} \tag{4.16a}$$

$$\begin{aligned} Z_{L1} &= R_L \| \frac{1}{j\omega(C_{BC} + C_L)} \\ &= \frac{R_L}{1 + j\omega R_L (C_{BC} + C_L)} \end{aligned} . \tag{4.16b}$$

Several factors make this gain frequency dependent. The relatively large feedback capacitance, typically 85 fF < C_{BC} < 150 fF, causes the feedback factor to increase as the impedance of the capacitor decreases with frequency, thus decreasing the transconductance gain. However this effect is often negligible since a typical collector current of 1.5 mA with typical a feedback capacitor value of 100 fF and a 100 Ω load results in only a 2 dB drop in voltage gain from 1 GHz to 20 GHz.

A more important consideration is the output pole of the amplifier. The transfer function of the input matching network has been shown to be approximately constant over the band of interest and thus there is a single dominant pole at the output of the amplifier given by

$$\omega_{Po} = \frac{1}{R_L (C_{BC} + C_L)} . \tag{4.17}$$

Due to the increased capacitance with the addition of the feedback capacitor as well as the relatively large R_L required for large gain the pole is often within the band of interest resulting in a -20 dB per decade roll-off in the frequency response of the gain.

Even if this is not the case, the gain-bandwidth product (GBP) or f_T of the transistor will often not allow large gain for operation up to frequencies as high as 20 GHz. Even though further gain can be provided by subsequent stages the value of C_F affects the NF at the high frequency end and as such high gain in the first stage is desirable to minimize this value. If the gain is higher than f_T/f_H there will be a -20 dB per decade roll-off of gain regardless of the position of the output pole.

4.3.3 Second stage gain and gain flattening

To equalize the gain of the amplifier and compensate for the gain roll-off of the first amplifier stage which is often present as discussed above an inductive load can be used to provide peaking at high frequencies. Since a second amplifier stage is usually required to realize the desired gain at high frequencies, the inductive load can be used in the second stage to not add additional complexity to the mathematical model of the first stage from which the design equations are derived. Where necessary this peaking can be limited by also including a resistor in parallel with the inductive load. The schematic of the second stage is included in Figure 4.5.

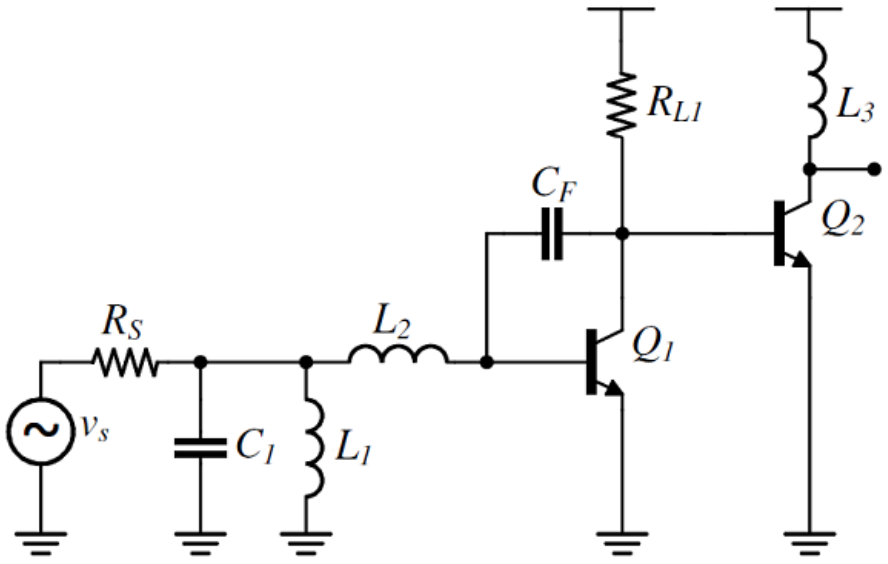

Figure 4.5. Schematic of the LNA including the second amplifier stage used to generate a zero in the frequency response for pole-zero cancellation.

The gain of the second stage is given by

$$A_{v,2} = G_{M2} \cdot Z_{L2} \tag{4.18}$$

where G_{M2} is simply the transconductance gain of the transistor, g_{m2}, and the load impedance is given by

$$Z_{L2} = j\omega L_3 . \tag{4.19}$$

The overall gain of the LNA is then

$$A_{v,T} = A_{v,in} \cdot A_{v,1} \cdot A_{v,2} \tag{4.20}$$

and can be expressed in terms of the scattering parameter S_{21} as

$$S_{21} = 2A_{v,in} \frac{(g_{m1} - j\omega C_{BC})R_{L1} \cdot (j\omega L_3 g_{m2})}{1 + j\omega R_{L1}(C_{BC} + C_{L1})} . \tag{4.21}$$

Since the frequency dependence of the first stage transconductance can usually be neglected, a flat wideband gain response can be achieved by the cancellation of the pole and zero in the equation. The bandwidth of the amplifier is then determined solely by the gain of the input matching network, $A_{v,in}$.

4.3.4 Further gain stages

The LNA configuration of Figure 4.5 provides wideband conjugate input matching as well as gain with a flat frequency response. Depending on the transistor process that is used it might however not be possible to achieve the desired gain specification. In such a case additional common-emitter stages employing resistive loads may be added to increase the overall gain further [**62**].

4.4 LNA DESIGN EQUATIONS

From the equations discussed thus far it is possible to derive compact design equations for a LNA using this configuration for a given frequency band and gain specification [**62**].

The design of the first stage entails selection of the LC-ladder components, the collector current of Q_1, the load resistance R_{L1} and the feedback capacitance C_F. The equivalent resistance at the base of the transistor is also affected by C_{L1}, but the value of this

capacitance should always be minimized to maximize the output pole frequency discussed in Section 4.3.2, and as such is not available for setting the input resistance.

The frequency specification for the LNA is met through selection of the reactive elements in the LC-ladder input matching network, and these values are determined using (4.1a) and (4.1b).

With the bandwidth determined, the voltage gain of the first stage should be selected, ideally as f_T/f_H to achieve the maximum gain up to the upper corner frequency f_H. Once this value of $A_{v,1}$ is selected the feedback capacitance required to synthesize C_2 can be determined by rewriting (4.6) as

$$C_F = \frac{C_2 - C_{\pi 1}}{1 + A_{v,1}} - C_{\mu 1}, \tag{4.22}$$

where A_{v1} has been approximated as $g_{m1}R_{L1}$.

The input resistance of the first stage, which should be equal to 50 Ω to provide proper matching, has been defined in (4.7). If $g_{m1}R_{L1} >> 1$, which is usually the case, this equation can be simplified to

$$R_{IN} \approx \frac{1}{g_{m1}}\left(1 + \frac{C_L}{C_{BC}}\right), \tag{4.23}$$

when also noting that C_M is usually in the hundreds of femtofarads or even the picofarad range while C_π is a few tens of femtofarads and thus $C_M + C_\pi \approx C_M$.

Once the load capacitance is determined, being the total node capacitance at the output excluding C_F, the value of I_{C1} can be derived from (4.23) as

$$I_{C1} \approx \left(1 + \frac{C_L}{C_{BC}}\right)\frac{V_T}{R_S}. \tag{4.24}$$

While C_L would usually be much smaller than C_{BC} resulting in the familiar $I_{C1} \approx g_m V_T$ the load capacitance can be increased to maintain the desired input matching even when I_{C1}

has been increased to improve the noise performance (see Section 5.3.2) which makes the ratio of the capacitances significant.

Finally the value of R_{L1} is derived from the selected voltage gain and collector current as

$$R_{L1} = A_{v,1} \frac{V_T}{I_{C1}}. \tag{4.25}$$

In the design of the second amplifier stage there is more freedom in the selection of the collector current and the load inductance L_3. Once the gain required at the upper corner frequency has been determined, which is the deficit in gain between the upper and lower corner of the first stage, this can be substituted in (4.18) along with ω_H. The value of L_3, and thus chip area, can then be traded with the collector current, which translates to power consumption, in order to achieve this gain.

4.5 INPUT MATCHING MODELLING IMPROVEMENT

The impedance seen at the base of the transistor has been defined in (4.14) based on the input resistance and capacitance from (4.6) and (4.7) respectively derived from the small-signal analysis of the circuit in Figure 4.3. However when the calculated and simulated input reflection coefficients were compared it was found that they do not track each other sufficiently. This is due to the simple case of a constant load resistance and capacitance being used in the derivation of the transistor input impedance, where the inductive load of the second stage in fact results in a second order equation for load impedance [**63**].

The input impedance of the second stage is defined as

$$Z_{IN,2} = R_{\pi 2} \left\| \frac{1}{j\omega C_{\pi 2}} \right\| Z_{M2}, \tag{4.26}$$

where Z_{M2} is the Miller impedance, and using the Miller theorem $Y_{IN,2}$ can be written as

$$\begin{aligned} Y_{IN,2} &= \frac{1}{R_\pi} + j\omega\left[C_\pi + C_\mu\left(1 - A_{v,2}\right)\right] \\ &= \frac{1}{R_\pi} + j\omega\left[C_\pi + C_\mu\left(1 + j\omega L_3 g_{m2}\right)\right]. \\ &= \frac{1}{R_\pi} + j\omega\left(C_\pi + C_\mu\right) - \omega^2 g_{m2} L_3 C_\mu \end{aligned} \tag{4.27}$$

Thus the load impedance of the first stage, Z_{L1}, should instead be defined as

$$Z_{L1} = R_{L1} \left\| Z_{IN,2} \right\| \frac{1}{j\omega\left(C_{BC} + C_L\right)}. \tag{4.28}$$

The same small-signal derivation can then be used to define the first stage input impedance more accurately by replacing R_L and C_L in Figure 4.3 with Z_{L1} which results in

$$\begin{aligned} v_i &= \left(i_i - g_m v_i\right) Z_{L1} + i_i \frac{1}{j\omega C_{BC}} \\ \Rightarrow \quad Z_{T,IN} &= \frac{Z_{L1} + \dfrac{1}{j\omega C_{BC}}}{1 + g_m Z_{L1}} \end{aligned} . \tag{4.29}$$

Although the simple case is sufficient and convenient in the initial design, the derivation of $Z_{T,IN}$ in (4.29) should be used in (4.13) to determine the gain of the input matching network, and Z_{L1} in (4.28) should also be used to calculate the first stage gain in (4.15). This leads to the calculated results tracking simulation results sufficiently.

4.6 NOISE FIGURE DERIVATION

As mentioned in Section 2.3.3 NF can either be expressed in terms of a deviation from the minimum NF of a transistor according to the deviation of the source impedance from the optimal noise impedance, which is often used in a distributed design, or an equation incorporating the noise from all the various noise sources in the circuit can be derived. Since the LNA topology in question is designed using a lumped element or RF analogue approach the latter option is more suited in this case, and it will also be shown that important insights regarding optimization for low noise can be gleaned from the derived NF equation which would not be as obvious if a distributed design approach was followed.

4.6.1 Noise sources

The schematic in Figure 4.6 includes all the noise sources of the first amplifier stage. The parasitic resistances of the inductors are given by

$$R_x = \frac{\omega L_x}{Q_x}, \tag{4.30}$$

where Q_x is the quality factor of the passive on-chip inductor and the subscript denotes the inductor in question. The thermal noise contributed by these parasitic resistors, the transistor base resistance r_b, as well as the noise from the source resistance is determined by (2.2a). The transistor current noise sources i_B and i_C are both due to shot noise and given by (2.3).

Although the NF equation could be derived directly from this circuit, the analysis is complicated by the presence of the feedback capacitance as well as the R_S and R_1 noise sources which form part of the parallel RLC circuit. Thus there is no convenient way to translate all the noise sources to the input necessitating certain transformations to a more suitable equivalent circuit.

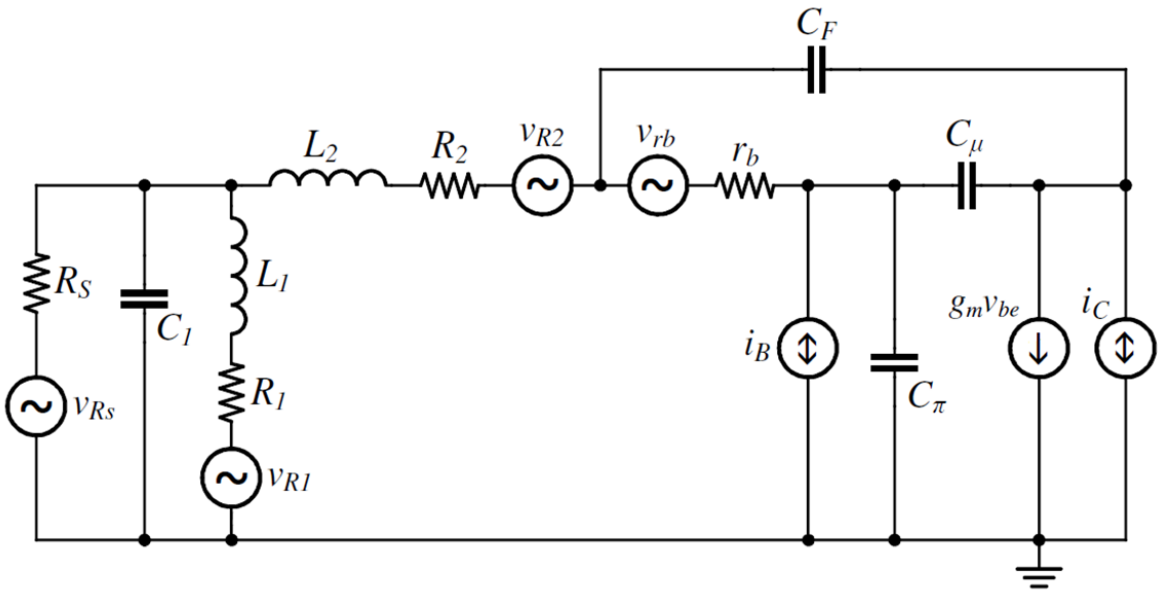

Figure 4.6. Equivalent circuit of the first amplification stage showing parasitic components and noise sources.

4.6.2 Simplifying the circuit

The first simplification that can be made is viewing the transistor as a noise free amplifier with the well known equivalent common-emitter noise generators given by [**29**] and (2.15):

$$\begin{aligned}\overline{v_{CE}^2} &= 4kTr_b + \frac{2qI_C}{g_m^2} + \frac{2qI_C}{\beta_0}\cdot r_b^2 \\ &\approx 4kTr_b + \frac{2qI_C}{g_m^2}\end{aligned}, \tag{4.31}$$

$$\begin{aligned}\overline{i_{CE}^2} &= \frac{2qI_C}{\beta_0} + \frac{2qI_C}{\beta_{RF}^2} \\ &= 2qI_C\left(\frac{1}{\beta_0} + \left(\frac{\omega(C_\pi + C_\mu)}{g_m}\right)^2\right).\end{aligned} \tag{4.32}$$

The shunt-shunt feedback due to the capacitor has no effect on the noise voltage of the transistor, however v_{CE} induces an additional noise current in the feedback network [**26**] which results in the final equivalent noise generators at the base of the noise free amplifier being defined as

$$\overline{v_{EQ}^2} \approx \overline{v_{CE}^2}, \tag{4.33}$$

$$\overline{i_{EQ}^2} \approx \overline{i_{CE}^2} + \left(\omega^2 C_F^2\right)\overline{v_{CE}^2}. \tag{4.34}$$

The schematic can then be redrawn as in Figure 4.7. In this schematic the source noise generator and the noise generator of the L_1 parasitic resistance has also been moved in series with the various impedances and other noise voltage sources. This was done by first using a Norton and then Thévenin transformation on respectively v_{RS}, R_S and Z_S, as well as v_{R1}, Z_1 and Z_S, with Z_1 defined in (4.10a). Thus the PSD of the equivalent noise generators are given by

$$\overline{v_{RS,eq}^2} = \frac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2} \quad \text{and} \quad \overline{v_{R1,eq}^2} = \frac{|Z_S|^2}{|Z_1|^2}\overline{v_{R1}^2}. \tag{4.35}$$

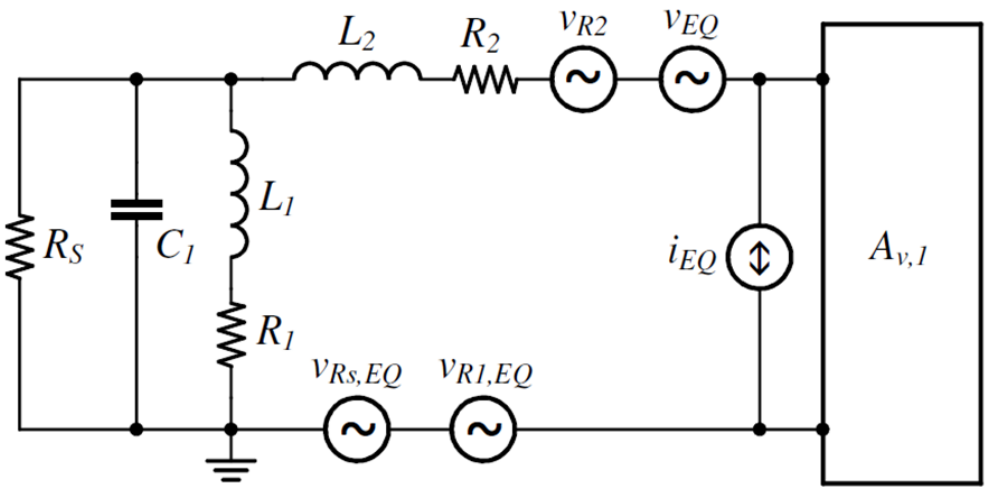

Figure 4.7. Equivalent circuit of the first amplification stage redrawn to allow convenient NF derivation.

4.6.3 Noise figure equation derivation

The NF can be conveniently derived from the circuit in Figure 4.7 by first expressing the noise voltage generated over the v_{be} junction of the transistor by each noise generator. In Figure 4.7 this is the voltage over the input terminals of the noise free amplifier. The input impedance of the amplifier is the input impedance of the transistor in parallel with C_F since the output of the amplifier is shorted to ground in the definition of NF.

It has already been shown in Section 2.5.2 that R_π becomes negligible compared to C_π in the SHF range. Thus the input impedance of the transistor is the base resistance in series with the total input capacitance $C_i = C_\pi + C_\mu$. As the impedance of C_i drops at high frequencies a greater portion of the input voltage will fall across r_b decreasing the voltage gain by introducing a pole as seen from

$$v_{be}^{'} = \frac{1/j\omega C_i}{r_b + 1/j\omega C_i} = \frac{1}{1 + j\omega C_i r_b}. \tag{4.36}$$

However for a typical C_i of 100 fF and a base resistance of less than 50 Ω this pole is above 30 GHz and as such r_b can be neglected, resulting in an input impedance consisting simply of the total input capacitance of the amplifier which is

$$C_T = C_\pi + C_\mu + C_F . \tag{4.37}$$

Using a simple voltage divider equation the noise PSD at the v_{be} junction contributed by each voltage noise generator is then defined as

$$\overline{v_{\pi,Veq}^2} = \left| \frac{\frac{1}{j\omega C_T}}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{v_{EQ}^2} , \tag{4.38a}$$

$$\overline{v_{\pi,RL2}^2} = \left| \frac{\frac{1}{j\omega C_T}}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{v_{RL2}^2} , \tag{4.38b}$$

$$\overline{v_{\pi,RL1}^2} = \frac{|Z_s|^2}{|Z_1|^2} \left| \frac{\frac{1}{j\omega C_T}}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{v_{RL1}^2} , \tag{4.38c}$$

and

$$\overline{v_{\pi,RS}^2} = \frac{|Z_s|^2}{R_s^2} \left| \frac{\frac{1}{j\omega C_T}}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{v_{RS}^2} . \tag{4.38d}$$

The voltage noise contribution of the current noise generator is the product of the current noise PSD and the impedance seen by this source, namely the parallel combination of the amplifier input impedance and the matching network, given by

$$\begin{aligned} \overline{v_{\pi,Ieq}^2} &= \left| \frac{1}{j\omega C_T} \middle\| \left(Z_s + Z_2\right) \right|^2 \overline{i_{EQ}^2} \\ &= \left| \frac{\frac{1}{j\omega C_T}\left(Z_s + Z_2\right)}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{i_{EQ}^2} . \end{aligned} \tag{4.39}$$

Z_2 and Z_S has been defined in (4.10b) and (4.11) respectively.

The noise factor of the first stage can now be defined as

$$F_1 = \frac{\overline{v_{\pi,Veq}^2} + \overline{v_{\pi,Ieq}^2} + \overline{v_{\pi,R1}^2} + \overline{v_{\pi,R2}^2} + \overline{v_{\pi,RS}^2}}{\overline{v_{\pi,RS}^2}}, \tag{4.40}$$

and with the substitution of (4.38a–d) and (4.39), as well as (4.33) and (4.34) the noise factor becomes

$$\begin{aligned} F_1 &= \frac{\overline{v_{EQ}^2} + |Z_S + Z_2|^2 \overline{i_{EQ}^2} + \frac{|Z_S|^2}{|Z_1|^2}\overline{v_{R1}^2} + \overline{v_{R2}^2} + \frac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2}}{\frac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2}} \\ &= 1 + \frac{\overline{v_{CE}^2} + |Z_S + Z_2|^2\left[\overline{i_{CE}^2} + |\omega C_F|^2 \overline{v_{CE}^2}\right] + \frac{|Z_S|^2}{|Z_1|^2}\overline{v_{R1}^2} + \overline{v_{R2}^2}}{\frac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2}} \end{aligned}. \tag{4.41}$$

The NF is simply defined as the noise factor expressed in dB [**29**] and thus becomes

$$NF_1 = 10\log F_1. \tag{4.42}$$

4.7 IMPROVING NOISE FIGURE AND GAIN

From (4.41) it is seen that the NF is to a large extent determined by passive components that make up the matching network and first amplifier stage. Therefore reducing the NF would entail optimizing these component values, but from the design steps given in Section 4.4 there is apparently little freedom in this selection. However this is not entirely the case.

The primary concern when changing the component values in the matching network is that the S_{11} specification would no longer be met; however, solving the standard definition of S_{11} in (4.8a), with a 50 Ω source resistance, it is found that the input impedance can vary from 26 Ω to 96 Ω while still maintaining S_{11} < -10 dB. This allows for some freedom in

the selection of these component values. In addition, since there is a strong interaction between the reactive elements the effects of these changes tend to cancel one another.

This makes it possible to optimize the performance of the LNA by modifying the passive component values through simulation after the initial design is completed [**13**].

4.7.1 Noise figure improvement

In order to improve the NF it is valuable to know which of the noise generators dominate the overall NF. To this end (4.41) can be rewritten as

$$F_1 = \frac{\left(1+\left|Z_S+Z_2\right|^2\cdot\left|\omega C_F\right|^2\right)\overline{v_{CE}^2}+\left|Z_S+Z_2\right|^2\overline{i_{CE}^2}+\left|\frac{Z_S}{Z_1}\right|^2\overline{v_{R1}^2}+\overline{v_{R2}^2}+\left|\frac{Z_S}{R_S}\right|^2\overline{v_{RS}^2}}{\left|\frac{Z_S}{R_S}\right|^2\overline{v_{RS}^2}}. \quad (4.43)$$

Inspection of the numerator of (4.43) shows that each noise generator in Figure 4.7 is present only once and each as a separate term with a coefficient comprised of the matching network passive components. Thus it is possible to plot each noise contribution separately and thus determine the dominant contributor. Such a plot is shown in Figure 4.8, which also includes the noise contribution of the second amplifier stage.

To derive this contribution it is convenient to calculate the total current noise at the input of the second stage, since the first transistor is treated as a transconductance amplifier, and then divide that by the transconductance gain of the first stage to get the equivalent voltage noise at the base of the first transistor. The noise generators of the second stage are the first stage load resistance thermal noise PSD as defined in (2.2b), the common-emitter current noise, and the current noise PSD evoked in the equivalent admittance seen by the common-emitter voltage noise generator as show in

$$n_{A2} = \frac{\overline{i_{RL1}^2}+\overline{i_{CE2}^2}+\overline{v_{CE2}^2}\cdot\left|1/R_{L1}+j\omega(C_{BC}+C_{IN2})\right|^2}{\left|G_{M1}\right|^2}. \quad (4.44)$$

The dominant noise generator was found to be the common-emitter voltage noise and as such minimizing this contribution has priority. To determine how this can be achieved the noise factor equation in (4.43) can be rewritten again to obtain

$$F_1 = \left[\left(\frac{1}{|Z_S|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \cdot |\omega C_F|^2 \right) \overline{v_{CE}^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \overline{i_{CE}^2} + \frac{\overline{v_{R1}^2}}{|Z_1|^2} + \frac{\overline{v_{R2}^2}}{|Z_S|^2} + \frac{\overline{v_{RS}^2}}{R_S^2} \right] \cdot \frac{R_S^2}{\overline{v_{RS}^2}}, \quad (4.45)$$

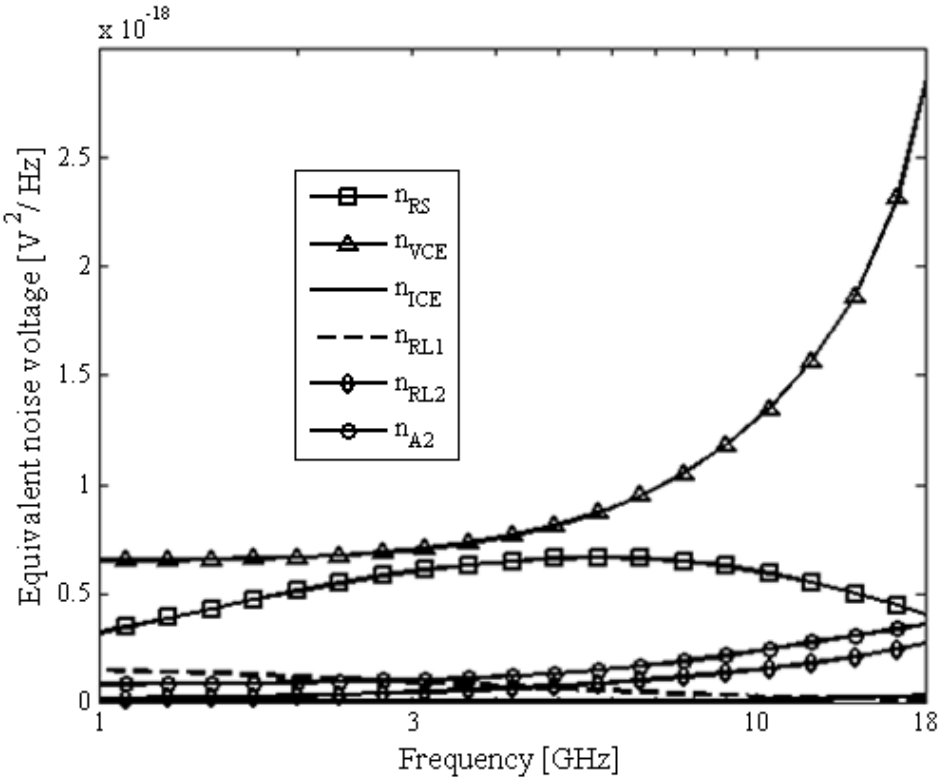

Figure 4.8. Noise PSD contribution of the individual noise generators versus frequency over the 800 MHz to 18 GHz band.

where only the fixed R_S and subsequently fixed v_{RS} is not included in the individual coefficients. The CE voltage noise contribution can then be minimized by minimizing

$$\begin{aligned} n_{Vce} &= \left(\frac{1}{|Z_S|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \cdot |\omega C_F|^2 \right) \frac{\overline{v_{CE}^2}}{\overline{v_{RS}^2}} \cdot R_S^2 \\ &= \left(\frac{1}{|Z_S|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \cdot |\omega C_F|^2 \right) \left(\frac{4kTr_b + 2qI_C / g_m^2}{4kTR_S} \right) \cdot R_S^2, \\ &= \left(\frac{1}{|Z_s|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \cdot |\omega C_F|^2 \right) \left(r_b + \frac{V_T}{2I_C} \right) \cdot R_S \end{aligned} \quad (4.46)$$

where (4.31) has been substituted for the CE voltage noise PSD.

Figure 4.8 also shows that the inductors in the input matching network, L_1 and L_2, contribute somewhat at the low and high frequency end respectively, while the amplifier current noise and the second stage practically makes no contribution.

Thus to minimize the NF of the LNA according to (4.46), and in fact throughout (4.45), Z_S should be minimized. From (4.11) this implies increasing L_1 and decreasing C_1. Increasing L_1 will also decrease the contribution of the parasitic resistance of this inductor as seen from

$$\begin{aligned} n_{RL1} &= \frac{1}{|Z_1|^2}\frac{\overline{v_{R1}^2}}{v_{RS}^2}R_S^2 \\ &= \frac{1}{|R_1 + j\omega L_1|^2}\frac{R_1}{R_S}R_S^2 \\ &= \frac{R_1}{R_1^2 + \omega^2 L_1^2}R_S \\ &= \frac{\omega L_1/Q_1}{\omega^2 L_1^2/Q_1 + \omega^2 L_1^2}R_S \\ &= \frac{R_S}{\omega L_1(1+Q_1)} \end{aligned} \quad . \tag{4.47}$$

Decreasing L_2 will decrease (4.46) through Z_2, as well as the contribution from the CE current PSD, and will also decrease R_2 and subsequently its noise PSD.

The final passive component found in (4.46) is the feedback capacitor C_F which causes the NF to increase rapidly at high frequencies and should thus be minimized. Since C_F is used to synthesize C_2 this would mean a decrease in the value of C_2 as well; but although some deviation in C_2 can be allowed, C_F often remains too large to achieve suitable performance at high frequencies. In such a case the gain of the first stage needs to be increased; the gain is however limited by the f_T of the transistor. Fortunately since an inductive load is used in the second stage the high frequency peaking provided by the inductor can compensate for the voltage roll-off of the first stage should the gain be increased above this limit, thus allowing smaller values of C_F to be used. Since C_2 determines the lower corner frequency of the LNA, the decrease in this Miller capacitance with the gain roll-off at high frequencies does not severely affect the input matching and although S_{11} is increased as a result, it can still be kept below -10 dB.

The transistor size and biasing also affects the NF through the second term of (4.46). It is clear that increasing the first stage collector current will decrease the CE voltage noise contribution. Although this may increase the CE current noise, Figure 4.8 indicates that this contribution is generally negligible and thus a small increase will not be significant. Maximizing the emitter length of the transistor will also minimize r_b. The large emitter length results in large C_π and C_μ parasitic capacitance, however since these are included in the design equations this will not be to the determent of the LNA performance and in fact merely results in a smaller feedback capacitance being required which is the desired case.

It has been noted in Section 4.2.2 that the collector current is used to determine the equivalent input resistance at the base of the transistor and as such increasing I_C to reduce noise will worsen input matching. The first stage load capacitance can however be increased to restore the input matching while also lowering the output pole of the first stage; however this is usually not a significant problem while the inductively loaded second stage can still equalize the voltage gain.

Figure 4.9 shows the noise contributions of the respective generators after the suggestions above have been applied to a typical LNA. The contribution of the parasitic resistance R_2 has been reduced by one third at the upper cut-off frequency and the contribution of R_1 is also somewhat reduced.

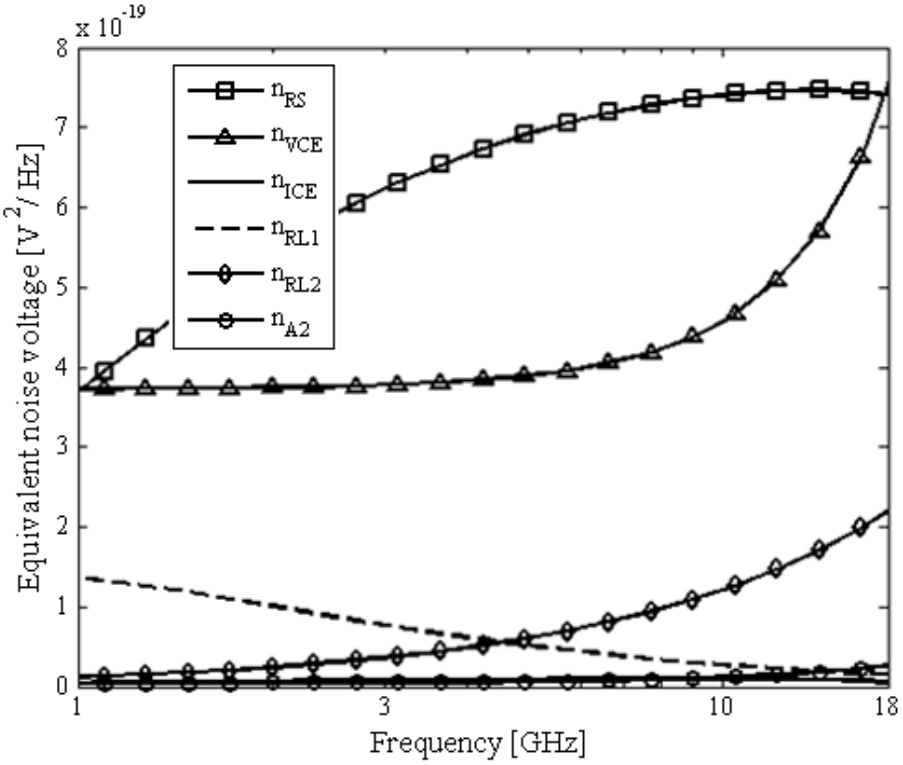

Figure 4.9. Noise PSD contribution of the individual noise generators versus frequency after optimization of the input matching network.

The transistor voltage noise contribution has been increased at high frequencies, however it can be seen that there is still a large improvement in NF resulting from the source resistance noise, and thus also the input signal, undergoing a larger gain through the matching network. This serves to improve the output signal-to-noise ratio which implies a lower NF.

4.7.2 Simultaneous gain improvement

The overall gain of the LNA has been defined in (4.21) and by also substituting (4.13) can be written as

$$S_{21} = \frac{2Z_S R_{L1}(R_S + 1/j\omega C_2)(g_{m1} - j\omega C_{BC})(j\omega L_3 g_{m2})}{R_S(Z_S + Z_2 + 1/j\omega C_2 + R_S)(1 + j\omega R_{L1}(C_{BC} + C_{L1}))}, \tag{4.48}$$

with $R_{IN} = R_S$ and $C_{IN} = C_2$.

Thus increasing the gain of the LNA would require decreasing L_2, C_2 and C_{BC} (and thus C_F) as well as increasing Z_S. These are the same requirements as for NF optimization discussed in Section 4.7.1. Furthermore, increasing I_{C1} to increase the gain will decrease

the NF as shown. This, as well as increasing the gain by increasing R_{L1}, will also both result in further reduction of the NF of the second stage improving the overall NF.

Thus with the LC-ladder and shunt-shunt capacitive feedback LNA configuration NF and gain can always be optimized simultaneously and there is no trade-off between these two performance measures.

4.8 LINEARITY APPROXIMATION

Although NF and gain can be quantified relatively well using small-signal analysis amplifier linearity, being a large signal phenomenon, is harder to evaluate. Section 2.4 discusses the use of a Volterra-series to analyze circuits operating in weak non-linearity, however the derivation of the Volterra-series is very laborious and offer little insight that cannot be gained through large signal circuit simulations. Therefore only an approximation that can be used as an initial estimate of the IIP3 is derived here.

The IIP3 voltage of a CE amplifier can be approximated as [**34**]

$$V_{IIP3(CE)} = 2\sqrt{2}V_T\,, \tag{4.49}$$

where V_T is the thermal voltage. Since the proposed LNA consists of two cascaded common-emitter stages in which the first stage acts as a pre-amplifier to the second stage, thus reducing the second stage IIP3 [**12**], the final IIP3 voltage of the LNA can be approximated as

$$\begin{aligned} V_{IIP3(LNA)} &\approx \frac{V_{IIP3(CE2)}}{A_{v,in}\cdot A_{v,1}}\,, \\ &\approx \frac{4\sqrt{2}V_T}{A_{v,1}} \end{aligned} \tag{4.50}$$

where $A_{v,in}$ is approximately equal to ½. Since the voltage gain of the first stage often rolls off within the band of interest this will cause a similar increase (improvement) of the IIP3.

The IIP3 can be expressed in dBm through

$$IIP3 \approx 10\log\left(\frac{16 \cdot V_T^2}{A_{v,1}^2 \cdot R_S} \cdot 10^3\right). \quad (4.51)$$

As discussed in Section 2.4 the linearity can be improved by employing feedback providing an improvement of approximately

$$V'_{IIP3(CE)} \approx V_{IIP3(CE)} \times (1 + A\beta)^{3/2}. \quad (4.52)$$

Such local feedback should be employed in the last amplifier stage since it dominates the IIP3 of the LNA. Local feedback in prior stages will also improve linearity by decreasing the gain of these stages and thus linearity can be traded for gain and NF.

Alternatively overall feedback can be used between the output and the first amplifier stage, however this greatly affects the input matching since feedback changes the input impedance. For example using series feedback in the emitter of the first stage increases the input impedance, thus requiring an increase in C_F to maintain the correct C_2 value for proper matching; however this is usually impossible to do while maintaining reasonable high frequency NF which increases with C_F.

It is suggested that the linearity of the initial LNA design is determined through simulation and subsequently optimized if desired using the techniques described in Section 2.4. The process that was followed in completing this research is discussed in Section 5.3.5 with the simulation results.

4.9 PERFORMANCE LIMITS AND TRADE-OFFS

Although the LC-ladder network can theoretically achieve a conjugate input match over an arbitrary bandwidth, two fundamental limits to the bandwidth of this LNA configuration can be identified, which leads to trade-offs with the other performance measures [**63**].

4.9.1 Noise figure vs. bandwidth

In Section 4.7.1 it has been shown that the common-emitter voltage noise of the first stage dominates the NF. From (4.46) it can be seen that the feedback capacitor C_F subsequently causes a sharp rise in NF at high frequencies due to the ωC_F term, as also shown in Figure 4.8. This increase in NF places a limit on the upper corner frequency ω_H for a given

maximum NF specification. It also follows that ω_H can be increased by decreasing C_F, provided no other frequency limitations are present.

The value of C_F is derived from the desired C_2 value using (4.22) after the gain of the first stage has been selected. The value of C_2 is in turn determined by the lower corner frequency ω_l through (4.1a), and a lower ω_l requires a larger C_2. This interdependence of ω_l and ω_u results in a fundamental limit on the bandwidth for a given maximum NF.

This noise figure-bandwidth trade-off can be quantified by substituting (4.1a) into an approximated version of (4.22), where C_2 is assumed much larger than $C_{\pi 1}$ and $A_{v,1}$ approximated as $g_{m1}R_{L1}$, giving

$$C_{BC} \approx \frac{1}{\omega_l R_S \left(1+g_{m1}R_{L1}\right)}. \tag{4.53}$$

Since the noise factor can be approximated using (4.46) as

$$F_1 \approx 1+\left(\frac{1}{\left|Z_s\right|^2}+\left|1+\frac{Z_2}{Z_S}\right|^2 \cdot \left|\omega C_{BC}\right|^2\right)\left(r_b+\frac{V_T}{2I_C}\right)\cdot R_S, \tag{4.54}$$

equation (4.53) can then be substituted to obtain the noise factor as a function of ω_l as

$$F_1 \approx 1+\left(\frac{1}{\left|Z_s\right|^2}+\left|1+\frac{Z_2}{Z_S}\right|^2 \cdot \left|\frac{\omega}{\omega_l R_S \left(1+g_{m1}R_{L1}\right)}\right|^2\right)\left(r_b+\frac{V_T}{2I_C}\right)\cdot R_S, \tag{4.55}$$

where $F_{1\max}$ and ω_u can be substituted and then solved for ω_l as

$$\omega_l \approx \left[\frac{R_S\left(1+g_m R_L\right)}{\omega}\sqrt{\left(\frac{\left(F_{1\max}-1\right)}{\left(r_b+\frac{V_T}{2I_C}\right)R_S}-\frac{1}{\left|Z_S\right|^2}\right)\div\left|1+\frac{Z_2}{Z_S}\right|^2}\right]^{-1}\Bigg|_{\omega=\omega_u}, \tag{4.56}$$

where Z_2 and Z_S are also frequency dependent as given in (4.10b) and (4.11) respectively. Since a change in ω_l will result in Z_S being modified through L_1 according to (4.1a), finding the correct solution for ω_l will be an iterative process.

It is however noticed that ω_l will decrease as $g_m R_L$ is increased, since C_2 is increased in this case without changing C_F. This means that this equation can also be used to determine the required low frequency first stage gain for a given frequency range and maximum NF specification when it is rewritten as

$$A_{v1} \approx g_m R_L \approx \left[R_S \frac{\omega_l}{\omega} \sqrt{\left(\frac{(F_{1\max} - 1)}{\left(r_b + \frac{V_T}{2I_C}\right) R_S} - \frac{1}{|Z_S|^2} \right) \div \left| 1 + \frac{Z_2}{Z_S} \right|^2} \right]^{-1} - 1 \Bigg|_{\omega=\omega_u} . \tag{4.57}$$

Since the thermal noise of the parasitic resistance of L_2 defined as

$$\begin{aligned} n_{RL2} &= \left| \frac{R_S}{Z_S} \right|^2 \frac{\overline{v_{R2}^2}}{\overline{v_{RS}^2}} = \left| \frac{R_S}{Z_S} \right|^2 \frac{R_2}{R_S} \\ &= \frac{R_2 R_S}{|Z_S|^2} \end{aligned} \tag{4.58}$$

also contributes somewhat to the NF at high frequencies according to Figure 4.8, the approximated noise factor equation in (4.55) can be modified to include this term, leading to more accurate results. The noise factor equation solved for ω_l then becomes

$$\omega_l \approx \left[\frac{R_S (1 + g_m R_L)}{\omega} \sqrt{\left(\frac{\left(F_{1\max} - 1 - R_2 R_S / |Z_S|^2\right)}{\left(r_b + \frac{V_T}{2I_C}\right) R_S} - \frac{1}{|Z_S|^2} \right) \div \left| 1 + \frac{Z_2}{Z_S} \right|^2} \right]^{-1} \Bigg|_{\omega=\omega_u} \tag{4.59}$$

4.9.2 Parasitic base-collector capacitance vs. lower corner frequency

Since there is a minimum base-collector feedback capacitance that can be implemented, which is the parasitic C_μ of the transistor without an additional C_F, it is apparent from (4.53) that there will be a maximum ω_l that can be achieved for a given first stage gain.

If the equation for C_2 in (4.1a) is written in terms of ω_l, and the equation for C_2 in (4.6) substituted with $C_{BC} = C_\mu$, the maximum lower corner frequency is given by

$$\omega_{l\max} = \frac{1}{R_S \left(C_{\pi 1} + C_{\mu 1} (1 + g_{m1} R_{L1}) \right)} . \tag{4.60}$$

With capacitances of $C_{\pi 1}$ = 25 fF and $C_{\mu 1}$ = 20 fF found in the 0.13 µm IBM 8HP process, and a first stage gain of 10 dB, the maximum lower corner frequency that can be achieved is approximately 30 GHz in a 50 Ω system.

By substituting $\omega_{l\max}$ and $C_{BC} = C_{\mu}$ in (4.59) and numerically solving for ω_u an associated maximum upper corner frequency can also be found.

It is possible to scale the transistor emitter length in order to reduce the parasitic capacitances of the transistor to make operation at higher frequencies more feasible; however the NF increases quite rapidly with increase in r_b since r_b is the dominating noise source in the system. Thus the NF vs. bandwidth trade-off remains as decreasing the emitter length to decrease capacitances will increase r_b.

4.10 LIMITS OF THE MODEL AND CONFIGURATION

Although the equations derived in the preceding sections do well to quantify the performance of this LNA topology and track simulations reasonably well, it remains a first order analysis which may cause results to deviate from those expected at very high frequencies. Some of the critical assumptions that were made as well as other factors that may be causes of such deviations at high frequency operation are discussed next [**64**].

4.10.1 Input matching approximation

The input impedance of the transistor as defined by C_{IN} and R_{IN} in (4.6) and (4.7) respectively is found by neglecting $j\omega R_{L1}C_{L1}$ when it is assumed that $(1 + g_{m1}R_{L1}) >> j\omega R_{L1}C_{L1}$. When the assumption no longer holds at high frequencies the $j\omega R_{L1}C_{L1}$ term should be included in the equation for the Miller impedance which is then found to be

$$Z_M = \frac{R_{L1}}{(1+ j\omega R_{L1}C_{L1} + g_{m1}R_{L1})} + \frac{1}{j\omega\left(C_{\pi 1} + C_{BC}\left(1+\frac{g_{m1}R_{L1}}{1+ j\omega R_{L1}C_{L1}}\right)\right)}. \qquad (4.61)$$

Equation (4.61) shows that in such a case C_2 will decrease with frequency as the voltage gain decreases due to the output pole of the first stage. The equivalent resistance also

becomes frequency dependent and will only appear resistive over a limited frequency band.

Although this will cause the calculated results to deviate from simulation, this problem can be avoided by using the more accurate equation for the transistor input impedance in (4.29) which does not rely on the said approximation.

4.10.2 Hybrid-π transistor model and assumptions with regards to parasitics

The simple high frequency small-signal transistor model was used in the derivations since it includes only the most essential parasitic components, resulting in easily comprehensible equations describing the circuit performance. While this is sufficient for a first order design the following additional important parasitic components/effects present in more advanced transistor models (see the HICUM [**60**] in Figure 3.2) are not taken into account:

- The presence of the series base and emitter resistances (r_b and r_e, respectively) were neglected in the *S*-parameter derivation.
- The degeneration due to the feedback afforded by r_e was also not taken into account.
- The typical parasitic capacitance values as given in the process datasheets were used as constants while these capacitances are in fact dependent on the collector current.
- The model assumes that the external C_F and parasitic C_μ can be added in parallel directly; the terminals of these capacitances are, however, separated by r_b and r_c, and C_μ is also distributed around the internal and external base series resistances (*rbi* and *rbx*).

The above effects will result in deviations from the predicted results and may to an extent be responsible for the measured gain, shown in Section 7.3, being much lower than expected.

4.10.3 Gain bandwidth product

It has been mentioned in Section 4.3.3 that the f_T of the first stage transistor often results in a gain roll-off at -20 dB/decade above a corner frequency within the band of interest. Although the design attempts to compensate for this roll-off through the inductive load of

the second stage which introduces a zero in the overall frequency response and thus, ideally, results in a flat voltage gain at the output, the second stage also has a finite f_T and as such cannot maintain a transfer function rising at +20 dB/decade at very high frequencies. Therefore the GBP remains a fundamental limit to the bandwidth that can be achieved while maintaining reasonable gain per stage.

4.10.4 Passive on-chip components

The most fundamental limit to the achievable frequency range is the available passive component values in a given transistor process.

All matching network components scale with inverse proportionality to corner frequency and as such the upper corner frequency, determined by L_2 and C_1, is limited by the minimum inductance and capacitance values that are available.

It would be possible to use parallel connected inductors to decrease the effective inductance; however this would consume a large chip area and also introduce additional large parasitic components into the circuit. The use of series connected capacitors to achieve a smaller effective capacitance is more feasible, however C_1 is usually implemented as the pad capacitance and as such the use of another series capacitor is invalid.

The lower corner frequency is limited by the maximum inductance value that is available for L_1. Although C_2 also influences the lower corner the limitation on C_2 is due to the high frequency NF as discussed earlier and not due to passive component limitations. Since the latter is usually the dominant limitation the maximum available L_1 is not significant.

4.10.5 Simplified inductor model

Since use of the complete on-chip spiral inductor model shown in Figure 2.12 [**47**] would be too cumbersome in the derivation of a practically useful mathematical model, inductors were modelled as only a series inductance and frequency dependent series resistance. The value of the resistance was derived from the inductor *Q*-factor which was assumed constant over frequency within the band of interest; this is, however, not truly the case and will cause deviations in the actual responses from the predicted performance. The complete inductor model would include this frequency dependence of the *Q*-factor.

The impact of the simplification is further apparent in the spike caused in the simulated frequency response in Section 5.3 by the self-resonant frequency of the large inductor L_1, which does not show up in the predicted response. The resulting simplified noise model will also cause deviations in the noise performance.

4.10.6 Base- and collector current noise correlation

It was stated in Section 2.3 that collector current shot noise is not introduced at the base-collector junction as often assumed but in fact originates from the base-emitter junction where majority carrier electrons (in *npn* transistors) from the emitter cross the junction into the base. These noisy electrons are transported across the base to the base-collector junction at the rate quantified in the base transit time, resulting in correlation between the base- and collector current noise.

In the derivation of the equation for NF in Section 4.6 this correlation between the base- and collector current noise is neglected. This is similar to assuming the collector current shot noise is generated at the base-collector junction by setting the base transit time equal to zero, resulting in the conventional SPICE noise model. Although this approximation is feasible when $\omega << 1/\tau_F$, at 60 GHz which is much closer to the device f_T the noise correlation becomes non-negligible and the mathematical model no longer predicts the NF of the LNA accurately [**63**].

4.11 THEORETICAL RESULTS

Figure 4.10 and Figure 4.11 offer some insight into the theoretical performance of this configuration following a design process based on the analysis in the preceding sections. An amplifier with desired S_{21} of 20 dB was designed for operation over the 3 to 10 GHz band (the UWB). A maximum NF of 4 dB was specified.

It was assumed that the IBM 8HP process would be used and the results were obtained with a supply voltage of 1.5 V and a pessimistic β_0 of 300 and on-chip passive inductor Q-factor of 5.

The resulting input reflection was calculated to be less than -10 dB over the entire frequency band, and as desired a flat S_{21} response of 20 dB was obtained. The calculated maximum NF of the first stage is 3.34 dB and the minimum 2.57 dB close to the centre of

the frequency band even without any optimization of the component values. As expected IIP3 increases linearly at approximately 20 dB per decade with frequency from -31.4 dBm to -23.5 dBm over the band of interest due to the -20 dB per decade roll-off in first stage voltage gain.

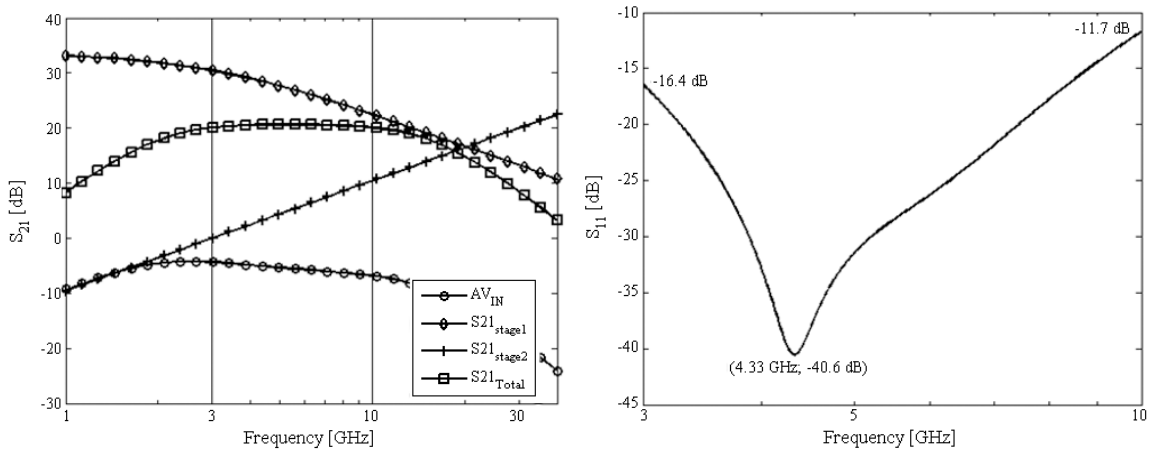

Figure 4.10. Calculated input reflection coefficient and gain versus frequency.

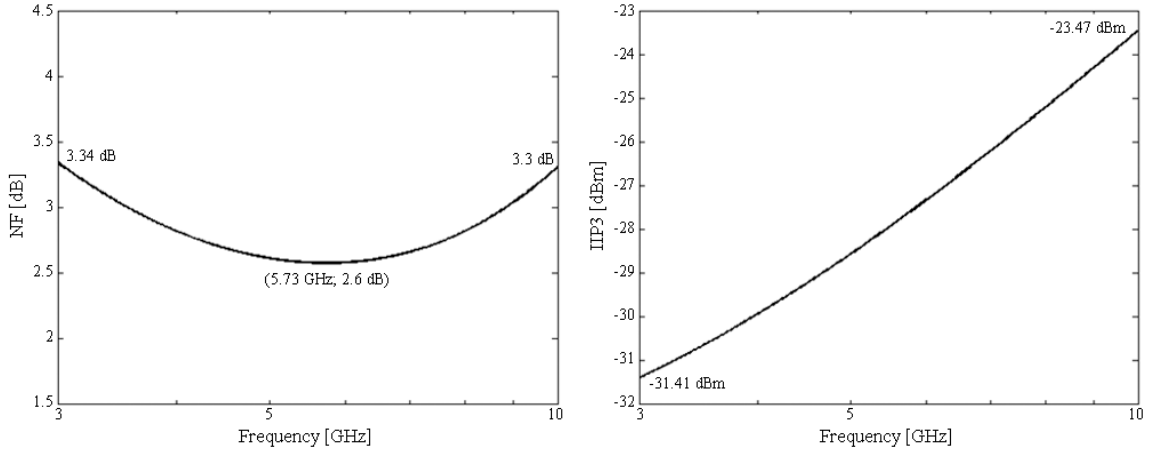

Figure 4.11. Calculated noise figure of the first amplifier stage and approximated IIP3 versus frequency.

4.12 LNA ELECTRONIC DESIGN AUTOMATION

The discussion in Sections 4.2 through 4.10 provide all the groundwork necessary to implement EDA software similar to the software implemented in [**49**] for the design of power amplifiers (PA). A preliminary implementation of such software has been done in MATLAB and was used in the design of the LNAs presented in Chapter 5. The routine was also used to generate the calculated plots for key performance measures and noise source contributions. This MATLAB code is presented in Appendix A.

The software takes as inputs the desired frequency band, gain and maximum NF specifications. The transistor process parameters, including the values of the parasitic components at the chosen emitter length should also be given.

It is then possible to first determine whether the proposed design is feasible based on the desired frequency range and NF specification using the equations given in Section 4.9, or alternatively to find the first stage gain that is required to allow a sufficiently small C_F to achieve the high frequency NF specification. If feasible, the LC-ladder equations (4.1a) and (4.1b) is used to determine the respective reactive component values; after which the rest of the design equations detailed in Section 4.4 is used to find values for the remaining passive components and the collector currents. If it is found that the gain specification cannot be met with the limitations of the transistor process the need for a third stage should be indicated, however this is not included in this preliminary version.

Once these initial values have been derived the S_{11}, S_{21}, NF and approximated IIP3 frequency responses are plotted using (4.8a,b), (4.21), (4.43) and (4.51) respectively, as well as the terms in the numerator of (4.51) which are plotted separately as in Figure 4.8. The component values and collector currents can then be modified one by one and the plots redrawn to observe its effect on the performance measures to optimize the NF as discussed in Section 4.7.

These results are a sound first order design with very little effort from the designer, which can then be optimized further using simulation software and the proper HIT-kits for the transistor process.

Ideally the optimal inductor dimensions should also be calculated for the final inductance values by incorporating that part of the software from [**49**], or preferably by combining them into a complete RF amplifier design package capable of providing rapid LNA and PA design for wireless transceivers.

4.13 CONCLUSION

This chapter discussed the mathematical modelling that was required to quantify the performance of the LC-ladder and capacitive shunt-shunt feedback LNA configuration.

An initial derivation of input reflection and gain equations was presented with subsequent improvement of the accuracy of these equations; which also showed the need for adding a second inductively loaded stage thereby defining the final LNA topology. This led to the definition of compact design equations.

The NF equation was derived and means for optimizing the design to achieve low NF were also discussed. Although a full and accurate quantization of the linearity of the LNA was not included in this study, equations for approximating the IIP3 were given. The noise figure-bandwidth trade-off was discussed as well as other fundamental limits to the performance of this topology.

A means of implementing complete EDA of LNAs employing this topology was defined, and theoretical performance results of such a design were plotted and proved to be very promising.

In summary, the LC-ladder and capacitive shunt-shunt feedback topology proved to be a viable means of implementing very wideband LNAs and as such was manufactured after further simulation as detailed in the following chapters.

CHAPTER 5: SIMULATION RESULTS

5.1 INTRODUCTION

In order to verify the mathematical derivations in Chapter 4, as well as optimizing the design of a LNA for operation over the 1 GHz to 18 GHz range the configuration was simulated using Spectre RF with the HIT-kits provided by IBM. The required specifications are provided in this chapter and then a design in the IBM 8HP SiGe BiCMOS process is simulated to verify the expected results. Various attempts to improve the linearity of the LNA are also discussed and simulation results given.

To also test the feasibility of the configuration for use at mm-wave frequencies, an implementation for 57 GHz to 64 GHz is simulated. It was however found that the first order design done using the equations in Chapter 4 does not predict results accurately as expected from the discussion in Sections 4.9 and 4.10.

The 8HP process is preferable for this implementation, having a f_T of 200 GHz which is ten times larger than the desired f_H. However, due to the availability of a free IBM 7WL run provided by MOSIS through the MOSIS educational program[5] (MEP), this process was used for fabrication instead, and offers an f_T of only 60 GHz. The free run is a grant obtained through the acceptance of the research proposal for this work by MOSIS. The simulation results of the design using this process are also shown and discussed, and would be expected to repeat in the measured results of the implemented LNA.

The schematic entry, simulations and layout (discussed in Chapter 6) were done using Cadence Virtuoso v5.1.41[6]. Details on the packages that were used are provided in Table 5.1.

Small-signal simulations were used to find the input return loss, forward gain and NF of the LNA. Monte Carlo analyses and a temperature sweep were performed to find the sensitivity of the performance measures to parameter and temperature changes. Large signal analysis was used to find the noise floor and for determining the IIP3 and P_{1dB} of the LNA.

[5] http://www.mosis.com/products/mep/mep-about.html
[6] www.cadence.com

Table 5.1. Packages that were used form the Cadence Virtuoso Software Suite and their functionality.

Package name	Functionality
Virtuoso Schematic Editor	Graphical user interface for schematic entry
Analog Design Environment (ADE), and Spectre RF v5.10.41.072908	ADE is a graphical user interface that can be used to compile the simulator input file for various IC simulators, such as Spectre RF which is capable of AMS simulation.
Virtuoso Layout Editor	Graphical user interface for drawing circuit layouts
Assura	Design rule check (DRC) Layout versus schematic check (LVS)

The VBIC transistor model used in the simulations as well as other important considerations regarding the 8HP/7WL process simulations have been discussed in Sections 3.2 and 3.7. Simulations were done with temperature specified at 27 °C which is frequently assumed as room temperature. All simulations were done using parameterized cells which include all device parasitics, and as such only the interconnect capacitances were neglected.

5.2 CIRCUIT SCHEMATIC AND SPECIFICATIONS OF THE DESIGN

To show the feasibility of the configuration a wideband LNA operating from 1 GHz to 18 GHz was implemented. The LNA will be used in a multi-channel environment where switching between various 800 MHz channels is required. Therefore minimizing the overhead of the demodulation stages would require good input matching, a constant gain as well as low NF over the entire frequency band. It is also important to have a high (and preferably constant) P_{1dB} point over the entire band of operation. The specifications given in Table 5.2 were defined, and the final complete circuit schematic is shown in Figure 5.1.

Although the cascode configuration is commonly used in RF amplifiers, the feedback capacitance C_F introduced between the input and output of the first stage negates most of the advantages obtained from the fact that the cascode configuration serves to decouple the input and output. Therefore the simple common emitter configuration was used. The cascode configuration could have been used for latter stages though, but simulations did

not show any marked improvement and the extra transistor would have merely reduced an already small voltage over the load even further.

Table 5.2. Desired LNA specifications for implementation.

	Specification
Bandwidth	1 GHz to 18 GHz
Gain	18-22 dB
NF	< 4 dB
P_{1dB}	-10 dBm

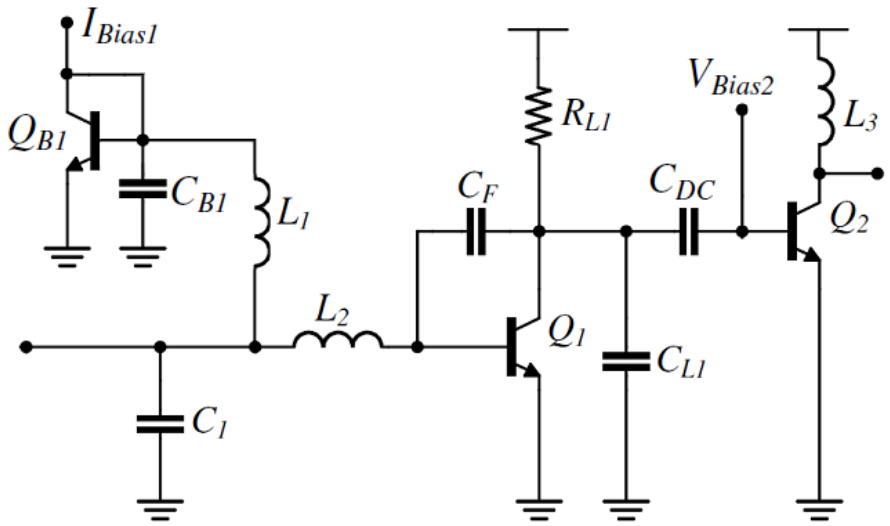

Figure 5.1. Complete schematic of a LNA designed for operation from 1 to 18 GHz.

5.2.1 Transistor biasing

Biasing techniques were kept as simple as possible to allow easy adjustment of the bias currents during experimental testing. The first stage bias network is shown in Figure 5.1. Since inductor L_1 can also act as the bias choke, the biasing of this stage could be done on-chip. A simple current mirror was used to generate the correct V_{BE} for Q_1. An off-chip resistor will be used to bias the current mirror which allows for adjusting the bias current.

Unfortunately the second amplifier stage requires an off-chip bias choke. Although relatively large inductors are available in this process the Q-factor at high frequencies are very low and thus the signal is attenuated when on-chip biasing is attempted. The active bias circuit suggested in [**65**] shown in Figure 5.2 will be used.

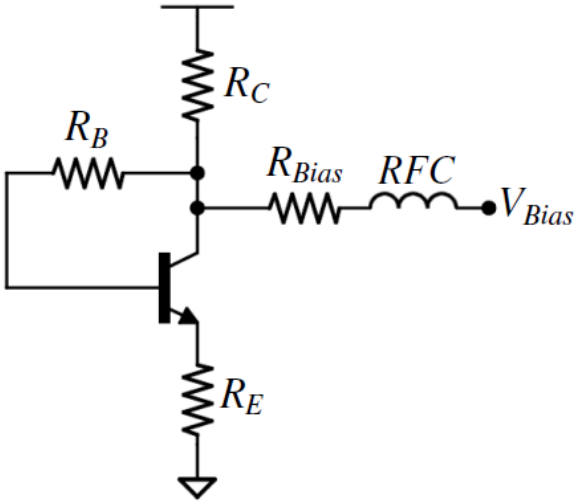

Figure 5.2. Off-chip active bias network [65].

5.3 8HP DESIGN FOR 1-18 GHZ

5.3.1 Initial design

The design process described in Chapter 4 was used in the initial design of a LNA over the 1 GHz to 18 GHz band using the 0.13 µm IBM 8HP BiCMOS process. Using the design equations in Section 4.4 the component values in

Table 5.3 were derived with transistor emitter lengths of 12 µm and a power supply of 1.5 V. Both the calculated and simulated *S*-parameter and NF results for this design are shown Figure 5.3 and Figure 5.4 respectively. A small-signal *S*-parameter analysis was performed in Spectre RF to find the S_{11} and S_{21} frequency response, as well as the NF. The calculated *S*-parameters track the simulations very well, and the deviation of the calculated NF is deemed acceptable. The spike in the response at 16 GHz is due to the self resonant frequency of the large L_1 inductor.

The noise contributions of the various noise sources of this LNA are plotted in Figure 5.5 and shows the very large contribution of the common-emitter voltage noise as a result of the large C_F. It is also apparent that none of the specifications are met by this initial design.

Table 5.3. Initial component values derived using the design equations.

Symbol	Value
C_1	177 fF
C_F	266 fF
L_1	7.96 nH
L_2	442 pH
L_3	1 nH
R_{L1}	417 Ω
I_{C1}	0.6 mA
I_{C2}	5 mA

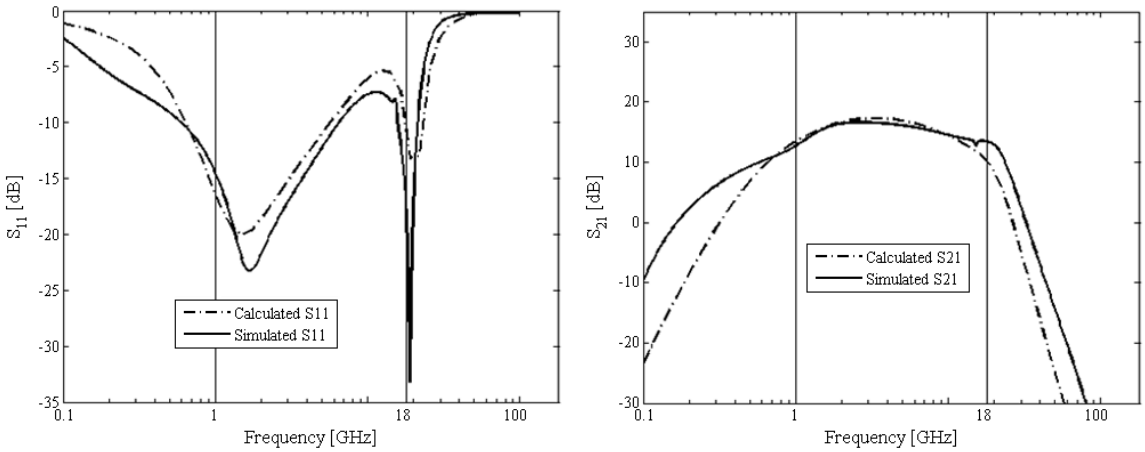

Figure 5.3. Calculated and simulated *S*-parameters without any optimization.

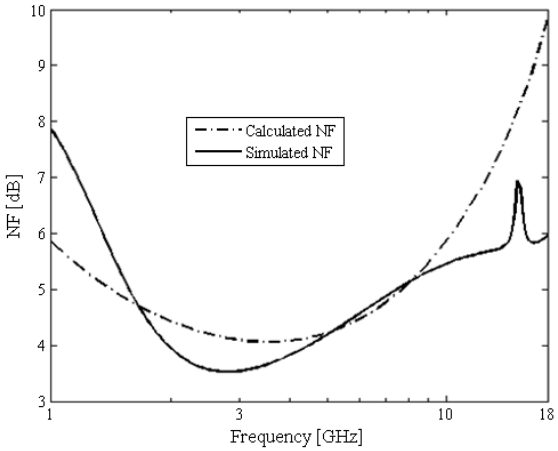

Figure 5.4. Calculated and simulated NF without any optimization.

5.3.2 Noise optimization

Assuming that noise optimization of the collector current and passive components would provide a 2 dB NF improvement a maximum NF of 6 dB was used in equation (4.56) and it was found that a low frequency first stage gain of 30 is necessary to meet the bandwidth versus NF requirement. Once the first stage gain is increased the noise contributions shown in the plot on the right of Figure 5.5 result. A large reduction in CE noise voltage is observed since the value of C_F has now been reduced to 92 fF.

As discussed in Section 4.7.1 the collector current can be increased to reduce the noise. This was done while keeping the voltage gain constant at thirty by simultaneously changing the value of R_{L1}. To improve the input matching after increasing the collector current it was also necessary to add a 150 fF load capacitor to the output of the first stage. The resulting noise contributions are shown in Figure 5.6 on the left and the calculated and simulated NF on the right. With the steps taken thus far the NF has already been improved by 3.5 dB at the lower corner frequency and by more than 2 dB at the upper corner.

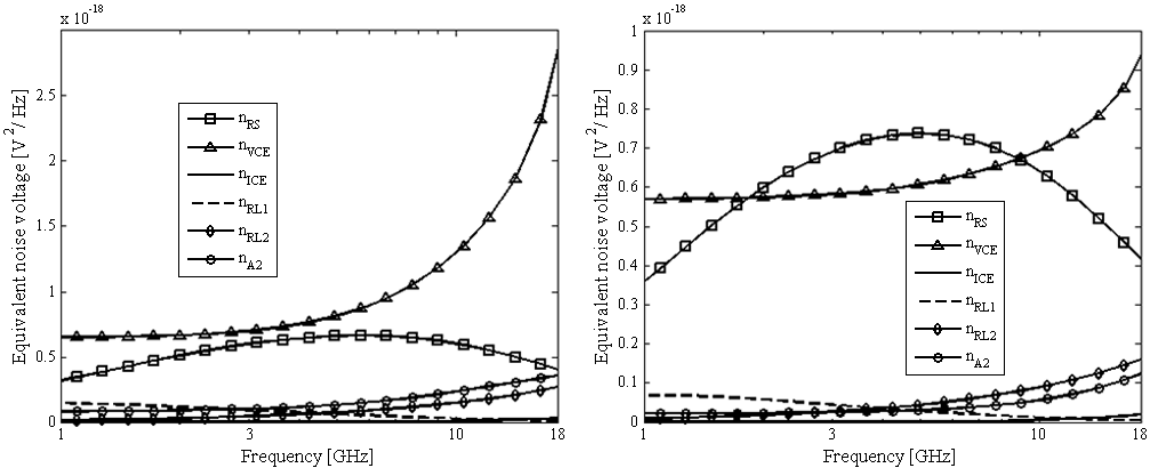

Figure 5.5. Noise contribution of the various noise sources before any optimization (left) and after increasing the first stage gain to 30 (right).

Following the above, the passive component values of the input matching network were also optimized based on the discussion in Section 4.7.1. The noise optimized values are shown in Table 5.4, and the final noise contributions are plotted in Figure 5.7. This optimization has increased the high frequency CE noise voltage contribution slightly, but has also resulted in a larger increase in the gain of the source resistor noise through the input matching network which also implies a larger gain of the input signal, and as such

improves the NF. The final NF and *S*-parameters of the design after noise optimization are shown in Figure 5.8 through Figure 5.10. A final NF improvement of 4.4 dB at the lower corner, 1.3 dB in the mid-band and 2.35 dB at the upper corner frequency can be observed compared to the initial NF in Figure 5.4. Good tracking between mathematical and simulation results are again observed confirming the accuracy of the mathematical model.

The sharp deviations in both the *S*-parameter responses and NF around 10 GHz are due to the self-resonance of inductor L_1. Since L_1 is used to set the lower corner frequency its capacitive response at very high frequencies does not have a large impact on matching, the fluctuations are however undesirable and thus a smaller inductance value should be used whenever possible to increase the self-resonant frequency.

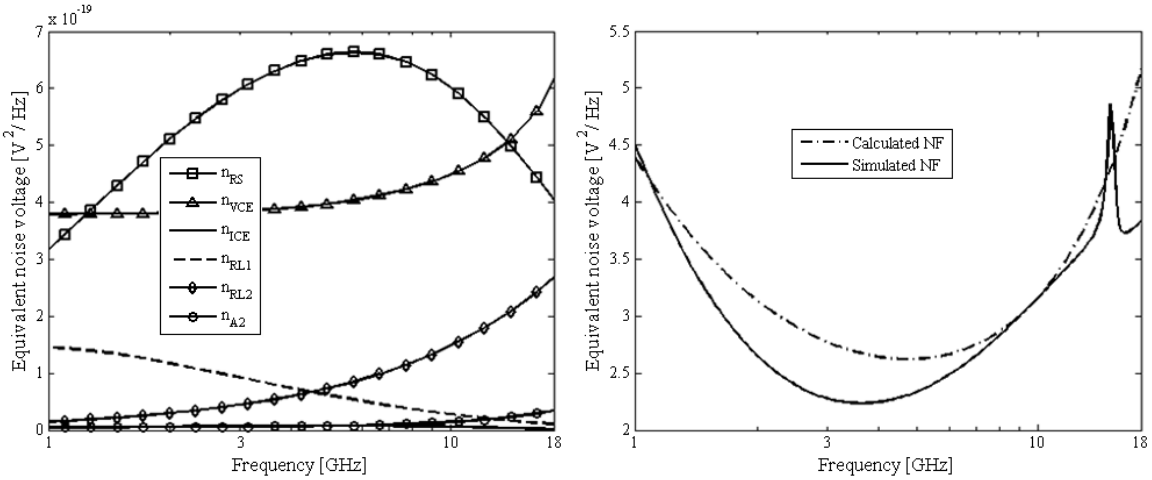

Figure 5.6. Noise contributions and calculated and simulated NF after collector current and C_{L1} optimization.

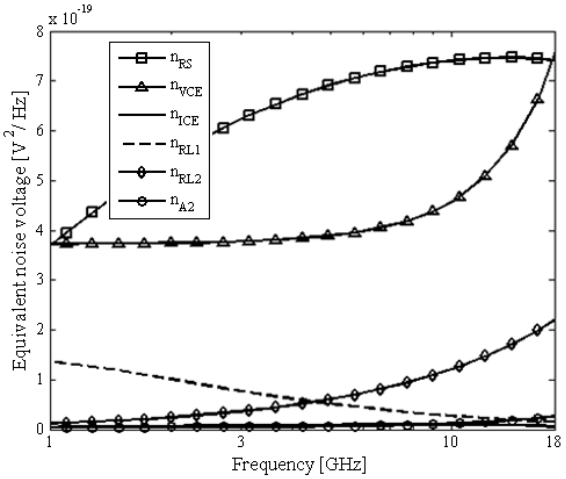

Figure 5.7. Final noise contributions of the noise sources after optimization of the passive components and collector current.

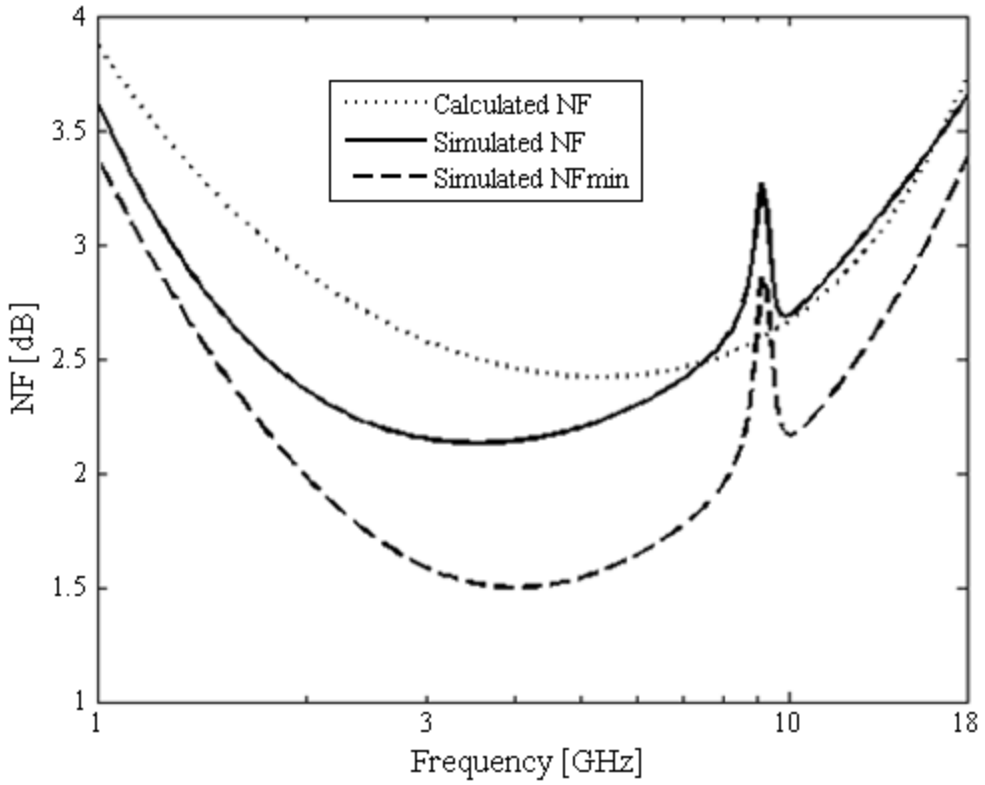

Figure 5.8. Final simulated and calculated NF after optimization of the passive components and collector current.

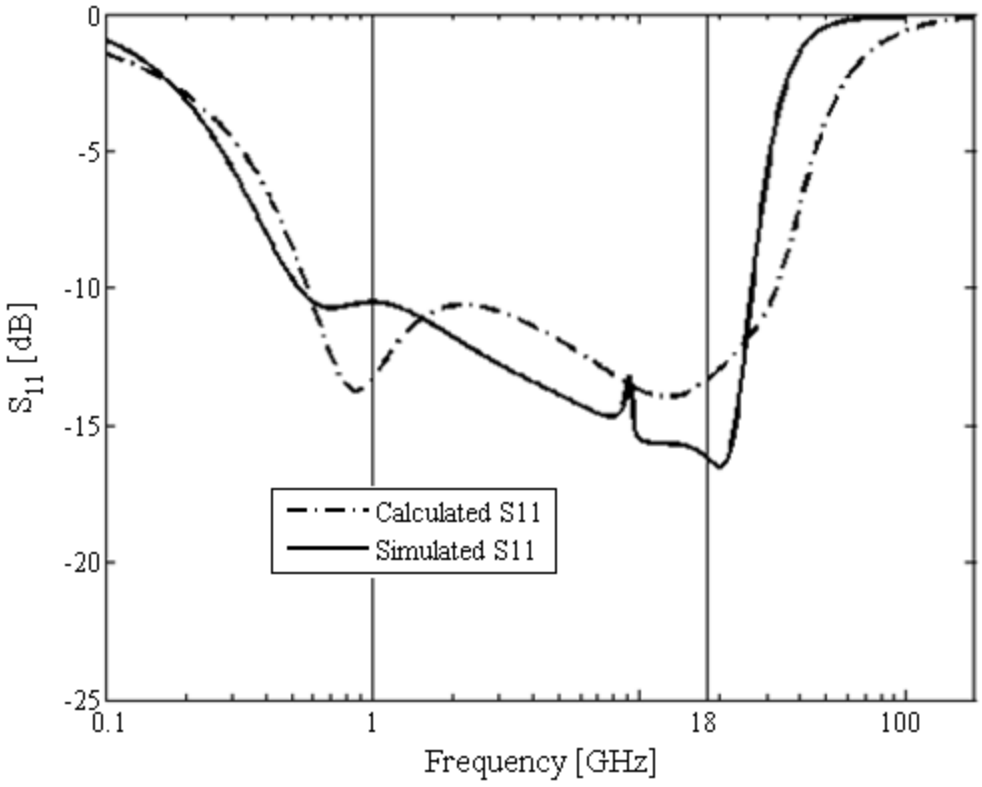

Figure 5.9. Final simulated and calculated S_{11} after optimization of the passive components and collector current.

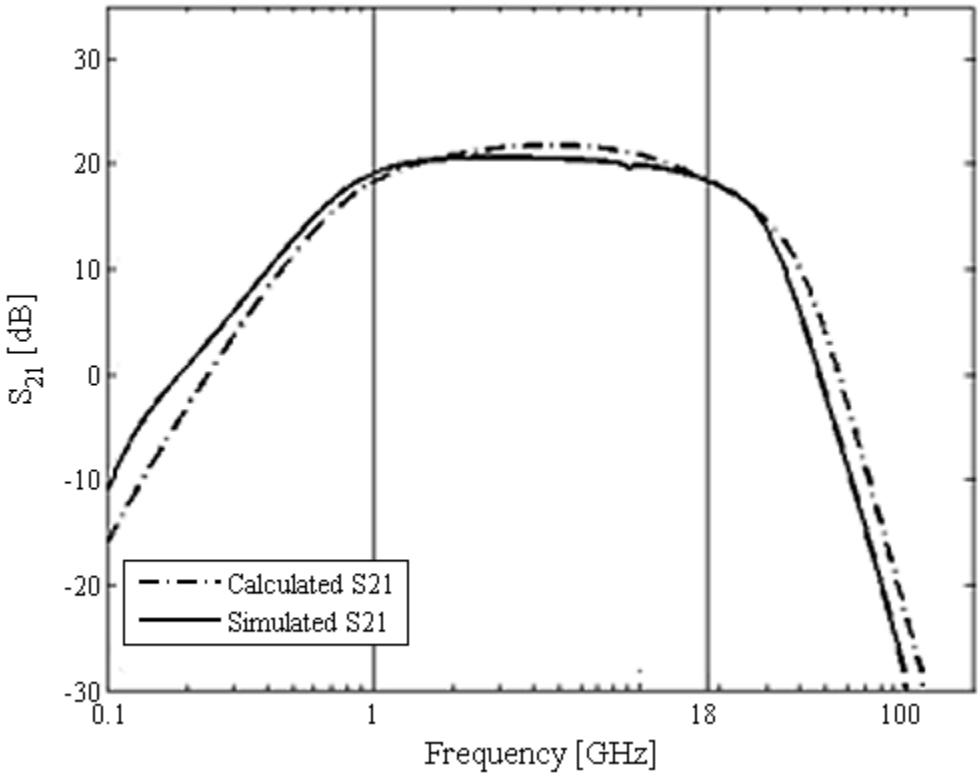

Figure 5.10. Final simulated and calculated S_{21} after optimization of the passive components and collector current.

Table 5.4. Comparison of initial component values and values after noise optimization.

Symbol	Initial value	Optimized value
C_1	177 fF	40 fF
C_F	266 fF	92 fF
C_{L1}	0	150 fF
L_1	7.96 nH	9.91 nH
L_2	442 pH	363 pH
L_3	1 nH	465 pH
R_{L1}	417 Ω	230 Ω
I_{C1}	0.6 mA	3.5 mA
I_{C2}	5 mA	5 mA

Figure 5.10 shows that the maximum gain of the final amplifier is 21.4 dB and falls to 18.2 dB at 18 GHz which is the upper corner frequency. At the lower corner frequency the gain is 19.9 dB. The input reflection coefficient in Figure 5.9 is shown to be less than

-10 dB over the frequency band of interest and thus all specifications except for the P_{1dB} compression point have now been met.

The simulated reverse isolation of the LNA is excellent with S_{12} < -25 dB. The output reflection coefficient is very large however since no attempt at output matching was made. Such matching is complicated by the large bandwidth which renders tuned reactive network matching infeasible. A straightforward solution would be to add a final amplifier stage with a load resistance close in value to the characteristic impedance of the system; ignoring the effect of any parasitic elements this will match the output over the entire bandwidth. This technique was followed in matching the amplifier designed for the 7WL process which is presented in Section 5.5.

5.3.3 Stability

The minimum value of the K stability factor is 1.85 which is larger than 1, and the B_f factor minimum is 0.027 which is larger than zero. These two criteria are necessary and sufficient to ensure the unconditional stability of the LNA [**65**]. Simulations were done over the entire frequency range and up to the f_{max} (280 GHz) of the transistor to also ensure that there are no instabilities at frequencies beyond the range of interest.

5.3.4 Monte Carlo analysis and temperature sweep

To find the sensitivity of the design to process parameter variations a Monte Carlo analysis was performed. Since many of the process parameters are physically correlated it is important to take these correlations into account when doing a statistical analysis. The statistical design kit included in the PDK provided by IBM does capture these correlations in the skew values used during the analysis [**56**]. The variations in the *S*-parameters with 100 simulated cases are shown in Figure 5.11 and that of the NF in Figure 5.12.

S_{11} varies by approximately 2 dB above 2 GHz, but remains below -10 dB. Between 1 GHz and 2 GHz the S_{11} varies by as much as 2.5 dB and, ignoring the one extreme case, reaches a maximum value of -9 dB. Even this is a good input return loss value and as such the effects of the variation on LNA performance should not be noticeable.

The low to mid-band S_{21} varies from 18.5 dB to 22 dB, which is a variation of 3.5 dB, and thus remains within the specified range of 18 to 22 dB. When the low frequency gain

increases above approximately 20.5 dB the gain at the upper corner frequency no longer increases due to the gain-bandwidth product of the transistor. This means that the -3 dB cut-off frequency is reduced to less than 18 GHz. It is however emphasized that the gain at 18 GHz is not reduced, but remains constant while lower frequency gain increases and thus operation in a sub-band at the upper frequency end remains feasible.

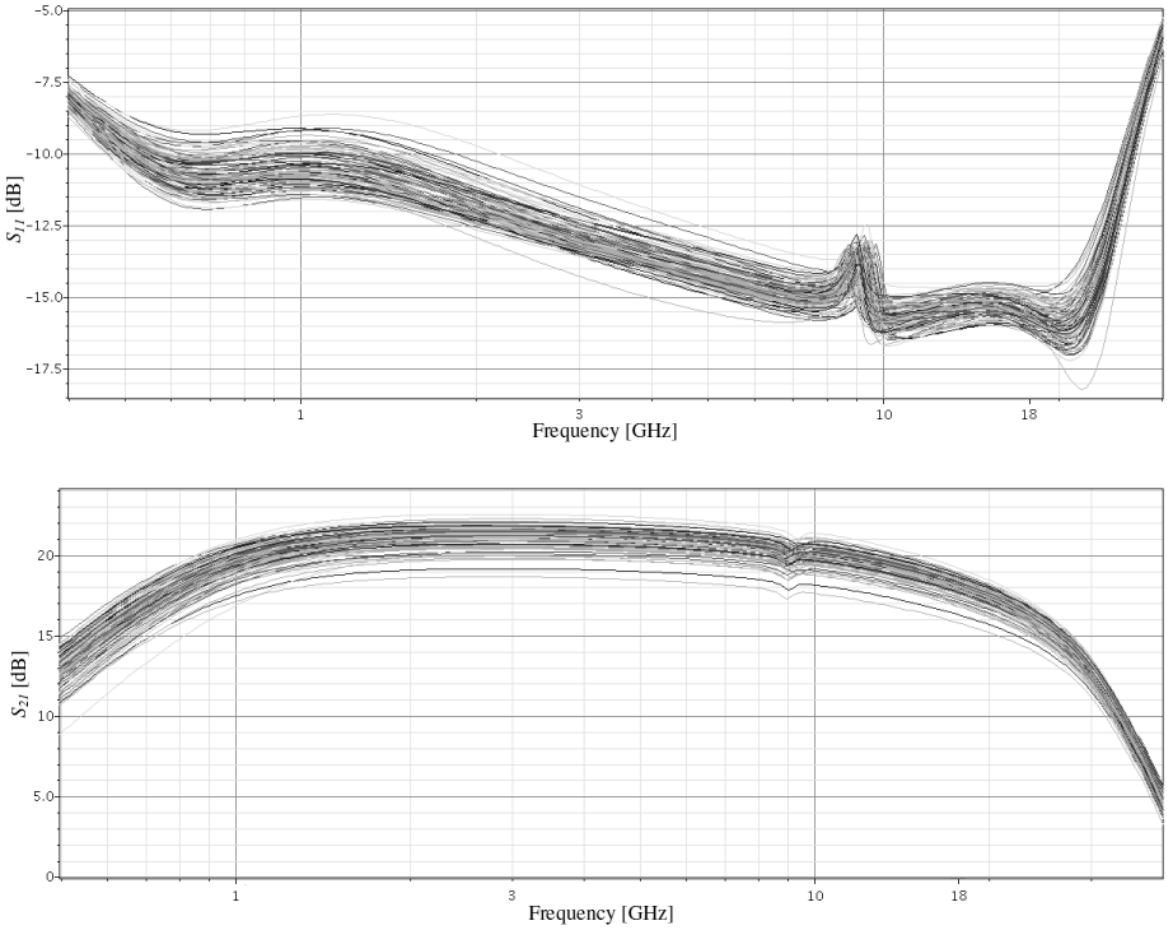

Figure 5.11. Variation in S_{11} (top) and S_{21} (bottom) resulting from a Monte Carlo analysis.

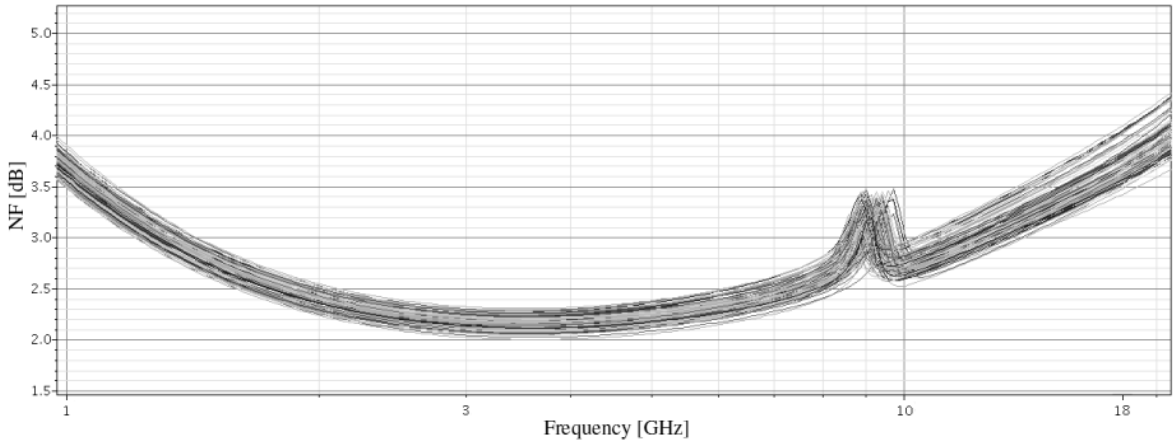

Figure 5.12. Variation in NF resulting from a Monte Carlo analysis.

The NF varies by less than 0.5 dB over most of the frequency band and only becomes more than 4 dB in extreme cases above 16 GHz, where the variation is approximately 0.7 dB.

Through the one-by-one substitution of the circuit elements with ideal components it was found that the most parameter sensitive components are inductor L_1 and the transistors. Based on this finding a circuit with ideal passive components was simulated and the transistor emitter length was swept over a 2 µm range from 10 µm to 12 µm. The variation in the performance measures are shown in Figure 5.13. The relatively small deviations over such a wide range of emitter lengths indicate that the emitter length has very little impact on the performance and as such the transistors are most sensitive to either emitter width- or doping variations. Unfortunately there is no straightforward way of differentiating between these effects using Spectre RF.

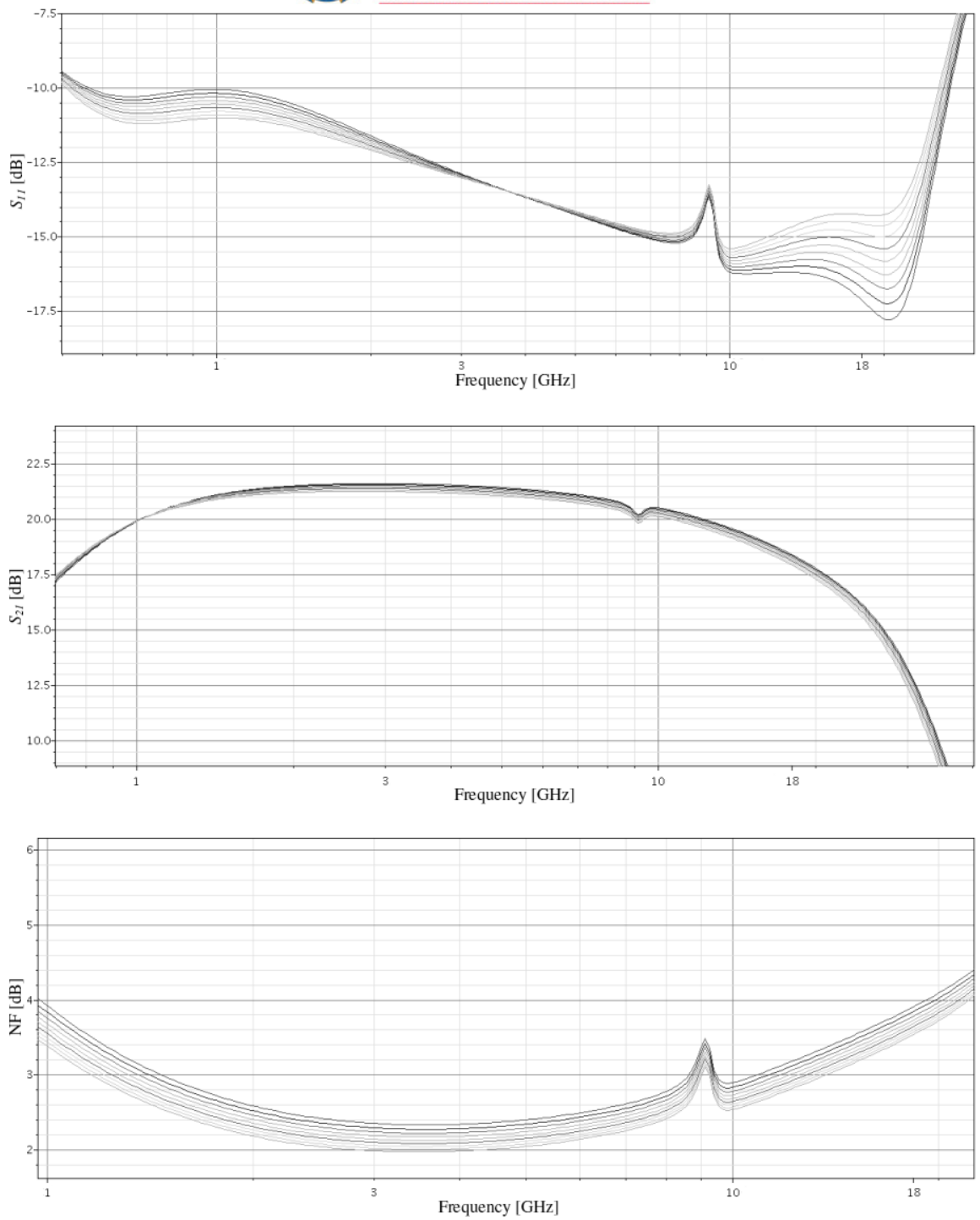

Figure 5.13. Variation in performance with l_e swept from 10 µm to 12 µm.

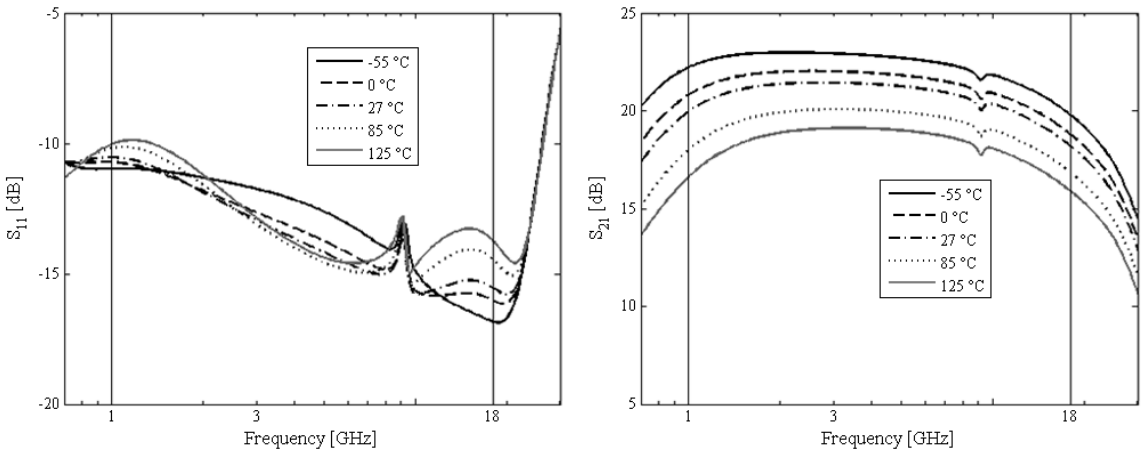

Figure 5.14. S_{11} and S_{21} variation with temperature from -55 °C to 125 °C.

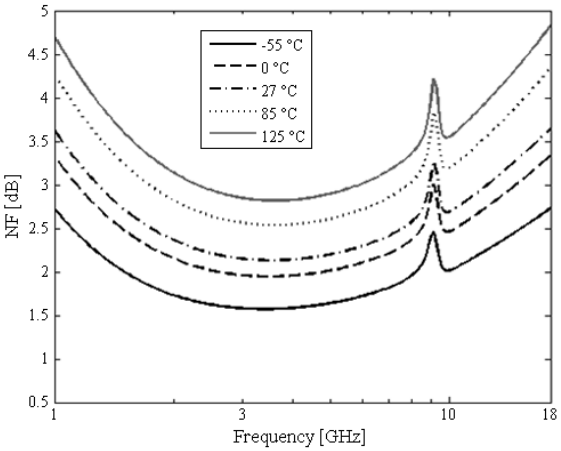

Figure 5.15. NF variation with temperature swept from -55 °C to 125 °C.

5.3.5 Linearity of the LNA and its optimization

The linearity of the noise optimized LNA was determined by simulating both the P_{1dB} compression point and IIP3 using a large signal analysis in Spectre RF. Input power was swept from -50 dBm to 0 dBm at various frequencies over the band of interest and the results are plotted versus frequency in Figure 5.16.

The linearity of the LNA is the only performance measure that is below specification with the IIP3 -27.5 dBm at 1 GHz, increasing approximately linearly to -22 dBm at 9 GHz above which the IIP3 remains constant. It is likely that the non-linearity of the second stage transistor is the determining factor in this maximum value for IIP3, while the high gain of the first stage decreases the IIP3 below 9 GHz. It can also be seen that the approximation used for IIP3 in the mathematical model over estimates the simulated IIP3 significantly over most of the band, and then underestimates it at high frequencies. Therefore a more

accurate model such as one derived using a Volterra-series should be used if more accurate modelling is desired. P_{1dB} varies from -26.5 dBm at 1 GHz to -14 GHz at 9 GHz from where it remains constant with frequency.

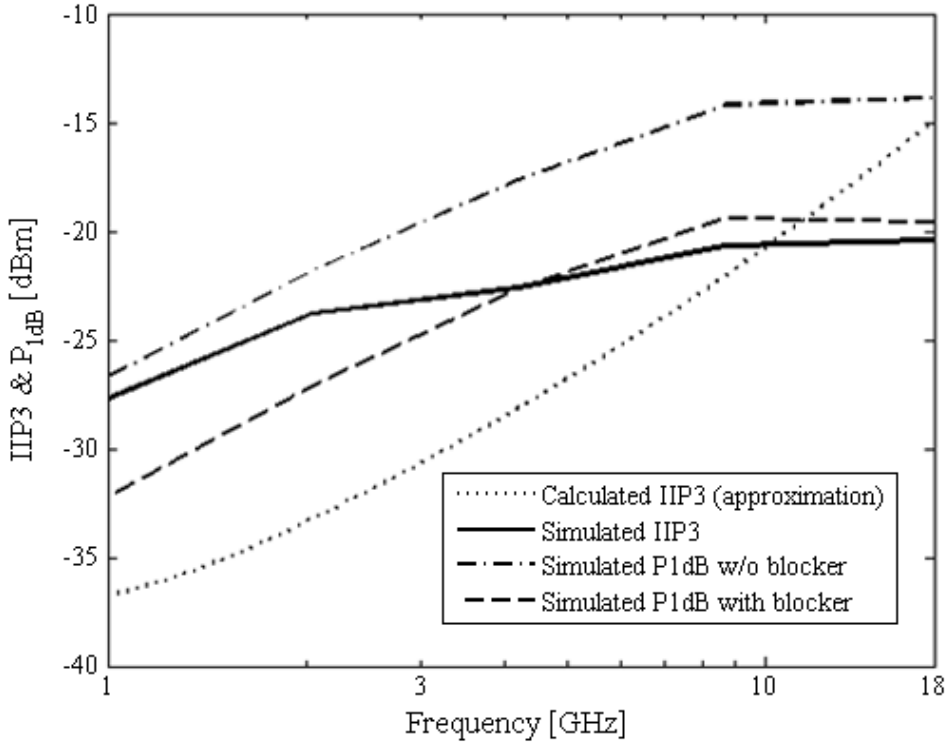

Figure 5.16. Simulated IIP3 and P_{1dB} compression point versus frequency of the noise optimized LNA.

The first attempt that was made towards improving the linearity of the LNA was to use the cascode configuration in the second stage in order to reduce the voltage drop over the BC-capacitance and also decrease avalanche multiplication. However, it has been pointed out that it is the exponential $I_{CE} - V_{CE}$ non-linearity that dominates at currents lower than 5 mA [**37**] and as such no improvement was observed.

It was shown that an I_C of around 25 mA produces the optimal IIP3 [**37**], but this is not practical for the second stage as this will result in too high a low frequency gain which will decrease the high frequency gain due to the gain-bandwidth product. The current density will also be very close or even beyond the peak f_T where many other second order effects also become important. Finally such a large increase in power consumption is not an acceptable trade-off for the increase in linearity.

The use of overall feedback was also considered but has the shortcoming of greatly affecting the input matching and noise performance of the LNA as discussed in Section 4.8. It was also found that the linearity improvement due to overall feedback is not more than what can be obtained by using feedback only in the last amplifier stage as discussed next.

Since the last amplifier stage of a LNA dominates the linearity of the LNA as a whole, and its linearity is reduced by the gain of the preceding stages it stood to reason that improving the linearity of this stage would be the most feasible means of improving performance. Resistive emitter degeneration was used to provide series-series feedback. Since this decreases the transconductance both the collector current and load impedance was increased to maintain a constant gain for this stage. The collector current was increased to a the rather high value of 12 mA since the $I_{CE} - V_{CE}$ non-linearity due to avalanche multiplication (which typically dominates for 5 mA < I_C < 25 mA) improves with collector current [**37**]. The improvement observed in the linearity of the amplifier is given in Figure 5.17 which illustrates the plots of the improved IIP3 and P_{1dB}. An emitter resistance of only 4 Ω was used since larger degeneration resulted in the -3 dB cut-off frequency going below 18 GHz. It is interesting to note that while the IIP3 has been improved, the linearization attempt has decreased the P_{1dB} compression point.

Adding emitter degeneration to the first stage does not improve linearity further. Initially there appeared to be some improvement, however upon closer investigation it was seen this was due to the reduction in the gain of the first stage (and thus less reduction of second stage linearity) and not due to the first stage linearity improvement. According to (4.51) a reduction in the first stage gain given in dB should lead to a one-to-one improvement of overall IIP3, and this was indeed the case; thus there is no advantage in degenerating the first stage as this only influences the input matching, gain and NF negatively without improving linearity as the second stage remains completely dominant.

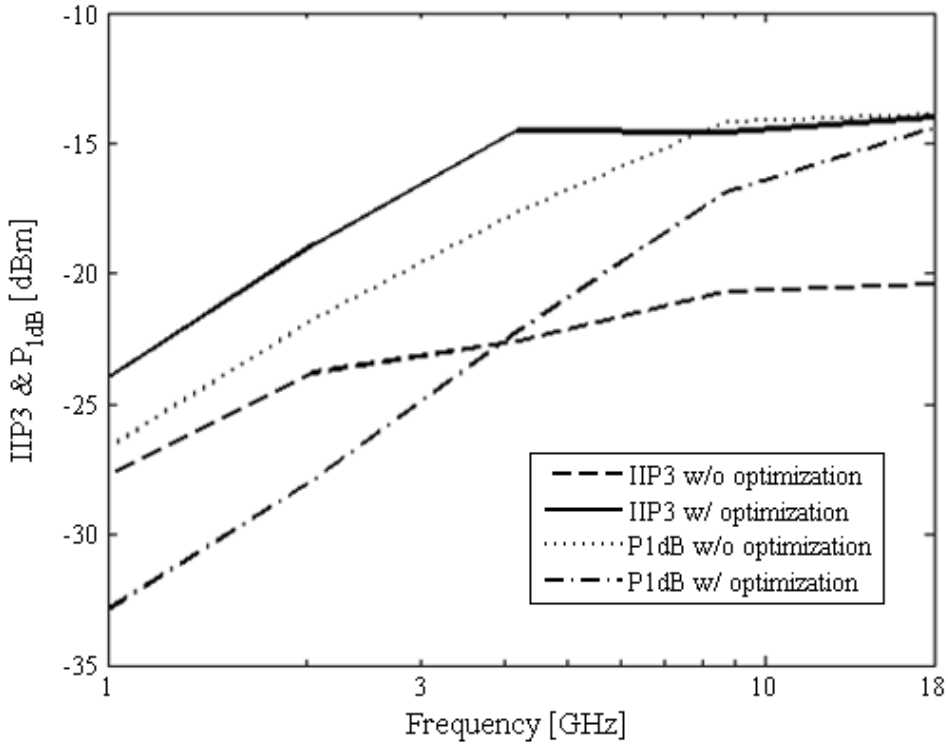

Figure 5.17. Simulated IIP3 and P_{1dB} compression point versus frequency with and without second stage emitter degeneration.

It was also considered that a third amplifier stage could be added to allow smaller gain per stage, and thus larger emitter degeneration resulting in more linear stages. However since the third stage linearity is now reduced by both the first and second stage gain it was found that the linearity is worsened even when relatively large emitter resistors are used.

It was therefore concluded that only using emitter degeneration in the final stage is the most effective means of improving the linearity of the amplifier, while also reasonably maintaining the results of the other performance measures. The shape of forward gain and NF remained the same as before the linearity improvement and thus are not shown again, but gain was decreased by 0.9 dB to 20.0 dB and NF was increased on average by 0.5 dB to 2.15 dB at the minimum and 3.85 dB at the upper corner frequency. Although the S_{11} curve versus frequency changed somewhat in shape it remained below the specified -10 dB.

In closing a remark on the P_{1dB} being higher than the IIP3 in both Figure 5.16 and Figure 5.17 is warranted. In a single transistor amplifier stage with constant power coefficients it is usually found that the single tone P_{1dB} compression point is theoretically 9.6 dB lower than the IIP3. In more complex systems this is not necessarily the case as the

coefficients also become more complex. In broadband amplifiers the IP3 is affected by the harmonics above the third harmonic which may also fall in the band of interest and therefore act as significant blockers of the first harmonic which would result in a much lower IIP3 than expected.

The sharp increase in IIP3 observed in both Figure 5.16 and Figure 5.17 corroborates this. For a 1 GHz signal all harmonics up to the 17th harmonic fall within the pass-band of the LNA resulting in a very low IIP3. For a 3 GHz signal the harmonics up to the 5th order are still passed. It is only above 6 GHz that the 3rd order harmonic falls outside of the pass band, and this coincides with the frequency where the rapid increase in IIP3 tapers off. Above this frequency it is likely that the further improvement in linearity is due to the high frequency gain roll-off of the two amplifier stages.

With these considerations in mind it is reasonable that the P_{1dB} could be higher than the IIP3 in broadband LNAs. In Figure 5.17 where the emitter resistor has been included the P_{1dB}/IIP3 relation is closer to the theoretical response, especially at high frequencies.

5.3.6 Sensitivity of the LNA optimized for linearity

Since the use of feedback makes the gain and other LNA performance measures less dependent on the transistor parameters it was justified to investigate the effect of the linearity optimization, i.e. the addition of local shunt-shunt feedback, on the LNA sensitivity. The same Monte Carlo analysis and temperature sweeps were performed as for the original LNA and the results are shown in Figure 5.18 to Figure 5.21.

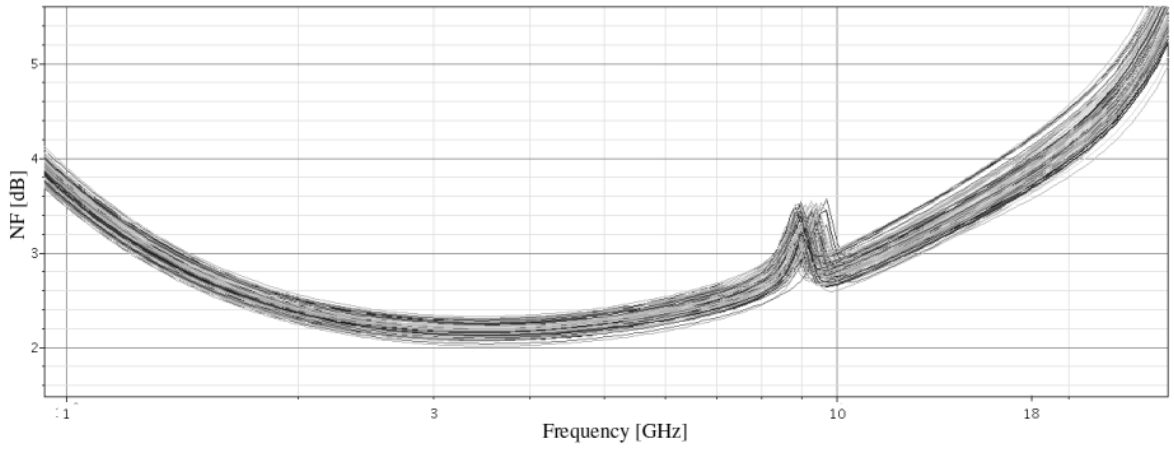

Figure 5.18. Variation in NF resulting from a Monte Carlo analysis on the LNA with emitter degeneration.

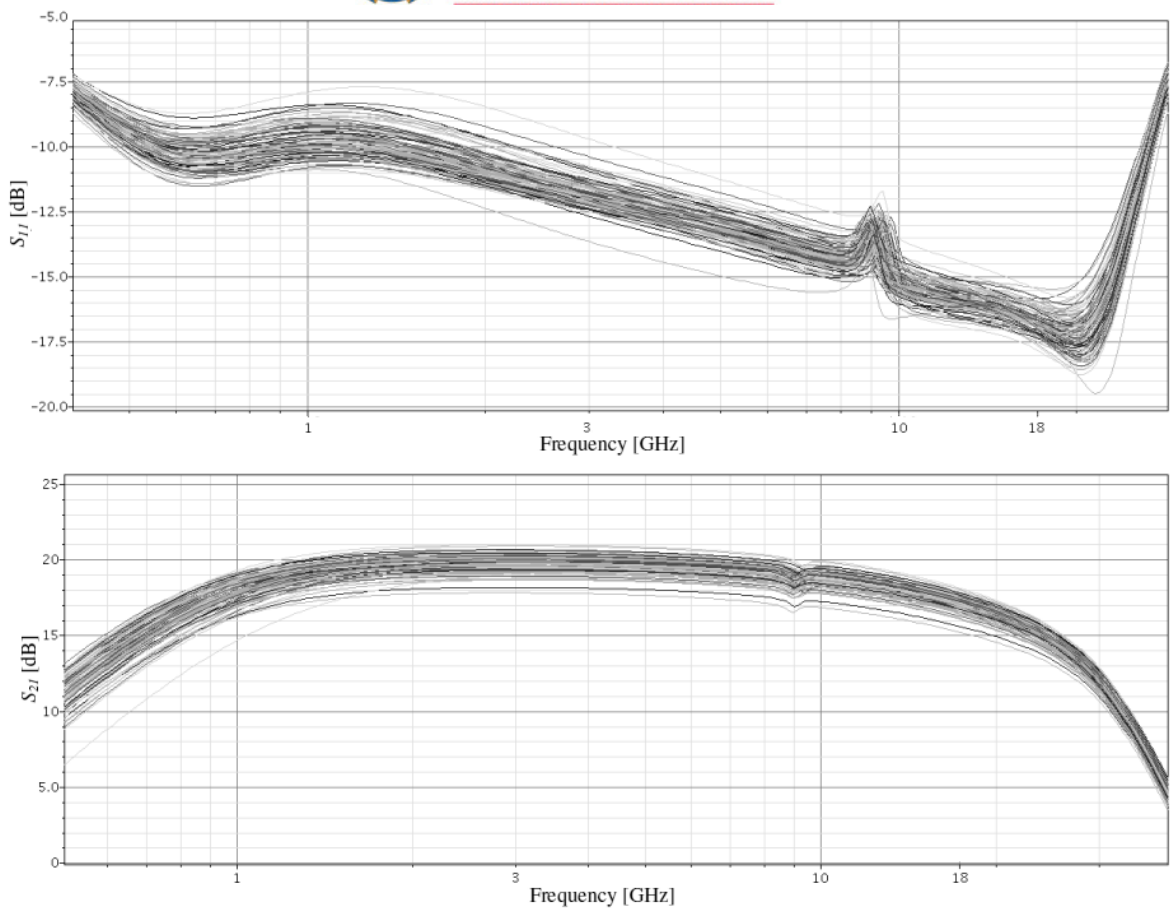

Figure 5.19. Variation in S_{11} (top) and S_{21} (bottom) resulting from a Monte Carlo analysis on the LNA with emitter degeneration.

The S_{11} varies between -10 dB and -8.4 dB at 1 GHz and remains above -10 dB in some cases up to 2.6 GHz, from where it is always within specification. This is a similar deviation to the 2 dB variation reported in the LNA without feedback.

A large improvement can however be seen in the gain variation with S_{21} varying between 16.3 and 19.3 dB at 1 GHz, 18.8 and 20.9 dB in the mid-band and from 16 to 17.9 dB at 18 GHz. That is an average variation of only 2.4 dB compared to 3.5 dB in the previous case. A more important observation however is that the gain never increases above the designed gain, namely 21.4 dB, but only decreases by at most 3 dB. This means that the problem of the reduced upper -3 dB cut-off frequency due to the gain-bandwidth product when low frequency gain is increased has been resolved through the addition of emitter degeneration to the latter stages of the LNA.

The NF varies by only 0.3 dB up to 12 GHz compared to the 0.4-0.5 dB variation reported for the previous case, and also remains below 4 dB at frequencies lower than 16 GHz as

before. At 18 GHz the total variation in NF is 0.64 dB with a maximum of 4.25 dB. Thus although the NF variation has been reduced the absolute NF is slightly higher at the high frequency end.

Thus although the low frequency input matching and the high frequency noise performance has been slightly reduced, a large improvement in the robustness with process variations of both the *S*-parameters and NF resulted from the addition of feedback. The increase in maximum NF of 0.25 dB is easily justified through these gains in addition to the improvement in the linearity of the LNA which was the initial objective. The disadvantage of poor input return loss at the low frequency end can also be easily compensated for by overdesigning for the S_{11} parameter in future designs based on the knowledge obtained here.

Robustness with temperature is also very good and shows a large improvement to the results presented in Section 5.3.4. Input return loss remains below the specified -10 dB over most of the temperature and frequency range. The only exception is the case below 2 GHz at 85 °C and 125 °C.

Gain varies by only 2.5 dB (as opposed to 4.5 dB before) in the mid-band over the entire military specification temperature range. The upper -3 dB cut-off frequency is also once again maintained despite this variation due to the upper limit placed on low frequency gain by the degeneration resistors. At -55 °C where the mid-band gain is at its maximum the gain at 18 GHz is 18 dB, and when the gain is decreased to its minimum at 125 °C the mid-band gain is 18.4 dB with the gain at 1 GHz an 18 GHz at respectively 15.5 dB and 15.4 dB.

The NF varies by 2 dB on average over the entire temperature range and an increase in the absolute NF of 0.6 dB at high frequencies is again observed similar to the discussion above.

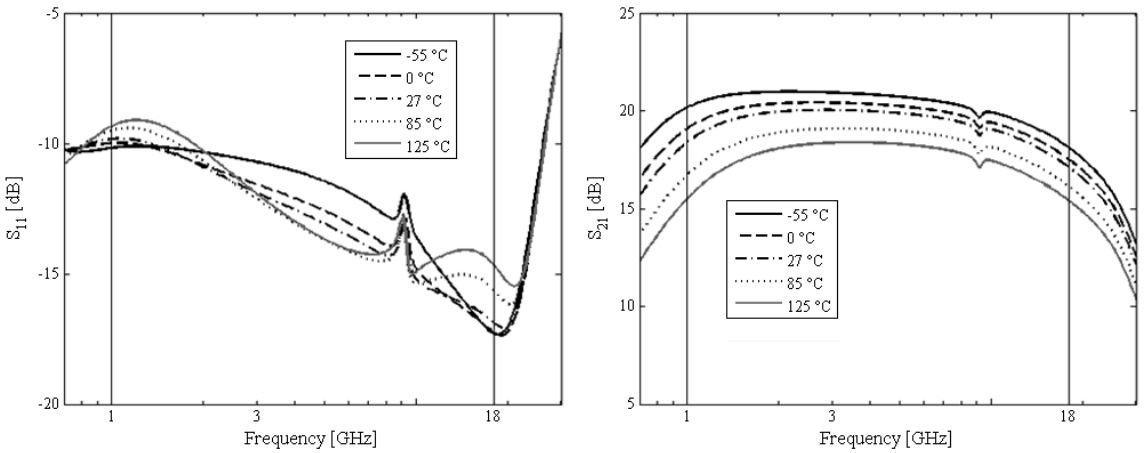

Figure 5.20. S_{11} and S_{21} variation with temperature from -55 °C to 125 °C for the LNA optimized for linearity.

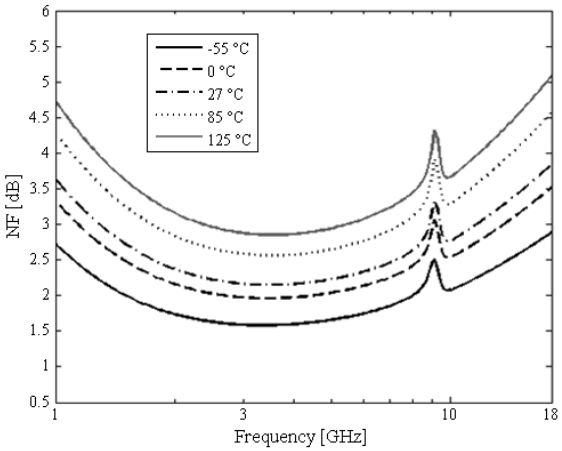

Figure 5.21. Variation in NF of the LNA optimized for linearity with temperature from -55 °C to 125 °C.

5.3.7 Dynamic range and group delay

To determine the dynamic range of the LNA the output noise of the LNA optimized for linearity was simulated. The plot of the output noise voltage spectral density (S_o) is shown in Figure 5.22 with the estimated noise bandwidth of 30 GHz. The average S_o in the band of operation is 39 aV^2/Hz and thus the rms output noise voltage (v_{no}) is 1.08 mV, which is -29.3 dBm in a 50 Ω system; and when reduced by the 20 dB voltage gain when referred to the input becomes -49.3 dBm which is the minimum detectable signal (MDS) of the LNA. Thus the dynamic range, using the average IIP3 of -17.2 dBm, is

$$\begin{aligned} \mathrm{IIP3}-\mathrm{MDS} &= -17.2\ \mathrm{dB}-\left(-49.3\ \mathrm{dB}\right) \\ &= 32.1\ \mathrm{dB} \end{aligned}. \qquad (5.1)$$

The group delay of both variations of this LNA was simulated and are shown in Figure 5.23.

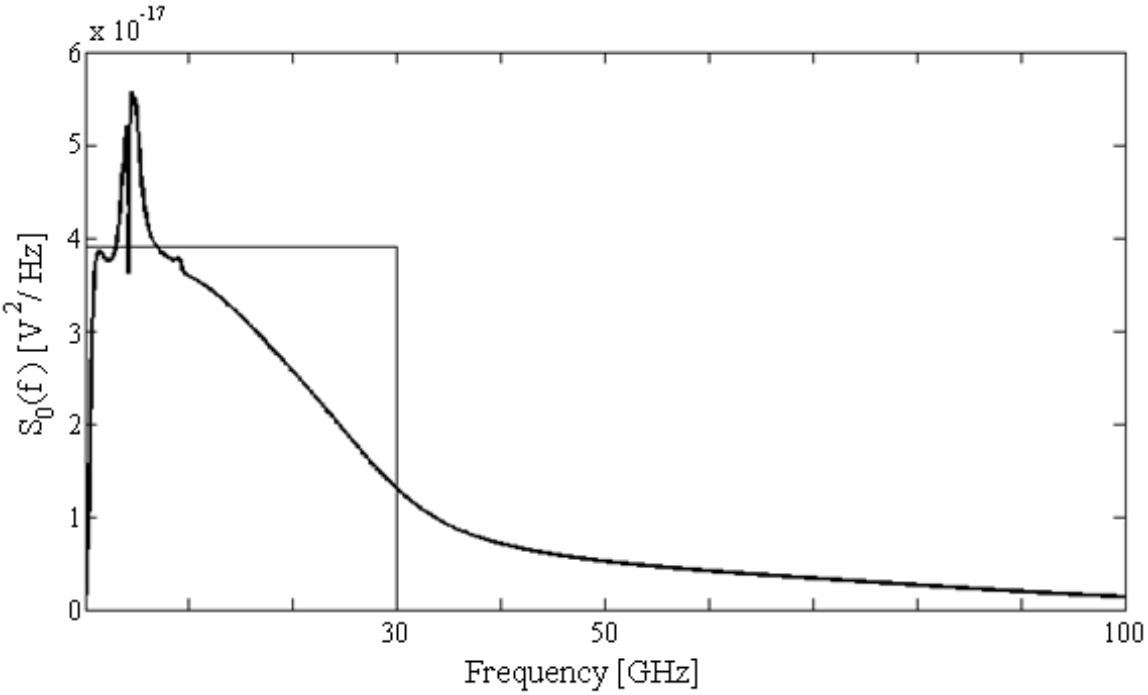

Figure 5.22. Simulated output noise voltage spectral density versus frequency of the linearity optimized LNA.

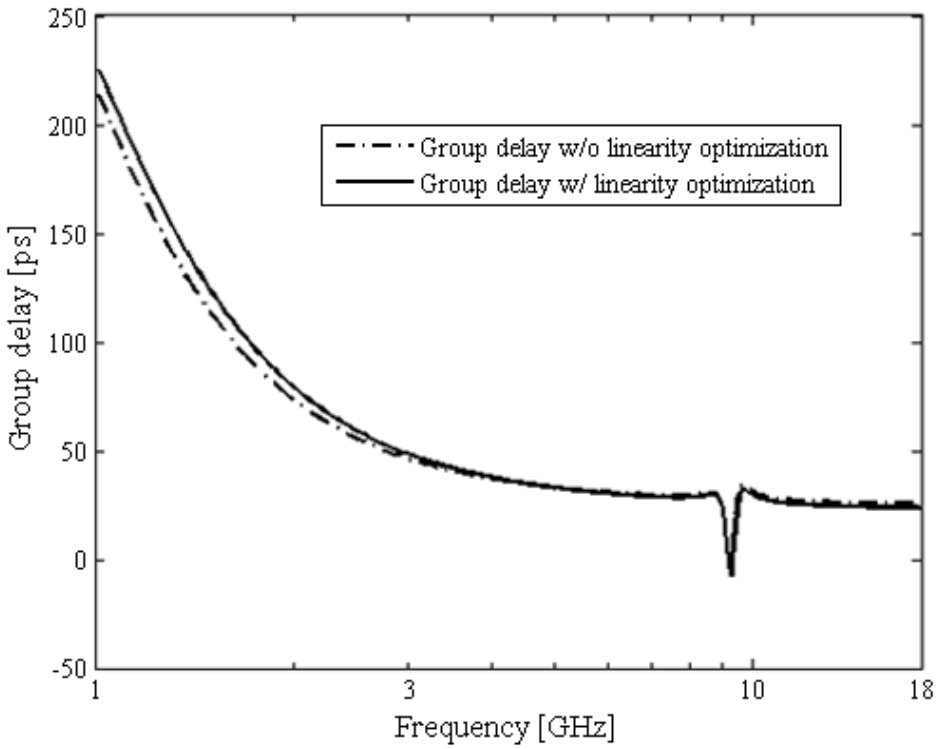

Figure 5.23. Group delay of the LNA with and without linearity optimization over the 1 GHz to 18 GHz band.

5.3.8 Third amplifier stage

If a third amplifier stage is used care should be taken to avoid unnecessary peaking in the frequency response due to the second stage load inductor. An additional parallel resistance could be used to limit the gain at high frequencies. Peaking will increase the gain of the signal which reduces the IIP3 of the third stage further.

5.3.9 Final LNA specifications

The final specifications of both the LNA with and without linearity improvement are given in Table 5.5.

Table 5.5. Final specifications of the 1-18 GHz LNAs designed in the 8HP process

	BW [GHz]	**S_{11} [dB]**	**S_{21} [dB]**	**NF [dB]**	**IIP3 [dBm]**	**P [mW]**
w/o linearity optimization	1–18	< -10	21	2.1–3.6	-22.6 @ 4.2 GHz	12.75
with linearity optimization	1–18	< -9.8	20	2.2–3.9	-14.5 @ 4.2 GHz	23.25

5.4 8HP DESIGN AT 60 GHZ

Wideband wireless network schemes such as the UWB have mostly failed to deliver on their promise of high bandwidth since they are reliant on extensive baseband processing which quickly becomes complex and consume large amounts of power [**16**]. In contrast there is an abundance of bandwidth available in the unlicensed part of the mm-wave frequency band (57–64 GHz), which can be leveraged against power consumption in mobile devices. In addition Silicon Germanium (SiGe) technology has offered a low cost alternative to the more traditional III-V compounds making mm-wave radios a very attractive prospect.

The use of the LC-ladder and capacitive feedback LNA configuration at mm-wave frequencies is discussed below. Simulation results of a design are given with remarks on the effectiveness of the IMN and also suggestions for alternative design methods.

Since the Q-factor of the on-chip spiral inductors decay very rapidly above 30 GHz [**56**] microstrip transmission line inductors, also discussed in Section 2.7, were used throughout in the 60 GHz design.

The design equations discussed in Chapter 4 were used in the same way as in Section 5.3.1. The component and collector current values that were obtained are given in Table 5.6, and the input impedance, *S*-parameters and NF results are shown in Figure 5.24 and Figure 5.25.

Table 5.6. Calculated component values of the 60 GHz LNA.

Symbol	Calculated value
C_1	177 fF
C_F ($C_{BC} = C_\mu$)	0 fF
L_1	140 pH
L_2	124 pH
L_3	540 pH
R_{L1}	117 Ω
I_{C1}	5 mA
I_{C2}	12 mA

Most importantly it should be noted from the results that the mathematical model no longer describes the performance of the LNA with sufficient accuracy at such high frequencies. Various possible reasons for this have been given in Section 4.10. Figure 5.24 shows that the resonant frequencies of the input matching network are not predicted correctly. The calculated gain is also less than the simulated value and the calculated NF more, as seen in Figure 5.25.

The LNA achieves relatively good performance for a 60 GHz LNA compared to the published results of other LNA configurations in Table 5.7. Although it can be seen that the very low input reflection coefficient is not due to input impedance at the centre of the matched band being equal to 50 Ω and centred on the operating frequency, but rather due to the upper resonant peak of the input matching network being close to 60 GHz and approximately equal to 50 Ω.

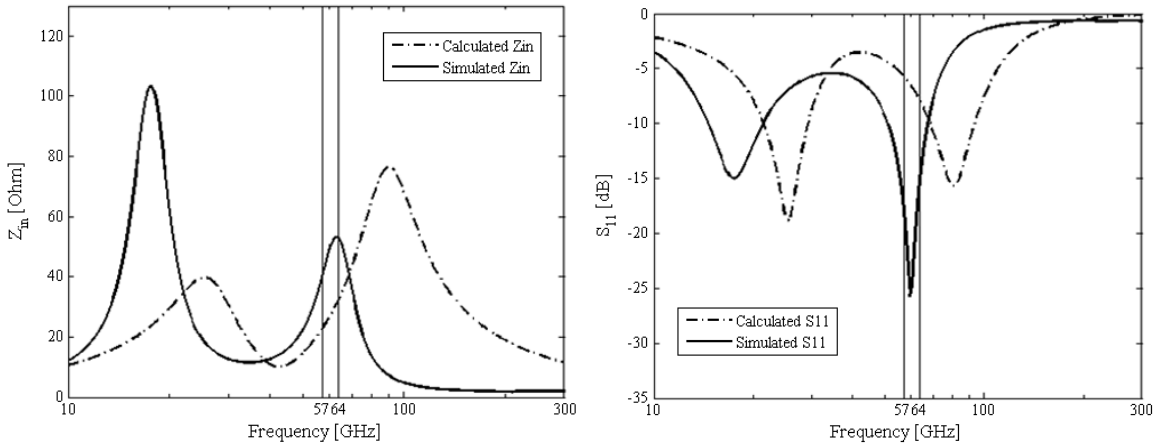

Figure 5.24. Calculated and simulated input impedance and S_{11} of the 60 GHz LNA.

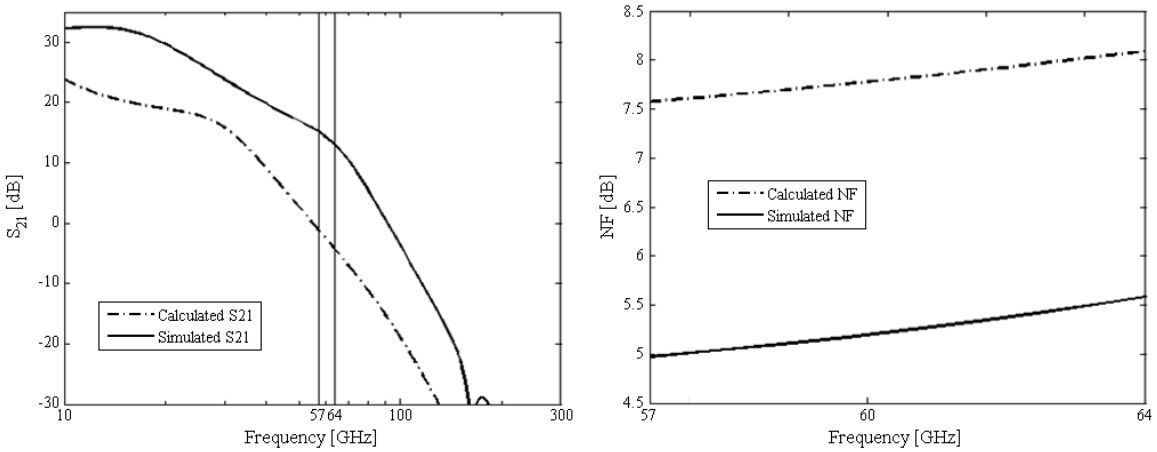

Figure 5.25. Calculated and simulated forward gain and NF of the 60 GHz LNA.

Table 5.7. 60 GHz LNA results and comparison to published results of other LNA configurations.

Ref.	Technology	f [GHz]	S_{11} [dB]	S_{21} [dB]	NF [dB]	IIP3 [dBm]	P_{1dB} [dBm]	P [mW]
This work	0.13 µm SiGe BiCMOS	60	< -15	14.2	5.2	-8.4	-20	25.5
[**66**]	90 nm CMOS	58	< -10	14.6	5.5	-6.8	-	24
[**67**]	0.13 µm SiGe BiCMOS	60	< -10	18	5	-	-	7.5
[**68**]	0.25 µm SiGe BiCMOS	60	< -10	18	6.7	-	-18	20
[**69**]	0.12 µm SiGe BiCMOS	58	< -10	14.8	4.1	-2	-12	8.1

The above observation means that the part of the IMN determining the lower corner frequency is no longer important since it is the resonant frequency of the upper corner frequency components that now provide conjugate input matching. The components that determine the lower corner frequency are C_2 and L_1. The capacitance is synthesized using the Miller impedance at the base of the transistor and as such cannot be removed. The inductor is implemented as a transmission line which is not only used for matching but also acts as a bias choke. Since the bias choke remains a necessary part of the circuit this inductor cannot simply be removed, however if it is desired to save the chip area occupied by L_1 it can be removed and a large off-chip bias choke could be used instead without significantly affecting the performance of the LNA. The simulated results of a circuit where this has been applied are shown in Figure 5.26 and Figure 5.27.

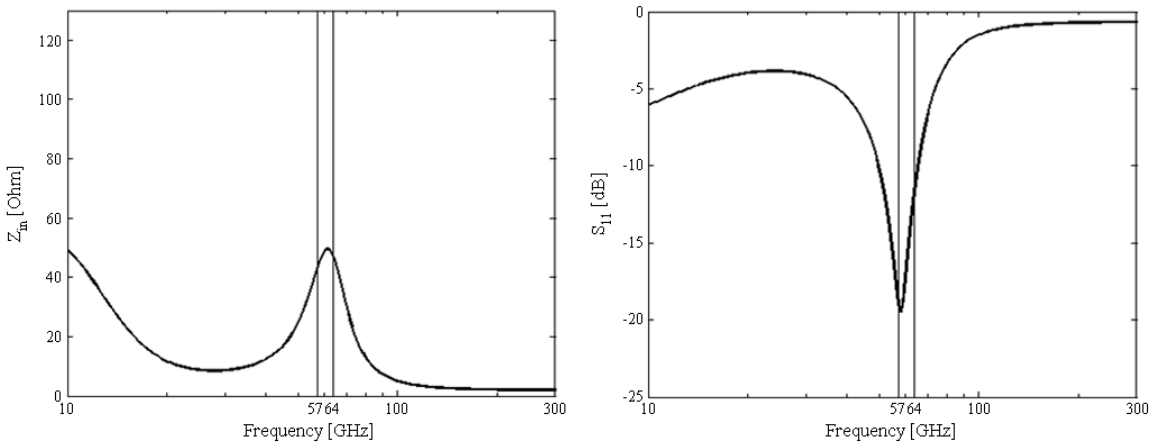

Figure 5.26. Simulated input impedance and S_{11} of the 60 GHz LNA without L_1.

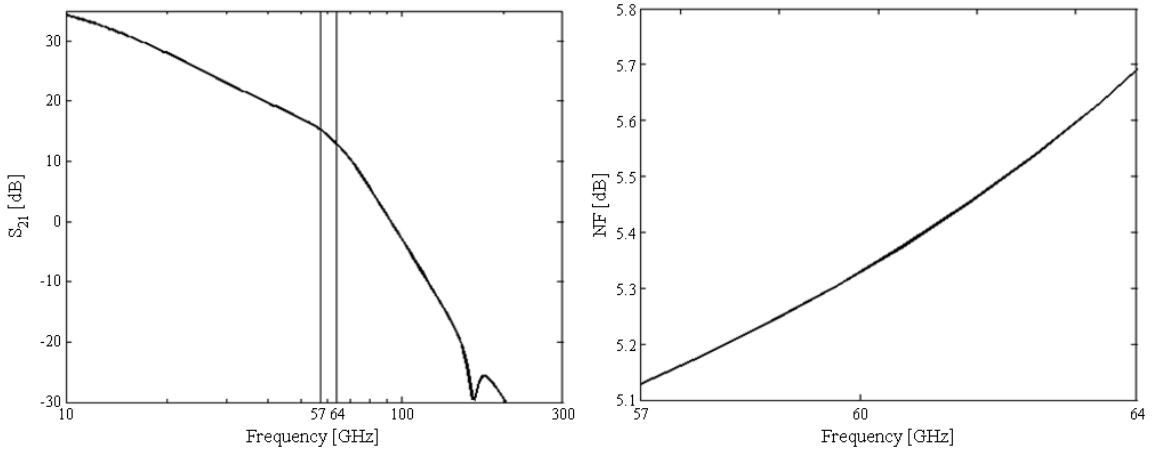

Figure 5.27. Simulated forward gain and NF of the 60 GHz LNA without L_1.

In conclusion, although results comparable to those in literature were obtained, the theory of the design process is no longer consistent with simulated results due to various second

order effects present when operating close to the device f_T; it is therefore suggested that a distributed design approach, discussed in Section 2.5, should be applied to mm-wave design with the current transistor technology.

Lastly it is noted that parasitics have a very large impact on circuit performance above 20 GHz and especially at 60 GHz. This requires EM simulations of the final layout to ensure extraction of all parasitic elements that will be present in a fabricated LNA; however since the conclusion is not to use the discussed design approach at 60 GHz with current transistor technology, and since a design at 60 GHz is not the focus of this study but rather wideband LNAs at lower frequencies, such simulations were not performed.

5.5 7WL DESIGN FOR 3-14 GHZ

5.5.1 Initial design

The design process followed for the LNA in the 7WL for fabrication was identical to process described in Section 5.3. The design specifications were kept the same except for the frequency range which was changed to the 3 GHz to 14 GHz range since the process has a lower f_T meaning less gain could be achieved per stage due to the GBP. A voltage gain of approximately 3.3 per stage or 10 dB is achievable over this frequency band. Because of this limitation it was necessary to add a third amplifier stage with a gain of 10 dB as suggested in Section 4.12 to attain the required overall gain of 20 dB, with the first and second stage together providing a flat 10 dB gain over the frequency band. Transistor emitter lengths of 20 µm and a 1.8 V power supply were used.

The values in Table 5.8 were derived for the initial design and the calculated and simulated *S*-parameters and NF results are shown in Figure 5.28 and Figure 5.29. Again the calculated *S*-parameters track the simulations sufficiently, and the calculated NF is very accurate in this case.

Table 5.8. Initial component values derived using the design equations and the final optimized values.

Symbol	Value	Optimized value
C_1	227 fF	150 fF
C_F	208 fF	50 fF
L_1	2.65 nH	3.7 nH
L_2	568 pH	525 pH
L_3	600 pH	293 pH
R_{L1}	325 Ω	90 Ω
R_{L2}	80 Ω	70 Ω
R_{L3}	75 Ω	60 Ω
I_{C1}	0.66 mA	2.5 mA
I_{C2}	2.7 mA	2.7 mA
I_{C3}	2.7 mA	2.7 mA

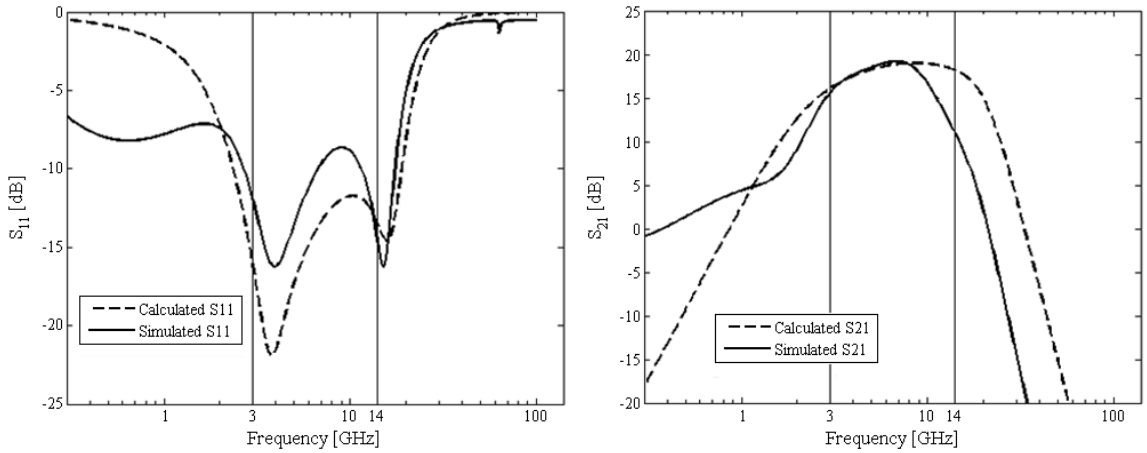

Figure 5.28. Calculated and simulated *S*-parameters without any optimization.

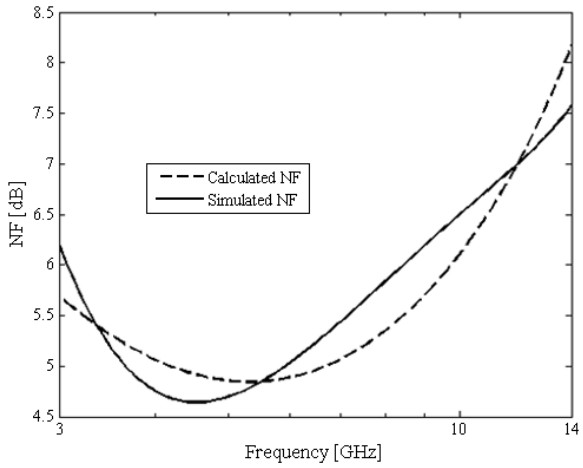

Figure 5.29. Calculated and simulated NF without any optimization.

5.5.2 Noise optimization

Noise optimization was applied to the LNA with the same procedure followed in Section 5.3.2. Using (4.56) it was found that a first stage gain of 9.8 dB is required to meet a maximum NF requirement of 6 dB, taking into account a potential subsequent NF improvement of 2 dB. The first stage gain was adjusted as such and the collector current and load resistance optimized. The use of an additional load capacitance (C_{L1}) was not feasible in this case as the reduction in gain was too large, however S_{11} remained below -10 dB after this optimization. Finally the passive component values were also optimized.

The noise optimized component and current values are shown in Table 5.8. The initial noise contribution of the various noise sources and those after optimization are plotted in Figure 5.30 and the final *S*-parameters and improved NF plots are shown in Figure 5.31 and Figure 5.32 respectively. An improvement of 2.68 dB, 3.07 dB and 1.79 dB has been obtained at the lower corner-, upper corner- and minimum NF frequencies respectively compared to the initial NF in Figure 5.29. The minimum NF is 2.8 dB at 5.3 GHz and the maximum 4.3 dB at the upper corner frequency.

The average gain of the final amplifier is 20.7 dB which falls to 19.6 dB at 3 GHz and 17.8 dB at 14 GHz, the lower- and upper corner frequencies. The inductive load of the second stage causes peaking in the S_{21} response at high frequencies with the maximum value of 21.4 dB at 8.6 GHz. The simulated input reflection coefficient in Figure 5.31 remains below -10 dB. In this case the gain and input return loss specifications have been met with the NF only going slightly above 4 dB at frequencies higher than 12.7 GHz.

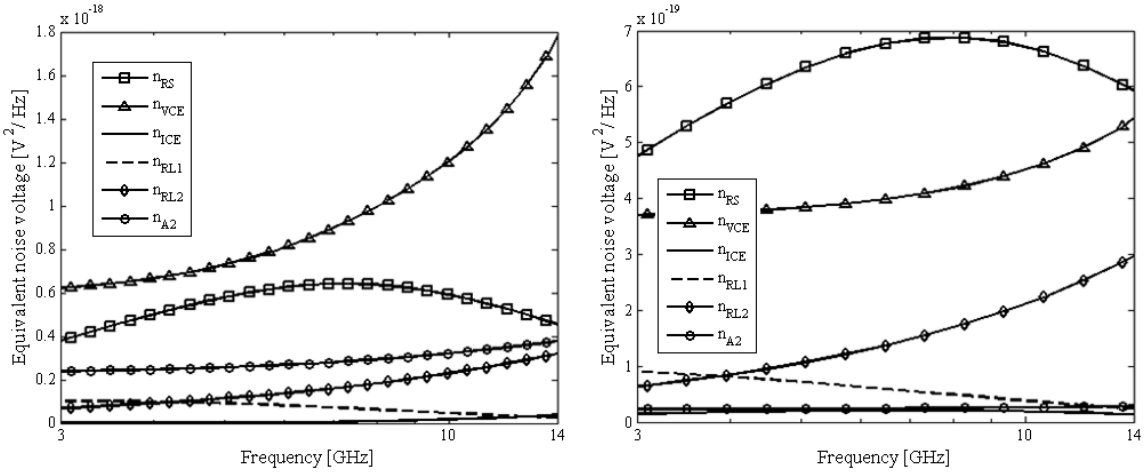

Figure 5.30. Noise contribution of the various noise sources before optimization (left) and after the noise optimization process (right).

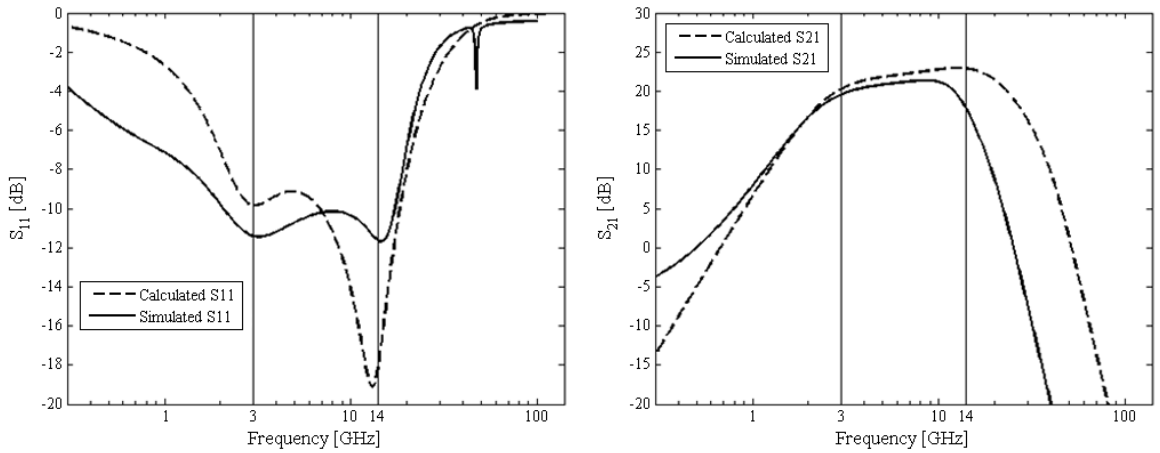

Figure 5.31. Final simulated and calculated S_{11} and S_{21} after optimization of the passive components and collector current.

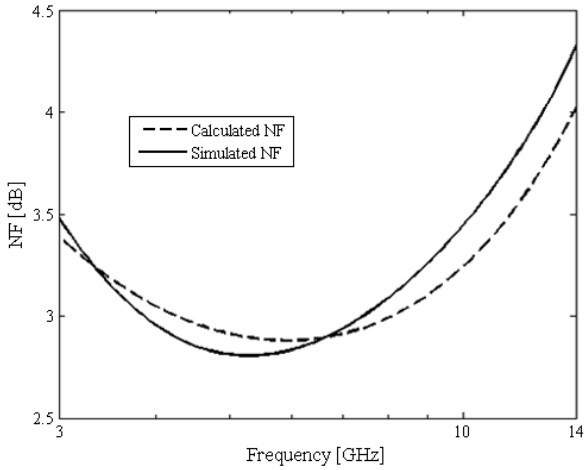

Figure 5.32. Calculated and simulated NF after optimization of the passive components and collector current.

Two observations regarding the correlation between the calculated and simulated results were made which indicate improvements that are still required to make it more accurate. Firstly, the calculated gain is overestimated at high frequencies where the finite GBP of the transistor causes a roll-off in the simulated gain. The effect of the GBP should thus be included in the mathematical model if it is to be used in designs operating at the limits of the transistor technology. Secondly, it was found that the Q-factor of the inductors has a very large impact on the calculated NF and also impacts the *S*-parameters somewhat. It is only once the correct Q-factors were found that the good NF correlation was obtained. This means that the selection of average Q-factors for the inductors which are assumed constant over frequency is not an acceptable simplification and frequency dependent Q-factor modelling based on inductor dimensions should be included.

A large spike is also observed in the calculated S_{11} at the upper corner which is not present in the simulated result. It was found that removing the capacitance of the bond pad from the total input shunt capacitance C_1 removed this spike and although there was still a 2 dB difference in the two curves the shape was similar. This raises the question as to whether the capacitance of the bond pad is modelled correctly in the 7WL HIT-kit. It should be possible to clarify this from the measured results.

The simulated reverse isolation (S_{12}) of the LNA is less than -56 dB over the frequency band of interest. As suggested in Section 5.3.2 the load resistance of the third amplifier stage was used to provide output matching. A 75 Ω resistance was used to achieve the desired gain with the least possible collector current while at least maintaining S_{22} < -10 dB, and proved very effective with the final simulated S_{22} remaining below -13.5 dB over the operating frequency range.

5.5.3 Stability

The minimum value of the *K* stability factor is 52.6 due to the good reverse isolation and output matching. The minimum of the B_f factor is 0.956 and since it is above zero and the *K*-factor above 1 the LNA is unconditionally stable over the entire frequency range [**65**]. Simulations were also done up to the f_{max} (280 GHz) of the transistor to ensure that there are no instabilities at frequencies beyond the range of interest.

5.5.4 Monte Carlo analysis and temperature sweep

To find the sensitivity of the design to process parameter variations a Monte Carlo analysis was performed. The variations in the *S*-parameters with 100 simulated cases are shown in Figure 5.33 and that of the NF in Figure 5.34.

S_{11} varies by approximately 2 dB over most of the frequency band with slightly larger deviations just below 14 GHz. The input return loss remains below -10 dB for most of the simulated cases and never goes above -9.5 dB.

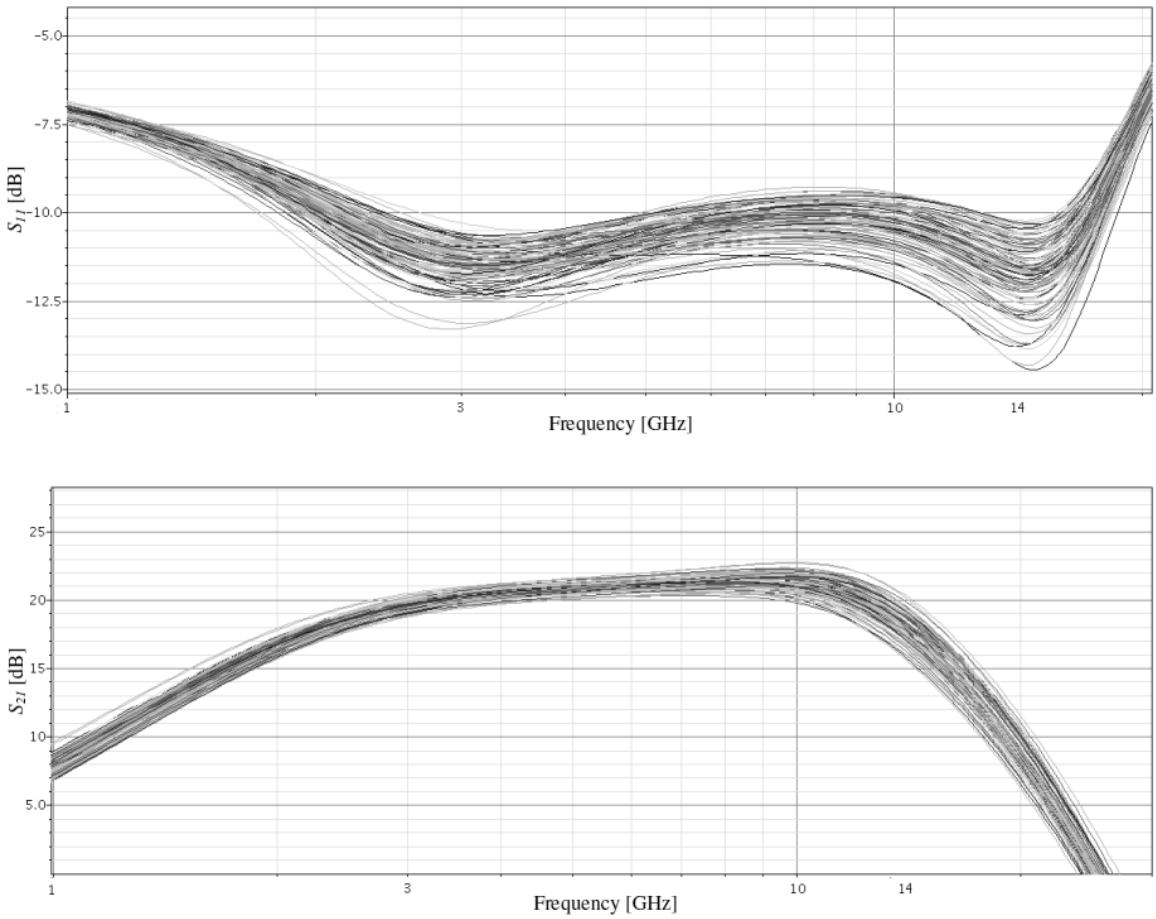

Figure 5.33. Variation in S_{11} (top) and S_{21} (bottom) resulting from a Monte Carlo analysis.

The S_{21} varies by 2 dB over most of the operating range, only showing larger deviations in the region where peaking due to the inductive load is present. The gain is between 19 and 21 dB below 4.3 GHz, between 20 and 22 dB up to 7 GHz, and then the gain variation increases to a maximum of 4 dB at 14 GHz. In most cases the gain at 14 GHz remains above 17 dB which is the designed gain and also the -3 dB cut-off with the designed average gain of 20 dB; though in some cases the effective -3 dB cut-off point may be less than 14 GHz when the low frequency gain is increased above 20 dB by process variations.

The NF variation is 1 dB over most of the frequency band and increases slightly above 10 GHz. The NF is less than 4 dB from 3 GHz to 10 GHz, and is also the maximum NF at these respective frequencies. NF remains below 5 dB up to 14 GHz.

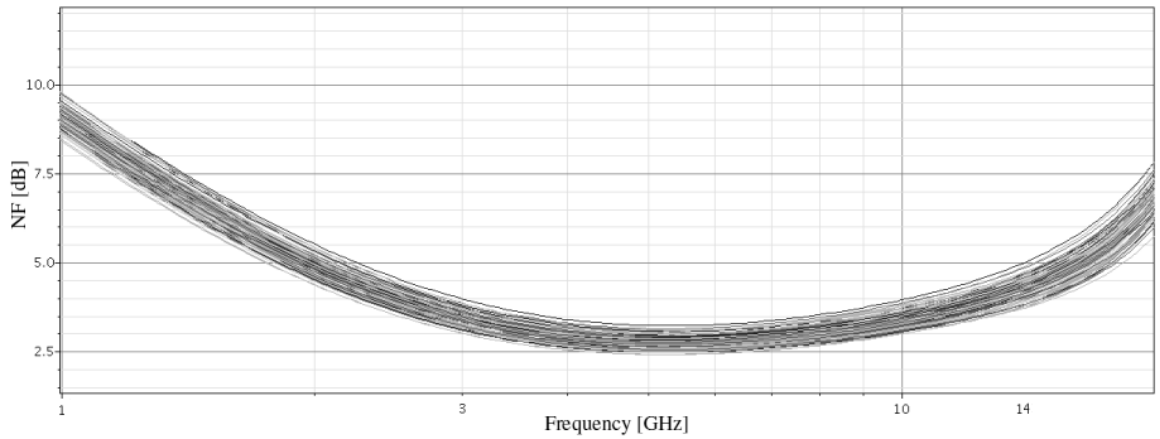

Figure 5.34. Variation in NF resulting from a Monte Carlo analysis.

A temperature sweep was performed to test the robustness of the LNA over a -55 °C to 125 °C temperature range. The results are shown in Figure 5.35 and Figure 5.36. Temperature variations have a relatively small impact on the input return loss and since S_{11} remains below -9 dB the variation will not be a concern in most applications. The gain however is very temperature dependent since it is directly dependent on temperature through V_T when emitter degeneration is not used. S_{21} varies between 14.5 dB at 125 °C and 27 dB at -55 °C below 10 GHz which is a very large 12.5 dB variation. Over the 0 °C to 85 °C commercial temperature range the gain varies from 17 dB to 23 dB, which is closer to the specified 18-22 dB gain.

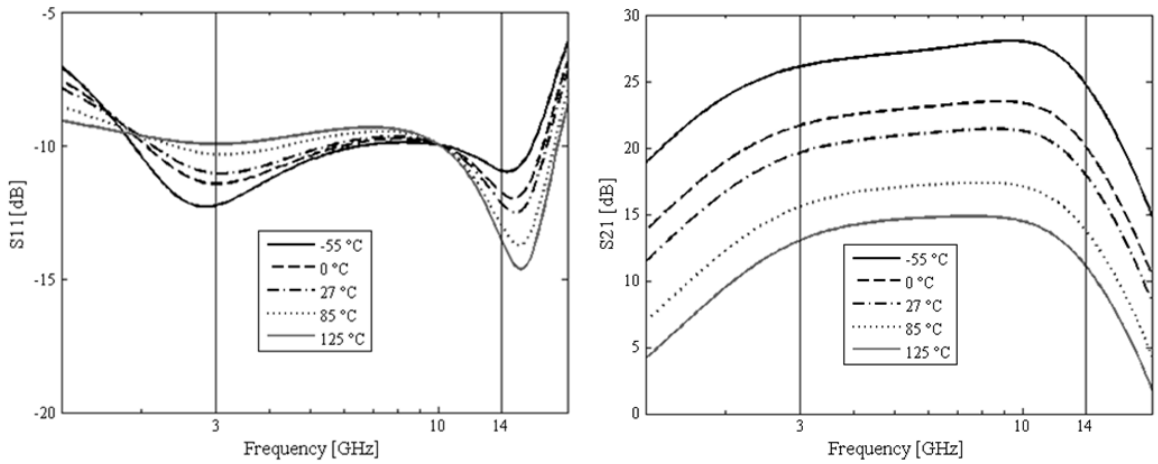

Figure 5.35. S_{11} and S_{21} variation with temperature from -55 °C to 125 °C.

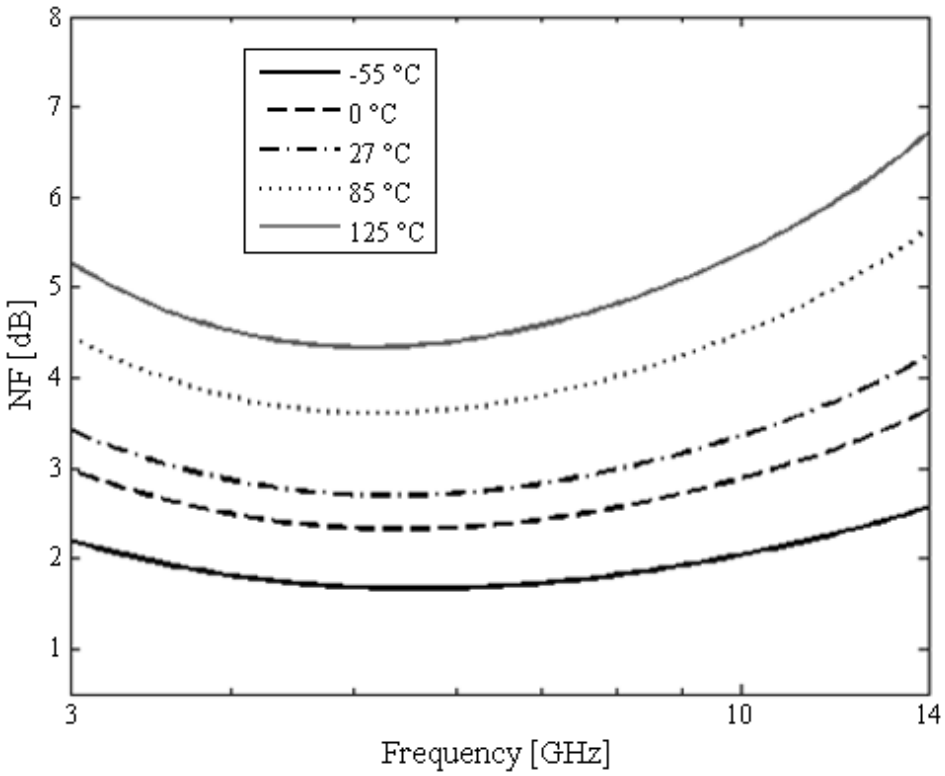

Figure 5.36. NF variation with temperature swept from -55 °C to 125 °C.

The total NF variation is approximately 3 dB below 10 GHz and increases to 4 dB at 14 GHz. At both 85 °C and 125 °C the NF is above the specified 4 dB over most of the operating frequency range.

5.5.5 Linearity of the LNA and its improvement

The linearity of the noise optimized LNA was again determined by simulating the P_{1dB} intercept point and IIP3 using a large signal analysis. The results are plotted in Figure 5.37. In this case the simulated IIP3 is much closer to the approximated IIP3 derived from calculation compared to the design in Section 5.3.5.

The last (third) amplifier stage once again dominates the linearity of the LNA, but the high gain of the first stage at lower frequencies also causes much distortion in the second stage. Therefore both the second and third stage was degenerated with emitter resistors to improve linearity. To compensate for the decreased gain the adjustments shown in Table 5.9 was made to the circuit. The improvement observed in the linearity of the amplifier is shown in Figure 5.38 which shows the plots of the IIP3 and P_{1dB} with and without emitter degeneration.

Once again the P_{1dB} is higher than the IIP3 in some cases. A possible explanation for this has been given at the end of Section 5.3.5.

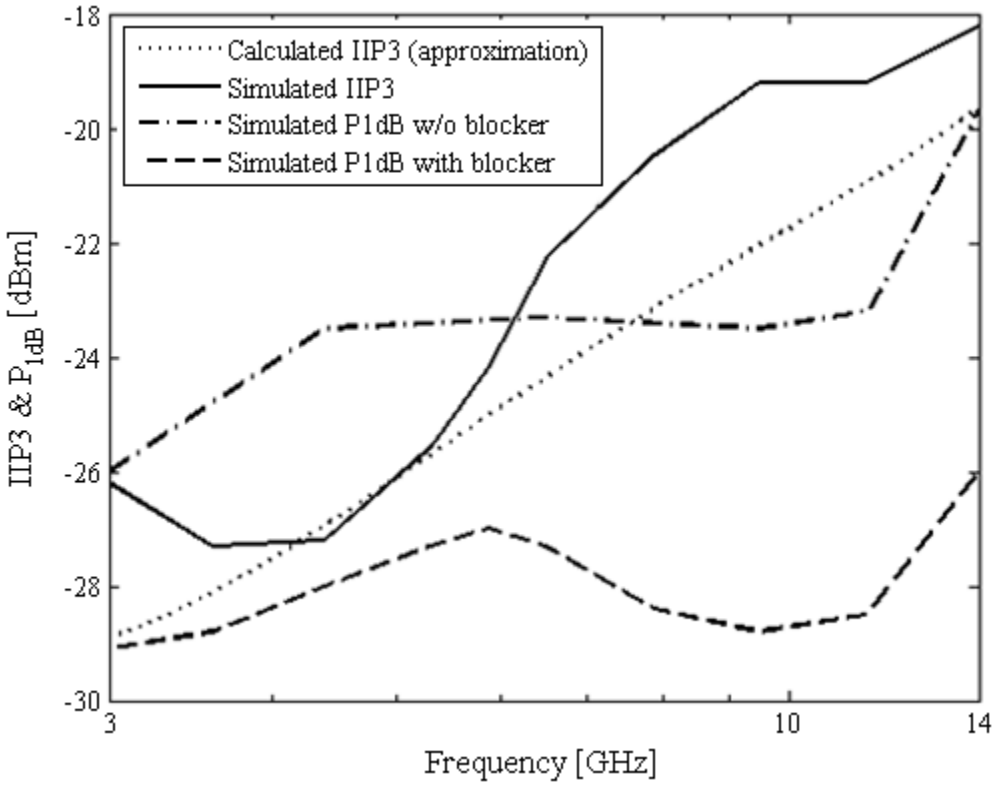

Figure 5.37. Simulated P_{1dB} compression point and IIP3 versus frequency of the noise optimized LNA.

Table 5.9. Changes in component values to compensate for the gain reduction when feedback was added.

Symbol	Original value	Noise optimized	Linearity optimized
L_3	600 pH	293 pH	315 pH
R_{L3}	75 Ω	60 Ω	80 Ω
I_{C2}	2.7 mA	2.7 mA	8 mA
I_{C3}	2.7 mA	2.7 mA	8 mA
R_{E2}	-	-	9 Ω
R_{E3}	-	-	8 Ω

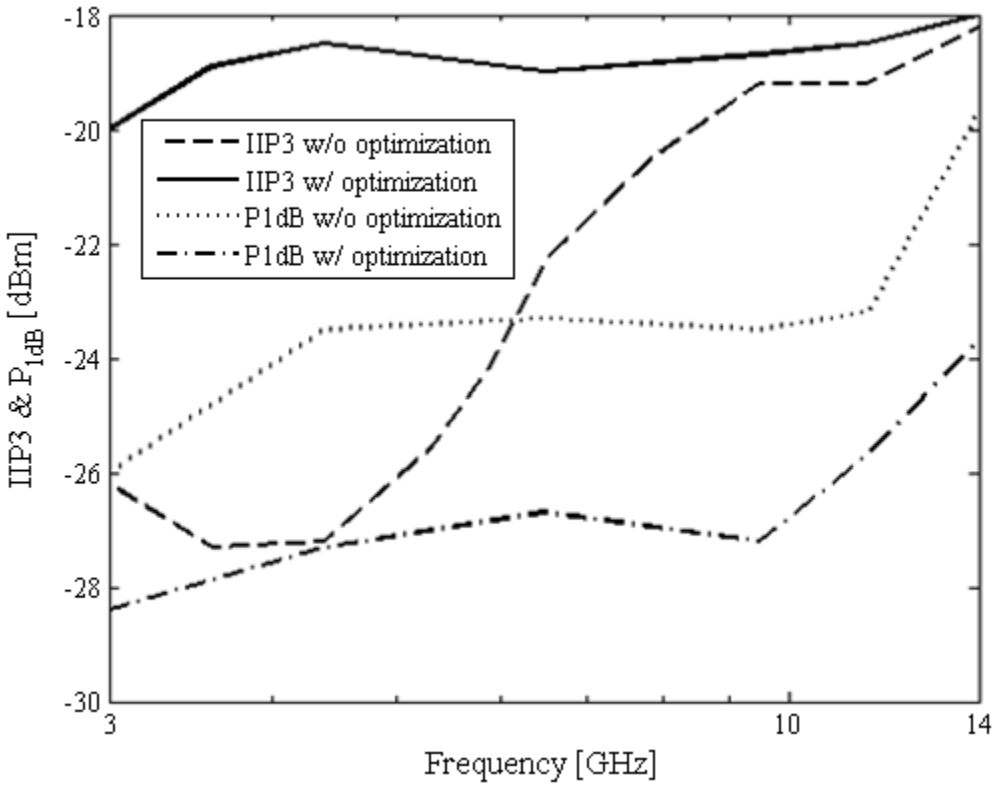

Figure 5.38. Simulated IIP3 and P_{1dB} compression point versus frequency with and without second and third stage emitter degeneration.

5.5.6 Sensitivity of the LNA optimized for linearity

The sensitivity of the LNA to process parameters and temperature was again determined. A Monte Carlo analysis revealed a 2 dB variation in S_{11} similar to the LNA without feedback, however in this case the average value is higher, resulting in a S_{11} between -10 and -9 dB in many cases. NF varies by approximately 1 dB over the entire frequency band and S_{21} by 2 dB and 3 dB in the low to mid and high frequency parts of the band respectively. This is similar to the variation observed without feedback. The -3 dB cut-off frequency is only slightly reduced below 14 GHz in extreme cases.

The NF and input return loss variation with temperature is the same in the case without feedback although the average NF at high frequencies has increased by 0.8 dB. The maximum S_{11} is -8.9 dB and occurs at-55 °C. A large improvement was however observed in the sensitivity of the gain to temperature, with the gain variation, originally between 14.5 and 27 dB from 125 °C to -55 °C, now being reduced to 16.3 and 23.3 dB.

Thus the improvement in the sensitivity of this design is not as significant as in the case presented in Section 5.3.6, but the IIP3 improvement and added temperature stability of the

gain due to its reduced dependence on transistor g_m by the emitter resistors will still warrant the use of this technique in many applications.

5.5.7 Dynamic range and group delay

To determine the dynamic range of the LNA the output noise of the LNA optimized for linearity was simulated. The plot of S_o is shown in Figure 5.39 with the estimated noise bandwidth from 2 GHz to 14 GHz. The average S_o in this band is 69 aV^2/Hz and thus v_{no} is 910 µV, which, in a 50 Ω system, is -30.8 dBm; and when reduced by the 20 dB voltage gain when referred to the input becomes -50.8 dBm, the MDS of the LNA. Thus the dynamic range, using the average optimized IIP3 of -18.8 dBm, is

$$\begin{aligned} \text{IIP3} - \text{MDS} &= -18.8\ \text{dB} - \left(-50.8\ \text{dB}\right) \\ &= 32\ \text{dB} \end{aligned}. \tag{5.2}$$

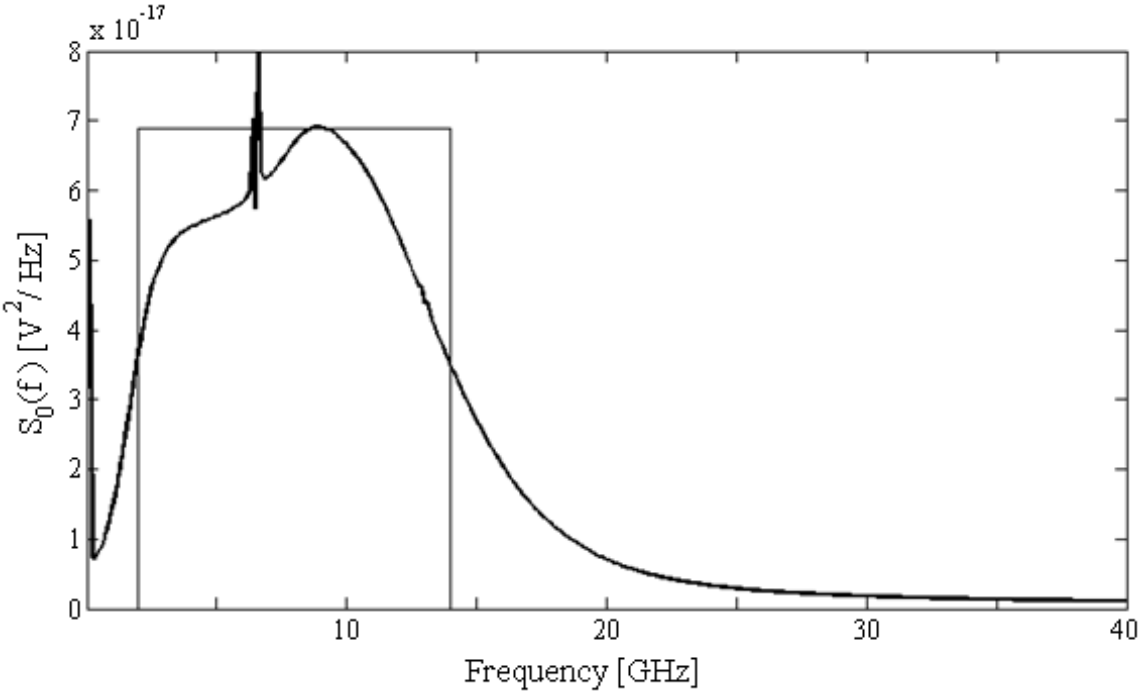

Figure 5.39. Simulated output noise voltage spectral density versus frequency of the linearity optimized LNA.

The group delay of the LNA with and without linearity improvement is given in Figure 5.40.

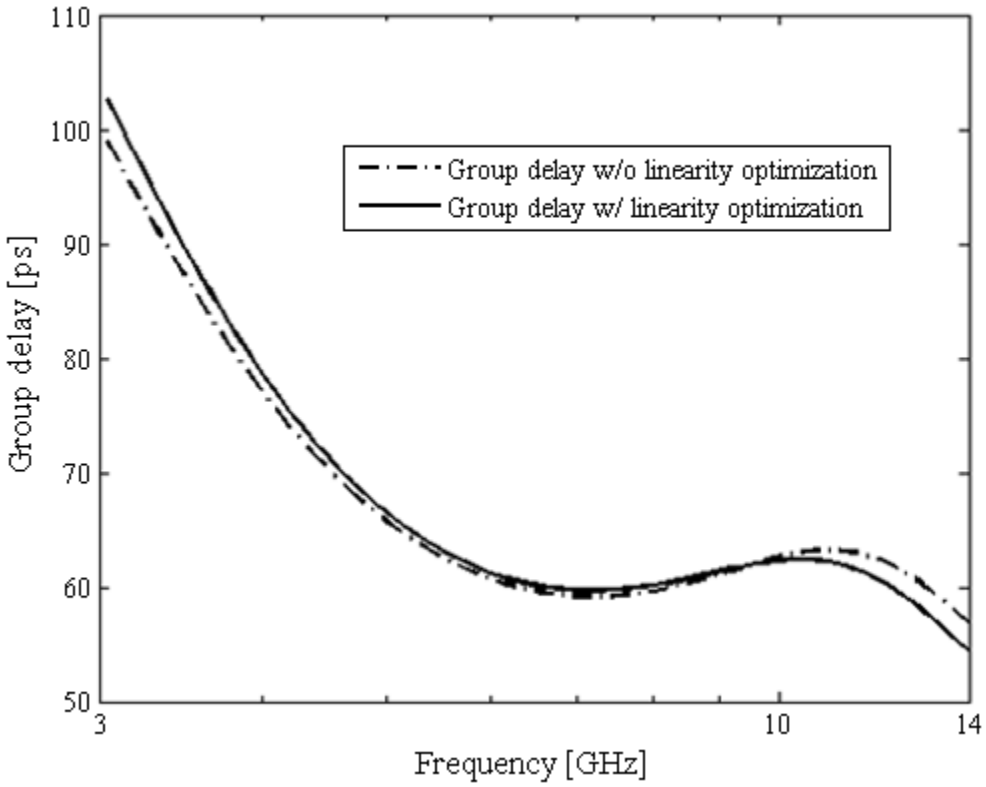

Figure 5.40. Group delay of the LNA with and without linearity improvement over the 3 GHz to 14 GHz band.

5.5.8 Final LNA specifications

The final specifications of both the LNA with and without linearity improvement are given in Table 5.10.

Table 5.10. Final specifications of the 3-14 GHz LNAs designed in the 7WL process.

	BW [GHz]	**S_{11} [dB]**	**S_{21} [dB]**	**NF [dB]**	**IIP3 [dBm]**	**P [mW]**
w/o linearity optimization	3–14	< -10	20.7	2.8–4.3	-22.5 @ 6.5 GHz	14.22
with linearity optimization	3–14	< -9.7	20.1	2.9–4.8	-19.0 @ 6.5 GHz	33.3

5.6 CONCLUSION

Three different LNA designs using the LC-ladder and capacitive shunt-shunt feedback configuration were presented in this chapter. Using the 200 GHz f_T 8HP process in the design for the 1-18 GHz LNA was successful as all the design specifications except P_{1dB}

were met over this very wide frequency band, and even so a good IIP3 of -14.5 dBm was still obtained. The design using the 7WL process also showed good simulations results when considering the much lower f_T of this process.

Although the use of this configuration in a design at 60 GHz produced results comparable to those in literature it was determined not to be the optimal configuration at such high frequencies. This is due to the 57-64 GHz band being a narrow band relative to the 60 GHz centre frequency and as such the wideband design approach is redundant. The mathematical model also does not predict the results accurately when the transistor is operated this close to f_T.

Nonetheless the LC-ladder and capacitive shunt-shunt feedback LNA configuration has proven to be an effective means of implementing very wideband LNAs with good specifications and in many cases improved performance compared to other LNA topologies in literature as shown in Table 1.1 of Chapter 1.

The mathematical model derived in Chapter 4 was also shown to give an accurate description of the LNA performance. Simulated and calculated results showed good correlation in most cases and some comments were made regarding future improvements that could be added to the model to reduce deviations, such as calculating the frequency dependent Q-factor of the inductors to improve the accuracy of noise calculations and also including the effect of the GBP in the gain equations.

CHAPTER 6: LAYOUT AND FABRICATION

6.1 INTRODUCTION

In order to verify the simulated results given in Chapter 5 the LNA was submitted for fabrication in the IBM 7WL 0.18 µm SiGe BiCMOS process on a MPW run. Thirty prototypes were received.

The layout of the LNA was done using the Virtuoso Layout Editor. The HIT-kit provided by IBM offers parameterized cells which greatly simplifies the layout process. Assura was used to do the DRC based on the rule file included in the HIT-kit and also for layout-versus-schematic checking to verify the correctness of the layout. The above process is discussed in this chapter along with the packaging considerations.

A test PCB was designed for the measurement of the LNA performance. The schematic of the bias circuits on this PCB and other related considerations are also discussed.

6.2 CIRCUIT LAYOUTS

Two versions of the LNA was submitted for fabrication as well as a separate first and second amplifier stage to allow verification of those sections of the LNA separately should unforeseen errors prevent correct characterisation of the complete LNA circuits. The first LNA that was implemented is the version without linearity improvement discussed in Section 5.5. The second is the LNA optimized for linearity by adding emitter degeneration in the second and third stages as discussed in Section 5.5.5. The layouts of the individual circuits are shown in Figure 6.1 to Figure 6.4. Additional layout views showing more detail of each amplifier stage are provided in Appendix B.

Spiral inductors were laid out within an 80 µm perimeter free of substrate contacts and other components as suggested in the process documentation and discussed in Section 3.7. A ring of substrate contacts was placed around this perimeter, and sufficient substrate contacts were placed close to the other circuit components as well. An interconnect current density of 1 mA/µm has been used throughout.

The final chip area occupied by the LNA without bonding pads is 740 µm x 750 µm which is 0.555 mm^2. There is however a significant chip area that is not used for the LNA and

could contain other circuits in an integrated system or the three inductors could be placed length wise to minimize the occupied area. The total area covered by the LNA circuit itself is 0.4272 mm^2.

As discussed in Section 2.8 active inductors can be substituted for passive inductors in circuits where noise is not very important and also at the cost of increased power consumption. The advantages of active inductors are increased Q-factors and greatly reduced chip area. If the load inductor of stage 2 (L_3) is implemented as an active inductor since the noise at the second stage output is greatly reduced when referred to the input, the total chip area can be reduced by 78,400 µm^2 if the active inductor circuit is placed in the open area left of C_F in Figure 6.1. That is 18.4 % reduction in chip area.

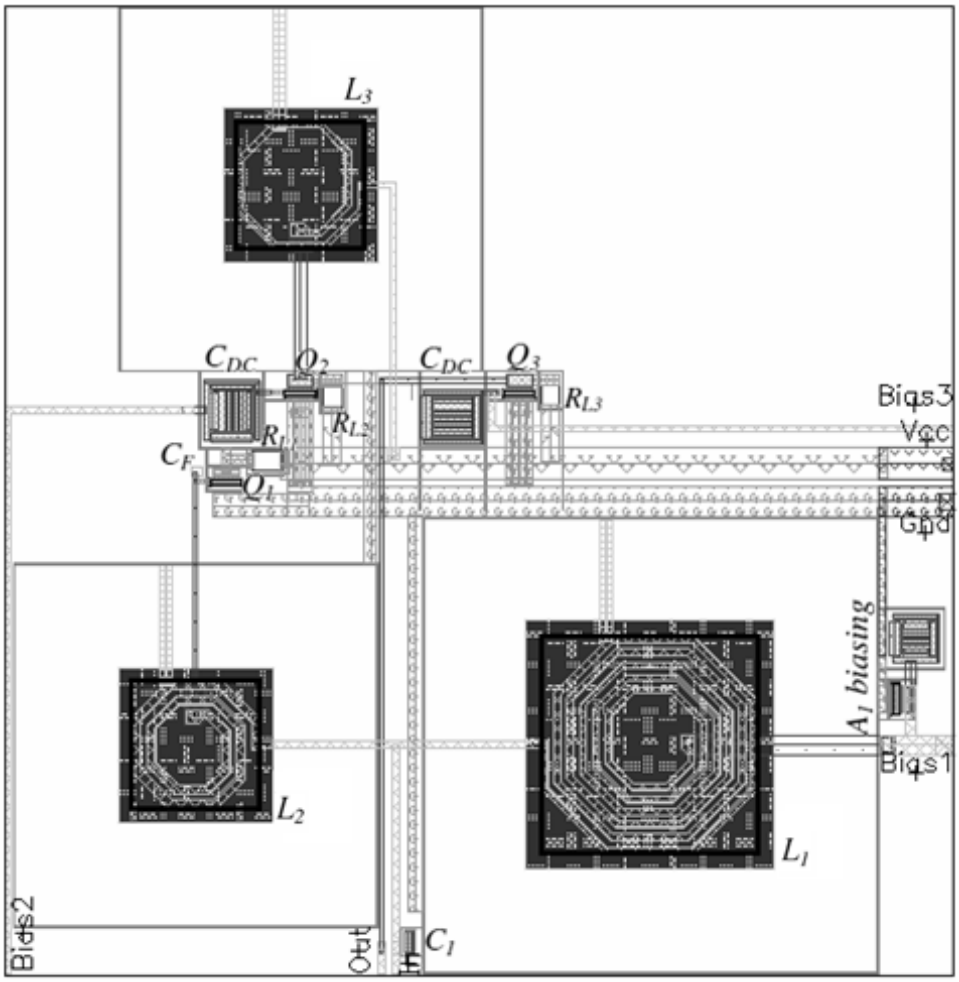

Figure 6.1. Layout of the standard LC-ladder and capacitive shunt-shunt feedback LNA.

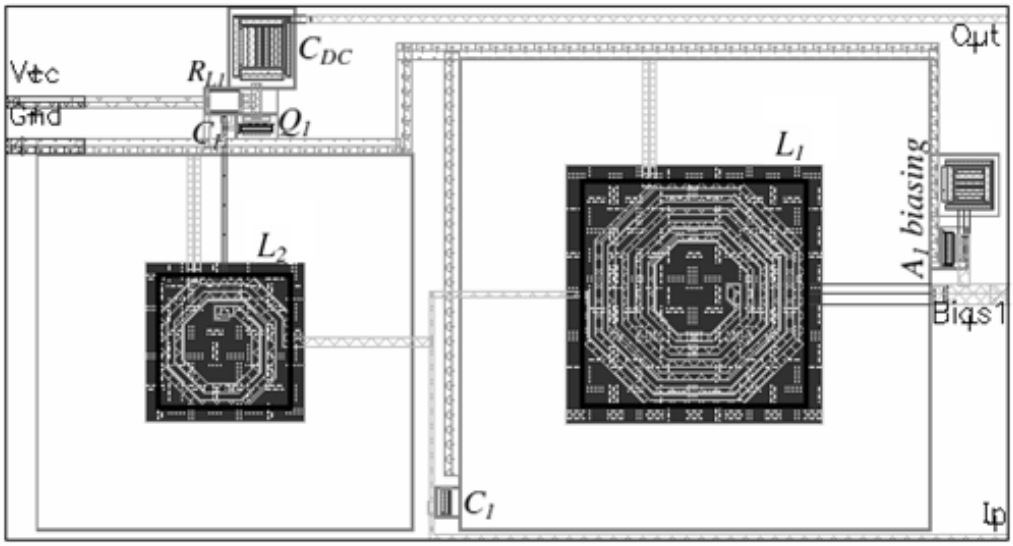

Figure 6.2. Layout of the first amplifier stage and input matching network.

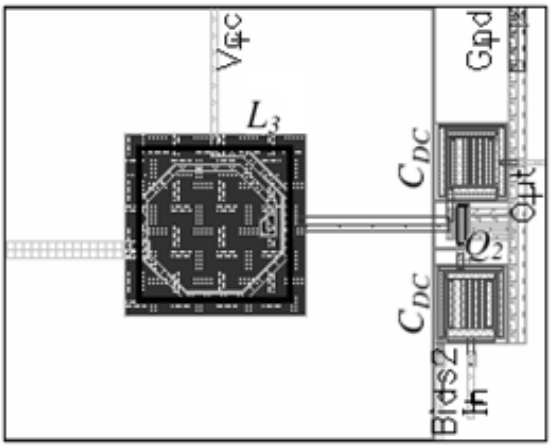

Figure 6.3. Layout of the second amplifier stage.

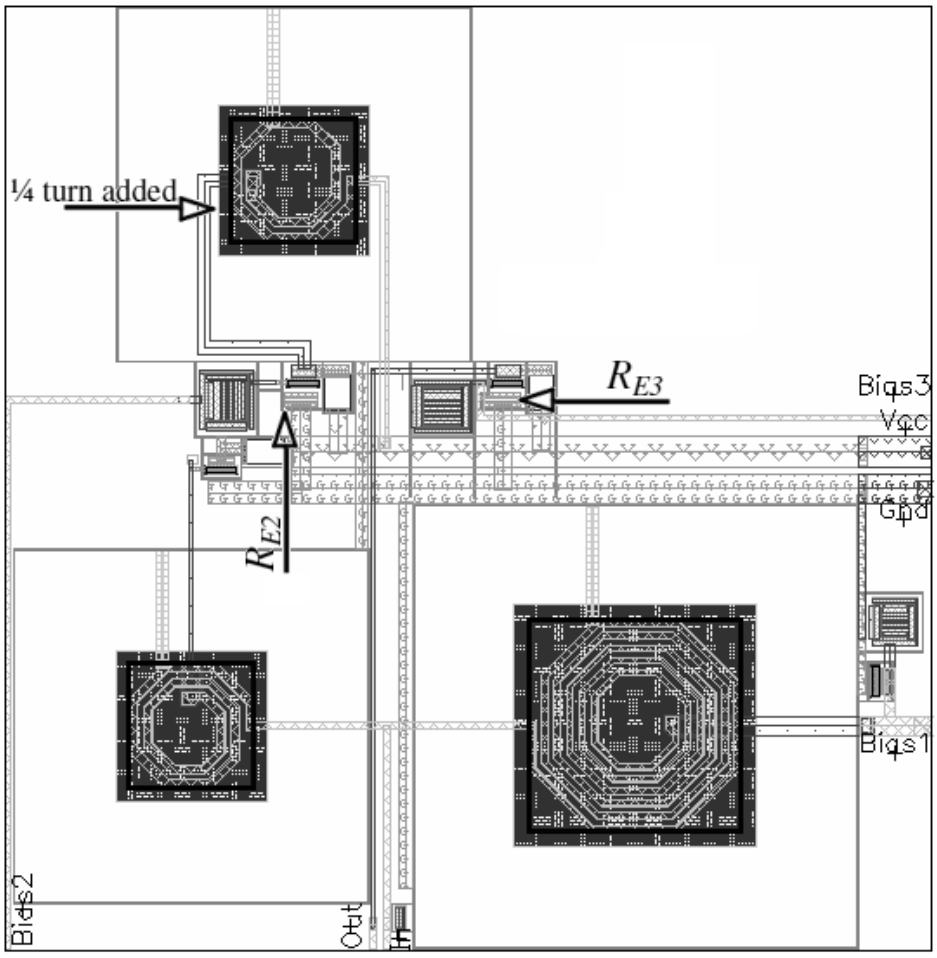

Figure 6.4. Layout of the LC-ladder and capacitive feedback LNA optimized for linearity indicating the additional resistors and modified inductor.

6.3 PHOTOS OF THE FABRICATED CHIP

The fabricated chip was photographed under a microscope. These photos are shown in Figure 6.5 to Figure 6.9. The top metal layers are clearly visible, showing the inductors, capacitors and most of the interconnects. In Figure 6.5 the LNAs are in the top left corner as indicated. The circuits for two other projects are also included on this chip.

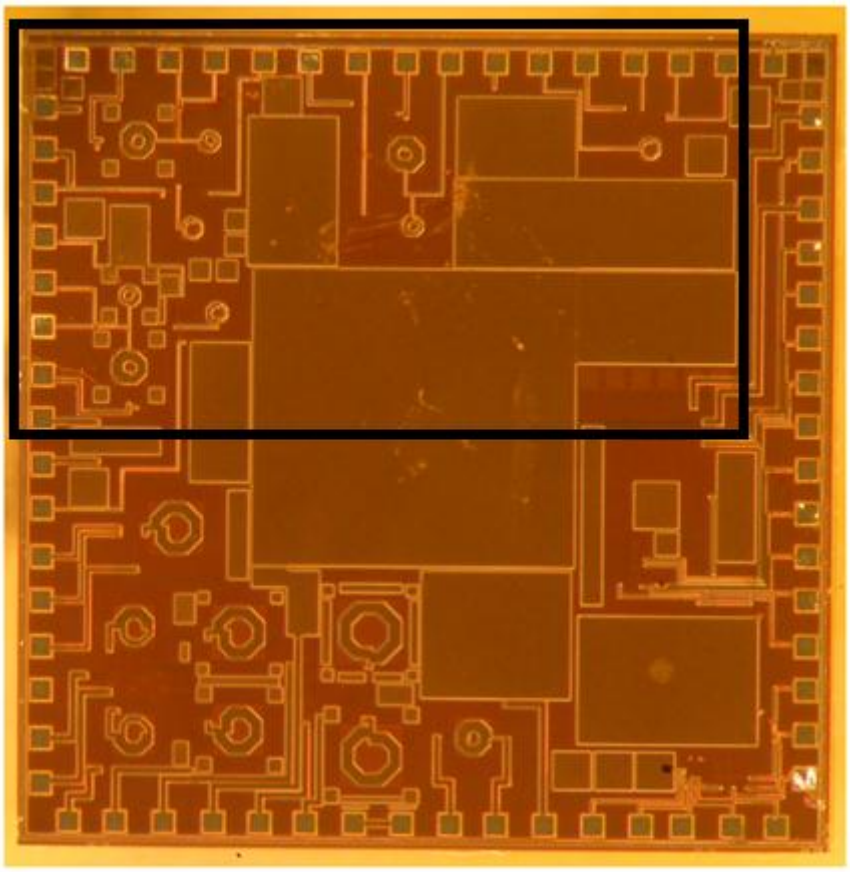

Figure 6.5. Overall view of the fabricated chip showing the LNAs (compare to the bonding diagram in Figure B.7).

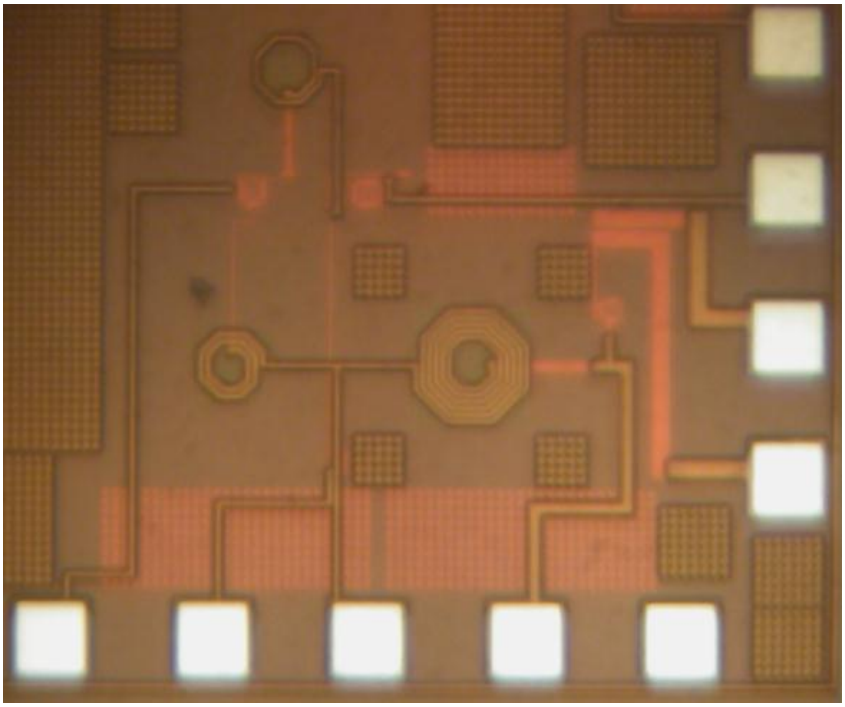

Figure 6.6. Fabricated standard LC-ladder and capacitive shunt-shunt feedback LNA (compare to Figure 6.1).

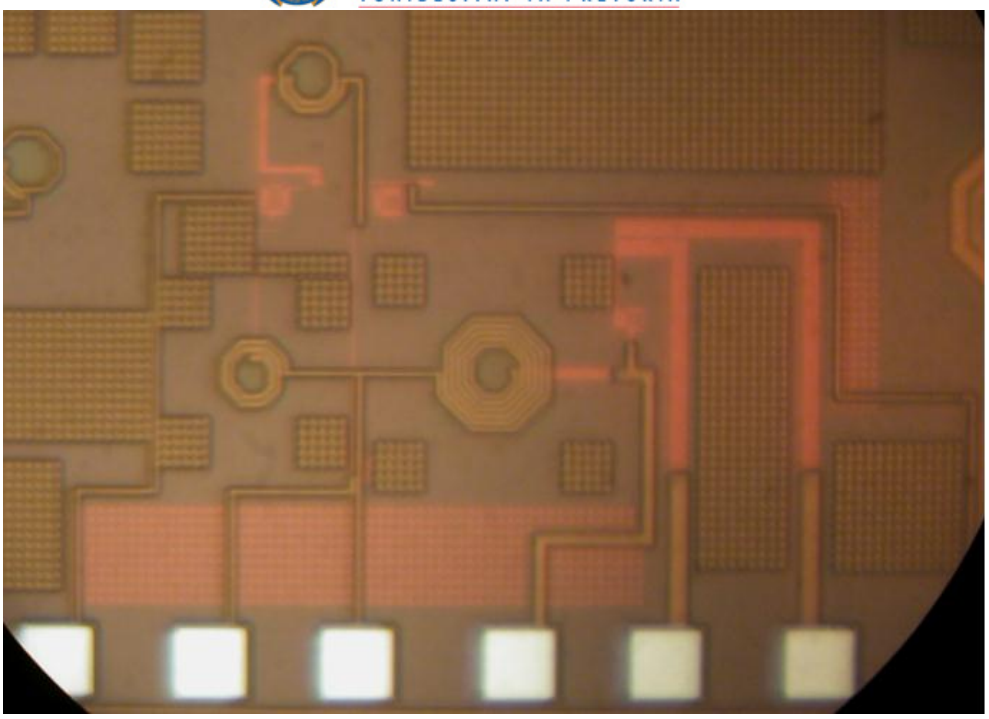

Figure 6.7. Fabricated LC-ladder and capacitive feedback LNA optimized for linearity (compare to Figure 6.4).

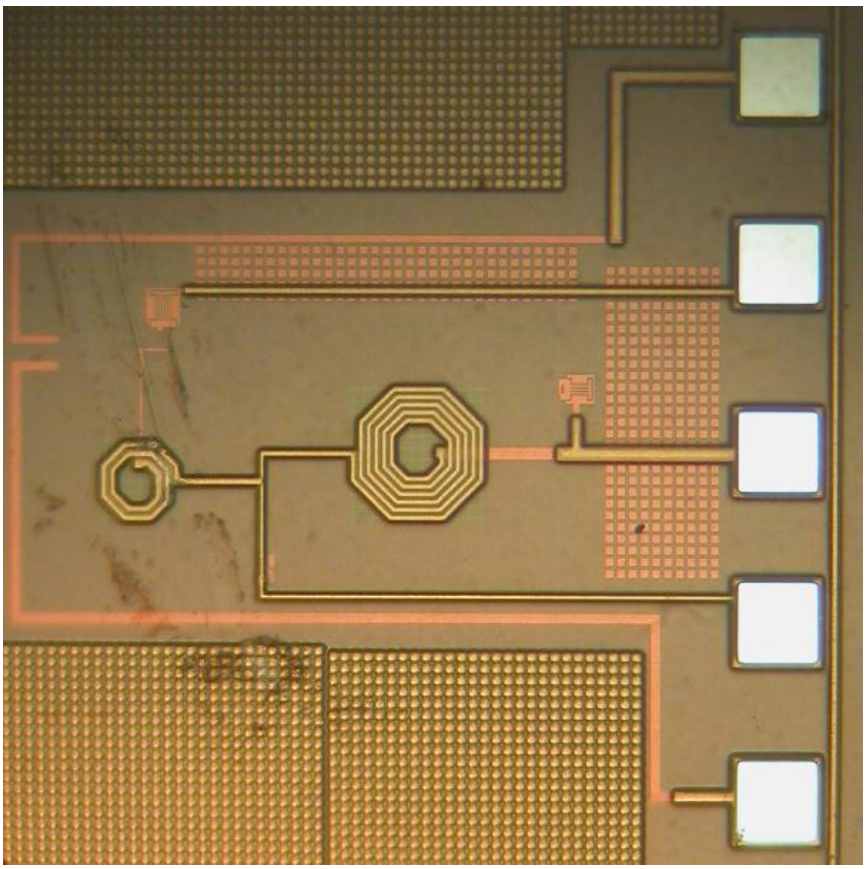

Figure 6.8. Fabricated first amplifier stage and input matching network (compare to Figure 6.2).

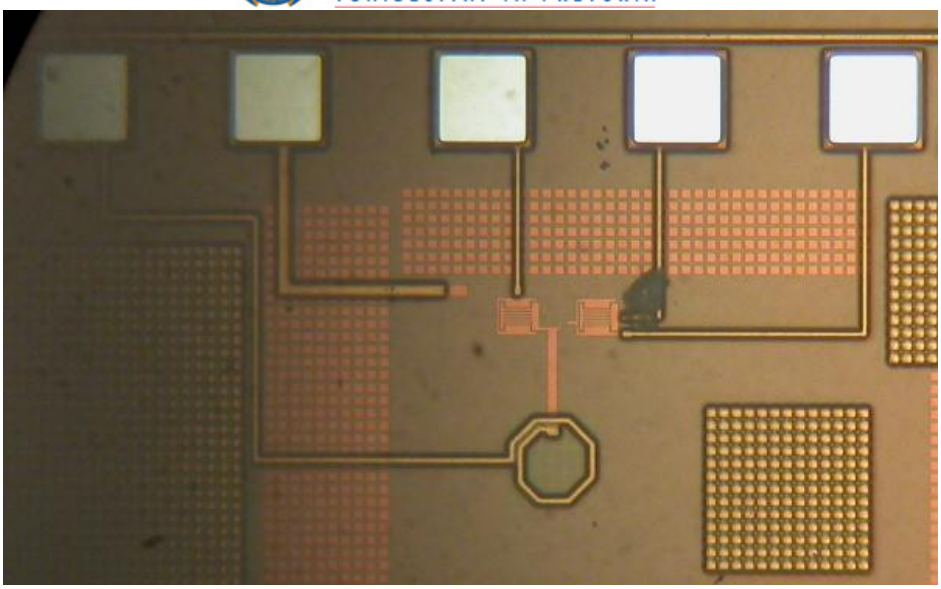

Figure 6.9. Fabricated second amplifier stage (compare to Figure 6.3).

6.4 PACKAGING

Since on-wafer measurement equipment was not available the dies were packaged and mounted on a PCB. Two packaging options were considered namely QFN and BGA packages. Since the solder joints of BGAs are error prone due to uneven heat distribution and cracking due to stresses QFN packages were chosen.

The LNA was fabricated in a MPW run with two other projects on the same chip and as such a 64 pin QFN package was used of which a drawing is shown in Figure 6.10 and the final IC mounted on the test PCB is shown in Figure 6.11. The outer dimensions of the package are 9 mm x 9 mm x 1.4 mm.

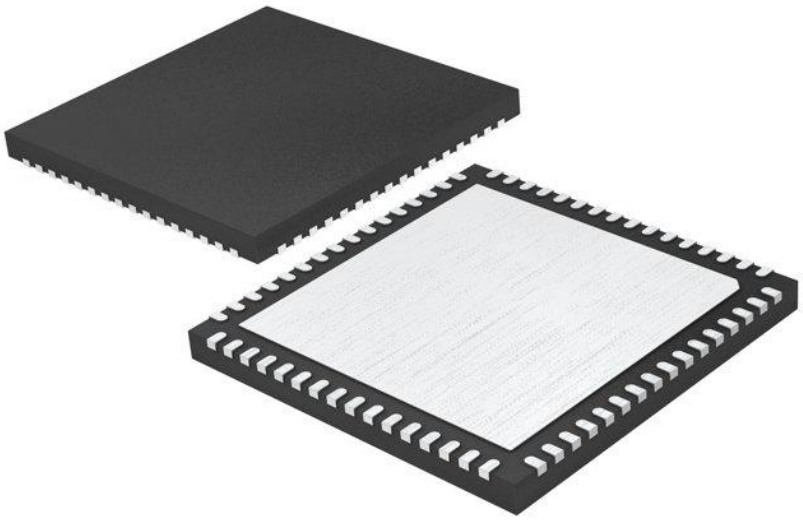

Figure 6.10. Drawing of a 64 pin QFN package.

Figure 6.11. Photo of the 64 pin QFN packaged IC mounted on the test PCB.

6.5 PACKAGE PARASITICS AND ITS EFFECT ON PERFORMANCE

Unfortunately the bond wire inductance in QFN packages is approximately 1 nH per millimetre which greatly attenuates the signal above 10 GHz. To evaluate the effect of the bond wire inductance the circuit in Figure 6.12 was simulated with the most important package parasitics included. Since the package model was not available 1 nH inductance was assumed for each bond wire. The bond pad at the input is not shown since it has already been absorbed into C_1 of the IMN.

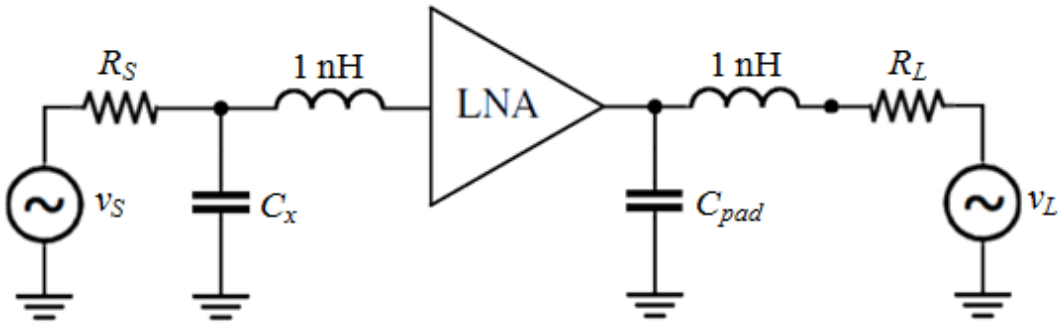

Figure 6.12. Schematic of the test bench circuit including package parasitics – the input pad capacitance has been absorbed in the IMN.

It was found that performance is severely degraded above 10 GHz by the bond wire inductance as shown in Figure 6.13 to Figure 6.15. The output pad capacitance has only a negligible influence on the high frequency gain. Through subsequent simulations it was found that increasing the shunt capacitance on either side of the bond wire inductance improves the performance somewhat and this is also shown. The final implemented value

of C_1 is 230 fF and an off-chip shunt capacitance (C_x) of 150 fF will be added close to the IC pin.

In an attempt to characterize the losses due to the package and test PCB a calibration path was included on the chip for which two bond pads were directly connected. The loss through this path could be subtracted from the measured LNA S_{21} and served to de-embed the LNA performance to an extent.

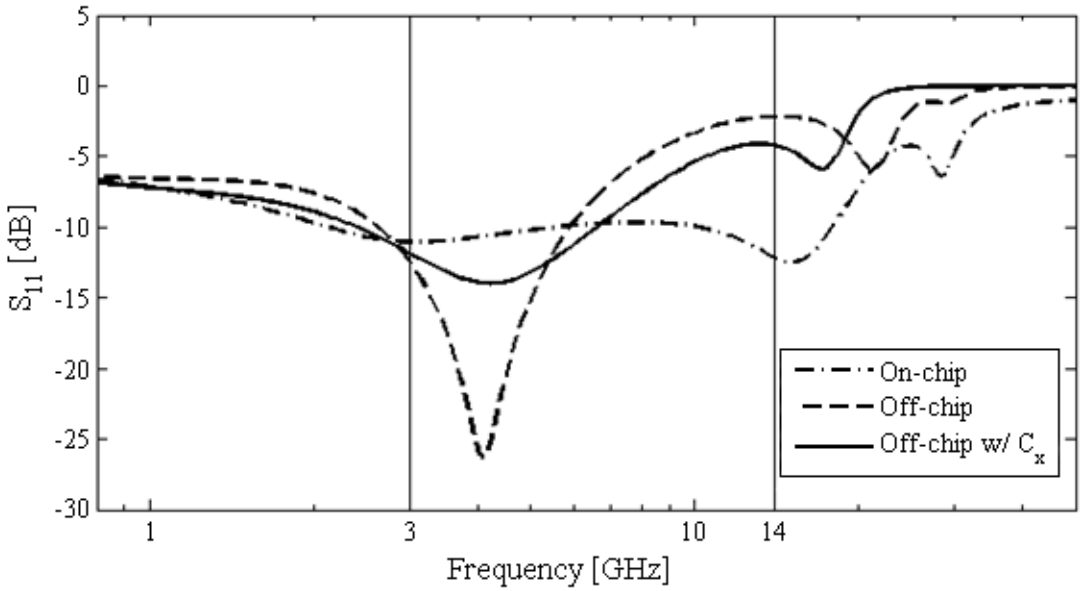

Figure 6.13. S_{11} of the LNA with package parasitics with and without the off-chip shunt capacitor.

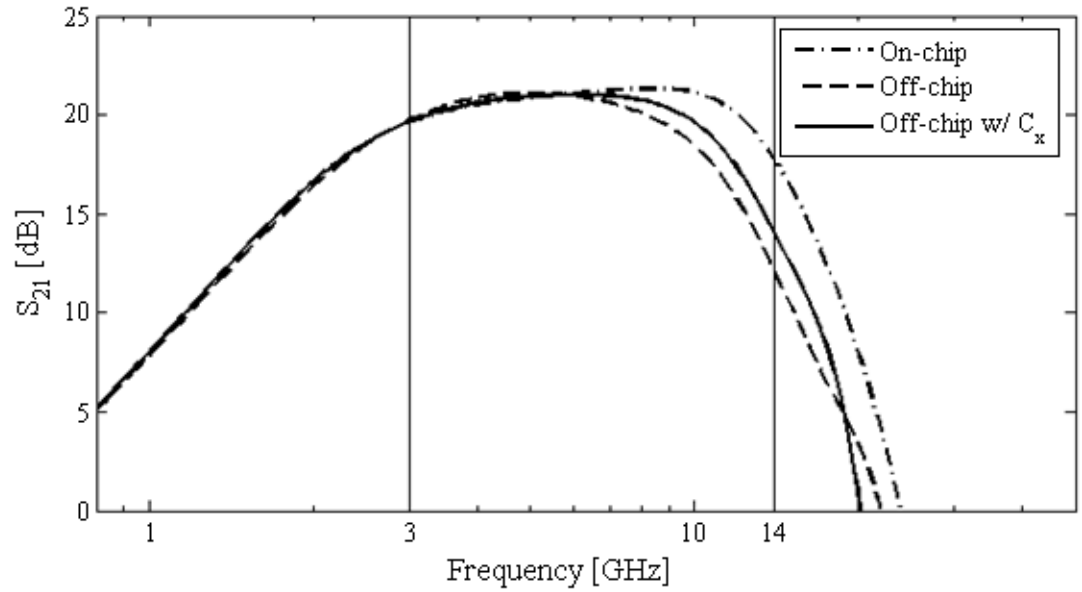

Figure 6.14. S_{21} of the LNA with package parasitics with and without the off-chip shunt capacitor.

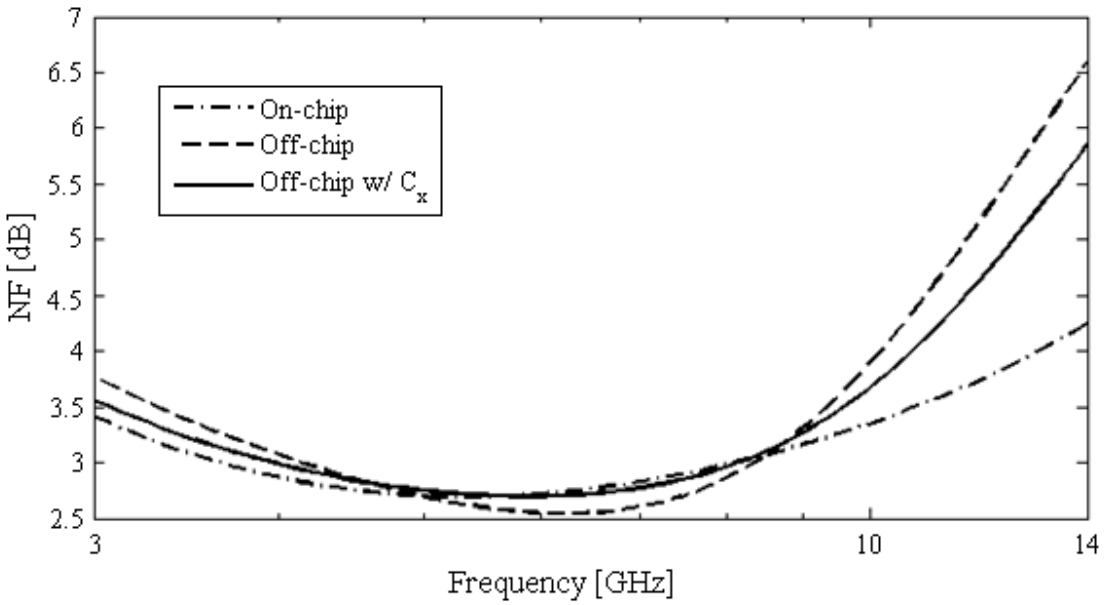

Figure 6.15. NF of the LNA with package parasitics with and without the off-chip shunt capacitor.

6.6 TEST PCB

As discussed in Section 6.4 on-wafer measurement equipment was not available and therefore the dies were packaged using QFN packages and soldered onto a PCB for testing purposes. This PCB consisted of biasing circuitry and also transmission lines from the IC to SMA connectors. Microstrip co-planar waveguides were used as signal interconnects.

The first amplifier stage requires current biasing and thus a resistor to the positive supply was used to set the collector current. The second and third stages use voltage biasing and were biased using the active voltage bias configuration seen in Figure 6.16. The potentiometers can be used to vary the collector current and set it to the desired value.

To facilitate setting the collector currents of the stages individually while using only two 1.8 V power supplies, one for the bias circuits and one for V_{CC}, jumpers were placed in series with the bias circuits. By removing two of the jumpers the biasing of any one of the three stage can be turned on individually and the total collector current flowing into V_{CC} measured with a multi-meter is the collector current of that particular stage.

The bias circuit in Figure 6.16 was duplicated and used for both LNAs, and subsections of it was used for the individual LNA stages as well. A photo of the final populated PCB is

presented in Figure 6.17, including the test circuitry for the two other projects on this chip. Rogers RO4003 material was used for the RF layers of the PCB.

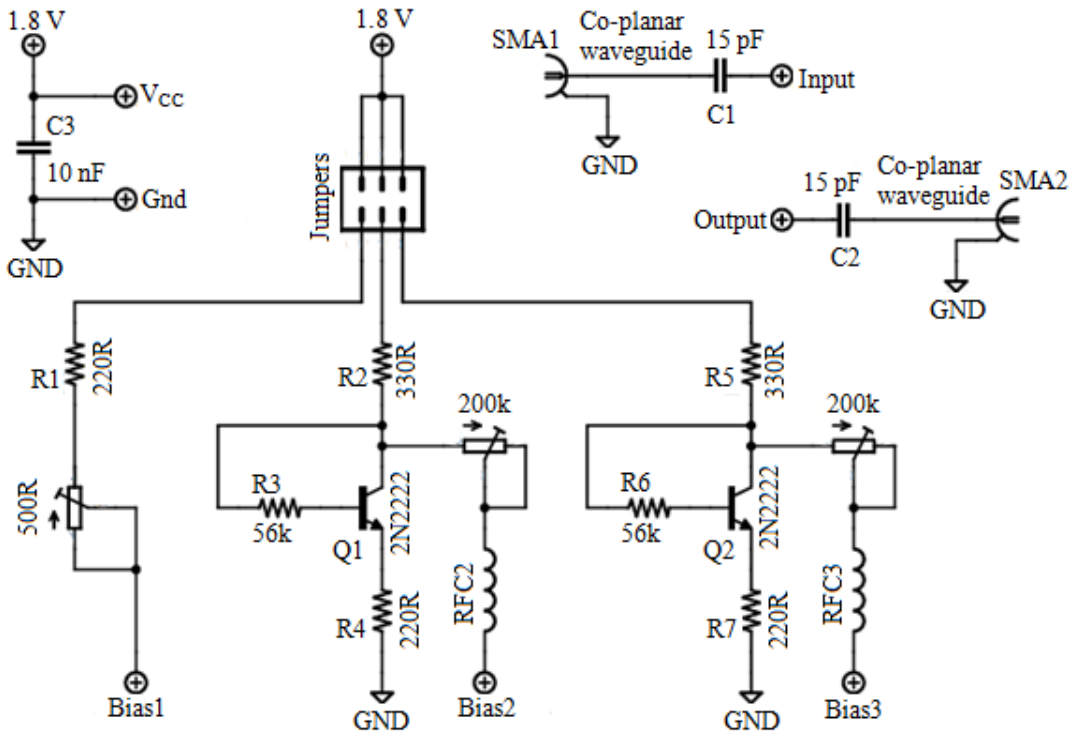

Figure 6.16. Schematic of the test PCB.

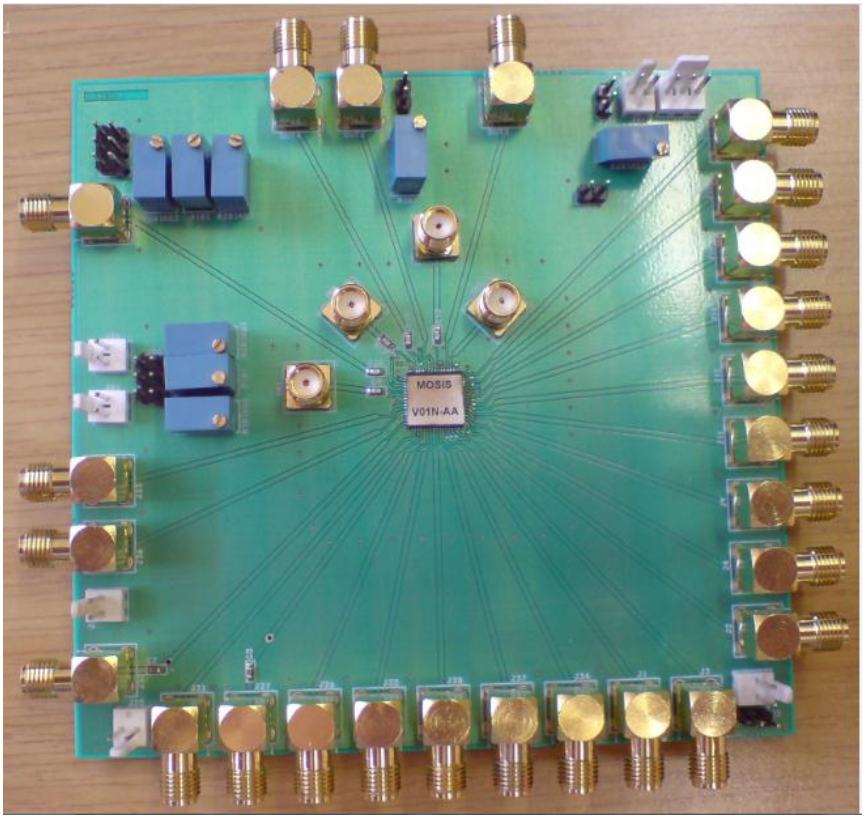

Figure 6.17. Photo of the test PCB.

6.7 SHORTCOMINGS OF THE TEST PCB

6.7.1 SMA connectors

Although many SMA connector datasheets specify a maximum frequency of at least 12 GHz for SMA connectors in general the right-angle connectors that were used on the PCB had a cut-off frequency of about 2 GHz. This is due to the through-hole pins of the connectors shown in Figure 6.18.

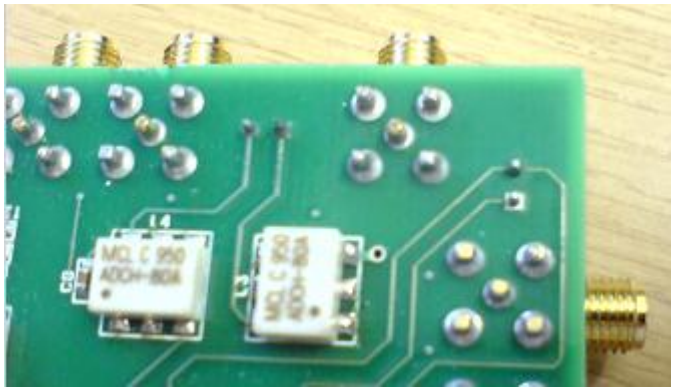

Figure 6.18. Through-hole pins of the PCB mounted SMA connectors

Since measurements up to at least 14 GHz were necessary the board had to be modified using coaxial cable and cable mounted SMA connectors with a cut-off frequency of about 18 GHz. The modifications are shown in Figure 6.19. Although this still resulted in significant signal loss measurement up to 6 GHz was feasible and allowed characterization of the LNAs up to this frequency.

Figure 6.19. Modifications to the PCB to allow measurement above 2 GHz.

For high speed circuits with operating frequencies above 2 GHz the SMA connector of choice should be the Emerson SMA connector with part number 142-0761-841 which mounts onto the side of the PCB in line with the waveguide offering a true 18 GHz cut-off frequency. This type of connector is shown in Figure 6.20.

Figure 6.20. Emerson 142-0761-841 side mounting SMA connector.

6.7.2 On chip DC blocking capacitors

When the LNA circuit design was done the input DC blocking capacitor was kept off-chip to avoid affecting the input matching network where the bond pad capacitance was absorbed into C_1. An on-chip DC blocking capacitor would need to be inserted in between this pad capacitance and the rest of the IMN.

In retrospect however the use of off-chip capacitors is far more detrimental to the circuit performance due to the package parasitics of these capacitors. Even with the use of C06CF150J range porcelain RF capacitors from Dielectric Laboratories, Inc. the performance was still degraded. Although these capacitors have an equivalent series resistance (ESR) of less than 1 Ω they still have a self resonant frequency of only 3.2 GHz [**70**].

6.7.3 Layout recommendations for future testing

Although co-planar waveguides were correctly used as transmission lines a technique called RF-stitching should be incorporated as well on future test boards. This technique dictates that vias be placed at short regular intervals next to the waveguide to the ground plane below. This shortens the path along the ground plane from one side of the waveguide to the other.

Another problem with the layout is the extremely thin tracks connecting the ends of the transmission lines to the IC pins which can be seen clearly in Figure 6.11. These thin tracks act as inductors at high frequencies and attenuate the signal from about 5 GHz upwards with severe attenuation above 10 GHz. Based on cost considerations a single board for testing the circuits of all three projects on the chip was used. Had a dedicated PCB rather been designed for testing only the LNAs the space might have been less constrained allowing the transmission lines to end closer to the chip, and thicker and shorter tracks with lower inductance to be used for connecting them to the chip.

6.8 CONCLUSION

This chapter presented the layouts of the LNA circuits submitted for fabrication as well as the photographs of the fabricated circuits. The packaging options were also discussed and the limitations of the QFN package and its effect on performance above 10 GHz have been indicated.

The small-signal simulation results of the circuit including the package parasitics are the expected results of the experimental measurements and will be used for comparison. In order to compare the performance of the fabricated devices to the simulations a method of de-embedding the on-chip LNA performance has to be used. A calibration path has been included on the chip to this end which was used to characterize the loss due to the PCB and IC package.

The design and schematic of the test PCB with bias circuitry was discussed. The shortcomings of this PCB in terms of the signal interconnects were pointed out along with the lessons learnt.

CHAPTER 7: EXPERIMENTAL RESULTS

7.1 INTRODUCTION

The fabricated chip and test PCB described in Chapter 6 were used to measure the performance of the LNAs. The measurement equipment and test procedures are described in this chapter. The experimental results are also given and compared to the expected results obtained from the simulations. The forward gain and input reflection as well as the noise figure of the LNAs were measured. The P_{1dB} compression point was also derived from the gain measurements.

7.2 MEASUREMENT EQUIPMENT AND TEST PROCEDURE

The *S*-parameters were measured using a Rohde & Schwarz ZVA40 Vector Network Analyzer capable of measuring 2 port networks up to 40 GHz. A photo of this analyzer is shown in Figure 7.1. A frequency range from 10 MHz to 20 GHz was used during the measurements.

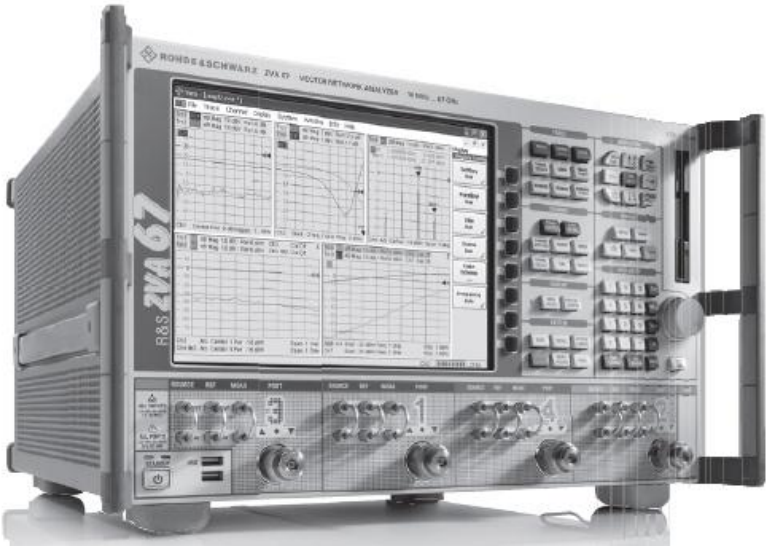

Figure 7.1. Photo of the Rohde & Schwarz ZVA40 Vector Network Analyzer [71**].**

To compensate for the losses in the PCB and the bond wire inductance of the IC package the S_{21} of a calibration path, made by connecting two bond pads together on the chip, was measured first. The loss in this path was subtracted from the S_{21} measurements of the LNA in order to de-embed the LNA itself from the PCB and package parasitics.

To obtain the P_{1dB} compression point the input power from the network analyzer was increased from -30 dBm by 1 dBm increments until a drop in the S_{21} was observed.

To measure noise figure an Agilent E4440A PSA spectrum analyser was used. It has a frequency range from 3 Hz to 26.5 GHz. A photo of the spectrum analyser is shown in Figure 7.2. A 20 dB excess noise ratio (ENR) Agilent 346B noise source was used to generate a noise floor above the minimum detectable noise level.

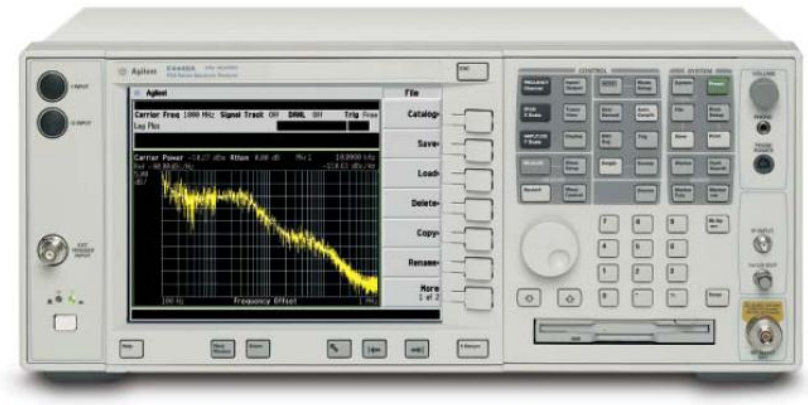

Figure 7.2. Photo of the Agilent E4440A PSA high performance spectrum analyser [72**].**

The frequency range for the measurements was set to 1 to 9 GHz which is the range over which reliable gain was obtained and the noise source ENR values were available. The *Y*-factor NF measurement and calculation method was used [**73**]. The noise source was first connected in series with the spectrum analyzer noise source control output and the RF input as shown in Figure 7.3. Taking measurements with the noise source turned on and off provided the reference noise power levels.

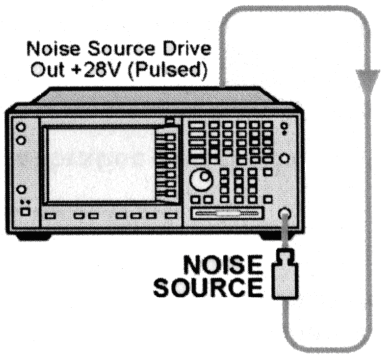

Figure 7.3. Calibration of the Agilent E4440A PSA with a noise source [74**].**

The LNA was then placed in series with the noise source as shown in Figure 7.4 and the noise power levels with the noise source turned on and off recorded. This provided all the data necessary for the *Y*-factor NF calculations [**73**] which were done in MATLAB. The noise figure was measured at room temperature and not at 290 °K as specified in the definition of noise figure [**1**].

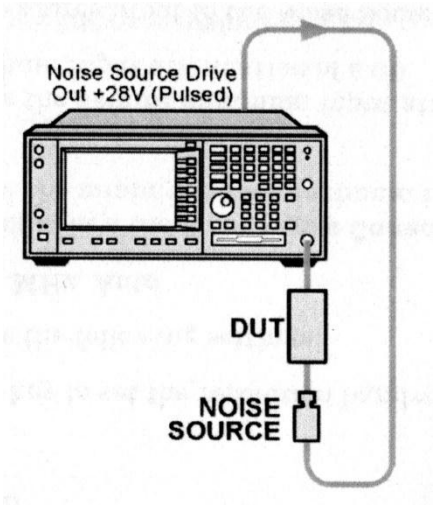

Figure 7.4. Connection of the device under test (DUT) to make NF and gain measurements [74**].**

Since only a single prototype was tested the results do not include all potential variations present in a large production run. The results are however sufficient to prove the concept and the capabilities of this LNA configuration.

7.3 MEASURED *S*-PARAMETERS

A plot of the calibration path S_{21} versus frequency is shown in Figure 7.5. Above 3 GHz there are significant spikes in the response due to the effects of the parasitic inductance in the last part of the PCB tracks as well as the bond wire inductance, and possibly also the parasitic capacitance of the IC package and PCB. Although the losses in the calibration path can be subtracted from the LNA S_{21} measurements to compensate, the harmonic spikes would not be at the exact same frequencies due to for example different track lengths. This means that some smoothing of the measured results could give a better indication of the response that would be measured on a naked die. A 5-point moving average smoothing function was used in MATLAB as discussed in the sections that follow.

The use of a smoothing function introduces the possibility of two major errors though. First, the smoothness of the curve could be too optimistic if overcompensated. Second, the function could result in a total average gain which is lower than the actual LNA gain which would have been obtained without the package parasitics. These factors should be kept in mind when interpreting the results.

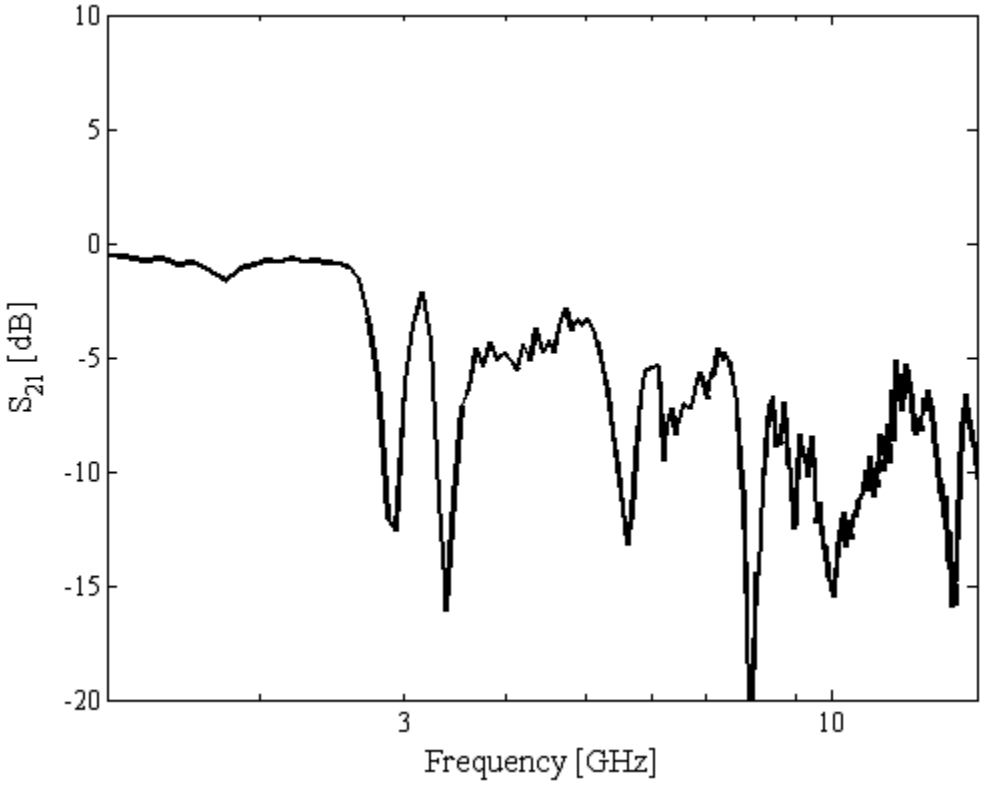

Figure 7.5. Calibration path S_{21} measurement

After de-embedding and smoothing of the measured results the shape of the *S*-parameter curves of both the standard and linearity optimized LNAs were similar to the simulated curves. Interestingly the linearity optimized version were a much closer match than the standard version though, as shown in the following plots. Since the designed collector currents of the standard LNA were low values the currents were adjusted to improve the gain of the LNA, although this had a detrimental effect on the S_{11}. The alternative current values are given in Table 7.1 and the effects on the *S*-parameters are shown in Figure 7.6 to Figure 7.8.

Table 7.1Table 7.1. Modified collector current values of the standard LNA to improve the gain.

Current	Original value	Adjusted value
I_{C2}	2.7 mA	3.6 mA
I_{C3}	2.7 mA	4.7 mA

7.3.1 Standard LNA

Figure 7.6 shows the measured S_{21} of the standard LC-ladder and capacitive shunt-shunt feedback LNA before and after the calibration path was subtracted for both the original and adjusted collector currents.

The comparison of the de-embedded plots after application of a moving average smoothing function is shown in Figure 7.7. The difference in the S_{11} can be seen in Figure 7.8. A comparison of smoothed S_{11} curves shows an average worsening 2 dB above 4 GHz. From the plots in Figure 7.7 the gain has been improved by about 5 dB over the entire band of interest up to 10 GHz where the parasitics cause a rapid cut-off of the gain.

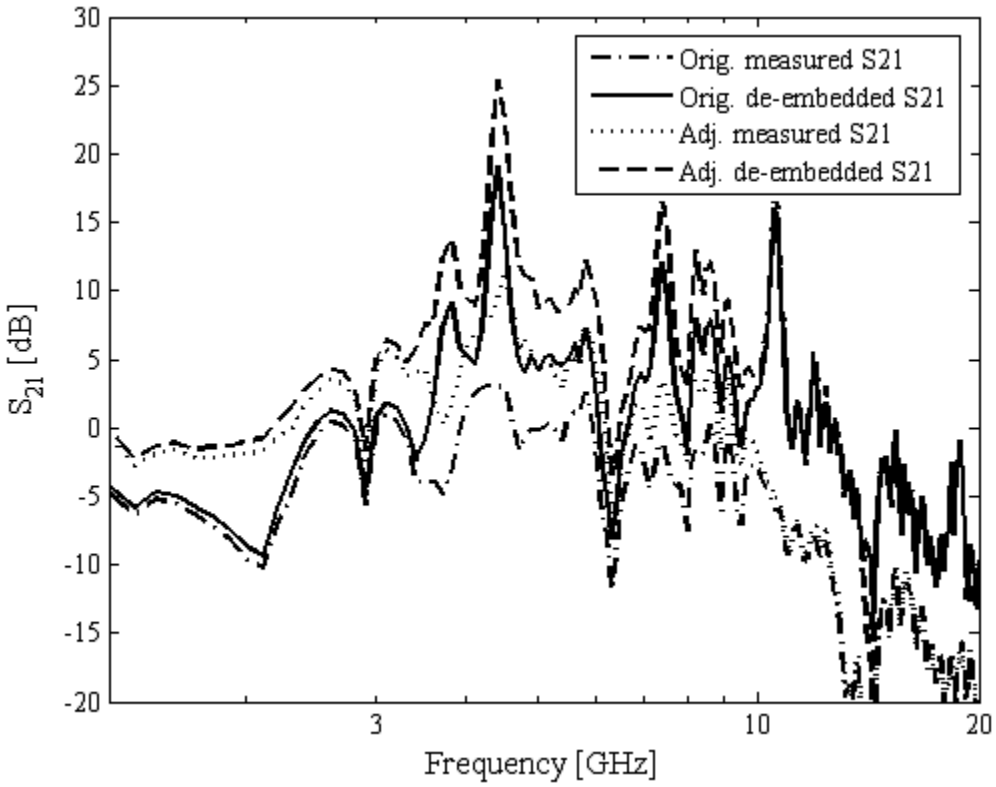

Figure 7.6. Measured S_{21} of the standard LNA before and after subtraction of the calibration path for the original and adjusted collector currents.

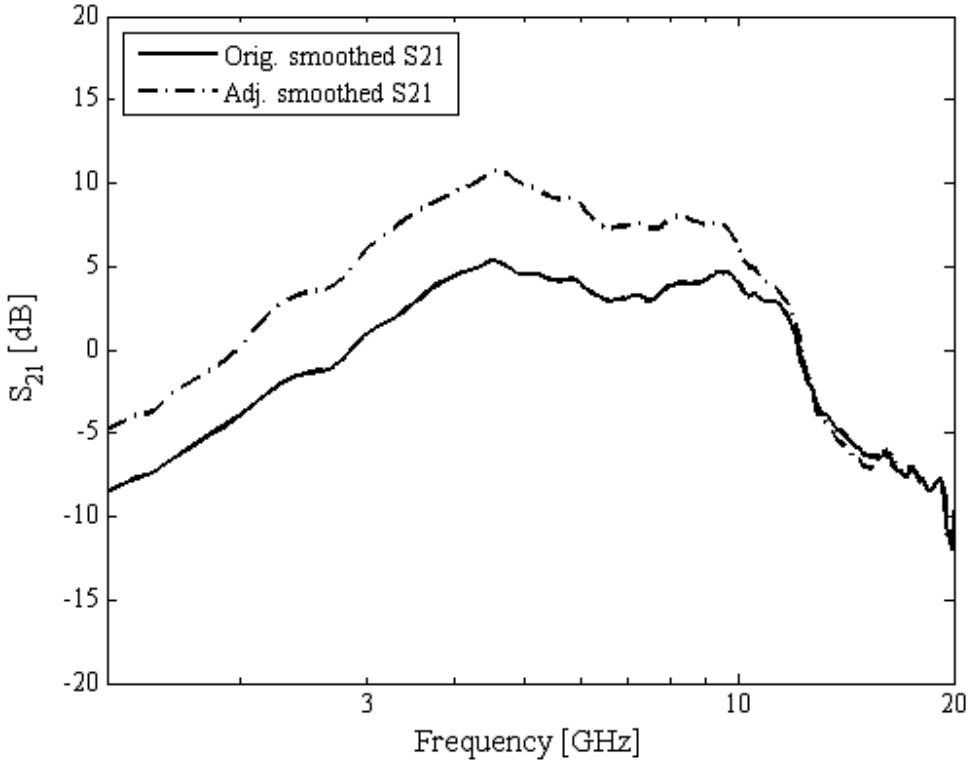

Figure 7.7. Comparison of the de-embedded and smoothed S_{21} of the standard LNA with the original and adjusted collector currents.

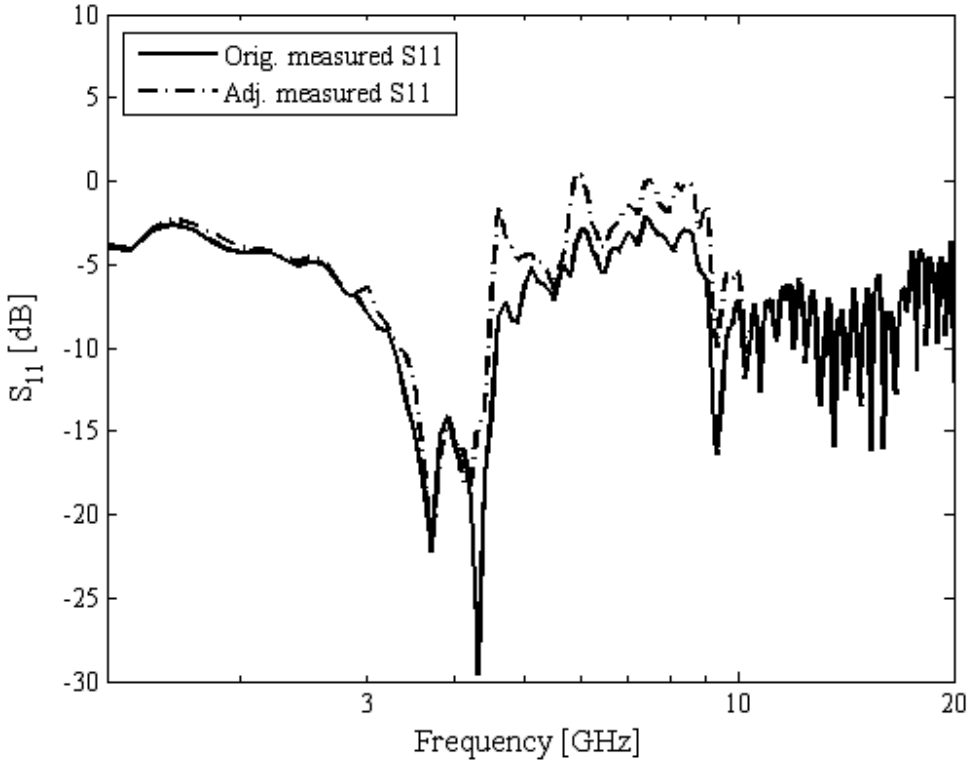

Figure 7.8. Measured S_{11} of the standard LNA with original and adjusted collector current.

In Figure 7.9 the smoothed S_{11} and S_{21} of the standard version of the LNA are compared to the simulated responses given in Section 6.5. The measured mid-band gain is 8 dB which is 12 dB lower than the expected simulated gain; the lower -3 dB cut-off frequency is at 3 GHz as expected though. The S_{11} is worse than expected by 2 dB below 4 GHz, and up to 5 dB above.

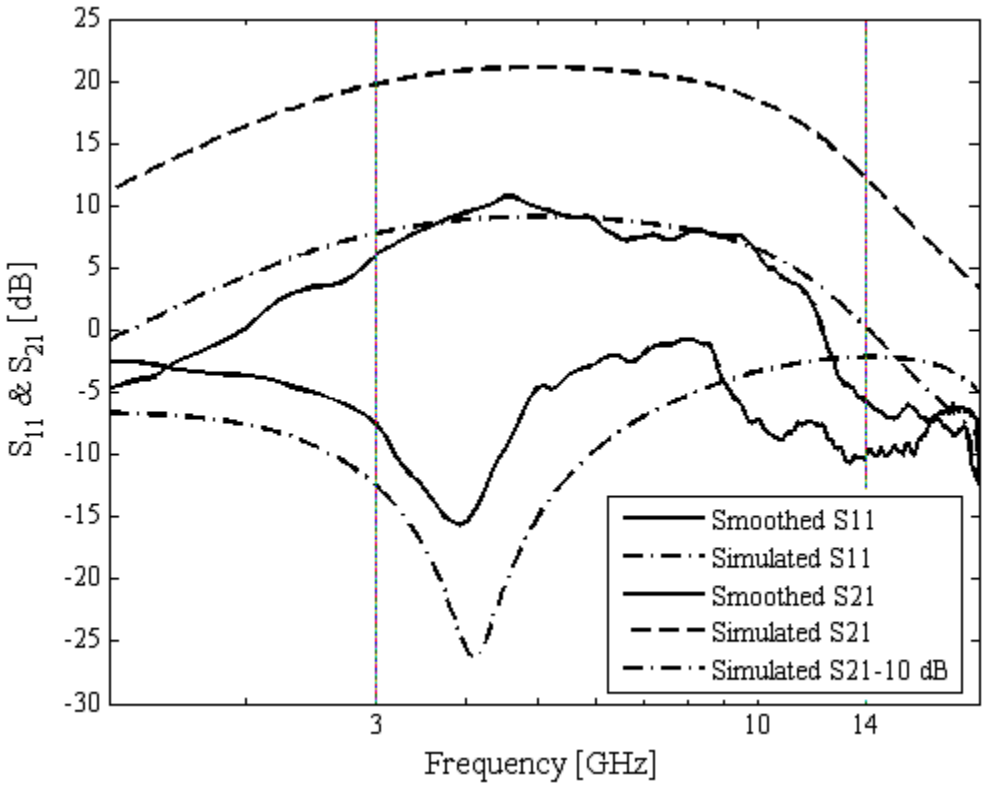

Figure 7.9. Smoothed S_{11} and S_{21} of the standard LNA with adjusted currents compared to the simulated result from Section 6.5.

7.3.2 LNA optimized for linearity

The measured and de-embedded S_{21} of the LNA optimized for linearity is shown in Figure 7.10, and the smoothed de-embedded version in Figure 7.11. The measured and smoothed S_{11} of this LNA is given in Figure 7.12.

The comparison of the smoothed results to the simulated results from section 6.5 is shown in Figure 7.13. In contrast to the response of the standard version of the LNA the measured S_{11} of the linearity optimized LNA tracks the simulated response very well. It dips below -10 dB just above 3 GHz, and then goes above -10 dB again at 6 GHz. This is the expected response due to the package parasitics though as predicted by the simulations.

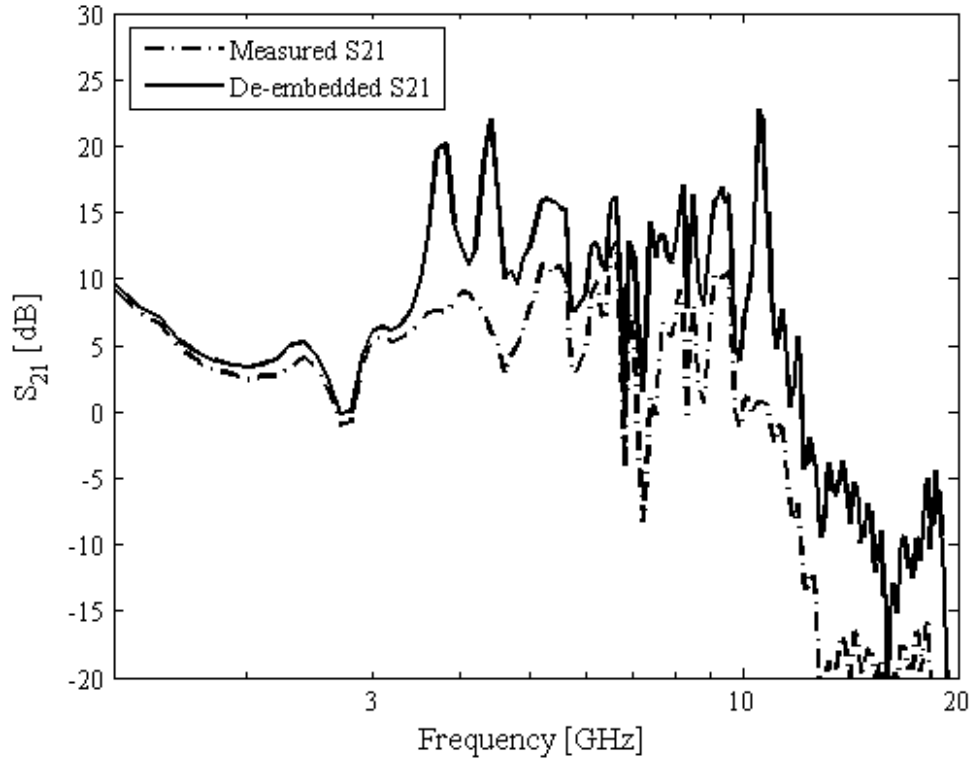

Figure 7.10. Measured S_{21} of the LNA optimized for linearity before and after subtraction of the calibration path.

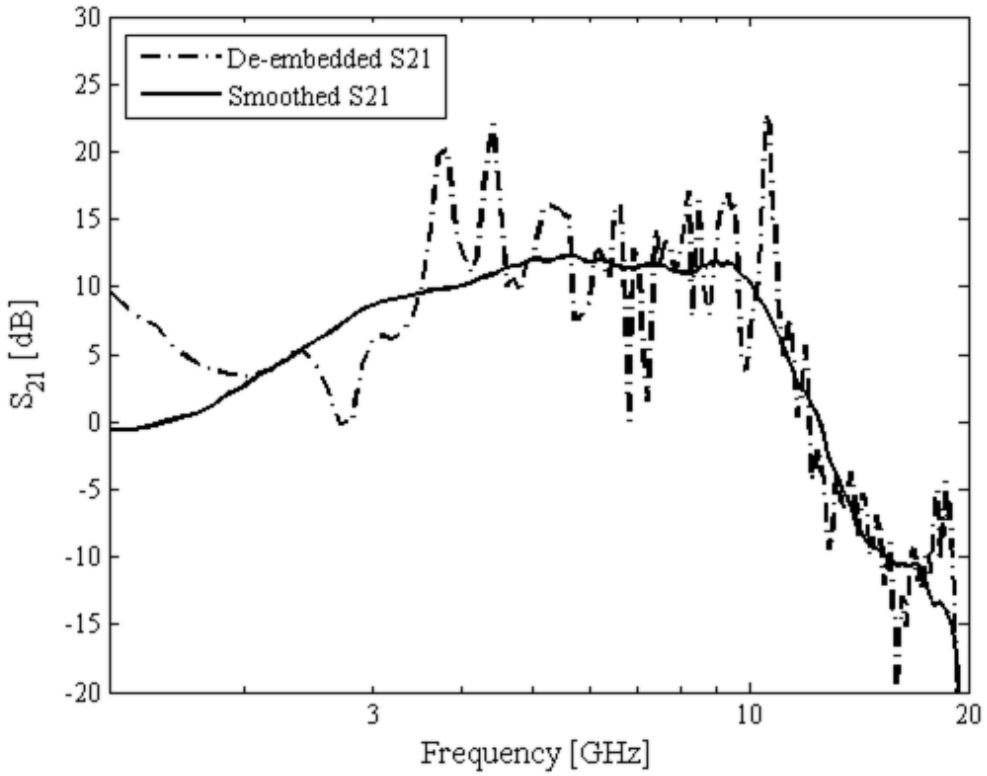

Figure 7.11. De-embedded S_{21} of the LNA optimized for linearity before and after smoothing with a moving average algorithm.

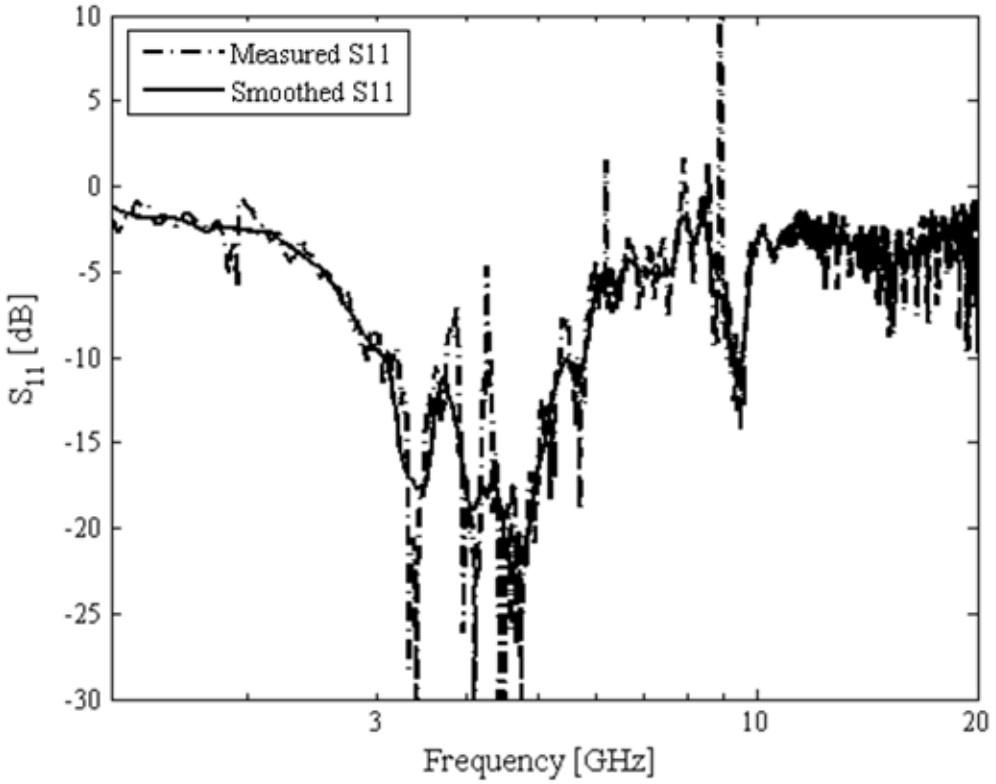

Figure 7.12. Measured S_{11} of the LNA optimized for linearity before and after smoothing with a moving average algorithm.

Although the measured gain of 10 dB is 10 dB lower than expected the shape of the plot closely matches that of the simulated S_{21} and shows the lower cut-off frequency at 3 GHz as designed. Above 10 GHz the measured cut-off is still much sharper than simulated though, possibly due to the inductance of the narrow tracks connecting the transmission lines to the IC pins which becomes dominant above this frequency. This effect was not included in the simulation. The only deviation from the expected results is therefore the gain which is 10 dB lower than the designed value, but this could to an extent be due to the smoothing of the curve, and also result from the degradation of the input and output return losses by the package and PCB parasitics.

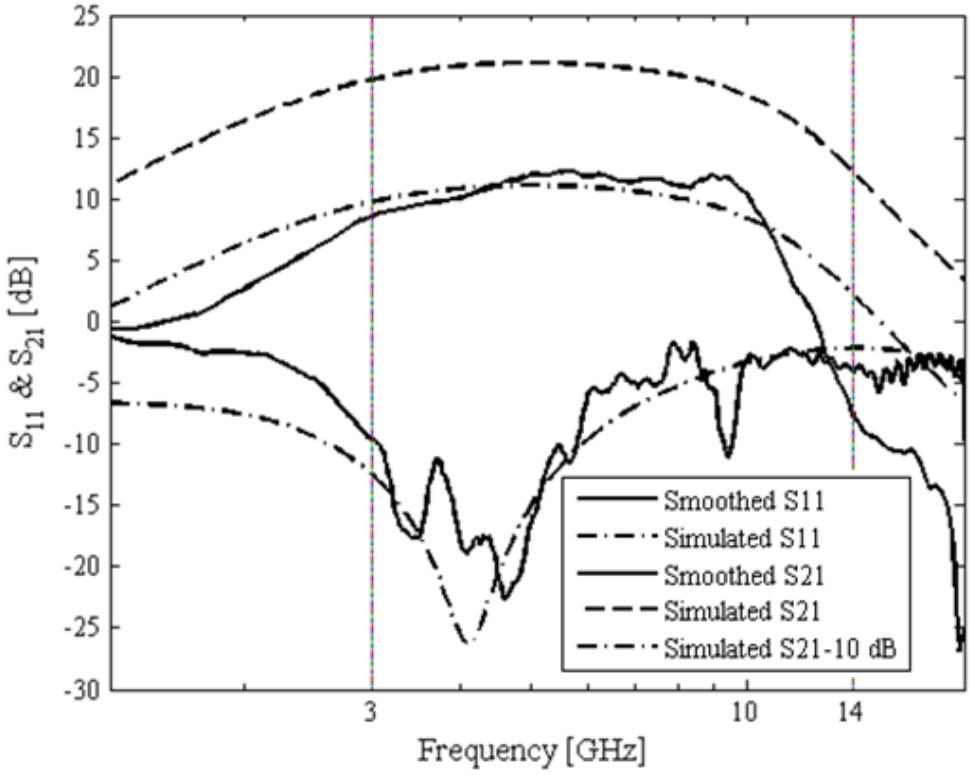

Figure 7.13. Smoothed S_{11} and S_{21} of the LNA optimized for linearity compared to the simulated result from Section 6.5.

7.4 MEASURED NOISE FIGURE

The measured noise figures of the LNAs are very high. Unfortunately the noise measurements are dependent on the system gain which can of course not be physically de-embedded when doing noise measurements. Therefore the already relatively low gain of the two systems at 10 dB is in fact even less when performing these measurements due to the path loss resulting from the PCB and package parasitics. Such a low gain introduces a large margin of error which means the actual NFs are potentially much lower than the measured values.

In addition the 20 dB ENR noise source only barely resulted in a reference noise level above the noise floor of the spectrum analyzer. This introduced further uncertainty into the measurements. Ideally a pre-amplifier should have been used to raise the reference level higher, however a pre-amp which operates over this frequency range was not available.

The measured noise figures are shown in Figure 7.14. The NF of both LNAs has an average of 20 dB.

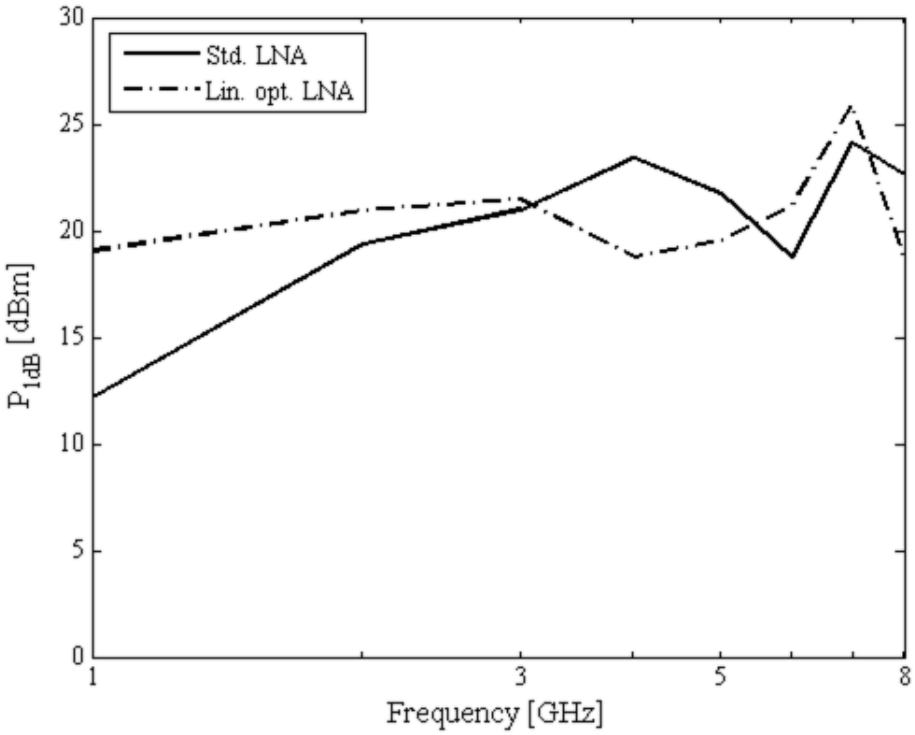

Figure 7.14. Measured noise figure of the two LNAs.

7.5 MEASURED P_{1DB} COMPRESSION

To find the P_{1dB} compression point the S_{21} at various input powers were plotted on the graphs shown in Figure 7.15 and Figure 7.16. These plots were visually inspected to find the 1 dB compression at various frequencies. Since the 1 dB compression of the S_{21} response before smoothing varied by large amounts depending on whether the gain at a specific frequency was at the peak of a spike in the response or a valley the smoothed versions of the S_{21} measurements were used to obtain a rough approximation of the actual P_{1dB} compression curve.

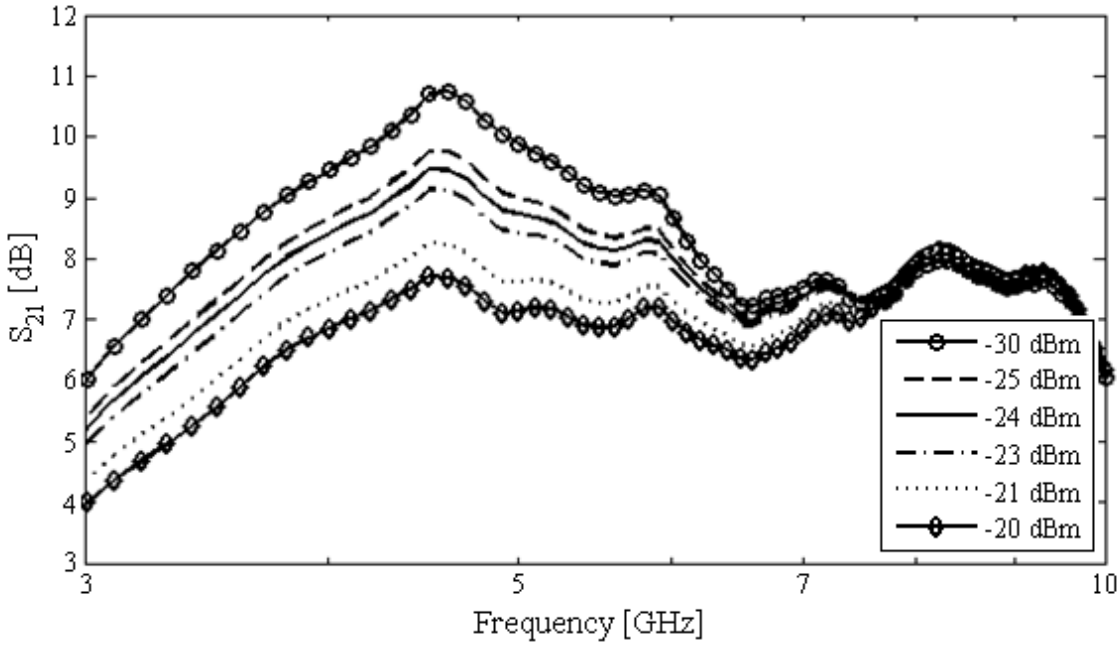

Figure 7.15. Smoothed measured S_{21} of the standard LNA at various input powers.

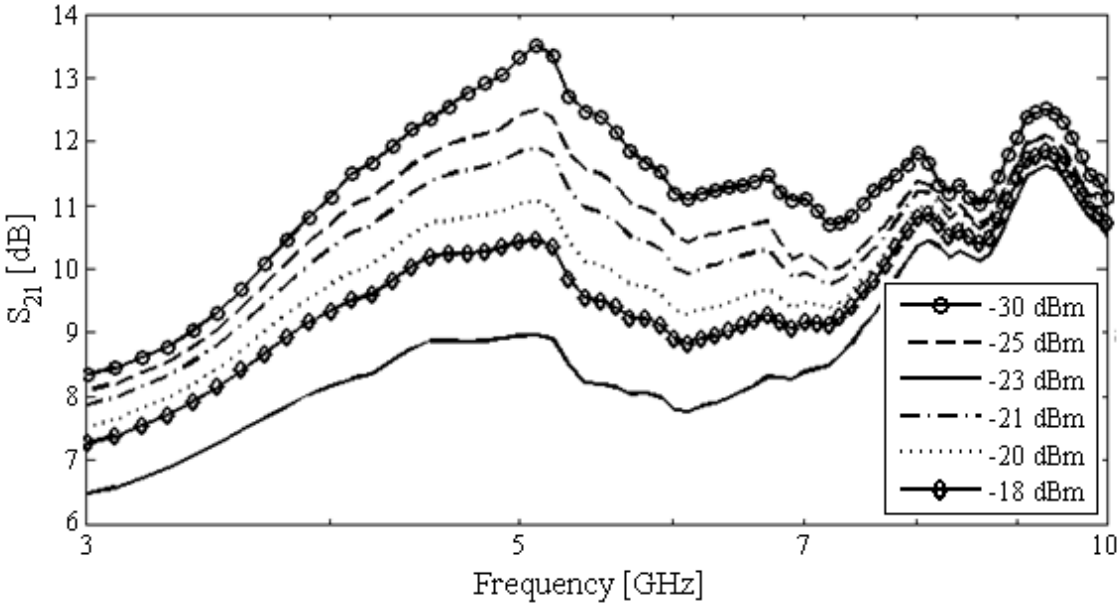

Figure 7.16. Smoothed measured S_{21} of the LNA optimized for linearity at various input powers.

The compression was determined over the 3 GHz to 8 GHz band over which the gains of both LNAs are relatively flat. The P_{1dB} compression curves over this band are plotted in Figure 7.17. Both the standard version and the one optimized for linearity's compression points vary between -20 dBm and -24 dBm with an average of -23 dBm for the standard and -22 dBm for the more linear version.

The more linear LNA clearly has an improved P_{1dB} compression point at the lower frequencies from 3 GHz to 5 GHz. From 5 GHz onwards the performance of the two LNAs becomes very similar; however if taken into account that the linear LNA has a gain of 10 dB compared to a gain of 8 dB for the standard LNA the former is effectively more linear over the entire band with improved P_{1dB}.

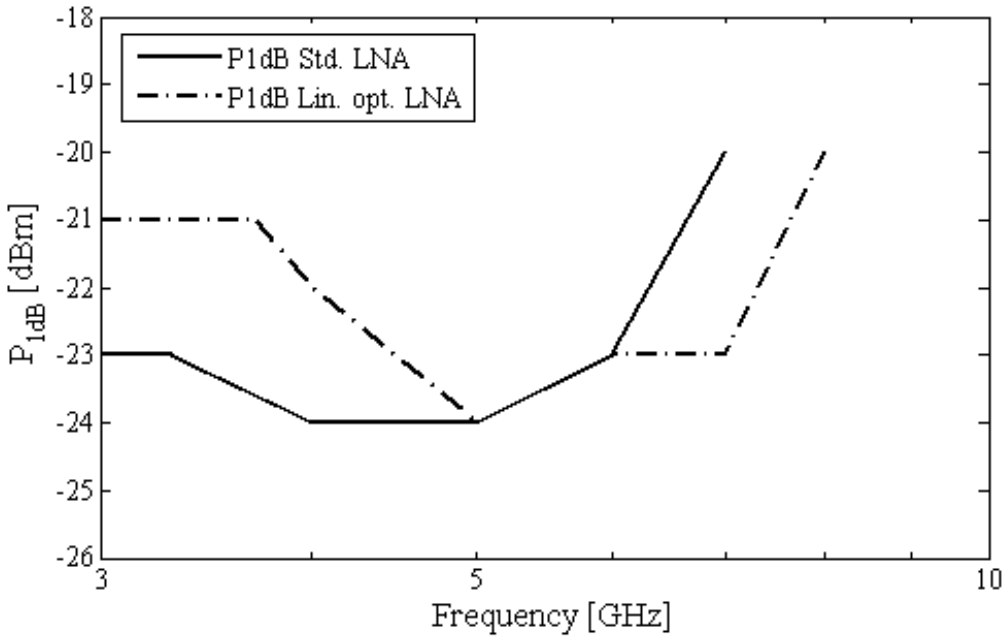

Figure 7.17. P_{1dB} compression curve of the standard and linearity optimized LNAs.

7.6 CONCLUSION

This chapter discussed the measuring equipment and the test procedure used during characterization of the fabricated LNAs. The measured results of both the standard and linearity optimized versions of the LC-ladder and capacitive shunt-shunt feedback LNA were presented.

The measured *S*-parameters compared very well with the simulations where the package parasitic components were included. The measured S_{21} of the standard version of the LNA is 8 dB with an S_{11} 2 dB higher than expected, but still below -10 dB over a reasonable section of the frequency band. The average S_{21} of the linearity optimized version of the LNA was 10 dB, and the S_{11} remained below -10 dB over the entire feasible range predicted by the simulations and showed very good tracking of these simulated results.

The P_{1dB} compression point was between -20 dBm and -24 dBm for both LNAs over the 3 GHz to 8 GHz range. The average compression point of the linear LNA showed a 1 dBm improvement over the standard one at -22 dBm compared to -23 dBm. If the higher gain of the LNA optimized for linearity is also taken into account it is clearly the more linear of the two.

The NF is the only parameter that was not measured with high enough accuracy to provide reliable results due to the low gain of the LNAs and unavailability of a pre-amp to provide an adequately high noise power above the spectrum analyzer noise floor. The average measured NF of both LNAs was 20 dB, but with the above PCB related shortcomings taken into account the actual device NF could be much lower.

Although it was suspected that the emitter degeneration resistors in the linearity optimized version of the LNA would be detrimental to the gain and S_{11} of the LNA it turned out to be the LNA exhibiting improved gain performance. This means that with the added benefit of better linearity this should be the version of choice based on current findings.

Although a complete characterization of the LNA performance was not possible these measured results prove the feasibility of the LC-ladder and capacitive shunt-shunt feedback configuration for the implementation of wideband LNAs and validates it as an area for further research.

CHAPTER 8: CONCLUSION

This research dealt with the question of whether a combined LC-ladder and capacitive shunt-shunt feedback matching network could be used successfully in wideband LNA implementations, especially with improved performance compared to current LNA implementations in literature.

Through the derivation of a mathematical model and subsequent design and simulation of such a LNA in the IBM 8HP 0.13 µm SiGe BiCMOS process as well as fabrication in the IBM 7WL 0.18 µm process, it was proved that this is indeed an effective means of implementing very wideband LNAs with low NF and power consumption while achieving typical gain and input matching specifications. These results are compared to state-of-the-art LNA performance available in literature in Table 1.1.

A critical evaluation of this research is presented in this chapter along with suggestions for future research on this topic.

8.1 CRITICAL EVALUATION OF THE WORK

In Section 1.2 it was hypothesized that if a fourth order LC-ladder filter can be used to realize input matching over an arbitrary frequency band, and a shunt-shunt capacitive feedback common emitter configuration can be modelled as an equivalent series RC circuit, then a combination of these two circuits can be used as a wideband LNA overcoming certain shortcomings of current LNAs in literature; most notably the pole introduced at the lower corner frequency resulting in the four on-chip inductor requirement of the emitter degenerated LC-ladder configuration, and also the tight coupling between the collector current and the lower corner frequency values.

This hypothesis has been corroborated and the research questions answered through the successful modelling, design, simulation, fabrication and measurement of a LC-ladder and capacitive shunt-shunt feedback LNA.

- The derived mathematical model shows that not only can wideband matching be realized, but also very low noise operation with typical gain performance.

- As shown in Section 4.2.4 the pole at the lower corner frequency found in the emitter degenerated LC-ladder configuration [**11**] is not present in this topology.
- This configuration does not require an emitter inductor in the first stage due to the capacitive feedback which means only three rather than four on-chip inductors are required. In addition, if the design is done over a smaller frequency range where the first stage gain does not have to be increased beyond the limit set by the GBP, and an increase of the first stage load capacitance would also not be required, the output pole of the first stage will be beyond the operating frequency band and the second stage load inductance could also be exchanged for a resistive load, thereby decreasing the inductor count to two.
- Since the matching is realized using the Miller-capacitance rather than transistor parasitic capacitances there is significant freedom in the selection of collector current which can be used to tune the circuit for optimal performance.
- It is also a wideband configuration and not a narrowband amplifier applied to wideband applications as done with the inductive emitter degeneration or capacitive feedback techniques in other works [**12**].

The configuration presented here shows improved simulated NF compared to the results found in literature. The power consumption has also been greatly reduced while maintaining the standard LNA *S*-parameters of S_{11} < -10 dB and S_{21} = 20 dB. Preliminary measured results, although not fully attaining the simulated performance, confirmed the potential of this configuration to achieve good wideband performance when considering the shortcomings of the measurement process. These improvements were made at the cost of linearity, mainly due to the removal of degeneration from the first amplifier stage; however linearity can be improved by trading power consumption while the NF and gain can be kept relatively constant where higher linearity is required as shown in Sections 5.3.5 and 5.5.5.

This research also produced a thorough analysis of existing LNA configurations and input matching techniques, and especially the inductively degenerated common-emitter topology was discussed in great detail as it is one of the most common LNA implementations found in literature. A discussion of the trade-offs between NF, gain and linearity of the techniques was also given.

The largest contribution of this work towards the future implementation of the proposed LNA topology is the derived mathematical model characterizing the configuration. This can be used to both predict the performance the LNA and also includes design equations to facilitate EDA. Preliminary MATLAB code towards the implementation of such EDA software is provided in Appendix A. A process of simultaneously minimizing the NF and improving the gain of the LNA was also deduced from this model and presented; as was the bandwidth versus NF trade-off.

The accuracy of the mathematical model was proved with thorough simulations of two LNA designs using different transistor processes. The sensitivity of the LNA performance with variations in process parameters and temperature was also shown. Although simulated and calculated results showed good correlation, some assumptions were made in the derivation of the model and these are listed below, with some suggestions for future improvement of the model also provided in Section 8.2.

- The simple high frequency small-signal model of the bipolar transistor was used in the derivation. This however proved to be sufficient for first order designs done using this model.
- Inductors were modelled as an inductance and parasitic series resistance which was derived from a Q-factor estimated from data found in the process model guides [**56**], [**58**] and assumed to be constant with frequency. Although the simple inductor model proved sufficient the Q-factor has a large influence on both the NF and input matching and as such should be derived from the inductor layout parameters in a frequency dependent form.
- The gain bandwidth product is currently not taken into account by the model and proves problematic when transistors are operated close to their performance limits as shown in Section 5.5.1.
- The correlation between the base- and collector current shot noise is not included in the NF equation; however this only becomes noticeable at very high frequencies where, as shown in Section 5.4, the use of this configuration is not optimal and as such this is an acceptable simplification.
- Only an approximation of the worst case IIP3 has been included in the model.

Since the absence of emitter degeneration in the first amplifier stage leads to poorer linearity of the amplifier a thorough investigation of the non-linear sources in HBTs was performed and suggestions made for the improvement of linearity. The improved IIP3 performance with the use of emitter degeneration in the second and third amplifier stages was also presented.

Finally, the layout of two LNAs implementing the LC-ladder and capacitive shunt-shunt feedback topology, with and without linearity improvement, was shown and have been submitted for fabrication in the IBM 7WL 0.18 µm SiGe BiCMOS process. These devices were measured to obtain experimental results which showed good promise, however the measurement equipment was not optimal for measuring performance at such high frequencies. Most notably the PCB layout and choice of SMA connector type was not appropriate for operation above 2 GHz, and the fact that a pre-amplifier was not available for noise measurements resulted in large uncertainty.

8.2 SUGGESTIONS FOR FUTURE WORK

Suggestions for the improvement and expansion of the mathematical model derived in this work for future research are given in the list below.

- Although *S*-parameters and NF equations were derived from the small-signal circuit of the amplifier using first principles only a rough approximation of the IIP3 was used. The model could be expanded to include a more accurate representation of the linearity using a Volterra series. This would also make it possible to isolate the various sources of non-linearity in the LNA [**35**] to analytically determine the dominant sources so subsequent optimization processes can focus on those non-linear sources (similar to the noise optimization done in this work).
- The effect of the GBP due to the finite f_T of the transistors should be added to the gain equations. It should be possible to maintain a relatively simple model if the f_T is calculated as a function of g_m and the parasitic components.
- Although it was pointed out that neglecting the base- and collector current noise correlation at the frequencies where this configuration is effective, including that could be useful in making the model more robust.
- Following the same RF analogue approach used in this research to derive similar equations for the performance measures of other LNA topologies would allow a

direct comparison of the performance of different topologies based on the specifications for a given application. This could then be used to choose the optimal configuration. Two configurations suggested for such a comparison would be the inductive emitter degeneration [**9**] and emitter degenerated LC-ladder topologies [**11**].

- The sensitivity of the simulated performance of this LNA to variations in transistor model parameters, as well as performance sensitivity to temperature and process variations can also be investigated as a possible figure of merit when comparing it to other LNA configurations in the selection of a LNA for a specific system. Furthermore such data could indicate which parameters of a given transistor model are most essential to extract with high accuracy. These variations as well as the results obtained for the reference case when simulated with the HICUM, VBIC and Mextram transistor models could then be compared.
- As mentioned in Section 8.1 the use of accurate inductor Q-factor values is imperative for achieving calculated results that correlate with the actual circuit performance. Inductor modelling software that could be used to determine the frequency dependent Q-factor based on inductor layout parameters is available in literature [**49**] and should be included in the model and any EDA implementation.
- The inductor modelling software referenced in the previous point forms part of EDA software for class-E and class-F power amplifiers. If such software could be combined with the LNA design automation presented in this work a complete RF amplifier EDA software package could be obtained.
- As pointed out in Section 2.8, passive inductors can be traded with active inductors to reduce the physical size of the circuit. In this case a reduction of approximately 18.4 % can be obtained by replacing the second stage load inductor. Thus the investigation into practical active inductor circuits presented in the literature study could be extended and the feasibility of a LNA employing such an active load investigated.

Improved characterization of the fabricated LNAs should be done with a redesigned test PCB adhering to the suggestions made in Section 6.7. In a future production run LNAs with on-chip input and output DC-blocking capacitors should also be fabricated and tested. Performing on-chip measurements would provide the most accurate characterization of a LNA.

Other bias options should also be investigated such as using the same voltage biasing technique used in stages two and three for the first stage of the LNA. The inductor L_1 could still be used as an on-chip RF choke in such a case. Ideally four different power supplies should also be used, one for the biasing circuit, and a separate supply for the V_{CC} of each stage. This will allow verification of each collector current during the operation of the LNA. With the current PCB design the collector currents could be set individually, but there was no way of measuring the extent to which the stages operating simultaneously affected the current of individual stages. It is believed that this did take place since the overall collector current during operation did not always match the sum of the individual collector currents that were set.

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ADDENDUM A: PRELIMINARY MATLAB CODE FOR EDA

The preliminary code towards the implementation of EDA software written in MATLAB and used throughout this research to design the LNAs is given below.

```
clear all;

%----- SPECIFICATIONS ------------%
%The specified frequency range, gain and max NF for the design are set here
fl = 1e9;   wl = 2*pi*fl;
fu = 18e9;  wu = 2*pi*fu;
S21_spec = 20;  %dB
NFmax = 4;  %dB
RS = 50;


%----- PLOT SETTINGS -------------%
%Settings related to the display of the result plots
flcalc = fl/10;      % The range overwhich values are
fucalc = fu*10;      %   calculated beyond the operting frequency band
pts = 500;           % Number of points in the plot
linewidth = 2;       % Linewidth used in plots
calc_colour = 'k-.'; % Colour and line style used for calculated and
sim_colour = 'k-';   %   simulated result plots
%---------------------------------%

%----- PLOT FLAGS ----------------%
% Flags for choosing when to plot input impedance, individual noise
% contributions, IIP3 or simulated results read from a csv file
plotZIN = 0;
plotNSources = 0;
plotIIP3 = 0;
plot_sim = 0;


%----- SIMULATED RESULTS READIN -------------%
if( plot_sim == 1 )
    cnt = 451;
    load sim_1GHz_to_18GHz_gain_cur_pas/S11_s.csv;
    load sim_1GHz_to_18GHz_gain_cur_pas/S21_s.csv;
    load sim_1GHz_to_18GHz_gain_cur_pas/NF_s.csv;
    f_sim = 1:cnt;
    S11_sim = 1:cnt;
    S21_sim = 1:cnt;
    NF_sim = 1:cnt;
    for u = 1:cnt
        f_sim(u) = S11_s( u, 1 );
        S11_sim(u) = S11_s( u, 2 );
        S21_sim(u) = S21_s( u, 2 );
        NF_sim(u) = NF_s( u, 2 );
    end;
end;


%*************************************************************************
%Environment setup
%*************************************************************************
%Create logarithmic frequency values based on the range and no. of points
ll = log10( flcalc );
lh = log10( fucalc );
l_inc = (lh-ll)/pts;
lf = ll:l_inc:lh;
f = 10.^lf;
w = 2*pi.*f;
```

```
%Physical constants definition
k = 1.38e-23;       %   Boltzmann's constant
q = 1.602e-19;      %   Electron charge
T = 290;            %   Temperature in Kelvin
VT = k*T/q;         %   Thermal voltage

%Load transistor parasitic values and process parameters
%---- TRANSISTOR1 PARAMETERS -----%
Rb1  = 13.7 + 5.8;
Re1  = 1.53;
Cmu1 = 1.38e-15 + 9.52e-15 + 9.11e-15;
Cpi1 = 18.1e-15 + 18.6e-15;

%---- TRANSISTOR2 PARAMETERS -----%
Rb2  = 13.7 + 5.8;
Re2  = 1.53;
Cmu2 = 1.38e-15 + 9.52e-15 + 9.11e-15;
Cpi2 = 18.1e-15 + 18.6e-15;

%------ PROCESS PARAMETERS -------%
Beta0 = 300;
Vcc = 1.5;
Vce = 0.2;
VA = 16.36;
Q1 = 1.5;
Q2 = 3;
Q3 = 5;
%---------------------------------%


%*************************************************************************
%These values are changed during the design phase
%These and selected calculated values are printed in the output to aid
%in the optimization process.
%*************************************************************************
%------- DESIGN PARAMETERS -------%
Av1_set = 27;  %Used to modify the first stage gain - initial value should
               %be the maximum allowed by the GBP

NF_impr = 2;   %Expected NF improvement through optimization process
               %Allows for less stringent yet appropriate Av1_req values

%Equations to calculate the initial IMN reactive elements
C1 = 1/RS/wu;
C2 = 1/RS/wl;
L1 = RS/wl;
L2 = RS/wu;
%During optimization the above equations are commented and the values
%  modified below
%C1 = 40e-15;
%C2 = 3.18e-12;
%L1 = 9.91e-9;
%L2 = 363e-12;

%Additional first stage load capacitance added during optimization
CL1_add = 0e-15;   %Initial value = 0

%Amount by which the first stage collector current is increased above the
%  calculated value; RL1 is modified to maintain the gain specified in Av1_set
Ic1_factor = 1;

%At the moment the second stage Ic2 and L3 is set by hand, but could be
%  determined from the calculated first stage gain
Ic2 = 5e-3;
L3 = 376e-12;

%Value of the second stage bias choke
LB2 = 400e-9;
```

```
%************************************************************************
%Performance measure calculations
%************************************************************************

%------- INPUT MATCHING: IC1 AND CAPS -------%
CL1  = Cpi2 + Cmu2 + CL1_add;

CBC  = (C2-Cpi1) / (1+Av1_set);
if( CBC < Cmu1 )
    CBC = Cmu1;
end;
CF   = CBC - Cmu1;

Ic1 = (1 + CL1/CBC) * VT / RS * Ic1_factor;


%------- CALCULATED TRANSISTOR PARAMETERS -------%
gm1   = Ic1/VT;
Beta1 = Beta0 ./ ( 1 + Beta0*(Cpi1+Cmu1)/gm1*i.*w );
Rpi1  = Beta1/gm1;
Ro1   = VA/Ic1;

gm2 = Ic2/VT;
Beta2 = Beta0 ./ ( 1 + Beta0*(Cpi2+Cmu2)/gm2*i.*w );
Rpi2  = Beta0/gm2;
Ro2 = VA/Ic2;


%------- EQUIVALENT IMPEDANCES FOR LATER USE -------%
R_L1  = L1.*w/Q1;  %Inductor parasitic resistance
R_L2  = L2.*w/Q2;
R_L3  = L3.*w./Q3;
Z_L1  = R_L1 + i.*w*L1;  %Equivalent impedance of inductor with parasitics
Z_L2  = R_L2 + i.*w*L2;
Z_L3  = R_L3 + i.*w*L3;
ZS    = 1./(1/RS + 1./Z_L1 + i.*w*C1);  %Parallel combination of RS/C1/L1
Yin2  = 1/Rpi2 + i.*w*(Cpi2+Cmu2) - gm2.*w.^2*Cmu2*L3; %2nd stage Yin


%------- STAGE 1 LOAD RESISTANCE & IMPEDANCE -------%
RL1   = Av1_set / gm1;
ZL1   = 1 ./ ( Yin2 + 1/RL1 + 1/Ro1 + i.*w*CBC + 1./(i.*w.*LB2) + i.*w*CL1_add );


%------- S11 CALCULATION -------%
ZM   = (ZL1 + 1/i./w/CBC)./(1 + gm1.*ZL1);
ZTeq = 1./( 1./Rpi1 + i.*w*Cpi1 + 1./ZM );

Zin = 1./( 1./( ZTeq + Z_L2 ) + i.*w*C1 + 1./Z_L1 );
S11 = 20*log10( abs( (Zin-RS)./(Zin+RS) ) );


%------- S21 CALCULATION -------%
Avin = ZS./RS.*( ZTeq./(ZTeq + Z_L2 + ZS) );

GM1  = gm1 - i.*w*CBC;
Av1  = GM1.*ZL1;

ZL2  = 1./( 1./Z_L3 + 1/RS );
Av2  = gm2.*ZL2;

Av   = Avin.*Av1.*Av2;

AV_IN = 20*log10( abs(Avin) );

AV1   = 20*log10( abs(Av1) );
AV2   = 20*log10( abs(Av2) );
S21   = 20*log10( abs(2*Av) );
```

```
%------- REQUIRED VOLTAGE GAIN - NF vs BW TRADE-OFF -------%
Fmax  = 10^((NFmax+NF_impr)/10);
ZS_fu = abs( 1/(1/RS + 1/(i*wu*L1 + wu*L1/Q1) + i*wu*C1) );
Z2_fu = abs( i*wu*L2 + wu*L2/Q2 );
Fvce  = Fmax - 1 - 1/ZS_fu^2*RS*wu*L2/Q2;
CF_max = sqrt( ((Fvce)/RS/(Rb1 + VT/2/Ic1) - 1/ZS_fu^2) / (1+Z2_fu/ZS_fu)^2 );
Av1_req = abs( 1/(RS*wl/wu*CF_max) );


%------- NOISE FIGURE STAGE 1 -------%
CiT = Cpi1 + CF + Cmu1;

eR_L1 = 4*k*T*R_L1;
eR_L2 = 4*k*T*R_L2;
eRs   = 4*k*T*RS;
VCE   = 4*k*T*(Rb1 + 1/2/gm1) + 2*q*Ic1/Beta0*Rb1^2;
ICE   = abs( 2*q*Ic1/Beta0 + 2*q*Ic1./(Beta1.^2) );

Veq_ICE = ICE .* abs(Z_L2+ZS).^2;
Veq_VCE = VCE .*(1 + abs(Z_L2+ZS).^2.*(w.*CiT).^2);
Veq_RL1 = eR_L1.*abs(ZS./Z_L1).^2;
Veq_RL2 = eR_L2;
Veq_RS  = eRs .*abs(ZS./RS).^2;

Veq1_T = Veq_ICE + Veq_VCE + Veq_RL1 + Veq_RL2 + Veq_RS;
F1  = Veq1_T./Veq_RS;
NF1 = 10*log10( abs(F1) );


%------- NOISE FIGURE STAGE 2 -------%
ZL1 = 1./(1/RL1 + i.*w*(CBC+CL1_add+Cpi2+Cmu2));

iRL1 = 4*k*T/RL1;
iRs  = 4*k*T/RS;
VCE2 = 4*k*T*(Rb2 + 1/2/gm2) + 2*q*Ic2/Beta0*Rb2^2;
ICE2 = abs( 2*q*Ic2/Beta0 + 2*q*Ic2./(Beta2.^2) );

In2_VCE = VCE2./abs(ZL1).^2;
In2_ICE = ICE2;
In2_RL1 = iRL1;

In2 = In2_VCE + In2_ICE + In2_RL1;
F2  = 1 + In2 ./ iRs;
NF2 = 10*log10( abs(F2) );

Veq_In2 = abs( In2./GM1.^2 );

FT  = F1 + Veq_In2./Veq_RS;
NFT = 10*log10( abs(FT) );


%------- IIP3 APPROXIMATION -------%
VIIP3_CE = 2*sqrt(2)*VT;
IIP3 = 10*log10( abs( (VIIP3_CE ./ Av1 ./ Avin / sqrt(2)).^2 /  RS * 1e3 ) );



%------- POWER CONSUMPTION -------%
Pdc1 = Vcc * Ic1;
Pdc2 = Vcc * Ic2;


%**************************************************************************
%Plotting of performance measures
%**************************************************************************
%------- ZIN PLOT -------%
if plotZIN == 1
```

```
    figure( 1 );
    semilogx( f, abs( Zin ), calc_colour,'LineWidth',linewidth );
    hold on;
    y = 0:0.1:130;
    semilogx( fl, y, 'k' );
    semilogx( fu, y, 'k' );
    hold off;
    xlim( [ flcalc fucalc ] );
    ylim( [ 0 130 ] );
    xlabel( 'Frequency [Hz]' );
    ylabel( 'Zin [ohm]' );
end;

%------- S11 PLOT -------%
figure( 2 );
semilogx( f, S11, calc_colour,'LineWidth',linewidth );
hold on;
if plot_sim == 1
    semilogx( f_sim, S11_sim, sim_colour,'LineWidth',linewidth );
    legend( 'Calculated S_1_1', 'Simulated S_1_1', 'Location', 'Southwest' );
end
y = -25:0.02:0;
semilogx( fl, y, 'k' );
semilogx( fu, y, 'k' );
hold off;
xlim( [ flcalc fucalc ] );
xlabel( 'Frequency [Hz]' );
ylabel( 'S_1_1 [dB]' );

%------- S21 PLOT -------%
figure( 3 );
semilogx( f, S21-6, calc_colour,'LineWidth',linewidth );
hold on;
%semilogx( f, AV_IN, 'r','LineWidth',linewidth );
%semilogx( f, AV1, 'm','LineWidth',linewidth );
%semilogx( f, AV2, 'b','LineWidth',linewidth );
if plot_sim == 1
    semilogx( f_sim, S21_sim, sim_colour,'LineWidth',linewidth );
    legend( 'Calculated S_2_1', 'Simulated S_2_1', 'Location', 'South' );
end
y = -30:0.1:40;
semilogx( fl, y, 'k' );
semilogx( fu, y, 'k' );
hold off;
xlim( [ flcalc, fucalc ] );
ylim( [ -30 35 ] );
xlabel( 'Frequency [Hz]' );
ylabel( 'S_2_1 [dB]' );

%------- NOISE SOURCES PLOT -------%
if plotNSources == 1
    figure( 4 );
    semilogx( f, Veq_RS , 'k-s','LineWidth',linewidth );
    hold on;
    semilogx( f, Veq_VCE, 'k-^','LineWidth',linewidth );
    semilogx( f, Veq_ICE, 'k-','LineWidth',linewidth );
    semilogx( f, Veq_RL1, 'k--','LineWidth',linewidth );
    semilogx( f, Veq_RL2, 'k-d','LineWidth',linewidth );
    semilogx( f, Veq_In2, 'k-o','LineWidth',linewidth );
    hold off;
    xlim( [ fl fu ] );
    xlabel( 'Frequency [Hz]' );
    ylabel( 'Equivalent noise voltage [V  ^2/ Hz]' );
    legend( 'n_R_S', 'n_V_C_E', 'n_I_C_E', 'n_R_L_1', 'n_R_L_2', 'n_A_2',
'Location', 'Best' );
end;

%------- NOISE FIGURE PLOT -------%
figure( 5 );
```

```
semilogx( f, NFT, calc_colour,'LineWidth',linewidth );
hold on;
if plot_sim == 1
    semilogx( f_sim, NF_sim, sim_colour,'LineWidth',linewidth );
    legend( 'Calculated NF', 'Simulated NF', 'Location', 'North' );
end
hold off;
xlim( [ fl fu ] );
xlabel( 'Frequency [Hz]' );
ylabel( 'NF [dB]' );

%------- IIP3 PLOT -------%
if plotIIP3 == 1
    figure( 6 );
    semilogx( f, IIP3, calc_colour,'LineWidth',linewidth );
    xlim( [ fl fu ] );
    xlabel( 'Frequency [Hz]' );
    ylabel( 'IIP3 [dBm]' );
end;


%************************************************************************
%Print the design parameters to the output
%************************************************************************
disp( '-------------------------------------------' );
disp( 'Power consumption (excluding biasing):' );
power_stages = sprintf( 'Pdc1 = %g mW\tPdc2 = %g mW', Pdc1/1e-3, Pdc2/1e-3 );
disp( power_stages );
power_total = sprintf( 'Pdc  = %g mW\n', (Pdc1+Pdc2)/1e-3 );
disp( power_total );

disp( 'DC biasing:' );
dc_biasing = sprintf( 'Ic1 = %g mA\tIc2 = %.3g mA\n', Ic1/1e-3, Ic2/1e-3 );
disp( dc_biasing );

disp( '' );
required_av1 = sprintf( 'Required stage 1 gain: %.3g\n', Av1_req );
disp( required_av1 );

disp( 'Matching:' );
match_components_L = sprintf( 'L1 = %.3g nH\tL2 = %.3g pH',L1/1e-9, L2/1e-12 );
disp( match_components_L );
match_components_C = sprintf('C1 = %.3g fF\tC2 = %.3g pF\n',C1/1e-15, C2/1e-12 );
disp( match_components_C );

disp( 'Aplifier stage 1 components:' );
amp_components1_C = sprintf( 'CF = %.3g fF\tCL1 = %.3g fF',CF/1e-15, CL1_add/1e-
15 );
disp( amp_components1_C );
amp_components1_R = sprintf( 'RL1 = %.3g Ohm\n', RL1 );
disp( amp_components1_R );

disp( 'Aplifier stage 2 components:' );
amp_components2 = sprintf( 'L3 = %.3g nH\n', L3/1e-9 );
disp( amp_components2 );
```

ADDENDUM B: DETAILED FIGURES OF THE LAYOUT

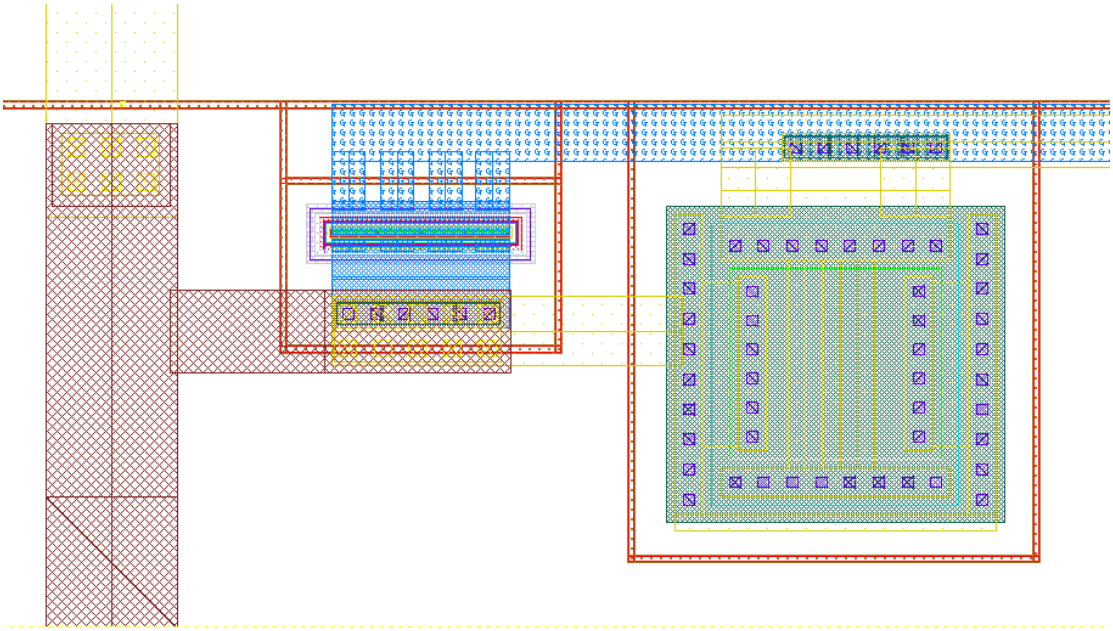


Figure B.1. Layout of the first stage on-chip bias circuit, showing the diode connected transistor and decoupling dual-MIM capacitor. To the left is the connection from the input pad to inductor L_1, and to the right the ground connection.

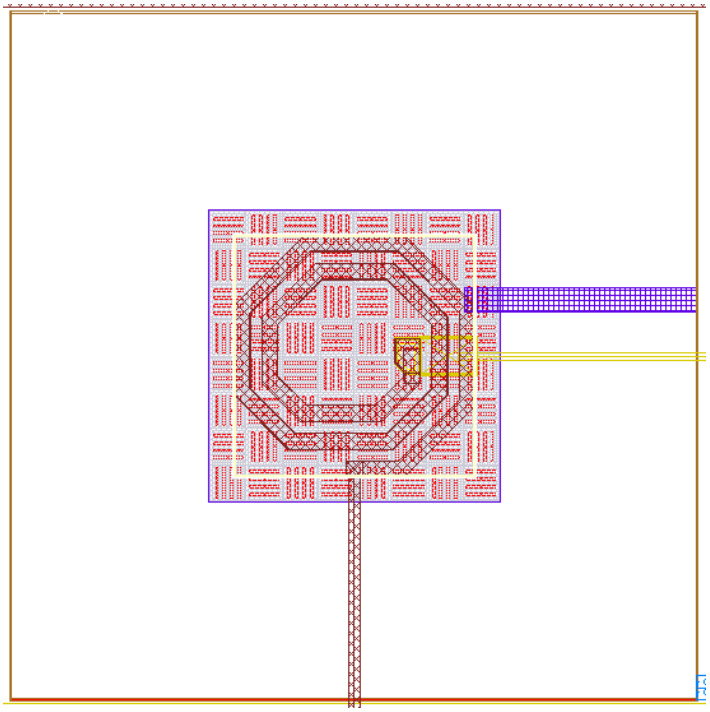


Figure B.2. On-chip spiral inductor layout showing the 80 µm guard ring where neither other components nor substrate contacts are placed. This area is enclosed by substrate contacts.

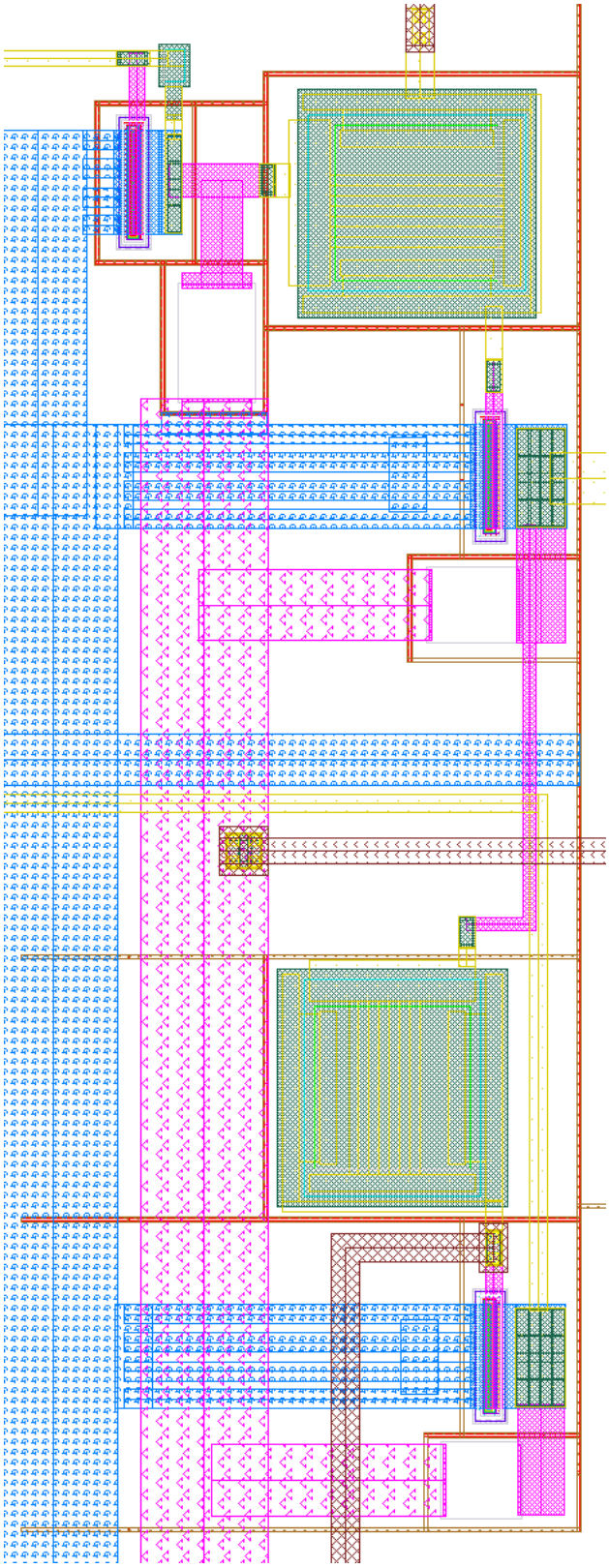


Figure B.3. First, second and third transistor stages with DC-blocking dual-MIM capacitors and load resistances. The connections on the right are to the second stage load inductor. At the top and bottom are the respective connections to the second and third stage bias pins, and at the top left the signal input to Q_1 and C_F from L_2.

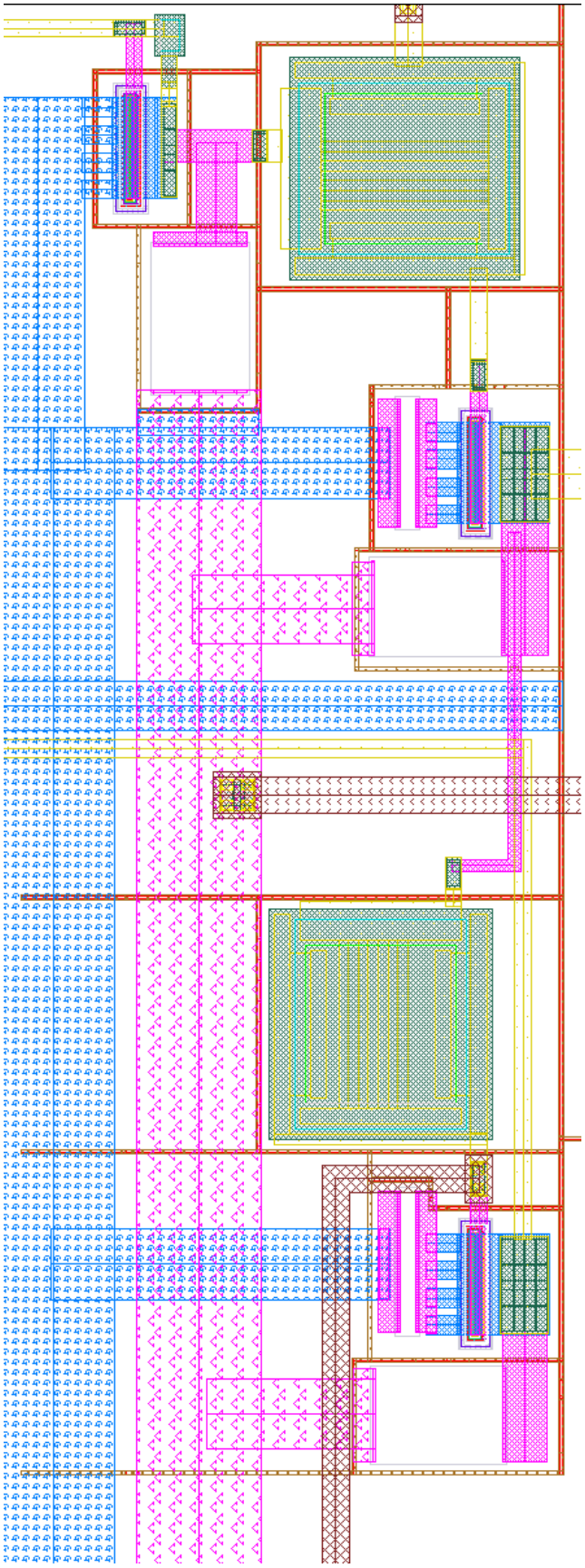


Figure B.4. Layout of the LNA with the linearity improvement showing the added emitter resistors of transistors Q_2 and Q_3.

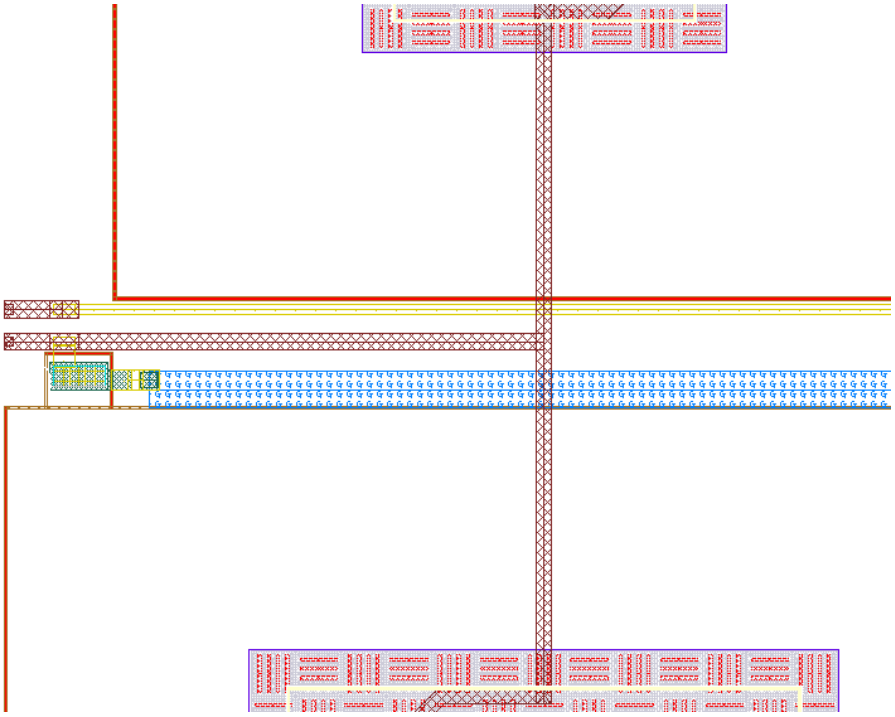


Figure B.5. Layout of the input matching network showing the connection from the input pin on the left connected to C_1 and also the shunt L_1 at the bottom and series L_2 at the top of which the other terminal is connected to Q_1 and C_F.

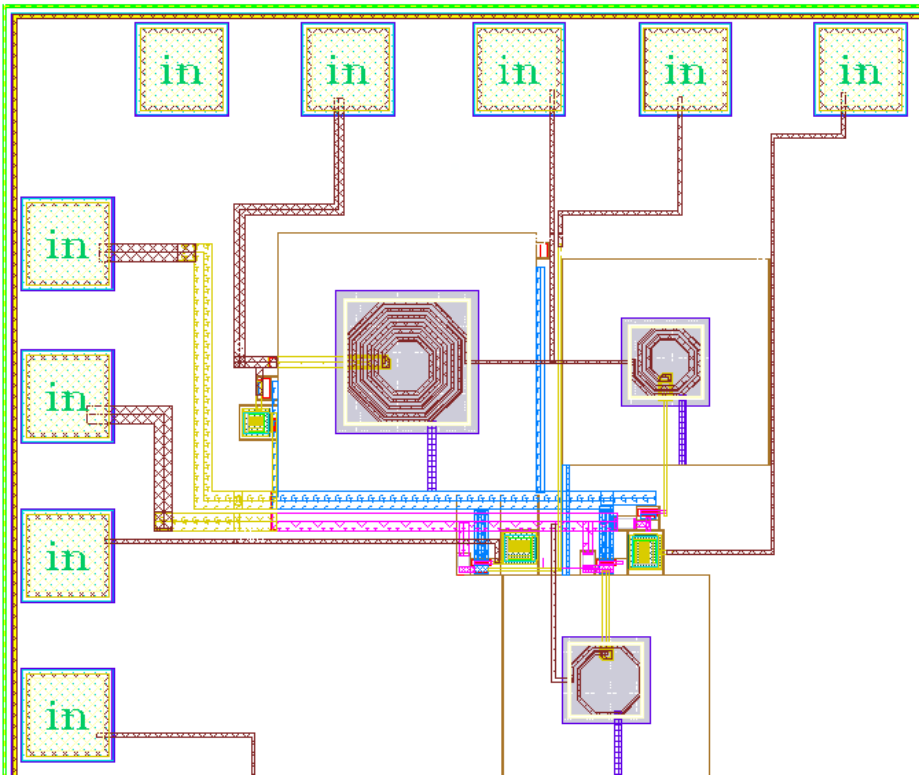
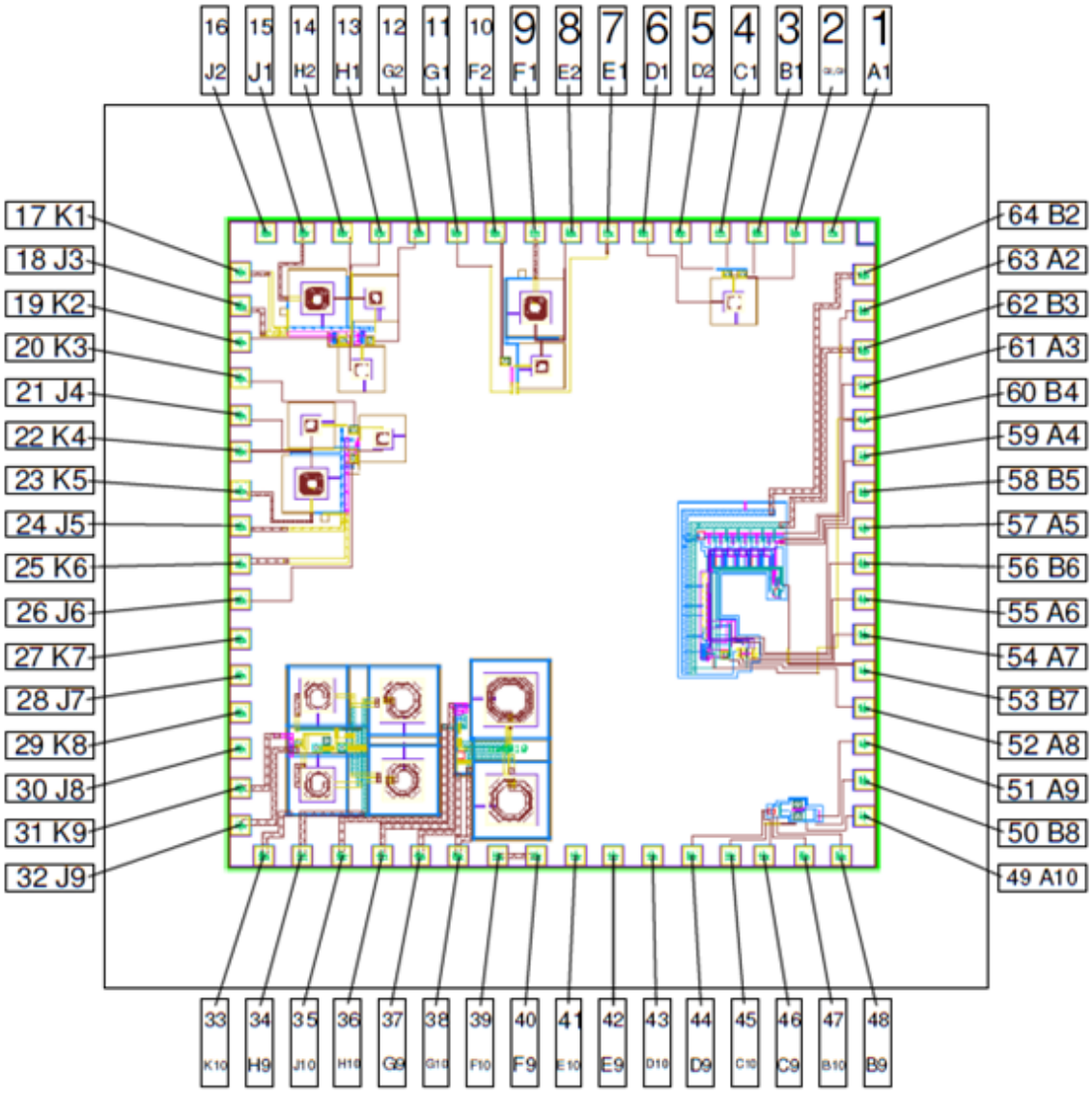


Figure B.6. Layout of the standard LNA (without local feedback) and its connection to bond pads.



Qty: 15	V01N-AA	OCP_QFN_9X9_64A
	(82439)	
Customer Providing Diagram		
Minimum pad size: 100 x 100; minimum pad pitch: 205 um		
Standard 1 mil Gold bond wires		
MOSIS	Design_name: LNA for Ku-Band Receivers / Reducing Jitter usi...	
	Customer Account: 5198	
	Die Size: 4093 (+0 / -72) x 4129 (+0 / -72) um	
	Die Rotation in Cavity: None	
	Cavity Size: 6900 um x 6900 um	18-MAR-2010 12:21:35

Figure B.7. Bonding diagram of the fabricated LNAs on the MPW chip, showing the standard LNA in the top left, the LNA with feedback below that and the separate first and second stages to the right.

In the research carried out toward the derivation of a mathematical model for the proposed LNA configuration, it was necessary to design certain LNAs to verify the model. As such two LNAs have been submitted for fabrication in order to absolutely corroborate the simulated results, and the datasheet below serves as a summary of these particular LNAs which will be used to obtain measured results.

3-14 GHz LNA Data Sheet

A very robust 3-14 GHz wideband LNA implemented with the LC-ladder and capacitive shunt-shunt feedback configuration. Both a standard LNA and one with improved linearity, but slightly poorer noise performance, are available. Two individual testing amplifier stages are also included.

Biasing

The first stage of the LNA uses current biasing and the current should be set using a 400 Ω series resistance to the positive supply.

The second and third stages require voltage biasing for which the active bias circuit in Figure 1 is suggested.

Signal connections

50 Ω input and output signal traces should be connected to the input and output pins through 15 pF DC-blocking capacitors.

Specifications

	Standard	High IIP3
BW	3-14 GHz	3-14 GHz
S_{11}	< -10 dB	< -9.8 dB
S_{21}	20.9 dB	20 dB
NF	1.7-3.3 dB	2.2-3.9 dB
IIP3	-22.6 dBm @ 4.2 GHz	-14.5 dBm @ 4.2 GHz
V_{CC}	1.8 V	1.8 V
I_{C1}	2.5 mA	2.5 mA
I_{C2}	2.7 mA	8 mA
I_{C3}	2.7 mA	8 mA

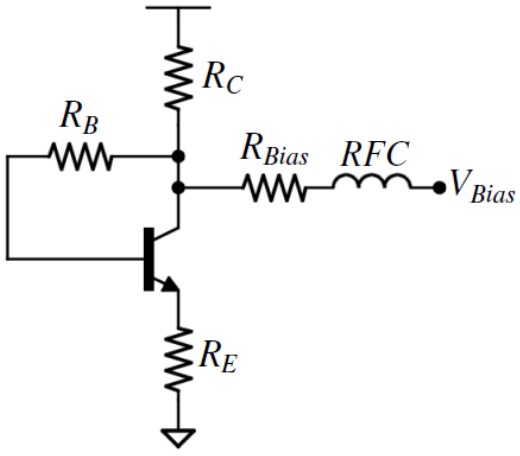


Figure 1. Active bias circuit example.

Pin Diagram

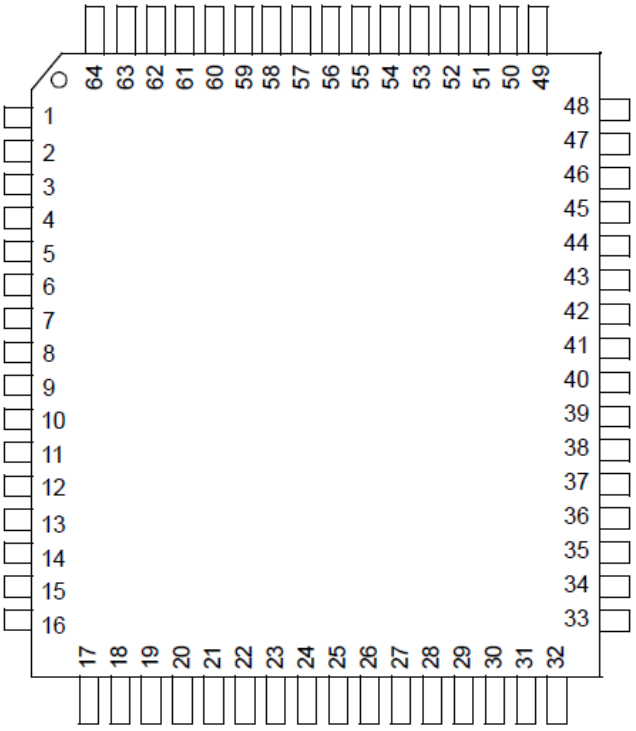


Figure 2. Pin diagram of the 3-14 GHz LNA

Pin	Name	Description
2	Std_Vcc	Standard LNA 1.8 V supply
1	Std_Gnd	Standard LNA ground
63	Std_Bias1	Standard LNA stage 1 current bias (400 Ω R to supply)
60	Std_Bias2	Standard LNA stage 2 voltage bias
3	Std_Bias3	Standard LNA stage 3 voltage bias
62	Std_In	Standard LNA RF input from 50 Ω source with15 pF DC-blocking capacitor
61	Std_Out	Standard LNA RF output to 50 Ω load with15 pF DC-blocking capacitor
9	Lin_Vcc	Linear LNA 1.8 V supply
8	Lin_Gnd	Linear LNA ground
7	Lin_Bias1	Linear LNA stage 1 current bias (400 Ω R to supply)
4	Lin_Bias2	Linear LNA stage 2 voltage bias
10	Lin_Bias3	Linear LNA stage 3 voltage bias

6	Lin_In	Linear LNA RF input from 50 Ω source with15 pF DC-blocking capacitor
5	Lin_Out	Linear LNA RF output to 50 Ω load with15 pF DC-blocking capacitor
59	S1_Vcc	Testing stage 1 LNA 1.8 V supply
56	S1_Gnd	Testing stage 1 LNA ground
57	S1_Bias1	Testing stage 1 current bias (400 Ω R to supply)
55	S1_In	Testing stage 1 LNA RF input from 50 Ω source with 15 pF DC-blocking capacitor
58	S1_Out	Testing stage 1 LNA RF output to 50 Ω load (on-chip blocking capacitor)
54	S2_Vcc	Testing stage 2 LNA 1.8 V supply
53	S2_Gnd	Testing stage 2 LNA ground
50	S2_Bias1	Testing stage 2 current bias (400 Ω R to supply)
51	S2_In	Testing stage 2 LNA RF input from 50 Ω source with (on-chip blocking capacitor)
52	S2_Out	Testing stage 2 LNA RF output to 50 Ω load (on-chip blocking capacitor)

Pins not referred above were used for prototyping by other parties/students (MPW).