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ADDENDUM A: PRELIMINARY MATLAB CODE FOR EDA

The preliminary code towards the implementation of EDA software written in MATLAB and used throughout this research to design the LNAs is given below.

```
clear all;

%----- SPECIFICATIONS ------------%
%The specified frequency range, gain and max NF for the design are set here
fl = 1e9;   wl = 2*pi*fl;
fu = 18e9;  wu = 2*pi*fu;
S21_spec = 20;  %dB
NFmax = 4;  %dB
RS = 50;


%----- PLOT SETTINGS -------------%
%Settings related to the display of the result plots
flcalc = fl/10;      % The range overwhich values are
fucalc = fu*10;      %   calculated beyond the operting frequency band
pts = 500;           % Number of points in the plot
linewidth = 2;       % Linewidth used in plots
calc_colour = 'k-.'; % Colour and line style used for calculated and
sim_colour = 'k-';   %   simulated result plots
%---------------------------------%

%----- PLOT FLAGS ----------------%
% Flags for choosing when to plot input impedance, individual noise
% contributions, IIP3 or simulated results read from a csv file
plotZIN = 0;
plotNSources = 0;
plotIIP3 = 0;
plot_sim = 0;


%----- SIMULATED RESULTS READIN -------------%
if( plot_sim == 1 )
    cnt = 451;
    load sim_1GHz_to_18GHz_gain_cur_pas/S11_s.csv;
    load sim_1GHz_to_18GHz_gain_cur_pas/S21_s.csv;
    load sim_1GHz_to_18GHz_gain_cur_pas/NF_s.csv;
    f_sim = 1:cnt;
    S11_sim = 1:cnt;
    S21_sim = 1:cnt;
    NF_sim = 1:cnt;
    for u = 1:cnt
        f_sim(u) = S11_s( u, 1 );
        S11_sim(u) = S11_s( u, 2 );
        S21_sim(u) = S21_s( u, 2 );
        NF_sim(u) = NF_s( u, 2 );
    end;
end;


%*************************************************************************
%Environment setup
%*************************************************************************
%Create logarithmic frequency values based on the range and no. of points
ll = log10( flcalc );
lh = log10( fucalc );
l_inc = (lh-ll)/pts;
lf = ll:l_inc:lh;
f = 10.^lf;
w = 2*pi.*f;
```

```
%Physical constants definition
k = 1.38e-23;       %   Boltzmann's constant
q = 1.602e-19;      %   Electron charge
T = 290;            %   Temperature in Kelvin
VT = k*T/q;         %   Thermal voltage

%Load transistor parasitic values and process parameters
%---- TRANSISTOR1 PARAMETERS -----%
Rb1  = 13.7 + 5.8;
Re1  = 1.53;
Cmu1 = 1.38e-15 + 9.52e-15 + 9.11e-15;
Cpi1 = 18.1e-15 + 18.6e-15;

%---- TRANSISTOR2 PARAMETERS -----%
Rb2  = 13.7 + 5.8;
Re2  = 1.53;
Cmu2 = 1.38e-15 + 9.52e-15 + 9.11e-15;
Cpi2 = 18.1e-15 + 18.6e-15;

%------ PROCESS PARAMETERS -------%
Beta0 = 300;
Vcc = 1.5;
Vce = 0.2;
VA = 16.36;
Q1 = 1.5;
Q2 = 3;
Q3 = 5;
%---------------------------------%


%*************************************************************************
%These values are changed during the design phase
%These and selected calculated values are printed in the output to aid
%in the optimization process.
%*************************************************************************
%------- DESIGN PARAMETERS -------%
Av1_set = 27;  %Used to modify the first stage gain - initial value should
               %be the maximum allowed by the GBP

NF_impr = 2;   %Expected NF improvement through optimization process
               %Allows for less stringent yet appropriate Av1_req values

%Equations to calculate the initial IMN reactive elements
C1 = 1/RS/wu;
C2 = 1/RS/wl;
L1 = RS/wl;
L2 = RS/wu;
%During optimization the above equations are commented and the values
%  modified below
%C1 = 40e-15;
%C2 = 3.18e-12;
%L1 = 9.91e-9;
%L2 = 363e-12;

%Additional first stage load capacitance added during optimization
CL1_add = 0e-15;   %Initial value = 0

%Amount by which the first stage collector current is increased above the
%  calculated value; RL1 is modified to maintain the gain specified in Av1_set
Ic1_factor = 1;

%At the moment the second stage Ic2 and L3 is set by hand, but could be
%  determined from the calculated first stage gain
Ic2 = 5e-3;
L3 = 376e-12;

%Value of the second stage bias choke
LB2 = 400e-9;
```

```
%************************************************************************
%Performance measure calculations
%************************************************************************

%------- INPUT MATCHING: IC1 AND CAPS -------%
CL1  = Cpi2 + Cmu2 + CL1_add;

CBC  = (C2-Cpi1) / (1+Av1_set);
if( CBC < Cmu1 )
    CBC = Cmu1;
end;
CF   = CBC - Cmu1;

Ic1 = (1 + CL1/CBC) * VT / RS * Ic1_factor;


%------- CALCULATED TRANSISTOR PARAMETERS -------%
gm1   = Ic1/VT;
Beta1 = Beta0 ./ ( 1 + Beta0*(Cpi1+Cmu1)/gm1*i.*w );
Rpi1  = Beta1/gm1;
Ro1   = VA/Ic1;

gm2 = Ic2/VT;
Beta2 = Beta0 ./ ( 1 + Beta0*(Cpi2+Cmu2)/gm2*i.*w );
Rpi2  = Beta0/gm2;
Ro2 = VA/Ic2;


%------- EQUIVALENT IMPEDANCES FOR LATER USE -------%
R_L1  = L1.*w/Q1;  %Inductor parasitic resistance
R_L2  = L2.*w/Q2;
R_L3  = L3.*w./Q3;
Z_L1  = R_L1 + i.*w*L1;  %Equivalent impedance of inductor with parasitics
Z_L2  = R_L2 + i.*w*L2;
Z_L3  = R_L3 + i.*w*L3;
ZS    = 1./(1/RS + 1./Z_L1 + i.*w*C1);  %Parallel combination of RS/C1/L1
Yin2  = 1/Rpi2 + i.*w*(Cpi2+Cmu2) - gm2.*w.^2*Cmu2*L3; %2nd stage Yin


%------- STAGE 1 LOAD RESISTANCE & IMPEDANCE -------%
RL1   = Av1_set / gm1;
ZL1   = 1 ./ ( Yin2 + 1/RL1 + 1/Ro1 + i.*w*CBC + 1./(i.*w.*LB2) + i.*w*CL1_add );


%------- S11 CALCULATION -------%
ZM   = (ZL1 + 1/i./w/CBC)./(1 + gm1.*ZL1);
ZTeq = 1./( 1./Rpi1 + i.*w*Cpi1 + 1./ZM );

Zin = 1./( 1./( ZTeq + Z_L2 ) + i.*w*C1 + 1./Z_L1 );
S11 = 20*log10( abs( (Zin-RS)./(Zin+RS) ) );


%------- S21 CALCULATION -------%
Avin = ZS./RS.*( ZTeq./(ZTeq + Z_L2 + ZS) );

GM1  = gm1 - i.*w*CBC;
Av1  = GM1.*ZL1;

ZL2  = 1./( 1./Z_L3 + 1/RS );
Av2  = gm2.*ZL2;

Av   = Avin.*Av1.*Av2;

AV_IN = 20*log10( abs(Avin) );

AV1   = 20*log10( abs(Av1) );
AV2   = 20*log10( abs(Av2) );
S21   = 20*log10( abs(2*Av) );
```

```
%------- REQUIRED VOLTAGE GAIN - NF vs BW TRADE-OFF -------%
Fmax  = 10^((NFmax+NF_impr)/10);
ZS_fu = abs( 1/(1/RS + 1/(i*wu*L1 + wu*L1/Q1) + i*wu*C1) );
Z2_fu = abs( i*wu*L2 + wu*L2/Q2 );
Fvce  = Fmax - 1 - 1/ZS_fu^2*RS*wu*L2/Q2;
CF_max = sqrt( ((Fvce)/RS/(Rb1 + VT/2/Ic1) - 1/ZS_fu^2) / (1+Z2_fu/ZS_fu)^2 );
Av1_req = abs( 1/(RS*wl/wu*CF_max) );


%------- NOISE FIGURE STAGE 1 -------%
CiT = Cpi1 + CF + Cmu1;

eR_L1 = 4*k*T*R_L1;
eR_L2 = 4*k*T*R_L2;
eRs   = 4*k*T*RS;
VCE   = 4*k*T*(Rb1 + 1/2/gm1) + 2*q*Ic1/Beta0*Rb1^2;
ICE   = abs( 2*q*Ic1/Beta0 + 2*q*Ic1./(Beta1.^2) );

Veq_ICE = ICE .* abs(Z_L2+ZS).^2;
Veq_VCE = VCE .*(1 + abs(Z_L2+ZS).^2.*(w.*CiT).^2);
Veq_RL1 = eR_L1.*abs(ZS./Z_L1).^2;
Veq_RL2 = eR_L2;
Veq_RS  = eRs .*abs(ZS./RS).^2;

Veq1_T = Veq_ICE + Veq_VCE + Veq_RL1 + Veq_RL2 + Veq_RS;
F1  = Veq1_T./Veq_RS;
NF1 = 10*log10( abs(F1) );


%------- NOISE FIGURE STAGE 2 -------%
ZL1 = 1./(1/RL1 + i.*w*(CBC+CL1_add+Cpi2+Cmu2));

iRL1 = 4*k*T/RL1;
iRs  = 4*k*T/RS;
VCE2 = 4*k*T*(Rb2 + 1/2/gm2) + 2*q*Ic2/Beta0*Rb2^2;
ICE2 = abs( 2*q*Ic2/Beta0 + 2*q*Ic2./(Beta2.^2) );

In2_VCE = VCE2./abs(ZL1).^2;
In2_ICE = ICE2;
In2_RL1 = iRL1;

In2 = In2_VCE + In2_ICE + In2_RL1;
F2  = 1 + In2 ./ iRs;
NF2 = 10*log10( abs(F2) );

Veq_In2 = abs( In2./GM1.^2 );

FT  = F1 + Veq_In2./Veq_RS;
NFT = 10*log10( abs(FT) );


%------- IIP3 APPROXIMATION -------%
VIIP3_CE = 2*sqrt(2)*VT;
IIP3 = 10*log10( abs( (VIIP3_CE ./ Av1 ./ Avin / sqrt(2)).^2 /  RS * 1e3 ) );



%------- POWER CONSUMPTION -------%
Pdc1 = Vcc * Ic1;
Pdc2 = Vcc * Ic2;


%**************************************************************************
%Plotting of performance measures
%**************************************************************************
%------- ZIN PLOT -------%
if plotZIN == 1
```

```
    figure( 1 );
    semilogx( f, abs( Zin ), calc_colour,'LineWidth',linewidth );
    hold on;
    y = 0:0.1:130;
    semilogx( fl, y, 'k' );
    semilogx( fu, y, 'k' );
    hold off;
    xlim( [ flcalc fucalc ] );
    ylim( [ 0 130 ] );
    xlabel( 'Frequency [Hz]' );
    ylabel( 'Zin [ohm]' );
end;

%------- S11 PLOT -------%
figure( 2 );
semilogx( f, S11, calc_colour,'LineWidth',linewidth );
hold on;
if plot_sim == 1
    semilogx( f_sim, S11_sim, sim_colour,'LineWidth',linewidth );
    legend( 'Calculated S_1_1', 'Simulated S_1_1', 'Location', 'Southwest' );
end
y = -25:0.02:0;
semilogx( fl, y, 'k' );
semilogx( fu, y, 'k' );
hold off;
xlim( [ flcalc fucalc ] );
xlabel( 'Frequency [Hz]' );
ylabel( 'S_1_1 [dB]' );

%------- S21 PLOT -------%
figure( 3 );
semilogx( f, S21-6, calc_colour,'LineWidth',linewidth );
hold on;
%semilogx( f, AV_IN, 'r','LineWidth',linewidth );
%semilogx( f, AV1, 'm','LineWidth',linewidth );
%semilogx( f, AV2, 'b','LineWidth',linewidth );
if plot_sim == 1
    semilogx( f_sim, S21_sim, sim_colour,'LineWidth',linewidth );
    legend( 'Calculated S_2_1', 'Simulated S_2_1', 'Location', 'South' );
end
y = -30:0.1:40;
semilogx( fl, y, 'k' );
semilogx( fu, y, 'k' );
hold off;
xlim( [ flcalc, fucalc ] );
ylim( [ -30 35 ] );
xlabel( 'Frequency [Hz]' );
ylabel( 'S_2_1 [dB]' );

%------- NOISE SOURCES PLOT -------%
if plotNSources == 1
    figure( 4 );
    semilogx( f, Veq_RS , 'k-s','LineWidth',linewidth );
    hold on;
    semilogx( f, Veq_VCE, 'k-^','LineWidth',linewidth );
    semilogx( f, Veq_ICE, 'k-','LineWidth',linewidth );
    semilogx( f, Veq_RL1, 'k--','LineWidth',linewidth );
    semilogx( f, Veq_RL2, 'k-d','LineWidth',linewidth );
    semilogx( f, Veq_In2, 'k-o','LineWidth',linewidth );
    hold off;
    xlim( [ fl fu ] );
    xlabel( 'Frequency [Hz]' );
    ylabel( 'Equivalent noise voltage [V  ^2/ Hz]' );
    legend( 'n_R_S', 'n_V_C_E', 'n_I_C_E', 'n_R_L_1', 'n_R_L_2', 'n_A_2',
'Location', 'Best' );
end;

%------- NOISE FIGURE PLOT -------%
figure( 5 );
```

```
semilogx( f, NFT, calc_colour,'LineWidth',linewidth );
hold on;
if plot_sim == 1
    semilogx( f_sim, NF_sim, sim_colour,'LineWidth',linewidth );
    legend( 'Calculated NF', 'Simulated NF', 'Location', 'North' );
end
hold off;
xlim( [ fl fu ] );
xlabel( 'Frequency [Hz]' );
ylabel( 'NF [dB]' );

%------- IIP3 PLOT -------%
if plotIIP3 == 1
    figure( 6 );
    semilogx( f, IIP3, calc_colour,'LineWidth',linewidth );
    xlim( [ fl fu ] );
    xlabel( 'Frequency [Hz]' );
    ylabel( 'IIP3 [dBm]' );
end;


%************************************************************************
%Print the design parameters to the output
%************************************************************************
disp( '-------------------------------------------' );
disp( 'Power consumption (excluding biasing):' );
power_stages = sprintf( 'Pdc1 = %g mW\tPdc2 = %g mW', Pdc1/1e-3, Pdc2/1e-3 );
disp( power_stages );
power_total = sprintf( 'Pdc  = %g mW\n', (Pdc1+Pdc2)/1e-3 );
disp( power_total );

disp( 'DC biasing:' );
dc_biasing = sprintf( 'Ic1 = %g mA\tIc2 = %.3g mA\n', Ic1/1e-3, Ic2/1e-3 );
disp( dc_biasing );

disp( '' );
required_av1 = sprintf( 'Required stage 1 gain: %.3g\n', Av1_req );
disp( required_av1 );

disp( 'Matching:' );
match_components_L = sprintf( 'L1 = %.3g nH\tL2 = %.3g pH',L1/1e-9, L2/1e-12 );
disp( match_components_L );
match_components_C = sprintf('C1 = %.3g fF\tC2 = %.3g pF\n',C1/1e-15, C2/1e-12 );
disp( match_components_C );

disp( 'Aplifier stage 1 components:' );
amp_components1_C = sprintf( 'CF = %.3g fF\tCL1 = %.3g fF',CF/1e-15, CL1_add/1e-
15 );
disp( amp_components1_C );
amp_components1_R = sprintf( 'RL1 = %.3g Ohm\n', RL1 );
disp( amp_components1_R );

disp( 'Aplifier stage 2 components:' );
amp_components2 = sprintf( 'L3 = %.3g nH\n', L3/1e-9 );
disp( amp_components2 );
```

ADDENDUM B: DETAILED FIGURES OF THE LAYOUT

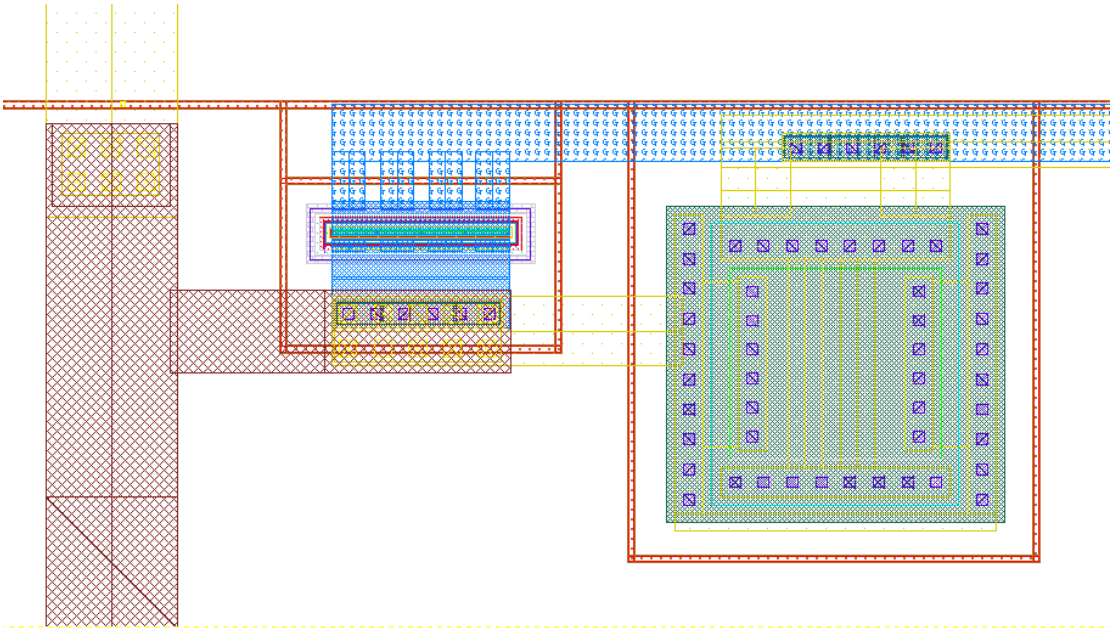


Figure B.1. Layout of the first stage on-chip bias circuit, showing the diode connected transistor and decoupling dual-MIM capacitor. To the left is the connection from the input pad to inductor L_1, and to the right the ground connection.

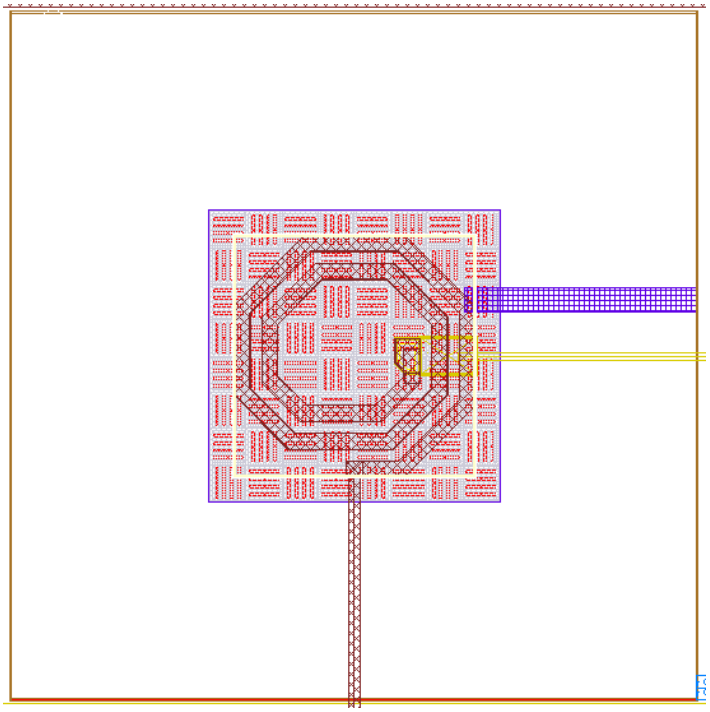


Figure B.2. On-chip spiral inductor layout showing the 80 µm guard ring where neither other components nor substrate contacts are placed. This area is enclosed by substrate contacts.

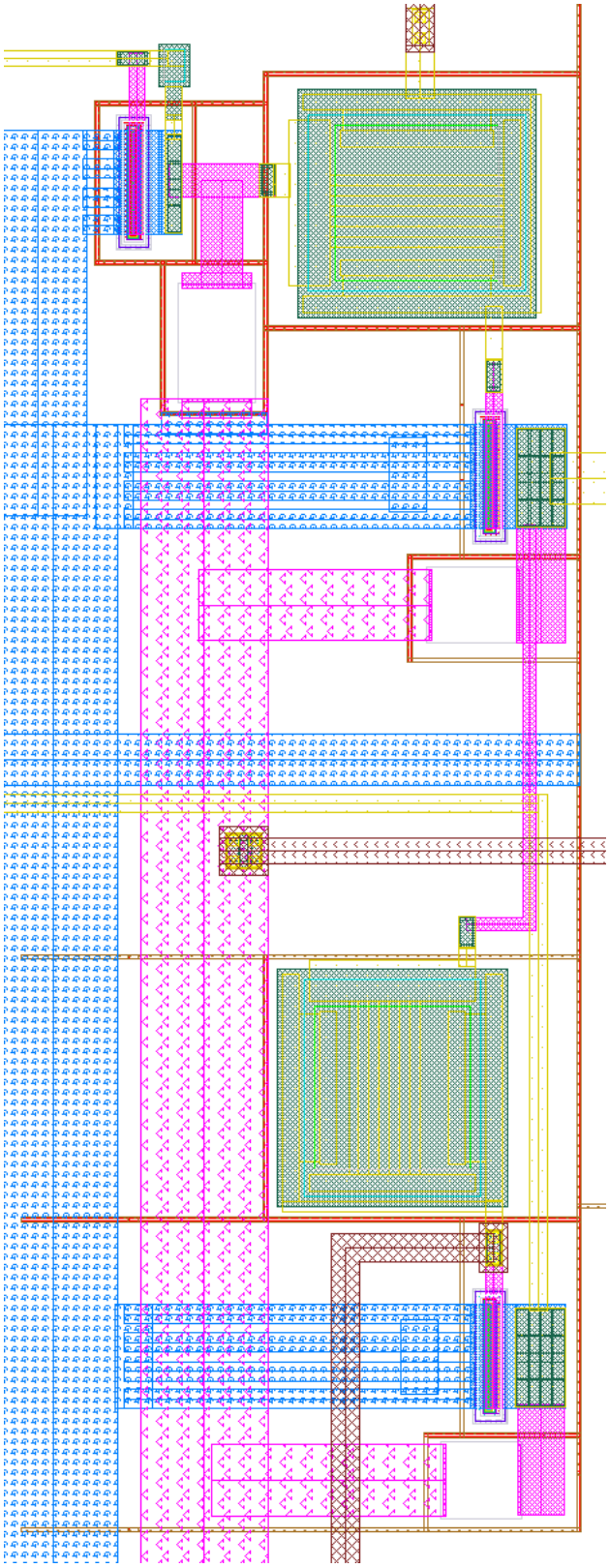


Figure B.3. First, second and third transistor stages with DC-blocking dual-MIM capacitors and load resistances. The connections on the right are to the second stage load inductor. At the top and bottom are the respective connections to the second and third stage bias pins, and at the top left the signal input to Q_1 and C_F from L_2.

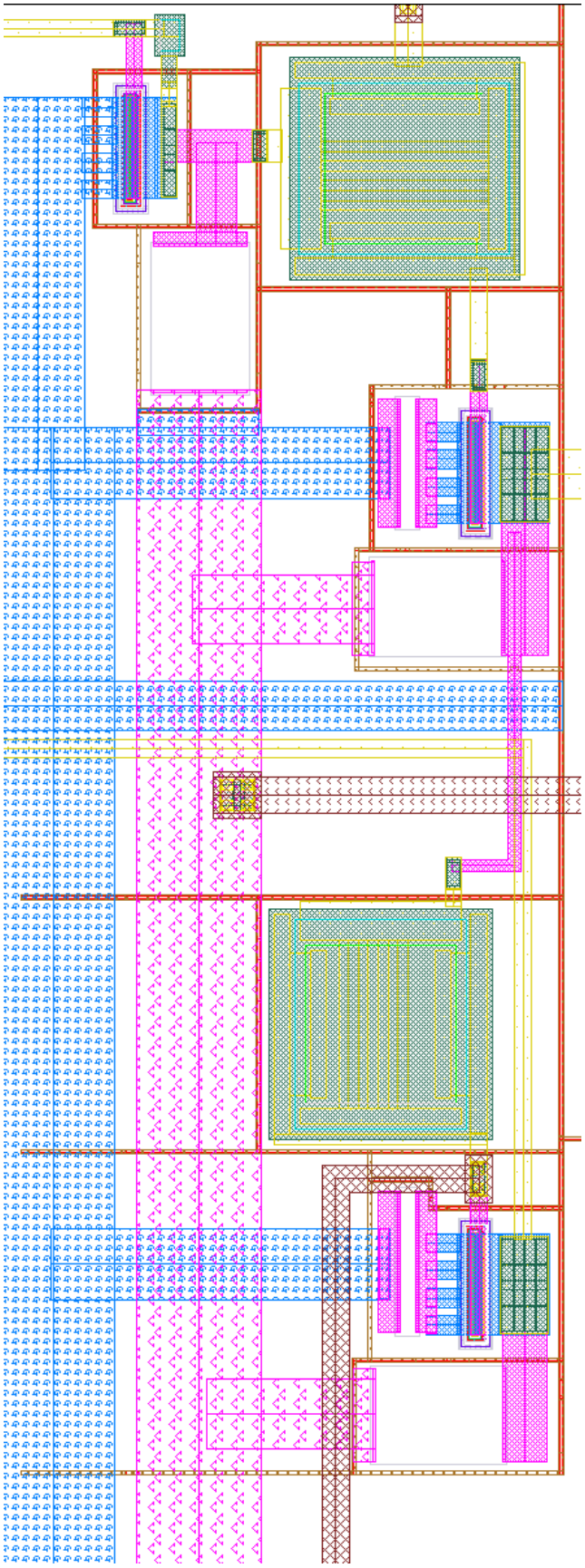


Figure B.4. Layout of the LNA with the linearity improvement showing the added emitter resistors of transistors Q_2 and Q_3.

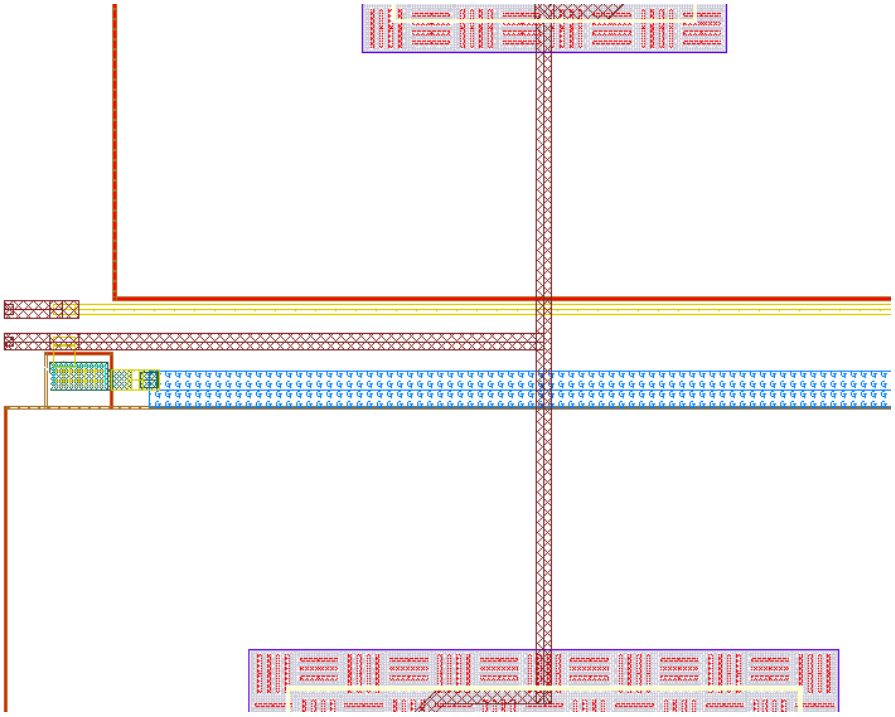


Figure B.5. Layout of the input matching network showing the connection from the input pin on the left connected to C_1 and also the shunt L_1 at the bottom and series L_2 at the top of which the other terminal is connected to Q_1 and C_F.

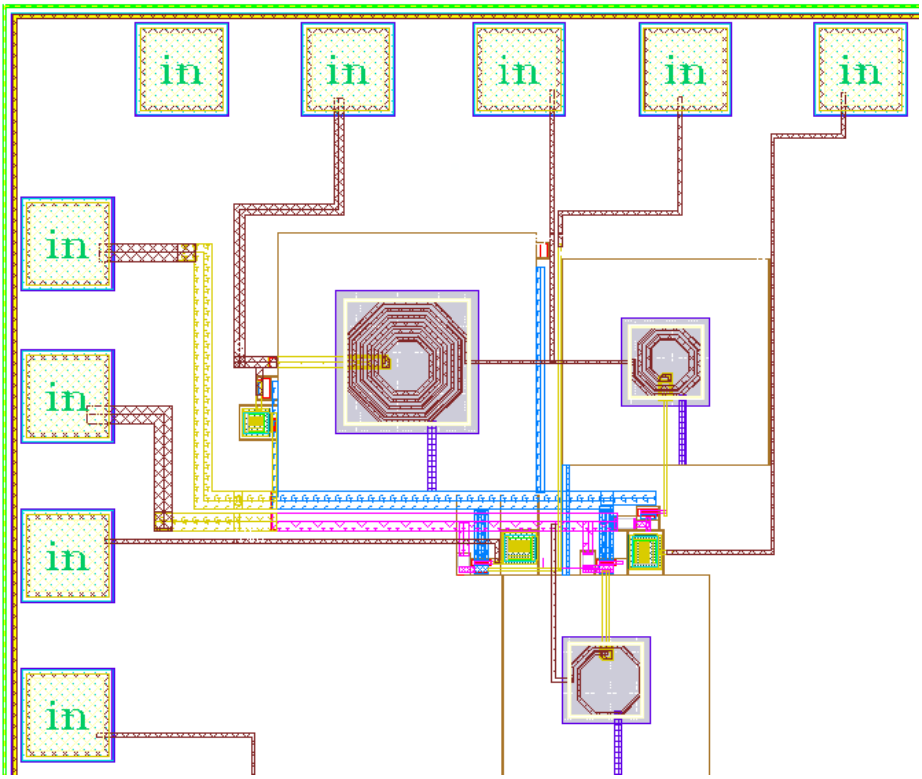
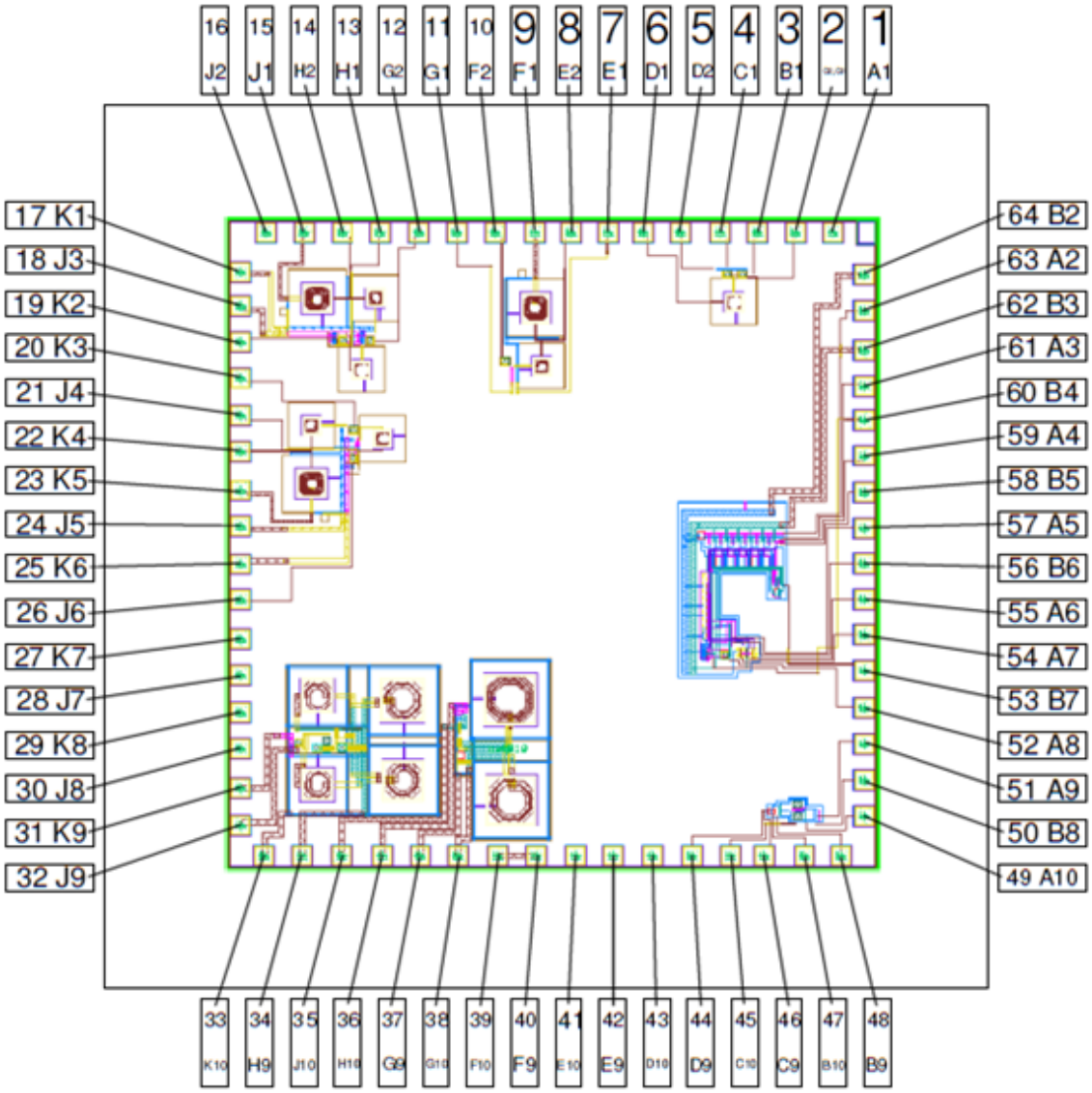


Figure B.6. Layout of the standard LNA (without local feedback) and its connection to bond pads.



Qty: 15	V01N-AA	OCP_QFN_9X9_64A
	(82439)	
Customer Providing Diagram		
Minimum pad size: 100 x 100; minimum pad pitch: 205 um		
Standard 1 mil Gold bond wires		
MOSIS	Design_name: LNA for Ku-Band Receivers / Reducing Jitter usi...	
	Customer Account: 5198	
	Die Size: 4093 (+0 / -72) x 4129 (+0 / -72) um	
	Die Rotation in Cavity: None	
	Cavity Size: 6900 um x 6900 um	18-MAR-2010 12:21:35

Figure B.7. Bonding diagram of the fabricated LNAs on the MPW chip, showing the standard LNA in the top left, the LNA with feedback below that and the separate first and second stages to the right.

In the research carried out toward the derivation of a mathematical model for the proposed LNA configuration, it was necessary to design certain LNAs to verify the model. As such two LNAs have been submitted for fabrication in order to absolutely corroborate the simulated results, and the datasheet below serves as a summary of these particular LNAs which will be used to obtain measured results.

3-14 GHz LNA Data Sheet

A very robust 3-14 GHz wideband LNA implemented with the LC-ladder and capacitive shunt-shunt feedback configuration. Both a standard LNA and one with improved linearity, but slightly poorer noise performance, are available. Two individual testing amplifier stages are also included.

Biasing

The first stage of the LNA uses current biasing and the current should be set using a 400 Ω series resistance to the positive supply.

The second and third stages require voltage biasing for which the active bias circuit in Figure 1 is suggested.

Signal connections

50 Ω input and output signal traces should be connected to the input and output pins through 15 pF DC-blocking capacitors.

Specifications

	Standard	High IIP3
BW	3-14 GHz	3-14 GHz
S_{11}	< -10 dB	< -9.8 dB
S_{21}	20.9 dB	20 dB
NF	1.7-3.3 dB	2.2-3.9 dB
IIP3	-22.6 dBm @ 4.2 GHz	-14.5 dBm @ 4.2 GHz
V_{CC}	1.8 V	1.8 V
I_{C1}	2.5 mA	2.5 mA
I_{C2}	2.7 mA	8 mA
I_{C3}	2.7 mA	8 mA

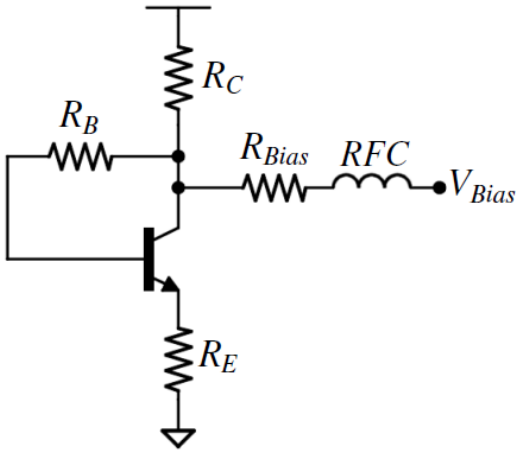


Figure 1. Active bias circuit example.

Pin Diagram

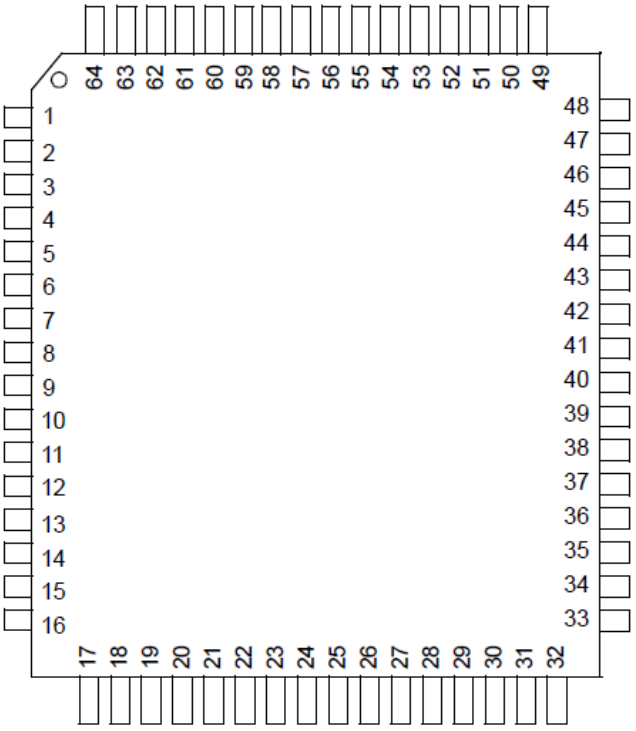


Figure 2. Pin diagram of the 3-14 GHz LNA

Pin	Name	Description
2	Std_Vcc	Standard LNA 1.8 V supply
1	Std_Gnd	Standard LNA ground
63	Std_Bias1	Standard LNA stage 1 current bias (400 Ω R to supply)
60	Std_Bias2	Standard LNA stage 2 voltage bias
3	Std_Bias3	Standard LNA stage 3 voltage bias
62	Std_In	Standard LNA RF input from 50 Ω source with15 pF DC-blocking capacitor
61	Std_Out	Standard LNA RF output to 50 Ω load with15 pF DC-blocking capacitor
9	Lin_Vcc	Linear LNA 1.8 V supply
8	Lin_Gnd	Linear LNA ground
7	Lin_Bias1	Linear LNA stage 1 current bias (400 Ω R to supply)
4	Lin_Bias2	Linear LNA stage 2 voltage bias
10	Lin_Bias3	Linear LNA stage 3 voltage bias

6	Lin_In	Linear LNA RF input from 50 Ω source with15 pF DC-blocking capacitor
5	Lin_Out	Linear LNA RF output to 50 Ω load with15 pF DC-blocking capacitor
59	S1_Vcc	Testing stage 1 LNA 1.8 V supply
56	S1_Gnd	Testing stage 1 LNA ground
57	S1_Bias1	Testing stage 1 current bias (400 Ω R to supply)
55	S1_In	Testing stage 1 LNA RF input from 50 Ω source with 15 pF DC-blocking capacitor
58	S1_Out	Testing stage 1 LNA RF output to 50 Ω load (on-chip blocking capacitor)
54	S2_Vcc	Testing stage 2 LNA 1.8 V supply
53	S2_Gnd	Testing stage 2 LNA ground
50	S2_Bias1	Testing stage 2 current bias (400 Ω R to supply)
51	S2_In	Testing stage 2 LNA RF input from 50 Ω source with (on-chip blocking capacitor)
52	S2_Out	Testing stage 2 LNA RF output to 50 Ω load (on-chip blocking capacitor)

Pins not referred above were used for prototyping by other parties/students (MPW).