## 7.1   INTRODUCTION

The fabricated chip and test PCB described in Chapter 6 were used to measure the performance of the LNAs. The measurement equipment and test procedures are described in this chapter. The experimental results are also given and compared to the expected results obtained from the simulations. The forward gain and input reflection as well as the noise figure of the LNAs were measured. The P_{1dB} compression point was also derived from the gain measurements.

7.2   MEASUREMENT EQUIPMENT AND TEST PROCEDURE

The S-parameters were measured using a Rohde & Schwarz ZVA40 Vector Network Analyzer capable of measuring 2 port networks up to 40 GHz. A photo of this analyzer is shown in Figure 7.1. A frequency range from 10 MHz to 20 GHz was used during the measurements.
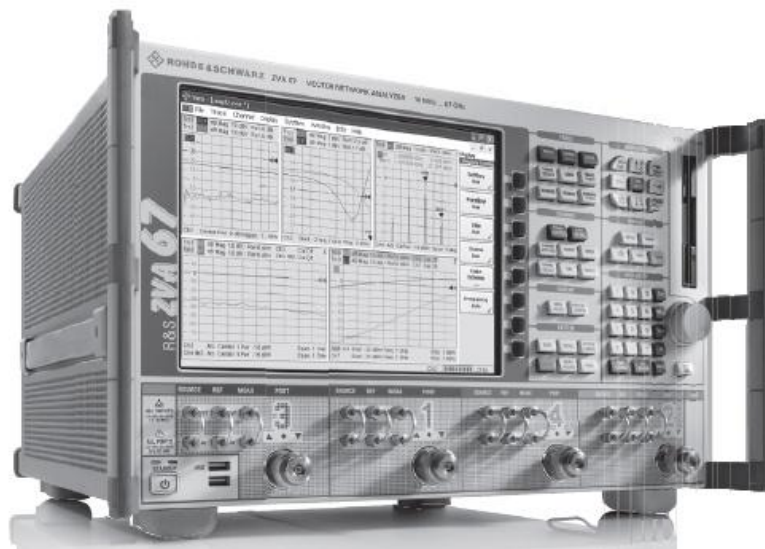

Figure 7.1. Photo of the Rohde & Schwarz ZVA40 Vector Network Analyzer [71]**.**

To compensate for the losses in the PCB and the bond wire inductance of the IC package the S_{21} of a calibration path, made by connecting two bond pads together on the chip, was measured first. The loss in this path was subtracted from the S_{21} measurements of the LNA in order to de-embed the LNA itself from the PCB and package parasitics.

To obtain the P_{1dB} compression point the input power from the network analyzer was increased from -30 dBm by 1 dBm increments until a drop in the S_{21} was observed.

To measure noise figure an Agilent E4440A PSA spectrum analyser was used. It has a frequency range from 3 Hz to 26.5 GHz. A photo of the spectrum analyser is shown in Figure 7.2. A 20 dB excess noise ratio (ENR) Agilent 346B noise source was used to generate a noise floor above the minimum detectable noise level.
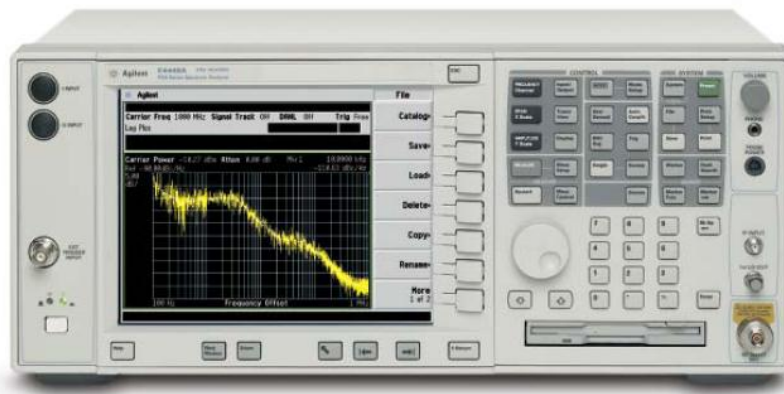

Figure 7.2. Photo of the Agilent E4440A PSA high performance spectrum analyser [72].

The frequency range for the measurements was set to 1 to 9 GHz which is the range over which reliable gain was obtained and the noise source ENR values were available. The *Y*-factor NF measurement and calculation method was used [**73**]. The noise source was first connected in series with the spectrum analyzer noise source control output and the RF input as shown in Figure 7.3. Taking measurements with the noise source turned on and off provided the reference noise power levels.
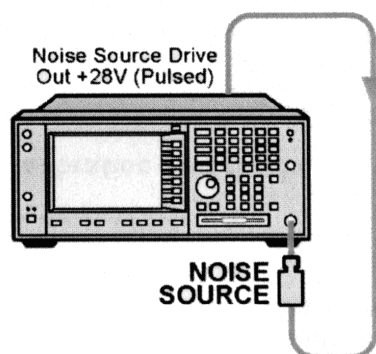
Figure 7.3. Calibration of the Agilent E4440A PSA with a noise source [74].

The LNA was then placed in series with the noise source as shown in Figure 7.4 and the noise power levels with the noise source turned on and off recorded. This provided all the data necessary for the *Y*-factor NF calculations [73] which were done in MATLAB. The noise figure was measured at room temperature and not at 290 °K as specified in the definition of noise figure [1].
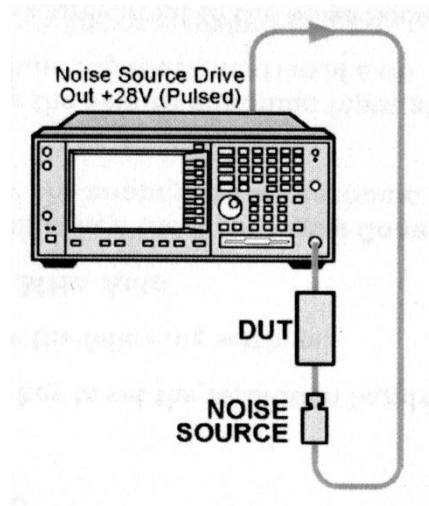

Figure 7.4. Connection of the device under test (DUT) to make NF and gain measurements [74].

Since only a single prototype was tested the results do not include all potential variations present in a large production run. The results are however sufficient to prove the concept and the capabilities of this LNA configuration.

7.3   MEASURED *S*-PARAMETERS

A plot of the calibration path S_{21} versus frequency is shown in Figure 7.5. Above 3 GHz there are significant spikes in the response due to the effects of the parasitic inductance in the last part of the PCB tracks as well as the bond wire inductance, and possibly also the parasitic capacitance of the IC package and PCB. Although the losses in the calibration path can be subtracted from the LNA S_{21} measurements to compensate, the harmonic spikes would not be at the exact same frequencies due to for example different track lengths. This means that some smoothing of the measured results could give a better indication of the response that would be measured on a naked die. A 5-point moving average smoothing function was used in MATLAB as discussed in the sections that follow.

The use of a smoothing function introduces the possibility of two major errors though. First, the smoothness of the curve could be too optimistic if overcompensated. Second, the function could result in a total average gain which is lower than the actual LNA gain which would have been obtained without the package parasitics. These factors should be kept in mind when interpreting the results.
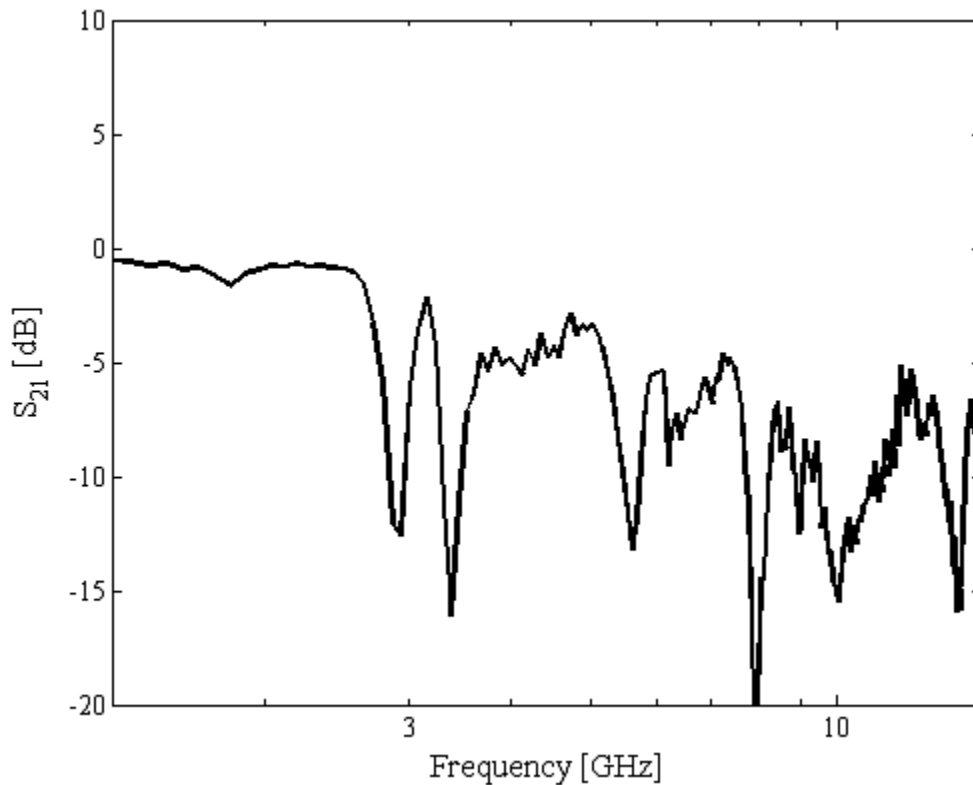
Figure 7.5. Calibration path S_{21} measurement

After de-embedding and smoothing of the measured results the shape of the *S*-parameter curves of both the standard and linearity optimized LNAs were similar to the simulated curves. Interestingly the linearity optimized version were a much closer match than the standard version though, as shown in the following plots. Since the designed collector currents of the standard LNA were low values the currents were adjusted to improve the gain of the LNA, although this had a detrimental effect on the S_{11}. The alternative current values are given in Table 7.1 and the effects on the *S*-parameters are shown in Figure 7.6 to Figure 7.8.

Table 7.1Table 7.1. Modified collector current values of the standard LNA to improve the gain.

| Current	Original value	Adjusted value
I_{C2}	2.7 mA	3.6 mA
I_{C3}	2.7 mA	4.7 mA

7.3.1   Standard LNA

Figure 7.6 shows the measured S_{21} of the standard LC-ladder and capacitive shunt-shunt feedback LNA before and after the calibration path was subtracted for both the original and adjusted collector currents.

The comparison of the de-embedded plots after application of a moving average smoothing function is shown in Figure 7.7. The difference in the S_{11} can be seen in Figure 7.8. A comparison of smoothed S_{11} curves shows an average worsening 2 dB above 4 GHz. From the plots in Figure 7.7 the gain has been improved by about 5 dB over the entire band of interest up to 10 GHz where the parasitics cause a rapid cut-off of the gain.
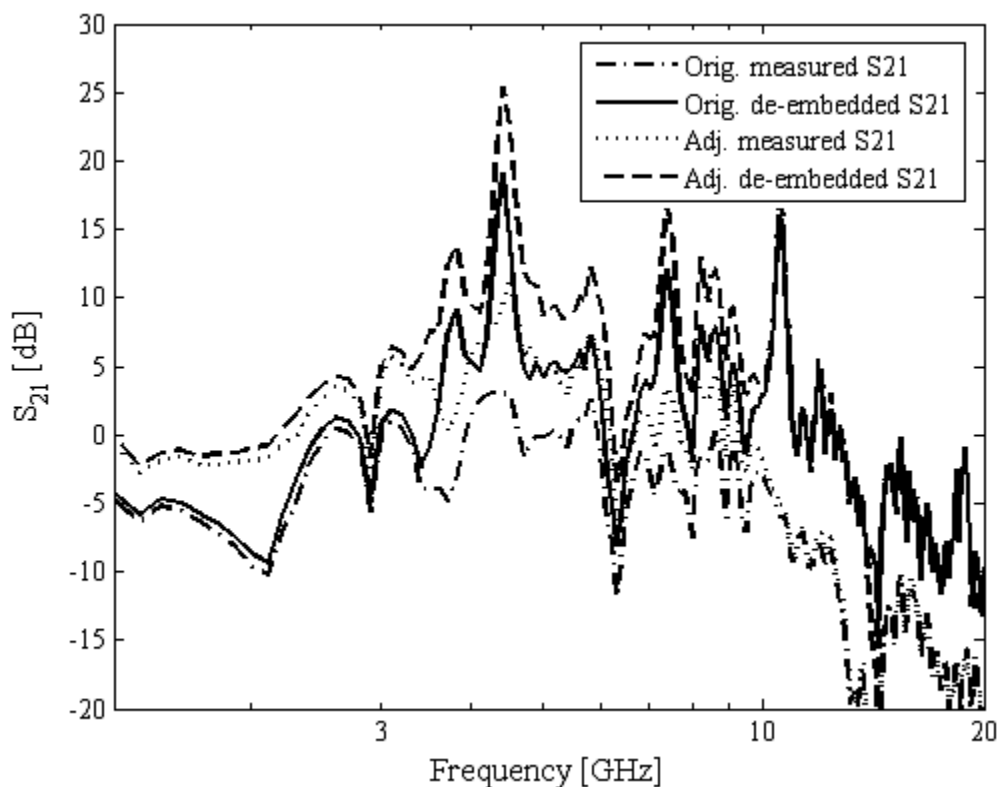
Figure 7.6. Measured S_{21} of the standard LNA before and after subtraction of the calibration path for the original and adjusted collector currents.
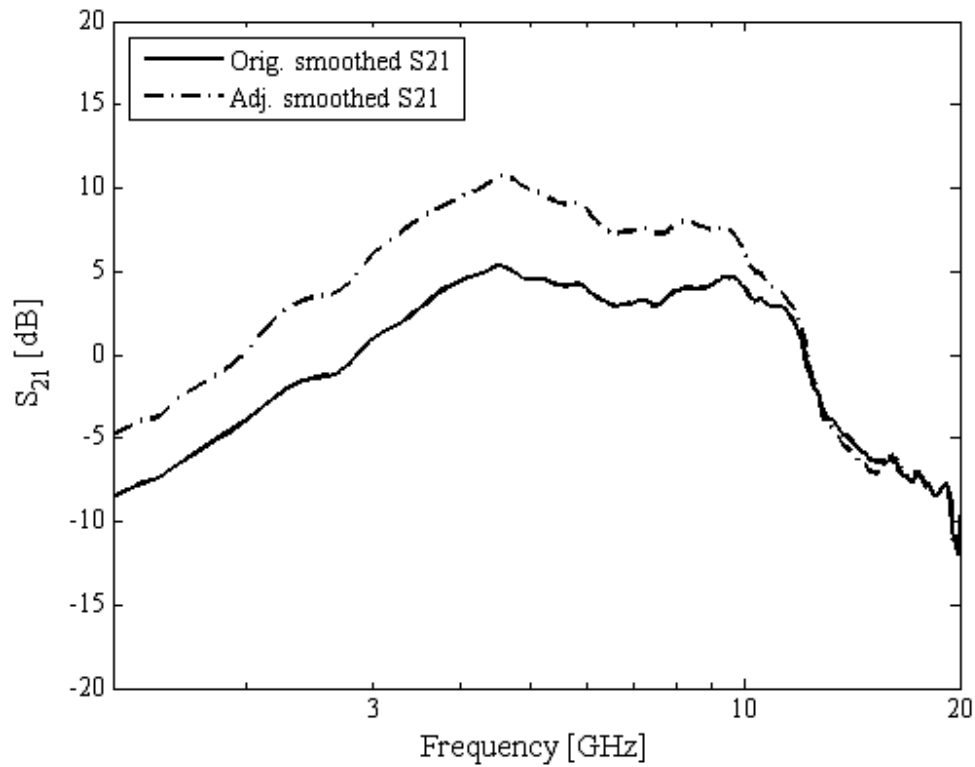
Figure 7.7. Comparison of the de-embedded and smoothed S_{21} of the standard LNA with the original and adjusted collector currents.
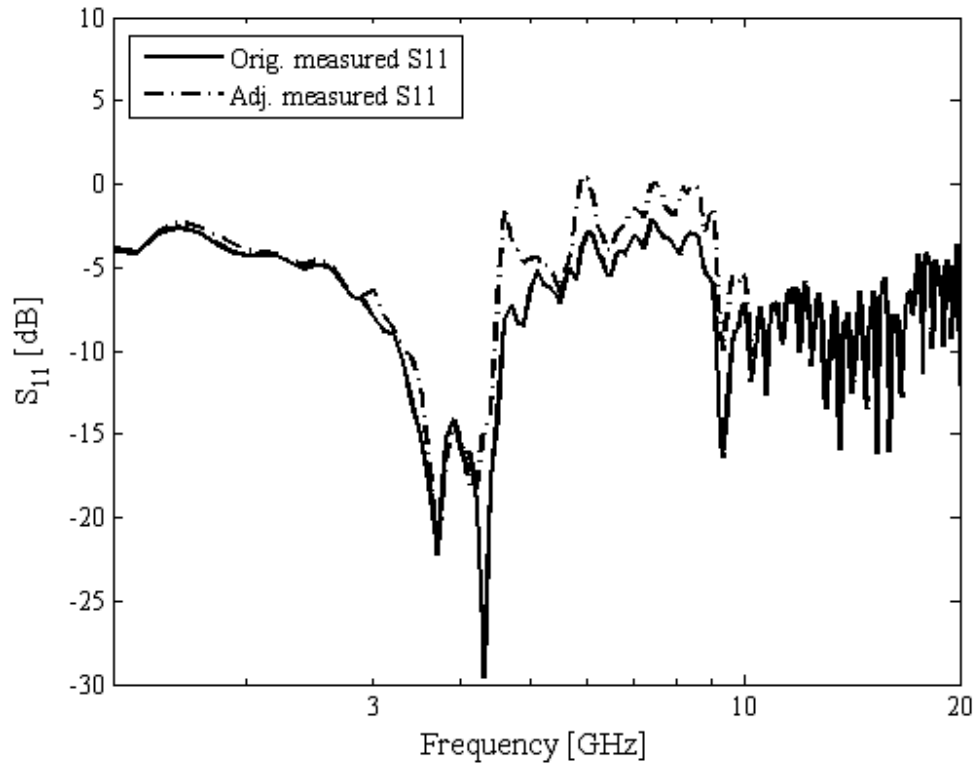
Figure 7.8. Measured S_{11} of the standard LNA with original and adjusted collector current.

In Figure 7.9 the smoothed S_{11} and S_{21} of the standard version of the LNA are compared to the simulated responses given in Section 6.5. The measured mid-band gain is 8 dB which is 12 dB lower than the expected simulated gain; the lower -3 dB cut-off frequency is at 3 GHz as expected though. The S_{11} is worse than expected by 2 dB below 4 GHz, and up to 5 dB above.
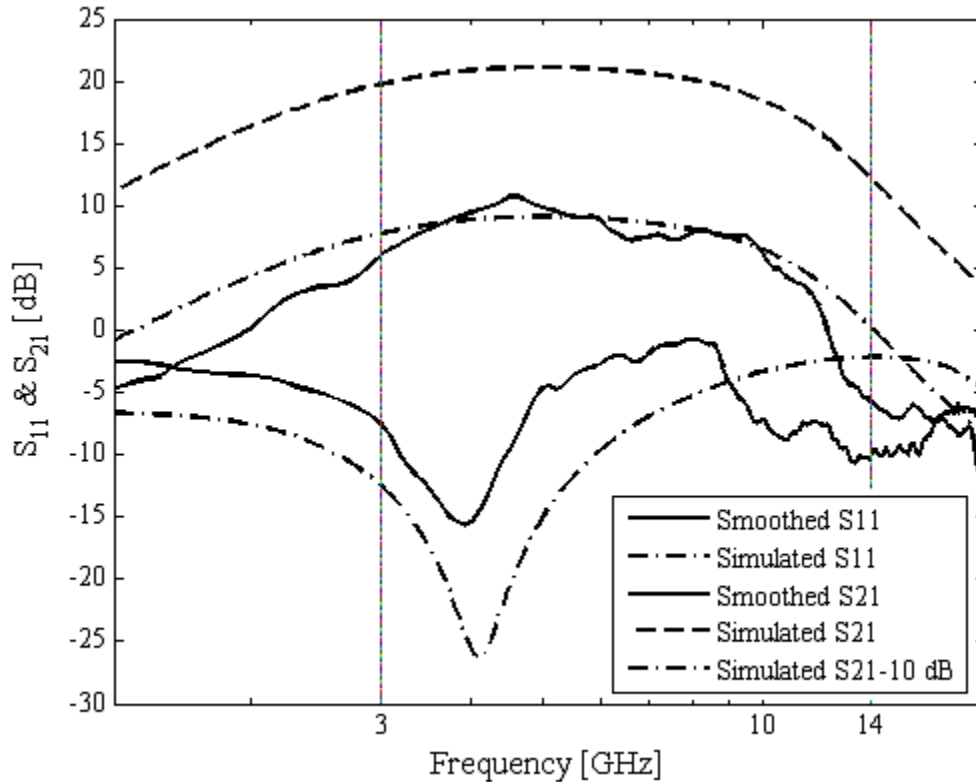

Figure 7.9. Smoothed S_{11} and S_{21} of the standard LNA with adjusted currents compared to the simulated result from Section 6.5.

7.3.2   LNA optimized for linearity

The measured and de-embedded S_{21} of the LNA optimized for linearity is shown in Figure 7.10, and the smoothed de-embedded version in Figure 7.11. The measured and smoothed S_{11} of this LNA is given in Figure 7.12.

The comparison of the smoothed results to the simulated results from section 6.5 is shown in Figure 7.13. In contrast to the response of the standard version of the LNA the measured S_{11} of the linearity optimized LNA tracks the simulated response very well. It dips below -10 dB just above 3 GHz, and then goes above -10 dB again at 6 GHz. This is the expected response due to the package parasitics though as predicted by the simulations.
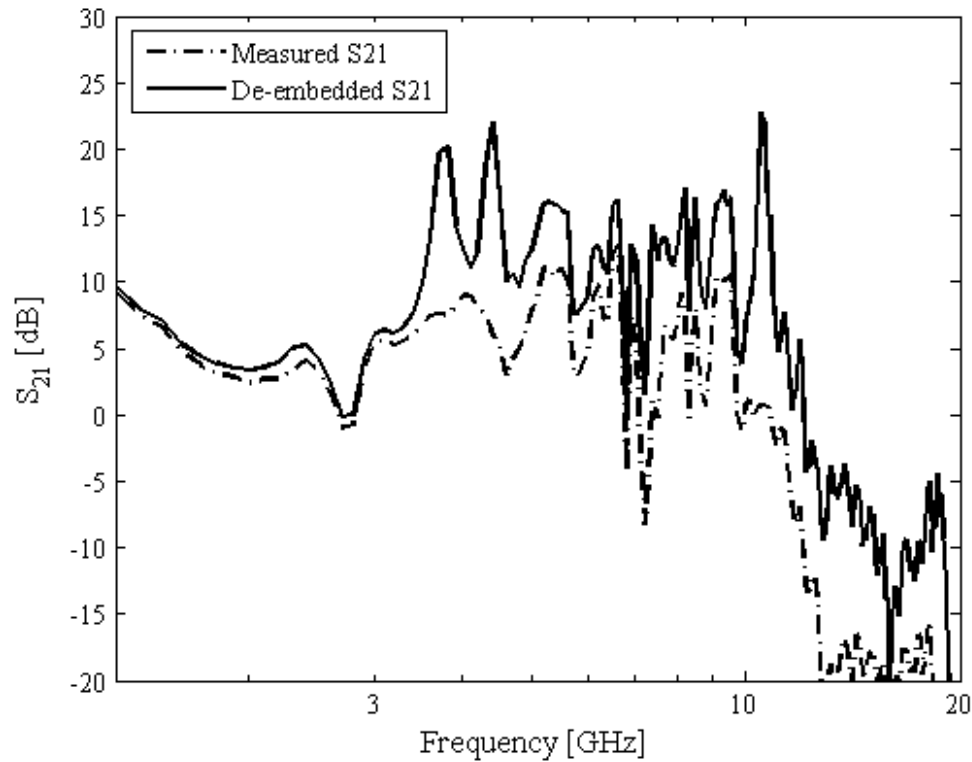
Figure 7.10. Measured S_{21} of the LNA optimized for linearity before and after subtraction of the calibration path.
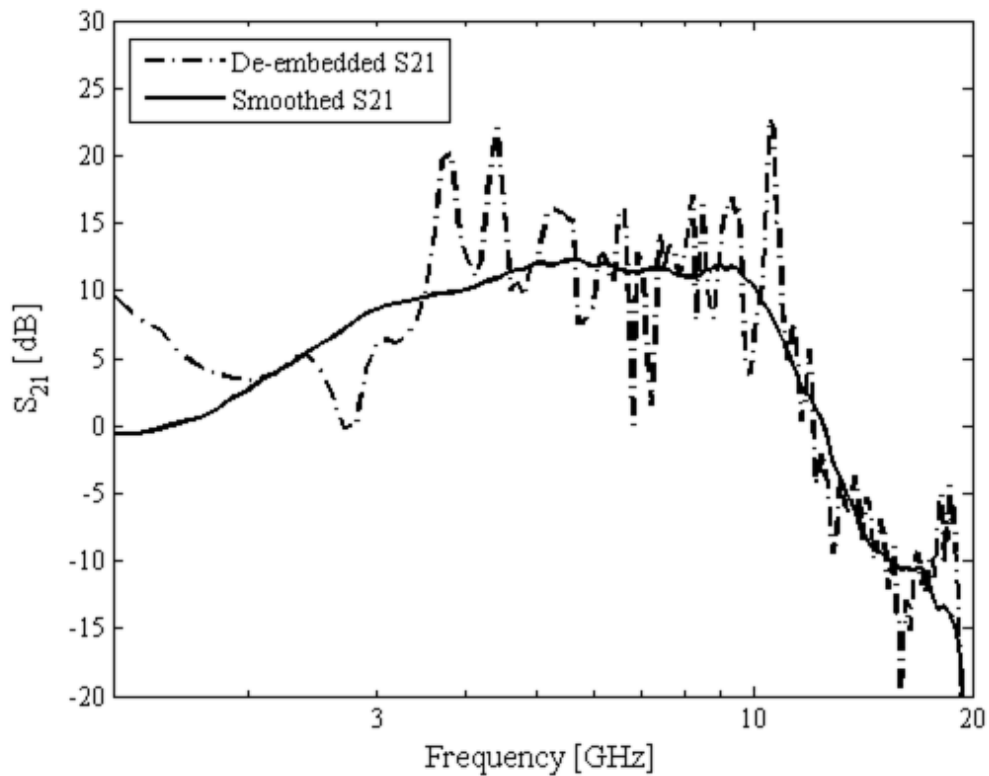
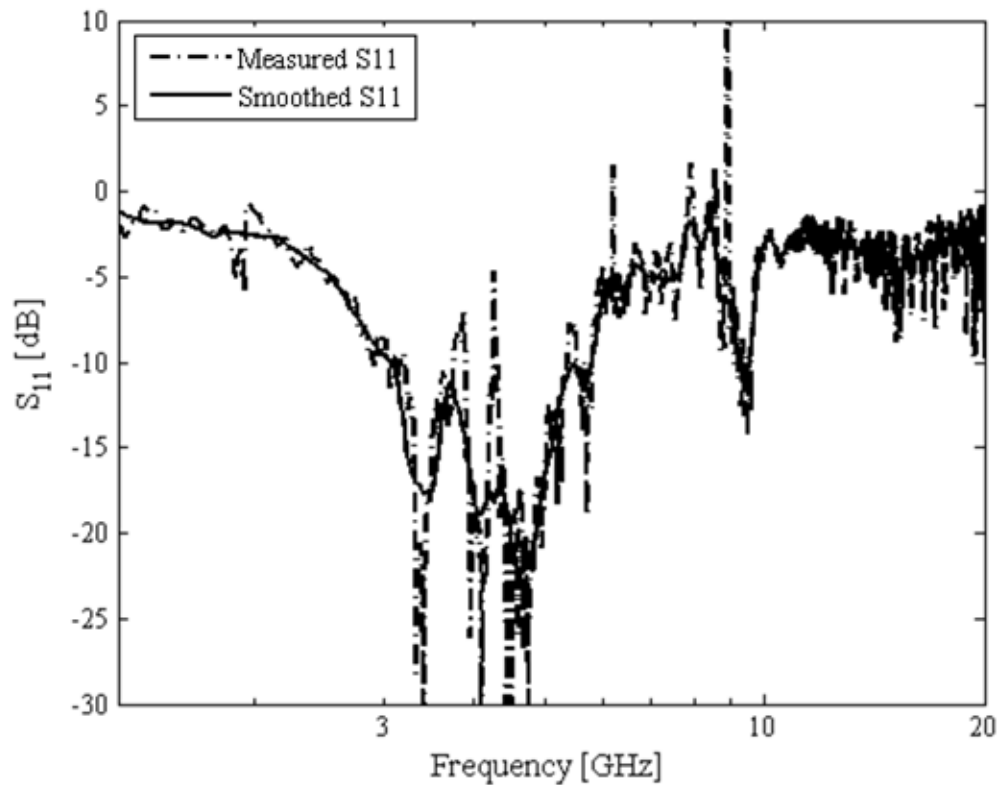**Figure 7.11. De-embedded S_{21} of the LNA optimized for linearity before and after smoothing with a moving average algorithm.**

Figure 7.12. Measured S_{11} of the LNA optimized for linearity before and after smoothing with a moving average algorithm.

Although the measured gain of 10 dB is 10 dB lower than expected the shape of the plot closely matches that of the simulated S_{21} and shows the lower cut-off frequency at 3 GHz as designed. Above 10 GHz the measured cut-off is still much sharper than simulated though, possibly due to the inductance of the narrow tracks connecting the transmission lines to the IC pins which becomes dominant above this frequency. This effect was not included in the simulation. The only deviation from the expected results is therefore the gain which is 10 dB lower than the designed value, but this could to an extent be due to the smoothing of the curve, and also result from the degradation of the input and output return losses by the package and PCB parasitics.
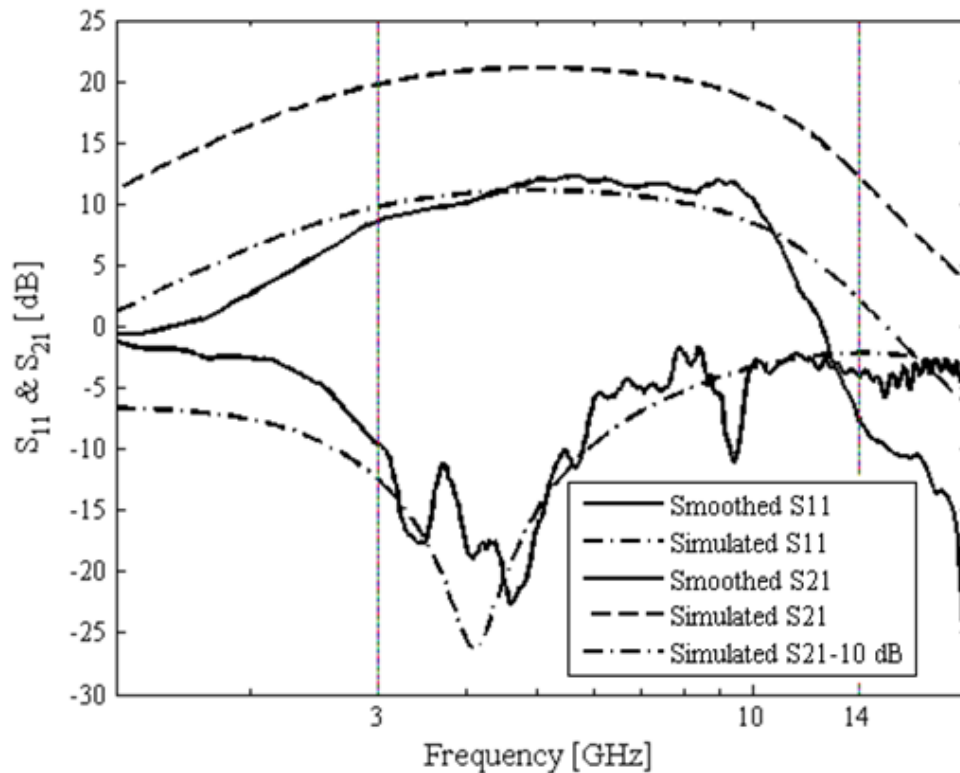
Figure 7.13. Smoothed S_{11} and S_{21} of the LNA optimized for linearity compared to the simulated result from Section 6.5.
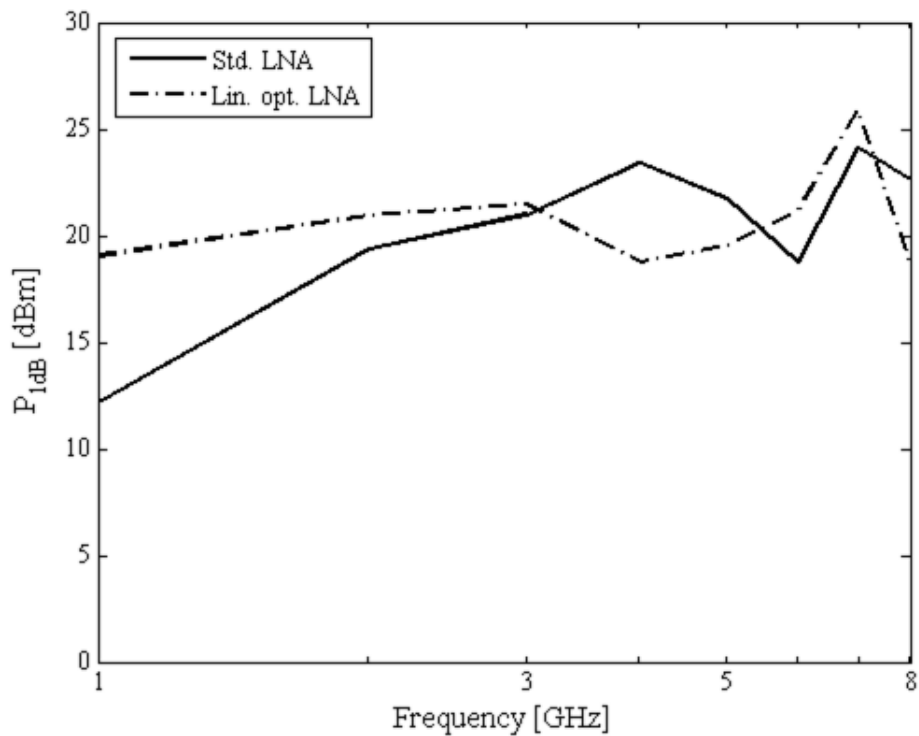
7.4   MEASURED NOISE FIGURE

The measured noise figures of the LNAs are very high. Unfortunately the noise measurements are dependent on the system gain which can of course not be physically de-embedded when doing noise measurements. Therefore the already relatively low gain of the two systems at 10 dB is in fact even less when performing these measurements due to the path loss resulting from the PCB and package parasitics. Such a low gain introduces a large margin of error which means the actual NFs are potentially much lower than the measured values.

In addition the 20 dB ENR noise source only barely resulted in a reference noise level above the noise floor of the spectrum analyzer. This introduced further uncertainty into the measurements. Ideally a pre-amplifier should have been used to raise the reference level higher, however a pre-amp which operates over this frequency range was not available.

The measured noise figures are shown in Figure 7.14. The NF of both LNAs has an average of 20 dB.

Figure 7.14. Measured noise figure of the two LNAs.

7.5   MEASURED P$_{1DB}$ COMPRESSION

To find the P$_{1dB}$ compression point the S_{21} at various input powers were plotted on the graphs shown in Figure 7.15 and Figure 7.16. These plots were visually inspected to find the 1 dB compression at various frequencies. Since the 1 dB compression of the S_{21} response before smoothing varied by large amounts depending on whether the gain at a specific frequency was at the peak of a spike in the response or a valley the smoothed versions of the S_{21} measurements were used to obtain a rough approximation of the actual P$_{1dB}$ compression curve.
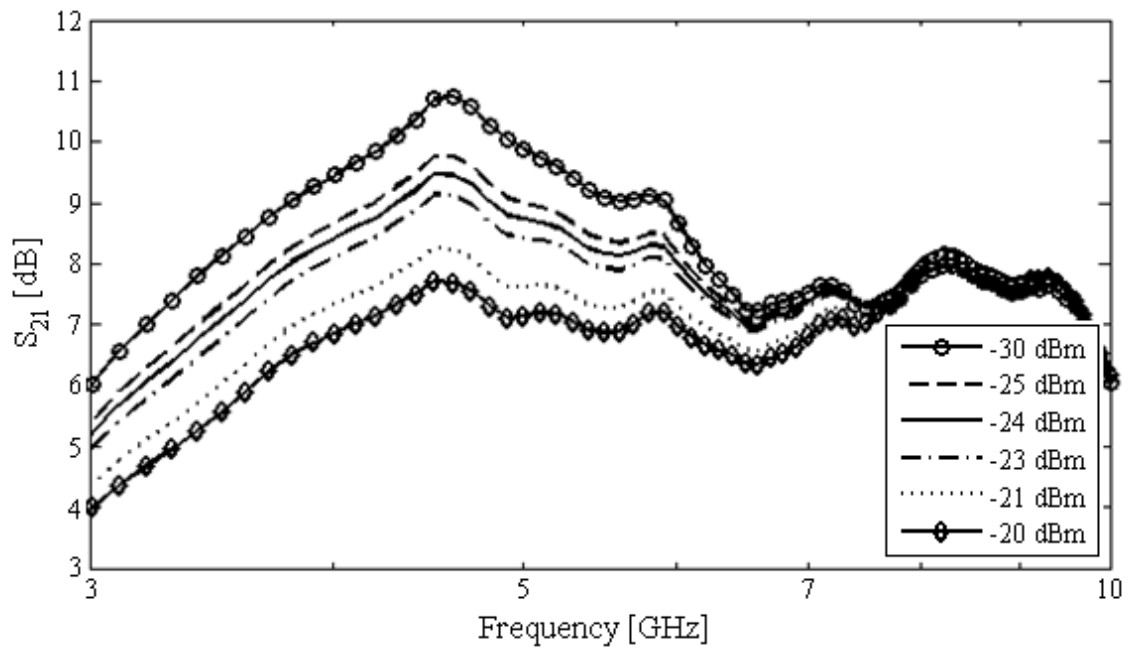
Figure 7.15. Smoothed measured S_{21} of the standard LNA at various input powers.
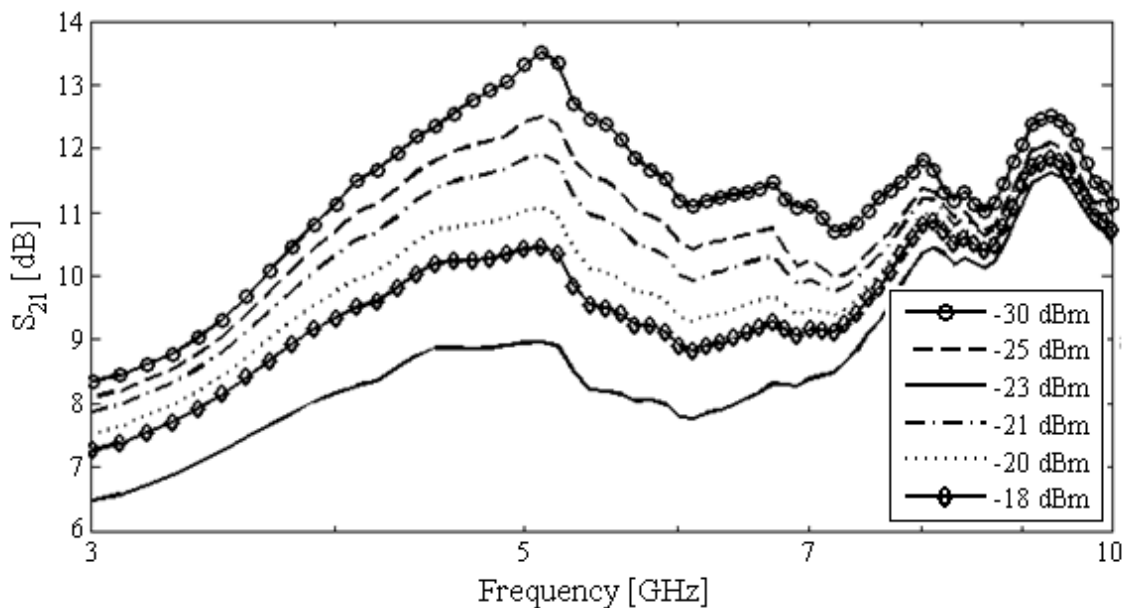
Figure 7.16. Smoothed measured S_{21} of the LNA optimized for linearity at various input powers.

The compression was determined over the 3 GHz to 8 GHz band over which the gains of both LNAs are relatively flat. The P_{1dB} compression curves over this band are plotted in Figure 7.17. Both the standard version and the one optimized for linearity's compression points vary between -20 dBm and -24 dBm with an average of -23 dBm for the standard and -22 dBm for the more linear version.

The more linear LNA clearly has an improved P_{1dB} compression point at the lower frequencies from 3 GHz to 5 GHz. From 5 GHz onwards the performance of the two LNAs becomes very similar; however if taken into account that the linear LNA has a gain of 10 dB compared to a gain of 8 dB for the standard LNA the former is effectively more linear over the entire band with improved P_{1dB}.
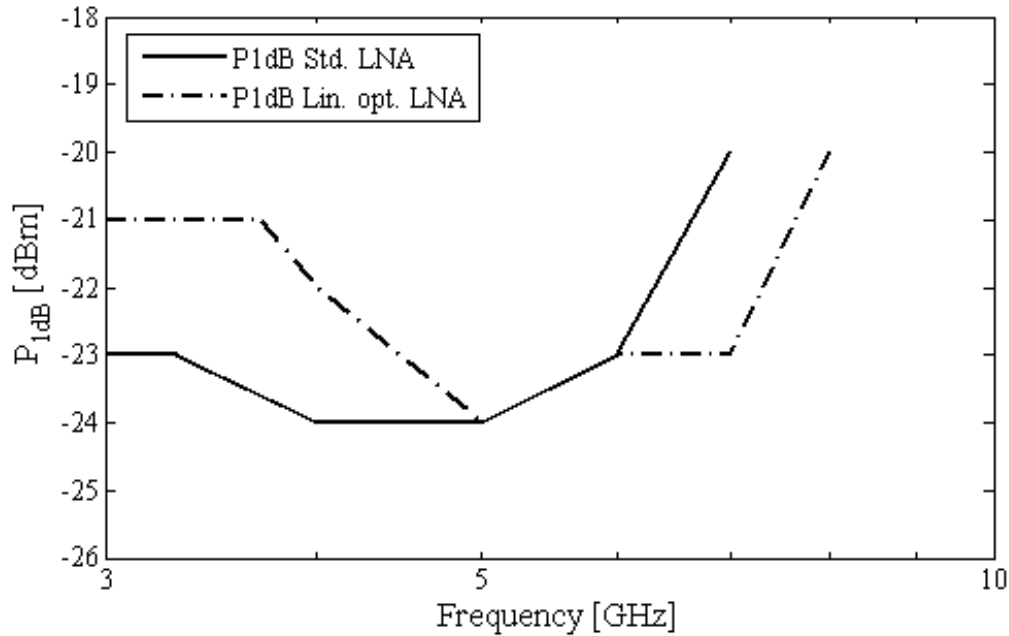
Figure 7.17. P_{1dB} compression curve of the standard and linearity optimized LNAs.

7.6   CONCLUSION

This chapter discussed the measuring equipment and the test procedure used during characterization of the fabricated LNAs. The measured results of both the standard and linearity optimized versions of the LC-ladder and capacitive shunt-shunt feedback LNA were presented.

The measured *S*-parameters compared very well with the simulations where the package parasitic components were included. The measured S_{21} of the standard version of the LNA is 8 dB with an S_{11} 2 dB higher than expected, but still below -10 dB over a reasonable section of the frequency band. The average S_{21} of the linearity optimized version of the LNA was 10 dB, and the S_{11} remained below -10 dB over the entire feasible range predicted by the simulations and showed very good tracking of these simulated results.

The P_{1dB} compression point was between -20 dBm and -24 dBm for both LNAs over the 3 GHz to 8 GHz range. The average compression point of the linear LNA showed a 1 dBm improvement over the standard one at -22 dBm compared to -23 dBm. If the higher gain of the LNA optimized for linearity is also taken into account it is clearly the more linear of the two.

The NF is the only parameter that was not measured with high enough accuracy to provide reliable results due to the low gain of the LNAs and unavailability of a pre-amp to provide an adequately high noise power above the spectrum analyzer noise floor. The average measured NF of both LNAs was 20 dB, but with the above PCB related shortcomings taken into account the actual device NF could be much lower.

Although it was suspected that the emitter degeneration resistors in the linearity optimized version of the LNA would be detrimental to the gain and S_{11} of the LNA it turned out to be the LNA exhibiting improved gain performance. This means that with the added benefit of better linearity this should be the version of choice based on current findings.

Although a complete characterization of the LNA performance was not possible these measured results prove the feasibility of the LC-ladder and capacitive shunt-shunt feedback configuration for the implementation of wideband LNAs and validates it as an area for further research.

This research dealt with the question of whether a combined LC-ladder and capacitive shunt-shunt feedback matching network could be used successfully in wideband LNA implementations, especially with improved performance compared to current LNA implementations in literature.

Through the derivation of a mathematical model and subsequent design and simulation of such a LNA in the IBM 8HP 0.13 µm SiGe BiCMOS process as well as fabrication in the IBM 7WL 0.18 µm process, it was proved that this is indeed an effective means of implementing very wideband LNAs with low NF and power consumption while achieving typical gain and input matching specifications. These results are compared to state-of-the-art LNA performance available in literature in Table 1.1.

A critical evaluation of this research is presented in this chapter along with suggestions for future research on this topic.

8.1   CRITICAL EVALUATION OF THE WORK

In Section 1.2 it was hypothesized that if a fourth order LC-ladder filter can be used to realize input matching over an arbitrary frequency band, and a shunt-shunt capacitive feedback common emitter configuration can be modelled as an equivalent series RC circuit, then a combination of these two circuits can be used as a wideband LNA overcoming certain shortcomings of current LNAs in literature; most notably the pole introduced at the lower corner frequency resulting in the four on-chip inductor requirement of the emitter degenerated LC-ladder configuration, and also the tight coupling between the collector current and the lower corner frequency values.

This hypothesis has been corroborated and the research questions answered through the successful modelling, design, simulation, fabrication and measurement of a LC-ladder and capacitive shunt-shunt feedback LNA.

- The derived mathematical model shows that not only can wideband matching be realized, but also very low noise operation with typical gain performance.

- As shown in Section 4.2.4 the pole at the lower corner frequency found in the emitter degenerated LC-ladder configuration [11] is not present in this topology.

- This configuration does not require an emitter inductor in the first stage due to the capacitive feedback which means only three rather than four on-chip inductors are required. In addition, if the design is done over a smaller frequency range where the first stage gain does not have to be increased beyond the limit set by the GBP, and an increase of the first stage load capacitance would also not be required, the output pole of the first stage will be beyond the operating frequency band and the second stage load inductance could also be exchanged for a resistive load, thereby decreasing the inductor count to two.

- Since the matching is realized using the Miller-capacitance rather than transistor parasitic capacitances there is significant freedom in the selection of collector current which can be used to tune the circuit for optimal performance.

- It is also a wideband configuration and not a narrowband amplifier applied to wideband applications as done with the inductive emitter degeneration or capacitive feedback techniques in other works [12].

The configuration presented here shows improved simulated NF compared to the results found in literature. The power consumption has also been greatly reduced while maintaining the standard LNA S-parameters of $S_{11} < $ -10 dB and $S_{21} = $ 20 dB. Preliminary measured results, although not fully attaining the simulated performance, confirmed the potential of this configuration to achieve good wideband performance when considering the shortcomings of the measurement process. These improvements were made at the cost of linearity, mainly due to the removal of degeneration from the first amplifier stage; however linearity can be improved by trading power consumption while the NF and gain can be kept relatively constant where higher linearity is required as shown in Sections 5.3.5 and 5.5.5.

This research also produced a thorough analysis of existing LNA configurations and input matching techniques, and especially the inductively degenerated common-emitter topology was discussed in great detail as it is one of the most common LNA implementations found in literature. A discussion of the trade-offs between NF, gain and linearity of the techniques was also given.

The largest contribution of this work towards the future implementation of the proposed LNA topology is the derived mathematical model characterizing the configuration. This can be used to both predict the performance the LNA and also includes design equations to facilitate EDA. Preliminary MATLAB code towards the implementation of such EDA software is provided in Appendix A. A process of simultaneously minimizing the NF and improving the gain of the LNA was also deduced from this model and presented; as was the bandwidth versus NF trade-off.

The accuracy of the mathematical model was proved with thorough simulations of two LNA designs using different transistor processes. The sensitivity of the LNA performance with variations in process parameters and temperature was also shown. Although simulated and calculated results showed good correlation, some assumptions were made in the derivation of the model and these are listed below, with some suggestions for future improvement of the model also provided in Section 8.2.

- The simple high frequency small-signal model of the bipolar transistor was used in the derivation. This however proved to be sufficient for first order designs done using this model.

- Inductors were modelled as an inductance and parasitic series resistance which was derived from a Q-factor estimated from data found in the process model guides [56], [58] and assumed to be constant with frequency. Although the simple inductor model proved sufficient the Q-factor has a large influence on both the NF and input matching and as such should be derived from the inductor layout parameters in a frequency dependent form.

- The gain bandwidth product is currently not taken into account by the model and proves problematic when transistors are operated close to their performance limits as shown in Section 5.5.1.

- The correlation between the base- and collector current shot noise is not included in the NF equation; however this only becomes noticeable at very high frequencies where, as shown in Section 5.4, the use of this configuration is not optimal and as such this is an acceptable simplification.

- Only an approximation of the worst case IIP3 has been included in the model.

Since the absence of emitter degeneration in the first amplifier stage leads to poorer linearity of the amplifier a thorough investigation of the non-linear sources in HBTs was performed and suggestions made for the improvement of linearity. The improved IIP3 performance with the use of emitter degeneration in the second and third amplifier stages was also presented.

Finally, the layout of two LNAs implementing the LC-ladder and capacitive shunt-shunt feedback topology, with and without linearity improvement, was shown and have been submitted for fabrication in the IBM 7WL 0.18 μm SiGe BiCMOS process. These devices were measured to obtain experimental results which showed good promise, however the measurement equipment was not optimal for measuring performance at such high frequencies. Most notably the PCB layout and choice of SMA connector type was not appropriate for operation above 2 GHz, and the fact that a pre-amplifier was not available for noise measurements resulted in large uncertainty.

8.2   SUGGESTIONS FOR FUTURE WORK

Suggestions for the improvement and expansion of the mathematical model derived in this work for future research are given in the list below.

- Although *S*-parameters and NF equations were derived from the small-signal circuit of the amplifier using first principles only a rough approximation of the IIP3 was used. The model could be expanded to include a more accurate representation of the linearity using a Volterra series. This would also make it possible to isolate the various sources of non-linearity in the LNA [35] to analytically determine the dominant sources so subsequent optimization processes can focus on those non-linear sources (similar to the noise optimization done in this work).
- The effect of the GBP due to the finite f_T of the transistors should be added to the gain equations. It should be possible to maintain a relatively simple model if the f_T is calculated as a function of g_m and the parasitic components.
- Although it was pointed out that neglecting the base- and collector current noise correlation at the frequencies where this configuration is effective, including that could be useful in making the model more robust.
- Following the same RF analogue approach used in this research to derive similar equations for the performance measures of other LNA topologies would allow a

direct comparison of the performance of different topologies based on the specifications for a given application. This could then be used to choose the optimal configuration. Two configurations suggested for such a comparison would be the inductive emitter degeneration [**9**] and emitter degenerated LC-ladder topologies [**11**].

- The sensitivity of the simulated performance of this LNA to variations in transistor model parameters, as well as performance sensitivity to temperature and process variations can also be investigated as a possible figure of merit when comparing it to other LNA configurations in the selection of a LNA for a specific system. Furthermore such data could indicate which parameters of a given transistor model are most essential to extract with high accuracy. These variations as well as the results obtained for the reference case when simulated with the HICUM, VBIC and Mextram transistor models could then be compared.

- As mentioned in Section 8.1 the use of accurate inductor Q-factor values is imperative for achieving calculated results that correlate with the actual circuit performance. Inductor modelling software that could be used to determine the frequency dependent Q-factor based on inductor layout parameters is available in literature [**49**] and should be included in the model and any EDA implementation.

- The inductor modelling software referenced in the previous point forms part of EDA software for class-E and class-F power amplifiers. If such software could be combined with the LNA design automation presented in this work a complete RF amplifier EDA software package could be obtained.

- As pointed out in Section 2.8, passive inductors can be traded with active inductors to reduce the physical size of the circuit. In this case a reduction of approximately 18.4 % can be obtained by replacing the second stage load inductor. Thus the investigation into practical active inductor circuits presented in the literature study could be extended and the feasibility of a LNA employing such an active load investigated.

Improved characterization of the fabricated LNAs should be done with a redesigned test PCB adhering to the suggestions made in Section 6.7. In a future production run LNAs with on-chip input and output DC-blocking capacitors should also be fabricated and tested. Performing on-chip measurements would provide the most accurate characterization of a LNA.

Other bias options should also be investigated such as using the same voltage biasing technique used in stages two and three for the first stage of the LNA. The inductor L_1 could still be used as an on-chip RF choke in such a case. Ideally four different power supplies should also be used, one for the biasing circuit, and a separate supply for the V_{CC} of each stage. This will allow verification of each collector current during the operation of the LNA. With the current PCB design the collector currents could be set individually, but there was no way of measuring the extent to which the stages operating simultaneously affected the current of individual stages. It is believed that this did take place since the overall collector current during operation did not always match the sum of the individual collector currents that were set.