CHAPTER 5: SIMULATION RESULTS

5.1 INTRODUCTION

In order to verify the mathematical derivations in Chapter 4, as well as optimizing the design of a LNA for operation over the 1 GHz to 18 GHz range the configuration was simulated using Spectre RF with the HIT-kits provided by IBM. The required specifications are provided in this chapter and then a design in the IBM 8HP SiGe BiCMOS process is simulated to verify the expected results. Various attempts to improve the linearity of the LNA are also discussed and simulation results given.

To also test the feasibility of the configuration for use at mm-wave frequencies, an implementation for 57 GHz to 64 GHz is simulated. It was however found that the first order design done using the equations in Chapter 4 does not predict results accurately as expected from the discussion in Sections 4.9 and 4.10.

The 8HP process is preferable for this implementation, having a f_T of 200 GHz which is ten times larger than the desired f_H. However, due to the availability of a free IBM 7WL run provided by MOSIS through the MOSIS educational program[5] (MEP), this process was used for fabrication instead, and offers an f_T of only 60 GHz. The free run is a grant obtained through the acceptance of the research proposal for this work by MOSIS. The simulation results of the design using this process are also shown and discussed, and would be expected to repeat in the measured results of the implemented LNA.

The schematic entry, simulations and layout (discussed in Chapter 6) were done using Cadence Virtuoso v5.1.41[6]. Details on the packages that were used are provided in Table 5.1.

Small-signal simulations were used to find the input return loss, forward gain and NF of the LNA. Monte Carlo analyses and a temperature sweep were performed to find the sensitivity of the performance measures to parameter and temperature changes. Large signal analysis was used to find the noise floor and for determining the IIP3 and P_{1dB} of the LNA.

[5] http://www.mosis.com/products/mep/mep-about.html
[6] www.cadence.com

Table 5.1. Packages that were used form the Cadence Virtuoso Software Suite and their functionality.

Package name	Functionality
Virtuoso Schematic Editor	Graphical user interface for schematic entry
Analog Design Environment (ADE), and Spectre RF v5.10.41.072908	ADE is a graphical user interface that can be used to compile the simulator input file for various IC simulators, such as Spectre RF which is capable of AMS simulation.
Virtuoso Layout Editor	Graphical user interface for drawing circuit layouts
Assura	Design rule check (DRC) Layout versus schematic check (LVS)

The VBIC transistor model used in the simulations as well as other important considerations regarding the 8HP/7WL process simulations have been discussed in Sections 3.2 and 3.7. Simulations were done with temperature specified at 27 °C which is frequently assumed as room temperature. All simulations were done using parameterized cells which include all device parasitics, and as such only the interconnect capacitances were neglected.

5.2 CIRCUIT SCHEMATIC AND SPECIFICATIONS OF THE DESIGN

To show the feasibility of the configuration a wideband LNA operating from 1 GHz to 18 GHz was implemented. The LNA will be used in a multi-channel environment where switching between various 800 MHz channels is required. Therefore minimizing the overhead of the demodulation stages would require good input matching, a constant gain as well as low NF over the entire frequency band. It is also important to have a high (and preferably constant) P_{1dB} point over the entire band of operation. The specifications given in Table 5.2 were defined, and the final complete circuit schematic is shown in Figure 5.1.

Although the cascode configuration is commonly used in RF amplifiers, the feedback capacitance C_F introduced between the input and output of the first stage negates most of the advantages obtained from the fact that the cascode configuration serves to decouple the input and output. Therefore the simple common emitter configuration was used. The cascode configuration could have been used for latter stages though, but simulations did

not show any marked improvement and the extra transistor would have merely reduced an already small voltage over the load even further.

Table 5.2. Desired LNA specifications for implementation.

	Specification
Bandwidth	1 GHz to 18 GHz
Gain	18-22 dB
NF	< 4 dB
P_{1dB}	-10 dBm

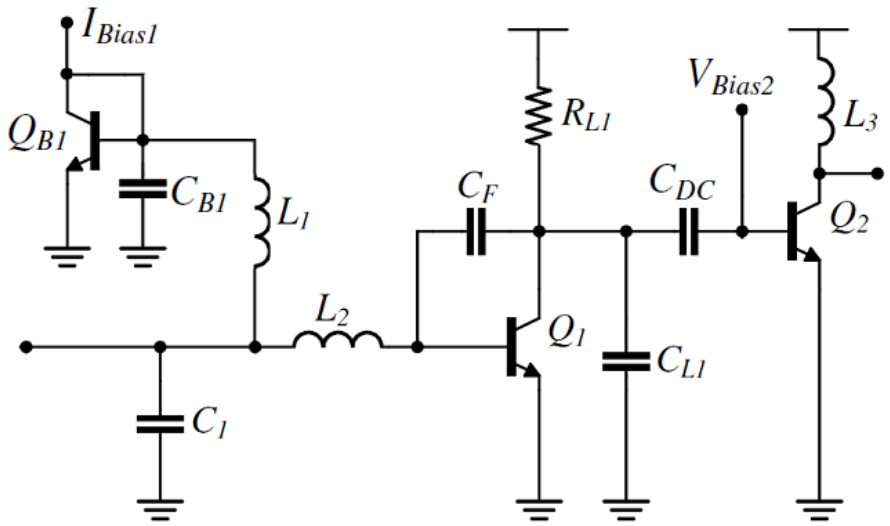

Figure 5.1. Complete schematic of a LNA designed for operation from 1 to 18 GHz.

5.2.1 Transistor biasing

Biasing techniques were kept as simple as possible to allow easy adjustment of the bias currents during experimental testing. The first stage bias network is shown in Figure 5.1. Since inductor L_1 can also act as the bias choke, the biasing of this stage could be done on-chip. A simple current mirror was used to generate the correct V_{BE} for Q_1. An off-chip resistor will be used to bias the current mirror which allows for adjusting the bias current.

Unfortunately the second amplifier stage requires an off-chip bias choke. Although relatively large inductors are available in this process the Q-factor at high frequencies are very low and thus the signal is attenuated when on-chip biasing is attempted. The active bias circuit suggested in [**65**] shown in Figure 5.2 will be used.

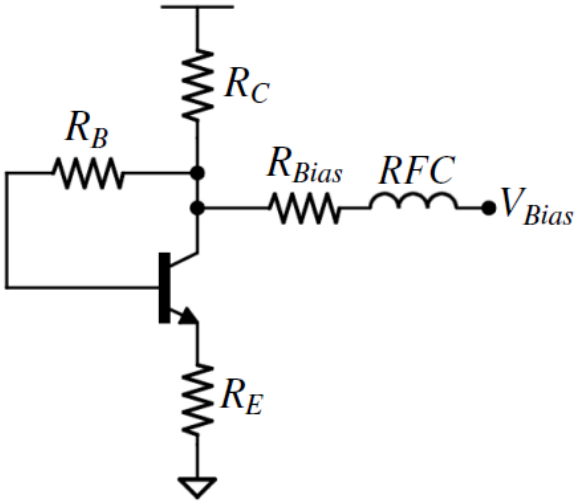

Figure 5.2. Off-chip active bias network [65].

5.3 8HP DESIGN FOR 1-18 GHZ

5.3.1 Initial design

The design process described in Chapter 4 was used in the initial design of a LNA over the 1 GHz to 18 GHz band using the 0.13 µm IBM 8HP BiCMOS process. Using the design equations in Section 4.4 the component values in

Table 5.3 were derived with transistor emitter lengths of 12 µm and a power supply of 1.5 V. Both the calculated and simulated *S*-parameter and NF results for this design are shown Figure 5.3 and Figure 5.4 respectively. A small-signal *S*-parameter analysis was performed in Spectre RF to find the S_{11} and S_{21} frequency response, as well as the NF. The calculated *S*-parameters track the simulations very well, and the deviation of the calculated NF is deemed acceptable. The spike in the response at 16 GHz is due to the self resonant frequency of the large L_1 inductor.

The noise contributions of the various noise sources of this LNA are plotted in Figure 5.5 and shows the very large contribution of the common-emitter voltage noise as a result of the large C_F. It is also apparent that none of the specifications are met by this initial design.

Table 5.3. Initial component values derived using the design equations.

Symbol	Value
C_1	177 fF
C_F	266 fF
L_1	7.96 nH
L_2	442 pH
L_3	1 nH
R_{L1}	417 Ω
I_{C1}	0.6 mA
I_{C2}	5 mA

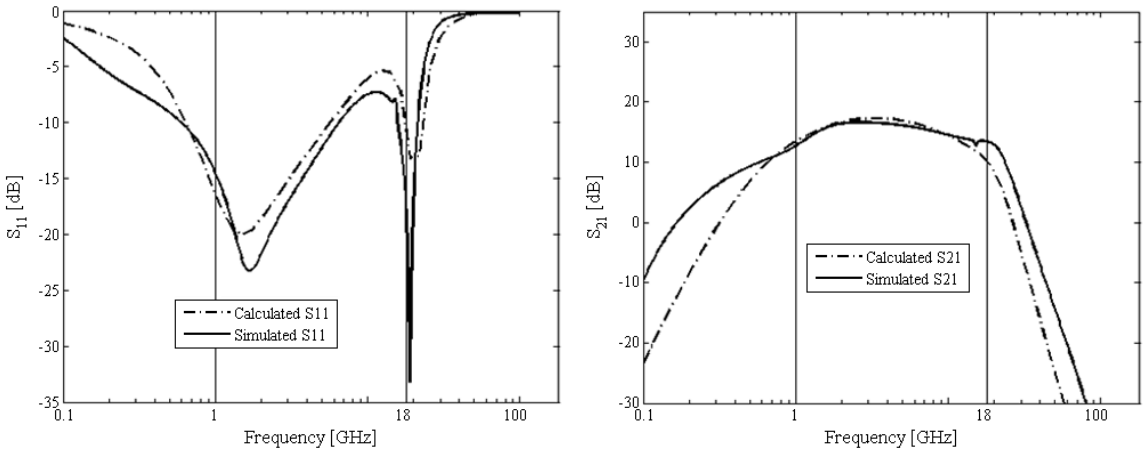

Figure 5.3. Calculated and simulated *S*-parameters without any optimization.

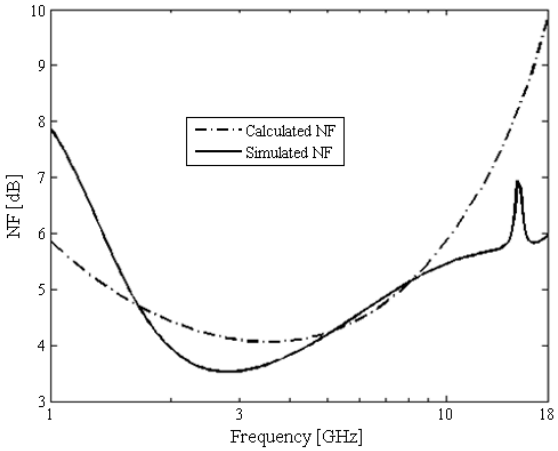

Figure 5.4. Calculated and simulated NF without any optimization.

5.3.2 Noise optimization

Assuming that noise optimization of the collector current and passive components would provide a 2 dB NF improvement a maximum NF of 6 dB was used in equation (4.56) and it was found that a low frequency first stage gain of 30 is necessary to meet the bandwidth versus NF requirement. Once the first stage gain is increased the noise contributions shown in the plot on the right of Figure 5.5 result. A large reduction in CE noise voltage is observed since the value of C_F has now been reduced to 92 fF.

As discussed in Section 4.7.1 the collector current can be increased to reduce the noise. This was done while keeping the voltage gain constant at thirty by simultaneously changing the value of R_{L1}. To improve the input matching after increasing the collector current it was also necessary to add a 150 fF load capacitor to the output of the first stage. The resulting noise contributions are shown in Figure 5.6 on the left and the calculated and simulated NF on the right. With the steps taken thus far the NF has already been improved by 3.5 dB at the lower corner frequency and by more than 2 dB at the upper corner.

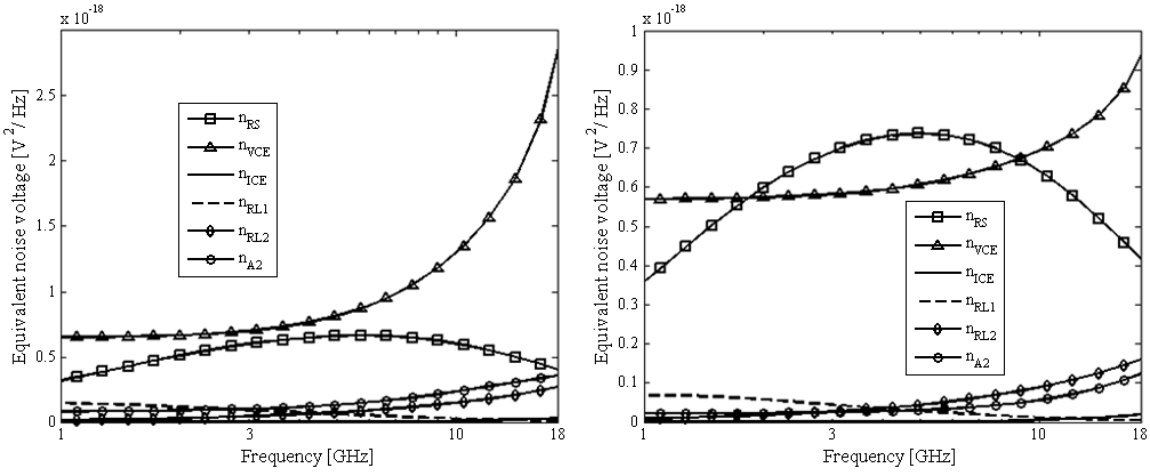

Figure 5.5. Noise contribution of the various noise sources before any optimization (left) and after increasing the first stage gain to 30 (right).

Following the above, the passive component values of the input matching network were also optimized based on the discussion in Section 4.7.1. The noise optimized values are shown in Table 5.4, and the final noise contributions are plotted in Figure 5.7. This optimization has increased the high frequency CE noise voltage contribution slightly, but has also resulted in a larger increase in the gain of the source resistor noise through the input matching network which also implies a larger gain of the input signal, and as such

improves the NF. The final NF and *S*-parameters of the design after noise optimization are shown in Figure 5.8 through Figure 5.10. A final NF improvement of 4.4 dB at the lower corner, 1.3 dB in the mid-band and 2.35 dB at the upper corner frequency can be observed compared to the initial NF in Figure 5.4. Good tracking between mathematical and simulation results are again observed confirming the accuracy of the mathematical model.

The sharp deviations in both the *S*-parameter responses and NF around 10 GHz are due to the self-resonance of inductor L_1. Since L_1 is used to set the lower corner frequency its capacitive response at very high frequencies does not have a large impact on matching, the fluctuations are however undesirable and thus a smaller inductance value should be used whenever possible to increase the self-resonant frequency.

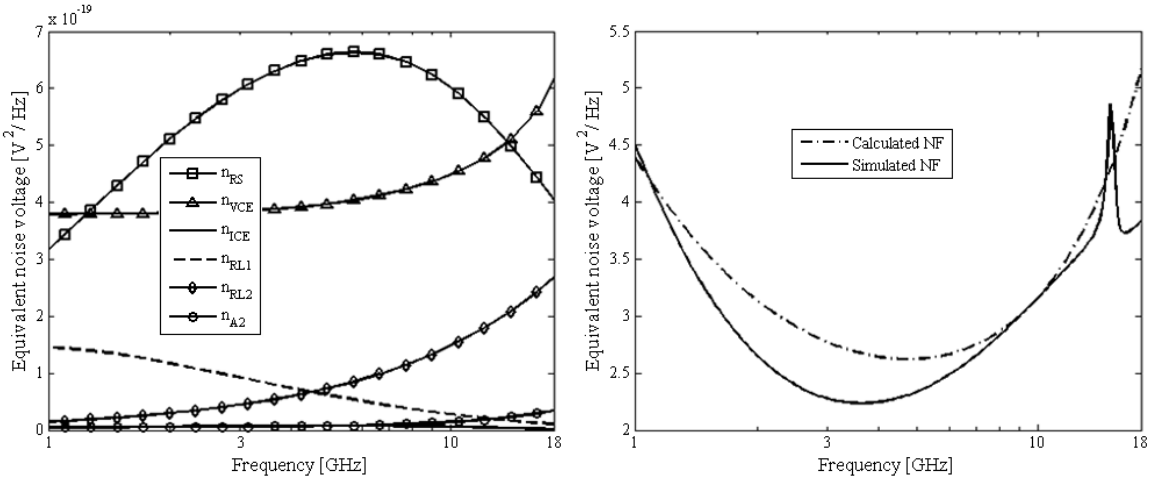

Figure 5.6. Noise contributions and calculated and simulated NF after collector current and C_{L1} optimization.

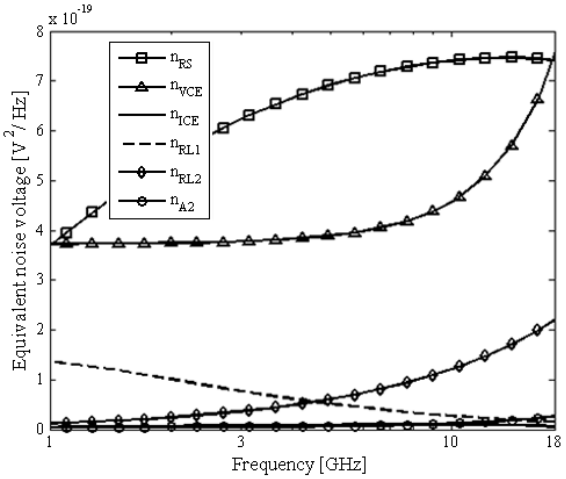

Figure 5.7. Final noise contributions of the noise sources after optimization of the passive components and collector current.

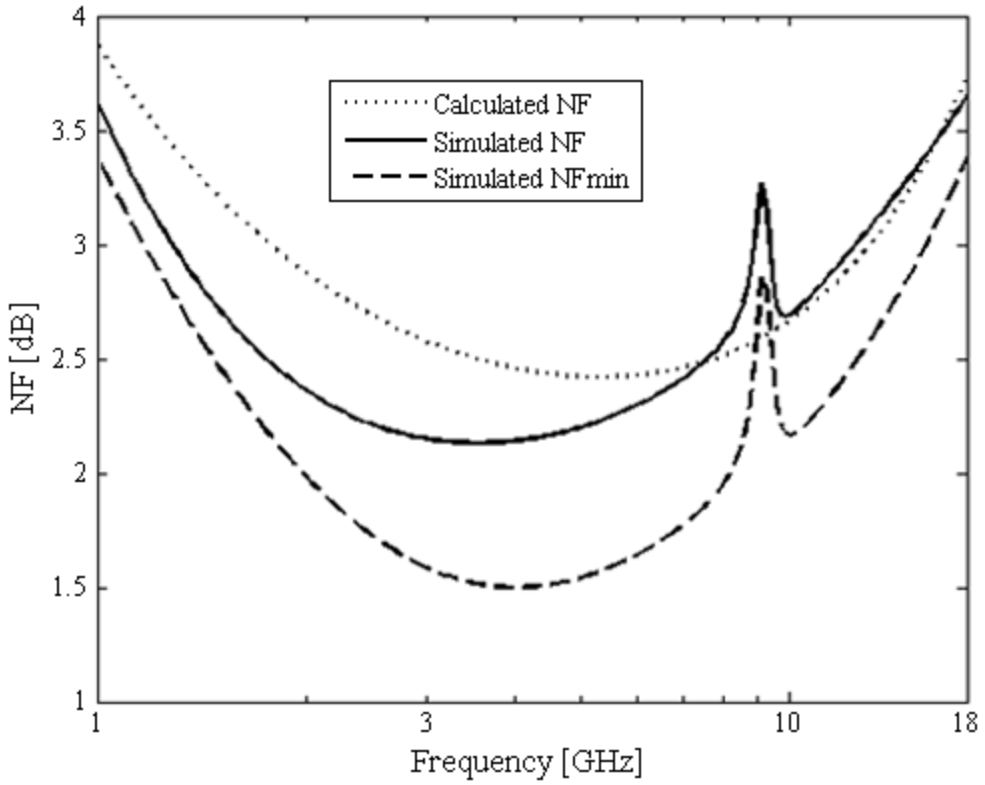

Figure 5.8. Final simulated and calculated NF after optimization of the passive components and collector current.

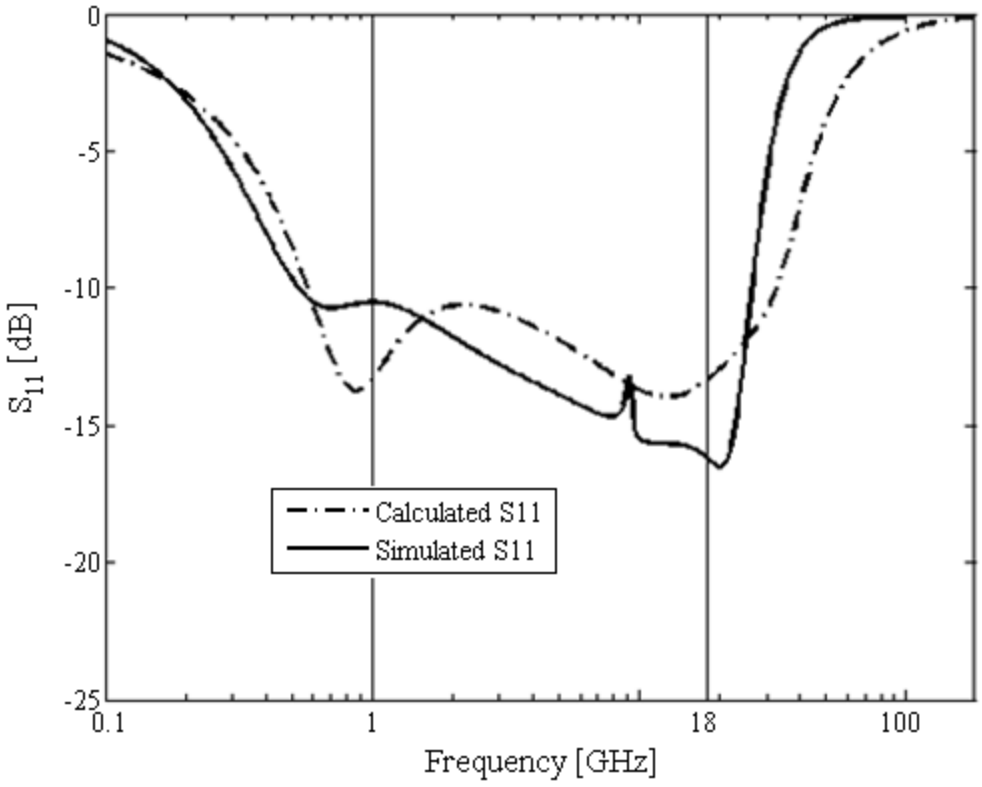

Figure 5.9. Final simulated and calculated S_{11} after optimization of the passive components and collector current.

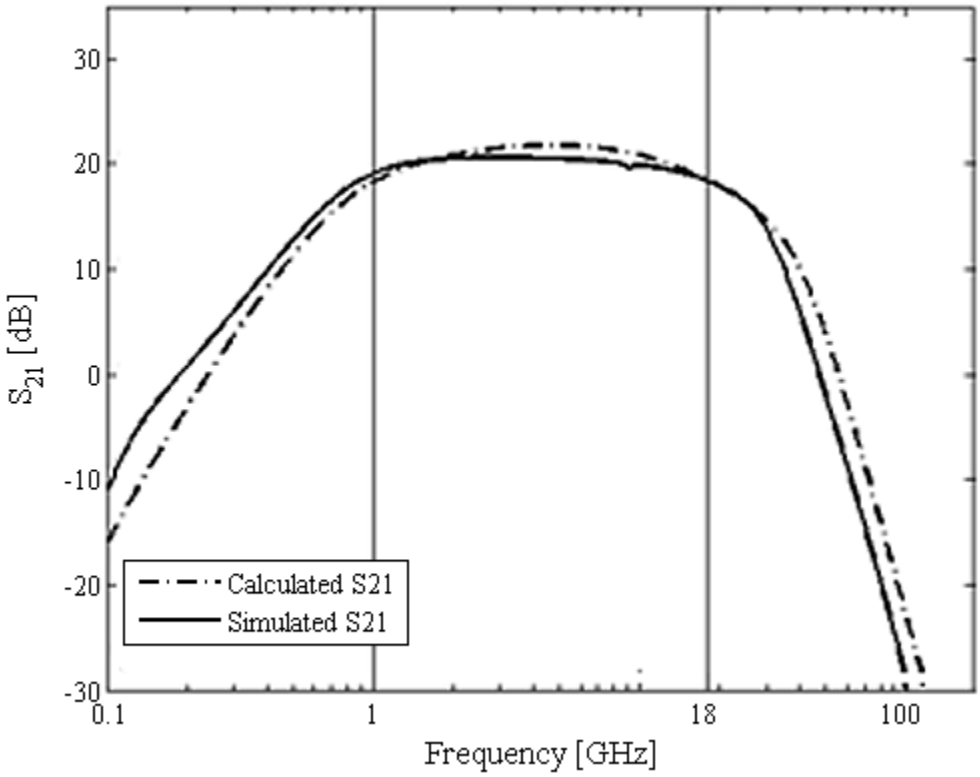

Figure 5.10. Final simulated and calculated S_{21} after optimization of the passive components and collector current.

Table 5.4. Comparison of initial component values and values after noise optimization.

Symbol	Initial value	Optimized value
C_1	177 fF	40 fF
C_F	266 fF	92 fF
C_{L1}	0	150 fF
L_1	7.96 nH	9.91 nH
L_2	442 pH	363 pH
L_3	1 nH	465 pH
R_{L1}	417 Ω	230 Ω
I_{C1}	0.6 mA	3.5 mA
I_{C2}	5 mA	5 mA

Figure 5.10 shows that the maximum gain of the final amplifier is 21.4 dB and falls to 18.2 dB at 18 GHz which is the upper corner frequency. At the lower corner frequency the gain is 19.9 dB. The input reflection coefficient in Figure 5.9 is shown to be less than

-10 dB over the frequency band of interest and thus all specifications except for the P_{1dB} compression point have now been met.

The simulated reverse isolation of the LNA is excellent with S_{12} < -25 dB. The output reflection coefficient is very large however since no attempt at output matching was made. Such matching is complicated by the large bandwidth which renders tuned reactive network matching infeasible. A straightforward solution would be to add a final amplifier stage with a load resistance close in value to the characteristic impedance of the system; ignoring the effect of any parasitic elements this will match the output over the entire bandwidth. This technique was followed in matching the amplifier designed for the 7WL process which is presented in Section 5.5.

5.3.3 Stability

The minimum value of the K stability factor is 1.85 which is larger than 1, and the B_f factor minimum is 0.027 which is larger than zero. These two criteria are necessary and sufficient to ensure the unconditional stability of the LNA [**65**]. Simulations were done over the entire frequency range and up to the f_{max} (280 GHz) of the transistor to also ensure that there are no instabilities at frequencies beyond the range of interest.

5.3.4 Monte Carlo analysis and temperature sweep

To find the sensitivity of the design to process parameter variations a Monte Carlo analysis was performed. Since many of the process parameters are physically correlated it is important to take these correlations into account when doing a statistical analysis. The statistical design kit included in the PDK provided by IBM does capture these correlations in the skew values used during the analysis [**56**]. The variations in the *S*-parameters with 100 simulated cases are shown in Figure 5.11 and that of the NF in Figure 5.12.

S_{11} varies by approximately 2 dB above 2 GHz, but remains below -10 dB. Between 1 GHz and 2 GHz the S_{11} varies by as much as 2.5 dB and, ignoring the one extreme case, reaches a maximum value of -9 dB. Even this is a good input return loss value and as such the effects of the variation on LNA performance should not be noticeable.

The low to mid-band S_{21} varies from 18.5 dB to 22 dB, which is a variation of 3.5 dB, and thus remains within the specified range of 18 to 22 dB. When the low frequency gain

increases above approximately 20.5 dB the gain at the upper corner frequency no longer increases due to the gain-bandwidth product of the transistor. This means that the -3 dB cut-off frequency is reduced to less than 18 GHz. It is however emphasized that the gain at 18 GHz is not reduced, but remains constant while lower frequency gain increases and thus operation in a sub-band at the upper frequency end remains feasible.

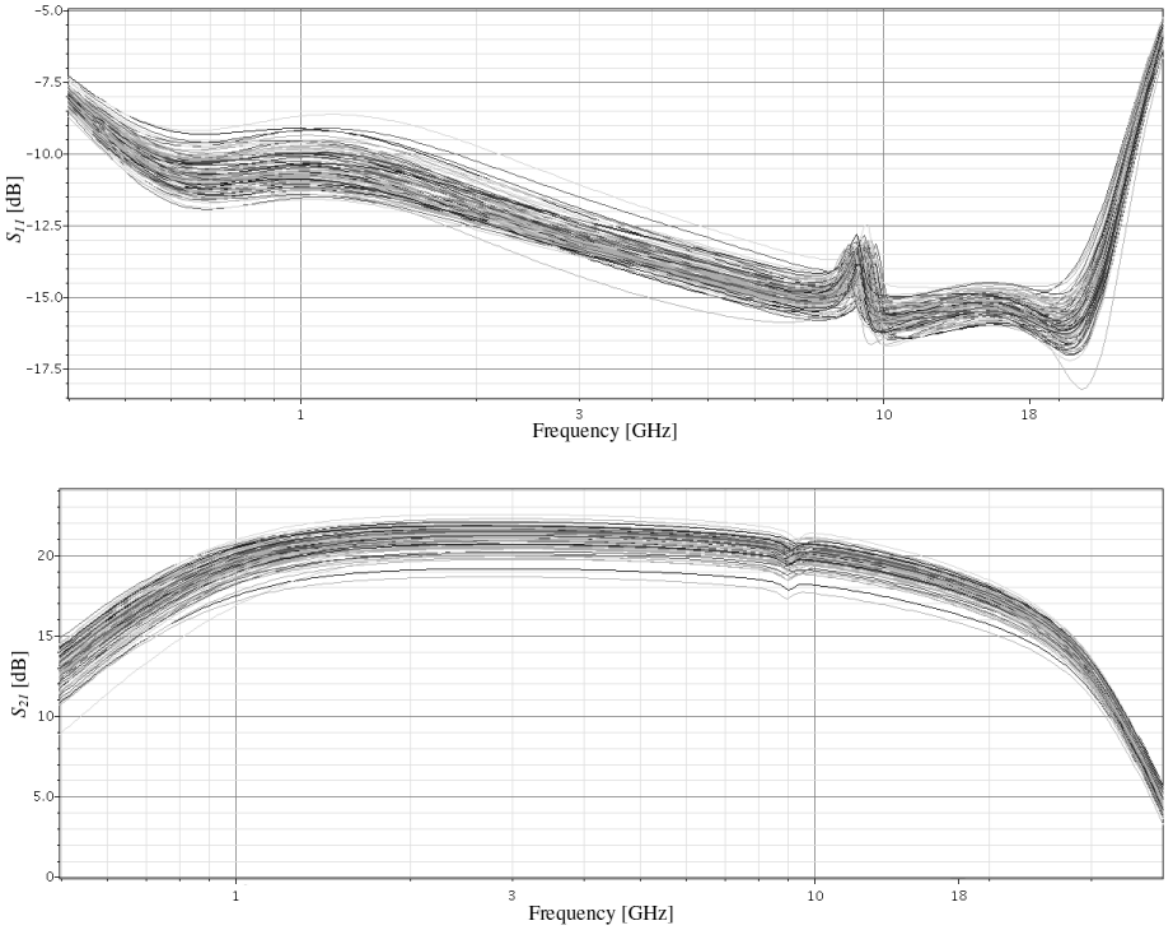

Figure 5.11. Variation in S_{11} (top) and S_{21} (bottom) resulting from a Monte Carlo analysis.

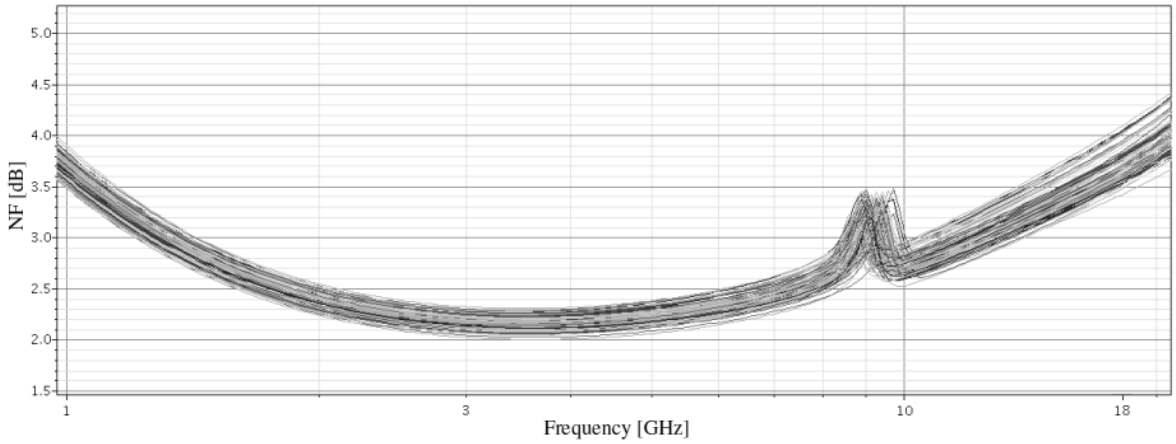

Figure 5.12. Variation in NF resulting from a Monte Carlo analysis.

The NF varies by less than 0.5 dB over most of the frequency band and only becomes more than 4 dB in extreme cases above 16 GHz, where the variation is approximately 0.7 dB.

Through the one-by-one substitution of the circuit elements with ideal components it was found that the most parameter sensitive components are inductor L_1 and the transistors. Based on this finding a circuit with ideal passive components was simulated and the transistor emitter length was swept over a 2 µm range from 10 µm to 12 µm. The variation in the performance measures are shown in Figure 5.13. The relatively small deviations over such a wide range of emitter lengths indicate that the emitter length has very little impact on the performance and as such the transistors are most sensitive to either emitter width- or doping variations. Unfortunately there is no straightforward way of differentiating between these effects using Spectre RF.

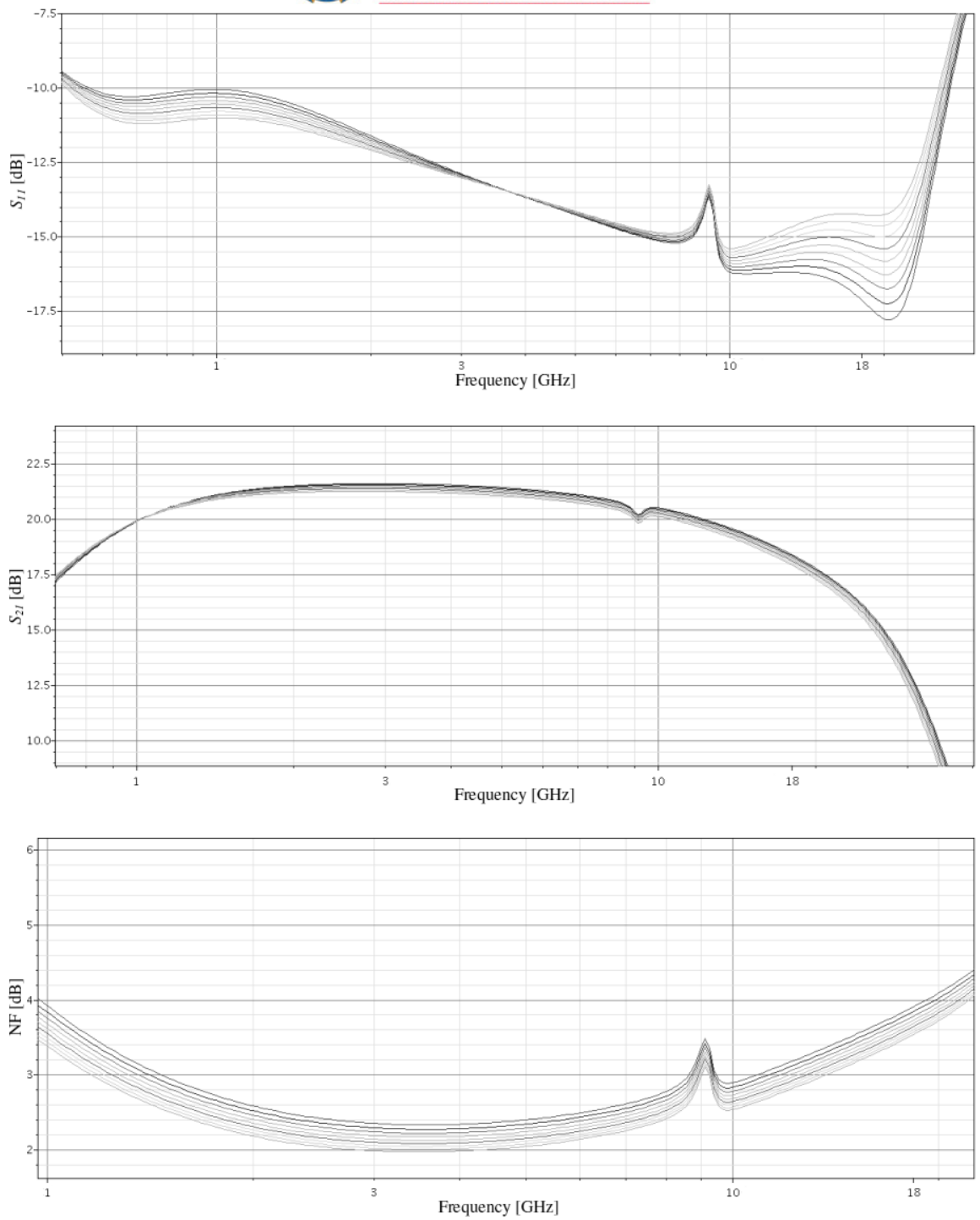

Figure 5.13. Variation in performance with l_e swept from 10 µm to 12 µm.

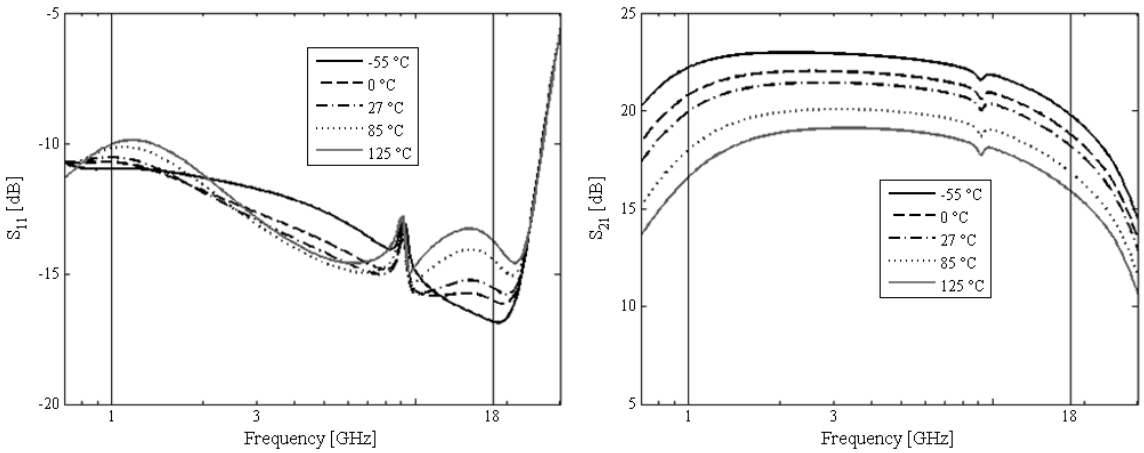

Figure 5.14. S_{11} and S_{21} variation with temperature from -55 °C to 125 °C.

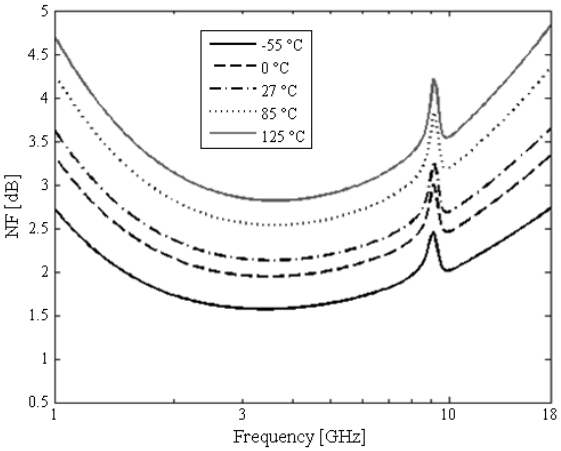

Figure 5.15. NF variation with temperature swept from -55 °C to 125 °C.

5.3.5 Linearity of the LNA and its optimization

The linearity of the noise optimized LNA was determined by simulating both the P_{1dB} compression point and IIP3 using a large signal analysis in Spectre RF. Input power was swept from -50 dBm to 0 dBm at various frequencies over the band of interest and the results are plotted versus frequency in Figure 5.16.

The linearity of the LNA is the only performance measure that is below specification with the IIP3 -27.5 dBm at 1 GHz, increasing approximately linearly to -22 dBm at 9 GHz above which the IIP3 remains constant. It is likely that the non-linearity of the second stage transistor is the determining factor in this maximum value for IIP3, while the high gain of the first stage decreases the IIP3 below 9 GHz. It can also be seen that the approximation used for IIP3 in the mathematical model over estimates the simulated IIP3 significantly over most of the band, and then underestimates it at high frequencies. Therefore a more

accurate model such as one derived using a Volterra-series should be used if more accurate modelling is desired. P_{1dB} varies from -26.5 dBm at 1 GHz to -14 GHz at 9 GHz from where it remains constant with frequency.

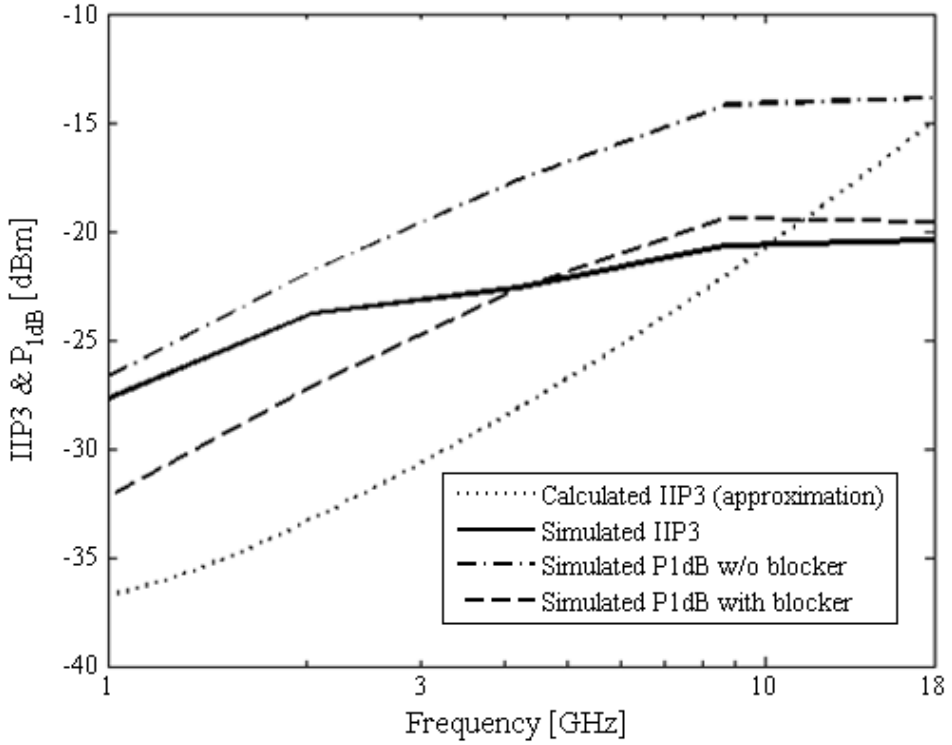

Figure 5.16. Simulated IIP3 and P_{1dB} compression point versus frequency of the noise optimized LNA.

The first attempt that was made towards improving the linearity of the LNA was to use the cascode configuration in the second stage in order to reduce the voltage drop over the BC-capacitance and also decrease avalanche multiplication. However, it has been pointed out that it is the exponential $I_{CE} - V_{CE}$ non-linearity that dominates at currents lower than 5 mA [**37**] and as such no improvement was observed.

It was shown that an I_C of around 25 mA produces the optimal IIP3 [**37**], but this is not practical for the second stage as this will result in too high a low frequency gain which will decrease the high frequency gain due to the gain-bandwidth product. The current density will also be very close or even beyond the peak f_T where many other second order effects also become important. Finally such a large increase in power consumption is not an acceptable trade-off for the increase in linearity.

The use of overall feedback was also considered but has the shortcoming of greatly affecting the input matching and noise performance of the LNA as discussed in Section 4.8. It was also found that the linearity improvement due to overall feedback is not more than what can be obtained by using feedback only in the last amplifier stage as discussed next.

Since the last amplifier stage of a LNA dominates the linearity of the LNA as a whole, and its linearity is reduced by the gain of the preceding stages it stood to reason that improving the linearity of this stage would be the most feasible means of improving performance. Resistive emitter degeneration was used to provide series-series feedback. Since this decreases the transconductance both the collector current and load impedance was increased to maintain a constant gain for this stage. The collector current was increased to a the rather high value of 12 mA since the $I_{CE} - V_{CE}$ non-linearity due to avalanche multiplication (which typically dominates for 5 mA < I_C < 25 mA) improves with collector current [**37**]. The improvement observed in the linearity of the amplifier is given in Figure 5.17 which illustrates the plots of the improved IIP3 and P_{1dB}. An emitter resistance of only 4 Ω was used since larger degeneration resulted in the -3 dB cut-off frequency going below 18 GHz. It is interesting to note that while the IIP3 has been improved, the linearization attempt has decreased the P_{1dB} compression point.

Adding emitter degeneration to the first stage does not improve linearity further. Initially there appeared to be some improvement, however upon closer investigation it was seen this was due to the reduction in the gain of the first stage (and thus less reduction of second stage linearity) and not due to the first stage linearity improvement. According to (4.51) a reduction in the first stage gain given in dB should lead to a one-to-one improvement of overall IIP3, and this was indeed the case; thus there is no advantage in degenerating the first stage as this only influences the input matching, gain and NF negatively without improving linearity as the second stage remains completely dominant.

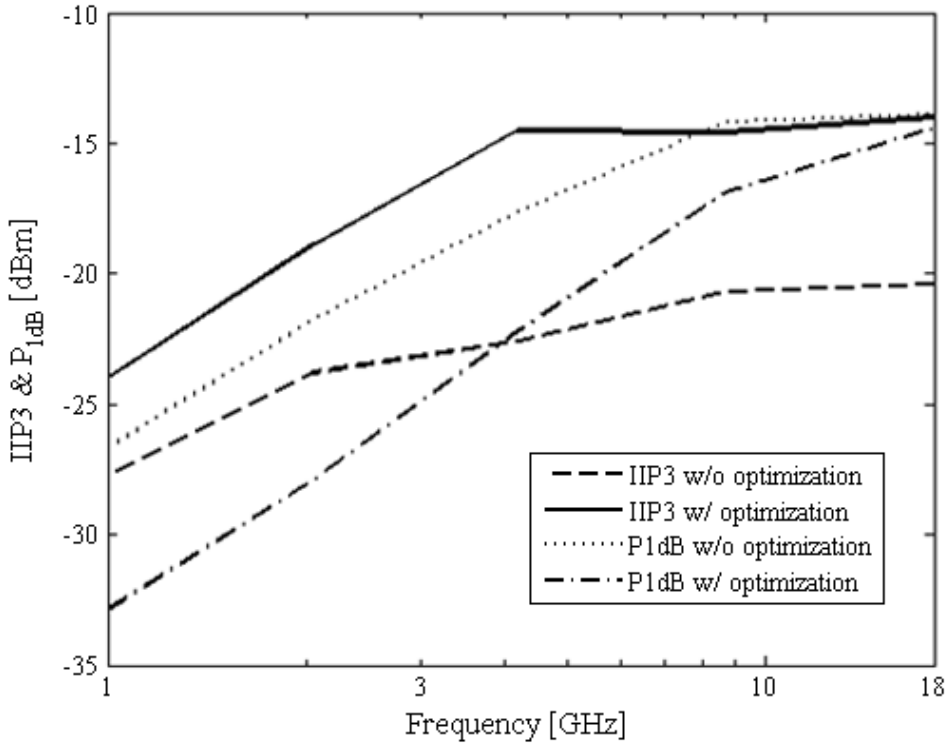

Figure 5.17. Simulated IIP3 and P_{1dB} compression point versus frequency with and without second stage emitter degeneration.

It was also considered that a third amplifier stage could be added to allow smaller gain per stage, and thus larger emitter degeneration resulting in more linear stages. However since the third stage linearity is now reduced by both the first and second stage gain it was found that the linearity is worsened even when relatively large emitter resistors are used.

It was therefore concluded that only using emitter degeneration in the final stage is the most effective means of improving the linearity of the amplifier, while also reasonably maintaining the results of the other performance measures. The shape of forward gain and NF remained the same as before the linearity improvement and thus are not shown again, but gain was decreased by 0.9 dB to 20.0 dB and NF was increased on average by 0.5 dB to 2.15 dB at the minimum and 3.85 dB at the upper corner frequency. Although the S_{11} curve versus frequency changed somewhat in shape it remained below the specified -10 dB.

In closing a remark on the P_{1dB} being higher than the IIP3 in both Figure 5.16 and Figure 5.17 is warranted. In a single transistor amplifier stage with constant power coefficients it is usually found that the single tone P_{1dB} compression point is theoretically 9.6 dB lower than the IIP3. In more complex systems this is not necessarily the case as the

coefficients also become more complex. In broadband amplifiers the IP3 is affected by the harmonics above the third harmonic which may also fall in the band of interest and therefore act as significant blockers of the first harmonic which would result in a much lower IIP3 than expected.

The sharp increase in IIP3 observed in both Figure 5.16 and Figure 5.17 corroborates this. For a 1 GHz signal all harmonics up to the 17th harmonic fall within the pass-band of the LNA resulting in a very low IIP3. For a 3 GHz signal the harmonics up to the 5th order are still passed. It is only above 6 GHz that the 3rd order harmonic falls outside of the pass band, and this coincides with the frequency where the rapid increase in IIP3 tapers off. Above this frequency it is likely that the further improvement in linearity is due to the high frequency gain roll-off of the two amplifier stages.

With these considerations in mind it is reasonable that the P_{1dB} could be higher than the IIP3 in broadband LNAs. In Figure 5.17 where the emitter resistor has been included the P_{1dB}/IIP3 relation is closer to the theoretical response, especially at high frequencies.

5.3.6 Sensitivity of the LNA optimized for linearity

Since the use of feedback makes the gain and other LNA performance measures less dependent on the transistor parameters it was justified to investigate the effect of the linearity optimization, i.e. the addition of local shunt-shunt feedback, on the LNA sensitivity. The same Monte Carlo analysis and temperature sweeps were performed as for the original LNA and the results are shown in Figure 5.18 to Figure 5.21.

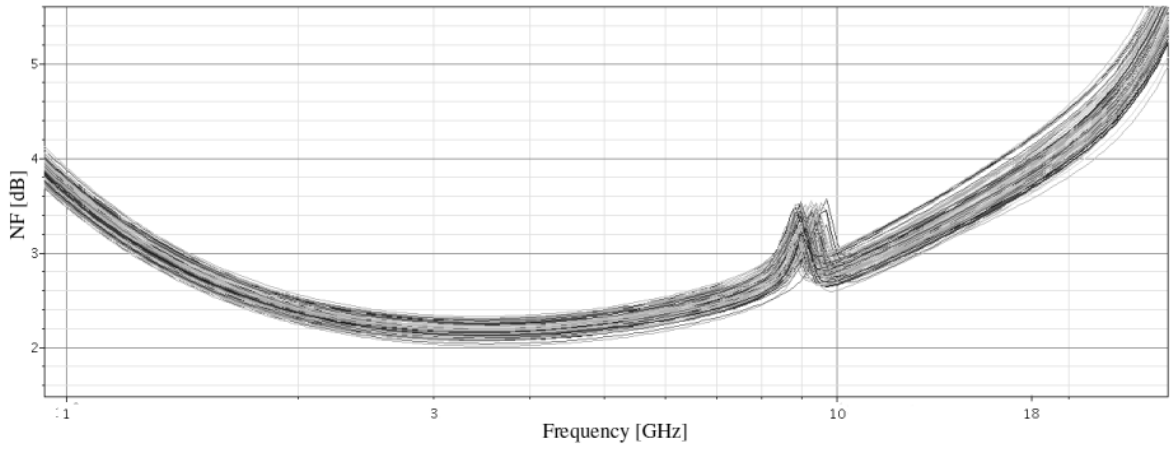

Figure 5.18. Variation in NF resulting from a Monte Carlo analysis on the LNA with emitter degeneration.

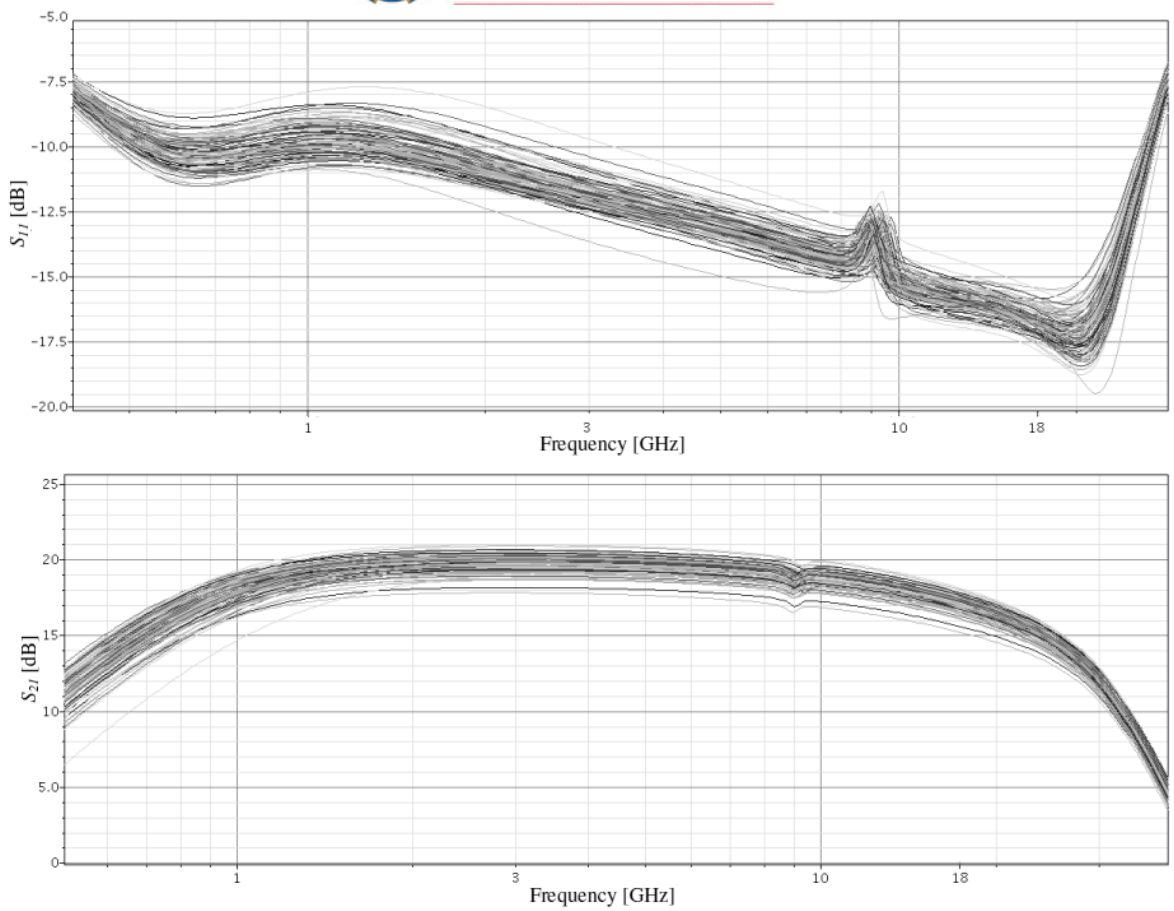

Figure 5.19. Variation in S_{11} (top) and S_{21} (bottom) resulting from a Monte Carlo analysis on the LNA with emitter degeneration.

The S_{11} varies between -10 dB and -8.4 dB at 1 GHz and remains above -10 dB in some cases up to 2.6 GHz, from where it is always within specification. This is a similar deviation to the 2 dB variation reported in the LNA without feedback.

A large improvement can however be seen in the gain variation with S_{21} varying between 16.3 and 19.3 dB at 1 GHz, 18.8 and 20.9 dB in the mid-band and from 16 to 17.9 dB at 18 GHz. That is an average variation of only 2.4 dB compared to 3.5 dB in the previous case. A more important observation however is that the gain never increases above the designed gain, namely 21.4 dB, but only decreases by at most 3 dB. This means that the problem of the reduced upper -3 dB cut-off frequency due to the gain-bandwidth product when low frequency gain is increased has been resolved through the addition of emitter degeneration to the latter stages of the LNA.

The NF varies by only 0.3 dB up to 12 GHz compared to the 0.4-0.5 dB variation reported for the previous case, and also remains below 4 dB at frequencies lower than 16 GHz as

before. At 18 GHz the total variation in NF is 0.64 dB with a maximum of 4.25 dB. Thus although the NF variation has been reduced the absolute NF is slightly higher at the high frequency end.

Thus although the low frequency input matching and the high frequency noise performance has been slightly reduced, a large improvement in the robustness with process variations of both the *S*-parameters and NF resulted from the addition of feedback. The increase in maximum NF of 0.25 dB is easily justified through these gains in addition to the improvement in the linearity of the LNA which was the initial objective. The disadvantage of poor input return loss at the low frequency end can also be easily compensated for by overdesigning for the S_{11} parameter in future designs based on the knowledge obtained here.

Robustness with temperature is also very good and shows a large improvement to the results presented in Section 5.3.4. Input return loss remains below the specified -10 dB over most of the temperature and frequency range. The only exception is the case below 2 GHz at 85 °C and 125 °C.

Gain varies by only 2.5 dB (as opposed to 4.5 dB before) in the mid-band over the entire military specification temperature range. The upper -3 dB cut-off frequency is also once again maintained despite this variation due to the upper limit placed on low frequency gain by the degeneration resistors. At -55 °C where the mid-band gain is at its maximum the gain at 18 GHz is 18 dB, and when the gain is decreased to its minimum at 125 °C the mid-band gain is 18.4 dB with the gain at 1 GHz an 18 GHz at respectively 15.5 dB and 15.4 dB.

The NF varies by 2 dB on average over the entire temperature range and an increase in the absolute NF of 0.6 dB at high frequencies is again observed similar to the discussion above.

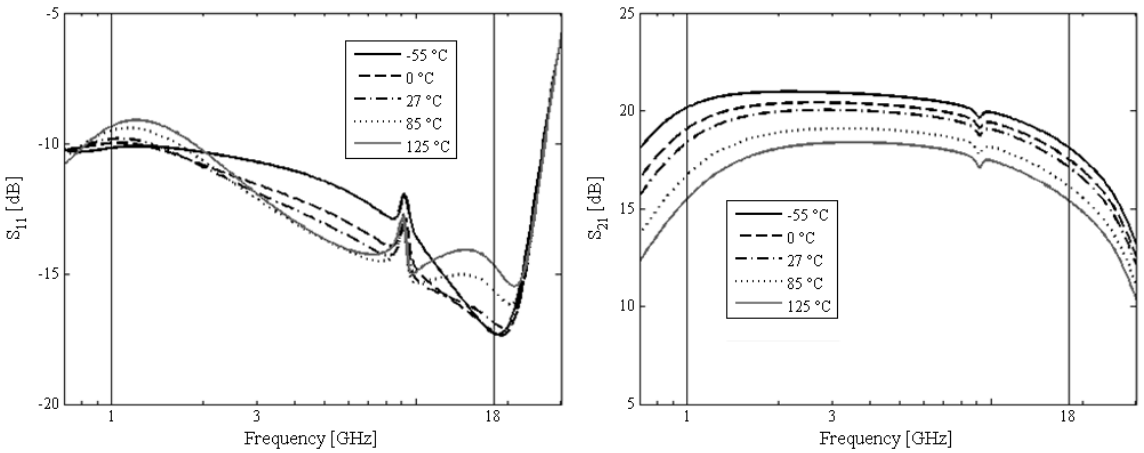

Figure 5.20. S_{11} and S_{21} variation with temperature from -55 °C to 125 °C for the LNA optimized for linearity.

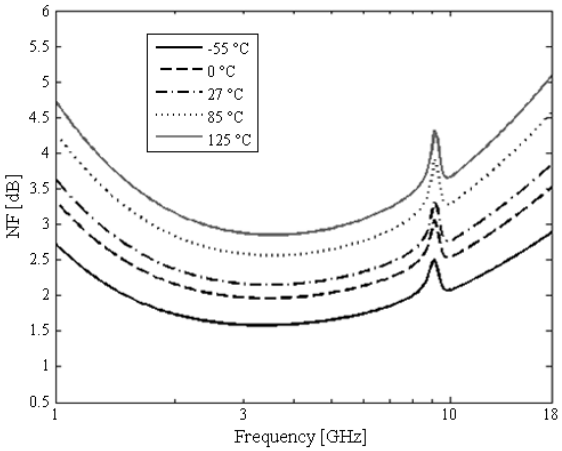

Figure 5.21. Variation in NF of the LNA optimized for linearity with temperature from -55 °C to 125 °C.

5.3.7 Dynamic range and group delay

To determine the dynamic range of the LNA the output noise of the LNA optimized for linearity was simulated. The plot of the output noise voltage spectral density (S_o) is shown in Figure 5.22 with the estimated noise bandwidth of 30 GHz. The average S_o in the band of operation is 39 aV^2/Hz and thus the rms output noise voltage (v_{no}) is 1.08 mV, which is -29.3 dBm in a 50 Ω system; and when reduced by the 20 dB voltage gain when referred to the input becomes -49.3 dBm which is the minimum detectable signal (MDS) of the LNA. Thus the dynamic range, using the average IIP3 of -17.2 dBm, is

$$\begin{aligned} \mathrm{IIP3}-\mathrm{MDS} &= -17.2\ \mathrm{dB}-\left(-49.3\ \mathrm{dB}\right) \\ &= 32.1\ \mathrm{dB} \end{aligned}. \qquad (5.1)$$

The group delay of both variations of this LNA was simulated and are shown in Figure 5.23.

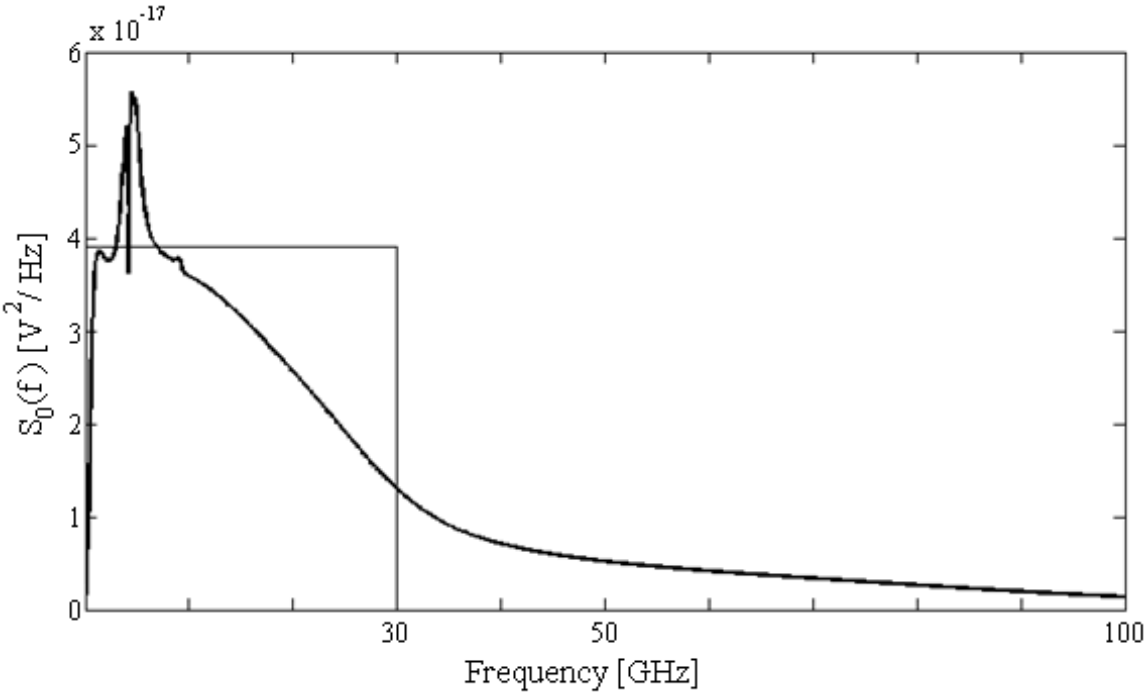

Figure 5.22. Simulated output noise voltage spectral density versus frequency of the linearity optimized LNA.

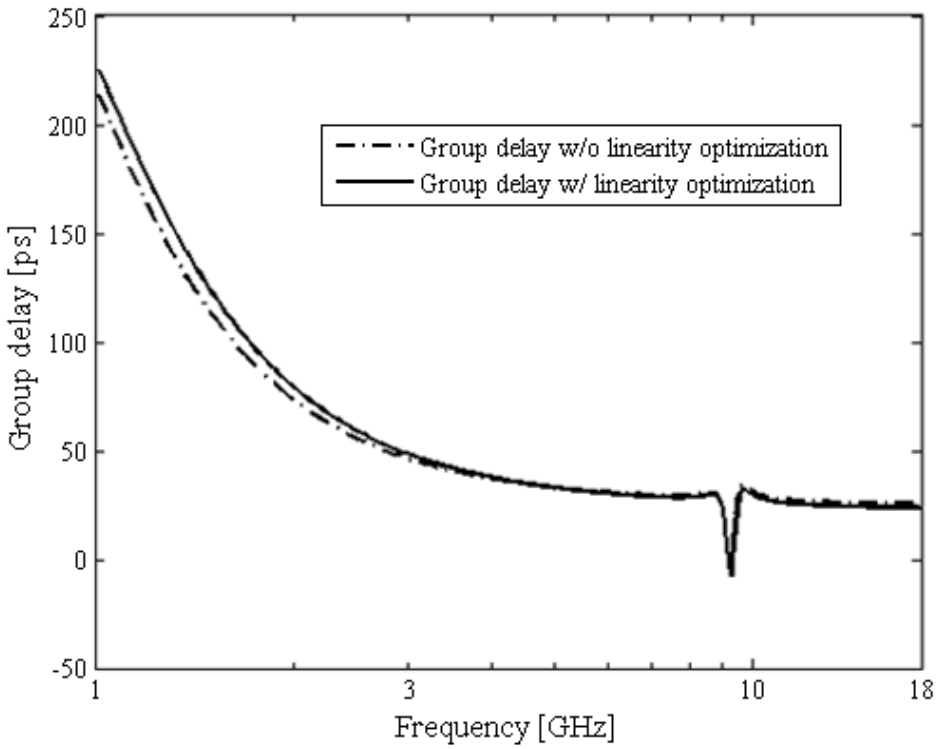

Figure 5.23. Group delay of the LNA with and without linearity optimization over the 1 GHz to 18 GHz band.

5.3.8 Third amplifier stage

If a third amplifier stage is used care should be taken to avoid unnecessary peaking in the frequency response due to the second stage load inductor. An additional parallel resistance could be used to limit the gain at high frequencies. Peaking will increase the gain of the signal which reduces the IIP3 of the third stage further.

5.3.9 Final LNA specifications

The final specifications of both the LNA with and without linearity improvement are given in Table 5.5.

Table 5.5. Final specifications of the 1-18 GHz LNAs designed in the 8HP process

	BW [GHz]	**S_{11} [dB]**	**S_{21} [dB]**	**NF [dB]**	**IIP3 [dBm]**	**P [mW]**
w/o linearity optimization	1–18	< -10	21	2.1–3.6	-22.6 @ 4.2 GHz	12.75
with linearity optimization	1–18	< -9.8	20	2.2–3.9	-14.5 @ 4.2 GHz	23.25

5.4 8HP DESIGN AT 60 GHZ

Wideband wireless network schemes such as the UWB have mostly failed to deliver on their promise of high bandwidth since they are reliant on extensive baseband processing which quickly becomes complex and consume large amounts of power [**16**]. In contrast there is an abundance of bandwidth available in the unlicensed part of the mm-wave frequency band (57–64 GHz), which can be leveraged against power consumption in mobile devices. In addition Silicon Germanium (SiGe) technology has offered a low cost alternative to the more traditional III-V compounds making mm-wave radios a very attractive prospect.

The use of the LC-ladder and capacitive feedback LNA configuration at mm-wave frequencies is discussed below. Simulation results of a design are given with remarks on the effectiveness of the IMN and also suggestions for alternative design methods.

Since the Q-factor of the on-chip spiral inductors decay very rapidly above 30 GHz [**56**] microstrip transmission line inductors, also discussed in Section 2.7, were used throughout in the 60 GHz design.

The design equations discussed in Chapter 4 were used in the same way as in Section 5.3.1. The component and collector current values that were obtained are given in Table 5.6, and the input impedance, *S*-parameters and NF results are shown in Figure 5.24 and Figure 5.25.

Table 5.6. Calculated component values of the 60 GHz LNA.

Symbol	Calculated value
C_1	177 fF
C_F ($C_{BC} = C_\mu$)	0 fF
L_1	140 pH
L_2	124 pH
L_3	540 pH
R_{L1}	117 Ω
I_{C1}	5 mA
I_{C2}	12 mA

Most importantly it should be noted from the results that the mathematical model no longer describes the performance of the LNA with sufficient accuracy at such high frequencies. Various possible reasons for this have been given in Section 4.10. Figure 5.24 shows that the resonant frequencies of the input matching network are not predicted correctly. The calculated gain is also less than the simulated value and the calculated NF more, as seen in Figure 5.25.

The LNA achieves relatively good performance for a 60 GHz LNA compared to the published results of other LNA configurations in Table 5.7. Although it can be seen that the very low input reflection coefficient is not due to input impedance at the centre of the matched band being equal to 50 Ω and centred on the operating frequency, but rather due to the upper resonant peak of the input matching network being close to 60 GHz and approximately equal to 50 Ω.

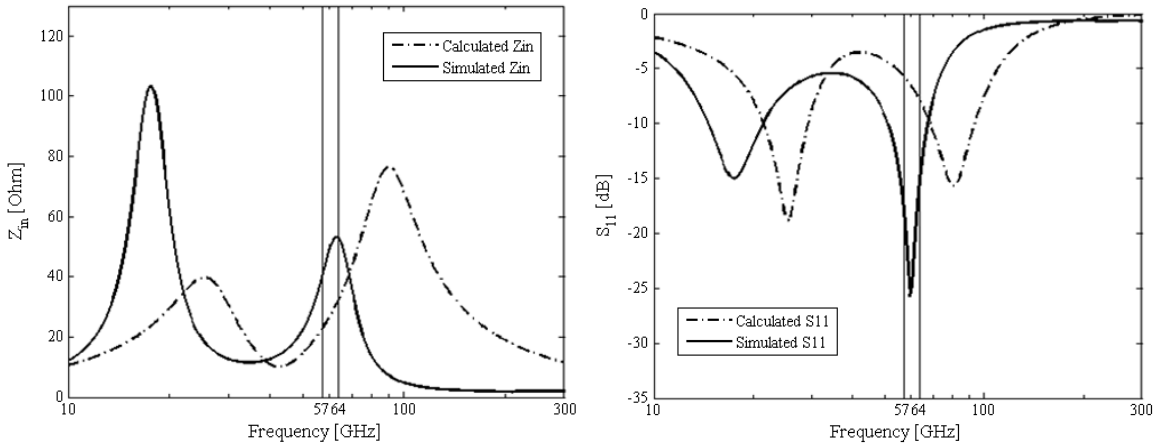

Figure 5.24. Calculated and simulated input impedance and S_{11} of the 60 GHz LNA.

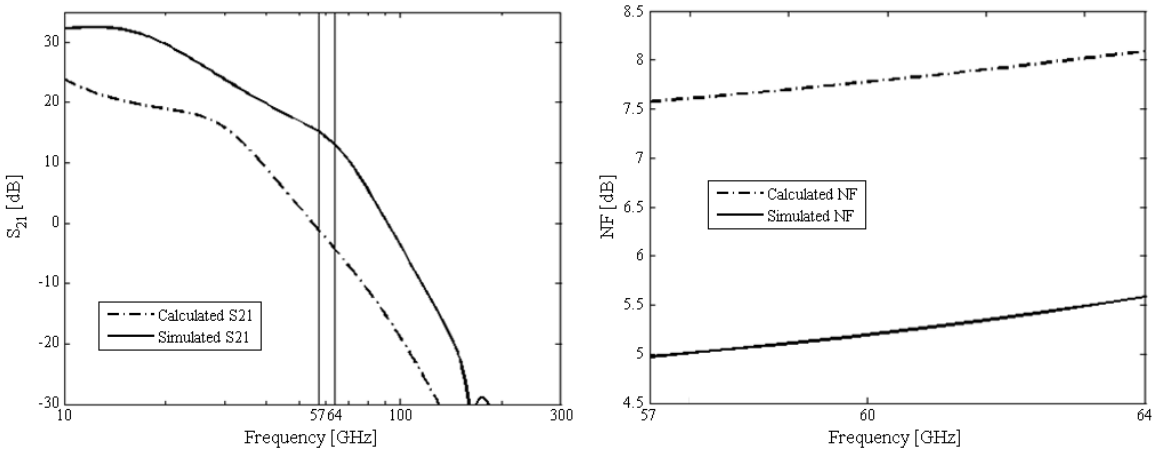

Figure 5.25. Calculated and simulated forward gain and NF of the 60 GHz LNA.

Table 5.7. 60 GHz LNA results and comparison to published results of other LNA configurations.

Ref.	Technology	f [GHz]	S_{11} [dB]	S_{21} [dB]	NF [dB]	IIP3 [dBm]	P_{1dB} [dBm]	P [mW]
This work	0.13 µm SiGe BiCMOS	60	< -15	14.2	5.2	-8.4	-20	25.5
[**66**]	90 nm CMOS	58	< -10	14.6	5.5	-6.8	-	24
[**67**]	0.13 µm SiGe BiCMOS	60	< -10	18	5	-	-	7.5
[**68**]	0.25 µm SiGe BiCMOS	60	< -10	18	6.7	-	-18	20
[**69**]	0.12 µm SiGe BiCMOS	58	< -10	14.8	4.1	-2	-12	8.1

The above observation means that the part of the IMN determining the lower corner frequency is no longer important since it is the resonant frequency of the upper corner frequency components that now provide conjugate input matching. The components that determine the lower corner frequency are C_2 and L_1. The capacitance is synthesized using the Miller impedance at the base of the transistor and as such cannot be removed. The inductor is implemented as a transmission line which is not only used for matching but also acts as a bias choke. Since the bias choke remains a necessary part of the circuit this inductor cannot simply be removed, however if it is desired to save the chip area occupied by L_1 it can be removed and a large off-chip bias choke could be used instead without significantly affecting the performance of the LNA. The simulated results of a circuit where this has been applied are shown in Figure 5.26 and Figure 5.27.

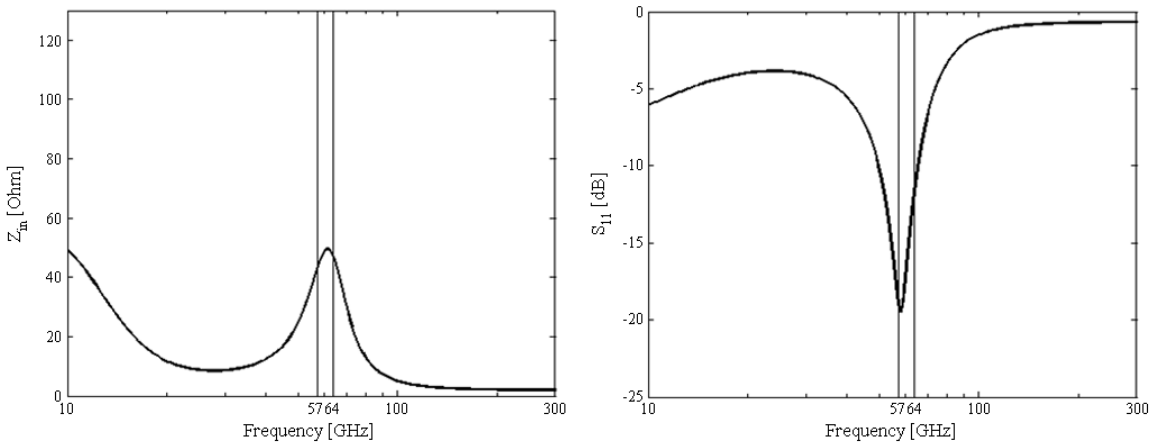

Figure 5.26. Simulated input impedance and S_{11} of the 60 GHz LNA without L_1.

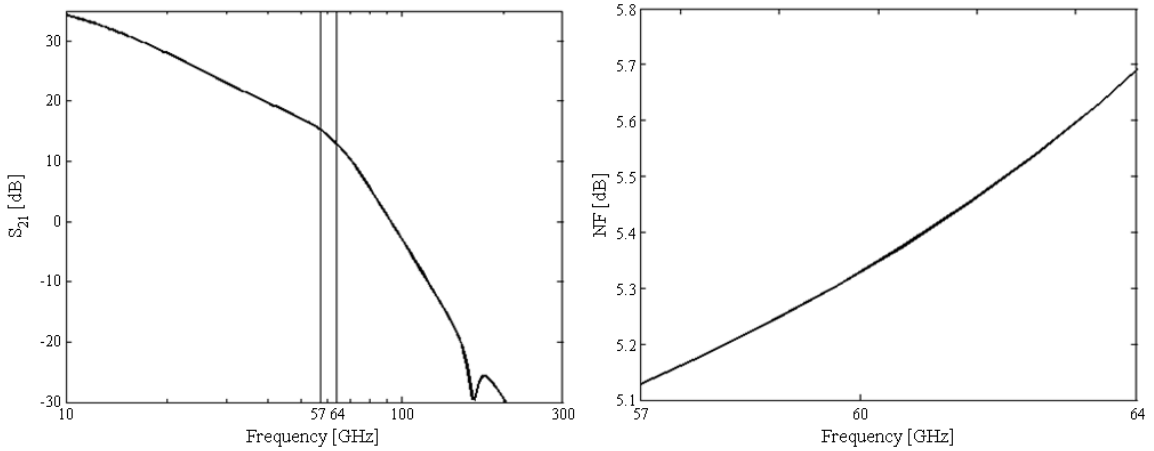

Figure 5.27. Simulated forward gain and NF of the 60 GHz LNA without L_1.

In conclusion, although results comparable to those in literature were obtained, the theory of the design process is no longer consistent with simulated results due to various second

order effects present when operating close to the device f_T; it is therefore suggested that a distributed design approach, discussed in Section 2.5, should be applied to mm-wave design with the current transistor technology.

Lastly it is noted that parasitics have a very large impact on circuit performance above 20 GHz and especially at 60 GHz. This requires EM simulations of the final layout to ensure extraction of all parasitic elements that will be present in a fabricated LNA; however since the conclusion is not to use the discussed design approach at 60 GHz with current transistor technology, and since a design at 60 GHz is not the focus of this study but rather wideband LNAs at lower frequencies, such simulations were not performed.

5.5 7WL DESIGN FOR 3-14 GHZ

5.5.1 Initial design

The design process followed for the LNA in the 7WL for fabrication was identical to process described in Section 5.3. The design specifications were kept the same except for the frequency range which was changed to the 3 GHz to 14 GHz range since the process has a lower f_T meaning less gain could be achieved per stage due to the GBP. A voltage gain of approximately 3.3 per stage or 10 dB is achievable over this frequency band. Because of this limitation it was necessary to add a third amplifier stage with a gain of 10 dB as suggested in Section 4.12 to attain the required overall gain of 20 dB, with the first and second stage together providing a flat 10 dB gain over the frequency band. Transistor emitter lengths of 20 µm and a 1.8 V power supply were used.

The values in Table 5.8 were derived for the initial design and the calculated and simulated *S*-parameters and NF results are shown in Figure 5.28 and Figure 5.29. Again the calculated *S*-parameters track the simulations sufficiently, and the calculated NF is very accurate in this case.

Table 5.8. Initial component values derived using the design equations and the final optimized values.

Symbol	Value	Optimized value
C_1	227 fF	150 fF
C_F	208 fF	50 fF
L_1	2.65 nH	3.7 nH
L_2	568 pH	525 pH
L_3	600 pH	293 pH
R_{L1}	325 Ω	90 Ω
R_{L2}	80 Ω	70 Ω
R_{L3}	75 Ω	60 Ω
I_{C1}	0.66 mA	2.5 mA
I_{C2}	2.7 mA	2.7 mA
I_{C3}	2.7 mA	2.7 mA

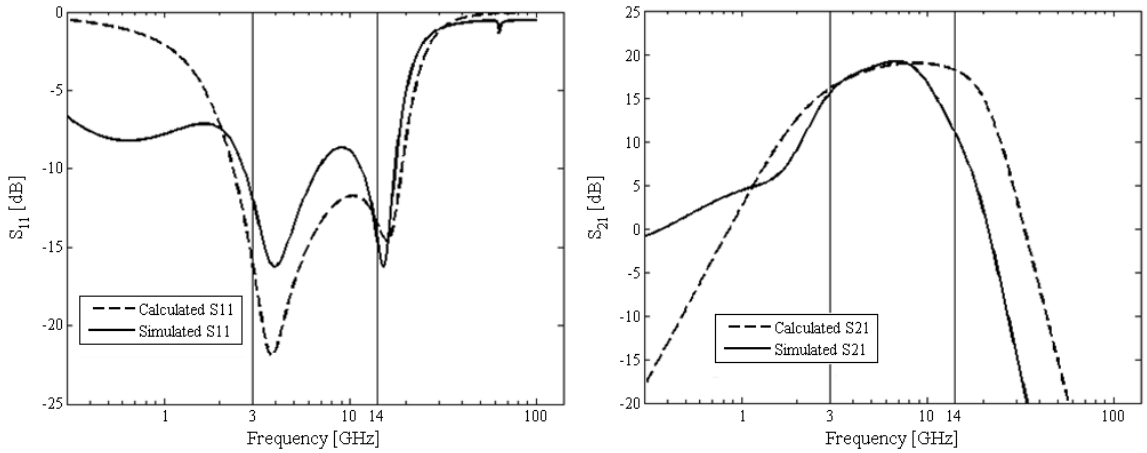

Figure 5.28. Calculated and simulated *S*-parameters without any optimization.

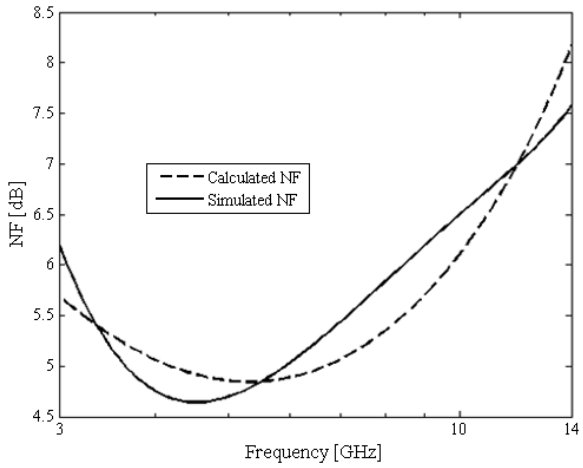

Figure 5.29. Calculated and simulated NF without any optimization.

5.5.2 Noise optimization

Noise optimization was applied to the LNA with the same procedure followed in Section 5.3.2. Using (4.56) it was found that a first stage gain of 9.8 dB is required to meet a maximum NF requirement of 6 dB, taking into account a potential subsequent NF improvement of 2 dB. The first stage gain was adjusted as such and the collector current and load resistance optimized. The use of an additional load capacitance (C_{L1}) was not feasible in this case as the reduction in gain was too large, however S_{11} remained below -10 dB after this optimization. Finally the passive component values were also optimized.

The noise optimized component and current values are shown in Table 5.8. The initial noise contribution of the various noise sources and those after optimization are plotted in Figure 5.30 and the final *S*-parameters and improved NF plots are shown in Figure 5.31 and Figure 5.32 respectively. An improvement of 2.68 dB, 3.07 dB and 1.79 dB has been obtained at the lower corner-, upper corner- and minimum NF frequencies respectively compared to the initial NF in Figure 5.29. The minimum NF is 2.8 dB at 5.3 GHz and the maximum 4.3 dB at the upper corner frequency.

The average gain of the final amplifier is 20.7 dB which falls to 19.6 dB at 3 GHz and 17.8 dB at 14 GHz, the lower- and upper corner frequencies. The inductive load of the second stage causes peaking in the S_{21} response at high frequencies with the maximum value of 21.4 dB at 8.6 GHz. The simulated input reflection coefficient in Figure 5.31 remains below -10 dB. In this case the gain and input return loss specifications have been met with the NF only going slightly above 4 dB at frequencies higher than 12.7 GHz.

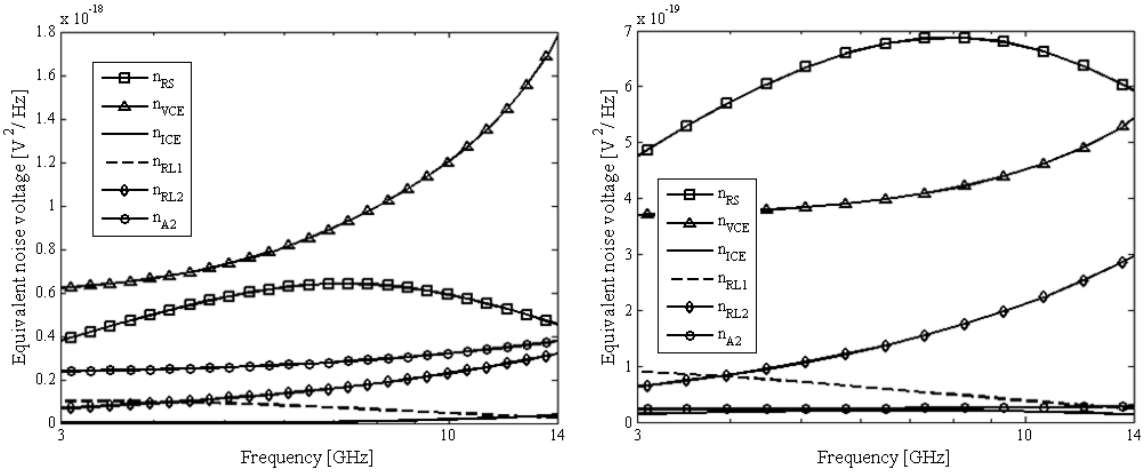

Figure 5.30. Noise contribution of the various noise sources before optimization (left) and after the noise optimization process (right).

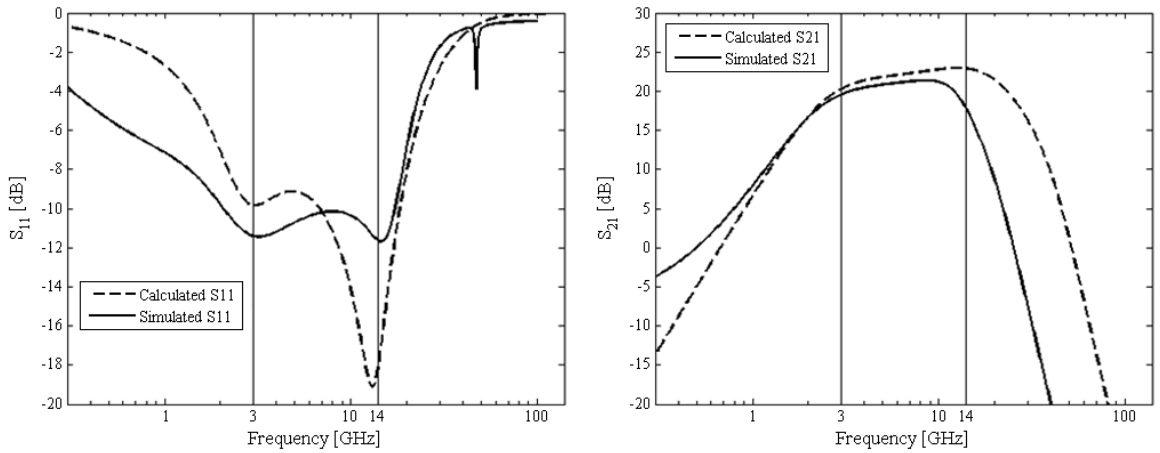

Figure 5.31. Final simulated and calculated S_{11} and S_{21} after optimization of the passive components and collector current.

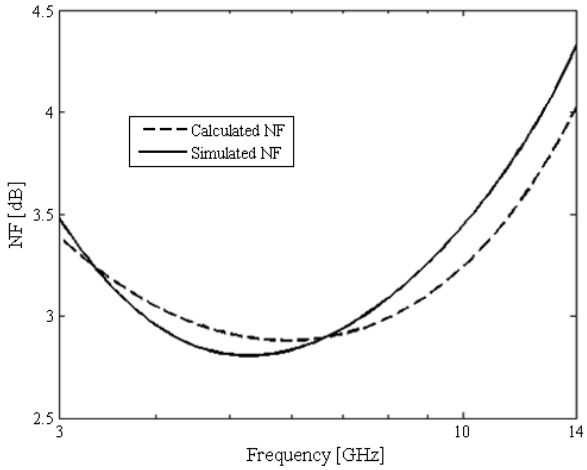

Figure 5.32. Calculated and simulated NF after optimization of the passive components and collector current.

Two observations regarding the correlation between the calculated and simulated results were made which indicate improvements that are still required to make it more accurate. Firstly, the calculated gain is overestimated at high frequencies where the finite GBP of the transistor causes a roll-off in the simulated gain. The effect of the GBP should thus be included in the mathematical model if it is to be used in designs operating at the limits of the transistor technology. Secondly, it was found that the Q-factor of the inductors has a very large impact on the calculated NF and also impacts the *S*-parameters somewhat. It is only once the correct Q-factors were found that the good NF correlation was obtained. This means that the selection of average Q-factors for the inductors which are assumed constant over frequency is not an acceptable simplification and frequency dependent Q-factor modelling based on inductor dimensions should be included.

A large spike is also observed in the calculated S_{11} at the upper corner which is not present in the simulated result. It was found that removing the capacitance of the bond pad from the total input shunt capacitance C_1 removed this spike and although there was still a 2 dB difference in the two curves the shape was similar. This raises the question as to whether the capacitance of the bond pad is modelled correctly in the 7WL HIT-kit. It should be possible to clarify this from the measured results.

The simulated reverse isolation (S_{12}) of the LNA is less than -56 dB over the frequency band of interest. As suggested in Section 5.3.2 the load resistance of the third amplifier stage was used to provide output matching. A 75 Ω resistance was used to achieve the desired gain with the least possible collector current while at least maintaining S_{22} < -10 dB, and proved very effective with the final simulated S_{22} remaining below -13.5 dB over the operating frequency range.

5.5.3 Stability

The minimum value of the *K* stability factor is 52.6 due to the good reverse isolation and output matching. The minimum of the B_f factor is 0.956 and since it is above zero and the *K*-factor above 1 the LNA is unconditionally stable over the entire frequency range [**65**]. Simulations were also done up to the f_{max} (280 GHz) of the transistor to ensure that there are no instabilities at frequencies beyond the range of interest.

5.5.4 Monte Carlo analysis and temperature sweep

To find the sensitivity of the design to process parameter variations a Monte Carlo analysis was performed. The variations in the *S*-parameters with 100 simulated cases are shown in Figure 5.33 and that of the NF in Figure 5.34.

S_{11} varies by approximately 2 dB over most of the frequency band with slightly larger deviations just below 14 GHz. The input return loss remains below -10 dB for most of the simulated cases and never goes above -9.5 dB.

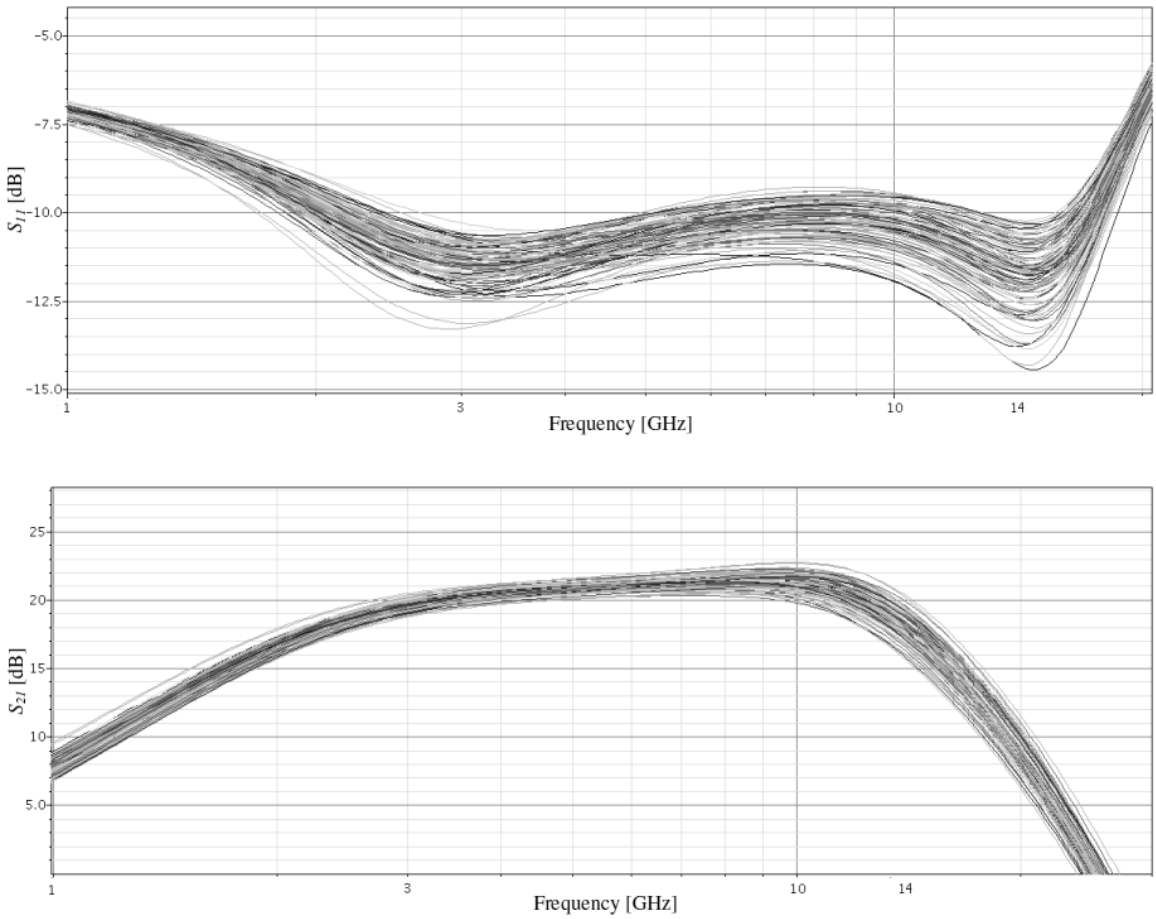

Figure 5.33. Variation in S_{11} (top) and S_{21} (bottom) resulting from a Monte Carlo analysis.

The S_{21} varies by 2 dB over most of the operating range, only showing larger deviations in the region where peaking due to the inductive load is present. The gain is between 19 and 21 dB below 4.3 GHz, between 20 and 22 dB up to 7 GHz, and then the gain variation increases to a maximum of 4 dB at 14 GHz. In most cases the gain at 14 GHz remains above 17 dB which is the designed gain and also the -3 dB cut-off with the designed average gain of 20 dB; though in some cases the effective -3 dB cut-off point may be less than 14 GHz when the low frequency gain is increased above 20 dB by process variations.

The NF variation is 1 dB over most of the frequency band and increases slightly above 10 GHz. The NF is less than 4 dB from 3 GHz to 10 GHz, and is also the maximum NF at these respective frequencies. NF remains below 5 dB up to 14 GHz.

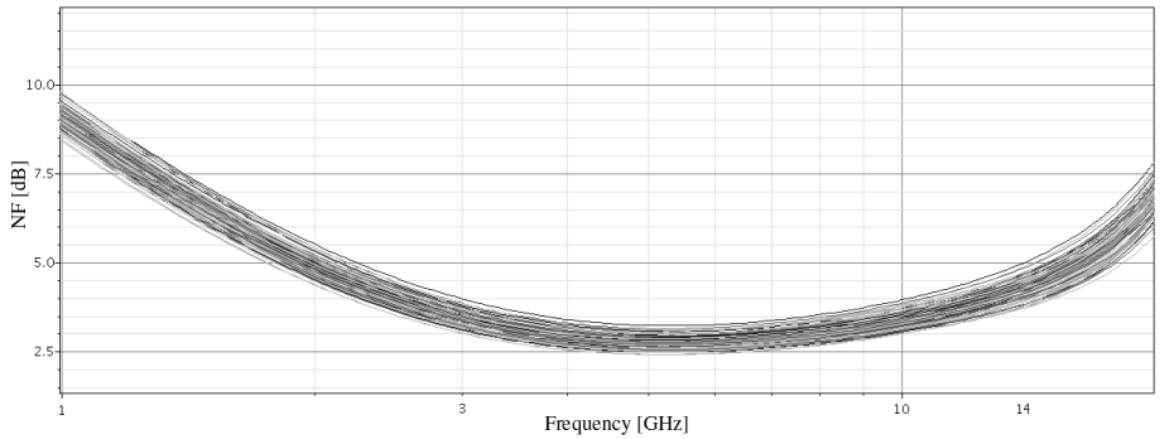

Figure 5.34. Variation in NF resulting from a Monte Carlo analysis.

A temperature sweep was performed to test the robustness of the LNA over a -55 °C to 125 °C temperature range. The results are shown in Figure 5.35 and Figure 5.36. Temperature variations have a relatively small impact on the input return loss and since S_{11} remains below -9 dB the variation will not be a concern in most applications. The gain however is very temperature dependent since it is directly dependent on temperature through V_T when emitter degeneration is not used. S_{21} varies between 14.5 dB at 125 °C and 27 dB at -55 °C below 10 GHz which is a very large 12.5 dB variation. Over the 0 °C to 85 °C commercial temperature range the gain varies from 17 dB to 23 dB, which is closer to the specified 18-22 dB gain.

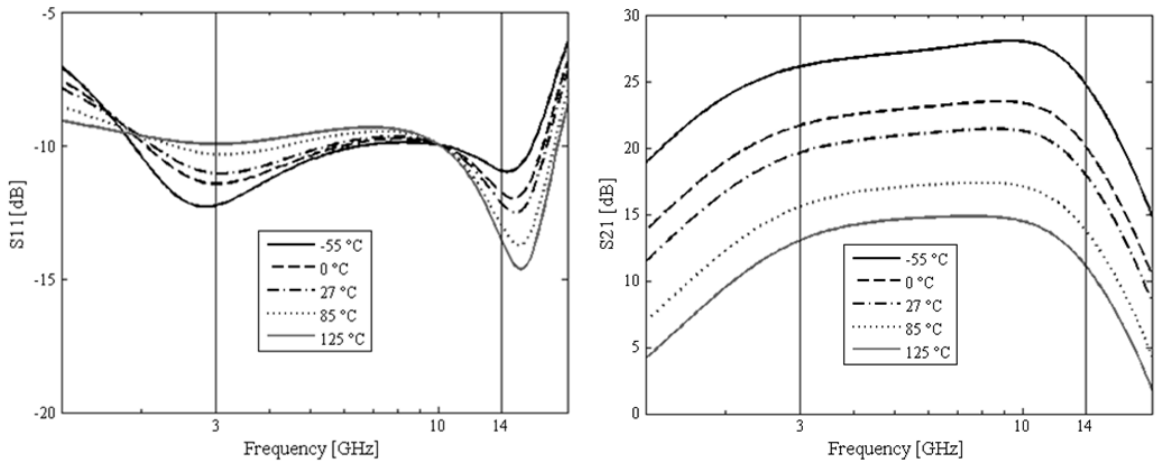

Figure 5.35. S_{11} and S_{21} variation with temperature from -55 °C to 125 °C.

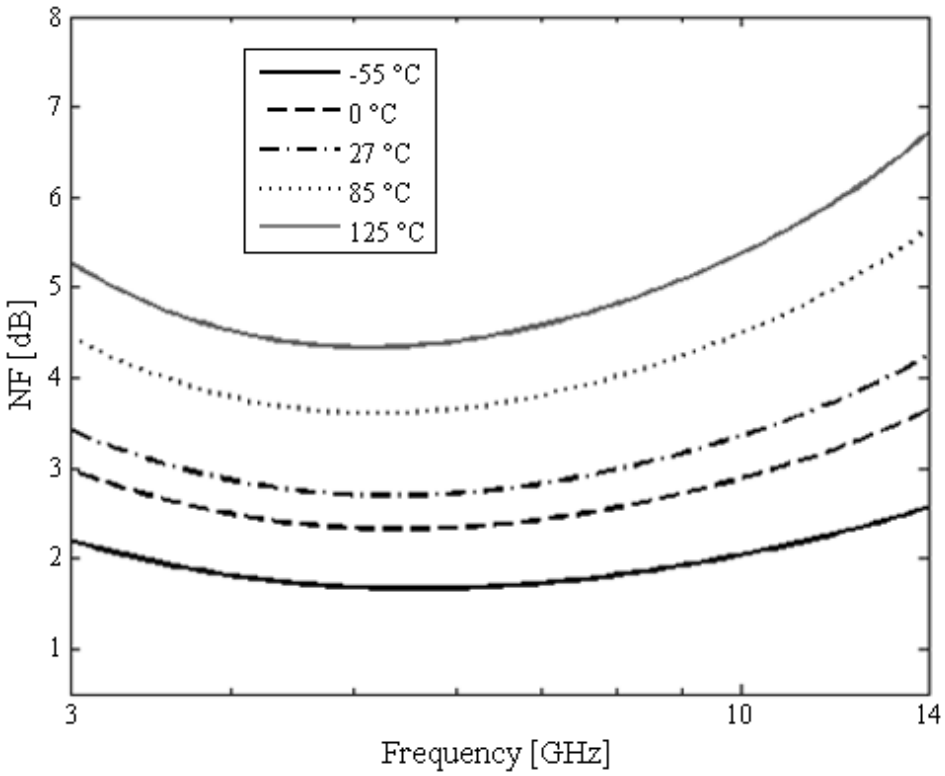

Figure 5.36. NF variation with temperature swept from -55 °C to 125 °C.

The total NF variation is approximately 3 dB below 10 GHz and increases to 4 dB at 14 GHz. At both 85 °C and 125 °C the NF is above the specified 4 dB over most of the operating frequency range.

5.5.5 Linearity of the LNA and its improvement

The linearity of the noise optimized LNA was again determined by simulating the P_{1dB} intercept point and IIP3 using a large signal analysis. The results are plotted in Figure 5.37. In this case the simulated IIP3 is much closer to the approximated IIP3 derived from calculation compared to the design in Section 5.3.5.

The last (third) amplifier stage once again dominates the linearity of the LNA, but the high gain of the first stage at lower frequencies also causes much distortion in the second stage. Therefore both the second and third stage was degenerated with emitter resistors to improve linearity. To compensate for the decreased gain the adjustments shown in Table 5.9 was made to the circuit. The improvement observed in the linearity of the amplifier is shown in Figure 5.38 which shows the plots of the IIP3 and P_{1dB} with and without emitter degeneration.

Once again the P_{1dB} is higher than the IIP3 in some cases. A possible explanation for this has been given at the end of Section 5.3.5.

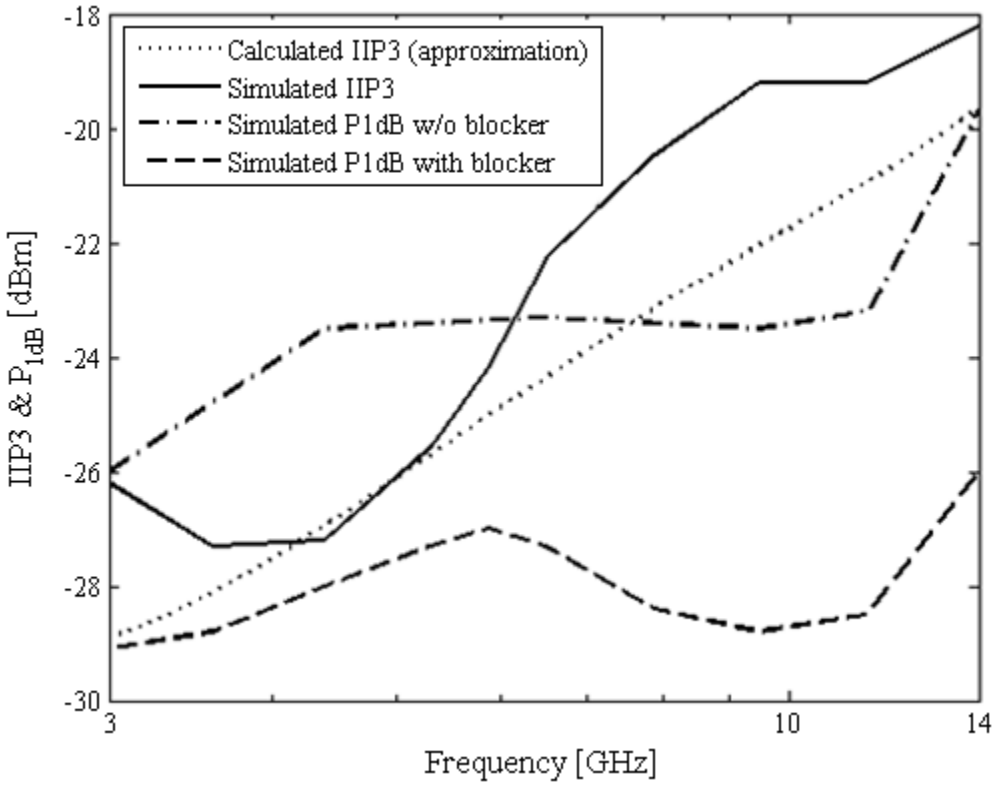

Figure 5.37. Simulated P_{1dB} compression point and IIP3 versus frequency of the noise optimized LNA.

Table 5.9. Changes in component values to compensate for the gain reduction when feedback was added.

Symbol	Original value	Noise optimized	Linearity optimized
L_3	600 pH	293 pH	315 pH
R_{L3}	75 Ω	60 Ω	80 Ω
I_{C2}	2.7 mA	2.7 mA	8 mA
I_{C3}	2.7 mA	2.7 mA	8 mA
R_{E2}	-	-	9 Ω
R_{E3}	-	-	8 Ω

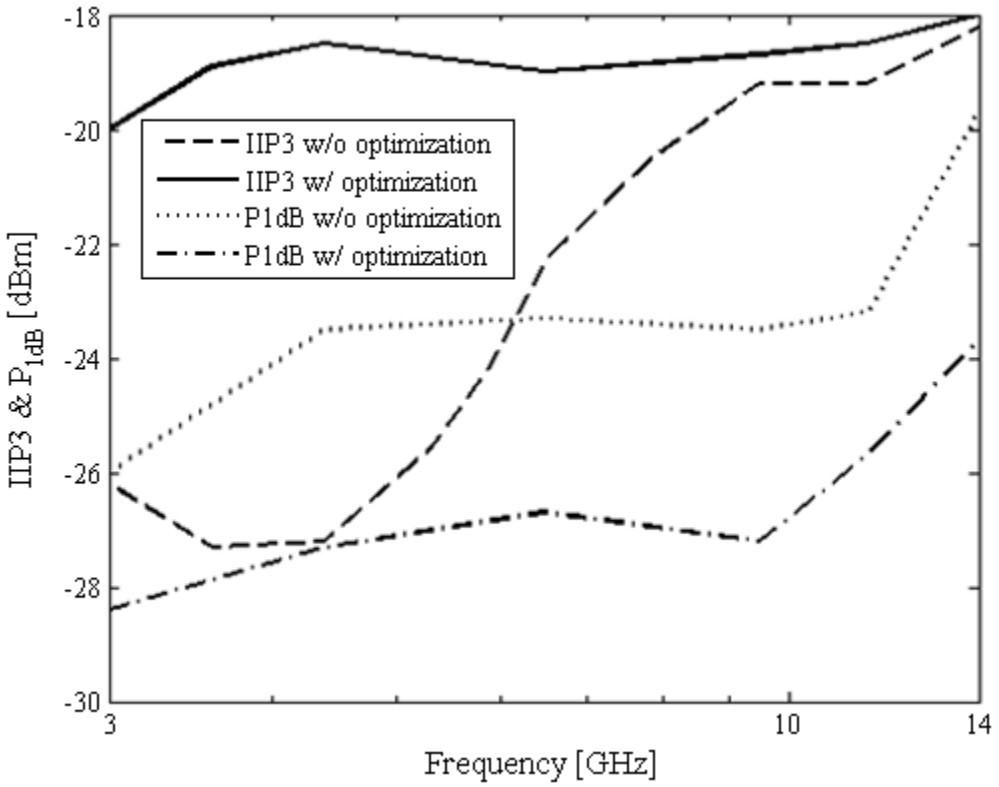

Figure 5.38. Simulated IIP3 and P_{1dB} compression point versus frequency with and without second and third stage emitter degeneration.

5.5.6 Sensitivity of the LNA optimized for linearity

The sensitivity of the LNA to process parameters and temperature was again determined. A Monte Carlo analysis revealed a 2 dB variation in S_{11} similar to the LNA without feedback, however in this case the average value is higher, resulting in a S_{11} between -10 and -9 dB in many cases. NF varies by approximately 1 dB over the entire frequency band and S_{21} by 2 dB and 3 dB in the low to mid and high frequency parts of the band respectively. This is similar to the variation observed without feedback. The -3 dB cut-off frequency is only slightly reduced below 14 GHz in extreme cases.

The NF and input return loss variation with temperature is the same in the case without feedback although the average NF at high frequencies has increased by 0.8 dB. The maximum S_{11} is -8.9 dB and occurs at-55 °C. A large improvement was however observed in the sensitivity of the gain to temperature, with the gain variation, originally between 14.5 and 27 dB from 125 °C to -55 °C, now being reduced to 16.3 and 23.3 dB.

Thus the improvement in the sensitivity of this design is not as significant as in the case presented in Section 5.3.6, but the IIP3 improvement and added temperature stability of the

gain due to its reduced dependence on transistor g_m by the emitter resistors will still warrant the use of this technique in many applications.

5.5.7 Dynamic range and group delay

To determine the dynamic range of the LNA the output noise of the LNA optimized for linearity was simulated. The plot of S_o is shown in Figure 5.39 with the estimated noise bandwidth from 2 GHz to 14 GHz. The average S_o in this band is 69 aV^2/Hz and thus v_{no} is 910 µV, which, in a 50 Ω system, is -30.8 dBm; and when reduced by the 20 dB voltage gain when referred to the input becomes -50.8 dBm, the MDS of the LNA. Thus the dynamic range, using the average optimized IIP3 of -18.8 dBm, is

$$\begin{aligned} \text{IIP3} - \text{MDS} &= -18.8\ \text{dB} - \left(-50.8\ \text{dB}\right) \\ &= 32\ \text{dB} \end{aligned}. \tag{5.2}$$

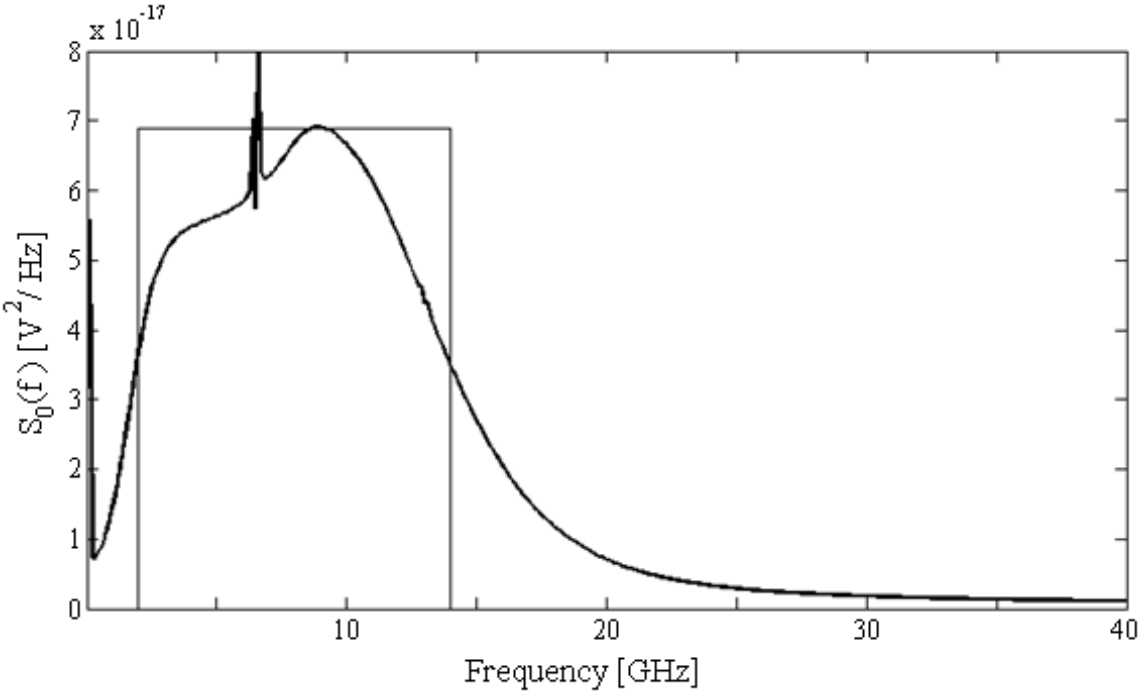

Figure 5.39. Simulated output noise voltage spectral density versus frequency of the linearity optimized LNA.

The group delay of the LNA with and without linearity improvement is given in Figure 5.40.

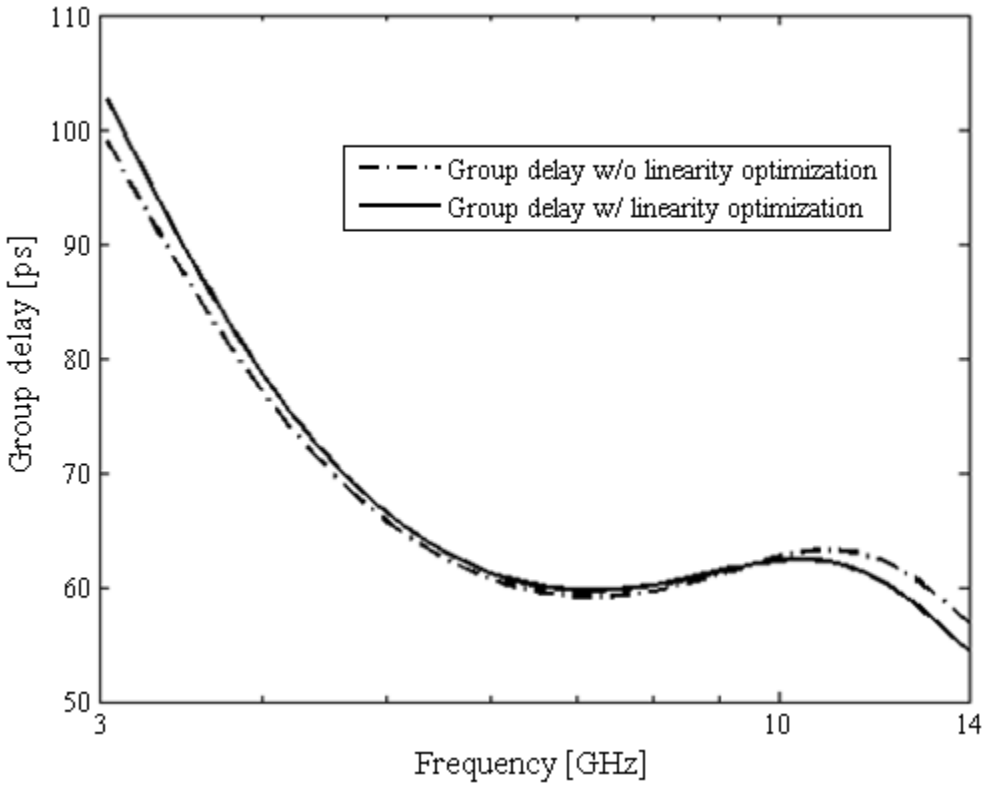

Figure 5.40. Group delay of the LNA with and without linearity improvement over the 3 GHz to 14 GHz band.

5.5.8 Final LNA specifications

The final specifications of both the LNA with and without linearity improvement are given in Table 5.10.

Table 5.10. Final specifications of the 3-14 GHz LNAs designed in the 7WL process.

	BW [GHz]	**S_{11} [dB]**	**S_{21} [dB]**	**NF [dB]**	**IIP3 [dBm]**	**P [mW]**
w/o linearity optimization	3–14	< -10	20.7	2.8–4.3	-22.5 @ 6.5 GHz	14.22
with linearity optimization	3–14	< -9.7	20.1	2.9–4.8	-19.0 @ 6.5 GHz	33.3

5.6 CONCLUSION

Three different LNA designs using the LC-ladder and capacitive shunt-shunt feedback configuration were presented in this chapter. Using the 200 GHz f_T 8HP process in the design for the 1-18 GHz LNA was successful as all the design specifications except P_{1dB}

were met over this very wide frequency band, and even so a good IIP3 of -14.5 dBm was still obtained. The design using the 7WL process also showed good simulations results when considering the much lower f_T of this process.

Although the use of this configuration in a design at 60 GHz produced results comparable to those in literature it was determined not to be the optimal configuration at such high frequencies. This is due to the 57-64 GHz band being a narrow band relative to the 60 GHz centre frequency and as such the wideband design approach is redundant. The mathematical model also does not predict the results accurately when the transistor is operated this close to f_T.

Nonetheless the LC-ladder and capacitive shunt-shunt feedback LNA configuration has proven to be an effective means of implementing very wideband LNAs with good specifications and in many cases improved performance compared to other LNA topologies in literature as shown in Table 1.1 of Chapter 1.

The mathematical model derived in Chapter 4 was also shown to give an accurate description of the LNA performance. Simulated and calculated results showed good correlation in most cases and some comments were made regarding future improvements that could be added to the model to reduce deviations, such as calculating the frequency dependent Q-factor of the inductors to improve the accuracy of noise calculations and also including the effect of the GBP in the gain equations.