3.1   INTRODUCTION

This chapter describes the two integrated circuit processes that were used in the verification of the designed LNAs. Full details of the process design kits (PDKs) cannot be disclosed due to a non-disclosure agreement (NDA) with the foundry; only those details already available in the public domain are given here. Two models commonly used in the simulation of bipolar transistors are also briefly discussed.

The process that was initially selected for the implementation of the LNA is the IBM 8HP[1] 0.13 µm SiGe BiCMOS process available through MOSIS[2]. The process offers HBTs with unity gain frequencies of 200 GHz thus still providing high gain in the Ku-band as well as the low noise characteristics inherent to HBTs as described in Chapter 2, making it ideal for this LNA implementation.

A second IBM process was however used for fabrication of the LNA due to the availability of a run sponsored by MOSIS in the 7WL[3] 0.18 µm SiGe BiCMOS process. This process has an f_T of only 60 GHz. Simulations were nonetheless done using both processes and are discussed in Chapter 5 and as such a summary of the specifications of both processes are given in the following subsections.

Unless otherwise noted all data relating to the 8HP process was taken from [55], [56] and data for the 7WL process from [57], [58]. The maximum power supply voltage for the 8HP process is 1.5 V and for the 7WL process 1.8 V.

3.2   HETEROJUNCTION BIPOLAR TRANSISTORS

Both the 8HP and 7WL technologies offer high performance and high breakdown vertical NPN bipolar transistor variations. Selected electrical parameters of the high performance HBTs are summarized in Table 3.1.

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[1] www.mosis.com/ibm/8hp/
[2] MOSIS is a multi-project wafer (MPW) IC fabrication service provider
[3] www.mosis.com/ibm/7wl/

Table 3.1. High performance HBT electrical parameters.

Parameter	Units	8HP Minimum	8HP Nominal	7WL Minimum	7WL Nominal
β	-	100	600	140	220
f_T (peak)	GHz	180	200	54	60
f_{max}	GHz	-	280	-	280
BV_{CE0}	V	1.5	1.77	2.8	3.3

3.3   HBT MODELS

Two high frequency transistor models commonly used in circuit simulation namely the vertical bipolar inter-company model (VBIC) and the high current model (HICUM) are discussed next.

3.3.1   VBIC – vertical bipolar inter-company model

For BJT simulation the VBIC transistor model included in the 8HP/7WL design kits was used by importing the appropriate model libraries into Spectre RF. The VBIC model is an extended Gummel-Poon model which has been created to overcome the deficiencies of the classic Gummel-Poon model. The large-signal equivalent circuit is shown in Figure 3.1.

The model provides built-in support for the following features [**59**]:

- Parasitic vertical PNP to substrate
- Weak avalanche multiplication (impact ionization)
- Thermal network (dV_{be}/dT)
- Fixed oxide capacitances for the emitter-base and collector-base junctions
- Quasi-saturation modelling
- Improved Early effect modelling (compared to the standard Gummel-Poon model)

The modelling of reverse base-emitter junction breakdown is not included as it is not supported by the VBIC equations. The NPN model in the 8HP process currently also support only one emitter stripe in either a c-b-e-b-c or c-b-e configuration. The 7WL process supports multiple emitters.
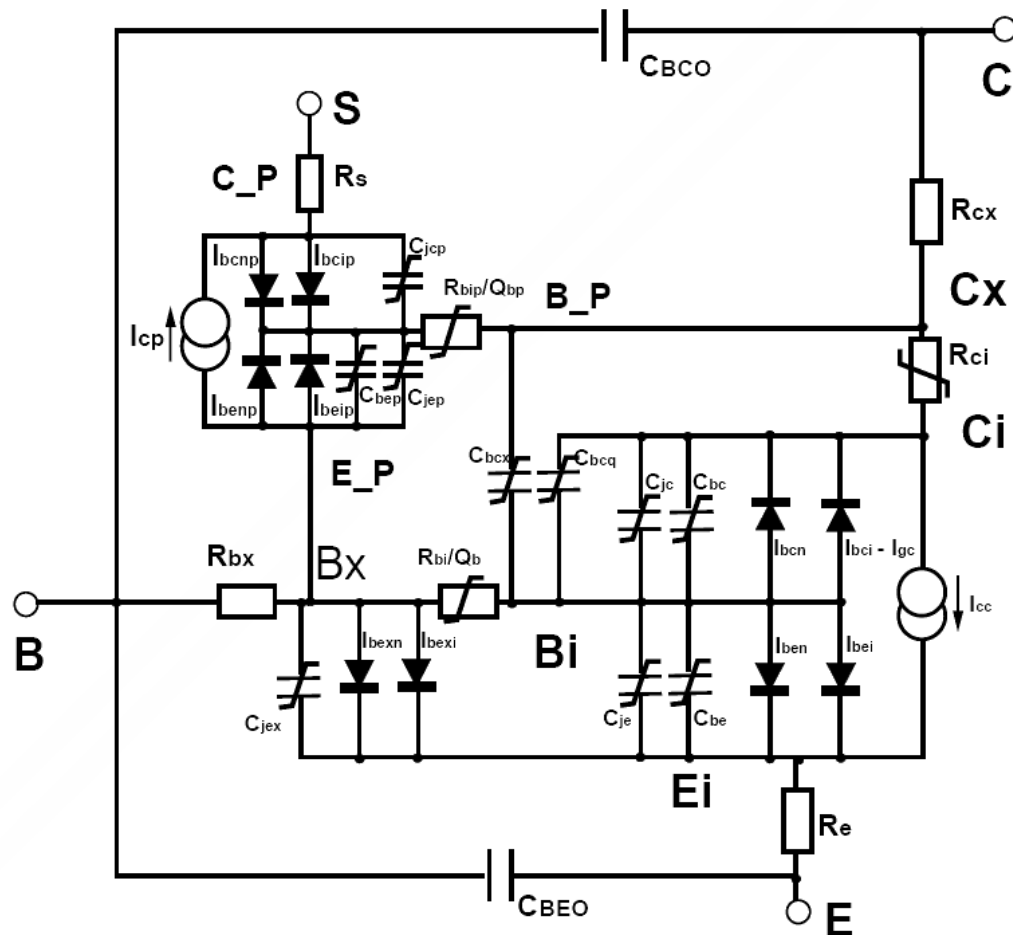
Figure 3.1. Equivalent large-signal circuit of the VBIC transistor model [59]**.**

3.3.2   HICUM – high current model

Although simulations using the HICUM parameters were not done in this study it is referenced in the suggestions for future work and thus described here. The HICUM targets the design of bipolar transistor circuits at high-frequencies and high-current densities using Si, SiGe or III-V based processes.

HICUM is a semi-physical compact bipolar transistor model. Semi-physical means that for arbitrary transistor configurations, defined by emitter size as well as the number and location of base, emitter and collector contacts, a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data (sheet resistances and capacitances per unit area or length etc.) [**60**]. The large-signal equivalent circuit for HICUM/LEVEL2 is shown in Figure 3.2.
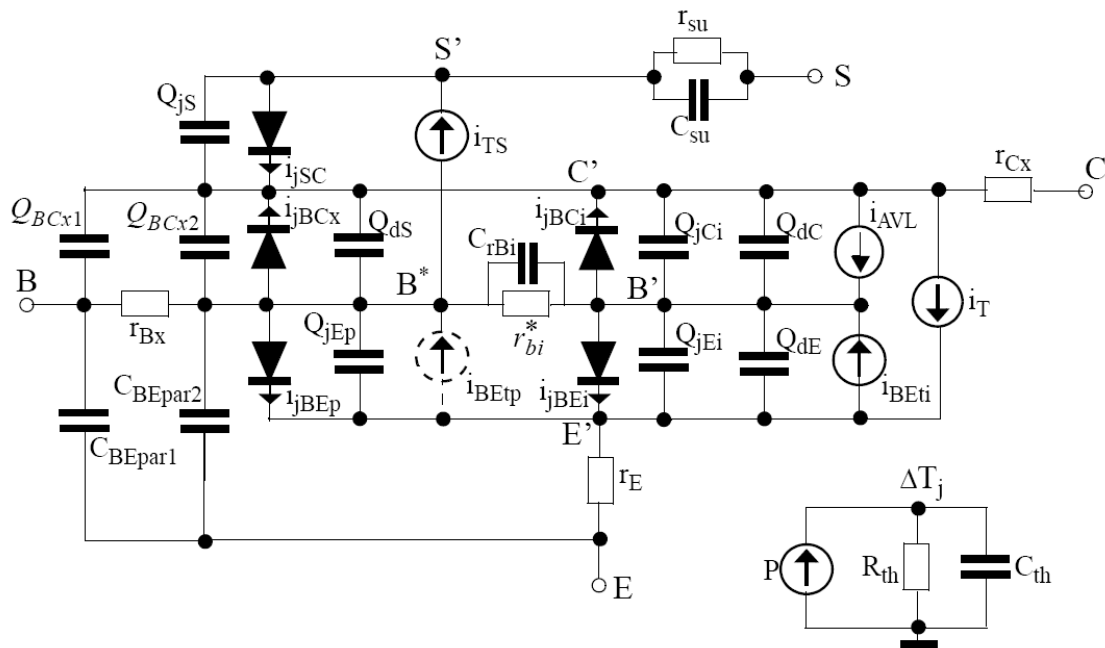
Figure 3.2. Large-signal HICUM/LEVEL 2 equivalent circuit [60].

The important physical and electrical effects taken into account by HICUM/LEVEL2 are [**60**]:

- High-current effects (including quasi-saturation).
- Distributed high-frequency model for the external base-collector region.
- Emitter periphery injection and associated charge storage.
- Emitter current crowding (through a bias dependent internal base resistance).
- Two- and three-dimensional collector current spreading.
- Parasitic (bias independent) capacitances between base-emitter and base-collector terminal.
- Vertical non-quasi-static (NQS) effects for transfer current and minority charge.
- Temperature dependence and self-heating.
- Weak avalanche breakdown at the base-collector junction.
- Tunnelling in the base-emitter junction.
- Parasitic substrate transistor.
- Band-gap differences (occurring in HBTs).
- Lateral (geometry) scalability.

3.4 METAL AND INTERCONNECT LAYERS

Both the 8HP and 7WL processes offer a maximum of seven metal layers. The first five layers of the 8HP process are copper interconnects with two analogue metal aluminium layers. In the 7WL process the first and sixth metal layers are copper and the other layers aluminium. In addition to these layers there is a special metal layer used to create metal resistors and an additional aluminium layer used to form the top plate of metal-insulator-metal capacitors.

3.5 8HP AND 7WL RESISTORS

The 8HP technology provides four types of resistors and the 7WL technology six, realized on different process layers. For a given sheet and contact resistance of the layer in question the resistance is calculated as

$$R = \left(R_S \frac{L}{W} \right) + \left(2 \frac{R_{end}}{W} \right),$$

(3.1)

where:

- R_S = Sheet resistance (Ω/sq)
- R_{end} = End contact resistance (Ω-μm)
- L = Design length from contact to contact
- W = Design width of the mask

Only square and rectangle geometries are supported. Since dog-bone and L-shapes are not supported this places a limit on the minimum dimensions which is larger than the general minimum feature rules.

3.6 CAPACITORS

The 8HP and 7WL processes provide three types of capacitors:

- MOS Varactors (thin or thick oxide MOS capacitor)
- HA varactors (hyper abrupt junction diode varactors)
- Single aluminium metal-insulator-metal (MIM) capacitors

Since the LNA does not require variable capacitance MIM capacitors were used. The 7WL process also has a dual MIM option effectively doubling the capacitance per area.

The nominal capacitance value of a single MIM capacitor can be calculated as

$$C = (C_A \cdot L \cdot W) + (C_P \cdot 2 \cdot (L + W)), \qquad (3.2)$$

where L is the design length and W the design width. The capacitance per area and periphery capacitances are indicated by C_A and C_P respectively. The simulation model includes the parasitic capacitance from the bottom plate of the MIM capacitor to the substrate. This parasitic capacitance depends on the BEOL metallization option (nlev = 5, 6 or 7) and can also be calculated using (3.2) with the appropriate capacitance values.

3.7   INDUCTORS AND TRANSMISSION LINES

The 8HP process supports single layer inductors on the top metal layer. In the 7WL process single layer inductors as well as series or parallel stacked inductors on the two top metal layers are available, however only single layer inductors were used in the this implementation.

At the frequency of interest the inductance and quality factor vary considerably with frequency due to both the turn-to-turn parasitic capacitance and the conductive substrate. The peak Q-factor and corresponding frequency is lower than an equivalent inductor realized in a semi-insulating substrate process such as GaAs. Depending on the inductor design the Q-factor peaks may vary from 500 MHz to 15 GHz with higher frequency peaks occurring for lower values of inductance.

3.7.1   Inductor and RF-line layout considerations

To ensure enough resistance between the spiral and the substrate contacts surrounding it for decoupling, all contacts must be placed at least 80 μm from the spiral. If not the simulation results obtained with the ideal AC ground connection are no longer valid. This rule is also applicable to RF-lines.

Metal areas adjacent to the spiral connected to AC ground will add capacitance in parallel with the inductance lowering the self resonance frequency and large planes or closed loops

of metal will support eddy and loop currents that will lower the peak Q-factor. Apart from other metal layers the bonding pads will also affect inductor performance and C4 solder ball contacts should be spaced at least 110 μm from the spiral and wire bond pads at least 83 μm away to ensure a maximized Q-factor and self resonance frequency.

3.8   BOND PADS

The 8HP and 7WL processes support both wire bond pads as well as C4 pads for ball grid arrays. Wire bond pads were used in the implementation. The typical pad capacitance of the 8HP process is approximately 30 fF and that of the 7WL process approximately 35 fF.

3.9   CONCLUSION

This chapter provided an overview of the IBM 8HP and 7WL IC processes used in the simulation of the proposed circuits. The 7WL process was also used to fabricate a LNA to obtain experimental results as discussed in Chapters 5 through 7.

4.1   INTRODUCTION

The literature study presented in Chapter 2 concluded that a LC-ladder matched amplifier with capacitive shunt-shunt feedback could be a feasible means of implementing a wideband LNA that overcomes many of the shortcomings in existing LNA topologies. To characterise the performance of such a LNA extensive mathematical modelling of this proposed configuration was performed in order to quantify the performance measures important in LNA design [61], [62]. A RF analogue approach was used and the model consists of equations for input impedance, input return loss (S_{11}), forward gain (S_{21}) and NF, as well as an approximation of the IIP3 of the LNA. From this model compact design equations were also derived. The above derivations are presented in this chapter. All mathematical modelling for the research has been done using MATLAB[4].

The simple high frequency small-signal transistor model was used in the derivation and proved to be sufficient for a first order design when calculations were compared to simulation results. In the noise analysis only base resistance thermal noise, and base- and collector current shot noise were considered since flicker noise is negligible above 1 GHz and it was assumed that the base-collector voltage would be small enough to limit avalanche noise. Finally, inductors were modelled consisting of a series inductance and frequency dependent series resistance derived from the inductor Q-factor which was assumed constant over frequency within the band of interest.

4.2   INPUT MATCHING

Since it remains common practice to use a 50 Ω characteristic impedance in RF circuit and antenna design it is required that the LNA have a 50 Ω input impedance (or at least S_{11} < -10 dB) over the entire frequency band. To achieve this wideband operation a fourth order LC-ladder filter is used which allows the realization of an arbitrary wide matched bandwidth [11]. This is combined with the capacitive shunt-shunt feedback technique [12], [45] which is used to synthesize the resistance and capacitance of the series RLC part of the LC-ladder circuit. The circuit diagram of this configuration is shown in Figure 4.1.

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[4] www.mathworks.com

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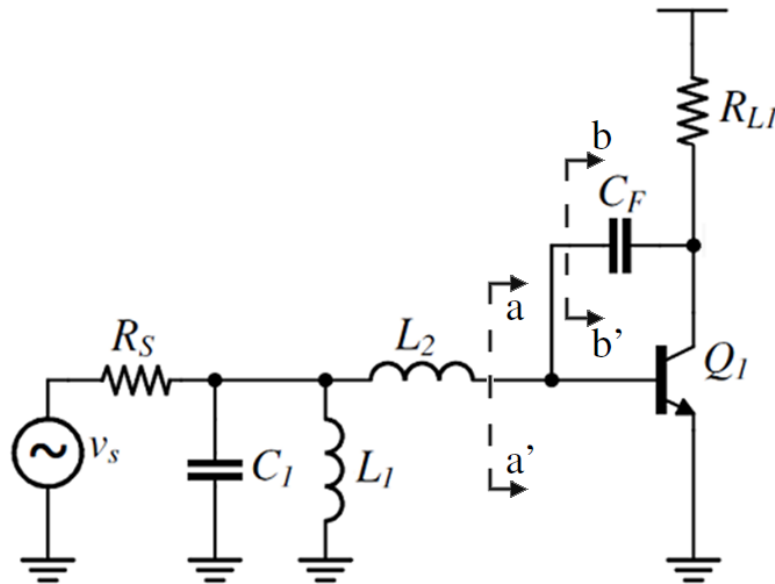YUNIBESITHI YA PRETORIA   Mathematical modelling

Figure 4.1. Schematic of the LC-ladder and capacitive shunt-shunt feedback input matching topology.

4.2.1 LC-ladder network

The LC-ladder consists of four reactive elements shown in Figure 4.2 where C_2 and L_1 determine the lower corner frequency of the matched band and C_1 and L_2 the upper corner frequency. The design of such a network was discussed in Section 2.5.5 and is repeated here for convenience. The appropriate values for these components are given by [11]

$$L_1 \approx \frac{R_S}{2\pi f_L} \quad and \quad C_2 \approx \frac{1}{2\pi f_L R_S} \tag{4.1a}$$

$$L_2 \approx \frac{R_S}{2\pi f_H} \quad and \quad C_1 \approx \frac{1}{2\pi f_H R_S} \tag{4.1b}$$

where R_S is the source resistance and f_L and f_H the lower and upper corner frequencies of the matched bandwidth respectively.
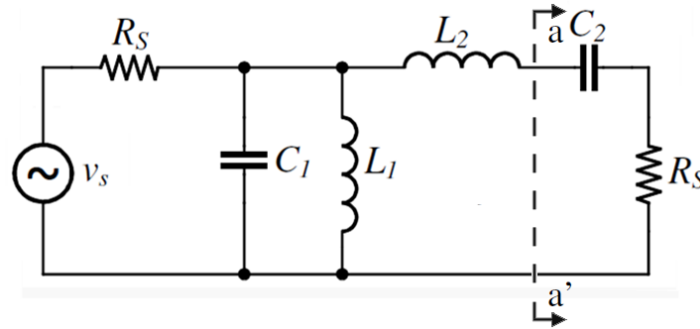
Figure 4.2. Schematic of a fourth order LC-ladder filter [11].

A benefit of using this configuration is that it takes advantage of what would in many cases be regarded as unwanted parasitic components and incorporates them into the matching network. The shunt capacitor C_1 can be implemented as the pad capacitance and in fact often requires an additional MIM capacitor in parallel to attain the required capacitance, thus there is no limitation due to the input pad. The shunt inductor L_1 can in turn be used as the DC bias choke, thus saving one extra on-chip inductor or the need for using an off-chip choke.

The series inductor L_2 is usually relatively small and implemented as a spiral inductor or transmission line depending on the frequency band. The series capacitor C_2 as well as the 50 Ω load resistance is derived from the transistor input impedance as seen when comparing the schematics in Figure 4.1 and Figure 4.2 along the line a-a'.

4.2.2   Capacitive feedback Miller impedance

The use of capacitive feedback to generate a series RC circuit for matching purposes was introduced in [12] as discussed in Section 2.5.4. The equations they provide can be verified using the small-signal circuit looking into the feedback capacitor C_F, and neglecting r_b. This is shown in Figure 4.3, where line b-b' has reference to Figure 4.1.
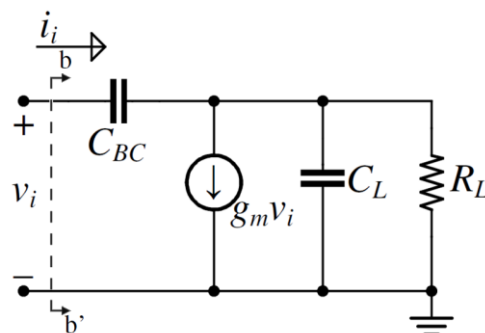

Figure 4.3. Small-signal equivalent of the capacitive feedback circuit when looking into the feedback capacitor.

The input voltage can be written in terms of the input current as

$$v_i = \left(i_i - g_m v_i\right)\left(R_L \left\|\frac{1}{j\omega C_L}\right.\right) + i_i \frac{1}{j\omega C_{BC}} . \tag{4.2}$$

Solving for v_i/i_i results in

$$\frac{v_i}{i_i} = \frac{\dfrac{R_L}{1+j\omega R_L C_L} + \dfrac{1}{j\omega C_{BC}}}{1 + g_m\left(\dfrac{R_L}{1+j\omega R_L C_L}\right)} ,$$
$$= \frac{R_L + \dfrac{1+j\omega R_L C_L}{j\omega C_{BC}}}{1 + g_m R_L + j\omega R_L C_L} \tag{4.3}$$

which when applying the approximation $(1 + g_m R_L) \gg |\omega R_L C_L|$ in the denominator, which is usually the case, becomes

$$Z_M = \underbrace{\frac{1}{j\omega C_{BC}\left(1+g_m R_L\right)}}_{C_M} + \underbrace{\frac{R_L}{1+g_m R_L}\left(1+\frac{C_L}{C_{BC}}\right)}_{R_M} . \tag{4.4}$$

The resulting equivalent circuit at the input of the transistor is thus as shown in Figure 4.4.
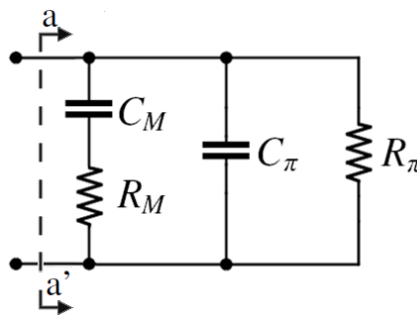

Figure 4.4. Equivalent circuit at the base of the transistor.

Using a successive series-to-parallel and then parallel-to-series transformation of R_M, while combining C_M and C_π, and neglecting R_π which is much larger than R_M results in

$$R_{M,p} = \frac{1}{\omega^2 C_M^2 R_M} \quad and \quad R_{IN} = \frac{1}{\omega^2 (C_\pi + C_M)^2 R_{M,p}} ,$$

$$\Rightarrow \quad R_{IN} = \frac{C_M^2}{(C_\pi + C_M)^2} R_M \tag{4.5}$$

and thus the input impedance is defined as the series combination of

$$C_{IN} = C_\pi + C_M$$
$$= C_\pi + (1 + g_m R_L)(C_\mu + C_F) \tag{4.6}$$

and

$$R_{IN} = \frac{R_L}{(1 + g_m R_L)} \left(1 + \frac{C_L}{C_{BC}} \right) \left(\frac{C_M}{C_\pi + C_M} \right)^2$$
$$\approx \frac{1}{g_m} \left(1 + \frac{C_L}{C_{BC}} \right) . \tag{4.7}$$

Although the conversions in (4.5) use the Q-factor of the capacitor which may change with frequency, conversion first to parallel and then back to series causes the Q-factor to cancel and thus the matching remains constant with frequency. The simplification in (4.7) also shows that the result of the conversion only has a small influence on the equivalent resistance since C_M is usually much larger than C_π.

4.2.3 Input reflection coefficient

With this configuration based on LC-ladder filter theory it is possible, by designing for $R_{IN} = 50\ \Omega$ and $C_{IN} = C_2$, to obtain a 50 Ω input impedance over an arbitrary frequency band. The input reflection coefficient from the definition of S_{11} is then

$$S_{11} = \frac{Z_{IN} - R_S}{Z_{IN} + R_S}, \tag{4.8a}$$

where Z_{IN} is defined as

$$Z_{IN} = j\omega L_1 \left\| \frac{1}{j\omega C_1} \right\| \left(j\omega L_2 + \frac{1}{j\omega C_{IN}} + R_{IN} \right). \tag{4.8b}$$

4.2.4   Comparison to the inductively degenerated LC-ladder technique

The LC-ladder matching technique combined with an emitter degenerated transistor as discussed in Section 2.5.5 had the disadvantage of introducing a pole at the lower corner frequency of the matched bandwidth, causing a -20 dB per decade roll-off in the base-emitter voltage as shown in (2.36) which has to be corrected by using an inductive load.

Since the emitter inductor is used to synthesize the series resistance, v_{be} is the voltage being evoked by the input current across the capacitor in the equivalent series RLC circuit which is the base-emitter capacitance C_π. The roll-off is due to the decreasing impedance of the capacitor with frequency.

In contrast, this roll-off is not present when combining the LC-ladder with capacitive feedback. In this case v_{be} is the voltage evoked across the input impedance of the transistor which includes both the capacitor and the resistor in the equivalent RLC circuit. When the current flowing into the transistor is approximated as $v_S/(2R_S)$ over the band of interest as before, the voltage over the v_{be} junction now becomes

$$
\begin{aligned}
v_{be} &= \frac{v_s}{2R_s}\left(R_s + \frac{1}{j\omega C_2}\right) \\
&= \frac{v_s}{2}\left(\frac{j\omega R_s C_2 + 1}{j\omega R_s C_2}\right) \\
&= \frac{v_s}{2}\left(\frac{j\frac{\omega}{\omega_L} + 1}{j\frac{\omega}{\omega_L}}\right)
\end{aligned}
\qquad (4.9)
$$

Thus the base-emitter voltage is a decreasing function at -20 dB per decade from infinity to a corner at -6 dB at the lower cut-off frequency, from where the zero results in a constant voltage drop over the base-emitter junction with frequency.

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4.3 GAIN EQUATIONS

4.3.1 Input matching network gain

To determine the gain of the input matching network a Norton and Thévenin equivalent transformation can be used to move the source voltage in series with the rest of the RLC circuit at the transistor input. To this end the impedances

$$Z_1 = R_{L1} + j\omega L_1 \tag{4.10a}$$

$$Z_2 = R_{L2} + j\omega L_2 \tag{4.10b}$$

were defined where L_1 and L_2 are the inductors in the LC-ladder network, and R_{L1} and R_{L2} the associated parasitic series resistance; as well as

$$Z_s = \frac{1}{\dfrac{1}{R_s} + \dfrac{1}{R_{L1} + j\omega L_1} + j\omega C_1} \tag{4.11}$$

which is the parallel combination of R_S, L_1 and C_1.

A Norton equivalent transformation of v_s and R_S to find i_s and then a Thévenin transformation with i_s and Z_S results in the series source voltage

$$v_{s,eq} = \frac{Z_s}{R_s} v_s \tag{4.12}$$

and source impedance of Z_S. The voltage gain of the input matching network can then be defined as

$$A_{v,in} = \frac{Z_s}{R_s} \cdot \frac{Z_{T,IN}}{Z_s + Z_2 + Z_{T,IN}}, \tag{4.13}$$

where $Z_{T,IN}$ is the impedance at the base of the transistor derived from (4.6) and (4.7) as

$$Z_{T,IN} = R_{IN} + \frac{1}{j\omega C_{IN}}. \tag{4.14}$$

4.3.2 First stage gain

Since the first amplifier stage is a common-emitter configuration without emitter feedback the voltage gain is defined as

$$A_{v,1} = G_{M1} \cdot Z_{L1} \tag{4.15}$$

with G_{M1} the transconductance gain and Z_{L1} the load impedance. From inspection of Figure 4.1 the transconductance and load impedance are given respectively by

$$G_{M1} = g_m - j\omega C_{BC} \tag{4.16a}$$

$$\begin{aligned} Z_{L1} &= R_L \Big\| \frac{1}{j\omega(C_{BC} + C_L)} \\ &= \frac{R_L}{1 + j\omega R_L(C_{BC} + C_L)} \end{aligned} \tag{4.16b}$$

Several factors make this gain frequency dependent. The relatively large feedback capacitance, typically 85 fF $< C_{BC} <$ 150 fF, causes the feedback factor to increase as the impedance of the capacitor decreases with frequency, thus decreasing the transconductance gain. However this effect is often negligible since a typical collector current of 1.5 mA with typical a feedback capacitor value of 100 fF and a 100 Ω load results in only a 2 dB drop in voltage gain from 1 GHz to 20 GHz.

A more important consideration is the output pole of the amplifier. The transfer function of the input matching network has been shown to be approximately constant over the band of interest and thus there is a single dominant pole at the output of the amplifier given by

$$\omega_{Po} = \frac{1}{R_L(C_{BC} + C_L)}. \tag{4.17}$$

Due to the increased capacitance with the addition of the feedback capacitor as well as the relatively large R_L required for large gain the pole is often within the band of interest resulting in a -20 dB per decade roll-off in the frequency response of the gain.

Even if this is not the case, the gain-bandwidth product (GBP) or f_T of the transistor will often not allow large gain for operation up to frequencies as high as 20 GHz. Even though further gain can be provided by subsequent stages the value of C_F affects the NF at the high frequency end and as such high gain in the first stage is desirable to minimize this value. If the gain is higher than f_T/f_H there will be a -20 dB per decade roll-off of gain regardless of the position of the output pole.

4.3.3   Second stage gain and gain flattening

To equalize the gain of the amplifier and compensate for the gain roll-off of the first amplifier stage which is often present as discussed above an inductive load can be used to provide peaking at high frequencies. Since a second amplifier stage is usually required to realize the desired gain at high frequencies, the inductive load can be used in the second stage to not add additional complexity to the mathematical model of the first stage from which the design equations are derived. Where necessary this peaking can be limited by also including a resistor in parallel with the inductive load. The schematic of the second stage is included in Figure 4.5.
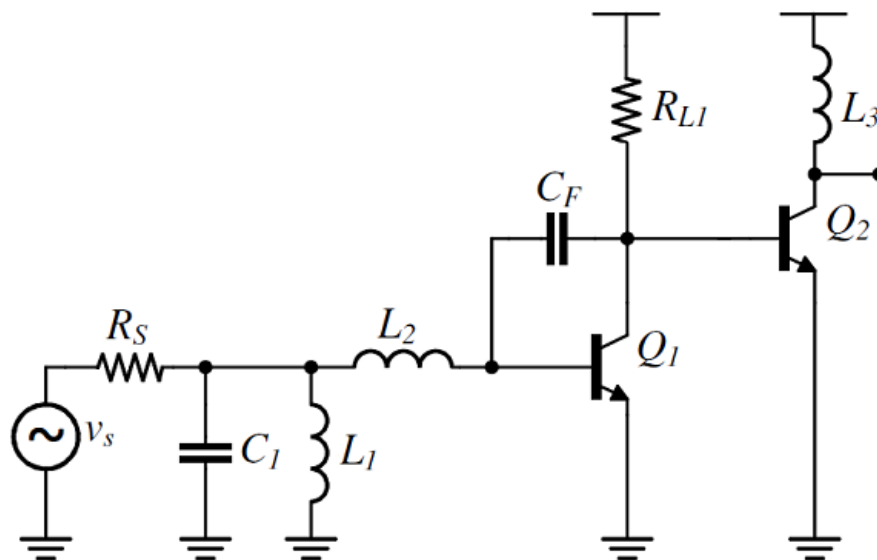

Figure 4.5. Schematic of the LNA including the second amplifier stage used to generate a zero in the frequency response for pole-zero cancellation.

The gain of the second stage is given by

$$A_{v,2} = G_{M2} \cdot Z_{L2} \tag{4.18}$$

where G_{M2} is simply the transconductance gain of the transistor, g_{m2}, and the load impedance is given by

$$Z_{L2} = j\omega L_3.$$ (4.19)

The overall gain of the LNA is then

$$A_{v,T} = A_{v,in} \cdot A_{v,1} \cdot A_{v,2}$$ (4.20)

and can be expressed in terms of the scattering parameter S_{21} as

$$S_{21} = 2A_{v,in} \frac{(g_{m1} - j\omega C_{BC})R_{L1} \cdot (j\omega L_3 g_{m2})}{1 + j\omega R_{L1}(C_{BC} + C_{L1})}.$$ (4.21)

Since the frequency dependence of the first stage transconductance can usually be neglected, a flat wideband gain response can be achieved by the cancellation of the pole and zero in the equation. The bandwidth of the amplifier is then determined solely by the gain of the input matching network, $A_{v,in}$.

4.3.4   Further gain stages

The LNA configuration of Figure 4.5 provides wideband conjugate input matching as well as gain with a flat frequency response. Depending on the transistor process that is used it might however not be possible to achieve the desired gain specification. In such a case additional common-emitter stages employing resistive loads may be added to increase the overall gain further [62].

4.4   LNA DESIGN EQUATIONS

From the equations discussed thus far it is possible to derive compact design equations for a LNA using this configuration for a given frequency band and gain specification [62].

The design of the first stage entails selection of the LC-ladder components, the collector current of Q_1, the load resistance R_{L1} and the feedback capacitance C_F. The equivalent resistance at the base of the transistor is also affected by C_{L1}, but the value of this

capacitance should always be minimized to maximize the output pole frequency discussed in Section 4.3.2, and as such is not available for setting the input resistance.

The frequency specification for the LNA is met through selection of the reactive elements in the LC-ladder input matching network, and these values are determined using (4.1a) and (4.1b).

With the bandwidth determined, the voltage gain of the first stage should be selected, ideally as f_T/f_H to achieve the maximum gain up to the upper corner frequency f_H. Once this value of $A_{v,1}$ is selected the feedback capacitance required to synthesize C_2 can be determined by rewriting (4.6) as

$$C_F = \frac{C_2 - C_{\pi 1}}{1 + A_{v,1}} - C_{\mu 1},$$ (4.22)

where A_{v1} has been approximated as $g_{m1}R_{L1}$.

The input resistance of the first stage, which should be equal to 50 Ω to provide proper matching, has been defined in (4.7). If $g_{m1}R_{L1} >> 1$, which is usually the case, this equation can be simplified to

$$R_{IN} \approx \frac{1}{g_{m1}}\left(1 + \frac{C_L}{C_{BC}}\right),$$ (4.23)

when also noting that C_M is usually in the hundreds of femtofarads or even the picofarad range while C_π is a few tens of femtofarads and thus $C_M + C_\pi \approx C_M$.

Once the load capacitance is determined, being the total node capacitance at the output excluding C_F, the value of I_{C1} can be derived from (4.23) as

$$I_{C1} \approx \left(1 + \frac{C_L}{C_{BC}}\right)\frac{V_T}{R_S}.$$ (4.24)

While C_L would usually be much smaller than C_{BC} resulting in the familiar $I_{C1} \approx g_m V_T$ the load capacitance can be increased to maintain the desired input matching even when I_{C1}

has been increased to improve the noise performance (see Section 5.3.2) which makes the ratio of the capacitances significant.

Finally the value of R_{L1} is derived from the selected voltage gain and collector current as

$$R_{L1} = A_{v,1} \frac{V_T}{I_{C1}}. \tag{4.25}$$

In the design of the second amplifier stage there is more freedom in the selection of the collector current and the load inductance L_3. Once the gain required at the upper corner frequency has been determined, which is the deficit in gain between the upper and lower corner of the first stage, this can be substituted in (4.18) along with ω_H. The value of L_3, and thus chip area, can then be traded with the collector current, which translates to power consumption, in order to achieve this gain.

4.5 INPUT MATCHING MODELLING IMPROVEMENT

The impedance seen at the base of the transistor has been defined in (4.14) based on the input resistance and capacitance from (4.6) and (4.7) respectively derived from the small-signal analysis of the circuit in Figure 4.3. However when the calculated and simulated input reflection coefficients were compared it was found that they do not track each other sufficiently. This is due to the simple case of a constant load resistance and capacitance being used in the derivation of the transistor input impedance, where the inductive load of the second stage in fact results in a second order equation for load impedance [63].

The input impedance of the second stage is defined as

$$Z_{IN,2} = R_{\pi 2} \left\| \frac{1}{j\omega C_{\pi 2}} \right\| Z_{M2}, \tag{4.26}$$

where Z_{M2} is the Miller impedance, and using the Miller theorem $Y_{IN,2}$ can be written as

$$Y_{IN,2} = \frac{1}{R_\pi} + j\omega\left[C_\pi + C_\mu\left(1 - A_{v,2}\right)\right]$$

$$= \frac{1}{R_\pi} + j\omega\left[C_\pi + C_\mu\left(1 + j\omega L_3 g_{m2}\right)\right]. \tag{4.27}$$

$$= \frac{1}{R_\pi} + j\omega\left(C_\pi + C_\mu\right) - \omega^2 g_{m2} L_3 C_\mu$$

Thus the load impedance of the first stage, Z_{L1}, should instead be defined as

$$Z_{L1} = R_{L1} \| Z_{IN,2} \| \frac{1}{j\omega\left(C_{BC} + C_L\right)}. \tag{4.28}$$

The same small-signal derivation can then be used to define the first stage input impedance more accurately by replacing R_L and C_L in Figure 4.3 with Z_{L1} which results in

$$v_i = \left(i_i - g_m v_i\right) Z_{L1} + i_i \frac{1}{j\omega C_{BC}}$$

$$\Rightarrow \quad Z_{T,IN} = \frac{Z_{L1} + \dfrac{1}{j\omega C_{BC}}}{1 + g_m Z_{L1}}. \tag{4.29}$$

Although the simple case is sufficient and convenient in the initial design, the derivation of $Z_{T,IN}$ in (4.29) should be used in (4.13) to determine the gain of the input matching network, and Z_{L1} in (4.28) should also be used to calculate the first stage gain in (4.15). This leads to the calculated results tracking simulation results sufficiently.

4.6 NOISE FIGURE DERIVATION

As mentioned in Section 2.3.3 NF can either be expressed in terms of a deviation from the minimum NF of a transistor according to the deviation of the source impedance from the optimal noise impedance, which is often used in a distributed design, or an equation incorporating the noise from all the various noise sources in the circuit can be derived. Since the LNA topology in question is designed using a lumped element or RF analogue approach the latter option is more suited in this case, and it will also be shown that important insights regarding optimization for low noise can be gleaned from the derived NF equation which would not be as obvious if a distributed design approach was followed.

4.6.1 Noise sources

The schematic in Figure 4.6 includes all the noise sources of the first amplifier stage. The parasitic resistances of the inductors are given by

$$R_x = \frac{\omega L_x}{Q_x},$$
(4.30)

where Q_x is the quality factor of the passive on-chip inductor and the subscript denotes the inductor in question. The thermal noise contributed by these parasitic resistors, the transistor base resistance r_b, as well as the noise from the source resistance is determined by (2.2a). The transistor current noise sources i_B and i_C are both due to shot noise and given by (2.3).

Although the NF equation could be derived directly from this circuit, the analysis is complicated by the presence of the feedback capacitance as well as the R_S and R_1 noise sources which form part of the parallel RLC circuit. Thus there is no convenient way to translate all the noise sources to the input necessitating certain transformations to a more suitable equivalent circuit.
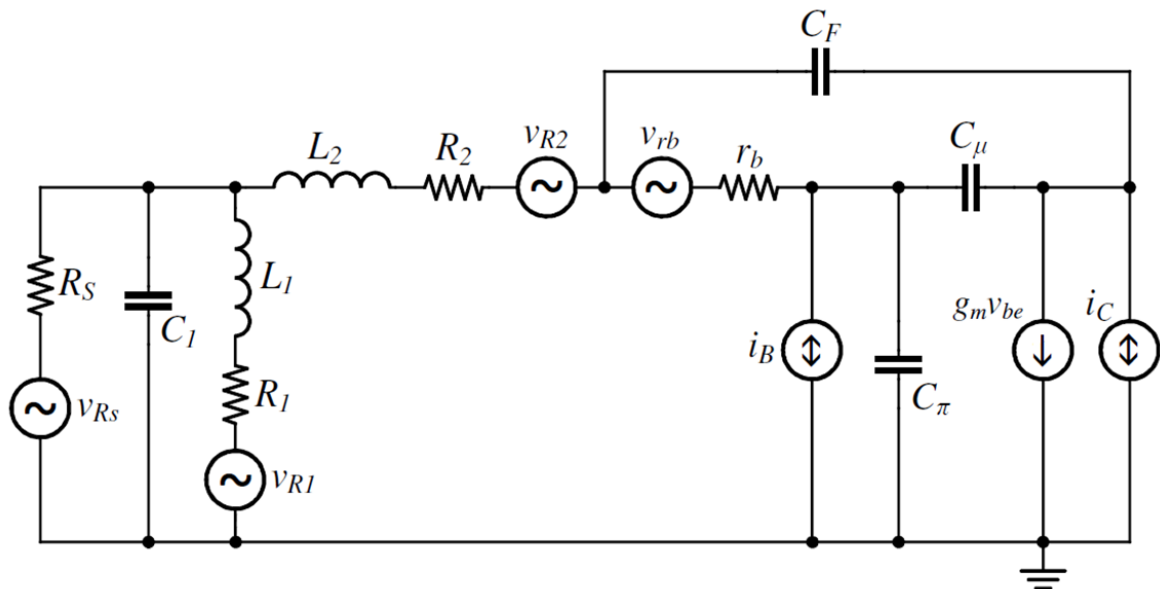

Figure 4.6. Equivalent circuit of the first amplification stage showing parasitic components and noise sources.

4.6.2   Simplifying the circuit

The first simplification that can be made is viewing the transistor as a noise free amplifier with the well known equivalent common-emitter noise generators given by [**29**] and (2.15):

$$
\begin{aligned}
\overline{v_{CE}^2} &= 4kTr_b + \frac{2qI_C}{g_m^2} + \frac{2qI_C}{\beta_0}\cdot r_b^2 \\
&\approx 4kTr_b + \frac{2qI_C}{g_m^2}
\end{aligned}, \tag{4.31}
$$

$$
\begin{aligned}
\overline{i_{CE}^2} &= \frac{2qI_C}{\beta_0} + \frac{2qI_C}{\beta_{RF}^2} \\
&= 2qI_C\left(\frac{1}{\beta_0} + \left(\frac{\omega(C_\pi + C_\mu)}{g_m}\right)^2\right).
\end{aligned} \tag{4.32}
$$

The shunt-shunt feedback due to the capacitor has no effect on the noise voltage of the transistor, however v_{CE} induces an additional noise current in the feedback network [**26**] which results in the final equivalent noise generators at the base of the noise free amplifier being defined as

$$
\overline{v_{EQ}^2} \approx \overline{v_{CE}^2}, \tag{4.33}
$$

$$
\overline{i_{EQ}^2} \approx \overline{i_{CE}^2} + \left(\omega^2 C_F^2\right)\overline{v_{CE}^2}. \tag{4.34}
$$

The schematic can then be redrawn as in Figure 4.7. In this schematic the source noise generator and the noise generator of the L_1 parasitic resistance has also been moved in series with the various impedances and other noise voltage sources. This was done by first using a Norton and then Thévenin transformation on respectively v_{RS}, R_S and Z_S, as well as v_{R1}, Z_1 and Z_S, with Z_1 defined in (4.10a). Thus the PSD of the equivalent noise generators are given by

$$
\overline{v_{RS,eq}^2} = \frac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2} \quad \text{and} \quad \overline{v_{R1,eq}^2} = \frac{|Z_S|^2}{|Z_1|^2}\overline{v_{R1}^2}. \tag{4.35}
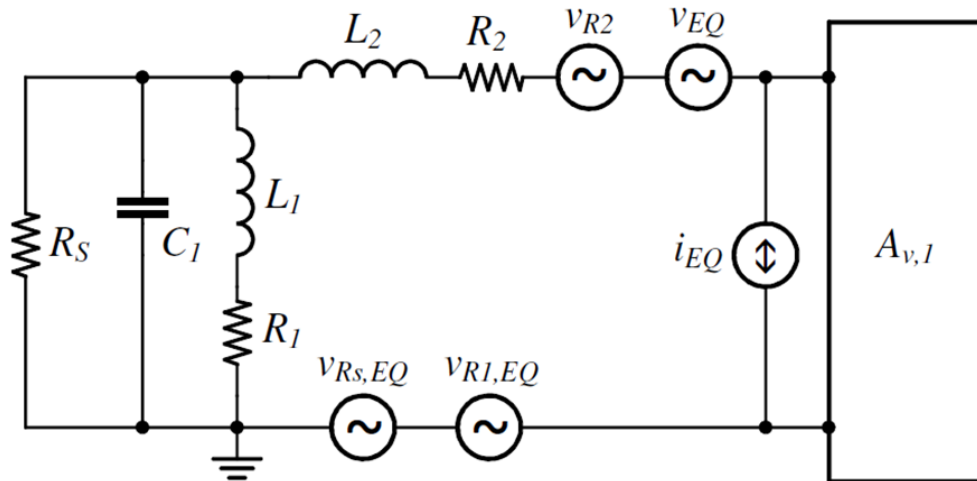$$

Figure 4.7. Equivalent circuit of the first amplification stage redrawn to allow convenient NF derivation.

4.6.3   Noise figure equation derivation

The NF can be conveniently derived from the circuit in Figure 4.7 by first expressing the noise voltage generated over the v_{be} junction of the transistor by each noise generator. In Figure 4.7 this is the voltage over the input terminals of the noise free amplifier. The input impedance of the amplifier is the input impedance of the transistor in parallel with C_F since the output of the amplifier is shorted to ground in the definition of NF.

It has already been shown in Section 2.5.2 that R_π becomes negligible compared to C_π in the SHF range. Thus the input impedance of the transistor is the base resistance in series with the total input capacitance $C_i = C_\pi + C_\mu$. As the impedance of C_i drops at high frequencies a greater portion of the input voltage will fall across r_b decreasing the voltage gain by introducing a pole as seen from

$$v_{be}^{'} = \frac{1/j\omega C_i}{r_b + 1/j\omega C_i}$$
$$= \frac{1}{1 + j\omega C_i r_b} . \qquad (4.36)$$

However for a typical C_i of 100 fF and a base resistance of less than 50 Ω this pole is above 30 GHz and as such r_b can be neglected, resulting in an input impedance consisting simply of the total input capacitance of the amplifier which is

$$C_T = C_\pi + C_\mu + C_F. \tag{4.37}$$

Using a simple voltage divider equation the noise PSD at the v_{be} junction contributed by each voltage noise generator is then defined as

$$\overline{v_{\pi,Veq}^2} = \left| \frac{\frac{1}{j\omega C_T}}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{v_{EQ}^2}, \tag{4.38a}$$

$$\overline{v_{\pi,RL2}^2} = \left| \frac{\frac{1}{j\omega C_T}}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{v_{RL2}^2}, \tag{4.38b}$$

$$\overline{v_{\pi,RL1}^2} = \frac{|Z_s|^2}{|Z_1|^2} \left| \frac{\frac{1}{j\omega C_T}}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{v_{RL1}^2}, \tag{4.38c}$$

and

$$\overline{v_{\pi,RS}^2} = \frac{|Z_s|^2}{R_s^2} \left| \frac{\frac{1}{j\omega C_T}}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{v_{RS}^2}. \tag{4.38d}$$

The voltage noise contribution of the current noise generator is the product of the current noise PSD and the impedance seen by this source, namely the parallel combination of the amplifier input impedance and the matching network, given by

$$\overline{v_{\pi,Ieq}^2} = \left| \frac{1}{j\omega C_T} \| (Z_s + Z_2) \right|^2 \overline{i_{EQ}^2}$$

$$= \left| \frac{\frac{1}{j\omega C_T}(Z_s + Z_2)}{Z_s + Z_2 + \frac{1}{j\omega C_T}} \right|^2 \overline{i_{EQ}^2}. \tag{4.39}$$

Z_2 and Z_S has been defined in (4.10b) and (4.11) respectively.

The noise factor of the first stage can now be defined as

$$F_1 = \frac{\overline{v_{\pi,Veq}^2} + \overline{v_{\pi,Ieq}^2} + \overline{v_{\pi,R1}^2} + \overline{v_{\pi,R2}^2} + \overline{v_{\pi,RS}^2}}{\overline{v_{\pi,RS}^2}}, \tag{4.40}$$

and with the substitution of (4.38a–d) and (4.39), as well as (4.33) and (4.34) the noise factor becomes

$$F_1 = \frac{\overline{v_{EQ}^2} + |Z_S + Z_2|^2 \overline{i_{EQ}^2} + \dfrac{|Z_S|^2}{|Z_1|^2}\overline{v_{R1}^2} + \overline{v_{R2}^2} + \dfrac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2}}{\dfrac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2}}$$

$$= 1 + \frac{\overline{v_{CE}^2} + |Z_S + Z_2|^2 \left[\overline{i_{CE}^2} + |\omega C_F|^2 \overline{v_{CE}^2}\right] + \dfrac{|Z_S|^2}{|Z_1|^2}\overline{v_{R1}^2} + \overline{v_{R2}^2}}{\dfrac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2}}. \tag{4.41}$$

The NF is simply defined as the noise factor expressed in dB [**29**] and thus becomes

$$NF_1 = 10\log F_1. \tag{4.42}$$

4.7   IMPROVING NOISE FIGURE AND GAIN

From (4.41) it is seen that the NF is to a large extent determined by passive components that make up the matching network and first amplifier stage. Therefore reducing the NF would entail optimizing these component values, but from the design steps given in Section 4.4 there is apparently little freedom in this selection. However this is not entirely the case.

The primary concern when changing the component values in the matching network is that the S_{11} specification would no longer be met; however, solving the standard definition of S_{11} in (4.8a), with a 50 Ω source resistance, it is found that the input impedance can vary from 26 Ω to 96 Ω while still maintaining $S_{11} < $ -10 dB. This allows for some freedom in

the selection of these component values. In addition, since there is a strong interaction between the reactive elements the effects of these changes tend to cancel one another.

This makes it possible to optimize the performance of the LNA by modifying the passive component values through simulation after the initial design is completed [**13**].

4.7.1 Noise figure improvement

In order to improve the NF it is valuable to know which of the noise generators dominate the overall NF. To this end (4.41) can be rewritten as

$$
F_1 = \frac{\left(1 + |Z_S + Z_2|^2 \cdot |\omega C_F|^2\right)\overline{v_{CE}^2} + |Z_S + Z_2|^2 \overline{i_{CE}^2} + \left|\dfrac{Z_S}{Z_1}\right|^2 \overline{v_{R1}^2} + \overline{v_{R2}^2} + \left|\dfrac{Z_S}{R_S}\right|^2 \overline{v_{RS}^2}}{\left|\dfrac{Z_S}{R_S}\right|^2 \overline{v_{RS}^2}} . \qquad (4.43)
$$

Inspection of the numerator of (4.43) shows that each noise generator in Figure 4.7 is present only once and each as a separate term with a coefficient comprised of the matching network passive components. Thus it is possible to plot each noise contribution separately and thus determine the dominant contributor. Such a plot is shown in Figure 4.8, which also includes the noise contribution of the second amplifier stage.

To derive this contribution it is convenient to calculate the total current noise at the input of the second stage, since the first transistor is treated as a transconductance amplifier, and then divide that by the transconductance gain of the first stage to get the equivalent voltage noise at the base of the first transistor. The noise generators of the second stage are the first stage load resistance thermal noise PSD as defined in (2.2b), the common-emitter current noise, and the current noise PSD evoked in the equivalent admittance seen by the common-emitter voltage noise generator as show in

$$
n_{A2} = \frac{\overline{i_{RL1}^2} + \overline{i_{CE2}^2} + \overline{v_{CE2}^2} \cdot |1/R_{L1} + j\omega(C_{BC} + C_{IN2})|^2}{|G_{M1}|^2} . \qquad (4.44)
$$

The dominant noise generator was found to be the common-emitter voltage noise and as such minimizing this contribution has priority. To determine how this can be achieved the noise factor equation in (4.43) can be rewritten again to obtain

$$F_1 = \left[\left(\frac{1}{|Z_S|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \cdot |\omega C_F|^2 \right) \overline{v_{CE}^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \overline{i_{CE}^2} + \frac{\overline{v_{R1}^2}}{|Z_1|^2} + \frac{\overline{v_{R2}^2}}{|Z_S|^2} + \frac{\overline{v_{RS}^2}}{R_S^2} \right] \cdot \frac{R_S^2}{v_{RS}^2} , \quad (4.45)$$
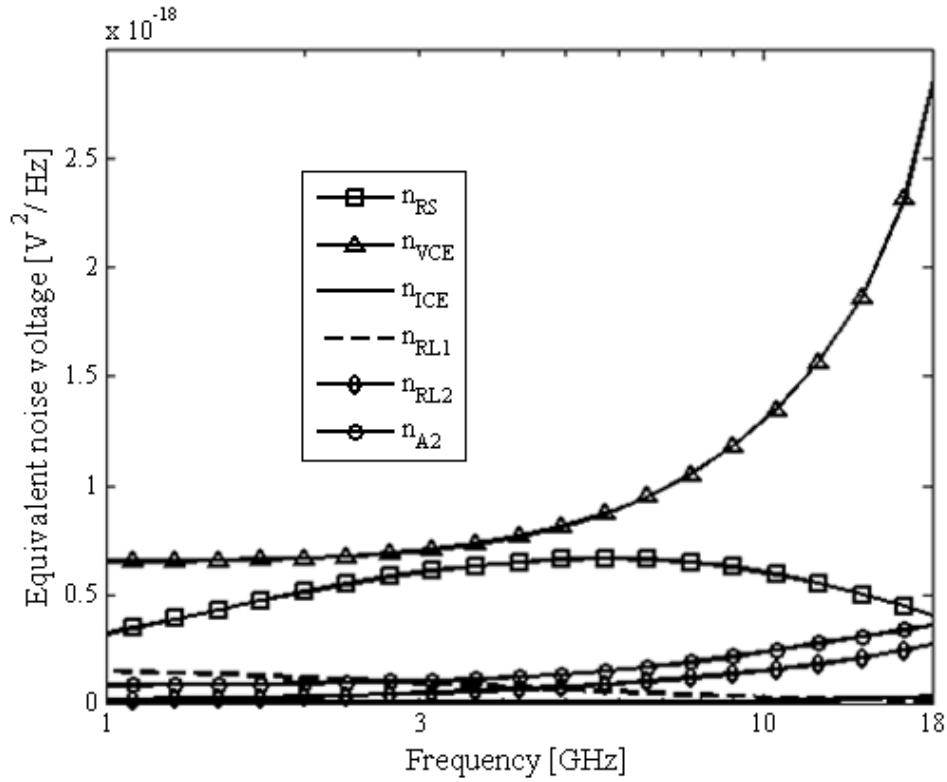

Figure 4.8. Noise PSD contribution of the individual noise generators versus frequency over the 800 MHz to 18 GHz band.

where only the fixed R_S and subsequently fixed v_{RS} is not included in the individual coefficients. The CE voltage noise contribution can then be minimized by minimizing

$$
\begin{aligned}
n_{Vce} &= \left(\frac{1}{|Z_S|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \cdot |\omega C_F|^2 \right) \frac{\overline{v_{CE}^2}}{v_{RS}^2} \cdot R_S^2 \\
&= \left(\frac{1}{|Z_S|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \cdot |\omega C_F|^2 \right) \left(\frac{4kTr_b + 2qI_C / g_m^2}{4kTR_S} \right) \cdot R_S^2 , \\
&= \left(\frac{1}{|Z_s|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 \cdot |\omega C_F|^2 \right) \left(r_b + \frac{V_T}{2I_C} \right) \cdot R_S
\end{aligned} \qquad (4.46)
$$

where (4.31) has been substituted for the CE voltage noise PSD.

Figure 4.8 also shows that the inductors in the input matching network, L_1 and L_2, contribute somewhat at the low and high frequency end respectively, while the amplifier current noise and the second stage practically makes no contribution.

Thus to minimize the NF of the LNA according to (4.46), and in fact throughout (4.45), Z_S should be minimized. From (4.11) this implies increasing L_1 and decreasing C_1. Increasing L_1 will also decrease the contribution of the parasitic resistance of this inductor as seen from

$$
\begin{aligned}
n_{RL1} &= \frac{1}{\left|Z_1\right|^2} \frac{\overline{v_{R1}^2}}{v_{RS}^2} R_S^2 \\
&= \frac{1}{\left|R_1 + j\omega L_1\right|^2} \frac{R_1}{R_S} R_S^2 \\
&= \frac{R_1}{R_1^2 + \omega^2 L_1^2} R_S \\
&= \frac{\omega L_1 / Q_1}{\omega^2 L_1^2 / Q_1 + \omega^2 L_1^2} R_S \\
&= \frac{R_S}{\omega L_1 \left(1 + Q_1\right)}
\end{aligned}
\qquad (4.47)
$$

Decreasing L_2 will decrease (4.46) through Z_2, as well as the contribution from the CE current PSD, and will also decrease R_2 and subsequently its noise PSD.

The final passive component found in (4.46) is the feedback capacitor C_F which causes the NF to increase rapidly at high frequencies and should thus be minimized. Since C_F is used to synthesize C_2 this would mean a decrease in the value of C_2 as well; but although some deviation in C_2 can be allowed, C_F often remains too large to achieve suitable performance at high frequencies. In such a case the gain of the first stage needs to be increased; the gain is however limited by the f_T of the transistor. Fortunately since an inductive load is used in the second stage the high frequency peaking provided by the inductor can compensate for the voltage roll-off of the first stage should the gain be increased above this limit, thus allowing smaller values of C_F to be used. Since C_2 determines the lower corner frequency of the LNA, the decrease in this Miller capacitance with the gain roll-off at high frequencies does not severely affect the input matching and although S_{11} is increased as a result, it can still be kept below -10 dB.

The transistor size and biasing also affects the NF through the second term of (4.46). It is clear that increasing the first stage collector current will decrease the CE voltage noise contribution. Although this may increase the CE current noise, Figure 4.8 indicates that this contribution is generally negligible and thus a small increase will not be significant. Maximizing the emitter length of the transistor will also minimize r_b. The large emitter length results in large C_π and C_μ parasitic capacitance, however since these are included in the design equations this will not be to the determent of the LNA performance and in fact merely results in a smaller feedback capacitance being required which is the desired case.

It has been noted in Section 4.2.2 that the collector current is used to determine the equivalent input resistance at the base of the transistor and as such increasing I_C to reduce noise will worsen input matching. The first stage load capacitance can however be increased to restore the input matching while also lowering the output pole of the first stage; however this is usually not a significant problem while the inductively loaded second stage can still equalize the voltage gain.

Figure 4.9 shows the noise contributions of the respective generators after the suggestions above have been applied to a typical LNA. The contribution of the parasitic resistance R_2 has been reduced by one third at the upper cut-off frequency and the contribution of R_1 is also somewhat reduced.
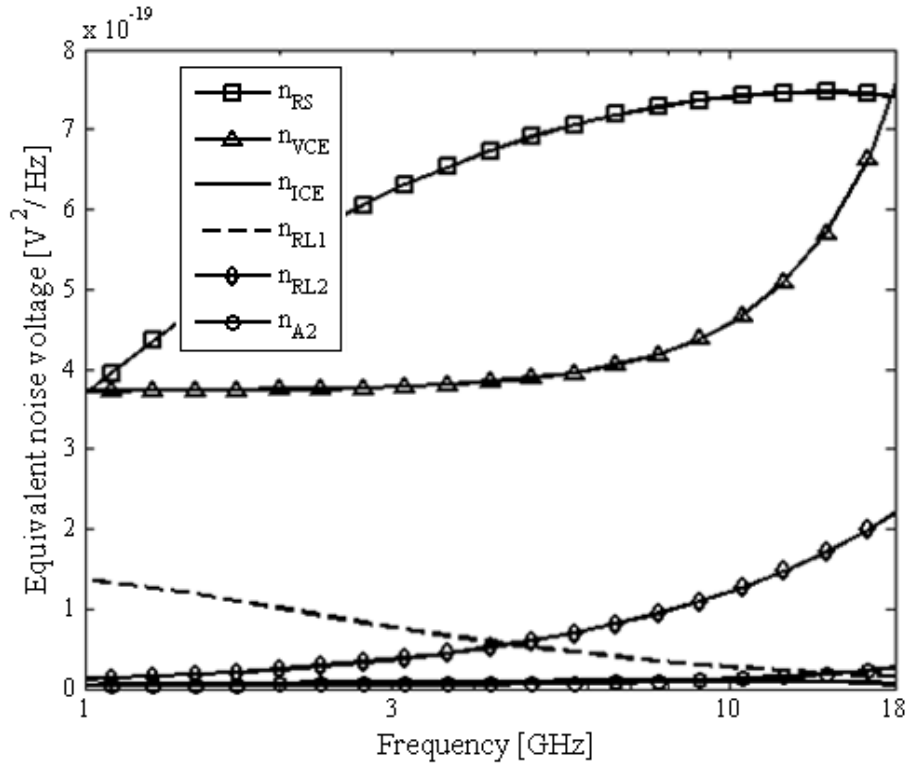
Figure 4.9. Noise PSD contribution of the individual noise generators versus frequency after optimization of the input matching network.

The transistor voltage noise contribution has been increased at high frequencies, however it can be seen that there is still a large improvement in NF resulting from the source resistance noise, and thus also the input signal, undergoing a larger gain through the matching network. This serves to improve the output signal-to-noise ratio which implies a lower NF.

4.7.2 Simultaneous gain improvement

The overall gain of the LNA has been defined in (4.21) and by also substituting (4.13) can be written as

$$S_{21} = \frac{2Z_S R_{L1} \left(R_S + 1/j\omega C_2 \right) \left(g_{m1} - j\omega C_{BC} \right) \left(j\omega L_3 g_{m2} \right)}{R_S \left(Z_S + Z_2 + 1/j\omega C_2 + R_S \right) \left(1 + j\omega R_{L1} (C_{BC} + C_{L1}) \right)}, \qquad (4.48)$$

with $R_{IN} = R_S$ and $C_{IN} = C_2$.

Thus increasing the gain of the LNA would require decreasing L_2, C_2 and C_{BC} (and thus C_F) as well as increasing Z_S. These are the same requirements as for NF optimization discussed in Section 4.7.1. Furthermore, increasing I_{C1} to increase the gain will decrease

the NF as shown. This, as well as increasing the gain by increasing R_{L1}, will also both result in further reduction of the NF of the second stage improving the overall NF.

Thus with the LC-ladder and shunt-shunt capacitive feedback LNA configuration NF and gain can always be optimized simultaneously and there is no trade-off between these two performance measures.

4.8   LINEARITY APPROXIMATION

Although NF and gain can be quantified relatively well using small-signal analysis amplifier linearity, being a large signal phenomenon, is harder to evaluate. Section 2.4 discusses the use of a Volterra-series to analyze circuits operating in weak non-linearity, however the derivation of the Volterra-series is very laborious and offer little insight that cannot be gained through large signal circuit simulations. Therefore only an approximation that can be used as an initial estimate of the IIP3 is derived here.

The IIP3 voltage of a CE amplifier can be approximated as [**34**]

$$V_{IIP3(CE)} = 2\sqrt{2}V_T \,, \tag{4.49}$$

where V_T is the thermal voltage. Since the proposed LNA consists of two cascaded common-emitter stages in which the first stage acts as a pre-amplifier to the second stage, thus reducing the second stage IIP3 [**12**], the final IIP3 voltage of the LNA can be approximated as

$$\begin{aligned} V_{IIP3(LNA)} &\approx \frac{V_{IIP3(CE2)}}{A_{v,in} \cdot A_{v,1}} \\ &\approx \frac{4\sqrt{2}V_T}{A_{v,1}} \end{aligned} \,, \tag{4.50}$$

where $A_{v,in}$ is approximately equal to ½. Since the voltage gain of the first stage often rolls off within the band of interest this will cause a similar increase (improvement) of the IIP3.

The IIP3 can be expressed in dBm through

$$IIP3 \approx 10\log\left(\frac{16 \cdot V_T^2}{A_{v,1}^2 \cdot R_S} \cdot 10^3\right). \tag{4.51}$$

As discussed in Section 2.4 the linearity can be improved by employing feedback providing an improvement of approximately

$$V_{IIP3(CE)}^{'} \approx V_{IIP3(CE)} \times (1 + A\beta)^{3/2}. \tag{4.52}$$

Such local feedback should be employed in the last amplifier stage since it dominates the IIP3 of the LNA. Local feedback in prior stages will also improve linearity by decreasing the gain of these stages and thus linearity can be traded for gain and NF.

Alternatively overall feedback can be used between the output and the first amplifier stage, however this greatly affects the input matching since feedback changes the input impedance. For example using series feedback in the emitter of the first stage increases the input impedance, thus requiring an increase in C_F to maintain the correct C_2 value for proper matching; however this is usually impossible to do while maintaining reasonable high frequency NF which increases with C_F.

It is suggested that the linearity of the initial LNA design is determined through simulation and subsequently optimized if desired using the techniques described in Section 2.4. The process that was followed in completing this research is discussed in Section 5.3.5 with the simulation results.

4.9   PERFORMANCE LIMITS AND TRADE-OFFS

Although the LC-ladder network can theoretically achieve a conjugate input match over an arbitrary bandwidth, two fundamental limits to the bandwidth of this LNA configuration can be identified, which leads to trade-offs with the other performance measures [**63**].

4.9.1   Noise figure vs. bandwidth

In Section 4.7.1 it has been shown that the common-emitter voltage noise of the first stage dominates the NF. From (4.46) it can be seen that the feedback capacitor C_F subsequently causes a sharp rise in NF at high frequencies due to the ωC_F term, as also shown in Figure 4.8. This increase in NF places a limit on the upper corner frequency ω_H for a given

maximum NF specification. It also follows that ω_H can be increased by decreasing C_F, provided no other frequency limitations are present.

The value of C_F is derived from the desired C_2 value using (4.22) after the gain of the first stage has been selected. The value of C_2 is in turn determined by the lower corner frequency ω_l through (4.1a), and a lower ω_l requires a larger C_2. This interdependence of ω_l and ω_u results in a fundamental limit on the bandwidth for a given maximum NF.

This noise figure-bandwidth trade-off can be quantified by substituting (4.1a) into an approximated version of (4.22), where C_2 is assumed much larger than $C_{\pi l}$ and $A_{v,1}$ approximated as $g_{m1}R_{L1}$, giving

$$C_{BC} \approx \frac{1}{\omega_l R_S \left(1 + g_{m1}R_{L1}\right)} . \tag{4.53}$$

Since the noise factor can be approximated using (4.46) as

$$F_1 \approx 1 + \left(\frac{1}{\left|Z_s\right|^2} + \left|1 + \frac{Z_2}{Z_S}\right|^2 \cdot \left|\omega C_{BC}\right|^2 \right)\left(r_b + \frac{V_T}{2I_C} \right) \cdot R_S , \tag{4.54}$$

equation (4.53) can then be substituted to obtain the noise factor as a function of ω_l as

$$F_1 \approx 1 + \left(\frac{1}{\left|Z_s\right|^2} + \left|1 + \frac{Z_2}{Z_S}\right|^2 \cdot \left|\frac{\omega}{\omega_l R_S \left(1 + g_{m1}R_{L1}\right)}\right|^2 \right)\left(r_b + \frac{V_T}{2I_C} \right) \cdot R_S , \tag{4.55}$$

where $F_{1\max}$ and ω_u can be substituted and then solved for ω_l as

$$\omega_l \approx \left[\frac{R_S\left(1 + g_m R_L\right)}{\omega} \sqrt{\left(\frac{\left(F_{1\max} - 1\right)}{\left(r_b + \frac{V_T}{2I_C}\right)R_S} - \frac{1}{\left|Z_S\right|^2} \right) \div \left|1 + \frac{Z_2}{Z_S}\right|^2} \right]^{-1} \Bigg|_{\omega=\omega_u} , \tag{4.56}$$

where Z_2 and Z_S are also frequency dependent as given in (4.10b) and (4.11) respectively. Since a change in ω_l will result in Z_S being modified through L_1 according to (4.1a), finding the correct solution for ω_l will be an iterative process.

It is however noticed that ω_l will decrease as $g_m R_L$ is increased, since C_2 is increased in this case without changing C_F. This means that this equation can also be used to determine the required low frequency first stage gain for a given frequency range and maximum NF specification when it is rewritten as

$$A_{v1} \approx g_m R_L \approx \left[R_S \frac{\omega_l}{\omega} \sqrt{\left(\frac{(F_{1\max} - 1)}{\left(r_b + \frac{V_T}{2I_C}\right)R_S} - \frac{1}{|Z_S|^2} \right) \div \left|1 + \frac{Z_2}{Z_S}\right|^2} \right]^{-1} - 1 \Bigg|_{\omega = \omega_u}. \qquad (4.57)$$

Since the thermal noise of the parasitic resistance of L_2 defined as

$$\begin{aligned} n_{RL2} &= \left|\frac{R_S}{Z_S}\right|^2 \frac{\overline{v_{R2}^2}}{v_{RS}^2} = \left|\frac{R_S}{Z_S}\right|^2 \frac{R_2}{R_S} \\ &= \frac{R_2 R_S}{|Z_S|^2} \end{aligned} \qquad (4.58)$$

also contributes somewhat to the NF at high frequencies according to Figure 4.8, the approximated noise factor equation in (4.55) can be modified to include this term, leading to more accurate results. The noise factor equation solved for ω_l then becomes

$$\omega_l \approx \left[\frac{R_S\left(1 + g_m R_L\right)}{\omega} \sqrt{\left(\frac{\left(F_{1\max} - 1 - R_2 R_S / |Z_S|^2\right)}{\left(r_b + \frac{V_T}{2I_C}\right)R_S} - \frac{1}{|Z_S|^2} \right) \div \left|1 + \frac{Z_2}{Z_S}\right|^2} \right]^{-1} \Bigg|_{\omega = \omega_u} \qquad (4.59)$$

4.9.2 Parasitic base-collector capacitance vs. lower corner frequency

Since there is a minimum base-collector feedback capacitance that can be implemented, which is the parasitic C_μ of the transistor without an additional C_F, it is apparent from (4.53) that there will be a maximum ω_l that can be achieved for a given first stage gain.

If the equation for C_2 in (4.1a) is written in terms of ω_l, and the equation for C_2 in (4.6) substituted with $C_{BC} = C_\mu$, the maximum lower corner frequency is given by

$$\omega_{l\max} = \frac{1}{R_S\left(C_{\pi1} + C_{\mu1}\left(1 + g_{m1} R_{L1}\right)\right)}. \qquad (4.60)$$

With capacitances of $C_{\pi 1} = 25$ fF and $C_{\mu 1} = 20$ fF found in the 0.13 μm IBM 8HP process, and a first stage gain of 10 dB, the maximum lower corner frequency that can be achieved is approximately 30 GHz in a 50 Ω system.

By substituting $\omega_{l\max}$ and $C_{BC} = C_{\mu}$ in (4.59) and numerically solving for ω_u an associated maximum upper corner frequency can also be found.

It is possible to scale the transistor emitter length in order to reduce the parasitic capacitances of the transistor to make operation at higher frequencies more feasible; however the NF increases quite rapidly with increase in r_b since r_b is the dominating noise source in the system. Thus the NF vs. bandwidth trade-off remains as decreasing the emitter length to decrease capacitances will increase r_b.

4.10 LIMITS OF THE MODEL AND CONFIGURATION

Although the equations derived in the preceding sections do well to quantify the performance of this LNA topology and track simulations reasonably well, it remains a first order analysis which may cause results to deviate from those expected at very high frequencies. Some of the critical assumptions that were made as well as other factors that may be causes of such deviations at high frequency operation are discussed next [64].

4.10.1 Input matching approximation

The input impedance of the transistor as defined by C_{IN} and R_{IN} in (4.6) and (4.7) respectively is found by neglecting $j\omega R_{L1}C_{L1}$ when it is assumed that $(1 + g_{m1}R_{L1}) \gg j\omega R_{L1}C_{L1}$. When the assumption no longer holds at high frequencies the $j\omega R_{L1}C_{L1}$ term should be included in the equation for the Miller impedance which is then found to be

$$Z_M = \frac{R_{L1}}{(1 + j\omega R_{L1}C_{L1} + g_{m1}R_{L1})} + \frac{1}{j\omega\left(C_{\pi 1} + C_{BC}\left(1 + \dfrac{g_{m1}R_{L1}}{1 + j\omega R_{L1}C_{L1}}\right)\right)}. \qquad (4.61)$$

Equation (4.61) shows that in such a case C_2 will decrease with frequency as the voltage gain decreases due to the output pole of the first stage. The equivalent resistance also

becomes frequency dependent and will only appear resistive over a limited frequency band.

Although this will cause the calculated results to deviate from simulation, this problem can be avoided by using the more accurate equation for the transistor input impedance in (4.29) which does not rely on the said approximation.

4.10.2 Hybrid-π transistor model and assumptions with regards to parasitics

The simple high frequency small-signal transistor model was used in the derivations since it includes only the most essential parasitic components, resulting in easily comprehensible equations describing the circuit performance. While this is sufficient for a first order design the following additional important parasitic components/effects present in more advanced transistor models (see the HICUM [60] in Figure 3.2) are not taken into account:

- The presence of the series base and emitter resistances (r_b and r_e, respectively) were neglected in the S-parameter derivation.
- The degeneration due to the feedback afforded by r_e was also not taken into account.
- The typical parasitic capacitance values as given in the process datasheets were used as constants while these capacitances are in fact dependent on the collector current.
- The model assumes that the external C_F and parasitic C_μ can be added in parallel directly; the terminals of these capacitances are, however, separated by r_b and r_c, and C_μ is also distributed around the internal and external base series resistances (*rbi* and *rbx*).

The above effects will result in deviations from the predicted results and may to an extent be responsible for the measured gain, shown in Section 7.3, being much lower than expected.

4.10.3 Gain bandwidth product

It has been mentioned in Section 4.3.3 that the f_T of the first stage transistor often results in a gain roll-off at -20 dB/decade above a corner frequency within the band of interest. Although the design attempts to compensate for this roll-off through the inductive load of

the second stage which introduces a zero in the overall frequency response and thus, ideally, results in a flat voltage gain at the output, the second stage also has a finite f_T and as such cannot maintain a transfer function rising at +20 dB/decade at very high frequencies. Therefore the GBP remains a fundamental limit to the bandwidth that can be achieved while maintaining reasonable gain per stage.

4.10.4 Passive on-chip components

The most fundamental limit to the achievable frequency range is the available passive component values in a given transistor process.

All matching network components scale with inverse proportionality to corner frequency and as such the upper corner frequency, determined by L_2 and C_1, is limited by the minimum inductance and capacitance values that are available.

It would be possible to use parallel connected inductors to decrease the effective inductance; however this would consume a large chip area and also introduce additional large parasitic components into the circuit. The use of series connected capacitors to achieve a smaller effective capacitance is more feasible, however C_1 is usually implemented as the pad capacitance and as such the use of another series capacitor is invalid.

The lower corner frequency is limited by the maximum inductance value that is available for L_1. Although C_2 also influences the lower corner the limitation on C_2 is due to the high frequency NF as discussed earlier and not due to passive component limitations. Since the latter is usually the dominant limitation the maximum available L_1 is not significant.

4.10.5 Simplified inductor model

Since use of the complete on-chip spiral inductor model shown in Figure 2.12 [47] would be too cumbersome in the derivation of a practically useful mathematical model, inductors were modelled as only a series inductance and frequency dependent series resistance. The value of the resistance was derived from the inductor Q-factor which was assumed constant over frequency within the band of interest; this is, however, not truly the case and will cause deviations in the actual responses from the predicted performance. The complete inductor model would include this frequency dependence of the Q-factor.

The impact of the simplification is further apparent in the spike caused in the simulated frequency response in Section 5.3 by the self-resonant frequency of the large inductor L_1, which does not show up in the predicted response. The resulting simplified noise model will also cause deviations in the noise performance.

4.10.6 Base- and collector current noise correlation

It was stated in Section 2.3 that collector current shot noise is not introduced at the base-collector junction as often assumed but in fact originates from the base-emitter junction where majority carrier electrons (in *npn* transistors) from the emitter cross the junction into the base. These noisy electrons are transported across the base to the base-collector junction at the rate quantified in the base transit time, resulting in correlation between the base- and collector current noise.

In the derivation of the equation for NF in Section 4.6 this correlation between the base- and collector current noise is neglected. This is similar to assuming the collector current shot noise is generated at the base-collector junction by setting the base transit time equal to zero, resulting in the conventional SPICE noise model. Although this approximation is feasible when $\omega << 1/\tau_F$, at 60 GHz which is much closer to the device f_T the noise correlation becomes non-negligible and the mathematical model no longer predicts the NF of the LNA accurately [63].

4.11 THEORETICAL RESULTS

Figure 4.10 and Figure 4.11 offer some insight into the theoretical performance of this configuration following a design process based on the analysis in the preceding sections. An amplifier with desired S_{21} of 20 dB was designed for operation over the 3 to 10 GHz band (the UWB). A maximum NF of 4 dB was specified.

It was assumed that the IBM 8HP process would be used and the results were obtained with a supply voltage of 1.5 V and a pessimistic β_0 of 300 and on-chip passive inductor Q-factor of 5.

The resulting input reflection was calculated to be less than -10 dB over the entire frequency band, and as desired a flat S_{21} response of 20 dB was obtained. The calculated maximum NF of the first stage is 3.34 dB and the minimum 2.57 dB close to the centre of

the frequency band even without any optimization of the component values. As expected IIP3 increases linearly at approximately 20 dB per decade with frequency from -31.4 dBm to -23.5 dBm over the band of interest due to the -20 dB per decade roll-off in first stage voltage gain.
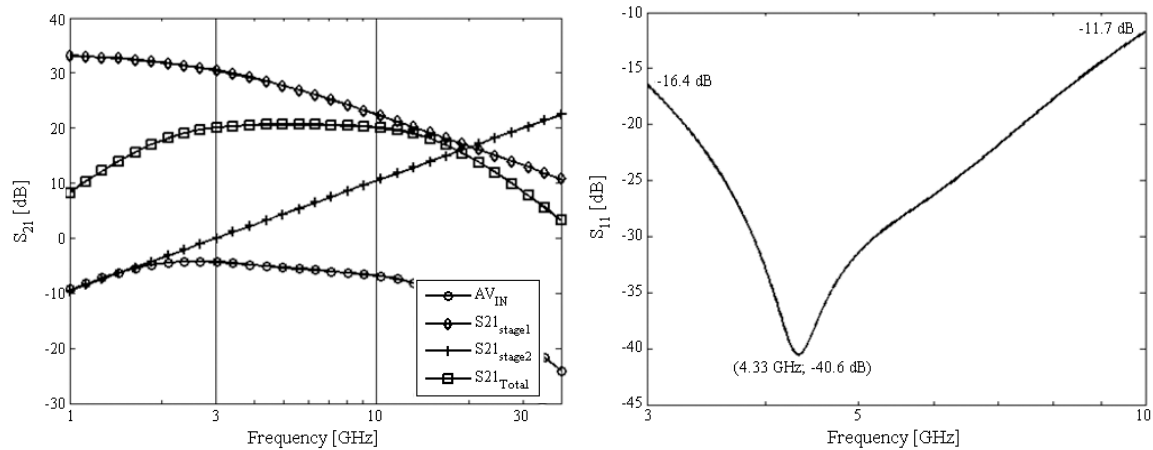

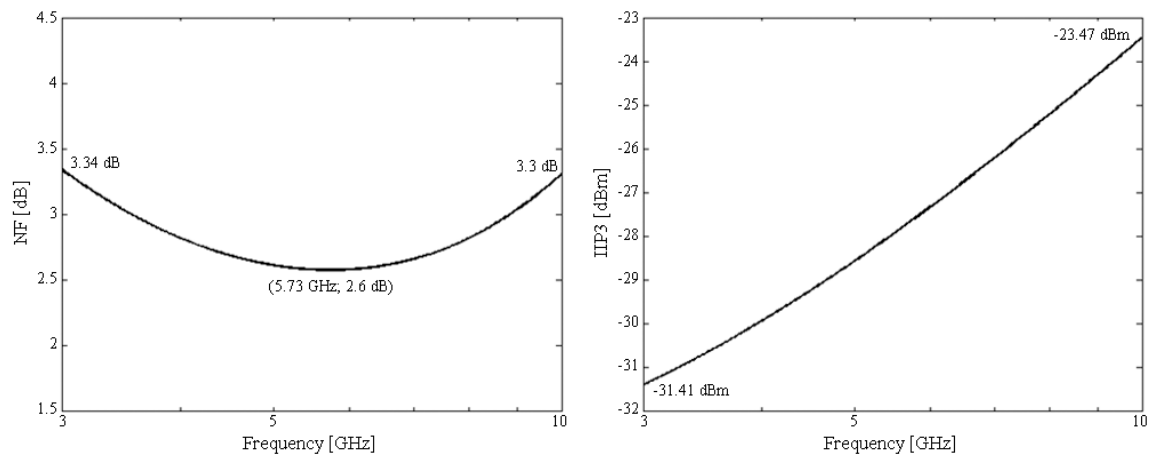**Figure 4.10. Calculated input reflection coefficient and gain versus frequency.**

Figure 4.11. Calculated noise figure of the first amplifier stage and approximated IIP3 versus frequency.

4.12   LNA ELECTRONIC DESIGN AUTOMATION

The discussion in Sections 4.2 through 4.10 provide all the groundwork necessary to implement EDA software similar to the software implemented in [**49**] for the design of power amplifiers (PA). A preliminary implementation of such software has been done in MATLAB and was used in the design of the LNAs presented in Chapter 5. The routine was also used to generate the calculated plots for key performance measures and noise source contributions. This MATLAB code is presented in Appendix A.

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The software takes as inputs the desired frequency band, gain and maximum NF specifications. The transistor process parameters, including the values of the parasitic components at the chosen emitter length should also be given.

It is then possible to first determine whether the proposed design is feasible based on the desired frequency range and NF specification using the equations given in Section 4.9, or alternatively to find the first stage gain that is required to allow a sufficiently small C_F to achieve the high frequency NF specification. If feasible, the LC-ladder equations (4.1a) and (4.1b) is used to determine the respective reactive component values; after which the rest of the design equations detailed in Section 4.4 is used to find values for the remaining passive components and the collector currents. If it is found that the gain specification cannot be met with the limitations of the transistor process the need for a third stage should be indicated, however this is not included in this preliminary version.

Once these initial values have been derived the S_{11}, S_{21}, NF and approximated IIP3 frequency responses are plotted using (4.8a,b), (4.21), (4.43) and (4.51) respectively, as well as the terms in the numerator of (4.51) which are plotted separately as in Figure 4.8. The component values and collector currents can then be modified one by one and the plots redrawn to observe its effect on the performance measures to optimize the NF as discussed in Section 4.7.

These results are a sound first order design with very little effort from the designer, which can then be optimized further using simulation software and the proper HIT-kits for the transistor process.

Ideally the optimal inductor dimensions should also be calculated for the final inductance values by incorporating that part of the software from [**49**], or preferably by combining them into a complete RF amplifier design package capable of providing rapid LNA and PA design for wireless transceivers.

4.13 CONCLUSION

This chapter discussed the mathematical modelling that was required to quantify the performance of the LC-ladder and capacitive shunt-shunt feedback LNA configuration.

An initial derivation of input reflection and gain equations was presented with subsequent improvement of the accuracy of these equations; which also showed the need for adding a second inductively loaded stage thereby defining the final LNA topology. This led to the definition of compact design equations.

The NF equation was derived and means for optimizing the design to achieve low NF were also discussed. Although a full and accurate quantization of the linearity of the LNA was not included in this study, equations for approximating the IIP3 were given. The noise figure-bandwidth trade-off was discussed as well as other fundamental limits to the performance of this topology.

A means of implementing complete EDA of LNAs employing this topology was defined, and theoretical performance results of such a design were plotted and proved to be very promising.

In summary, the LC-ladder and capacitive shunt-shunt feedback topology proved to be a viable means of implementing very wideband LNAs and as such was manufactured after further simulation as detailed in the following chapters.