CHAPTER 1: INTRODUCTION

The research question addressed in this thesis is whether a combined LC-ladder and capacitive shunt-shunt feedback matching network can be used successfully in wideband low noise amplifier (LNA) implementations, especially with improved performance compared to current LNA implementations in literature.

1.1 BACKGROUND TO THE RESEARCH

In wireless receiver modules the first subsystem is usually a LNA designed to provide sufficient amplification for subsequent stages while adding as little noise as possible. The ability of a design to meet this objective is quantified in the noise factor of the amplifier which is defined as the ratio of the signal-to-noise ratio at the output of the amplifier to the signal-to-noise ratio at the input. It is well known that the first amplification stage dominates the total noise figure (NF) of the system [**1**] and thus the noise optimization of this first stage is critical. In general the important characteristics of low noise amplifiers are: low noise figure, good input matching, sufficient flat gain over a required frequency band, good linearity and reasonable power consumption.

As applications move to higher frequencies new design challenges are introduced. At high frequencies with wide frequency bands the noise performance of silicon bipolar junction transistors (BJT) are no longer satisfactory. Traditionally III-V compounds such as GaAs or InP were used in high speed applications as they are capable of achieving high unity gain frequencies, albeit at a much higher fabrication cost than that of silicon processes [**2**]. III-V compound devices require high supply current to achieve this high speed performance though, which makes their usage less desirable. Although the optimal noise performance and fabrication cost of GaAs and InP devices are comparable to that of silicon-germanium (SiGe) processes, the SiGe heterojunction bipolar transistors (HBT) have higher associated gain in amplifiers designed for minimum noise figure [**3**].

The increased availability of SiGe processes has positioned it as an important alternative to III-V compounds and has led to the use of SiGe HBTs in many high frequency applications. One of the major reasons for the success of SiGe HBTs in wireless applications is its very low noise capability [**4**] due to very high beta as well as a small base spreading resistance due to aggressive lateral and vertical scaling. In addition, HBTs

are high speed devices with unity gain frequencies above 200 GHz in certain processes making it an attractive choice for amplifier design at high frequencies. Since the SiGe fabrication process is an extension of the CMOS fabrication process to which extra processing steps are added it is also possible to integrate digital logic with efficient radio frequency (RF) circuits on the same die.

It has been shown that the input impedance matching plays an important role in achieving minimum noise figure and that an optimal source impedance exists for achieving the best noise performance [**5**]. This impedance is usually different than for maximum power transfer. LNA design entails achieving a low noise figure and usually optimal noise matching for a first amplifier stage. The obvious trade-off between minimum noise and maximum available gain has sparked much research interest into achieving a simultaneous optimal noise and power match. A traditional approach is the use of shunt-shunt feedback to modify the amplifier input impedance achieving such a simultaneous match [**6**], [**7**]. This also provides wide band operation. Emitter scaling is also a very common method used to modify the optimal source resistance of a transistor which could then be set equal to the characteristic impedance of the system [**8**], [**9**] achieving a simultaneous match in narrowband applications.

The LNA configurations mentioned above often employ inductive input matching or emitter degeneration. Through process scaling and lower inductor values required at high frequencies, the use of on-chip passive inductors have become common in integrated RF applications; however, these on-chip inductors suffer from low quality factor (Q-factor) due to the high permittivity of silicon dioxide which has a relative permittivity of 3.9. Although active inductors increase the noise figure of an amplifier they offer an important alternative for achieving a high Q-factor and reducing chip size and have been used in low noise amplifiers with good results [**10**].

At present narrowband techniques are often applied directly to wideband LNA implementations and as such good performance over the entire frequency band is often not achieved. This emphasizes the need for novel wideband LNA topologies capable of achieving good and relatively constant performance over the entire band of interest.

1.2 HYPOTHESIS AND RESEARCH QUESTIONS

Use of the LC-ladder input matching network has been shown as an effective means of achieving an arbitrary wide conjugate input impedance match and has been implemented in conjunction with the emitter degeneration technique [**11**]. This configuration has the shortcoming of introducing a pole at the lower frequency end, and this in turn requires an inductive load to equalize the voltage gain with the result that the final LNA requires four area consuming inductors. Due to the nature of the matching network a given lower corner frequency also fixes the collector current limiting the design decisions.

The shunt-shunt capacitive feedback technique has been shown capable of synthesizing an equivalent series RC network and used effectively in the design of a LNA for the ultra-wideband (UWB) [**12**]. This is however a narrowband configuration and is not ideal for wideband implementation.

From the above, the following hypothesis was formulated:

> *If a fourth order LC-ladder filter can be used to realize input matching over an arbitrary frequency band, and a shunt-shunt capacitive feedback common-emitter configuration can be modelled as an equivalent series RC circuit, then a combination of these two circuits can be used as a wideband LNA overcoming selected shortcomings of current LNAs in literature.*

To prove the hypothesis the following research questions must be addressed:

- Can it be proven through mathematical modelling that the proposed configuration is capable of wideband matching and low noise operation?
- Does this configuration avoid introducing a pole at the lower corner frequency?
- Can the inductor count be reduced compared to the LC-ladder and inductive emitter degeneration configuration?
- Does this configuration decouple the collector current from the lower corner frequency value?

1.3 JUSTIFICATION FOR THE RESEARCH

The goal of most wireless communication systems is achieving a high data rate. Even with the vast improvements allowed by the coding schemes employed in wireless communications today the signal-to-noise ratio remains a fundamental limiting factor of data throughput. Since the LNA is the determining factor in the noise figure of a system any improvement in noise figure is of great importance. Good linearity, which also limits the data rate, should however be maintained as the high power consumption required to compensate for poor linearity is undesirable, especially in battery-powered devices.

Table 1.1 lists the specifications of some related work found in literature indicating the state-of-the-art LNA performance. The simulated and measured results of designs done in this research using the proposed LC-ladder and capacitive shunt-shunt feedback configuration are also shown. For the same input matching and gain specification a lower NF and power consumption is achieved compared to most of the listed LNAs at the cost of reduced IIP3. This makes the proposed configuration especially suited to applications were low noise is very important and linearity only a secondary concern. Furthermore it is suited to very wideband designs such as the designed LNA operating from 0.8 to 18 GHz [**13**].

The desired specifications of the LNA that was designed in this research were defined towards the implementation of a receiver that is able to operate at multiple 800 MHz bands over the 1 GHz to 18 GHz range. A configuration capable of achieving such a wide band can however also be used for software defined radio (SDR) applications [**14**], [**15**] in general, or applied directly to smaller application specific sub-bands.

Since there is an abundance of bandwidth available in the unlicensed part of the mm-wave frequency band (57-64 GHz) which can be leveraged against power consumption in mobile devices [**16**], the investigation of a design at these frequencies is also warranted.

Although this research was done towards bipolar transistor LNA implementations the simple high frequency small-signal transistor model was used in the derivation of the mathematical model with r_π neglected in the frequency range of operation. The described techniques can therefore also be easily applied to field effect transistors (FET) with the only required change being the substitution of the appropriate equivalent noise source equations and transconductance equation for FETs.

Table 1.1. Simulated and measured results of the LNAs designed for this research using the proposed topology compared to state-of-the-art measured LNA results from literature.

Ref.	Impact factor (IF)	5 year IF	Technique	Technology / f_T	BW [GHz]	S_{11} [dB]	S_{21} [dB]	NF [dB]	IIP3 [dBm]	P [mW]	Area [mm^2]
This work	-	-	LC-ladder & capacitive-feedback (simulated)	0.13 µm (8HP) / 200 GHz	1-18	< -10	21.4	1.7-3.6	-22.6 @ 4.2 GHz	12.75	-
This work	-	-	LC-ladder & capacitive-feedback (optimized for linearity) (simulated)	0.13 µm (8HP) / 200 GHz	1-18	< -9.8	20	2.2-3.9	-14.5 @ 4.2 GHz	23.25	-
This work	-	-	LC-ladder & capacitive-feedback (simulated)	0.18 µm (7WL) / 60 GHz	3-14	< -10	20.7	2.8-4.3	-22.5 @ 6.5 GHz	14.22	0.4272
This work	-	-	LC-ladder & capacitive-feedback (optimized for linearity) (simulated)	0.18 µm (7WL) / 60 GHz	3-14	< -9.7	20.1	2.9-4.8	-19.0 @ 6.5 GHz	33.3	0.4272
This work	-	-	LC-ladder & capacitive-feedback (optimized for linearity) (measured)	0.18 µm (7WL) / 60 GHz	3-6	< -9.7	11†	N/A‡	-22.0 (P_{1dB})	33.3	0.4272
[**17**]	3.4661[1]	4.037	Inductive emitter degeneration	0.6 µm CMOS	1.5	< -10	22	3.5	-9.3 @ 1.5 GHz	30	-
[**11**]	3.4661[1]	4.037	LC-ladder & inductive-emitter degeneration	0.18 µm (Jazz semicond.)	3-10	< -9	21	2.5-4.5	-5.5 @ 3.4 GHz	30	1.35*
[**6**]	Proc.	Proc.	Frequency controlled shunt-shunt feedback	0.18 µm CMOS	3-10	< -13	8	3.5-4.4	-	18.5	-
[**18**]	2.7111[1]	3.187	Resistive feedback	0.18 µm / 150 GHz	3–10	< -10	20	3.4-4.7	-17 @ 3.5 GHz	42.5	0.18
[**19**]	3.4661[1]	4.037	Inductive emitter degeneration	0.18 µm CMOS	3-10	< -10	9.3	4-7	-6.7 @ 6 GHz	9	1.1*
[**20**]	Proc.	Proc.	Emitter degeneration with added BE-capacitance	0.18 µm / 120 GHz	0.1-13	< -7.2	20.3	1.8-3.1	2.1 @ 6 GHz	26	0.72
[**12**]	2.7111[1]	3.187	Shunt-shunt capacitive-feedback	0.35 µm SiGe BiCMOS	3-14	< -9	23	2.5-5.8	-17 @ 5 GHz	25.8	0.2223
[**21**]	1.13[2]	-	Parallel LC resonators & emitter degeneration	0.13 µm CMOS	6.8-8.8	< -10	29.5	4.0-5.2	-8.5 @ 7.7 GHz	15	0.4
[**9**]	2.3021[1]	2.533	Inductive emitter degeneration	0.13 µm (8HP) / 200 GHz	28-40	< -10	23.5	2.3-3.2	-19.5 @ 35 GHz	11	0.09
[**22**]	Proc.	Proc.	Multiple resistive feedback paths	0.35 µm (Jazz semicond.)	3-10	< -10	21	4.0-4.9	-	-	-
[**23**]	Proc.	Proc.	Diff. emitter-coupled pair with emitter followers	0.8 µm	3.1-10.6	< -7	19.9	2.1-2.9	-17.5 @ 7 GHz	77	0.14*
[**24**]	Proc.	Proc.	Three stage with CE and resistive feedback	0.18 µm / 120 GHz	5.2-15.8	< -10	19.1	4.2-5.2	-6.47 @ 13 GHz	116	0.0954*

1. ISI web of knowledge
2. https://www.researchgate.net/journal/1549-7747_Circuits_and_Systems_II:_Express_Briefs,_IEEE_Transactions_on

† From 3 GHz to 10 GHz
‡ NF measurement was not feasible due to the low gain
* Including bond pads

1.4 RESEARCH METHODOLOGY

Various LNA configurations were investigated in a thorough literature study to find the most appropriate option for wideband implementations. The shortcomings of many configurations were subsequently identified and narrowband configurations were deemed unsuitable for the design. A new LNA topology which is a combination of the LC-ladder input matching network (IMN) and capacitive feedback topology was then proposed to overcome many of these shortcomings [**25**].

A complete mathematical model which characterizes this configuration was subsequently derived and MATLAB was used to model the LNA performance. The derivation was done using an RF analogue approach. This mathematical model was also used to define compact design equations for a first order design and a process for optimizing the circuit for minimum NF was determined.

The design equations were used in the design of wideband LNAs using two different IBM SiGe BiCMOS processes, namely the 0.18 µm 7WL process and the 0.13 µm 8HP process with f_T of 60 GHz and 200 GHz respectively. Selected process parameters are discussed in Chapter 3. The calculated results were verified through simulations using Cadence Virtuoso and the high performance interface tool kits (HIT-kits) supplied by IBM.

Finally, after the LNA was optimized further using simulations it was submitted for fabrication in the IBM 7WL 0.18 µm SiGe BiCMOS process. The dies were packaged in quad flat no-lead (QFN) packages and soldered onto a test printed circuit board (PCB). The noise figure, gain, input reflection coefficient and P_{1dB} of one prototype was measured using a Rohde & Schwarz ZVA40 Vector Network Analyzer and an Agilent E4440A PSA spectrum analyzer.

To verify the accuracy of the initial calculated results and subsequent simulations, the measured performance was compared to results of simulations which included the package parasitics.

1.5 DELIMITATIONS OF SCOPE AND KEY ASSUMPTIONS

In the derivation of the mathematical model of the LNA the simple high frequency small-signal transistor model was used to derive equations that could be easily interpreted. Inductors were also viewed simply as a series inductance and parasitic resistance. This is however sufficient for a first order design and in fact agrees well with simulations done using complex transistor models despite the simplicity of this approach.

In the circuit simulations parameterized cells (p-cells) were used which include the device parasitics present in the circuit. The interconnect capacitance was however not included in simulation and may cause slight deviations in the expected performance.

During the experimental testing the characteristics of only a single prototype was measured due to the shortcomings of the test PCB discussed in Section 6.7. Therefore the presented results merely offers a proof of concept, but more rigorous testing should be performed to fully characterize the LNA performance based on a larger sample.

The noise figure was measured at room temperature and not at 290 °K as specified in the definition of NF [**1**].

1.6 CONTRIBUTION TO THE FIELD

A new LNA configuration, namely the LC-ladder and capacitive shunt-shunt feedback topology, has been proposed for use in wideband applications up to 20 GHz. A detailed list of the resulting contributions to the body of knowledge is given here.

- This configuration has been demonstrated successfully through the design and simulation of a 1-18 GHz LNA achieving a simulated 21.4 dB gain and S_{11} < -10 dB with a minimum NF of 1.7 dB increasing to a maximum of 3.6 dB at the upper corner frequency. The power consumption of this LNA is only 12.7 mW and it occupies a chip area of 0.43 mm^2 including three on-chip inductors.

- A second LNA with improved linearity from -22.6 dBm IIP3 to -14.5 dBm is also presented and achieves 20 dB gain with a minimum and maximum NF of 2.2 dB and 3.9 dB respectively, and power consumption of 23.3 mW.

- This proposed technique followed a thorough literature study on existing LNA configurations which were analyzed to find the performance and shortcomings of each as now given and compared in Chapter 2.

    - It became apparent that there is a need for wideband LNA configurations that can be applied directly to wideband implementations – as is the case with the proposed configuration which is a true wideband topology – instead of, as is often done [**12**], [**20**], adapting more well known narrowband techniques to wideband applications leading to undesirable and, as proven in this work, to a large extent unnecessary trade-offs between input matching, noise and gain performance.

    - Many wideband configurations that do exist do not optimize all LNA performance measures simultaneously, as in [**6**] for instance where high NF and low gain negates the advantages of a wideband conjugate match. It has been shown that minimizing NF and maximizing gain in the LC-ladder and capacitive shunt-shunt feedback topology can always be obtained simultaneously.

    - A large number of on-chip inductors (three being typical in narrowband and four in wideband implementations [**9**], [**6**], [**11**]) usually characterizes topologies in the body of knowledge. The LC-ladder and capacitive feedback topology however requires only a maximum of three inductors when operating close to the limits of the technology node where the first stage output pole could fall within the band of interest. When this is not the case, the first amplifier stage produces constant gain with frequency and the number of on-chip inductors could be reduced to only two.

    - In some cases a pole is introduced in the frequency response by the IMN, which could be at the lower corner frequency [**11**] requiring an inductive load to equalize the voltage gain, this however is not the case with the proposed technique in which there is no such intrinsic pole introduce by the IMN.

- A Monte Carlo analysis and temperature sweep showed that this is a very robust configuration, especially when the feedback techniques proposed to improve linearity are applied.

    - The gain of the LNA varies by only 2.4 dB on average and between 18.8 dB and 21.4 dB in the mid-band. Although S_{11} also varies by 2 dB it remains within specification over most of the operating bandwidth, and NF varies by as little as 0.3 dB over most of the band with the maximum NF in extreme cases being 4.25 dB.

    - A sweep over the military specification temperature range revealed only a 2.5 dB variation in gain and a 2 dB variation in NF from -55 °C to 125 °C.

- A first order mathematical model has been derived to characterize the proposed topology, and this model has also been used to derive compact design equations for such a LNA. The most novel contribution in this model is the derivation of the NF equation, in which the individual noise source powers occur as individual terms in the equation from which the dominant contribution could be determined, and strategies for optimization deduced. This allowed for a more focussed procedure for noise optimization.

- The model is suitable for use in electronic design automation (EDA) software that determines component values for a LNA based on a specified frequency range, gain and maximum NF. Preliminary MATLAB source code for such software used successfully throughout this research is given in Appendix A; and as such the design-for-design of this configuration has also been done. At the moment only a complete derivation for IIP3 is lacking and suggestions regarding this have been made for future work. Implementation of such EDA software will also ensure the repeatability of this novel design procedure and effectively archive it for future use.

- Some limitations of this topology have been identified and were also demonstrated in a 60 GHz LNA design where the wideband nature of the configuration proved redundant and the design theory did not meet with the expected results due to second order effects.

- It was noted that this topology can be used to push a transistor of a given technology node to its limits and then allows for trading gain, NF, bandwidth and power consumption during the design process. This trade-off has been quantified in the noise figure versus bandwidth trade-off equation which forms part of the model.
- The accuracy of the model has been verified through simulations in Cadence Virtuoso using the IBM HIT-kits, and LNAs of two versions of this topology have been submitted for fabrication. The measured performance from these LNAs conform well to the expected results from simulations when the shortcomings of the PCB and test procedure are taken into account which further validates this topology as a candidate for wideband LNA implementations.

1.7 PUBLICATIONS LEADING FROM THIS RESEARCH

The following peer reviewed conference articles have been published and presented by the author as part of his research activities:

- M. Weststrate and S. Sinha, "Noise optimization of a wideband capacitive shunt-shunt feedback LNA design suitable for software-defined radio," *Proc. of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Hammamet, 13-16 December 2009.
- M. Weststrate, S. Sinha and D. Neculoiu, "Limitations of a LC-ladder and Capacitive Feedback LNA and Scaling to mm-Wave Frequencies," *Proc. of the IEEE CAS 2009 (International Semiconductor Conference)*, Sinaia, pp. 315-318, 12-14 October 2009.
- M. Weststrate and S. Sinha, "Analysis of a Low Noise Amplifier with LC-Ladder Matching and Capacitive Shunt-Shunt Feedback," *Proc. of IEEE Africon 2009*, Nairobi, 23-25 September 2009.
- M. Weststrate and S. Sinha, "Mathematical Analysis of Input Matching Techniques With Application in Wide-band LNA Design," *Proc. of the South African Conference on Semi- and Superconductor Technology (SACSST)*, Stellenbosch, pp. 128-132, 8-9 April 2009.
- D. Foty, S. Sinha, M. Weststrate, C. Coetzee, A.H. Uys, and E. Sibanda, "mm-Wave Radio Communications Systems: The Quest Continues," *Proc. of the 3rd International Radio Electronics Forum (IREF) on "Applied Radio Electronics. The State and Prospects of Development,"* Kharkov, pp. 14-17, 22-24 October 2008 (Invited Paper).

Presentations were also given by the author at both the 9th and 10th European high current model (HICUM) workshop. At the workshop held in Würzburg, Germany on 23 October 2009 the presentation entitled *Design and Simulation of Wideband LNAs up to 60 GHz* was given and at the workshop in Dresden, Germany on 24 September 2010 a presentation entitled *Sensitivity of LNA performance characteristics to individual HICUM parameters*.

The following peer reviewed journal articles submitted by the author as part of his research activities have been published. All journals except the ARJ are accredited by the Institute for Scientific Information (ISI). The ARJ is, however, a fully peer-reviewed accredited journal – Dept. of Higher Education and Training (DoHET), Ministry of Education, South Africa:

- M. Weststrate and S. Sinha, "Mathematical Modelling of the LC-Ladder and Capacitive Shunt-Shunt Feedback LNA Topology," *SAIEE Africa Research Journal (ARJ)*, vol. 100, pp. 72-78, September 2009.
- M. Weststrate, S. Sinha and D. Neculoiu, "Design Trade-offs and Limitations of a LC-Ladder and Capacitive Feedback LNA and its Application at mm-Wave Frequencies," *Romanian Journal of Information Science and Technology (ROMJIST)*, vol. 13, no. 1, pp. 98-107, 2010.
- M. Weststrate and S. Sinha, "Wideband LNA design using the LC-Ladder and Capacitive Shunt-Shunt Feedback Topology," *Microwave and Optical Technology Letters, accepted for publication in July 2011*.

The following article by the author has also been submitted and conditionally accepted in an ISI accredited peer reviewed journal:

- M. Weststrate, A. Mukherjee, S. Sinha and M. Schröter, "Sensitivity of narrow- and wideband LNA performance characteristics to individual HICUM parameters," submitted to the *International Journal of Electronics, submitted in March 2011, resubmitted in May 2011*.

1.8 OUTLINE OF THE THESIS

Chapter 1 serves as an introduction to the thesis providing a brief background to the research resented. The hypothesis is stated and the justification for the research is

provided. A summary of the research methodology as well as the contribution of the research to the body of knowledge is also given with a list of publications leading from this research.

Chapter 2 provides a review of the literature pertaining to this research topic. A brief general discussion on the noise sources in transistors is given, followed by the effects of these sources in HBT amplifier circuits, as well as the characteristics of HBTs making them suitable for low noise design. A general discussion on input matching techniques is presented after which various matching schemes found in present literature are discussed with comments on the advantages and disadvantages of each. These include the well known inductive emitter degeneration technique which by way of emitter scaling used to adjust the optimal noise resistance can achieve a simultaneous optimal noise and conjugate input match. Also some techniques using feedback to adjust the input impedance and topologies with more complex input matching networks. The discussion involves a comparison of the gain, noise and linearity of these configurations. Subsequently the use of on-chip inductors, as well as the trade-offs and characteristics of active inductors are presented. This chapter concludes with the proposal of a new LNA topology combining the LC-ladder and capacitive feedback approach to provide wideband matching and good noise performance.

Chapter 3 describes the SiGe transistor processes used in the wideband LNA designs intended to verify the soundness of the mathematical model, and also the transistor models used in simulations.

Chapter 4 discusses the derivation of the mathematical model of the proposed amplifier configuration. Equations for input matching, gain and noise figure are derived and these are also rewritten to provide compact design equations. An approximation for the linearity and quantification of certain design trade-offs are also presented. Finally the design steps are given in a way that can potentially be used in a software package to automate the design process.

Chapter 5 describes the design and simulation of three different amplifiers. The first is a design for the 1 GHz to 18 GHz range using the IBM 8HP 0.13 µm process. The second is a design at 60 GHz using the same process and finally the amplifier to be fabricated using the IBM 7WL 0.18 µm process is presented over the 3 GHz to 14 GHz frequency band.

The layouts of the circuits that were fabricated are presented in Chapter 6 with some discussion as well as the packaging choices and its limitations. The schematic of a test PCB for the biasing and measurement of the packaged devices is also given.

The measurement setup and test procedures are discussed in Chapter 7. The experimental results are also presented with some comments on its comparison with the expected results from simulations.

The conclusion, critical evaluation of the work and potential areas for future research are provided in Chapter 8.

CHAPTER 2: LITERATURE REVIEW

2.1 INTRODUCTION

The objective in LNA design is to achieve sufficient gain over a required frequency band while maintaining a very low noise figure. This is crucial for the first amplification stage since it dominates the NF of the system as a whole as shown in

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A1}G_{A2}} + \frac{F_4 - 1}{G_{A1}G_{A2}G_{A3}} + \cdots, \tag{2.1}$$

where F is the noise factor, G_A the associated gain and the subscripts indicate successive amplifier stages [**1**]. The linearity of the amplifier as well as power consumption are also important specifications and thus limitations that the design must contend with. This chapter provides a review of the literature pertaining to low noise amplifier design and achieving these design objectives.

The increased availability of silicon-germanium (SiGe) processes has led to the use of SiGe HBT in many high frequency applications. One of the major reasons for the success of the SiGe HBTs in wireless applications is its low noise capability [**4**] and high speed, which also makes it attractive for low noise amplifier design; thus the use of HBTs is elaborated. Inductors are also important in RF design and the availability of on-chip inductors have allowed for complete integration of RF circuits. However, passive on-chip inductors are costly in terms of chip area and suffer from a low Q-factor and thus various inductor types and optimization techniques are briefly discussed, as well as the possibility of employing active inductors to avoid these shortcomings at the cost of higher noise.

The first part of this chapter discusses the noise sources present in transistors, followed by the effect of these sources in HBT amplifier circuits. The characteristics of HBTs making them suitable for low noise design are discussed, as well as important linearity considerations. Various input matching techniques are then presented, including a detailed discussion of the very common use of emitter scaling to adjust the optimal noise resistance for a simultaneous optimal noise and power input match.

2.2 NOISE IN AMPLIFIER CIRCUITS

There are five types of well known noise sources present in circuits with active and passive devices. These are [**26**]: Thermal noise, shot noise, Flicker or 1/*f* noise, burst noise and avalanche noise.

Thermal noise occurs due to the random thermal motion of electrons. For a given circuit component with a resistance *R* the average thermal noise voltage is given by

$$\overline{v^2} = 4kTR\Delta f \ , \tag{2.2a}$$

and the equivalent noise current by

$$\overline{i^2} = \frac{4kT}{R}\Delta f \ , \tag{2.2b}$$

where k = 13.8E-24 J/K is Boltzmann's constant, Δf is the amplifier noise bandwidth and T is absolute temperature. Since the standard definition of noise figure is at T = 290 °K [**1**] this will be the assumed temperature throughout this thesis unless otherwise stated. Since the thermal noise spectrum is frequency independent within the noise bandwidth it contributes to amplifier white noise. The thermal noise voltage or current is minimized for very small or very large values of *R* respectively.

Shot noise is associated with direct current (DC) flow through a p-n junction and is always present in diodes, MOSFETs and bipolar transistors. In a forward biased p-n junction the forward current exists as a result of holes and electrons gaining enough energy to cross the electric field present in the depletion region. Thus the passage of each carrier across the junction is a random event occurring when a specific carrier has sufficient energy and velocity directed toward the junction and the apparent steady forward current is in fact composed of a large number of random independent current pulses [**26**]. The fluctuations that occur in this current are called shot noise and is usually specified in terms of its mean-square variation about the average value as

$$\overline{i^2} = 2qI_D\Delta f \ , \tag{2.3}$$

where q is the electron charge, I_D the average forward current and Δf the amplifier noise bandwidth. The spectrum of shot noise is also frequency independent and thus contributes to white noise.

Flicker noise and burst noise are both frequency dependent and occur at lower frequencies. Flicker noise is caused mainly by traps associated with contamination and crystal defects which capture and release carriers in a random fashion. The time constants associated with this process give rise to a noise signal with energy concentrated at low frequencies [**26**]. Burst noise is not fully understood but does show some relation to the presence of heavy-metal ion contamination. Since the dependence of the noise spectral density on frequency for flicker noise is $1/f$ (pink noise) and that of burst noise $1/f^2$ (brown noise) above a cut-off frequency, these noise sources are not important in super high frequency (SHF) circuits, with the exception of voltage controlled oscillators where flicker noise can be up-converted as phase noise [**4**].

Avalanche noise occurs in reverse biased p-n junctions where electrons in the depletion region acquire sufficient energy to create electron-hole pairs by colliding with silicon atoms. This creates large noise spikes and generally dominates all other noise sources when present. The noise magnitude is proportional to the DC flow [**26**]. This source of noise can be minimized by ensuring the reverse bias voltage is small enough to limit the occurrence of avalanche breakdown.

In summary, for high frequency amplifier circuits, assuming reverse bias is sufficiently low such that avalanche breakdown becomes negligible, the noise sources to contend with are thermal noise and shot noise.

2.3 NOISE IN HBT AMPLIFIERS

The LNA noise figure is tied to the physical noise sources in the transistor which are, for SiGe HBTs, the shot noise associated with the base and collector DC as well as the thermal noise of the base resistance (r_b) [**4**].

Although many virtual resistors such as the output resistance of a transistor are included in the complete transistor model shown in Figure 2.1, these resistances, being virtual, do not contribute to the transistor thermal noise. The actual resistances present in a transistor are the base, emitter and collector series resistances which exist due to the resistivity of the

p- and n-material. In SiGe HBTs the emitter and collector resistances can usually be neglected since the emitter resistance is very small and the collector resistance thermal noise is reduced by the gain of the transistor when referred back to the input. This makes the base resistance the most important contributor of thermal noise. Since this noise is applied at the base of the transistor it is not reduced by the amplifier voltage gain and forms a major limitation on minimum NF.

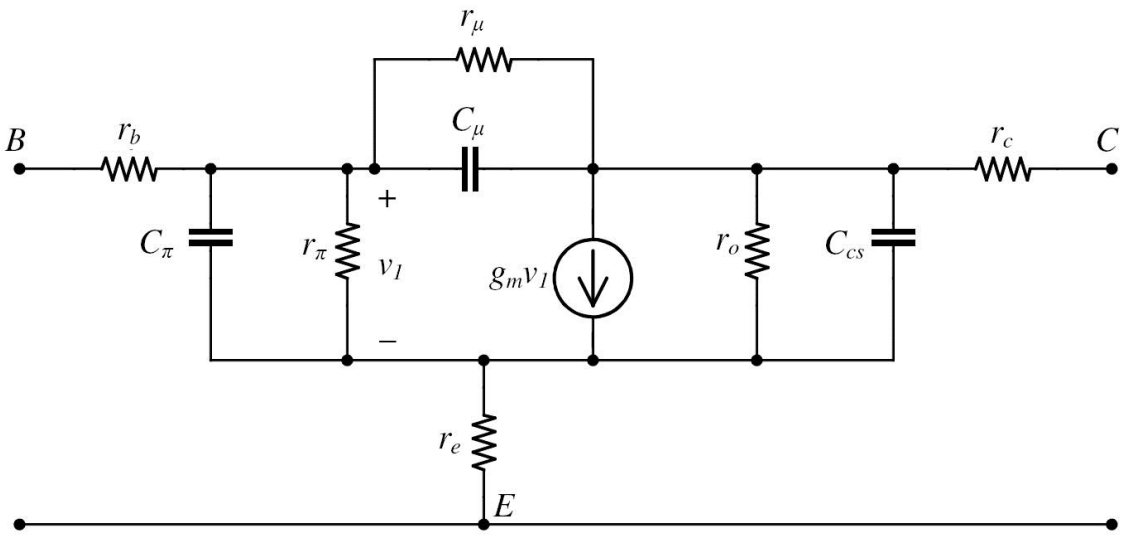

Figure 2.1. Complete bipolar transistor small-signal equivalent circuit.

As discussed in Section 2.2 shot noise is generated by DC flowing in forward [**26**] biased p-n junctions. In bipolar transistors both the base and collector currents introduce shot noise at the base-emitter junction. From the base majority carrier holes cross the base-emitter junction to form the base current and majority carrier electrons in the emitter cross the junction to form the collector current in *npn*-transistors. At the reverse biased collector-base junction the electric field causes a drift process which simply transports the electrons from the base into the collector without adding additional shot noise. The base transit time (τ_F) of the electrons across the base changes the correlation between the base and collector current noise in the common emitter configuration [**4**], however it is feasible to neglect this transit time (effectively assuming the noise is generated in the BC-junction) at frequencies much lower than $f_T/2$ [**8**]. In such cases the correlation admittance seen by the equivalent input noise voltage and current generators is only due to the collector current noise component (see (2.9) and (2.10) in Section 2.3.1) and equal to Y_{11} of the amplifier two-port.

2.3.1 Common-emitter amplifier noise and gain parameters

SHF LNAs are often implemented as narrowband amplifiers using active devices characterised by *S*-parameters and tuned with distributed passive structures. An alternative design technique is a RF analogue approach combining lumped passive devices with the transistor model to achieve the desired functionality [**27**].

The noise optimization methods of these approaches differ significantly. With the lumped element method the equivalent circuit of the transistor with the noise sources described in the previous section are considered with the elements comprising the matching networks and their noise sources in order to define an overall equation for the noise figure indicating which component values could be optimized. With a distributed design the minimum NF of a transistor (NF_{min}) is quantified and the deviation of the source impedance from the optimal noise match determines the final NF of the system. The following discussion assumes the latter approach.

Starting with the equations for a two-port's noise parameters in terms of the power spectral density (PSD) of the equivalent noise current and voltage as well as their correlation as given in [**5**], it can be shown that when written in terms of the intrinsic transistor parameters, the noise parameters of a common emitter amplifier are given by equations (2.4) through (2.7) [**4**].

$$R_n = r_b + \frac{1}{2g_m} \tag{2.4}$$

$$G_{s,opt} = \sqrt{\frac{g_m}{2R_n}\frac{1}{\beta} + \frac{(\omega C_i)^2}{2g_m R_n}\left(1 - \frac{1}{2g_m R_n}\right)} \tag{2.5}$$

$$B_{s,opt} = -\frac{\omega C_i}{2g_m R_n} \tag{2.6}$$

$$NF_{\min} = 1 + \frac{1}{\beta} + \sqrt{\frac{2g_m R_n}{\beta} + \frac{2R_n(\omega C_i)^2}{g_m}\left(1 - \frac{1}{2g_m R_n}\right)} \tag{2.7}$$

R_n is the noise resistance, $G_{s,opt} + jB_{s,opt}$ is the optimal source admittance and NF_{min} the minimum noise figure achieved when optimal noise input matching is used. Equation (2.7) can also be written in the more practically useful form [**8**]

$$NF_{\min} = 1 + \frac{n}{\beta_0} + \frac{f}{f_T}\sqrt{\frac{2I_C}{V_T}(r_E + r_B)\left(\frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{\beta_0 f^2}}, \tag{2.8}$$

where n is the collector current ideality factor, approximately equal to one, except under high current injection bias when its value can exceed 1.2. Equation (2.8) shows that the absolute minimum attainable noise figure is fixed for a specific process through the first and second terms. The third term indicates that NF_{min} is frequency dependent. It is apparent that at a given collector current the noise is primarily a function of four key parameters: the series resistances (r_b and r_e), the unity gain frequency (f_T), and the transistor common-emitter current gain (β) [**28**].

The two terms inside the second square root term become equal at $f = f_T / \sqrt{\beta}$ which defines the transition of NF_{min} from a white noise behaviour to becoming frequency dependent. Below this frequency NF_{min} is proportional to $\sqrt{r_b / \beta}$ which together with the second term indicate the need for high β and low r_b. Above this corner frequency NF_{min} increases with a slope proportional to $\sqrt{r_b} / f_T$ also making high f_T critical for achieving good noise performance. In this case β becomes irrelevant as long as it is sufficiently large (> ~50-100) [**28**].

When examined in terms of the physical noise sources in the transistor it can be seen that higher β reduces the base current (I_B) and the referred collector current shot noise which decreases the PSD of the equivalent input noise current (S_i) significantly as given by [**29**]

$$S_{i_n} = 2qI_B + \frac{2qI_C}{\beta^2}. \tag{2.9}$$

The frequency dependence of the noise current arises from the roll-off of β with frequency above $f_b = f_T / \sqrt{\beta}$ [**26**]. Lowering r_b causes a drop in the PSD of the equivalent input noise voltage (S_v) given by [**29**]

$$S_{v_n} \approx 4kT\left(r_b + \frac{1}{2g_m}\right). \tag{2.10}$$

The dependence of NF on I_C is apparent from both (2.9) and (2.10) through g_m.

The associated gain (G_a) of an amplifier is the power gain that can be achieved when the input of an amplifier is noise matched in order to minimize NF. It has been shown that the associated gain for HBT amplifiers is given by [**29**], [**30**]

$$G_a = \frac{1}{\omega^2 C_{bc} C_i r_b}\sqrt{\frac{g_m r_b + ½}{2}\frac{g_m^2}{\beta} + \frac{(\omega C_i)^2}{2} g_m r_b}\ . \tag{2.11}$$

It can be seen that increasing f_T by decreasing the input capacitance (C_i) serves to increase the gain in addition to improving noise performance. An increased β however decreases the associated gain since G_a is inversely proportional to the square-root of β. This is an important limitation since at low frequencies increasing β is the only means of reducing noise figure [**4**]. Although the base-collector capacitance (C_{bc}) does not impact NF_{min} directly, it does affect G_a which indicates that, in addition to large f_T, a large f_{max} is also desirable and is defined as [**31**]

$$f_{\max} = \sqrt{\frac{f_T}{8\pi r_b C_{bc}}}\ . \tag{2.12}$$

Finally it is seen that G_a increases with I_C through g_m indicating the need for a certain amount of I_C to have sufficient associated gain [**30**]. Equation (2.8) however shows that the NF also increases with g_m which implies a trade-off between NF and associated gain. To better quantify this trade-off the noise measure (M) which includes both the noise factor and associated gain in a single parameter is often used as a figure of merit (FOM) and is defined as [**28**]

$$M = \frac{F-1}{1-\frac{1}{G_a}}. \tag{2.13}$$

2.3.2 Low noise capability of HBTs

The intrinsic properties of SiGe HBTs make them especially well suited for low noise design. The additional freedom offered by band-gap engineering allows SiGe HBTs to simultaneously achieve high β, a high f_T and low r_b all of which are important for noise performance as described in the preceding section. This is in contrast to Si BJTs where these requirements often result in limiting constraints where for example decreasing r_b by increasing the base doping causes a drop in β [**30**]. Through the addition of germanium to the base of the transistor the band-gap energy of the base material is reduced which allows for much higher doping while maintaining good emitter injection efficiency.

A review of four generations of IBM technology [**28**] reveals the improvements in noise performance through both scaling and structural enhancements. Vertical scaling of the base and collector has resulted in a rise in f_T from 47 GHz in 0.25 µm technology to more than 200 GHz and even above 350 GHz in some 0.13 µm processes. With the reduction of base width using a higher Ge mole fraction to maintain a constant total Ge content in the base also increases β [**4**]. As a result of lateral scaling which reduced the minimum emitter area, f_T vs. I_C characteristics have been shifted toward lower currents allowing successive generations to achieve higher f_T at any given I_C value. This is especially desirable since SiGe HBTs typically have the best noise performance at less than 20 % of the peak f_T or f_{max} current density and high-current-density performance may be traded for improved noise at lower current densities [**28**].

Lateral scaling has also reduced the contribution of the sheet resistance of the intrinsic base to the overall r_b as it is inversely proportional to the emitter width. Although r_b could be further reduced by higher doping of the extrinsic base this is seldom done in traditional structures since the higher doping tends to diffuse toward the collector pedestal which increases C_{bc} and thus reduces f_{max} and the power gain. A key improvement in this regard has been the introduction of the raised base structure which is illustrated in Figure 2.2. The raised base decouples r_b and C_{bc} allowing extremely high extrinsic base doping for very low r_b without risk of a trade-off against C_{bc} [**28**].

The improvement of f_T has led to a 2.5 dB reduction in NF_{min} at 26 GHz and reduction of r_b has contributed another 1 dB drop. This gives a total NF improvement of 3.5 dB from the 0.5 µm to the 0.13 µm processes. At 15 GHz NF_{min} remains below 1 dB when I_C is varied

from 5 to 40 mA. The associated power gain is more than 10 dB with the highest value of 13 dB at 40 mA and continuing to rise beyond the maximum current used in the study [**28**].

These results show that HBTs are a good choice for high frequency and low noise applications.

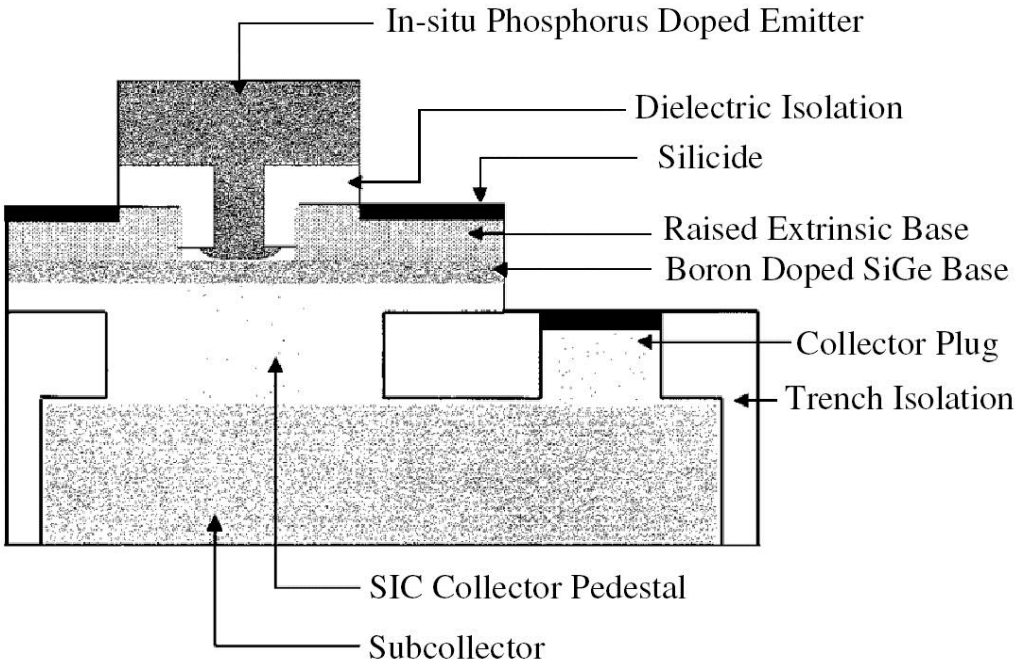

Figure 2.2. Cross section of a raised extrinsic base SiGe HBT [32**].**

2.3.3 Design for minimum transistor noise figure

It was shown in Section 2.3.1 that there is a minimum attainable noise figure for transistors in a given technology. The transistor deviates from this minimum noise figure through its dependence on the collector current through g_m, as well as an increase with frequency at higher frequencies as β starts to roll-off. From (2.7) it can be shown that NF_{min} first decreases with increasing I_C and then increases with I_C monotonically, if the dependence of C_i on I_C for bipolar transistors is observed [**4**]. This is shown in Figure 2.3 and indicates the absolute minimum noise figure that can be attained for this specific transistor by selection of a suitable I_C. Since the power gain is also dependent on I_C the associated gain was traded-off with a smaller NF which occurs at a f_T smaller than the maximum f_T for the device; typically at less than 20 % of the value for peak f_T in SiGe HBTs [**28**].

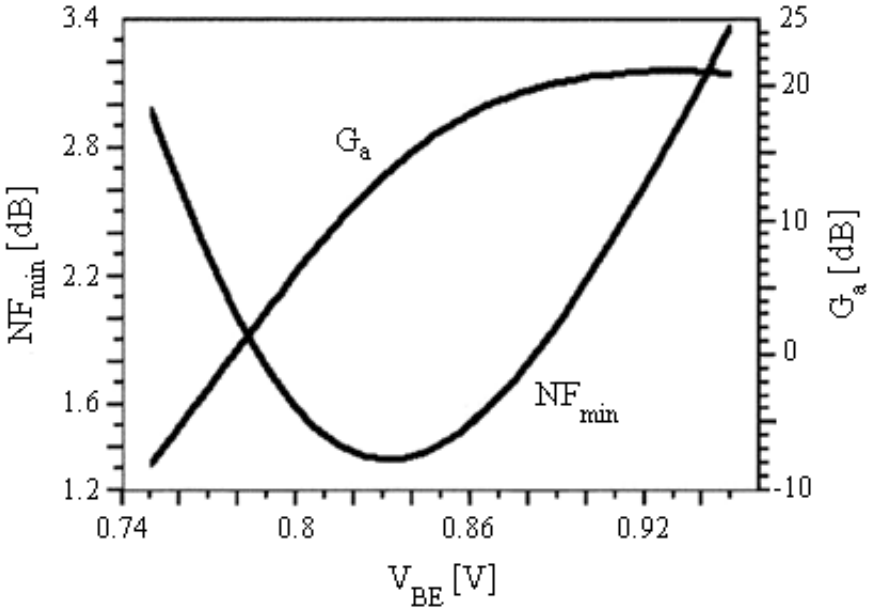

Figure 2.3. Typical minimum NF and current gain vs. VBE characteristic [4].

In selecting an amplifier topology for a multi-stage amplifier the FOM defined in Section 2.3.1 can be used as it captures both noise and available gain characteristics. The noise measure for identical SiGe HBTs in a common-emitter, common-base and cascode configuration was measured [**33**] at the minimum-noise bias and resulted in noise measures: M_{CE}=3.75, M_{CB}=3.40 and M_{casc}=3.47. These results show that for a simultaneous optimal noise and power match a common base amplifier stage would result in the best noise figure, however such a simultaneous match is not feasible for CB-amplifiers and thus a cascode configuration should be used instead [**33**]. Cascode amplifiers have the further advantage of good reverse isolation which simplifies the matching network design and also better frequency response due to reduced Miller multiplication of C_μ in the first transistor.

2.4 LINEARITY OF HBT AMPLIFIERS

The linearity of an amplifier can be quantified by either the 1 dB gain compression point (P_{1dB}) or the third order input intermodulation product (IIP3). P_{1dB} is the input power resulting in a 1 dB drop in the first harmonic power gain due to the output power present in the second and higher order harmonics. The IIP3 is the two tone input power resulting in the first and third harmonic output power becoming equal. It is usually necessary to extrapolate this value since it typically occurs at an input power larger than the onset of

gain compression and it can in fact be shown that P_{1dB} is typically 9.6 dB lower than IIP3 [**34**].

Five sources of non-linearity can be identified in bipolar transistor amplifiers. The collector current transported from the emitter (I_{CE}) is a nonlinear function of V_{BE}. The hole injection into the emitter (I_{BE}) is also a nonlinear function of V_{BE}. The avalanche multiplication current (I_{CB}) is a strong nonlinear function of both V_{BE} and V_{CB}. Finally, C_{BE} and C_{BC} are both nonlinear junction capacitance [**35**], [**36**].

In [**37**] a Volterra-series based approach was used which completely distinguishes individual nonlinearities and is practical in circuits operating in weak nonlinearity such as LNAs. It was found that in HBT amplifiers the nonlinearity is dominated by the $I_{CE} - V_{CE}$ nonlinearity for small collector currents, by the nonlinearity due to avalanche multiplication for 5 mA < I_C < 25 mA, and by the C_{CB} nonlinearity for collector currents above 25 mA.

The $I_{CE} - V_{CE}$ nonlinearity improves with higher collector current. Increasing J_C reduces the net charge density on the collector side of the CB junction which reduces $M - 1$ and thus also improves the avalanche multiplication nonlinearity. Therefore an improvement of IIP3 with collector current is seen until the C_{CB} nonlinearity starts to dominate after which the overall IIP3 is independent of collector current. It was also shown that an optimal V_{CE} exists for maximizing IIP3 for a given I_C [**37**]. This was found to be due mainly to the feedback provided by C_{BC} and the avalanche current.

Since the avalanche multiplication nonlinearity improves with higher J_C, and typical operating currents result in amplifiers operating where this nonlinearity dominates it is also clear why reducing the emitter area usually improves linearity.

Feedback is a well know method for improving linearity by either using local feedback in every amplifier stage or overall feedback between the input and output of the LNA. An improvement in IIP3 of $(1 + A\beta)^{3/2}$ is typically found when feedback is employed, where A is the forward gain and β the feedback gain of the amplifier [**38**].

The C_{BC} and avalanche nonlinearities can be reduced using the cascode instead of common-emitter configuration. With the cascode configuration V_{CB}, the voltage drop over the nonlinear C_{BC}, is greatly reduced, which also reduces the avalanche multiplication [**35**].

LNAs are often implemented as multi-stage amplifiers to achieve sufficient gain. In such cases the overall IIP3 is dominated by the IIP3 of the last amplifier stage, which is reduced by the gain of the preceding stages to find the overall IIP3. Therefore in multi-stage amplifiers the first stage should be optimized for minimum noise as it dominates the overall NF, and the final stage should be optimized for linearity [**39**].

2.5 INPUT MATCHING

Input matching is important in RF applications and even more so in LNA design. Not only is a conjugate match desirable to achieve maximum power transfer, but the final NF of the amplifier is also affected by the input matching network. The noise parameters of a two-port amplifier are the minimum noise figure NF_{min}, the optimal noise admittance $Y_{s,opt}$ and the noise resistance R_n [**5**] which were defined in Section 2.3.1. For an arbitrary source admittance Y_s the noise figure of an amplifier stage is given by

$$NF = NF_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{s,opt}\right|^2, \tag{2.14}$$

where G_s is the real part of Y_s and the other parameters are as defined in Section 2.3.1. The noise figure is minimized when $Y_s = Y_{s,opt}$ and R_n determines the sensitivity of the noise figure to deviations of Y_s from $Y_{s,opt}$. In general, the optimum Y_s for noise matching differs from the optimum source admittance for a conjugate match [**30**].

Various input matching techniques are presented in the following sub-sections followed by a discussion on the trade-offs of the performance measures that are involved [**25**].

2.5.1 Traditional input matching techniques

A number of traditional matching techniques with various tradeoffs exist to achieve both narrowband and wideband input matching. The simplest of these is a resistive match [**40**] where a 50 Ω shunt resistance (assuming a 50 Ω system) is used at the transistor base. Since the transistor input resistance is much larger than 50 Ω this results in a conjugate

match independent of frequency. The disadvantage of a resistive match is the increased voltage noise from the resistor usually leading to an unacceptably high NF. For this reason a resistive match is seldom used in practice.

Resistive shunt-shunt feedback can also be employed with much improved noise performance compared to a simple shunt resistor to ground, but the minimum NF is still not attained [**40**]. Since this configuration uses feedback, stability considerations also become important.

A third alternative is to use a common-base amplifier as the input stage [**40**]. The input impedance of a common-base amplifier is $1/g_m$ and, although sensitive to variations in temperature, a 50 Ω termination can be achieved by selecting I_C such that g_m = 0.02 S. However, this configuration still suffers from a high NF due to the collector current of the transistor not being optimized for low noise in the case of bipolar transistors; also since the common-base amplifier is a current buffer, any noise currents of subsequent stages are referred directly back to the input without reduction [**26**].

Of all traditional input matching techniques inductive emitter degeneration achieves the best noise performance [**17**] and was first introduced in [**41**] to generate the real part of the input impedance required for matching. It has further been shown that simultaneous optimal noise and conjugate matching is possible [**8**] by scaling the transistor emitter length. This technique is described in detail in Section 2.5.3.

2.5.2 Impedance matching in the super high frequency range

When designing amplifiers using the common-emitter or cascode configuration in the SHF range (3 GHz – 30 GHz), also referred to as the centimetre wave range, the transistor is operated far beyond the beta cut-off frequency f_β defined as f_T/β_0 where f_T is the transistor unity gain frequency and β_0 the DC current gain. Since the current gain rolls of at approximately -20 dB/decade above f_β it is found that

$$\begin{aligned}\beta_{RF} &= \frac{\beta_0}{1+\beta_0 \dfrac{C_\pi + C_\mu}{g_m} j\omega} \\ &= \frac{\beta_0}{1+\beta_0 \dfrac{1}{2\pi f_T} j\omega} \\ &\approx -j\frac{\omega_T}{\omega}\end{aligned} \tag{2.15}$$

for sufficiently high ω [**35**] where $\beta_0\omega/\omega_T >> 1$.

For the case where $\omega >> \omega_T/\beta$ one also finds that the impedance of the parasitic base-emitter capacitance (C_π) becomes small compared to the equivalent input resistance (r_π) as proved in (2.16).

$$\begin{gathered}When \quad \omega = \tfrac{\omega_T}{\beta} + \omega' \\ \left|y_{C_\pi}\right| = \omega C_\pi = \tfrac{\omega_T C_\pi}{\beta} + \omega' C_\pi \\ with \quad \omega_T \approx \tfrac{g_m}{C_\pi} \quad and \quad r_\pi = \tfrac{\beta}{g_m} \\ \left|y_{C_\pi}\right| = \tfrac{1}{r_\pi} + \omega' C_\pi \\ \therefore \quad \left|y_{C_\pi}\right| >> y_{r_\pi} = \tfrac{1}{r_\pi} \quad if \quad \omega' C_\pi >> 0 \\ \therefore \quad \tfrac{\omega_T C_\pi}{\beta} + \omega' C_\pi >> \tfrac{\omega_T C_\pi}{\beta} \\ or \quad \omega >> \tfrac{\omega_T}{\beta}\end{gathered} \tag{2.16}$$

This results in the base-emitter impedance (Z_π) being dominated by C_π and thus $Z_\pi \approx 1/(j\omega C_\pi)$.

Input matching is generally performed by generating an equivalent input resistance using either inductive series-series feedback in the emitter (L_E) of the transistor or shunt-shunt feedback between the collector and base terminals. This, together with a series inductor (L_B) at the base, results in an equivalent series RLC circuit seen at the input of the amplifier. The input impedance of such a RLC circuit is

$$Z_{IN} \approx sL_{IN} + R_{IN} + \frac{1}{sC_\pi}. \tag{2.17}$$

The frequency response of S_{11} is then [**12**]

$$S_{11} = \frac{Z_{IN} - R_S}{Z_{IN} + R_S} \approx \frac{s^2 + \frac{1}{C_{IN} L_{IN}}}{s^2 + s\frac{R_{IN} + R_S}{L_{IN}} + \frac{1}{C_{IN} L_{IN}}} \equiv \frac{s^2 + \omega_0^2}{s^2 + s\frac{\omega_0}{Q_{IN}} + \omega_0^2} \tag{2.18}$$

where $R_{IN} = R_s$ has been assumed, ω_0 is the resonant frequency of the RLC circuit and Q_{IN} the quality factor. Since S_{11} has a standard notch transfer function and it is required that $|S_{11}| < -10$ dB over the operating frequency range the Q-factor of the circuit is governed by [**12**]

$$\Delta f_{10dB} = \frac{\omega_0}{6\pi Q_{IN}} \approx \frac{R_{IN} + R_s}{6\pi L_{IN}}. \tag{2.19}$$

It follows that there is a limit on the maximum value of L_{IN} where $R_{IN} = R_s$ is fixed. This alludes to a limit on the bandwidth that can be achieved with this technique in practice and it will be shown that this implementation is indeed better suited to narrowband applications.

Two implementations based on this technique exist: the well known inductive emitter degeneration technique [**8**] as well as a relatively new topology employing capacitive shunt-shunt feedback [**12**].

2.5.3 Inductive emitter degeneration

Figure 2.4 shows the equivalent series RLC-circuit resulting from an emitter degenerative inductor (L_E). At high frequencies (with β defined as in (2.15)) β-multiplication of the emitter inductor results in the equivalent impedance

$$Z_{eq} = j\omega L_E (1 - j\frac{\omega_T}{\omega}) = j\omega L_E + \omega_T L_E \tag{2.20}$$

at the base of the transistor together with the base-emitter capacitance. With an additional series inductor at the base L_B+L_E can be chosen to resonate with C_π at the required centre

frequency, providing a real input impedance of $\omega_T L_E$ which can be chosen as 50 Ω providing conjugate matching for a 50 Ω source impedance.

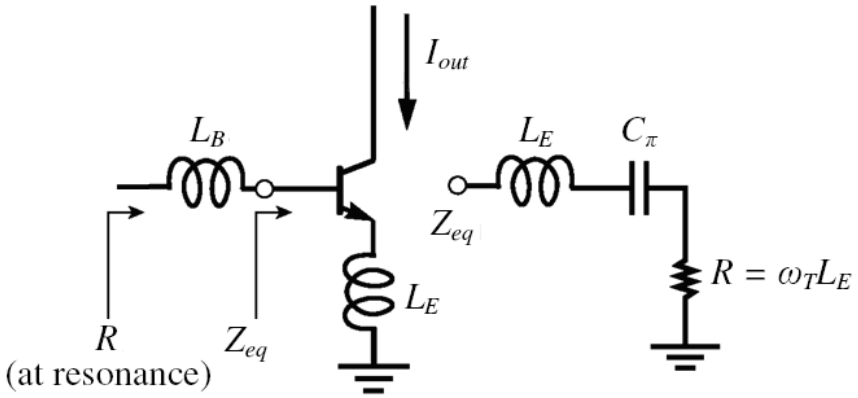

Figure 2.4. High frequency equivalent circuit at the base of an inductively degenerated common-emitter amplifier [11**].**

It has also been shown that simultaneous optimal noise and conjugate matching is possible [**8**] since $R_{s,opt}$ scales inversely with the transistor emitter length and the base inductor reduces the imaginary part of $Z_{s,opt}$ to zero resulting in an optimal noise match being achieved. Such a simultaneous conjugate and optimal noise match also results in the maximum attainable FOM.

Since the technique requires changing the optimal source impedance without increasing the minimum transistor noise figure, the effect of scaling the emitter length on NF should be investigated. The base resistance for a traditional silicon bipolar transistor is given by [**42**]

$$r_b = \frac{\sqrt{\rho_s \rho_c}}{2l_e} + \frac{\rho_s W_{eb}}{2l_e} + \frac{\rho_s w_e}{12 l_e}, \tag{2.22}$$

where ρ_s and ρ_c are the base and contact sheet resistances respectively, W_{eb} is the gap width between the base and emitter, w_e is the lateral emitter width and l_e is the emitter length. If the well known equation for the collector current of a bipolar transistor [**26**] is written in the form

$$I_C = J_S (w_e l_e) \exp\left(V_{BE} \Big/ nV_T \right), \tag{2.23}$$

where J_S is the saturation current density, n the ideality factor (approximately 1 in the process used for this research) and V_{BE} and V_T the base emitter voltage and thermal voltage respectively, and substituted into (2.8) together with (2.22) it can be shown that the minimum noise figure is independent of emitter length. This can also be shown for (2.7) when noted that C_i is dependent on I_C. This allows scaling of the emitter length without affecting noise figure while the emitter width is always kept at the minimum for a specific process since it has a large impact on the minimum noise figure. The dependence of NF_{min} on w_e is mostly due to the increased r_b with increased emitter width as seen in (2.22). Although the structure of SiGe HBTs is significantly more complicated and therefore not accurately described by (2.22) [**43**] the same qualitative result can still be obtained through such emitter scaling [**9**].

It was first suggested in [**8**] that the emitter length of a bipolar transistor could be scaled in order to change the optimal source impedance as both R_n and $R_{s,opt}$ scale with the inverse of emitter length as seen by substituting (2.22) into either (2.4) or (2.5), the latter resulting in the definition for $R_{s,opt}$ as a function of l_e as [**35**]

$$R_{s,opt} = \frac{\omega_T}{\omega}\frac{1}{l_e}\sqrt{\frac{2(r_b \cdot l_e)}{J_C \cdot w_e}V_T}\ , \tag{2.24}$$

where w_e is the emitter width, J_C is the collector current density and V_T the thermal voltage.

The following design steps were proposed:

1) Use simulations to find the collector current density J_C that minimizes NF_{min} and is set through V_{BE} as

$$J_C = J_S \exp\left(V_{BE}/nV_T\right). \tag{2.25}$$

2) Adjust the emitter length such that the optimum source resistance R_{opt} equals the characteristic impedance of the system (usually 50 Ω).

3) Add an emitter inductor L_E to match the real part of the input impedance. If lossless, L_E only changes X_{opt} but does not affect R_{opt}.

4) Add a base inductor L_B to cancel the transistor's input reactance and simultaneously transform the optimum noise reactance to 0 Ω.

The final circuit is then as shown in Figure 2.4.

This technique was used successfully in the design of low noise amplifiers at 1.9, 2.4 and 5.8 GHz [**8**] and also in a 52 GHz cascade LNA using SiGe HBTs [**33**]. It was found that the independence of NF_{min} on emitter length in practice is true for length-to-width ratios (l_E/w_E) larger than ten [**8**]. Furthermore when the finite Q-factor of the passive on-chip inductors, typically 7 to 10, was incorporated into the simulations the noise figure was degraded by 0.7–1.4 dB. This emphasizes the need for high Q-factor passive on-chip inductors.

More recent work done on this matching technique [**9**] points out the three key assumptions in the method discussed thus far:

1) NF_{min} is not a function of the emitter length at the optimal current density.

2) Inductor L_E does not affect R_{opt}, but only changes R_{in}.

3) The magnitudes of the optimal noise reactance and input reactance are always the same ($X_{in} = -X_{opt}$).

It was found that these assumptions do not hold well at mm-wave frequencies (the Ka-band was investigated in [**9**]) mostly due to the collector-base feedback capacitance C_μ. Since the Ku-band is also above 10 GHz it was important to investigate the effect of C_μ on the design of Ku-band amplifiers.

In the design steps above the real part of the input impedance is matched using an emitter inductor. As illustrated by Figure 2.4 an emitter degenerative inductor creates a series RLC-circuit at the input of the transistor which was shown to be

$$Z_{in} = \frac{g_m L_E}{C_\pi} + j\omega L_E + \frac{1}{j\omega C_\pi} = \underbrace{\omega_T L_E}_{R_{eff}} + j\omega L_E + \frac{1}{j\omega C_\pi} \tag{2.26}$$

neglecting C_μ. In this case the emitter inductor does not change R_{opt} but only X_{opt}. However, the input impedance and optimal source impedance changes substantially when C_μ is considered as shown in Figure 2.5, and for a cascode amplifier using the Miller approximation [**9**]

$$j\omega C_M = \frac{\omega^2 g_m L_E C_\mu}{1+(\omega g_m L_E)^2} + j\omega C_\mu \cdot \frac{2+(\omega g_m L_E)^2}{1+(\omega g_m L_E)^2} \tag{2.27}$$

From the real part of (2.27) it can be seen that L_E and C_μ generate a noiseless shunt conductance. The effect of this shunt conductance is illustrated in [**9**]. It can be seen that the optimal noise matching resistance does change with L_E through C_M (the Miller capacitance resulting from C_μ), and thus the L_E required for R_{in} = R_{opt} and X_{in} = –X_{opt} is no longer the same. This means that R_{opt} = R_{in} = 50 Ω is no longer the optimal value for simultaneous noise and conjugate match since X_{opt} is no longer equal to –X_{in} at that L_E value. Since the conductance of C_M is noiseless the value of L_E does not affect NF_{min}.

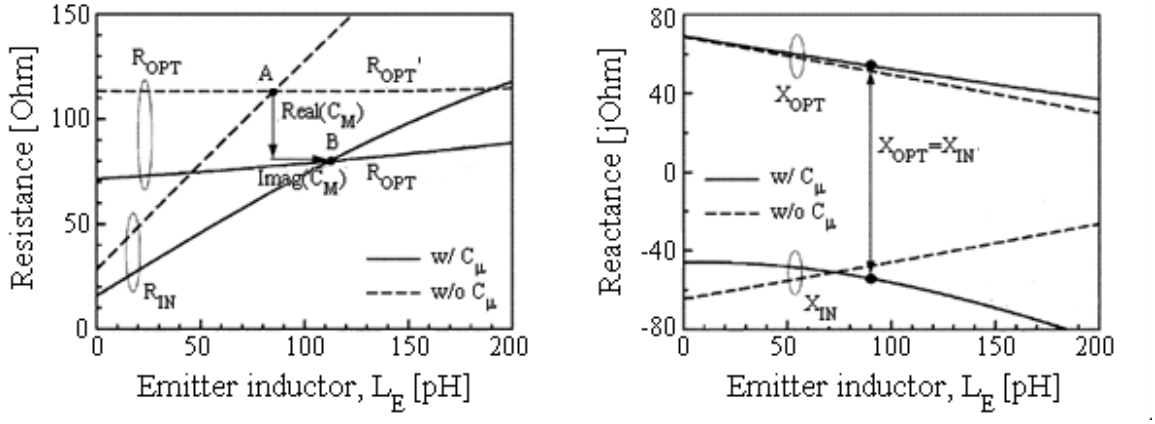

Figure 2.5. Simulated input and optimal noise resistance and reactance with and without Cμ [9].

To find the closest possible power match while still matching for optimum noise figure it is suggested [**9**] to minimize the reflection coefficient

$$\left|\Gamma_{opt-in}\right| = \left|\frac{Z_{opt} - Z_{in}^*}{Z_{opt} + Z_{in}^*}\right| \tag{2.28}$$

by adjusting the value of L_E. It is then possible to match for minimum noise figure at the resonance frequency with a single base inductor. At frequencies where the base inductor parasitic capacitances become important R_{opt} should be chosen larger than the characteristic impedance when adjusting the emitter length to compensate.

It has also been shown [**44**], and this was confirmed in [**9**], that there is some dependence of NF_{min} on l_E in SHF circuits and thus its effect should be taken into account for Ku-band designs. Assuming an optimal noise and power match condition with emitter and base inductors as described in Section 2.3.3 new forms of analytical equations were derived for the transistor IIP3, gain and NF and is shown as functions of collector current and emitter length in Figure 2.6 [**44**].

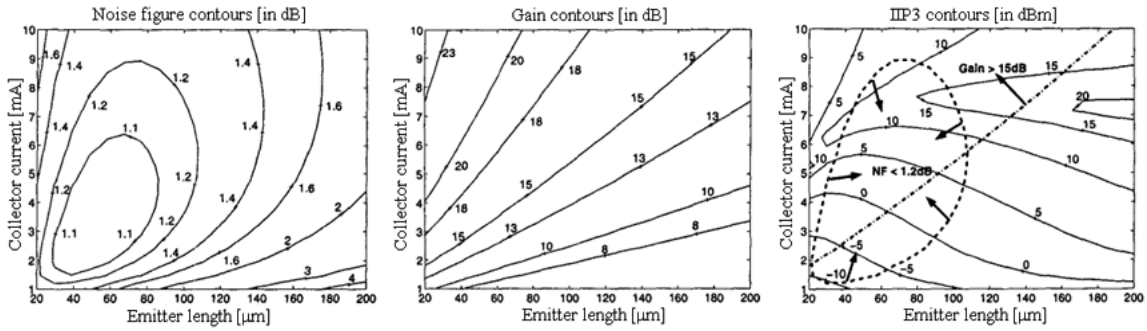

Figure 2.6. Noise figure, gain and IIP3 contours as a function of emitter length and collector current for an input impedance matched LNA at 2 GHz [44**].**

These equations/graphs can be used to design for a given NF, gain and IIP3 as indicated in the right most graph of Figure 2.6. The limit on NF and gain is drawn on the IIP3 plot to indicate the design space. In this specific design it was found that the IIP3 is 0 dBm at the optimum noise figure design point, however an IIP3 of 15 dBm was achievable with only a 0.15 dB increase in noise figure which is clearly the better design point. This shows the importance of considering all amplifier characteristics in choosing the operating point of a transistor. It is also important to note that fabrication tolerances in the emitter length will affect the amplifier performance.

Figure 2.7 shows the dependence of R_{opt} on emitter length and collector current with the plot of NF_{min} [**9**]. This is a further design constraint. To simplify the design of the first amplifier stage the gain may be regarded as less important since the required amplifier gain will be provided by subsequent stages. Power consumption places an upper limit on the

collector current, however for a substantial improvement of other amplifier characteristics slightly higher power consumption may be justified.

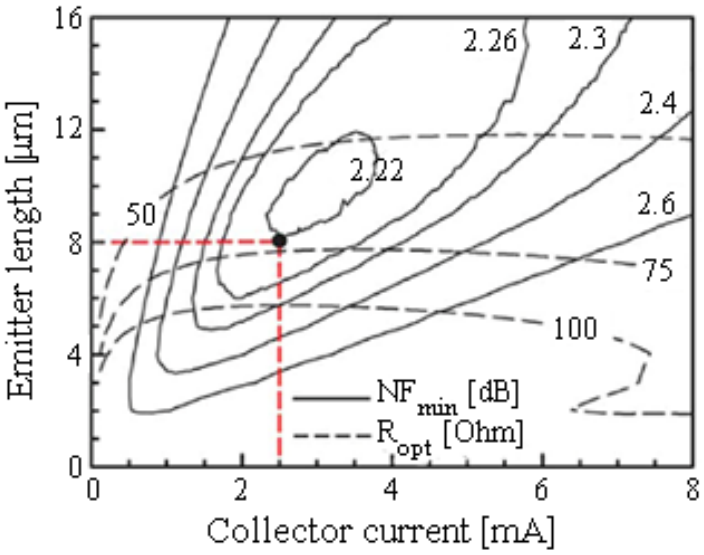

Figure 2.7. Simulated minimum NF and optimal noise resistance contour as a function of emitter length and collector current without emitter degeneration [9].

Form the above discussion it is clear that the selection of emitter length provides an important extra degree of freedom in the design of low noise amplifiers which may be easily overlooked as device dimensions do not form part of the traditional design parameters as is the case with MOSFETs.

The ability to match for optimum noise figure while achieving near optimal power matching makes this matching technique very attractive. However, a major disadvantage is that matching occurs only at resonance. In wideband applications this means that gain will degrade rapidly for frequencies away from the resonant frequency. The low Q-factor of the equivalent RLC circuit required for the S_{11} specification also severely degrades the NF as shown later in Section 2.6.1. Finally it was shown that the collector-base feedback capacitance and Miller effect neglected in the design equations modify the input impedance and thus the performance of implemented circuits differ from theoretical expectations.

2.5.4 Capacitive shunt-shunt feedback technique

An alternative method for generating an equivalent input RLC circuit which requires only one inductor, as opposed to the emitter degeneration technique which requires two area

consuming inductors, has been proposed which uses capacitive shunt-shunt feedback between the collector and base terminals as shown in Figure 2.8 [**12**].

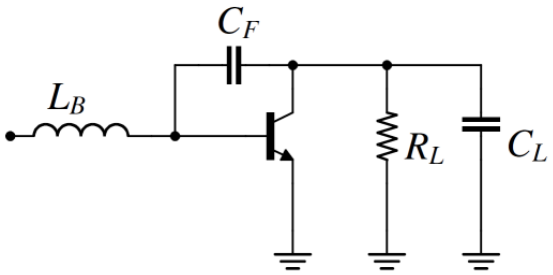

Figure 2.8. Circuit diagram of a capacitive shunt-shunt feedback circuit used to produce an equivalent input RLC circuit [12**].**

Using small-signal analysis the Miller impedance at the base of the transistor resulting from the feedback capacitor and load reactance can be written as

$$Z_M = \frac{1}{j\omega \underbrace{C_{BC}(1+g_m R_L)}_{C_M}} + \underbrace{\frac{R_L}{1+g_m R_L}\left(1+\frac{C_L}{C_{BC}}\right)}_{R_M}. \tag{2.29}$$

In this equation g_m is the transistor transconductance, C_{BC} the total base-collector capacitance comprised of the base-collector capacitance, C_μ, and an intentionally added capacitance, C_F, in parallel with C_μ where necessary. R_L and C_L are the respective parallel connected load resistance and capacitance as shown in Figure 2.8.

Thus the Miller impedance can be represented as an equivalent series resistor (R_M) and capacitor (C_M). This series combination can be converted to an equivalent parallel combination and can be combined with C_π which is also in parallel. Finally this total impedance can be converted back to a series RC circuit which forms the input impedance. The two components are then given by [**12**]

$$R_{IN} = \frac{R_L}{1+g_m R_L}\left(1+\frac{C_L}{C_{BC}}\right)\left(\frac{C_M}{C_\pi + C_M}\right)^2 \approx 50\,\Omega \tag{2.30a}$$

$$C_{IN} = C_\pi + (1+g_m R_L)(C_\mu + C_F) \tag{2.30b}$$

A base inductor is then used to set the resonant frequency of the circuit with C_{IN} similar to the emitter degeneration case.

A combination of inductive degeneration and capacitive feedback has also been used in with a cascode configuration [**45**]. The use of C_F provided an additional degree of freedom allowing improved linearity without degrading the NF.

2.5.5 LC-ladder input matching network with emitter degeneration

Both the emitter degeneration and capacitive feedback techniques are narrowband amplifiers due to the equivalent series RLC circuit at the input which is tuned to a centre frequency. The bandwidth is determined, and ultimately limited by the Q-factor of this RLC circuit.

As an alternative to using a low Q-factor series RLC circuit for input matching, a fourth-order doubly terminated bandpass filter has been used to produce a uniform input impedance over an arbitrary bandwidth through proper selection of the reactive elements [**11**]. This is illustrated in Figure 2.9. Inspection of the filter circuit reveals that the series RLC circuit required for the filter can be generated using the equivalent input circuit of the transistor, and thus a wideband 50 Ω input match can be achieved.

The values of the reactive elements are determined based on the upper (f_H) and lower (f_L) corner frequencies of the matched bandwidth by [**11**]

$$L_1 \approx \frac{R_S}{2\pi f_L} \quad and \quad C_2 \approx \frac{1}{2\pi f_L R_S} \tag{2.31a}$$

$$L_2 \approx \frac{R_S}{2\pi f_H} \quad and \quad C_1 \approx \frac{1}{2\pi f_H R_S} \tag{2.31b}$$

Two disadvantages of this configuration can however be identified. The series capacitance, C_2, (as in Figure 2.9) is the constant base-emitter capacitance of the transistor. From (2.31) the value of this C_π is then dependent on ω_L through

$$C_\pi = C_2 = \frac{1}{\omega_L Z_0}. \tag{2.32}$$

This can be substituted into the well know equation for ω_T

$$\omega_T = \frac{g_m}{(C_\pi + C_\mu)} \approx \frac{I_C}{V_T C_\pi} = \frac{I_C}{V_T C_2} \tag{2.33}$$

resulting in I_C being restricted to [**11**]

$$I_C = \frac{\omega_T V_T}{\omega_L Z_0}. \tag{2.34}$$

This prohibits the arbitrary selection of collector current to optimize NF or power consumption.

A further disadvantage is the pole introduced at the lower corner of the matched bandwidth by the input matching network. The current flowing into the matching network can be approximated as the source voltage divided by $2R_S$ over the matched bandwidth. The transistor output current is proportional to the base-emitter voltage which is the voltage over the series capacitor in the equivalent filter circuit since both the inductance and resistive parts are generated by the base and emitter inductors. The voltage over C_2 is given by [**11**]

$$v_\pi = \frac{v_s}{2R_S} \cdot \frac{1}{j\omega C_2} \tag{2.35}$$

which becomes

$$v_\pi = v_s \frac{f_L}{2f} \tag{2.36}$$

with the substitution of (2.31a) indicating a pole at the lower cut-off frequency. It is possible to compensate for this pole by using an inductive load.

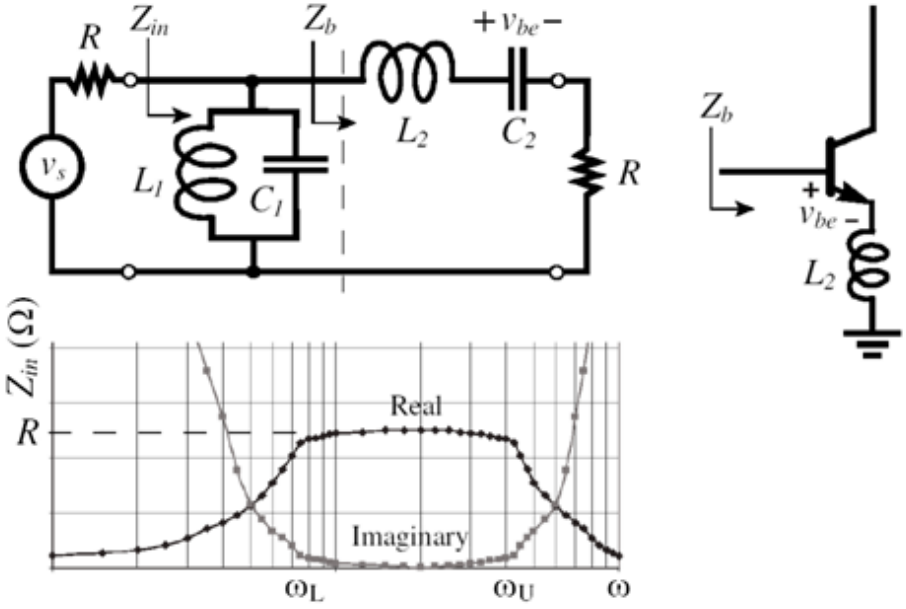

Figure 2.9. Band-pass resistor-terminated ladder filter, its input impedance vs. frequency and similarity with common-emitter amplifier degenerated with an inductor [11].

2.5.6 Wideband matching using shunt-shunt feedback

Feedback is often implemented in amplifier design as a means to linearize the gain, extend the amplifier bandwidth and also for input matching as described in Sections 2.5.3 and 2.5.4. A combination of series-series feedback in the emitter and shunt-shunt feedback between the base and collector has been used in [**6**] to achieve wideband matching as illustrated in Figure 2.10.

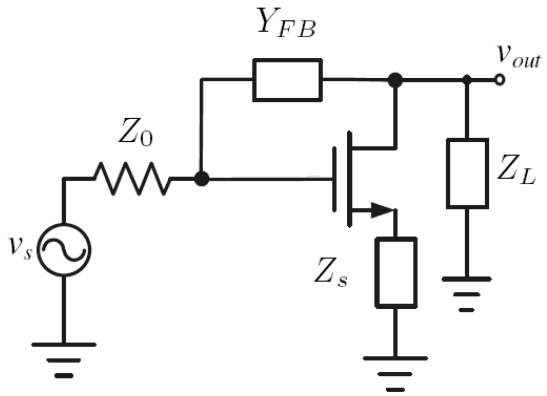

Figure 2.10. An emitter degenerated shunt-shunt feedback amplifier [6].

This configuration has been used to generate a combination of negative feedback and a controlled amount positive feedback at the high frequency end of the amplifier to achieve a

flat gain over the entire ultra wideband (3.1-10.6 GHz). Using the Miller effect a simultaneous wideband noise and power match was also achieved. The shunt-shunt feedback network is shown in Figure 2.11. The inductor L_d compensates for the typical gain roll-off of the transistor. The feedback network was designed to consist of a resistive component providing negative feedback over most of the amplifier bandwidth. A frequency dependent component (an inductor) was added to provide positive feedback at the higher frequency end, thereby compensating for the remaining gain roll-off of the transistor. A graphic design method to aid the design of the feedback network has been proposed [**7**].

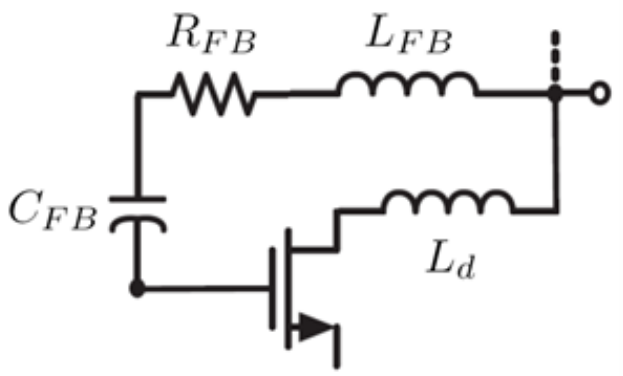

Figure 2.11. Shunt-shunt feedback network achieving a wideband flat gain response [6**].**

To perform input matching the Miller theorem was used to convert the feedback impedance to a shunt impedance at the input. The equivalent input impedance could be modelled as a parallel capacitor and resistor combination. This is due to the decreased effective inductance as the Miller effect decreases with the gain roll-off resulting in a capacitive reactance. This reactance was matched using a series inductor, which was also used to set the input impedance to the system's characteristic impedance as described earlier. The pad capacitance together with the inductor was used to absorb the input capacitance over a wide bandwidth resulting in an approximate wideband real input impedance. Thus a simultaneous noise and power match was achieved [**6**].

2.6 PERFORMANCE MEASURE TRADE-OFFS

Although all the matching techniques discussed in the previous section can be used to achieve good input matching, observations can be made regarding the trade-offs of NF, gain and linearity for the various configurations and are discussed next.

2.6.1 Noise figure

As mentioned earlier the matched bandwidth of the input impedance when using a narrowband matching technique is extended by lowering the Q-factor of the equivalent input RLC circuit. This however is in conflict with the goal of achieving high gain at ω_0 and it can also be shown that the collector current contribution to the NF is inversely proportional to the square of the Q-factor [**11**].

For a low-Q input RLC circuit $s^2 L_B C_{IN} \approx 0$ holds over the band of interest [**12**] and hence the NF contribution due to the collector current is given by

$$\begin{aligned} n_{ic} &\approx \frac{g_m}{2} Z_0 \left(\frac{\omega_0}{\omega_T} \right)^2 \\ &\approx \frac{R_S}{2g_m} \cdot (C_\pi + C_\mu)^2 \cdot \omega_0^2 \end{aligned} \tag{2.37}$$

which, when noting that $Q_{IN} = 1/\omega C_\pi R_S$, neglecting C_μ becomes

$$n_{ic} \approx \frac{1}{2g_m R_S Q_{IN}^2}. \tag{2.38}$$

This clearly indicates the trade-off between the NF and the input matched bandwidth.

In reality the base current also contributes to the NF and its contribution increases with Q_{IN} [**12**]. This means that an optimal Q_{IN} exists for achieving a minimum NF and can be set through proper transistor sizing. In addition it is well known that an I_C exists which results in minimum NF since collector current initially decreases with I_C while NF increases with I_B.

This allows use of the LNA optimization technique first formulated in [**17**] which has been adapted for use with bipolar transistor amplifiers in [**12**]; however the optimization is still restricted by the Q-factor requirement of the input matching.

Clearly it is desirable to decouple the input matching bandwidth from the input Q-factor to allow the Q-factor to be optimized for NF. The wideband LC-ladder matching network achieves this since the matched bandwidth is instead determined by the ladder filter

elements as in (2.31a) and (2.31b). The only remaining constraint on the input capacitance then results from ω_L through (2.32).

2.6.2 Linearity

While NF places a lower limit on the dynamic range of a LNA the IIP3 determines the upper limit. IIP3 is especially important in wideband LNAs where many signals stronger than the signal of interest may exist at surrounding frequencies compared to the narrowband case where out of band interference is filtered.

In the narrowband case it can be shown that the IIP3 is inversely proportional to the square of f_T [**11**]. This shows that maximizing f_T in order to minimize NF lowers (worsens) the IIP3 of the amplifier indicating a design trade-off.

In the wideband case, such as in Figure 2.9, the IIP3 can be defined as [**11**]

$$V_{IIP3_{LNA}} \approx 4\sqrt{2}V_T \cdot \left(1+\left(\frac{I_C \omega L_E}{V_T}\right)^2\right)^{3/4} \tag{2.39}$$

showing that the IIP3 improves with frequency in contrast to the NF, and the linearity can be improved by increasing the feedback through L_E. It was shown in [**45**] that feedback through an additional C_F also improves the IIP3 at the cost of gain. To maintain constant gain the collector current can be increased and the emitter area modified to maintain a constant J_C.

2.6.3 Gain

Although the first stage of a LNA typically focuses on achieving a low NF since a further amplifier stage can provide additional gain, the gain of the first stage remains important as it serves to reduce the noise of a second stage when referred to the input. In addition it is desirable to use a single stage LNA wherever possible to reduce physical size and power consumption.

As discussed, the magnitude of the current gain at the frequency range of interest for the applicable transistor process is given by $\beta = \omega_T/\omega$ and subsequently the power gain also increases with ω_T [**35**]. This satisfies intuitively why IIP3 would decrease with increased

f_T, which is a result of the higher gain. Increasing f_T however requires increased J_C which degrades the NF and thus NF must often be sacrificed to achieve a required gain specification.

A disadvantage of the techniques using capacitive feedback is that the gain is reduced further by the additional feedback. This will result in less reduction of the NF of a second amplification stage when referred to the input. The resulting higher input referred noise will then worsen the NF. This indicates the importance of considering all relevant design constraints in selecting the best amplifier topology.

2.7 ON-CHIP PASSIVE INDUCTORS

As the demand for RF ICs grew and devices started operating at higher frequencies requiring smaller inductor values, the use of on-chip inductors have come into widespread use. Although passive on-chip inductors allow for complete integration of RF applications, it comes at the cost of very large chip area and in many applications for example LNAs completely dominate the required chip area. These inductors also suffer from a low Q-factor (usually in the range of 7 to 15) which, to a large extent, is due to the poor permittivity of the silicon substrate and metal resistance. Higher substrate loss at high frequencies causes a further roll-off of the already low Q-factor as frequency increases.

Three main types of inductors can be integrated on chip [**46**]. Microstrip transmission line inductors are created by high-impedance transmission lines. However this technique is only available at very high frequencies such as the 60 GHz band where wavelength becomes comparable to the chip area. Even in these cases the transmission lines are costly in chip area and the narrow width of the lines introduce extra losses. With coplanar waveguide inductors both the centre conductor and the ground metal are in the top metal layer. Most of the electromagnetic field concentrates at the slot region minimizing the substrate loss. Although this inductor type exhibits the highest Q-factor it requires a very large chip area due to the ground metal also present on the metal layer. Finally, line inductors offer the highest inductance for a given chip area and are often implemented as spiral inductors. The smaller chip area tends to increase the Q-factor, however the magnetic field penetrates the lossy substrate and thus only moderate Q-factors can be achieved.

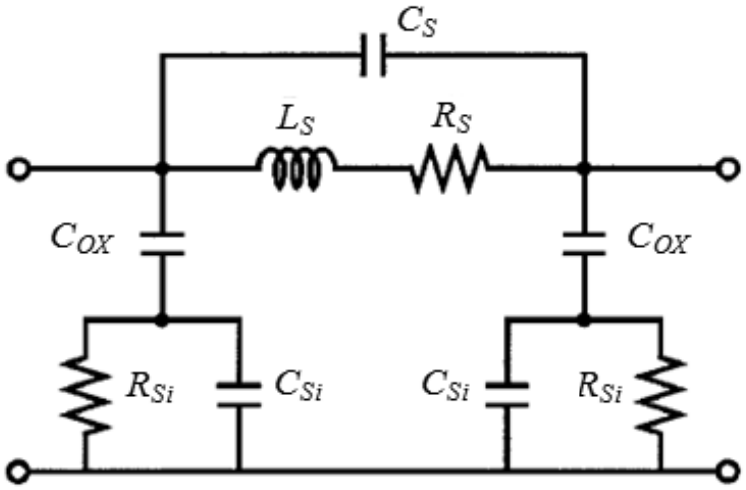

Figure 2.12. Lumped physical model of a spiral inductor on silicon [47**].**

A physical model which is commonly used to represent an on-chip spiral inductor and which also shows the introduced parasitic elements is illustrated in Figure 2.12 [**47**]. The series inductance is the desired component and results from the self inductance of the metal wire as well as the mutual inductance between the turns. The series resistance is due to the resistivity of the metal which is the dominant cause of low Q-factor at lower frequencies. The series capacitance results from the capacitive coupling between the spirals and the underpass of the inductor. The oxide capacitance between the inductor and the substrate as well as the capacitance and resistance of the silicon substrate are modelled as shunt components at the input and output of the inductor model.

The large number of parasitic elements involved in spiral inductor layout emphasizes the need for techniques to reduce these effects. The series resistance is a major contributor to low Q-factor and can be reduced by increasing the conductor thickness [**48**]. However, a disadvantage of this is that the inductance is inversely proportional to the metal thickness; and the skin effect becomes more pronounced as the thickness is increased which serves to increase the resistance in the higher RF range. The eddy current effect occurs when a conductor is subjected to time-varying magnetic fields and also contributes to the series resistance. These eddy currents manifest themselves as skin and proximity effects, where the skin effect causes the current in a conductor to induce eddy currents in the conductor itself and the proximity effect occurs when eddy currents are induced in a nearby conductor. In both cases the eddy currents serve to reduce the current flow and thus add to the series resistance. The eddy current effect is much less in the parallel turns of a planar spiral inductor, compared to the coupling between the conductors of stacked on-chip

inductors which is one reason for even further reduced Q-factor in stacked passive inductors [**47**].

Substrate loss is another major limitation of integrated inductors due to the high permittivity of silicon dioxide (ε_r = 3.9) and is the dominant factor in determining the self-resonant frequency. The relatively high conductivity of the doped substrate has further negative impact on performance. Since the inductor dimensions are usually comparable to the substrate thickness and much larger than the oxide thickness, the substrate capacitance and resistance are approximately proportional to the area of the inductor [**47**]. The substrate type however is also important in determining the substrate capacitance and resistance and this model is only valid for uniform substrate doping. It has been shown that higher doping result in higher capacitance and thus a lower self-resonant frequency [**48**].

Very thorough equations for the derivation of these parasitic effects are available [**47**] and are not repeated here. Losses can be minimized by proper selection of the conductor width, spacing and metal thickness for given substrate parameters. It may also be desirable to optimize for either low metal resistance at lower frequencies or lower substrate capacitance at high frequencies. The optimization of an inductor is crucial to achieve good performance, and computer optimization of the layout can achieve up to 50 % improvement in the Q-factor over un-optimized designs [**48**]. Such optimization software has been developed and is discussed in [**49**].

2.8 ACTIVE INDUCTORS

Active inductors provide a useful alternative to low Q-factor passive on-chip inductors. The parasitic elements of the active devices still limit the attainable Q-factor, however Q-factors in the high tens up to 100 are usually attainable using bipolar transistors. The main disadvantages of active inductors are increased power consumption, increased electrical noise from the active devices and limited dynamic range [**50**]. The noise introduced can be as much as 100 times larger than for a passive inductor [**51**]. This means the use of active inductors should be carefully considered as the increased noise makes it unsuitable for most low noise applications. Increased power consumption is also undesirable in most integrated applications, especially in portable devices.

Apart from the high Q-factor active inductors have the further advantage of offering a significant reduction in chip area compared to using on-chip passive spiral inductors. A three inductor LNA design has been reported where a 25 % reduction in chip area from 0.83 mm^2 to 0.6 mm^2 was achieved by implementing an active load inductance while doubling the amplifier's power consumption from 18.3 mW to 40.8 mW [**10**]. Although its use as a load inductance reduces the effect on the NF, the doubling of power consumption should be weighed carefully against the need for higher integration density in a specific application.

Many active inductor circuits employ a gyrator approach. An ideal gyrator is a linear two-port network that neither stores nor dissipates energy described by the volt-ampere characteristic [**50**]

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & g \\ -g & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{2.21}$$

where g is a designable transconductance parameter known as the gyration ratio. This implies that two voltage controlled current sources are required as shown in Figure 2.13. With the gyrator terminated in a capacitive load, the driving point input impedance is given by

$$Z_{in} = s\frac{C}{g^2}. \tag{2.22}$$

This is equivalent to an inductor $L = C/g^2$ and for an ideal lossless gyrator the Q-factor is infinitely large.

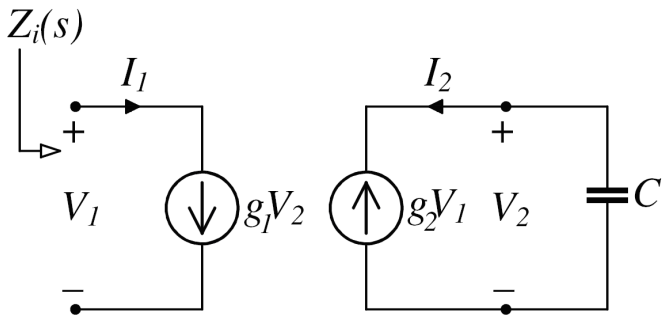

Figure 2.13. Two-port equivalent of an ideal gyrator terminated in a capacitive load resulting in an inductive input impedance [50**].**

In practical gyrator circuits both transconductance amplifiers will introduce parasitic elements. Not only will they have finite input and output resistances but also parasitic input and output shunt capacitances, as well as a feedback capacitance. In HBT amplifiers the input capacitance is derived from the depletion and diffusion components of the base-emitter junction capacitance and also from Miller multiplication of the base-collector junction capacitance [**50**] which can be quite large. The output capacitance in bipolar circuits is due to the collector-substrate capacitance which, depending on the amount of Miller multiplication, may not be a dominant energy storage element [**50**]. When the load capacitance value is calculated the parasitic capacitances at the port should be taken into account as this will serve to increase the effective capacitance. The input and feedback capacitances pose bigger problems which are discussed next.

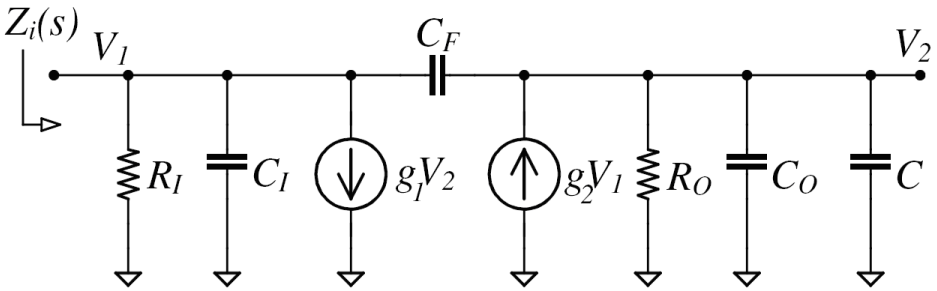

Figure 2.14. Linearized high frequency two-port equivalent circuit of an active inductor [50**].**

The active inductor gyrator circuit can be represented by the equivalent circuit in Figure 2.14. The input impedance of this circuit is [**50**]

$$Z_i(s) = \frac{R_e + sL_e}{1 + \left(\frac{2\zeta}{\omega_n}\right)s + \left(\frac{s}{\omega_n}\right)^2}. \tag{2.23}$$

At low frequencies the effective inductance L_e and series resistance R_e are given by

$$L_e \approx \frac{C_O + C_F + C}{g_1 g_2}, \tag{2.24}$$

and

$$R_e = \frac{1}{g_1 g_2 R_O}, \tag{2.25}$$

resulting in a finite Q-factor. Furthermore the denominator indicates undamped resonance at a frequency ω_n which is given by [**50**]

$$\omega_n = \sqrt{\frac{1}{L_e\left[C_I + \frac{C_F(C_O+C)}{C_O+C_F+C}\right]}}. \tag{2.26}$$

Thus the inductance produced at the input port effectively resonates with the net shunt input capacitance which limits the useful operating range of the active inductor. To ensure the stability of the circuit, g_2 (refer to Figure 2.14) should be larger or equal to g_1. If $g_2 \approx g_1$ and R_O is large, the damping factor (ζ) is given by

$$\zeta \approx \frac{\omega_n L_e}{2R_I}, \tag{2.27}$$

which shows that increasing the input resistance serves to increase the damping factor thereby circumventing potential oscillation problems [**50**].

Figure 2.15 shows a practical implementation of an active inductor with its equivalent circuit. The parallel capacitance is due to the input capacitance of transistor Q_1. The inductance is determined by the transconductance of the transistors and also by the base-emitter capacitance of transistor Q_2, which acts as the capacitive load for the gyrator circuit. This means that the inductor value could be increased by adding additional parallel capacitance between the base and emitter of this transistor; however this comes at the cost of bandwidth [**52**].

The ratio g_m/g_{ds} has also been identified as an indicator of active inductor performance, as the limited g_{ds} of FETs unavoidably raises the series resistance and degrades the inductor Q-factor [**52**]. Therefore using bipolar transistors improves the performance of the active inductor since the g_m/g_{ds} ratio can be in the order of thousands. The limitations of bipolar transistors include finite β, however this has little influence for β values above 100. The base-spreading resistance has a much greater impact on performance and should be kept to a minimum which can be done by using an appropriate transistor structure, usually with

multiple base contacts and a long stripe-shaped emitter region [**52**]. Another major advantage of using bipolar active inductors is its low power consumption compared to its FET counterpart. Only a fraction of the operating current is required to achieve similar performance [**52**].

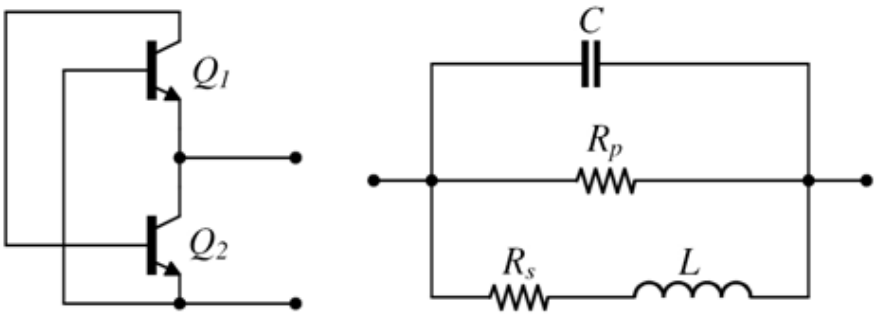

Figure 2.15. A two transistor active inductor configuration and its equivalent circuit representation [52**].**

A Q-factor enhancing method has been proposed [**52**] for this topology where a resistance is added in series with the base of the feedback transistor. The series resistor adds additional negative resistance to the circuit which serves to reduce losses at certain frequencies [**53**], [**54**]. This is especially useful in FET circuits since their lower gain and drain-source resistance reduces the Q-factor. However this is a narrowband technique and thus less suitable for wideband applications, indicating the need for bipolar transistors with inherent high gain in wideband designs.

2.9 CONCLUSION

The critical role of the LNA in a wireless receiver module makes LNA optimization an ongoing research topic where significant improvements are still being made. Since the input matching network is the determining factor in the NF for a given transistor technology, this has been identified as an area that would benefit from further research.

Both emitter scaling and shunt-shunt feedback can be used to achieve a simultaneous noise and power match, but the emitter scaling technique only provides an optimal match at resonance. Furthermore, due to the low Q-factor of the equivalent input circuit standard emitter degeneration configurations are not ideal for achieving a wideband low NF. This suggests that a wideband approach such as the LC-ladder input matching technique is the better choice in wideband LNA design.

The feedback offered by C_F in the capacitive shunt-shunt feedback configuration has proven to be an effective means of both generating an equivalent input RLC circuit, as well as improving linearity without degrading the NF. This technique also requires one less inductor compared to emitter degeneration, resulting in a smaller physical amplifier size.

Based on the findings in this chapter using a LC-ladder matched amplifier with capacitive shunt-shunt feedback a wideband conjugate match could be achieved. The matching bandwidth is decoupled from the Q-factor of the equivalent input circuit by the LC-ladder and C_2 is no longer restricted to the value of C_π due to the Miller capacitance resulting from C_F, thus overcoming many of the shortcomings identified in existing LNA configurations [**25**]. To the author's knowledge such a configuration has not been implemented.

Although geometry scaling and higher operating frequencies have enabled the use of on-chip inductors, allowing for the complete integration of RF circuits on chip, they remain an important limitation in such designs due to low Q-factor. The large parasitic resistance is especially important where NF is considered. At mm-wave frequencies using microstrip transmission lines are the most feasible implementation for inductors. In the SHF range the use of spiral line inductors offers the highest inductance per chip area and should be used and optimized as discussed in [**49**].

Active inductors are an alternative to passive on-chip inductors which achieves very high Q-factors and reduces chip area. This however comes at the cost of both higher noise and higher power consumption making them unsuitable for LNA input matching networks. Depending on the amount of noise reduction offered by the gain of preceding amplifier stages the use of active inductors as load inductors may be feasible.

To improve the linearity of the LNA local and/or overall feedback can be implemented and the cascode configuration can be used to reduce V_{CB}.