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LC-LADDER AND CAPACITIVE SHUNT-SHUNT FEEDBACK LNA MODELLING FOR WIDEBAND HBT RECEIVERS

by

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SUMMARY

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Although the majority of wireless receiver subsystems have moved to digital signal processing over the last decade, the low noise amplifier (LNA) remains a crucial analogue subsystem in any design being the dominant subsystem in determining the noise figure (NF) and dynamic range of the receiver as a whole.

In this research a novel LNA configuration, namely the LC-ladder and capacitive shunt-shunt feedback topology, was proposed for use in the implementation of very wideband LNAs. This was done after a thorough theoretical investigation of LNA configurations available in the body of knowledge from which it became apparent that for the most part narrowband LNA configurations are applied to wideband applications with suboptimal results, and also that the wideband configurations that exist have certain shortcomings.

A mathematical model was derived to describe the new configuration and consists of equations for the input impedance, input return loss, gain and NF, as well as an approximation of the worst case IIP3. Compact design equations were also derived from

this model and a design strategy was given which allows for electronic design automation of a LNA using this configuration. A process for simultaneously optimizing the circuit for minimum NF and maximum gain was deduced from this model and different means of improving the linearity of the LNA were given. This proposed design process was used successfully throughout this research.

The accuracy of the mathematical model has been verified using simulations. Two versions of the LNA were also fabricated and the measured results compared well with these simulations. The good correlation found between the calculated, simulated and measured results prove the accuracy of the model, and some comments on how the accuracy of the model could be improved even further are provided as well.

The simulated results of a LNA designed for the 1 GHz to 18 GHz band in the IBM 8HP process show a gain of 21.4 dB and a minimum NF of only 1.7 dB, increasing to 3.3 dB at the upper corner frequency while maintaining an input return loss below -10 dB. After steps were taken to improve the linearity, the IIP3 of the LNA is -14.5 dBm with only a small degradation in NF now 2.15 dB at the minimum. The power consumption of the respective LNAs are 12.75 mW and 23.25 mW and each LNA occupies a chip area of only 0.43 mm^2.

Measured results of the LNA fabricated in the IBM 7WL process had a gain of 10 dB compared to an expected simulated gain of 20 dB, however significant path loss was introduced by the IC package and PCB parasitics. The S_{11} tracked the simulated response very well and remained below -10 dB over the feasible frequency range. Reliable noise figure measurements could not be obtained. The measured P_{1dB} compression point is -22 dBm.

A 60 GHz LNA was also designed using this topology in a SiGe process with f_T of 200 GHz. A simulated NF of 5.2 dB was achieved for a gain of 14.2 dB and an input return loss below -15 dB using three amplifier stages. The IIP3 of the LNA is -8.4 dBm and the power consumption 25.5 mW. Although these are acceptable results in the mm-wave range it was however found that the wideband nature of this configuration is redundant in the unlicensed 60 GHz band and results are often inconsistent with the design theory due to second order effects.

The wideband results however prove that the LC-ladder and capacitive shunt-shunt feedback topology is a viable means for especially implementing LNAs that require a very wide operating frequency range and also very low NF over that range.

OPSOMMING

LC-LEER EN KAPASITIEWE SJUNT-SJUNT-TERUGVOER LRV-MODELLERING VIR WYEBAND-HBT-ONTVANGERS

deur

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Sleutelwoorde: Laeruis-versterker, wyeband, LC-leerfilters, kapasitiewe terugvoer, ruisbronne, impedansieaanpassing, wiskundige model, ruisoptimering, verrigtings-kompromieë, mm-golf, SiGe Heterovoegvlak- Bipolêre Transistor (HBT).

Alhoewel die meeste draadlose ontvangersubstelsels oor die laaste dekade na syfer-seinprosessering verskuif het, bly die laeruis-versterker (LRV) steeds ’n noodsaaklike analoogsubstelsel in enige ontwerp, aangesien dit die substelsel is met die grootste impak op die ruissyfer van die ontvanger as geheel.

In hierdie navorsing word ’n nuwe LRV-topologie, naamlik die LC-leer en kapasitiewe sjunt-sjunt-terugvoertopologie, voorgestel vir gebruik in uiters wyeband-LRVs. Dit is gedoen na ’n deeglike teoretiese ondersoek van huidige LRVs in die literatuur. Hieruit het dit duidelik geword dat smalband-LRV-topologië oor die algemeen vir wyeband-toepassings gebruik word, wat lei tot suboptimale resultate, en ook dat die wyeband-topologië wat wel bestaan, bepaalde tekortkominge het.

’n Wiskundige model is afgelei om hierdie nuwe topologie te beskryf en bestaan uit vergelykings vir die inset-impedansie, die inset-weerkaatsingsverlies, die spanningswins en die ruissyfer, asook ’n benadering vir die ergste IIP3-geval. Kompakte ontwerpvergelykings is ook van die model afgelei en ’n ontwerpstrategie geskik vir

elektroniese ontwerpsoutomatisasie van LRVs met hierdie topologie is voorgestel. ‘n Proses vir die optimering van die versterker om die ruissyfer te minimeer is afgelei van die model en verskillende metodes om die lineariteit van die LRV te verbeter, is bespreek. Die voorgestelde ontwerpproses is deurgaans suksesvol toegepas tydens hierdie navorsing.

Die akkuraatheid van die wiskundige model is bevestig deur simulasies. Twee weergawes van die LRV is vervaardig en die gemete resultate vergelyk goed met die simulasies. Die goeie korrellasie tussen die berekende, simulasie- en gemete resultate bewys die akkuraatheid van die model. Opmerkings oor moontlike verbeterings aan die model om die akkuraatheid selfs verder te verbeter, is ook gemaak.

Die simulasieresultate van ’n LRV wat ontwerp is vir die 1 GHz- tot 18 GHz-band in die IBM 8HP-proses wys ’n wins van 21.4 dB en ’n minimum ruissyfer van slegs 1.7 dB, wat vermeerder tot 3.3 dB by die boonste afsny-frekwensie, terwyl die inset-weerkaatsingsverlies onder -10 dB bly. Nadat stappe gedoen is om die lineariteit te verbeter, is die IIP3 van die LRV -14.5 dBm met slegs ’n klein verswakking in ruis, waar die minimumruissyfer nou 2.15 dB is. Die LRVs se drywingsverbruik is onderskeidelik 12.75 mW en 23.25 mW en elke LRV beslaan ’n oppervlak van slegs 0.43 mm^2.

Gemete resultate van die LRV wat in the IBM 7WL-proses vervaardig is, toon ’n wins van 10 dB teenoor ’n verwagte gesimuleerde wins van 20 dB. Merkwaardige verliese is egter teenwoordig as gevolg van die geïntegreerde stroombaanpakkie en die toets-etsbord. Die gemete S_{11} volg die simulasies egter besonder goed en bly onder -10 dB oor die totale moontlike frekwensiebereik soos gevind in die simulasies. ’n Betroubare ruissyfermeting kon nie geneem word nie. Die gemete P_{1dB}-winssaamperspunt is -22 dBm.

Verder is ’n 60 GHz LRV ontwerp met hierdie topologie in ’n SiGe-proses met ’n f_T van 200 GHz. ’n Gesimuleerde ruissyfer van 5.2 dB is behaal met ’n wins van 14.2 dB en insetweerkaastingsverlies laer as -15 dB deur drie versterkerstadiums te gebruik. Die IIP3 van die LRV is -8.4 dBm met ’n drywingsverbruik van 25.5 mW. Alhoewel die resultate aanvaarbaar is in die mm-golflengteband, is so ’n wyeband-implementasie oorbodig in die ongelisensieerde 60 GHz-band en is gevind dat die resultate ook dikwels nie ooreenstem met die ontwerpsteorie nie as gevolg van tweede-orde-effekte.

Die wyeband-resultate bewys egter dat die LC-leer en kapasitiewe sjunt-sjunt-terugvoertopologie goeie potensiaal inhou vir LRV implementasies, wat veral ’n uiters wye bandwydte nodig het, asook ’n baie lae ruissyfer oor daardie band.

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LIST OF ABBREVIATIONS

ADE	Analog Design Environment
ARJ	Africa Research Journal
BEOL	Back end of line
BGA	Ball grid array
BiCMOS	Bipolar and CMOS
BJT	Bipolar junction transistor
CMOS	Complementary metal oxide semiconductor
CSIR	Council for scientific and industrial research
DC	Direct current
DPSS	Defence, peace, safety and security
DUT	Device under test
EDA	Electronic design automation
ENR	Excess noise ratio
ESR	Equivalent series resistance
FET	Field effect transistor
FOM	Figure of merit
GaAs	Gallium arsenide
GBP	Gain-bandwidth product
HA	Hyper abrupt
HBT	Heterojunction bipolar transistor
HICUM	High current model
HIT-kit	High performance interface tool kit
IC	Integrated circuit
IF	Impact factor
IIP3	Third order input intermodulation product
InP	Indium phosphate
I/O	Input / output
IMN	Input matching network
ISI	Institute for Scientific Information
LNA	Low noise amplifier
LVS	Layout versus schematic
MDS	Minimum detectable signal

MIM	Metal-insulator-metal
MOS	Metal-oxide-semiconductor
MOSIS	MOS implementation service
MEP	MOSIS educational program
MPW	Multi-project wafer
NDA	Non-disclosure agreement
NF	Noise figure
PA	Power amplifier
PCB	Printed circuit board
PDK	Process design kit
PSD	Power spectral density
QFN	Quad flat no-lead (package)
RF	Radio frequency
SHF	Super high frequency
SiGe	Silicon-germanium
SPICE	Simulation program with integrated circuit emphasis
UWB	Ultra-wideband
VBIC	Vertical bipolar inter-company model