Chapter 5

Experimental Techniques

5.1 Introduction

The experimental techniques that are used for sample preparation, metallization, particle irradiation and defect characterization are described in this chapter. The sample preparation, (i.e. cleaning processes, Schottky and ohmic contacts fabrication) is presented in section 5.2. Section 5.3 deals with the irradiation of samples by high energy electrons or low energy noble gas ions. The Schottky contacts and the defects characterization tools, i.e. current-voltage (*I*-*V*), capacitance-voltage (*C*-*V*) current-temperature (*I*-*T*), capacitance-temperature (*C*-*T*), deep level transient spectroscopy (DLTS) and Laplace-DLTS (LDLTS) are outlined in section 5.4. The annealing studies set-up, which enables defect annealing analysis is presented in section 5.5.

5.2 Sample Preparations

Before metallization, samples were cut into 1 cm x 0.3 cm for silicon and 0.5 cm x 0.3 cm for germanium followed by a chemical cleaning process. It is important to note that immediately after the cleaning process, metallization should follow to reduce oxide layer build-up and recontamination of the sample.

5.2.1 Silicon Cleaning Process

The cleaning steps are used sequentially, as follows;

(1) Degreasing; removing of dust particles, or grease in boiling trichloroethylene (TCE) and then boiling isopropanol for 3 minutes, followed by rinsing in de-ionized water.

(2) Organic cleaning; removal of insoluble organic contaminants and metals using a H_2O : 30% H_2O_2 : 25% NH_4OH (5:1:1) solution at (75 – 80ºC) for 10 minutes followed by rinsing in de-ionized water.

(3) Oxide stripping; removal of the self-passivating oxide film is done in two steps. (a) etching in 40% HF : 70% HNO_3 : 96% glacial CH_3COOH (2:15:5) solution for 3 s and the outstanding oxide layer is stripped by (b) dipping in dilute 40% HF : H_2O (1:10) solution for 5 s followed by a rinse in de-ionized water. This, however, still leaves some amount of silicon oxide on the surface in addition to other species such as hydrogen, fluorine and hydroxyl groups [1].

(4) The samples are blow-dried in stream of N_2 gas and ready for the metallization step.

5.2.2 Germanium Cleaning Process

The germanium cleaning steps are in sequence, as follows;

(1) Degreasing in trichloroethylene (TCE), acetone and then methanol, each for 5 minutes in an ultrasonic bath at room temperature. This degreasing step is followed by rinsing in de-ionized water.

(2) Organic cleaning; removal of insoluble organic contaminants and metals in a solution of 30% H_2O_2 : H_2O (1:5) for 1 minute and then rinsing in de-ionized water.

(3) The samples are blow-dried in stream of N_2 gas and ready for the metallization step.

5.2.3 Ohmic and Schottky Contact Fabrication

Immediately after the chemical cleaning procedure, ohmic and Schottky contacts were fabricated. To form ohmic contacts on Ge, a 100 nm thick layer of Au-Sb (6% Sb) was deposited on the back surface of the sample by resistive deposition after evacuating the chamber to pressure levels of approximately 10^{-6} Torr. The ohmic contact was thereafter annealed at 350ºC for 10 minutes in Ar gas. This subsequent annealing step helps to optimize the ohmic contact by lowering the barrier height, hence reducing its resistivity [2]. The annealing temperature is chosen such that it optimize the ohmic contact [3]. The use of a reducing atmosphere avoids any further oxidation of the metal during annealing, while it can also reduce any interfacial oxide between the metal and semiconductor.

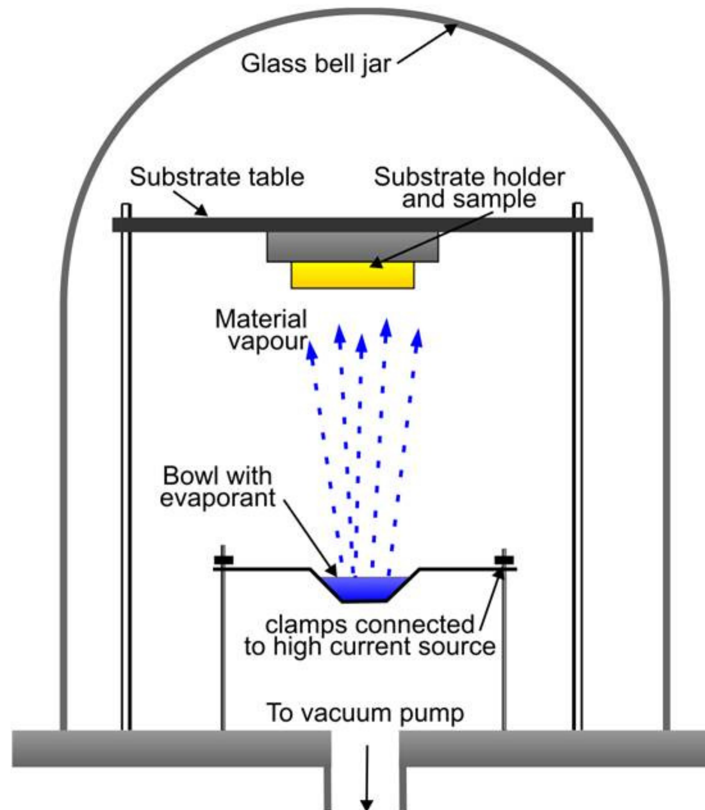

Fig. 5-1. The resistive deposition system.

The resistive deposition system is depicted in Fig. 5-1. In this technique, a current flows through the crucible containing the metal to be deposited until it reaches the melting point of the metal. The metal evaporates and deposits onto the sample above the crucible. The deposition rate is controlled by adjusting the current until the required evaporation rate has been achieved. The resistive deposition method is used for metals with low melting point (<1600°C) e.g. Al, Au, Pd or Ni and the technique cannot be used to deposit higher melting point metals.

The Schottky contacts, 100 nm thick layer, were fabricated on both Si and Ge by evaporating the metals e.g. palladium (Pd) or gold (Au) on the polished side, through masks with circular holes 0.60 mm in diameter. The contacts were fabricated using resistive deposition or electron beam deposition. A typical electron beam system (EBD) is shown in Fig. 5-2. In this technique, a hot filament emits electrons which are then accelerated and focused onto the target (crucible containing the metal) by electric and magnetic fields. This results in the melting and evaporation of the metal which deposites onto the sample.

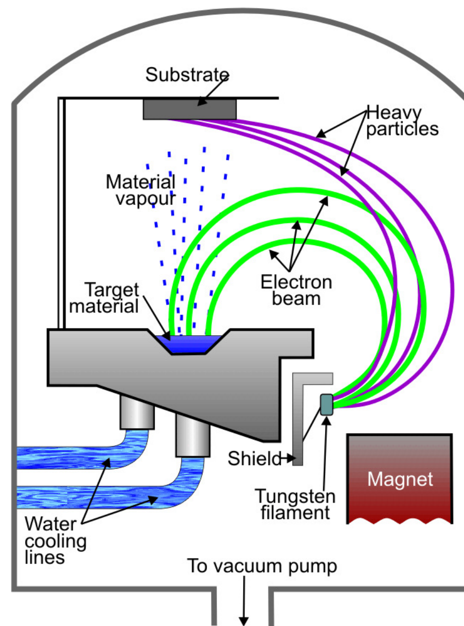

Fig. 5-2. The electron beam deposition (EBD) system.

The deposition rate is controlled by controlling the filament current. The EBD method can deposit any metal but its disadvantage is that it may introduce defects on and below the surface of the sample on which contacts are fabricated. After the sample metalization, as shown by an illustration in Fig. 5-3, the sample is ready for further processing, i.e. bombardment by energetic particles, and electrical characterization of the resulting defect levels.

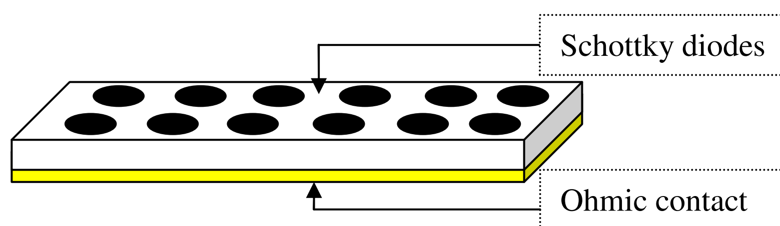

Fig. 5-3. A typical sample showing circular Schottky diodes on the top surface and ohmic layer on the back surface (the thickness of the ohmic layer has been enlarged for clarity).

5.3 Sample Irradiation

After metallization process, lattice defects were introduced by bombarding the samples from the Schottky side with high energy (MeV range) electrons, or noble gas ions (keV range) of well controlled fluencies as shown in Fig. 5-4.

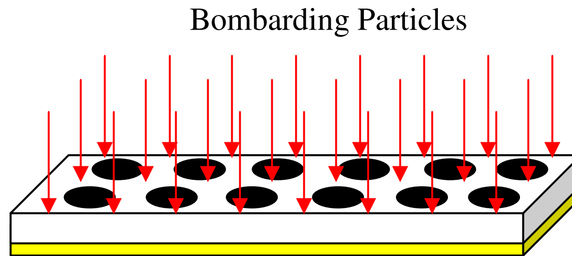

Fig. 5-4. Schematic diagram of a typical sample under irradiating particles.

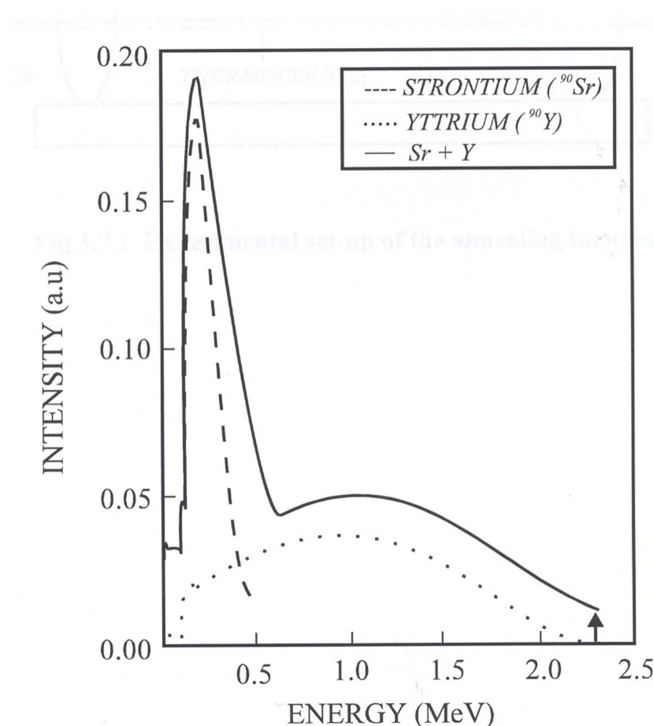

Fig. 5-5. Energy distribution of electrons emitted by a ^{90}Sr radionuclide. For clarity the sum of the Sr and Y contributions has been displaced by an amount indicated by the arrow, (redrawn from ref. 4).

Depending on the incident particle type, size and energy, some particles can go right through the sample and others may lose all their energy due to collision and eventually stop within the sample. All the irradiation processes were performed at room temperature.

5.3.1 Electron Irradiation

The electron irradiation of the samples was carried out using (1) a particle accelerator at Ohio State University in USA, for Si samples and (2) a strontium-90 (^{90}Sr) radionuclide source for Ge samples. The strontium source used is disc-shaped, with a diameter of 8.4 mm and an activity of 20 mCi. The ^{90}Sr radionuclide (half-life of 28.5 years) decays first to yttrium (Y) (half-life of 64.1 hours), with the emission of a 0.5 MeV electron. The Y in turn decays by the emission of a 2.27 MeV electron to zirconium (Zr). The electrons emitted from this radioactivity of ^{90}Sr have a continuous energy distribution as shown in Fig. 5-5. It is clear from this figure that, approximately 70% of the total number of emitted electrons, have energies above 250 keV, i.e. the threshold for producing defects by elastic collisions [4]. During the irradiation the samples were placed 1 mm below the center of the radioactive disc so that one can assume that the flux reaching the sample at this position is that which leaves the surface of the source. The total fluence rate of electrons emitted is calculated from the activity of the ^{90}Sr source. Each ^{90}Sr decay results in the emission of two electrons because the half-life of Y is much shorter than that of Sr. This total dose is equal to the area below the curve (Sr + Y) in Fig. 5-5. It is assumed that temperature of the sample remains constant during the irradiation process.

5.3.2 Low Energy Noble Gas Irradiation

The low energy (keV) noble gas ions irradiations were performed in the Auger electron spectroscopy system (AES). A collimated beam of Ar ions of energy 3 keV and fluencies in the range 10^{13} – 10^{14} ions/cm^2 was used for the sputtering process. The beam was incident on the sample at an angle of about 35° to the normal.

5.4 Electrical Characterization

After metallization, current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) measurements were used to monitor the quality and electrical properties of the diodes while deep level transient spectroscopy (DLTS) [5] and Laplace-DLTS (LDLTS) [6,7] were used to characterize defects in the semiconductor band gap before and after particle irradiation.

5.4.1 Current-Voltage and Capacitance-Voltage Measurement System

The diode properties which were extracted from (*I*-*V*) and (*C*-*V)* measurements are; series resistance R_s, free carrier density profiles N_D, barrier height ϕ_B, ideality factor *n*, and leakage currents I_r (measured at reverse bias of -1 V). These diode properties determine whether a diode is usable for DLTS measurements. A good diode for DLTS application is one that gives high signal-noise ratio, and these are diodes with high barrier height, low leakage current (<10^{-4} A) and low series resistance (<200 Ω). The diode electrical properties were monitored after each DLTS scan (since it is well known that diodes tend to degrade after several up-down temperature scans in DLTS system) and to monitor the carrier reduction after irradiation, or diode processing. The schematic diagram for the measurements is illustrated in Fig. 5-6 [8].

The (*I*-*V*) characteristics were measured using an HP 4140B pA meter/ DC voltage source with a lower current limit of 10^{-14} A and (*C*-*V*) measurements were done by an HP 4192A LF Impedance Analyzer. Samples were mounted in a metal box enclosure to eliminate light and electrical noise.

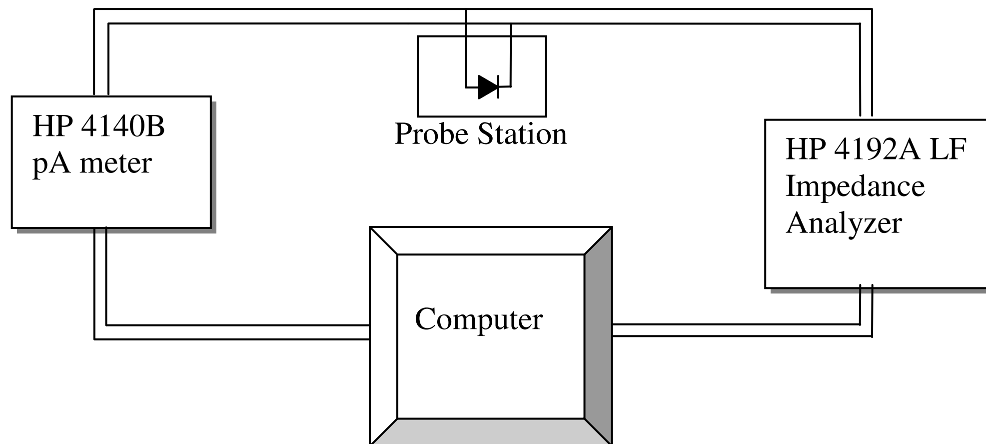

Fig. 5-6. Block diagram of (I-V) and (C-V) measurements station.

5.4.2 Deep Level Transient Spectroscopy (DLTS) and Laplace-DLTS Systems

The DLTS and L-DLTS system used for this study consists of the following units,

(a) A cryostat in which the sample is mounted. The temperature is controlled by a Lake Shore 340 temperature controller in the range (16 K – 380 K).

(b) A fast (1 MHz range) Boonton 7200 capacitance meter with 100 mV, 1 MHz ac voltage, which monitors thermal emission after excitation by a pulse generator.

(c) A Laplace card and software [7]. This card has an internal pulse generator for generating the desired quiescent bias voltage and pulses, and it is also the data collection and processing system which analyses and averages transients before displaying the spectra for both the conventional DLTS and LDLTS.

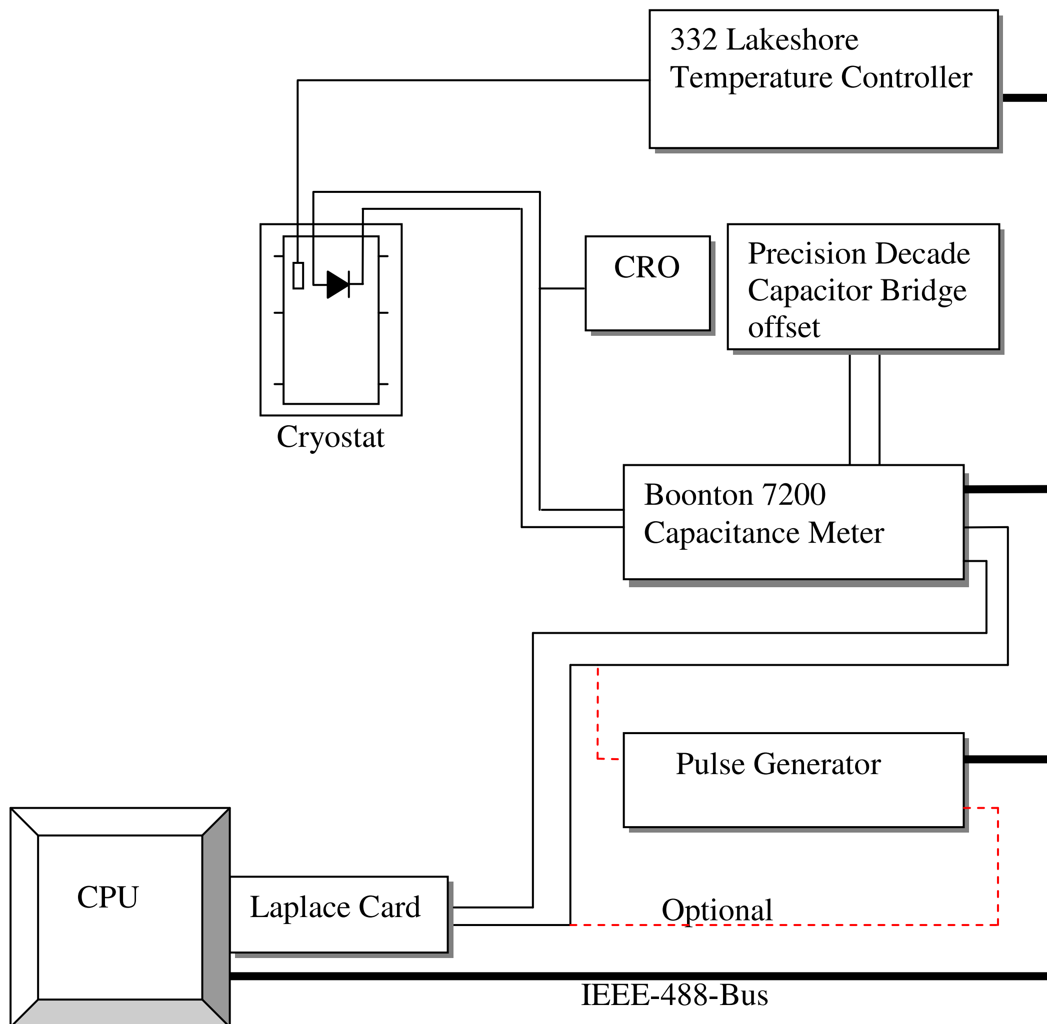

Fig. 5-7. The Schematic of the DLTS and LDLTS system used in this study.

(d) An external pulse generator (hp 33120A 15 MHz Function waveform generator), to provide the desired quiescent bias voltages and filling pulse to the diode which are not provided by the Laplace card.

The Schematic diagram of the DLTS and LDLTS used in this study is depicted in Fig. 5-7. The Laplace program sets the sample excitation parameters, the capacitance transient acquisition conditions, initiates the measurement, acquires the transient and

finally converts it into a conventional-DLTS or Laplace spectrum. In case of conventional DLTS the capacitance meter measures the capacitance transients after excitation. The transients are then processed by the Laplace card and as the temperature is ramped a DLTS spectrum is displayed on a computer for a particular '*rate window*' which can be set in the range 1 s^{-1} – 5000 s^{-1}. Similarly for the LDLTS the capacitance meter monitors the capacitance transients after excitation and the Laplace card then averages the transient and implements the inverse Laplace transforms to calculate the emission rates and magnitude of the signal using three different software routines CONTIN, FTIKREG and FLOG [7] before the computer displays the Laplace spectrum. The internal pulse generator (provided by the Laplace card) has been used when very good diodes were measured and the external pulse generator was connected in case of poor diodes since it has been established that very high signal: noise ratio (SNR) >1000:1, which is necessary to separate levels with close emission rates, could only be achieved with an external pulse generator but not with the internal pulse generator. When the external pulse generator is used a pulse from the Laplace card is used to trigger the pulse generator.

The Laplace card has also been used for the current-temperature (*I*-*T*) and capacitance-temperature (*C*-*T*) measurements by connecting the HP 4140B pA current meter and HP 4192A LF Impedance analyzer respectively and the measurements were automated by Labview routine.

5.5 Annealing Apparatus

The annealing studies were performed in a Lindberg "Hevi-duty" furnace with a maximum temperature of 1200ºC. The inert atmosphere was achieved by connecting the furnace to a supply of inert gas such as argon or nitrogen. The temperature was monitored using a thermo-couple with a digital display which was placed just under the sample holder.

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Chapter 6: Results

Radiation-induced defects in Ga-or B-doped silicon by 1 MeV electron irradiation

6.1 Introduction

Silicon (Si) integrated circuits are still currently dominating the technological advancement of semiconductor devices because of the several advantages of silicon over other semiconductors (such as, stable oxide, cheapest in its field of application, and better understood etc). The understanding of lattice defects in semiconductors is an important step in the device fabrication since defects can be detrimental to some devices (e.g. solar cells were they can act as minority carrier 'killers' thereby reducing the efficiency of the solar cells [1]) or beneficial to some (e.g. when they act as recombination centers in fast switching devices, hence enhancing the switching speeds [2]). Defects can be introduced into a semiconductor in a number of ways, (a) growth of semiconductor, (b) processing of device (e.g. plasma etching) or high-energy particle - irradiation and (c) under operating conditions. A notable example in the latter case is the degradation of B-doped Cz –Si solar cells under either illumination or carrier injection due to formation of a metastable defect involving B and O [2]. The lifetime degradation is not observed in Ga-doped Cz Si [2]. Silicon is a very useful material in the photovoltaic industry because of its relative high carrier lifetime ~1 ms, (hence larger diffusion lengths of ~1 mm) when compared to most semiconductors. Apart from germanium, silicon has a relatively low effective mass for holes and therefore p-type silicon is attractive for producing high frequency devices and solar cells.

Very little work has been done on Ga-related defects on p-type silicon [3-4]. The defects characterized by DLTS [5] and high-resolution Laplace-DLTS (LDLTS) [6-7] are presented in this chapter and the resolution of LDLTS is demonstrated.

6.2 Experimental Procedure

Boron and gallium-doped silicon with a carrier density of 1.5 x 10^{16} cm^{-3} and 3.5 x 10^{16} cm^{-3} respectively have been used. The samples were prepared for metal deposition by chemical cleaning (i.e. degreasing then dipping in dilute 10% HF solution). After blow-drying in N_2 gas, the samples were immediately loaded into the vacuum chamber, which was evacuated to a pressure of below 1 x 10^{-6} mbar to reduce oxidation before processing. Through a circular mask, of diameter 0.48 mm, Ti and then Al, 100 nm thick each, were deposited using electron beam deposition (EBD). After diode fabrication, the samples were then irradiated (at room temperature) with 1 MeV electrons to fluences of 1.5 x 10^{16} cm^{-2} (B-doped) and 3.5 x 10^{16} cm^{-2} (Ga-doped), respectively. Before the irradiation process the samples were annealed at 550°C to remove all the EBD induced defects. Prior to electrical characterization, {i.e. current-voltage (*I-V*), capacitance-voltage (*C-V*), DLTS and Laplace (LDLTS)} ohmic contacts were formed on the rear side of the sample using In-Ga eutectic. The defect 'signatures' {i.e activation enthalpy E_T (in eV), and apparent capture cross-section, σ_a (in cm^2)} were determined from Arrhenius plots of $ln(T^2/e_h)$ vs. $1000/T$, where e_h is the hole emission rate and T is the measurement temperature.

To study defect annealing characteristics of primary and secondary radiation induced defects isochronal annealing was performed on the Schottky contacts in the temperature range 30°C - 350°C in steps of 50°C for 20 minutes in Ar gas. Each annealing cycle was followed by electrical characterization of the defects.

6.3 Results

In this section the electronic and annealing properties of hole traps created in the samples by electron irradiation or proton irradiation are discussed. First, it is enlightening to look at the defect resolution capability of Laplace-DLTS over conventional DLTS.

6.3.1 Conventional DLTS versus Laplace-DLTS

The DLTS spectrum recorded from the Ga doped Cz Si sample after the electron irradiation is shown in Fig. 6-1. The spectra exhibit two dominant peaks positioned at around 115 K and 190 K with a shoulder peak at high temperature side of low temperature peak. On the other hand, the insets show the spectral density functions (SDF), i.e. LDLTS spectra (measured around the peak positions of the two broad peaks). LDLTS is clearly able to resolve the broad DLTS peaks into two groups of discrete levels as depicted in inset (a) and inset (b). Notably, the broad peak around 115 K is resolved into three discrete defects with levels at E_V + 0.18 eV, E_V + 0.19 eV, and E_V + 0.23 eV while the peak around 190 K is resolved into two discrete defects with levels at E_V + 0.33 eV and E_V + 0.34 eV. The levels E_V + 0.19 eV and E_V + 0.34 eV are the dominant peaks as evidenced by the height of the LDLTS signal.

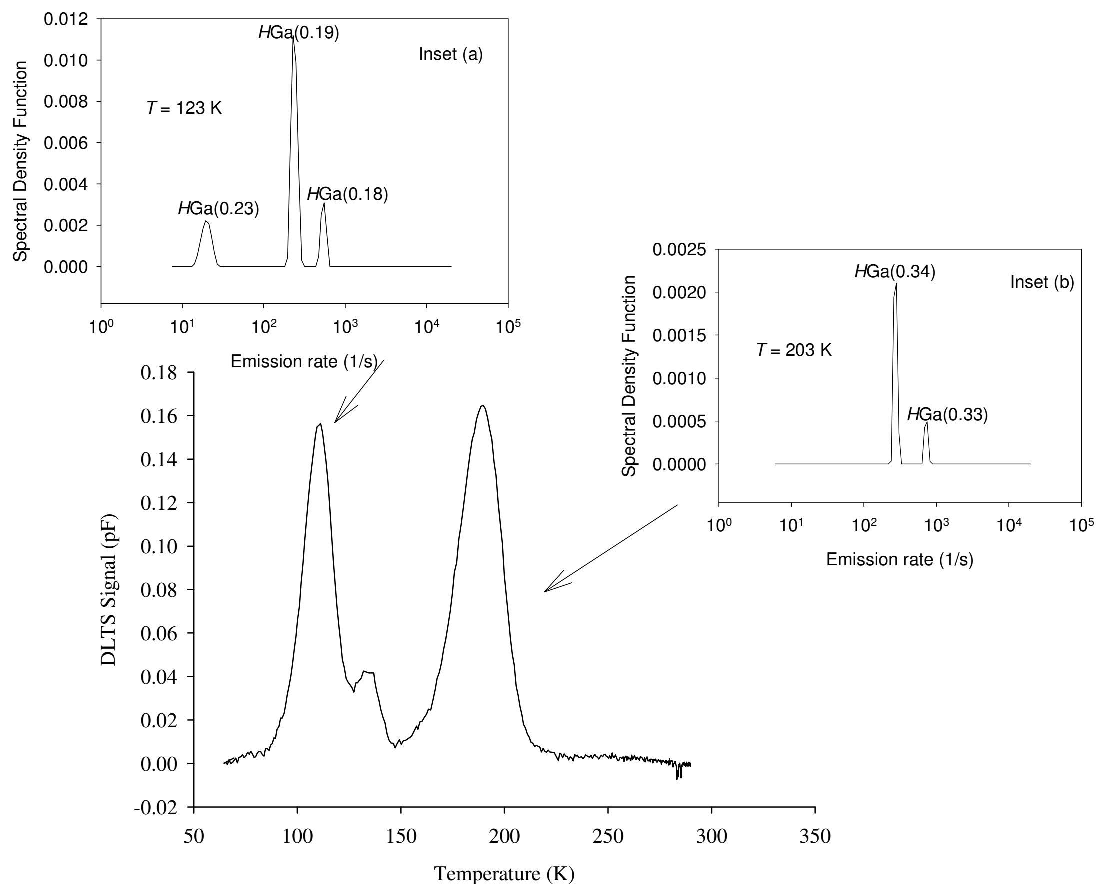

Fig. 6-1. Conventional DLTS spectra of electron irradiated Ga-doped Cz Si. Inset: The LDLTS spectra for each broad DLTS peak. The spectra were recorded at a reverse bias V_r = -2V, pulse voltage V_p = 0.5 V, pulse width of 1 ms and rate window (RW) of 80 s^{-1}.

6.3.2 Electron irradiation-induced defects in Ga –doped Czochralski grown Si

The DLTS spectra of primary and secondary defects introduced after electron irradiation of Ga-doped Czochralski (Cz) Si are shown in Fig. 6-2. The samples were defect free before the irradiation. The defects signatures (extracted from the Arrhenius plots, Fig. 6-4) and their annealing properties are summarized in Table 6.1 and Fig. 6-3. The defect levels, *H*Ga(0.18), *H*Ga(0.19), *H*Ga(0.23), *H*Ga(0.33) and *H*Ga(0.34) were observed after the irradiation as shown by DLTS spectra in Fig. 6-2 (a). In this nomenclature '*H*' is the hole trap, 'Ga' is the dopant and '0.19' is the activation enthalpy, i.e. (E_V + 0.19) eV. The origin of both *H*Ga(0.18) and *H*Ga(0.33) is not clear at the moment, but *H*Ga(0.34) has been assigned to the C_I-O_I complex [3,8,9].

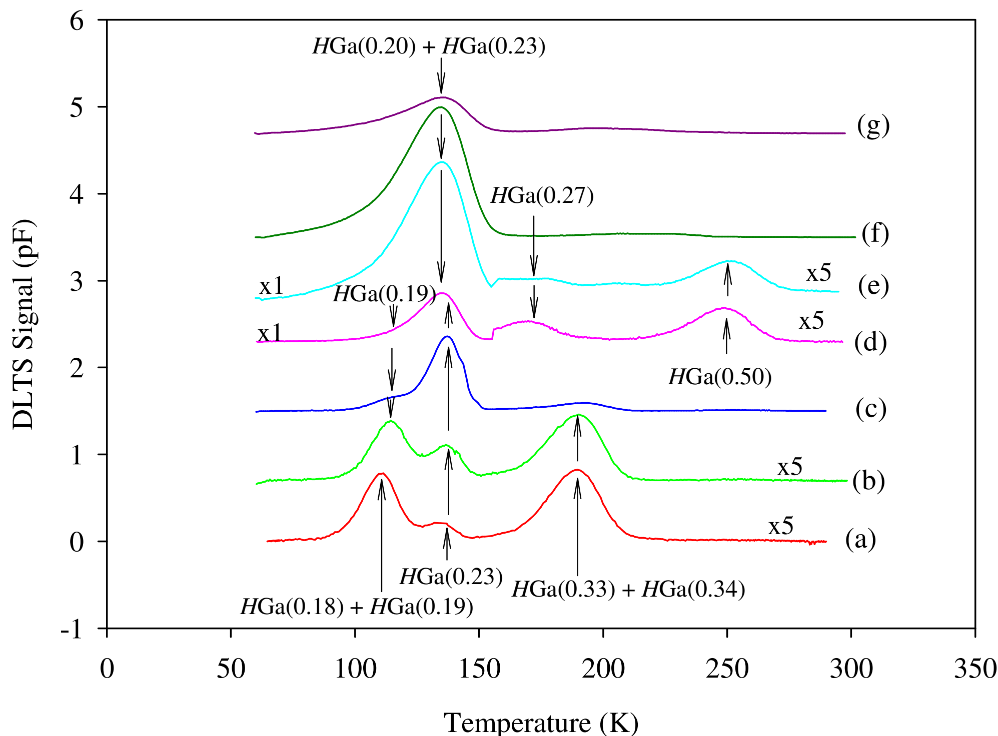

Fig. 6-2. DLTS spectra showing defects introduced in 1 MeV electron irradiated Ga –doped Cz Si for as (a) as-irradiated and after annealing for 20 minutes at (b) 100˚C, (c) 150˚C, (d) 175˚C, (e) 200˚C, (f) 300˚C and (g) 350˚C. These measurements were recorded at a quiescent reverse bias V_r = -2V, a filling pulse V_p = +0.5 V, pulse width of 1 ms and a rate window of 80 s^{-1}.

There has been some inconsistency in the literature about the identity of the divacancy in p-type Si, but *H*Ga(0.19) is identified as the (+/0) charge state of the divacancy

[3,10] because of its annealing behavior. *H*Ga(0.23) is suggested to be H related defect with the source of hydrogen being the wet etching processing step and it shows strong reverse annealing (i.e. increase in defect concentration with annealing temperature) around 150˚C, an indication that H could be coming from some passivated defect levels [11].

The introduction rates deduced from depth profile measurements for the dominant traps *H*Ga(0.34) and *H*Ga(0.19) are 2.5 x 10^{-2} cm^{-1} and 4.0 x 10^{-3} cm^{-1} respectively which is consistent with the results in the literature [12].

Table 6.1. Electronic properties of defects introduced in Ga-doped Cz Si.

Defect	E_T (eV)	σ_a (cm^2)	T_{peak} [a] (K)	T_{in} [b] (˚C)	T_{out} [c] (˚C)	Defect identity
After	*Irradiation*					
*H*Ga(0.18)	$E_V + 0.18$	1.4 x 10^{-15}	115	RT	100	? ref. 4
*H*Ga(0.19)	$E_V + 0.19$	5.1 x 10^{-16}	115	RT	225	$V_2^{+/0}$ [3,4,10,11, 12]
*H*Ga(0.23)	$E_V + 0.23$	2.6 x 10^{-16}	137	RT	---	H-related? [11]
*H*Ga(0.33)	$E_V + 0.33$	1.6 x 10^{-15}	190	RT	100	?
*H*Ga(0.34)	$E_V + 0.34$	8.0 x 10^{-16}	190	RT	175	C_I-O_I [3,8,9,11,12]
After	*Annealing*					
*H*Ga(0.20)	$E_V + 0.20$	3.2 x 10^{-16}	160	175	----	?
*H*Ga(0.27)	$E_V + 0.27$	2.9 x 10^{-16}	160	175	300	Ga-related?
*H*Ga(0.50)	$E_V + 0.50$	5.2 x 10^{-15}	250	175	300	Ga or H-related?

[a]Peak temperature at a rate window of 80 s^{-1}, [b]Temperature at which the defect is introduced. [c]Temperature at which the defect is removed.

The C_I-O_I complex is thought to be a recombination center which is responsible for the minority-carrier lifetime reduction and carrier removal in Si, thus has a dominant role to control the efficiency of Si solar cells [3].

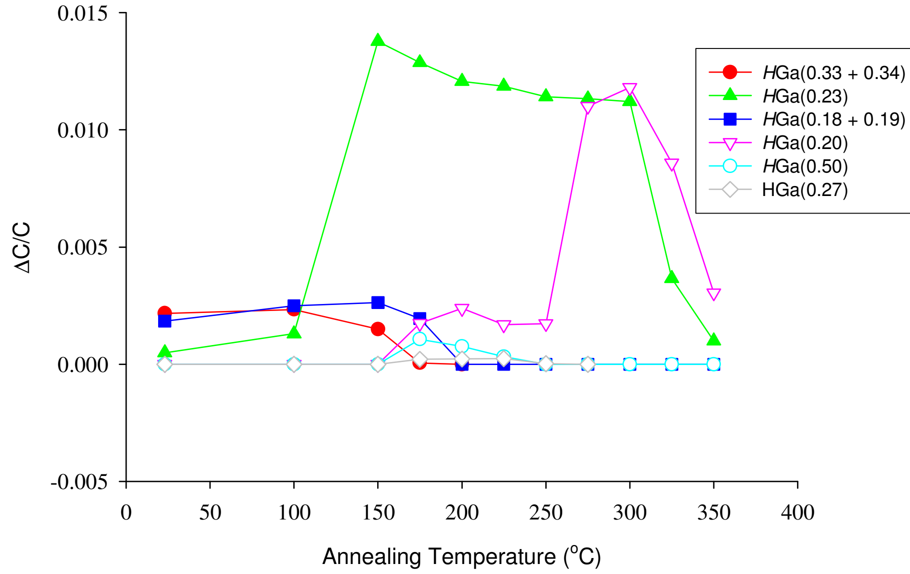

Fig. 6-3. Isochronal annealing behavior of defects in electron-irradiated B-doped epitaxial Si.

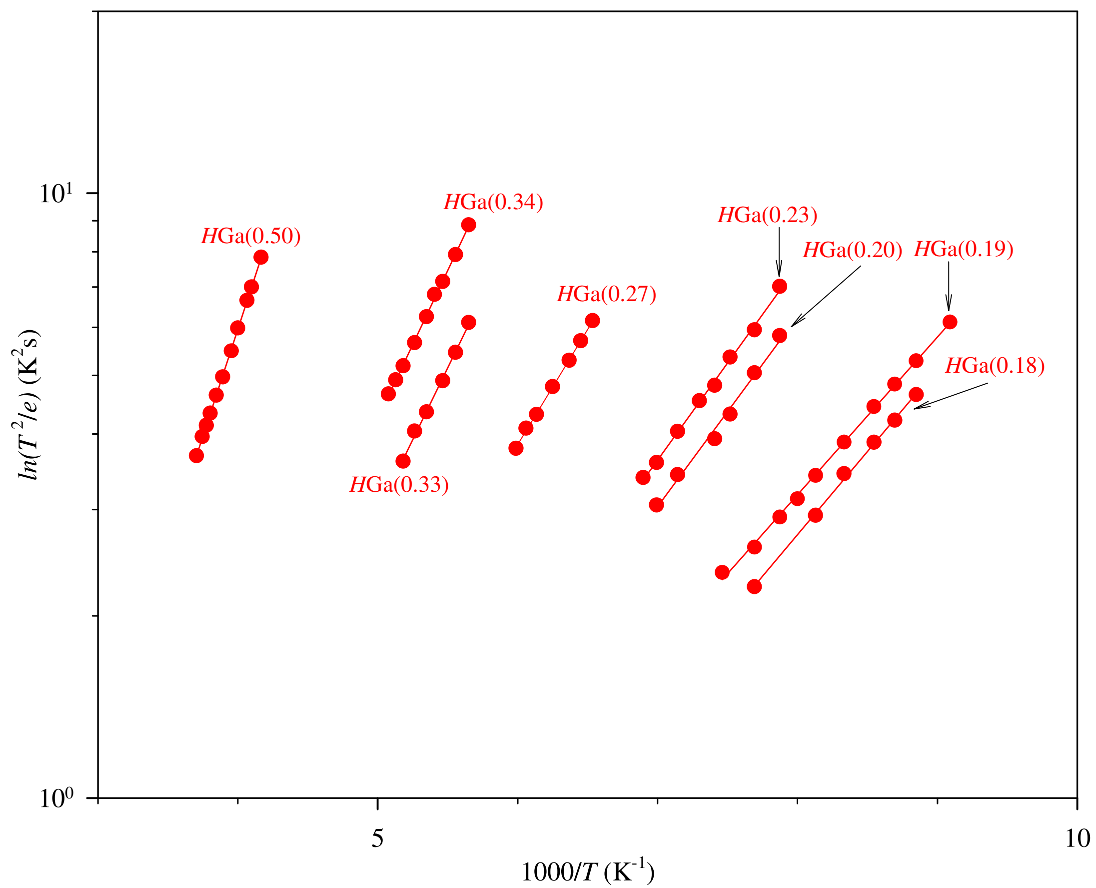

Fig. 6-4. Arrhenius plots of the defects introduced in Ga-doped Cz Si by 1 MeV electron irradiation.

From a practical perspective, the complete characterization of defects requires that the annealing kinetics of the defect is established. Annealing experiments serve to determine, amongst others, (i) the temperature range within which a defect can be removed after its initial introduction, (ii) whether secondary defects that may be detrimental to device performance are introduced during high-temperature steps in the processing of devices, and (iii) the structure of defects through comparative studies. Figures 6-2 and 6-3 show the annealing behavior of defects in electron-irradiated Ga doped Cz Si. The secondary hole traps *H*Ga(0.20), *H*Ga(0.27) and *H*Ga(0.50) are all introduced after annealing at 175˚C, Fig. 6-2 curve (d), and *H*Ga(0.27) and *H*Ga(0.50) anneal at 300˚C, curve (f), whereas the trap *H*Ga(0.20) is still present at the maximum annealing temperature of 350˚C used (note: the samples degraded beyond measurable conditions after annealing at >350˚C). The identity of these secondary defects is not clear at the moment.

Table 6.2. Electronic properties of defects introduced in B-doped epi-Si.

Defect	E_T (eV)	σ_a (cm^2)	T_{peak} [a] (K)	T_{in} [b] (˚C)	T_{out} [c] (˚C)	Defect identity
After	*Irradiation*					
*H*B(0.17)	$E_V + 0.17$	5.2×10^{-17}	115	RT	100	?
*H*B(0.18)	$E_V + 0.18$	1.3×10^{-16}	115	RT	225	$V_2^{+/0}$ [13,14.15]
*H*B(0.23)	$E_V + 0.23$	2.6×10^{-16}	137	RT	---	H-related? [11,15]
*H*B(0.34)	$E_V + 0.34$	1.6×10^{-15}	190	RT	100	?
*H*B(0.35)	$E_V + 0.35$	4.5×10^{-16}	190	RT	---	C_I-O_I [13,15]
*H*B(0.45)	$E_V + 0.45$	3.4×10^{-14}	240	RT	150	B-related?
After	*Annealing*					
*H*B(0.39)	$E_V + 0.39$	2.5×10^{-16}	230	150	300	B-related?

[a]Peak temperature at a rate window of 80 s^{-1}, [b]Temperature at which the defect is introduced. [c]Temperature at which the defect is removed.

6.3.3 Electron irradiation-induced defects in B-doped epitaxial grown Si

Primary hole traps *H*B(0.17), *H*B(0.18), *H*B(0.34), *H*B(0.35) and *H*B(0.45) were introduced by electron-irradiation in B-doped epitaxial Si, as depicted in Fig. 6-5 (a). The defect's electronic properties summarized in Table 6.2 were extracted from the Arrhenius plots shown in Fig. 6-7. Similar to the nomenclature used in the Ga doped sample, in this case '*H*' is the hole trap, 'B' is the dopant and '0.17' is the activation enthalpy, i.e. (E_V + 0.17) eV. The traps *H*B(0.17) and *H*B(0.18) have electronic structures (evidenced by the Arrhenius plots in Fig. 6-7) and annealing characteristics similar to *H*Ga(0.18) and *H*Ga(0.19) respectively, observed in the Ga-doped sample. *H*B(0.18) has been identified as the (+/0) of the divacancy [13,14], but the identity of *H*B(0.17) is not clear at the moment. The deduced introduction rates for the dominant levels *H*B(0.18) and *H*B(0.35) after 1 MeV electron irradiation were 5.0 x 10^{-3} cm^{-1} and 2.0 x 10^{-3} cm^{-1} respectively.

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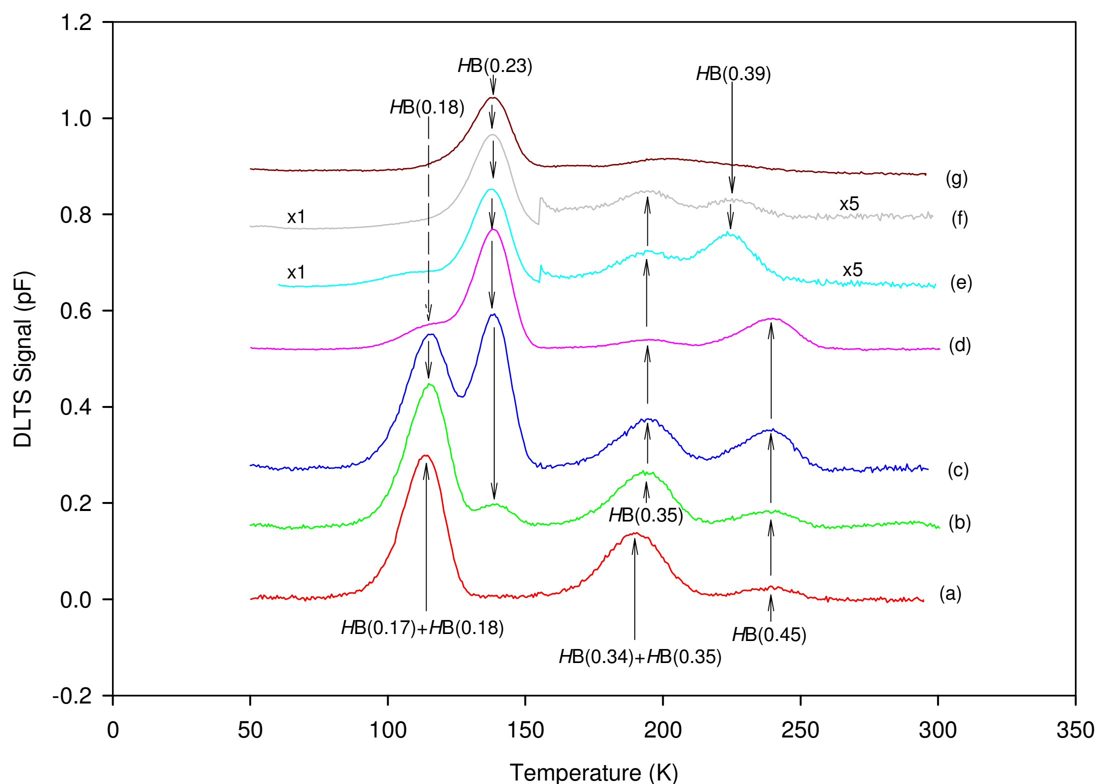

Fig. 6-5. DLTS spectra showing defects introduced in 1 MeV electron irradiated B – doped epitaxial Si for as (a) as-irradiated and after annealing for 20 minutes at (b) 100˚C, (c) 125˚C, (d) 150˚C, (e) 200˚C, (f) 250˚C and (g) 325˚C. The spectra were recorded at a rate window (RW) of 80 s^{-1}, a quiescent reverse bias of V_r = -2 V with a filling pulse V_p = 0.5 V and a pulse width of 1 ms.

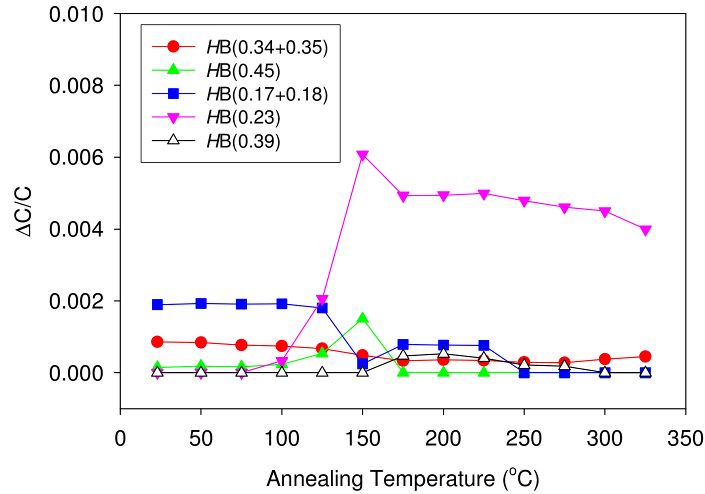

Fig. 6-6. Isochronal annealing behavior of defects in electron-irradiated B-doped epitaxial Si.

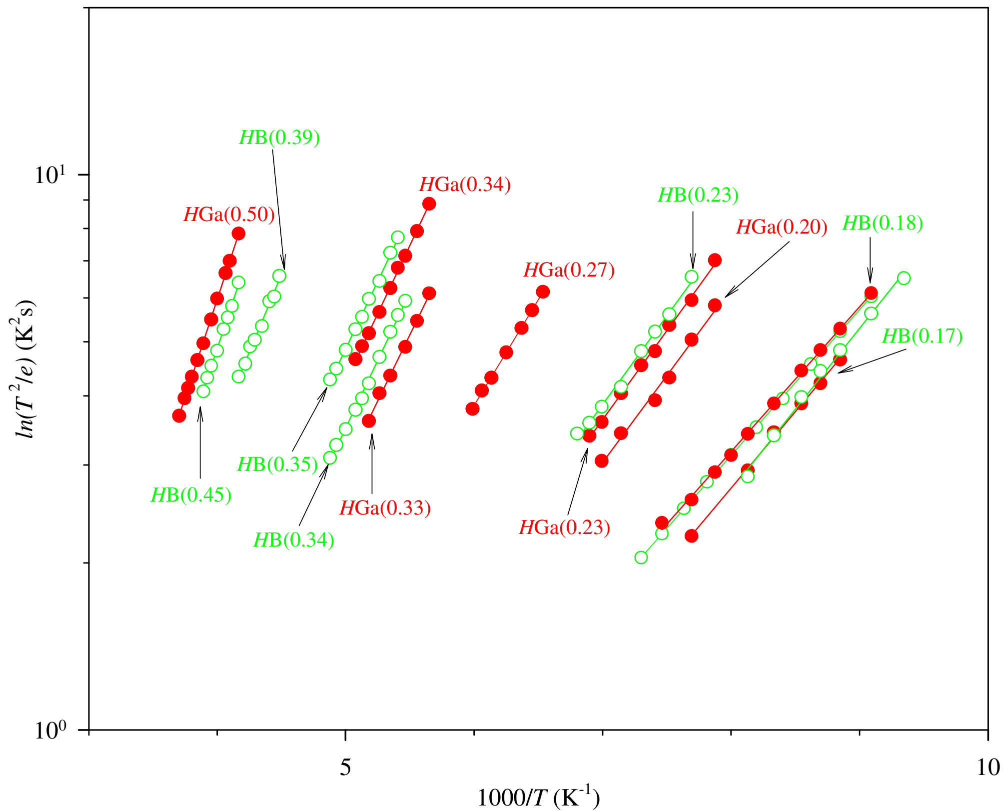

Fig. 6-7. Arrhenius plots of the primary and secondary defects introduced in B-doped epitaxial Si (green circles) compared to those introduced in Ga-doped Si (red circles) by 1 MeV electron irradiation.

*H*B(0.35) has been identified as the C_I-O_I complex [13,16] and the origin of *H*B(0.45) is speculated to be B related [13]. The annealing behavior of the defects introduced by

electron irradiation are depicted in Fig. 6-6 and Fig, 6-7. Similar to defects introduced in Ga-doped sample, *H*B(0.23) show reverse annealing characteristics in the temperature range between 100˚C and 150˚C as shown in Fig. 6-7 and this trap has been attributed to a H-related defect [11]. Upon annealing at 175˚C, *H*B(0.39) was introduced. Since this level is not observed in the Ga-doped sample, it is speculated that it might be B-related.

6.3.4 Electron irradiation-induced defects in B-doped Czochralski grown Si

In order to shed more light on the radiation induced defects in p-type silicon, defect characterization work has been extended to boron-doped Cz grown silicon. These samples have higher oxygen concentration when compared to epitaxial grown silicon.

Table. 6.3. Electronic properties of defects induced in B-doped Cz Si by 1 MeV electrons

Defect	E_T (eV)	σ_a (cm^2)	T_{peak}[a] (K)	T_{in}[b] (˚C)	T_{out}[c] (˚C)	Defect identity
After	*Irradiation*					
*H*B(0.17)	$E_V + 0.17$	1.3×10^{-17}	115	RT	100	?
*H*B(0.18)	$E_V + 0.18$	1.1×10^{-16}	115	RT	200	$V_2^{+/0}$ [4,10,11]
*H*B(0.23)	$E_V + 0.23$	2.0×10^{-16}	137	RT	---	H-related? [11]
*H*B(0.34)	$E_V + 0.34$	3.7×10^{-15}	190	RT	100	?
*H*B(0.35)	$E_V + 0.35$	2.5×10^{-16}	190	RT	175	C_I-O_I [4,13,17]
*H*B(0.45)	$E_V + 0.45$	3.2×10^{-14}	240	RT	150	B-related?
After	*Annealing*					
*H*B(0.22)	$E_V + 0.22$	2.1×10^{-15}	130	150	300	O-related?

[a]Peak temperature at a rate window of 80 s^{-1}, [b]Temperature at which the defect is introduced. [c]Temperature at which the defect is removed.

The electronic properties of defects introduced in B-doped Cz Si (extracted from the Arrhenius plots in Fig. 6-10) are summarized in Table 6-3. The primary hole traps observed after irradiation are *H*B(0.17), *H*B(0.18), *H*(0.23), *H*B(0.34), *H*B(0.35) and *H*B(0.45) they all have the same electronic structures to those introduced in epitaxial Si, as shown by Arrhenius plots in Fig. 6-10.

Upon annealing a new hole trap *H*B(0.22) is observed after annealing at 150˚C and this trap is not observed in the epitaxial sample, therefore it might be oxygen related. In Ga-doped a defect *H*Ga(0.20) has similar annealing characteristics. The trap level *H*B(0.23) is significantly suppressed after annealing at 150˚C and higher temperatures which is different from its annealing behavior as observed in the Ga-doped and epitaxial samples. The reason for this discrepancy is not clear at the moment.

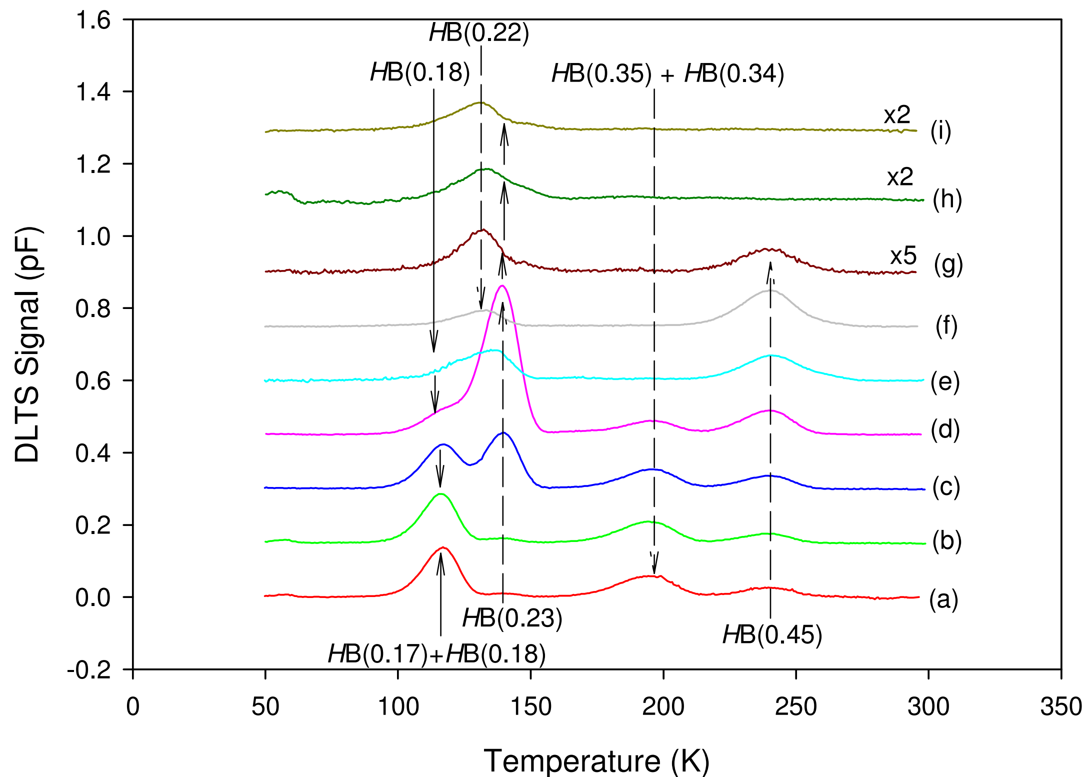

Fig. 6-8. Defects introduced in B-doped Cz Si after 1 MeV electron irradiation for (a) as-irradiated and after annealing at (b) 50˚C, (c) 100˚C, (d) 125˚C, (e) 150˚C (f) 175˚C, (g) 200˚C, (i) 275˚C . The spectra were recorded at a rate window (RW) of 80 s^{-1}, a quiescent reverse bias of V_r = -2 V with a filling pulse V_p = 0.5 V and a pulse width of 1 ms.

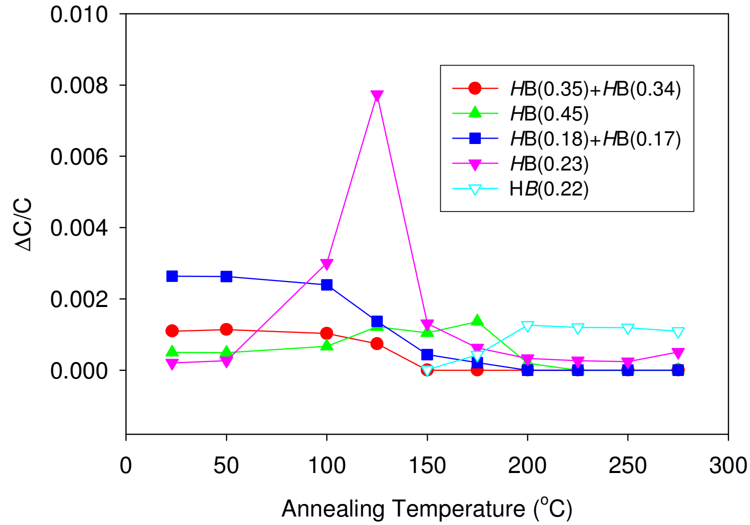

Fig. 6-9. Isochronal annealing behavior of defects in electron-irradiated B-doped Cz Si.

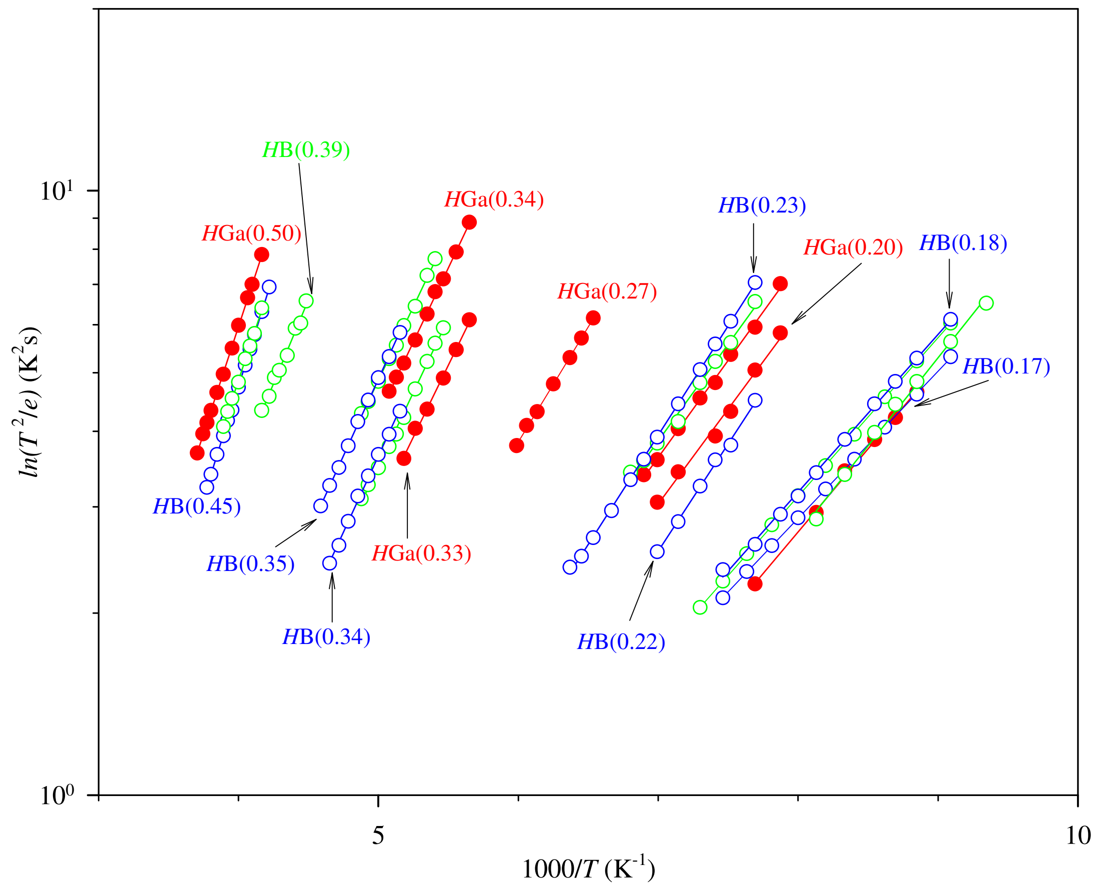

Fig. 6-10. Arrhenius plots of the primary and secondary defects introduced in B-doped epitaxial Si (green circles), Ga-doped Si (red circles) and B-doped Cz Si (blue circles) by 1 MeV electron irradiation.

6.4 Summary and conclusions

LDLTS has been succesfully used to separate closely spaced defects introduced in Ga-doped Cz, B-doped epitaxial and B-doped Cz silicon after 1 MeV electron irradiation. In Ga-doped samples, primary hole traps *H*Ga(0.18), *H*Ga(0.19), *H*Ga(0.23), *H*Ga(0.33) and *H*Ga(0.34) have been observed. The closely spaced pair of defects *H*Ga(0.18); *H*Ga(0.19) and *H*Ga(0.33); *H*Ga(0.34) appeared as a single peak in DLTS and was resolved by LDLTS. *H*Ga(0.19) has been identified as (+/0) charge state of the divacancy and *H*Ga(0.34) as the C_I-O_I center. The annealing studies further revealed the introduction of hole traps *H*Ga(0.20), *H*Ga(0.27), and *H*Ga(0.50). In the B-doped epitaxial and Cz silicon, the electron irradiation revealed similar hole traps *H*B(0.17), *H*B(0.18), *H*B(0.23), *H*B(0.34) *H*B(0.35) and *H*B(0.45). LDLTS was successfully used to separate the closely spaced defect levels *H*B(0.17) and *H*B(0.18) and similarly the levels *H*B(0.34) and *H*B(0.35) were resolved. *H*B(0.18) has been identified as the divacancy and *H*B(0.35) is the C_I-O_I complex. A defect level *H*B(0.22) was observed in the Cz sample but not in epitaxial sample, which may suggest that it is O-related. The deduced introduction rates for *H*B(0.17) and *H*B(0.35) after 1 MeV electron irradiation were 5.0 x 10^{-3} cm^{-1} and 2.0 x 10^{-3} cm^{-1} respectively, and introduction rates for *H*Ga(0.19) and *H*Ga(0.34) were 4.0 x 10^{-3} cm^{-1} and 2.5 x 10^{-2} cm^{-1} respectively and these rates are consistent with introductiomn rates related to electron irradiation.

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List of Publications

1. Cloud Nyamhere, P.N.K. Deenapanray, F.D. Auret and F.C. Farlow, "*Characterisation of Defects Created in Cz and epitaxial Si doped with Ga or B using Laplace-DLTS*", Physica B **376-277** (2006) 161-164.
2. Cloud Nyamhere, A.G.M. Das, F.D. Auret and M. Hayes, "*Deep Level Transient Spectroscopy Characterisation of Defects Introduced in p-Si Electron Beam Deposition and Proton Irradiation*", Journal of Physics, Conference Series, vol.**100** (2008), 042004.
3. A.G.M. Das, C. Nyamhere and F.D. Auret *"A Comparitive Study of electronic properties of defects introduced in p-Si (i) During Electron Beam Deposition of Ti/Mo, (ii) by proton irradiation and (iii) by electron irradiation*", Surface and Coatings Technology, Vol. **203** (2009) 2628-2631.