Chapter 1

Introduction

The modern day technological advancement is almost entirely dependent on the semiconductor devices. The application of semiconductors in the device fabrication commonly requires that defects be introduced in the semiconductor lattice, intentionally by radiating with energetic particles or unintentionally during processing stages. Defects can be introduced in the lattice during semiconductor processing techniques such as semiconductor growth, ion implantation, plasma etching, annealing, metallization, (sputter and electron beam deposition) or by particle irradiation. These defects modify the properties of the substrate and therefore influence the performance of devices fabricated thereon. Defects may have detrimental effects on the performance of devices such as solar cells, wherein they act as efficient recombination centers and degrade minority carrier lifetimes [1]. However, there are other instances when defects are created intentionally to produce impurity - related defect levels in the semiconductor band gap, i.e. to absorb low energy photons known as impurity photovoltaic effect and as efficient recombination centers in fast-switching silicon power devices [2]. A true understanding of a defect in a semiconductor usually requires achieving four steps (a) defect observation and characterization, (b) defect identification, (c) defect control, and (d) influence of defects on device performance. The knowledge of how defects influence the device performance is the basis for development of improved semiconductor devices. For this basic motivation, defect characterization is still a very much active field for all technological important semiconductors until all aspects of defects are well understood. Although a lot of work has been done on defects introduced in silicon (Si) materials in the last two decades, most of the defects have not been identified. Silicon integrated circuits presently dominate the semiconductor industry and recently it has been used to develop, high efficiency and low cost solar cells as the search for

alternative energy sources continues. To achieve high efficiency (i.e. faster switching speeds, low power consumption, etc) devices, great emphasis is now placed on decreasing the lateral and vertical dimensions of the individual transistors (miniaturization). With the reduction in size the devices become sensitive to minute defect concentration therefore it is essential to identify and control defects in the substrate, thereby reducing or eliminating those that are detrimental to the device and retaining those that are beneficial to the device operation.

It is interesting to note that the first transistor invented in 1947 by J. Bardeen and W.H Brattain used elemental germanium (Ge) as the semi-conducting material, but since then silicon soon replaced germanium as substrate material because of its inherent advantages, such as thermal stability, abundance and availability of a stable oxide, (SiO_2). Recently there has been a sudden growing interest in Ge as a possible candidate for high performance complimentary metal-oxide-semiconductor (CMOS) devices and faster switching transistors because of the higher electron and hole mobilities of Ge at low electric fields when compared to Si [3].

Conventional Deep Level Transient Spectroscopy (DLTS) [4] is a powerful junction capacitance tool that is used to study defects introduced in semiconductors. DLTS is particularly attractive because it can be used to characterize defects using various kinds of space-charge-based devices, ranging from simple Schottky barrier diodes (SBDs) and p-n junctions, MOS structures (which are all standard building blocks of solid state circuitry) to device structures with higher degrees of complexities [5]. The recent development of high-resolution Laplace – DLTS [6,7] has significantly increased its spectroscopic ability, by giving over an order of magnitude improved energy resolution in studies of thermal emission of carriers from deep states, thereby facilitating the separation of the closely spaced energy levels that show up as a single broad feature in conventional DLTS. The L-DLTS has a remarkable sensitivity (it can probe very low concentrations of defects $>10^{10}$ cm^{-3}), can be used to probe very narrow regions of semiconductors (e.g. regions of shallow implants) and even be used to study selectively the active regions of devices (Differential DLTS [8,9]).

Deep levels in crystalline Si and Ge have been systematically characterized by DLTS and LDLTS after exposing the materials to energetic particles (MeV electrons or keV

Ar ions) and metal deposition (resistive deposition, electron beam deposition or sputter deposition). Particle irradiation and metal deposition are crucial and necessary stages during device processing steps, such as ion implantation for doping, metallization for low resistive for low resistive ohmic contacts as well as rectifying contacts, and plasma etching. Therefore it is of paramount importance to study the properties of these defects and their effects on device application.

An overview of the semiconductor theory with the emphasis on Si and Ge is given in chapter 2 since these materials are the substrates used in this study. Defects, their creation and annealing mechanisms, resulting from bombardment with energetic particles in semiconductors, are described in chapter 3. The underlying theory behind DLTS and Laplace-DLTS is presented in chapter 4 followed by the experimental techniques in chapter 5. The results of defects created during processing steps or by irradiation of silicon and germanium are presented in chapters 6, 7, 8, 9 and 10, while chapter 11 gives a summary of the work covered in this thesis.

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Chapter 2

Semiconductor Theory

2.1 Introduction

In this chapter semiconductor theory is discussed. Section 2.2 presents the crystal structure and the energy band theory, particularly for silicon and germanium. The importance of energy band theories for a crystalline solid is due to the fact that many important physical and optical properties of a solid can be readily explained using its energy band structure. In principle, the energy band structure of a solid can be constructed by solving the Schrödinger equation for electrons in a crystalline solid that contains a large number of interacting electrons and atoms. Section 2.3 discusses the metal-semiconductor junctions. A metal–semiconductor contact will either form a Schottky or an ohmic contact. These contacts are very important since they make it possible to electrically probe the semiconductor underlying layer by various characterization tools, such as current-voltage, capacitance-voltage and deep level transient spectroscopy (DLTS) measurements, which have been employed in this work. Section 2.4 presents the current transport mechanism through the metal-semiconductor junctions.

2.2 The Crystal and Band Structure of Si and Ge

Elemental semiconductors such as silicon and germanium crystallize into the diamond structure. The diamond structure shown in Fig. 2-1 is actually formed by two interpenetrating face-centered cubic (fcc) lattices with the vertex atom of one fcc sublattice located at (0, 0, 0) and the vertex atom of another fcc sublattice located at (a/4, a/4, a/4), where a is the lattice constant. In the diamond lattice structure, the

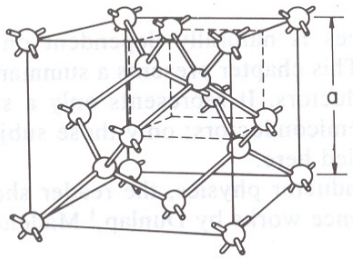


Fig. 2-1. Diamond structure redrawn from ref. 1.

primitive basis of two identical atoms located at (0, 0, 0) and (*a*/4, *a*/4, *a*/4) is associated with each lattice point of the fcc lattice. The band structure of a crystalline solid, that is, the energy-momentum (*E*-*k*) relationship is usually obtained by solving the Schrödinger equation of an approximate one-electron problem. The Bloch theorem, states that if a potential energy $V(\vec{r})$ is periodic with the periodicity of the lattice, then the solutions $\phi_k(\vec{r})$ of the Schrödinger equation [1-2]

$$\left[-\frac{\hbar^2}{2m}\nabla^2 + V(\vec{r})\right]\phi_k(\vec{r}) = E_k\phi_k(\vec{r}) \tag{2.1}$$

are of the form

$$\phi_k(\vec{r}) = e^{j\vec{k}.\vec{r}}U_n(\vec{k}.\vec{r}) \text{ (Bloch function)} \tag{2.2}$$

where, $U_n(\vec{k},\vec{r})$ is periodic in $\vec{r}$ with periodicity of the lattice and *n* is the band index. From the Bloch theorem one can show that the energy $E_{\vec{k}}$ is periodic in the reciprocal lattice. For a given band index, to label the energy uniquely, it is sufficient to use only *k*'s in a primitive cell of the reciprocal lattice.

The energy bands of solids have been studied theoretically using a variety of numerical methods. For semiconductors the three methods most frequently used are the orthogonalized plane-wave method [3-4], the pseudopotential method [5], and the **k.p** method [6]. Fig. 2-2 depicts the energy-band structures for Ge and Si [1,7]. For any semiconductor there is a forbidden energy region in which allowed states cannot exist, which is called the energy gap E_g. The energy gap is the most important

parameter in semiconductor physics. Electron states are permitted above and below this energy gap. The bands above the energy gap are called the conduction bands and below the energy gap, the valence bands. The two top valence bands (Fig. 2-2) can be approximately fitted by two parabolic bands with different curvature: the heavy-hole band (the wider band with a smaller $\partial^2 E/\partial k^2$) and light-hole band (the narrower band with larger $\partial^2 E/\partial k^2$). The lowest conduction minimum is along the $\langle 111 \rangle$ axes in Ge and along $\langle 100 \rangle$ axes in Si. The band structure of Si shows six equivalent conduction minima and three valence band maxima all at the center of Brillouin zone. The valence band tops are degenerate and the third one is split-off by 44 meV.

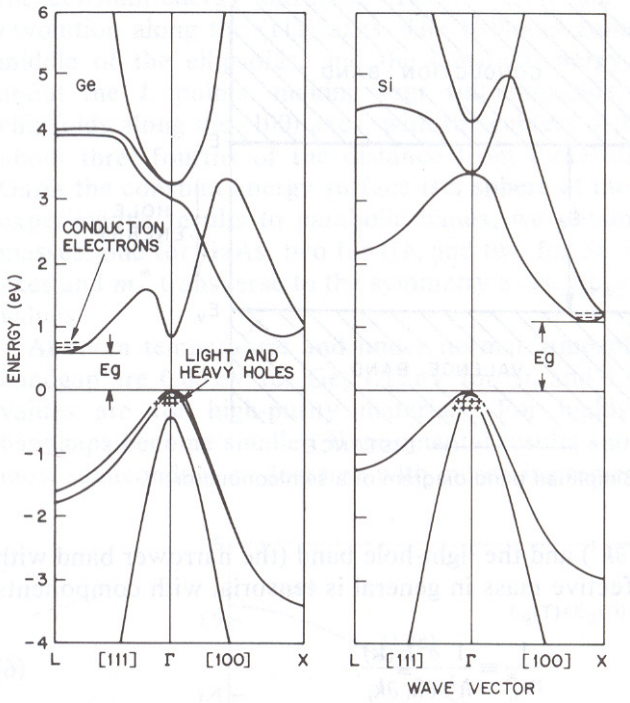


Fig. 2-2. Energy band structure of Ge and Si, where E_g is the energy band gap. Plus signs indicate the holes in the valence band and minus signs indicate electrons in the conduction band (after ref. 1).

At room temperature (300 K) and under normal atmosphere, the values of the band gap are 0.66 eV for Ge, and 1.12 eV for Si [1]. These values are for high-purity materials. For highly doped materials the band gaps become smaller. Experimental results show that the band gaps of Ge and Si decrease with increasing temperature and the relationship can be expressed approximately by a universal function given by equation (2.3),

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(T+\beta)} \tag{2.3}$$

where, $E_g(0)$ is the energy gap at T = 0 K , α and β are material constants given in Table 2.1.

Table 2.1. Coefficients for the temperature dependent energy band gap of Si and Ge.

Material	$E_g(0)$ (eV)	α (x 10^{-4} eV/K)	β (K)
Si	1.519	4.730	636
Ge	1.170	4.774	235

The temperature coefficient dE_g / dT is negative for Ge and Si [1]. Near room temperature, the band gap of Ge increases with pressure and that of Si decreases with pressure [8] as shown in equation (2.4),

$$\frac{dE_g}{dP} = \begin{cases} 5.0\times10^{-6} \text{ eV/(kg/cm}^2\text{)} & \text{for Ge} \\ -2.4\times10^{-6} \text{ eV/(kg/cm}^2\text{)} & \text{for Si} \end{cases} \tag{2.4}$$

The mobility of electrons and holes is an important semiconductor property, which depends on the band structure. For bulk-grown Si and Ge the hole and electron mobilities at room temperature are listed in Table 2.2.

Table. 2.2. Mobilities (at room temperature) in bulk Si and Ge

Material	μ_e (cm^2/Vs)	μ_h (cm^2/Vs)
Si	1500	450
Ge	3900	1900

The values show higher mobilities in Ge when compared to Si, by nearly a factor of 2 for electron mobility and a factor of 4 for hole mobility. Experiment [9] has shown that the band structure can be affected by the application of stress, breaking the

degeneracy of both the conduction and the valence band. This has an effect of increasing the electron and hole mobility in a given semiconductor.

2.3 Metal – Semiconductor Junctions

Metal-semiconductor contacts are an integral part of the semiconductor industry. It is well known that one of the most important aspects of realizing the potential of a semiconductor device is the preparation of high quality metal contacts to the material. There are two types of metal-semiconductor contacts, ohmic and Schottky (rectifying) contacts. The Schottky contacts can be used for a wide variety of device applications e.g. microwave receiver detectors, mixers [10] and used as gate electrodes of field-effect transistors (MESFETS), the drain and source in MOSFETS [1]. In addition to these several device applications, Schottky contacts may also be used to study bulk defects (introduced during material growth, during device processing or by energetic particles such electrons or protons) and interface properties of a metal-semiconductor system. In this study the Schottky contacts have been used to form the space charge region, which is used to probe the semiconductor forbidden gap and measure the electrical properties of the defect levels on and beneath the metal-semiconductor interface.

2.3.1 Schottky Barrier Junctions

In principle, for a Schottky barrier junction, there is nonlinear current flow through the device, allowing current to flow in one direction but not the other (rectifying effect). According to the Schottky-Mott model, [11-12] the barrier height of an ideal Schottky contact between a metal and an *n*-type semiconductor in the absence of surface states is equal to the difference between the metal work function ϕ_m and the electron affinity χ of the semiconductor, which can be written as

$$\phi_{Bn} = \phi_m - \chi \tag{2.5}$$

The work function of a metal ϕ_m is defined as the minimum amount of energy required to remove an electron completely from the metal into free space (the so called vacuum level). The work function of a metal is a fundamental property of the

particular metal (measured in eV). Similarly the work function of a semiconductor ϕ_{sc} is the difference in energy between the Fermi level and the vacuum level. The electron affinity χ is the difference between the vacuum level and bottom of the conduction band and is independent of the doping concentration of the semiconductor material. The work function of the semiconductor material ϕ_{sc} and the electron affinity χ are related by the following equation,

$$\phi_{sc} = \chi + \xi \tag{2.6}$$

where, ξ is the energy difference between the Fermi level and conduction band in the neutral region of the semiconductor and is given by

$$\xi = kT\ln(N_C / N_D) \tag{2.7}$$

where, k is the Boltzmann constant, T is the temperature, N_C is the effective density of states in the conduction band and N_D is the free carrier concentration. The schematic energy band diagrams in Fig. 2-3 show the process of barrier formation according to the Schottky-Mott theory. We assume a uniformly doped *n*-type semiconductor and that $\phi_m > \phi_{sc}$, Fig. 2-3a shows the case when the materials are isolated from each other. The average energy of electrons in the semiconductor is greater than the average energy of those in the metal. When the metal is brought into intimate (perfect) contact with the semiconductor (with no surface states), the difference in the average electron energy will transfer electrons from semiconductor to the metal. The electron transfer will take place until the Fermi levels coincide, and thermal equilibrium is established, Fig. 2-3b. Relative to the Fermi level in the metal, the Fermi level in the semiconductor is lowered by an amount equal to the difference between the two work functions, causing band bending. This difference between the work functions is called the built-in-voltage (V_{bi}) given by, $V_{bi} = (\phi_m - \phi_{sc})$. Simultaneously an electric field is created due to the negative charge on the surface of the metal that is balanced by an equal but positive charge in the semiconductor. Due to the relatively low dopant concentration, this positive charge is distributed

throughout a barrier region near the semiconductor surface, up to a thickness W_o in the semiconductor, which is the depletion width.

An electron at the Femi level in the metal will see a potential barrier towards the semiconductor of ϕ_{Bn} which is the difference between ϕ_m and χ. Whereas an electron deep in the semiconductor at $E = E_C$ sees a potential barrier towards the metal of $V_{bi} = (\phi_m - \phi_{sc})$.

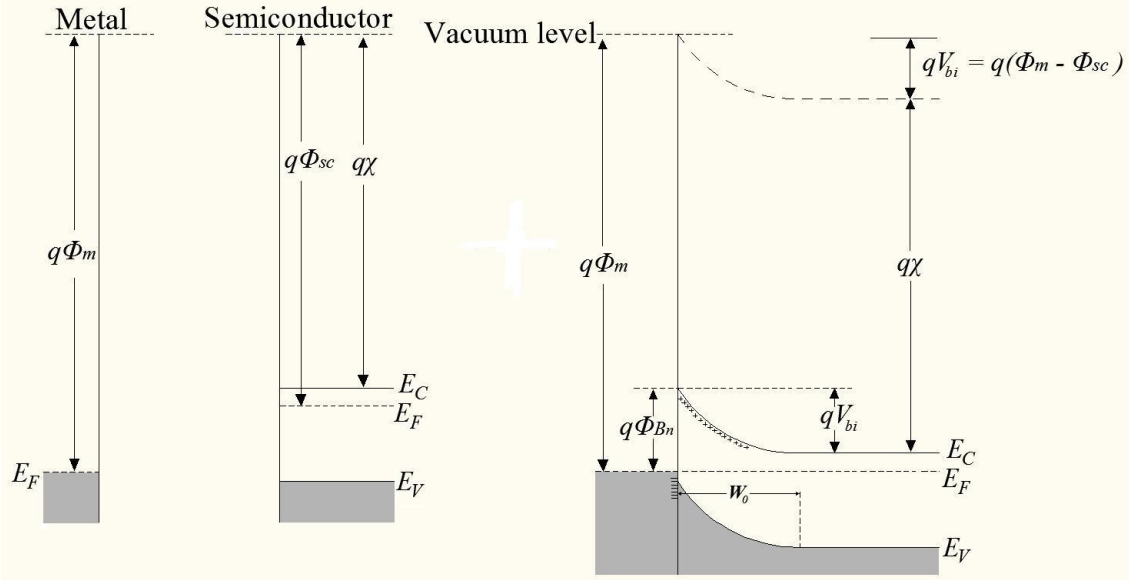
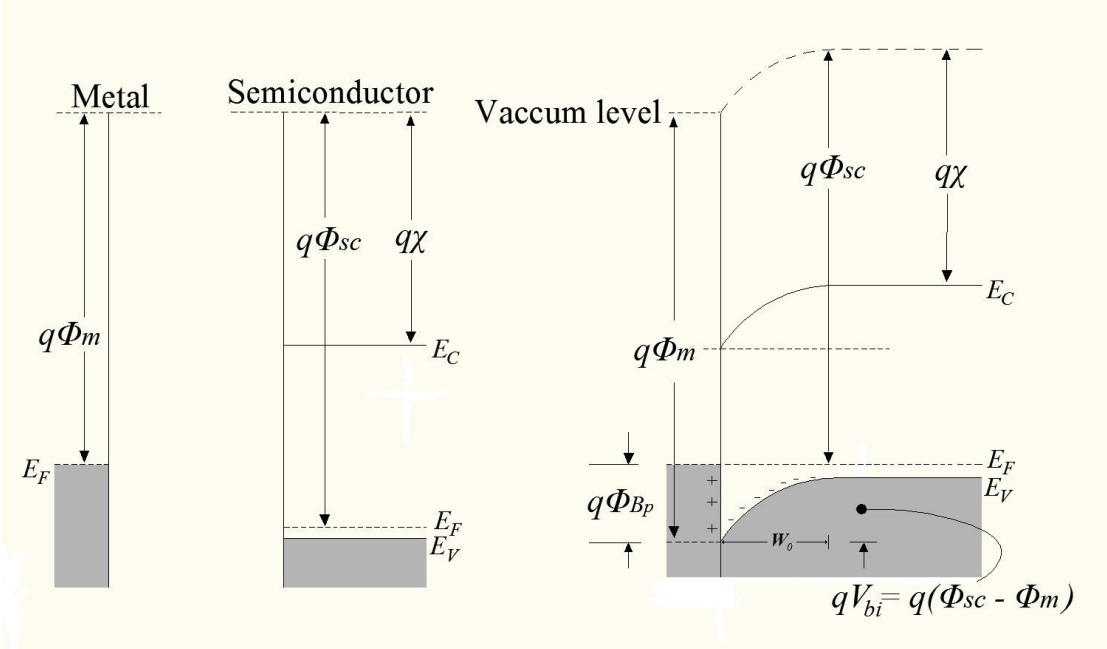


Fig. 2-3. Energy band diagrams of a metal/n-type semiconductor with $\phi_m > \phi_{sc}$ (a) materials isolated from each other and (b) at thermal equilibrium after contact is made, redrawn from ref. 13.

When a bias voltage is applied across the junction, non-equilibrium conditions are established. Under zero bias conditions, electrons at the Fermi level from both the metal and semiconductor see the same barrier height. Therefore there is no net flow of electrons over the barrier in either direction. Applying a negative potential V_a on the semiconductor side, causes the band bending to decrease. This reduces the barrier for electrons crossing from the semiconductor toward the metal from qV_{bi} to $q(V_{bi} - V_a)$, i.e. forward biasing condition. The electrons can now cross from the semiconductor to the metal more easily since they now see a reduced barrier. When a positive potential V_a is applied to the semiconductor, the barrier for electron from the metal increases by

qV_a. This also increases the depletion width. The number of electrons with enough energy to cross the barrier from the semiconductor to the metal is reduced due the increased barrier, i.e. reverse biasing condition. The barrier seen by electrons from the metal stays the same as the number of electrons crossing from the semiconductor to metal decreases.



(a) (b)

Fig. 2-4. Energy band diagrams of a metal/p-type semiconductor with $\phi_m < \phi_{sc}$ (a) materials isolated from each other and (b) at thermal equilibrium after contact is made, redrawn from ref. 13.

A barrier can also be formed between a metal and *p*-type semiconductor. Consider a *p*-type semiconductor having $\phi_m < \phi_{sc}$ with the two materials isolated from each other, Fig. 2-4(a). When the two substrates are brought into intimate contact, electrons will flow from the metal into the semiconductor until, E_F, is the same throughout, Fig. 2-4(b). Each electron flowing into the semiconductor removes a hole from the valence band, leaving behind an unneutralized charge of ionized acceptors in the semiconductor, forming a depletion region in the semiconductor. Since the current in *p*-type semiconductors is carried mainly by holes, the contact shown in Fig. 2-4(b) is therefore rectifying and in the absence of surface states the barrier height ϕ_{Bp} can be expressed by

$$\phi_{Bp} = \frac{E_g}{q} - (\phi_m - \chi) \tag{2.8}$$

where, E_g is the energy band gap and q is the electron charge. From equation (2.8) it follows that, according to the Schottky-Mott theory, for a given semiconductor and for any metal, the sum of the barrier heights on *n*-type and *p*-type substrates is equal to the band gap, or

$$q(\phi_{Bn} + \phi_{Bp}) = E_g \tag{2.9}$$

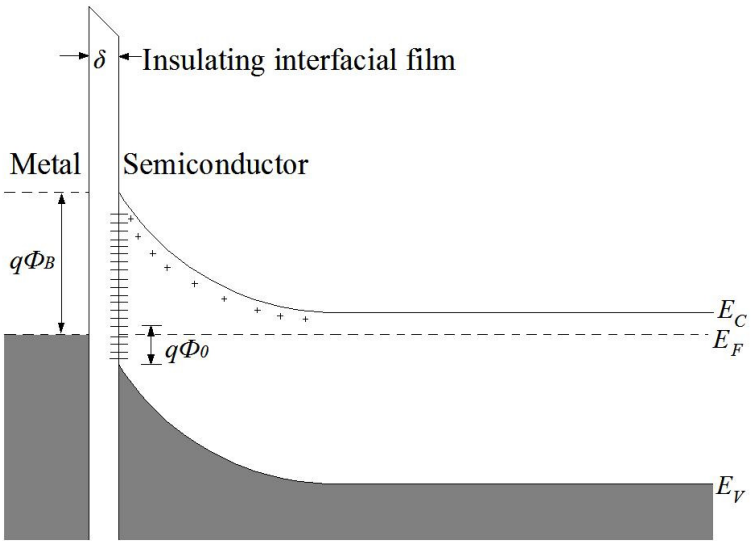


Fig. 2-5. Energy band diagram of a metal-semiconductor contact with surface states and an interfacial oxide layer of thickness δ.

It should be noted that in reality the measured barrier heights for most of the metal-semiconductor contacts do not always follow the simple predictions given by the equations (2.5) and (2.8) because in their derivation we did not consider the thin insulating layer of oxide on the semiconductor surface, interface states and the image force lowering effect. In fact, for most compound semiconductors, because of high surface state density and Fermi-level pinning at the interface states, the barrier height formed is found to be independent of the metals used [1], and this is also true for covalently bonded semiconductors like Ge and Si [13]. In a covalently bonded crystal, the surface atoms have no neighbors on the vacuum side, with which they can form covalent bond. Thus, each surface atom has one broken covalent bond known as the

dangling bond. Dangling bonds give rise to surface states that are continuously distributed in energy within the forbidden gap. These states pin the Fermi level at the surface and thus influence the barrier height. Prior to metal deposition, the semiconductor surface is chemically cleaned. This process invariably leaves a thin (5 to 20 Å thick) [13] insulating oxide layer on the semiconductor surface. In the presence of interface states and a thin interfacial layer (Fig.2-5) the barrier height is given by [14],

$$\phi_B = \gamma(\phi_m - \chi) + (1-\gamma)(E_g - \phi_o) \tag{2.10}$$

where,

$$\gamma = \frac{\varepsilon_i}{\varepsilon_i + q\delta D_s} \tag{2.11}$$

δ being the thickness of the interfacial layer, E_g the band gap, ϕ_o the so-called neutral level, ε_i the permittivity of this film and D_s the density of interface states per eV per unit area in the band gap. The surface states are characterized by the neutral level ϕ_o such that all the states below ϕ_o are filled, while those above are empty. Equilibrium is reached when electrons from the semiconductor adjacent to the surface occupy states above ϕ_o. Thus, the surface becomes negatively charged and a depletion region is created within the semiconductor near the surface. If a metal is now brought into contact with the semiconductor, exchange of the electrons takes place between the metal and the semiconductor surface states, while the depletion charge remains practically unchanged. Thus ϕ_B tends to the Schottky-Mott limit $(\phi_B = \phi_m - \chi)$ as $D_s \rightarrow 0$ and to the Bardeen limit $(\phi_B = E_g - \phi_o)$ as $D_s \rightarrow \infty$. Thus, if the density of surface states becomes high enough, the Fermi level is said to be pinned at $E_F \approx \phi_o$ so that,

$$\phi_B \approx E_g - \phi_o \tag{2.12}$$

which is the Bardeen limit.

2.3.2 Depletion Layer

It has been discussed in the previous section that when a metal is brought into intimate contact with a semiconductor, the conduction and valence bands of the semiconductor are brought into a definite energy relationship with the Fermi level in the metal. Once this relationship is known, it serves as the boundary condition on the solution of the Poison equation in the semiconductor. The boundary conditions are obtained from,

(i) barrier height and

(ii) taking electric field in the bulk of the semiconductor as zero.

At the interface, taking $x = 0$, the boundary condition can now be written as $V(0) = V_{bi}$ and $E(\infty) = 0$, where V is the contact potential, V_{bi} is built-in potential and E is the electric field. The Poisson's equation in the semiconductor can be written in one dimension as

$$\frac{d^2V}{dx^2} = -\frac{1}{\varepsilon_s}\rho(x) \tag{2.13}$$

where, $\rho(x)$ is the total charge density in the semiconductor at a depth x and ε_s is the permittivity of the semiconductor. Generally, $\rho(x)$ should include contributions form the valence band, conduction band, ionized donors and acceptors, and deep levels in the band gap. This will lead to a complicated equation which requires numerical methods to solve. To simplify the equation, the abrupt approximation is used. Considering the abrupt approximation, it is assumed that the semiconductor can be divided into two regions: (i) the depletion region, directly below the metal, which contains no free carriers, and (ii) the bulk semiconductor, which is electrically neutral, and in which no electric field exists. In the depletion region, $\rho(x) \approx qN_D$, and in the semiconductor bulk, $\rho(x) \approx 0$ and $dV/dx \approx 0$. If the width of the depletion region is W, the charge density in the semiconductor can be written as

$$\rho(x) = \begin{cases} qN_D & \text{if } x \le W \\ 0 & \text{if } x > W \end{cases} \tag{2.14}$$

where, N_D is the density of dopants and q the electronic charge. Integrating equation 2.13 twice and applying the boundary condition, the depletion width can be written as

$$W = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_D}} \tag{2.15}$$

When the contact is biased by an externally applied voltage V_a, the depletion width can be written as

$$W = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_{bi} - V_a - \frac{kT}{q}\right)} \tag{2.16}$$

where, the term kT/q arises from the contribution of the majority carrier distribution tail. It is seen from equation (2.16) that the depletion layer width is directly proportional to the square root of the applied voltage, and inversely proportional to the square root of the dopant density of the semiconductor. The electric field in the semiconductor is given by

$$E(x) = -\frac{qN_D}{\varepsilon_e}(W - x) = \frac{qN_D}{\varepsilon_s}x - E_m \tag{2.17}$$

where, E_m is the maximum field strength which occurs at $x = 0$. Integrating the electric field yields the electrostatic potential,

$$V(x) = \frac{qN_D}{\varepsilon_e}(Wx - \frac{1}{2}x^2) - \phi_{Bn} \tag{2.18}$$

The space charge Q_{sc} per unit area of the semiconductor and the depletion-layer capacitance C per unit area are given by

$$Q_{sc} = qN_D W = \sqrt{2q\varepsilon_e N_D\left(V_{bi} - V_a - \frac{kT}{q}\right)} \tag{2.19}$$

$$C = \frac{\left|\partial Q_{sc}\right|}{\partial V_a} = \sqrt{\frac{q\varepsilon_s N_D}{2(V_{bi} - V_a - kT/q)}} = \frac{\varepsilon_s}{W} \tag{2.20}$$

equation (2.20) can be written in the form,

$$\frac{1}{C^2} = \frac{2(V_{bi} - V_a - kT/q)}{q\varepsilon_s N_D} \tag{2.21}$$

or

$$N_D = \frac{2}{q\varepsilon_s}\left[-\frac{1}{d(1/C^2)/dV}\right] \tag{2.22}$$

If N_D is constant throughout the depletion region, a plot of $1/C^2$ versus V should yield a straight line graph. If N_D is not a constant then the differential capacitance method can be used to determine the doping profile from equation (2.22). Using the voltage axis intercept, the barrier height can be determined from the equation,

$$\varphi_{Bn} = V_i + \xi + \frac{kT}{q} - \Delta\phi \tag{2.23}$$

where V_i, is the voltage axis intercept (equivalent to V_{bi}), $\Delta\phi$ is the image force barrier lowering, and ξ, the depth of the Fermi level below the conduction band, which can be computed if the doping level is known.

2.3.3 Ohmic Contacts

An ohmic contact is defined as a metal-semiconductor contact that has a negligible contact resistance R_c, relative to the bulk or spreading resistance of the semiconductor, given by $R_C = \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0}$, when evaluated at zero bias. A good ohmic contact would have very small voltage drop even at large current levels, and that the voltage drop would be the same for both forward and reverse current flow.

The following two major approaches can be used to achieve ohmic contacts to semiconductors:

(a) If one can find metal-semiconductor combinations in which the barrier height is determined by the difference in their work functions, it should be possible to create an ohmic contact by choosing the metal with $\phi_m < \phi_{sc}$ in the case of *n*-type semiconductor, (Fig. 2-6a and b) and $\phi_m > \phi_{sc}$ in *p*-type semiconductor, a typical ideal ohmic contact. A low-resistance symmetrical contact to a semiconductor is obtained if the barrier is small compared with *kT*. When this is the case, carriers can flow over the barrier in either direction with little resistance as shown in Fig.2-6c. It can be shown that, [1]

$$R_C = \frac{k}{qA^*T}\exp\left(\frac{q\phi_{Bn}}{kT}\right) \qquad (2.24)$$

Equation (2.24) shows, that low barrier height should be used to obtain small R_c. Since for most semiconductors, because of the presence of interface states, ohmic contacts cannot be obtained by proper choice of metal work function and a metal does not generally exist with low-enough work function to yield a low barrier.

(b) An alternate and more practical contact is a tunnel contact shown in Fig. 2-6d. Such contacts have a high enough doping in the semiconductor so that there is only a thin barrier separating the metal from the semiconductor interface, and carriers can readily tunnel across such barrier. The required doping density for such contact is 10^{19} cm^{-3} or higher [1].

The fabrication of ohmic contacts frequently includes a high temperature annealing step so that the deposited metals can either alloy with the semiconductor or the high-temperature anneal, reduces the unintentional barrier at the interface. In case of Ge, Au-Sb alloy with (0.1% Sb) is first evaporated onto back of the Ge. These contacts are then annealed at 350˚C under inert conditions such as nitrogen or argon [12] to reduce contact resistance by increasing the tunneling current as shown in Fig 2-6 (d). The use of a reducing atmosphere reduces any further oxidation of the metal during

annealing, while it can also reduce any interfacial oxide between the metal and semiconductor.

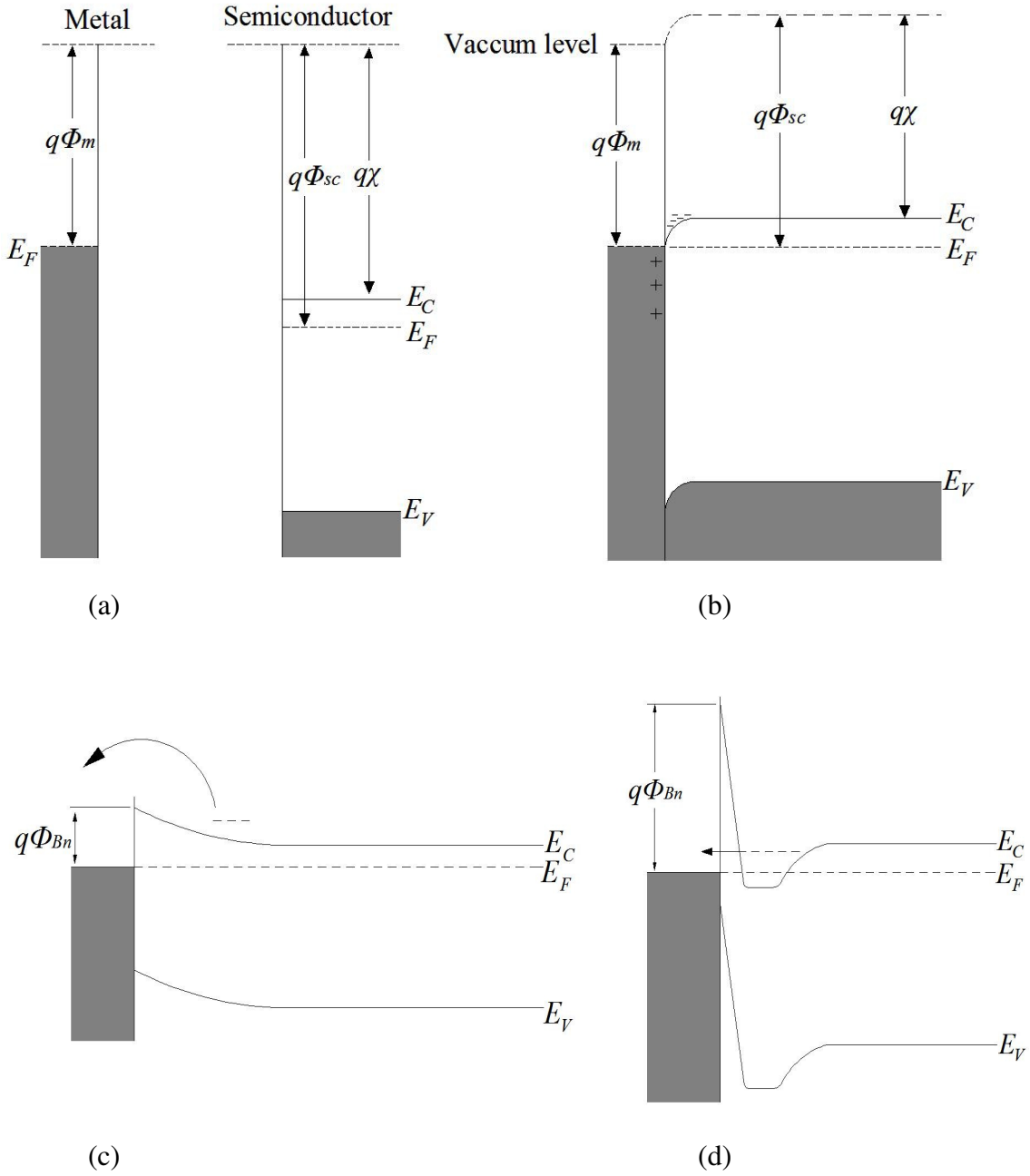


Fig. 2-6. Energy band diagrams of a metal/n-type semiconductor with $\phi_m < \phi_{sc}$. (a) Materials isolated from each other and (b) at thermal equilibrium after contact is made (ideal ohmic contact formation) redrawn from ref. 16. Ohmic contact formation by, (c) low barrier height and (d) high doping contacts, redrawn from ref. 1.

2.4 Current Transport Mechanisms in Metal – Semiconductor Junctions

The electrical properties of Schottky contacts are determined by the transport mechanisms across the barrier. The current transport in metal-semiconductor contacts is mainly due to majority carriers. The various ways in which electrons can be transported across a metal – semiconductor junction under a forward bias are:

(a) emission of electrons from the semiconductor over the top of the barrier into the metal [the dominant process for Schottky diodes with moderately doped semiconductor (e.g., $N_D \leq 10^{17}$ for Si) operated at moderate temperatures (e.g., 300 K)],

(b) quantum-mechanical tunneling through the barrier (important for heavily doped semiconductors and responsible for most ohmic contacts),

(c) recombination in the charged space region, and

(d) hole injection from the metal to semiconductor (equivalent to recombination in the neutral region).

In addition, we may have edge leakage current due to a high electric field at the contact periphery or interface current due to traps at the metal-semiconductor interface. The inverse processes occur under reverse bias. It is possible to make practical diodes in which (a) is the most important and such diodes are generally referred to as 'nearly ideal'. Process (b), (c) and (d) cause departures from ideality. There are two basic processes that govern the emission of electrons from the semiconductor over the top of the barrier into the metal, (i) electrons are transported from the bulk of the semiconductor and across the depletion region of the semiconductor by the mechanism of drift and diffusion in the electric field of the barrier, and (ii) at the interface, their emission into the metal is determined by the rate of transfer of electrons across the boundary between the metal and semiconductor. These two processes are effectively in series and according to the diffusion theory by Schottky [10] the first process is more important, whereas according to the thermionic–emission theory of Berthe [14] the assumption is that the current-limiting process is the actual transfer of electrons across the interface between the semiconductor and the metal. In case of the moderately doped Si and Ge Schottky diodes used in this study, the dominant mechanism for reverse bias and small forward bias is thermionic-emission. Assuming that the velocity distribution of the electrons in

the conduction band is Maxwellian and ideal rectifier characteristics, the current density, J flowing across the barrier can be written as,

$$J = A^{*}T^{2}\exp(-q\phi_{B}/kT)[\exp(qV/kT)-1] \tag{2.25}$$

where, A^{*} is the effective Richardson constant, ϕ_{B} is the barrier height and, T the temperature of the junction, provided the barrier height is independent of bias. The current density for a non-ideal diode can be written as,

$$J = J_{0}[\exp(qV/nkT)-1], \quad \text{where } J_{o} = A^{*}T^{2}\exp(-q\phi_{B}/kT) \tag{2.26}$$

with series resistance R_{s} and $V > 3kT/q$ equation (2.26) is now given by,

$$J \approx J_{0}\exp\left(\frac{q(V-IR_{s})}{nkT}\right) \tag{2.27}$$

where, J_{o}, is the saturation current density obtained by extrapolating the current density from the log-linear region to $V = 0$ and, n, is the ideality factor defined as

$$n = \frac{q}{kT}\left[\frac{\partial V}{\partial(\ln J)}\right] \tag{2.28}$$

The ideality factor has been introduced in equations (2.26) and (2.27) to account for deviation of the diodes from ideal behaviour. For an ideal Schottky diode, the barrier height is independent on the bias and current flows only due to thermionic emission. The saturation current density, J_{o}, can be expressed as,

$$J_{0} = A^{*}T^{2}\exp\left[-q\left(\frac{\phi_{Bo}-\Delta\phi_{ifl}}{kT}\right)\right] \tag{2.28}$$

where, ϕ_{Bo} is the zero bias barrier height, and $\Delta\phi_{ifl}$ is the barrier lowering by the image force. The effective zero bias barrier height is given by, $\phi_{e} = \phi_{Bo} - \Delta\phi_{ifl}$. From

the graph of $ln(J)$ versus V, it is possible to determine n, J_o and R_s. A least squares curve fitting procedure is applied to the linear region (forward bias region) of this graph. The ideality factor is proportional to the inverse of the gradient of this fit. The value of J_o, is obtained by the extrapolation of the linear fit to $V = 0$ V. An expression for the effective barrier height (at $V = 0$ V), is given by,

$$\phi_{eo}^{I-V} = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_o}\right) \tag{2.29}$$

A theoretical value for the effective Richardson constant, A^*, can be determined by using the following equation,

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{2.30}$$

where m^* is the electron effective mass.

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