

**DYNAMIC RANGE AND SENSITIVITY IMPROVEMENT OF INFRARED  
DETECTORS USING BICMOS TECHNOLOGY**

by

**Johan Venter**

Submitted in partial fulfilment of the requirements for the degree  
Master of Engineering (Microelectronic Engineering)

in the

Department of Electrical, Electronic and Computer Engineering  
Faculty of Engineering, Built Environment and Information Technology

UNIVERSITY OF PRETORIA

February 2013

## SUMMARY

---

### **DYNAMIC RANGE AND SENSITIVITY IMPROVEMENT OF INFRARED DETECTORS USING BICMOS TECHNOLOGY**

by

**Johan Venter**

Supervisor: Prof. S. Sinha

Department: Electrical, Electronic and Computer Engineering

University: University of Pretoria

Degree: Master of Engineering (Microelectronic Engineering)

Keywords: Bipolar complementary metal-oxide semiconductor integrated circuits, charged-coupled device image sensor, noise, dynamic range, sensitivity, quantum efficiency, SiGe, heterojunction bipolar transistor, infrared sensors, current, quantum wells

The field of infrared (IR) detector technology has shown vast improvements in terms of speed and performance over the years. Specifically the dynamic range (DR) and sensitivity of detectors showed significant improvements. The most commonly used technique of implementing these IR detectors is the use of charge-coupled devices (CCD). Recent developments show that the newly investigated bipolar complementary metal-oxide semiconductor (BiCMOS) devices in the field of detector technology are capable of producing similar quality detectors at a fraction of the cost. Prototyping is usually performed on low-cost silicon wafers. The band gap energy of silicon is 1.17 eV, which is too large for an electron to be released when radiation is received in the IR band. This means that silicon is not a viable material for detection in the IR band. Germanium exhibits a band gap energy of 0.66 eV, which makes it a better material for IR detection.

This research is aimed at improving DR and sensitivity in IR detectors. CCD technology has shown that it exhibits good DR and sensitivity in the IR band. CMOS technology exhibits a reduction in prototyping cost which, together with electronic design automation software, makes this an avenue for IR detector prototyping. The focus of this research is firstly on understanding the theory behind the functionality and performance of IR

detectors. Secondly, associated with this, is determining whether the performance of IR detectors can be improved by using silicon germanium (SiGe) BiCMOS technology instead of the CCD technology most commonly used.

The Simulation Program with Integrated Circuit Emphasis (SPICE) was used to realise the IR detector in software. Four detectors were designed and prototyped using the 0.35  $\mu\text{m}$  SiGe BiCMOS technology from ams AG as part of the experimental verification of the formulated hypothesis. Two different pixel structures were used in the four detectors, which is the silicon-only p-i-n diodes commonly found in literature and diode-connected SiGe heterojunction bipolar transistors (HBTs). These two categories can be subdivided into two more categories, which are the single-pixel-single-amplifier detectors and the multiple-pixel-single-amplifier detector. These were needed to assess the noise performance of different topologies. Noise influences both the DR and sensitivity of the detector.

The results show a unique shift of the detecting band typically seen for silicon detectors to the IR band, accomplished by using the doping feature of HBTs using germanium. The shift in detecting band is from a peak of 250 nm to 665 nm. The detector still accumulates radiation in the visible band, but a significant portion of the near-IR band is also detected. This can be attributed to the reduced band gap energy that silicon with doped germanium exhibits. This, however, is not the optimum structure for IR detection. Future work that can be done based on this work is that the pixel structure can be optimised to move the detecting band even more into the IR region, and not just partially.

## OPSOMMING

---

# VERBETERING VAN DIE DINAMIESE BEREIK EN DIE SENSITIWITEIT VAN INFRAROOI DETEKTORS DEUR VAN BICMOS-TEGNOLOGIE GEBRUIK TE MAAK

deur

**Johan Venter**

Studieleier: Prof. S. Sinha

Departement: Elektriese, Elektroniese en Rekenaaringenieurswese

Universiteit: Universiteit van Pretoria

Graad: Magister in Ingenieurswese (Mikro-elektroniese Ingenieurswese)

Sleutelwoorde: Bipolêre gekomplementeerde metaaloksiedhalfgeleier geïntegreerde baan, ladinggekoppelde toestel, ruis, dinamiese bereik, sensitiwiteit, beeldsensor, kwantumdoeltreffendheid, SiGe, heterovoegvlak-bipolêre transistor, infrarooi sensors, stroomvloei, kwantumput

Met verloop van tyd het verbetering in spoed en werkverrigting in die veld van infrarooi- (IR) bespeuring in sensors plaasgevind. Die omvang en sensitiwiteit van veral detektors in die besonder het vooruitgang getoon. Die implementeringtegniek wat die meeste gebruik word, is ladinggekoppelde toestelle (LGT). Onlangse ontwikkelinge toon dat nuwe navorsing oor bipolêre CMOS- (BiCMOS) toestelle dieselfde werkverrigting teen 'n veel laer koste kan lewer. Prototipe-ontwikkeling word gewoonlik gedoen op lae-koste silikonmateriaal. Die bandgapingenergie van silikon is 1.17 eV, wat te groot is om 'n elektron vry te stel wanneer IR-bestraling ontvang word. Dit beteken dat silikon nie 'n geskikte materiaal is vir bespeuring van bestraling in die IR-band nie. Germanium se bandgapingenergie is 0.66 eV, wat beteken dat dit beter is vir IR-bespeuring.

Hierdie navorsing is daarop gemik om dinamiese bereik (DB) en sensitiwiteit in IR-detektors te verbeter. LGT-tegnologie toon goeie DB en sensitiwiteit in die IR-band. CMOS-tegnologie behels 'n verlaging in prototipe-ontwikkelingskoste wat dit, tesame met elektroniese ontwerpoutomatisasie-sagteware 'n moontlikheid vir IR-detektorprototipe-ontwikkeling maak. Die fokus van die navorsing is eerstens om die onderliggende teorie



van die funksionering en werkverrigting van IR-detektors te verstaan. Tweedens, hiermee tesame, is dit om te bepaal of die werkverrigting van IR-detektors verbeter kan word deur silikon-germanium- (SiGe) CMOS-tegnologie te gebruik in plaas van die meer algemene LGT-tegnologie.

'n Simulasieprogram met geïntegreerde stroombaanbeklemtoning (SPICE) is gebruik om die detektor in sagteware te simuleer. Vier detektors is ontwerp en prototipes is vervaardig met die 0.35  $\mu\text{m}$  SiGe BiCMOS-tegnologie van ams AG as deel van die eksperimentele verifikasie van die geformuleerde hipotese. Twee verskillende tipes detektorstrukture is gebruik vir die vier detektors; die silikon-p-i-n-diodetipe wat gereeld in die literatuur genoem word en die diode-gekonnekteerde SiGe-hetero-aansluiting bipolar transistor (HBT) tipe. Die twee kategorieë kan verder verdeel word in twee sub-kategorieë, naamlik die enkel-piksel-enkel-versterkerdetektor en verskeie-piksels-enkel-versterkerdetektor. Dit was nodig om die werkverrigting van die ruis in die IR-detektor te bepaal vir verskeie topologieë. Ruis beïnvloed die DB sowel as die sensitiwiteit van 'n detektor.

Die resultate wys dat daar 'n unieke skuif in die ontvangerband is vanaf silikondetektors na die IR-band, deur gebruik te maak van die doteringsfunksie van HBTs met germanium. Die skuif is vanaf 'n piek by ongeveer 250 nm na 665 nm toe. Die detektor ontvang nog steeds bestraling in die sigbare band, maar dit vang ook 'n gedeelte van die nabygeleë IR-band op. Dit kan toegeskryf word aan die kleiner bandgapingenergie van silikon met gedoteerde germanium. Hoewel dit nie die optimumstruktuur vir IR-opsporing is nie, motiveer die werk die besluit om die ontvangerband nog verder in die IR band te skuif. Toekomstige werk wat gedoen kan word, is om die beeldsensorstrukture te optimaliseer om die ontvangerband nog verder in die IR-band te skuif, nie slegs gedeeltelik nie.

## ACKNOWLEDGEMENTS

At the top of the list of acknowledgements I would like to thank the Lord for providing the mental and physical strength to conduct and complete this research. I would also like to thank my parents (Ina and John Odendaal), and my sister, Karin Venter, for the continued support and motivation during the entire research period.

I would also like to thank Prof. Saurabh Sinha, Prof. Monuko du Plessis and all the CSIR and ARMSCOR personnel for their willingness to guide, support and assist me in this research despite their busy schedules. Their knowledge support based on years of experience is greatly appreciated.

A very special thanks to Prof. Saurabh Sinha, who is not only an experienced supervisor and researcher, but also a great friend at any time of the day or night, for his assistance and guidance in general with the research. This was not possible without his support.

I would like to thank my postgraduate friends, specifically Nicolaas Fauré, Antonie Alberts and Johny Sebastian, who were willing to support me at all times. Their inputs assisted me a lot in all aspects of the research.

Thanks to all the companies and personnel who assisted in the manufacturing of the prototypes. The companies involved were the foundry ams AG, which prototyped the detector with coordination from Steve Mattheus (Europractice-IC programme); Central Circuits, which fabricated the printed circuit board (PCB) used to mount the package for testing and Avanche-Tech, which soldered the packages to the fabricated PCBs.

A special thanks to Prof. Unil Perera and his research team at Georgia State University (GSU) in Atlanta, United States of America, for allowing me to make use of their specialised equipment to take the required measurements to verify the hypothesis in question. Their inputs are also greatly appreciated. I would also like to thank Keneta Brooks for the administrative tasks concerning the exchange visit to Georgia State University (GSU). Thanks also to the Department of International Relations of the University of Pretoria for funding my travel to GSU.

I would like to thank Armscor, the Armaments Corporation of South Africa Ltd (Act 51 of 2003) for providing a studentship and the Defence, Peace, Safety and Security business unit of the Council for Scientific and Industrial Research for the administration to obtain the grant via the University of Pretoria. Special thanks to Rob Calitz from Armscor for the initial idea and the grant allocation from which this research emanated.

## LIST OF ABBREVIATIONS

ADC	Analogue-to-digital Converter
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
BJT	Bipolar Junction Transistor
CCD	Charged-coupled Device
CDS	Correlated Double Sampling
CMOS	Complementary Metal-oxide Semiconductor
DC	Direct Current
DIP	Dual In-line Package
DR	Dynamic Range
DRC	Design Rule Check
DUT	Device Under Test
FFT	Fast Fourier Transform
FPN	Fixed Pattern Noise
GSU	Georgia State University
HBT	Heterojunction Bipolar Transistor
HIT-Kit	High Performance Interface Tool Kit
IC	Integrated Circuit
I-V	Current-to-voltage
LNA	Low Noise Amplifier
LVS	Layout Versus Schematic
MPW	Multi-project Wafer
MUX	Multiplexer
NMOS	<i>N</i> -channel Metal-oxide Semiconductor
PCB	Printed Circuit Board
PMOS	<i>P</i> -channel Metal-oxide Semiconductor
PPD	Pinned Photo-diode

ppm	Parts per Million
PTAT	Proportional to Absolute Temperature
QE	Quantum Efficiency
QFN	Quad Flat No-lead (package)
SiGe	Silicon Germanium
SNR	Signal-to-noise Ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
TIA	Transimpedance Amplifier
TG	Transmission Gate

# TABLE OF CONTENTS

<b>CHAPTER 1</b>	<b>INTRODUCTION .....</b>	<b>1</b>
1.1	PROBLEM STATEMENT .....	1
1.1.1	Context of the problem .....	1
1.1.2	Research gap .....	2
1.2	RESEARCH OBJECTIVE AND QUESTIONS.....	3
1.3	HYPOTHESIS AND RESEARCH QUESTIONS.....	3
1.4	METHODOLOGY .....	7
1.5	OUTLINE OF STUDY .....	7
1.6	DELIMITATIONS OF THE SCOPE OF THE RESEARCH.....	8
1.7	CONCLUSION .....	9
<b>CHAPTER 2</b>	<b>LITERATURE STUDY .....</b>	<b>10</b>
2.1	INTRODUCTION.....	10
2.2	EVOLUTION OF DETECTOR LAYOUT .....	10
2.3	PUBLISHED METHODS USED TO IMPROVE DYNAMIC RANGE AND SENSITIVITY .....	13
2.4	PHOTODETECTORS .....	15
2.5	SENSOR ARCHITECTURES.....	19
2.6	SENSITIVITY .....	20
2.6.1	Noise in sensitivity of detectors.....	22
2.7	QUANTUM EFFICIENCY .....	23
2.8	DYNAMIC RANGE.....	25
2.9	INTEGRATED CIRCUIT TECHNOLOGY .....	26
2.10	FABRICATION .....	27
2.11	CONCLUSION.....	29
<b>CHAPTER 3</b>	<b>RESEARCH METHODOLOGY .....</b>	<b>30</b>
3.1	INTRODUCTION.....	30
3.2	JUSTIFICATION OF THE METHODOLOGY .....	30
3.3	OUTLINE OF THE METHODOLOGY.....	30
3.4	BICMOS DETECTOR DESIGN METHODOLOGY.....	33
3.5	PERIPHERAL DESIGN .....	34
3.5.1	Overshoot problem.....	34

3.5.2	Clocking .....	34
3.6	MEASURING EQUIPMENT AND SETUP .....	35
3.6.1	Signal analyser .....	35
3.6.2	Monochromator.....	36
3.6.3	Low noise amplifier .....	37
3.6.4	Noise measurement setup .....	38
3.6.5	Sensitivity measurement setup.....	39
3.7	CONCLUSION .....	42
<b>CHAPTER 4 IR DETECTOR DESIGN AND SIMULATION .....</b>		<b>43</b>
4.1	INTRODUCTION.....	43
4.2	OVERALL SYSTEM DESIGN.....	43
4.3	CLOCK CIRCUITRY AND MUX.....	47
4.3.1	Frequency divider .....	48
4.3.2	Multiplexer.....	49
4.3.3	Duty cycle generator .....	50
4.4	PIXEL.....	51
4.5	TIA .....	52
4.6	TRANSMISSION GATE.....	53
4.7	OVERALL CIRCUIT .....	55
4.8	SIMULATIONS .....	56
4.8.1	Duty cycle generator .....	56
4.8.2	Full system .....	57
4.8.3	Noise simulation .....	59
4.8.4	QE .....	61
4.8.5	Sensitivity .....	62
4.9	CONCLUSION .....	64
<b>CHAPTER 5 LAYOUT AND FABRICATION .....</b>		<b>65</b>
5.1	INTRODUCTION.....	65
5.2	LAYOUT TECHNIQUES .....	65
5.2.1	HIT-Kits.....	67
5.2.2	Design Rule Check and Layout versus Schematic .....	67
5.3	LAYOUT OF PIXELS.....	67
5.4	LAYOUT OF PERIPHERAL CIRCUITRY.....	68

5.5	COMPLETE CIRCUIT LAYOUT .....	69
5.6	PLACEMENT ON THE CHIP .....	71
5.7	PACKAGING .....	72
5.8	PCB .....	75
5.8.1	Diode-connected SiGe HBT detector pin outputs .....	75
5.8.2	Actual manufactured PCB .....	76
5.8.3	External connections on the PCB. ....	77
5.9	CONCLUSION .....	77
<b>CHAPTER 6</b>	<b>EXPERIMENTAL RESULTS.....</b>	<b>78</b>
6.1	INTRODUCTION.....	78
6.2	TIME-DOMAIN .....	78
6.2.1	Non-illuminated detector .....	78
6.2.2	Illuminated detector .....	79
6.2.3	HBT I-V .....	80
6.2.4	Sensitivity curve of the HBT .....	80
6.3	NOISE .....	81
6.4	DYNAMIC RANGE .....	82
6.5	SENSITIVITY .....	83
6.6	QE.....	85
6.7	CONCLUSION .....	86
<b>CHAPTER 7</b>	<b>CONCLUSION .....</b>	<b>87</b>
7.1	INTRODUCTION.....	87
7.2	VERIFICATION OF THE HYPOTHESIS.....	87
7.3	SHORTCOMINGS .....	88
7.4	POSSIBLE FUTURE WORK.....	89
<b>REFERENCES</b>	<b>.....</b>	<b>90</b>
<b>APPENDIX A</b>	<b>COEFFICIENTS USED IN SIMULATION .....</b>	<b>96</b>
<b>APPENDIX B</b>	<b>TRANSIMPEDANCE AMPLIFIER DESIGN .....</b>	<b>104</b>
<b>APPENDIX C</b>	<b>DETECTOR READOUT CIRCUIT DESIGN.....</b>	<b>106</b>

# CHAPTER 1 INTRODUCTION

## 1.1 PROBLEM STATEMENT

### 1.1.1 Context of the problem

Charged-coupled device (CCD) technology for the specific application of imaging has been in use for a long time [1] - [5]. The primary reason is that CCD technology is capable of producing high-quality images. The dynamic range (DR) and sensitivity of these detectors are of a very high standard. These infrared (IR) detectors are also characterised by low noise in the image as a result of the almost ideal on-chip switching [3]. Sensitivity and DR are two key components in detector technology. It is a measure of how well a detector can capture images in a given band. Research in the field of detector technology has shown that detectors are capable of achieving high DR and sensitivity with CCD technology. The drawback is that these detectors are costly to manufacture. Recent developments in bipolar complementary metal-oxide semiconductor (BiCMOS) technology with specific application to detectors have shown that BiCMOS detectors are capable of producing the same quality detectors at a fraction of the cost of CCD. BiCMOS detectors showed improvements over CCD detectors because they have lower power consumption, high speed operation, system on-chip integration and lower manufacturing cost [2] - [4]. The introduction of the pinned photodiode aided in the improvement of BiCMOS imaging [4].

Researchers have shifted the focus of detector research to uncooled detectors [6] - [9] primarily owing to running costs, of which cryogenic cooling is one. One feasible material commonly used for uncooled detectors is silicon germanium (SiGe) [10]. Bandwidth, quantum efficiency (QE), saturation power and leakage current parameters are the determining factors of the best structure for a given application [11]. One way to maximise this is to reduce noise in the system. Noise decreases the DR and sensitivity in a system [11]. Some techniques that were used in the past to decrease noise, such as topology changes and other types of detector pixel elements are shown in [4], [12]. These techniques have a direct influence on the fill factor of the detector [6], [12]. The fill factor is a number



of pixels that can be fabricated on a given area. For example, if the size of the pixels increase, given that the prototyping area is kept constant, the number of pixels that can be fabricated will decrease; hence the fill factor will decrease.

With BiCMOS technology, pixels can be prototyped using the heterojunction bipolar transistor (HBT) available with the technology node used in this work. The HBTs were used as a reverse-biased diode-connected transistor, hence forming the photodiode [11]. The added advantage of using HBTs is that the pixel itself will provide some gain, overcoming noise issues with the pixels and producing better current flow. Compared to conventional photodiodes, illuminated diode-connected HBTs produce more current, which inherently exhibits a larger signal-to-noise ratio (SNR).

Some techniques that were used to improve DR were the use of current mode communication [13], signal DR extension [14] and mercury cadmium telluride (HgCdTe) material [11]. It is obvious that several different techniques exist to improve DR and sensitivity, but only one technique, namely noise reduction, was used in this research to improve both the DR and sensitivity. For both DR and sensitivity, a common factor is the output voltage swing. The minimum output voltage swing, when no radiation is present, is the noise content that is present, to which there are several contributors. The larger the noise, the less output voltage swing can be obtained which inhibits both DR and sensitivity.

### **1.1.2 Research gap**

The gap in the body of knowledge of detectors is that noise is a major problem for on-chip switching. Another problem is that IR detectors are difficult to realise by using conventional silicon CMOS technology because of the larger Si bandgap. These two factors deteriorate the DR and sensitivity performance of these detectors significantly. There is no ideal solution to this problem but there have been efforts to reduce noise. Among others, efforts to reduce noise have been presented in literature by changing the pixel circuit topology and pixel structures.

The research gap that this work addresses is reduction of switching noise, which will be a step in the direction of improving the overall performance of BiCMOS IR detectors over CCD IR detectors. Another research gap addressed is to determine if IR detectors can be realised in BiCMOS technology.

## 1.2 RESEARCH OBJECTIVE AND QUESTIONS

The primary objective of this research is to match or improve the DR and sensitivity of IR detectors by using BiCMOS technology instead of using CCD technology and by using pixel readout circuitry with comparable noise performance. The driving force behind this objective is the cost of manufacturing and ease of fabrication and integration of such detectors with other technologies.

From this objective, the following research questions arise:

- What limits or degrades the performance of BiCMOS sensors in terms of DR and sensitivity?
  - How can this limitation be reduced?
    - Determine a suitable readout topology (single pixels or grouped)
  - How can post-processing be used to improve IR detectors?
  - How can SiGe BiCMOS technology be used to realise a detector in the IR band?

## 1.3 HYPOTHESIS AND RESEARCH QUESTIONS

The proposed detector research can be specified in the following research hypothesis:

*If SiGe BiCMOS technology can be used as a detector in the near-IR band, then the DR and sensitivity of these detectors could be improved in a similar value to CCD IR detectors.*

The DR of a detector is the ratio of the pixel saturation level to the signal threshold and the sensitivity is the amount of photon current produced per watt of optical power. The primary inhibitors of these parameters are noise.

A  $2 \times 2$  pixel BiCMOS detector was proposed, realised and tested in the  $0.35 \mu\text{m}$  SiGe technology node. A  $2 \times 2$  pixel BiCMOS detector was chosen for the following reasons:

- The DR and sensitivity of a complete IR detector are dependent on the size and shape of the pixel element and not the number of pixels in the IR detector. This applies to CCD detectors as well.

Although the number of pixels is small, the contribution of this research is outlined below:

- SiGe HBT pixels can detect radiation in the IR band, although the detecting band only detects partial radiation in the near-IR band.
- This shift resulted in improvement in DR and sensitivity in the IR band compared to conventional BiCMOS detectors. Detectors in the IR band can be realised in BiCMOS technology.

Table I compares this work with other previously published research on IR detectors.

TABLE I  
COMPARISON OF OTHER PUBLISHED WORK WITH THIS WORK - CMOS

Reference	[9] 2008	[16] 2010	[17] 2008	[18] 2010	[19] 2011	This work
Technology node	$0.35 \mu\text{m}$ CMOS	$0.18 \mu\text{m}$ CMOS	$0.18 \mu\text{m}$ CMOS	$0.13 \mu\text{m}$ CMOS	$0.13 \mu\text{m}$ CMOS	$0.35 \mu\text{m}$ BiCMOS
Array size	$128 \times 128$	-	$64 \times 64$	-	-	$2 \times 2$
Pixel size	$40 \mu\text{m} \times$ $40 \mu\text{m}$	-	$30 \mu\text{m} \times$ $30 \mu\text{m}$	-	-	$6.6 \mu\text{m} \times$ $11 \mu\text{m}$
Pixel area	-	$60 \times 60 \mu\text{m}^2$	-	-	-	-
Chip size	$6.5 \text{ mm} \times$ $6.5 \text{ mm}$	-	$3 \text{ mm} \times$ $3 \text{ mm}$	-	-	$1.3 \text{ mm} \times$ $1.3 \text{ mm}$

Reference	[9] 2008	[16] 2010	[17] 2008	[18] 2010	[19] 2011	This work
Noise	0.76 $\mu\text{V}/\sqrt{\text{Hz}}$	72 $\mu\text{V}/\sqrt{\text{Hz}}$	-	-	50 $\text{nV}/\sqrt{\text{Hz}}$	2 $\mu\text{V}/\sqrt{\text{Hz}}$
DR	-	-	54 dB	47 dB	-	66 dB
Sensitivity	4.97 kV/W	0.1 A/W	2.75 kV/W	26.8 mV/dB	5 kV/W	180 kV/W or 180 mA/W
Power consumption	-	23.4 mW	125 mW	0.1 mW	-	10 mW

Table I shows how this work fits in with the current body of knowledge. The low power consumption can be attributed to the low component count. The pixels themselves do not dissipate a lot of power and therefore the consumption is primarily that of the peripheral circuitry. The noise performance is comparable to that of conventional CMOS detectors. DR and sensitivity values are usually given at the peak of the detecting bandwidth. The prototyped detector not only showed the capability of detecting radiation in the near-IR band, but also an increase in both DR and sensitivity compared to other detectors. This is due to the decrease in base resistance the Ge doping introduces into the pixel elements.

Table I only compares this work to work on other CMOS IR detectors previously published. Table II compares this IR detector to its CCD counterpart.

TABLE II  
 COMPARISON OF OTHER PUBLISHED WORK WITH THIS WORK - CCD

Reference	C9016 <sup>1</sup>	C9546 <sup>1</sup>	C9547 <sup>1</sup>	C7700 <sup>1</sup>	This work
Suffix	23	03	04	-	-
Detecting material	Multialkali	Multialkali	Multialkali	Multialkali	SiGe
Sensitivity	53 mA/W	53 mA/W	47 mA/W	-	180 mA/W
$\lambda_{PEAK}$	430 nm	430 nm	430 nm	450 nm	670 nm
DR	-	-	-	65 dB	70 dB
Quantum efficiency	15 %	15 %	14 %	-	30 %
Spectral response	185 - 900 nm	185 - 900 nm	185 - 900 nm	200 - 900 nm	500 -1100 nm
Power consumption	4.8 W	6 W	8 W	100 W	10 mW

Table II compares the IR detector prototyped in this research to its CCD equivalent. A noticeable shift to the IR band is observed with this IR detector. This IR detector also exhibits an improvement in DR, sensitivity and QE. A significant reduction in power consumption was recorded.

<sup>1</sup> <http://sales.hamamatsu.com>

## 1.4 METHODOLOGY

The proposed approach to conduct this research is as follows:

At first, a thorough literature study will be conducted to distinguish the difference between CCD and BiCMOS sensors. The literature survey will be extended to pinpoint methods used to improve the DR and sensitivity. Simulations will be conducted on methods separately and the same methods will be combined and simulated. The results will be compared to those of CCD sensors to verify the improvement. The proposed method will be evaluated experimentally with an implementation of the sensor in the ams AG 0.35  $\mu\text{m}$  SiGe process. The results obtained from experimental measurements will be compared to those of the simulations to verify the improvement over CCD and answer the research questions stated.

## 1.5 OUTLINE OF STUDY

The research is documented as follows:

- Chapter 1: Introduction  
This chapter introduces the research and a summary of the problems associated with BiCMOS detectors. The hypothesis, goals and contribution of this research are also given.
- Chapter 2: Literature review  
The most relevant literature needed to understand the significance of this research is reviewed in this chapter. The chapter is divided into four distinct sections, namely detector layout, methods to improve DR and sensitivity, sensor architecture and DR and sensitivity characteristics. Through a thorough study of these sections, a gap in the body of knowledge was noticed and as a result this research was conducted.
- Chapter 3: Research methodology  
This chapter describes the methodology used to complete this research. A description of the software used to develop a functional prototype is discussed briefly. An overview of the equipment needed to perform the required measurements and to obtain the necessary results is given.

- Chapter 4: Detector design and simulations

The design resulting from the mathematical derivation of the detector is outlined in this chapter. The chapter is divided into three main sections, namely clock circuitry, pixels and readout circuitry. Two detectors were designed, namely the single-pixel-single-amplifier detector and the multiple-pixel-single-amplifier detector. The purpose of this is to cancel out the effects of different technology nodes, such as different parasitic capacitances and doping levels. Two different pixel elements were used as well to verify the shift to the IR band. Time domain simulations of different parts of the detector, as well as overall simulations, are given to illustrate the inner workings of the detector. Noise simulations at the output of both detectors are also given to show the noise reduction and resulting DR and sensitivity. DR and sensitivity simulations were also performed to compare the silicon p-i-n diode with the diode-connected SiGe HBT.

- Chapter 5: Layout and fabrication

In this chapter, some issues regarding layout and the effect they have on this research are documented. Separate subsystem layouts, as well as the final layout, including dimensions, are given. A description of the package used for this research, as well as a bonding diagram, is included. The printed circuit board (PCB) used to mount the package and to perform the required measurements is given.

- Chapter 6: Experimental results

The time domain measurements, as well as noise measurements for the entire band of interest, are given for the prototype detector in this chapter.

- Chapter 7: Conclusion

This chapter concludes the research and critically evaluates the findings and the hypothesis. Possible further research suggested by this work is also documented.

## **1.6 DELIMITATIONS OF THE SCOPE OF THE RESEARCH**

Several detectors have been implemented in literature. Several different techniques are available to improve DR and sensitivity, but this research will be limited to noise reduction techniques, specifically to reduce on-chip switching noise. Noise is a large inhibitor of the performance of DR and sensitivity. The concept described in this work can be directly

applied to larger detectors (in terms of number of pixels) without affecting the DR and sensitivity, therefore only a few pixels will be implemented in this research. Because of the limited number of signal generators available at GSU, reset noise could not be measured and therefore the reset pin was tied to  $V_{DD}$  to avoid this problem. The resulting noise content will be lower, but since a detector will not be constantly reset, the reset noise content will not affect the outcome of this research significantly.

Oscillators can be divided into two main types, internal or external. Internal oscillators require some die area and have to be implemented using the process parameters of the technology node used. External oscillators are readily available with adequate performance. This work does not focus on the oscillator design and therefore it is limited to external oscillators only.

Several pixel structures exist in literature. This research is limited to typical structures that can be prototyped with the said process's components without breaking design rules. Future research can be conducted on other pixel structures optimised for IR radiation, but design rules may not hold as other structures are prototyped.

The peripheral circuitry makes use of High Performance Interface Tool Kits (HIT-Kits), since the research is not focused upon the peripheral circuitry, yet it is required in the implementation of the prototype integrated circuit (IC).

## 1.7 CONCLUSION

This chapter provided a summary of the research that was conducted to improve the performance of BiCMOS IR detectors. A brief description of the process used to validate the hypothesis and answer the research questions is also provided in this chapter.



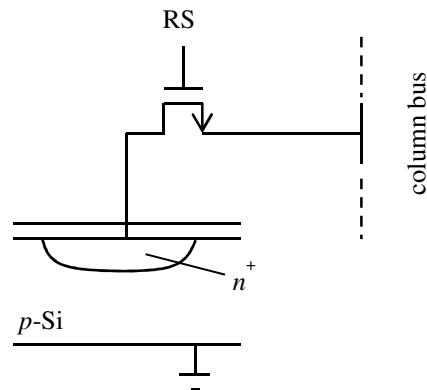
# CHAPTER 2 LITERATURE STUDY

## 2.1 INTRODUCTION

In this chapter, the most important literature needed to understand the fundamentals of IR detectors is summarised. Some methods used in the past to improve DR and sensitivity are included.

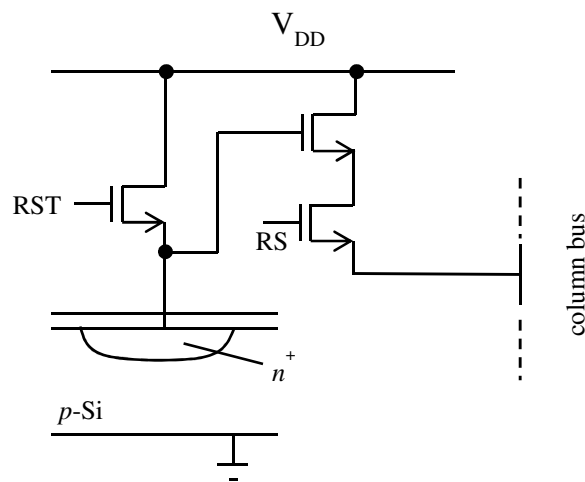
## 2.2 EVOLUTION OF DETECTOR LAYOUT

Because of the stringent requirement of DR and sensitivity of detectors, simply reducing the pixel size and pixel pitch will be a feasible solution to increase DR and sensitivity, up to a point where reducing the pixel size even further will degrade the DR and sensitivity of detectors [8]. The motivation for this is that the sensitivity of detectors is directly proportional to the size of the pixel transistor, as well as the analogue-to-digital converter (ADC) resolution required and memory needed [10]. This implies that the smaller the transistor size, the less the amount of current that can be generated. There is also a relationship between this decrease in size and the DR. As the fabrication technology of the transistor improves, the maximum saturation voltage decreases. This is due to switching noise from neighbouring components. The best structure of a pixel for a given application depends on various factors, such as bandwidth, QE, saturation power, linearity, ease of integration and leakage current [10]. Different techniques have been developed in the past to overcome these limitations, which are summarised in this dissertation. Fig. 2.2.1 depicts the passive CMOS pixel structure.



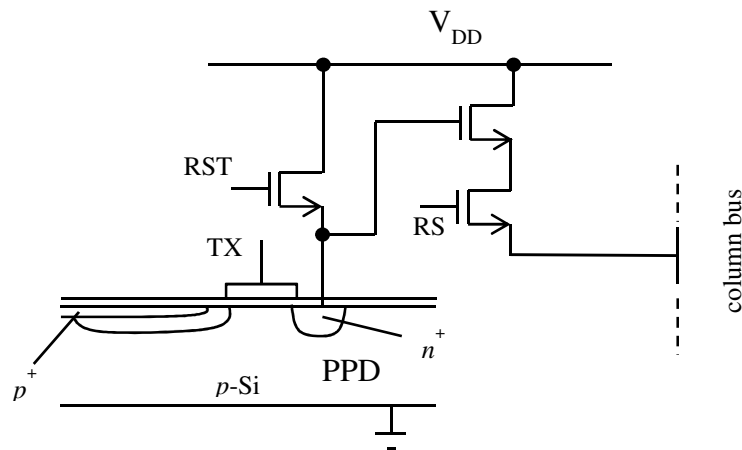
**Figure 2.2.1** Passive CMOS pixel structure [12] © [2007] IEEE

The advantage of the passive CMOS structure described in Fig. 2.2.1 is that a large overall fill factor (the number of pixels that can be fabricated on a single chip) is obtained. The fill factor does not affect the DR and sensitivity but it affects the size of the pixel. The disadvantage is that because of the fill factor, a considerable amount of noise is generated owing to the mismatch between neighbouring pixel capacitances and large vertical bus capacitances. There is a trade-off between the fill factor and the amount of switching noise present. The detector depicted by [9] exhibits low noise but with a fill factor of 44 %. The following subsections detail alternative techniques to reduce noise. The active pixel concept, which is illustrated in Fig. 2.2.2, is one such technique [12].



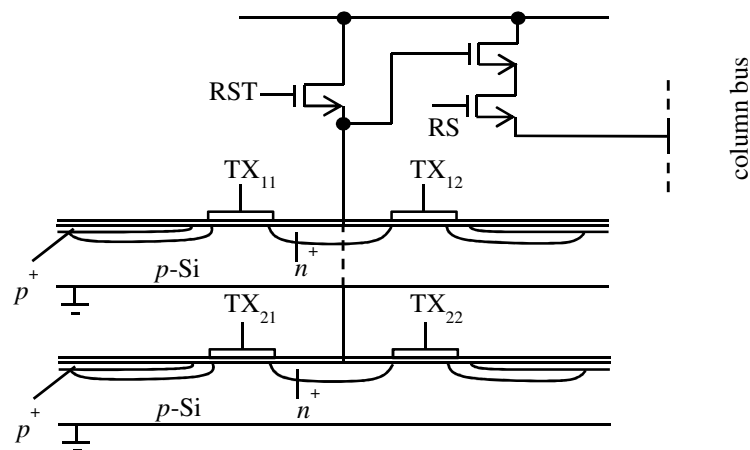
**Figure 2.2.2** Active CMOS pixel structure [12] © [2007] IEEE

As shown in Fig. 2.2.2, every pixel has its own current amplifier, which is a source follower. This greatly reduces noise in the sensor but it comes at a price. The fill factor is not as high as the passive pixel structure because fewer pixels can be fabricated owing to the extra active devices on the sensor. The only drawback of this structure is that it makes use of a reset photodiode, which generates thermal noise. To reduce this noise, the pinned photo-diode (PPD) concept was introduced, as shown in Fig. 2.2.3 [12].



**Figure 2.2.3** Active pixel structure with pinned photodiode [12] © [2007] IEEE

In the structure depicted in Fig. 2.2.3, the inclusion of the PPD exhibits a few advantages. The first is that with the use of correlated double sampling (CDS), kTC noise is almost completely eliminated [4], [12]. The second advantage is that the CDS has a positive influence on the  $1/f$  noise of the system. The kTC noise in the photodiode itself is zero. The disadvantage of this structure is that the size of the PPD is large. This greatly reduces the number of pixels that can be fabricated on a chip. However, with an approach like the shared pixel concept as shown in Fig. 2.2.4, the same size pixels can be fabricated, but with less pixel circuitry [4], [12].



**Figure 2.2.4** Shared pixel structure based on active pixel structure with pinned photodiode

[4] © [2006] IFIP, [12] © [2007] IEEE

A set of  $2 \times 2$  pixels share the same output amplifier and reset transistor, as described in Fig. 2.2.4. This effectively reduces the number of components in the in-pixel circuitry by four; hence a larger fill factor can be obtained in comparison to the active pixel structure with pinned photodiode. The drawback is that because no two components can ever be exactly the same because of manufacturing deviations, fixed pattern noise (FPN) is introduced in the sensor. This can be corrected with image-processing techniques in software [23], [24] and in hardware ([25] - [27]).

By using clocked comparators in the ADC architecture, noise can be reduced significantly [10]. This also reduces power consumption.

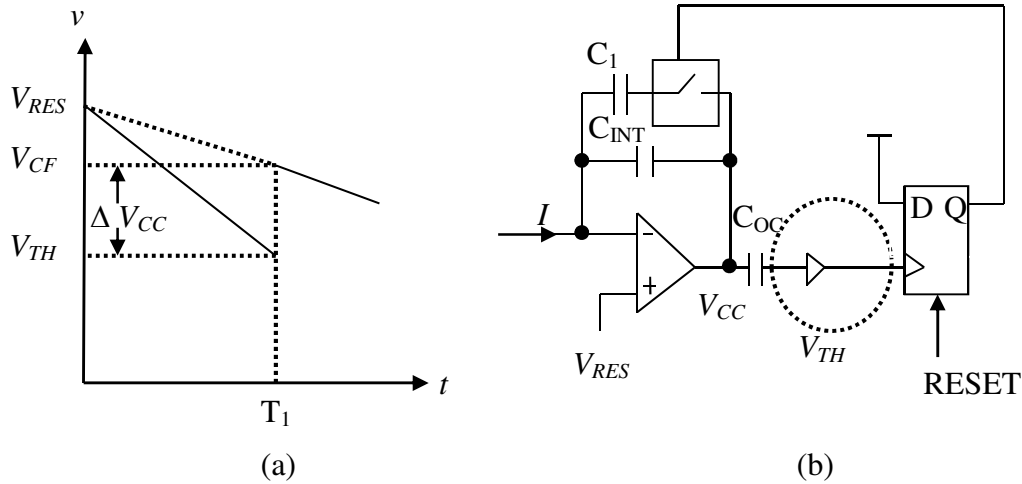
### **2.3 PUBLISHED METHODS USED TO IMPROVE DYNAMIC RANGE AND SENSITIVITY**

A test chip with a DR of 16 bits is depicted in [15]. It makes use of the charge balancing technique, which consists of counting the charge packets. By controlling the least significant bit of the ADC with the aid of floating point coding, further improvements to the DR of the detector were made. The final measured results yielded a DR of 19 bits, as well as a reduction in technology fluctuations between two different pixels.

A different technique to improve DR is described in [13]. This technique makes use of current mode communication, which entails the inclusion of a current buffer as an input stage. This enhances the DR owing to the better signal received.

Because of stringent requirements of speed and short integration times, detectors need to be 100 times more sensitive and respond 10 000 times faster than conventional thermal detectors. The sensitivity criterion is met by using an avalanche gain of 150 in the HgCdTe photodiodes and CMOS multiplexer. The required speed is met by having pixel level gating circuits to switch the detector on and off. Typical integration times of gated detectors should be less than a microsecond to achieve the required speeds.

A sensor with an auto-ranging circuit included, which boosts the sensor DR by 19 dB, is described in [14]. Further improvements are made by the signal DR extension technique. Fig. 2.3.1 depicts this technique graphically.



**Figure 2.3.1 (a)** Graphical representation of the technique signal DR extension (adapted from [14]) © [2007] IEEE

**Figure 2.3.1 (b)** Corresponding circuit diagram (adapted from [19]) © [2007] IEEE

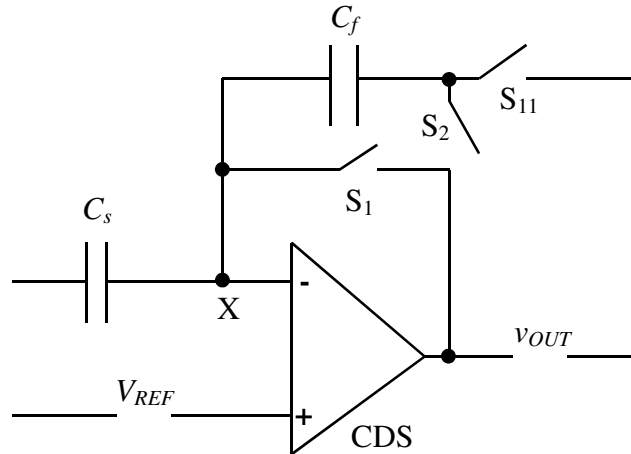
The signal DR extension technique shown in Fig. 2.3.1 makes use of automatic selection of the integrating capacitance in output circuits to boost the sensor DR.  $V_{CF}$  is related to the other parameters given in (2.3.1).

$$V_{CF} = V_{RES} \frac{C_1}{C_{INT} + C_1} + V_{TH} \frac{C_{INT}}{C_{INT} + C_1} \quad (2.3.1)$$

The selection of capacitance is based on a given set of conditions to maximise the DR. This requires prior knowledge of conditions and output DR, but the system is capable of adjusting the capacitance to produce the largest DR possible.

There are three main readout techniques in modern detectors, namely direct injection, current mirror integration and capacitor transimpedance amplification [20]. Direct injection is not widely used because of an integration increase when the voltage signal range is wide. This reduces the speed of the detector. Current mirror integration occurs where metal-oxide semiconductor (MOS) transistors are biased in the sub-threshold region. This technique has an improved DR but the disadvantage is that the structure has unstable and

inaccurate detection capabilities. The last technique in this category is the capacitor transimpedance amplifier technique shown in Fig 2.3.2.



**Figure 2.3.2** Capacitive transimpedance amplifier circuit diagram (adapted from [20])

© [2009] IEEE

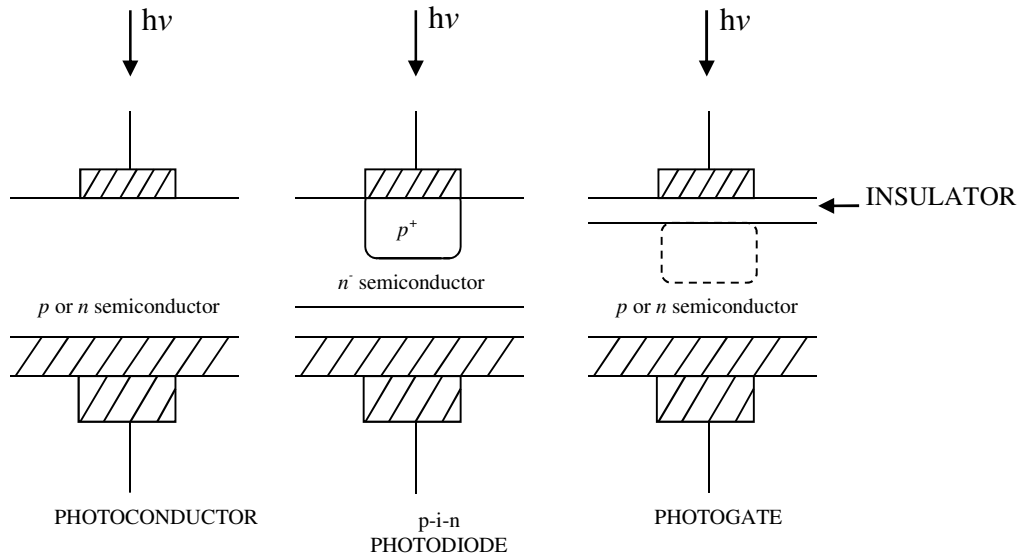
The capacitor transimpedance amplifier shown in Fig. 2.3.2 has good integration capabilities and linearity, together with a wide DR. This is due to the capability of selecting the integration capacitors.

As can be seen from the techniques presented in this section, to increase the DR and sensitivity of a sensor, some decision on the trade-offs has to be made. Most of the trade-offs are the different types of noise that are introduced into the system. To eliminate one type of noise, such as kTC noise or photon shot noise, another type of noise is introduced. This is the trade-off that has to be taken into consideration.

## 2.4 PHOTODETECTORS

A photodetector is a solid-state detector that converts incoming light energy to electrical energy [11]. Different semi-conductor photodetectors exist. Examples of these detectors are silicon, germanium and indium Gallium Arsenide. Each of the existing photodetectors exhibits unique properties of which the frequency band, in which the detector absorbs energy, is the most important. Theoretically there are 2 600 types of photodetectors, of which 100 types have been demonstrated in the past [11]. The three most common types of

photodetectors are the photoconductor, the p-i-n photodiode and the photogate. Fig. 2.4.1 describes the structure of these detectors.



**Figure 2.4.1** Three most common structures of photodetectors [11] Optical Society of America, (Michael Bass et al), Handbook of Optics Vol 1 2E © 1995 McGraw-Hill, reproduced with Permission of the McGraw-Hill Companies.

Fig. 2.4.1 describes the construction of the three most common types of detectors. For this research, the p-i-n photodiode was used to compare to the SiGe HBT based detectors. Photodetectors are classified according to their response time, QE and sensitivity [11].

Different types of material exhibit different operating conditions, of which wavelength and operating temperature are the main factors. Table III summarises the most commonly used materials for photodetectors.

TABLE III

SUMMARY OF THE MOST COMMONLY USED MATERIALS IN PHOTODETECTORS [11]

Type	$E_G$ (eV)	$\lambda_c$ (nm)	Band
Silicon	1.12	1100	Visible
Gallium Arsenide	1.42	875	Visible
Germanium	0.66	1800	Short-wavelength- infrared
Indium Gallium Arsenide	0.73 – 0.47	1700-2600	Short-wavelength- infrared
Indium Arsenide	0.36	3400	Medium- wavelength-infrared
Indium Antimonide	0.17	5700	Medium-wavelength infrared
Mercury Cadmium	0.7-0.1	1700-12500	Short-wavelength to long-wavelength infrared

The band gap energy ( $E_G$ ) is indirectly proportional to the wavelength of the detector. The relationship of the band gap energy and the cutoff wavelength ( $\lambda_c$ ) is given by (2.4.1).

$$\lambda_c = \frac{1.24 \times 10^3 \text{ nm}}{E_G(\text{eV})} \quad (2.4.1)$$

In the application of gated IR imaging, the typical operational temperatures of detectors are carefully controlled. Some detector materials have to be cooled to below room temperature with methods such as cryogenic cooling, since thermal agitation occurs at lower temperatures, where noise is also decreased. Table IV summarises the typical operating temperatures for different detector materials.



TABLE IV  
 TYPICAL OPERATING TEMPERATURES AND OPTIMAL DETECTING WAVELENGTH FOR  
 DIFFERENT MATERIALS [21] [22]

Detector	T (K) (typical operation)	$\lambda_{MAX}$ ( $\mu\text{m}$ )
Germanium	193	1.9
Silicon	300	1.1
Gallium arsenide	300	0.9
Cadmium selenide	300	0.69
Cadmium sulphide	300	0.52
Indium gallium arsenide	300	0.9-1.7
Mercury cadmium telluride	77-195	1 – 12
Indium antimonide	10-77	0.6 – 5.5

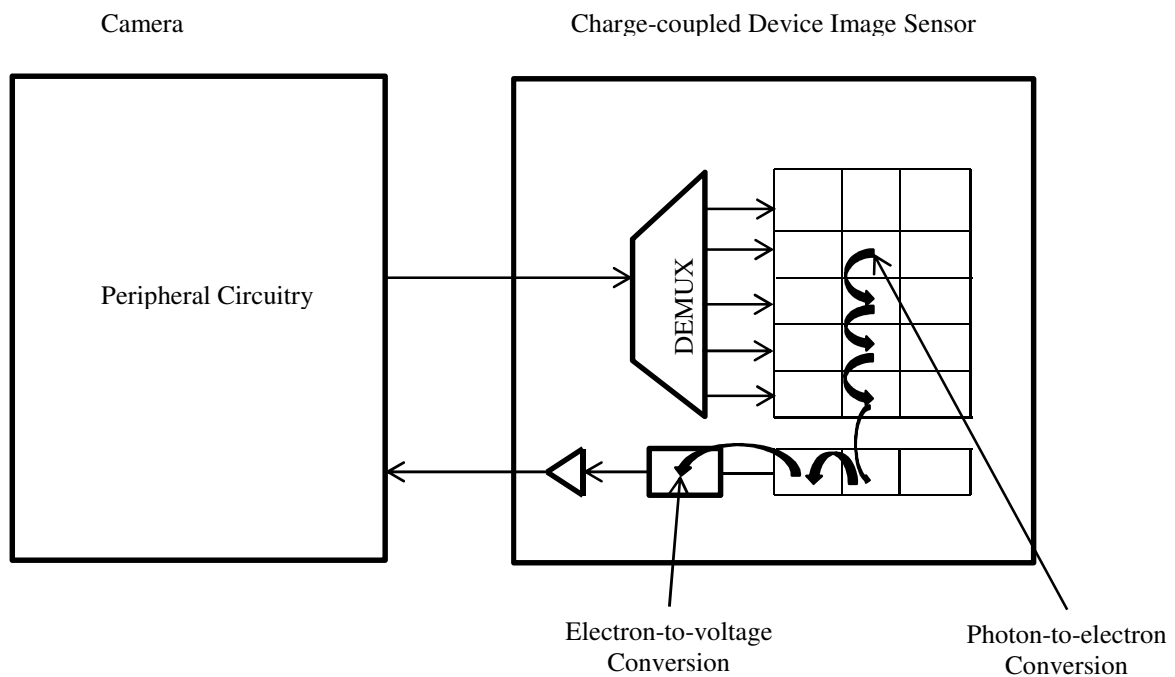
According to Table IV, silicon, gallium arsenide, cadmium selenide, cadmium sulphide and indium gallium arsenide do not require any cooling and as a result make the typical operational cost less expensive. Gallium nitride and aluminium gallium nitride detectors do not require any cooling either [28]. The antenna-coupled detector of [33] reduces the operational cost, as expensive cooling is omitted. However, the fabricating cost is still expensive. Mercury cadmium telluride (HgCdTe) has a wider bandwidth than most other materials, but it has to be operated at below room temperature. This material has to be cryogenically cooled, which escalates the operational cost compared to other materials.

Uncooled IR detectors have captured the interest of researchers working in fields relating to imaging in view of their low cost, low mass and low power in comparison to photon detectors [6] - [9]. Uncooled HgCdTe semiconductor detectors optimised for the mid-IR band range have a subnanosecond response time [32]. The problem with SiGe detectors is that they have a slower response time compared to HgCdTe detectors. Improvements in

uncooled image detection have been made by using mesoporous silica instead of pure silicon [31].

## 2.5 SENSOR ARCHITECTURES

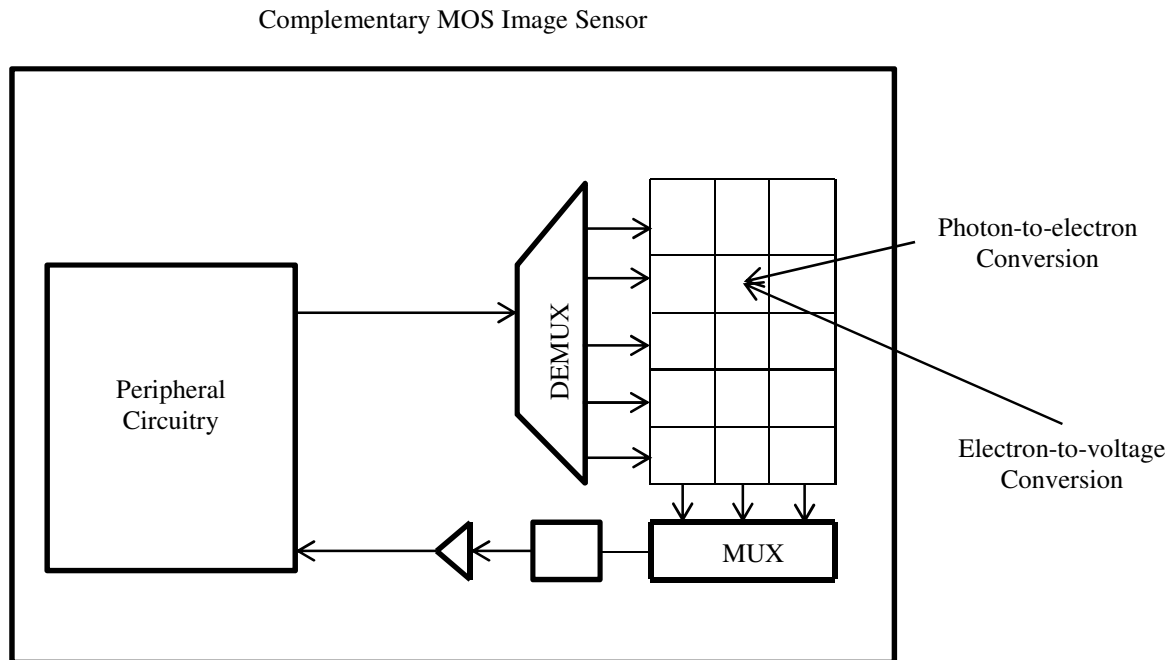
A CCD is a matrix of MOS devices operated in depletion mode. MOS capacitors are also widely used in CCDs [36]. The method of operation in a CCD sensor is to move the packets of charge at or near the surface of the silicon physically from the pixel to the output, where the charge is converted into a voltage or current signal [34]. The conversion process takes place off the chip with the aid of external circuitry. This operation can be explained in more detail using Fig. 2.5.1.



**Figure 2.5.1** CCD sensor concept (adapted from [36]) © [2001] D. Litwiller

As shown in Fig. 2.5.1, the captured photon is physically moved from the array to the external circuitry before it is converted to an electron and eventually a voltage. The number of on-chip components is reduced, which in turn decreases the amount of switching on the chip. The result of this reduced amount of switching is a significant reduction in noise. The disadvantage of CCD sensors is the cost of manufacturing the sensor.

A CMOS sensor also comprises an array of MOS devices [36]. The fundamental difference is that the charge-to-voltage conversion process takes place on the chip [34], whereas with CCD it takes place off the chip. Fig. 2.5.2 depicts the operation mode of a CMOS sensor.



**Figure 2.5.2** CMOS sensor concept (detection of visible photons) (adapted from [36]) © [2001] D. Litwiller

A CMOS sensor comprises an array of identical pixels, each having at least a sensing element and an addressing transistor [36]. It also consists of an  $X$ -addressing and  $Y$ -addressing register to address every single pixel individually. The last component is the output amplifier. The whole process of photon-electron-to-voltage conversion takes place on the chip. This makes the cost of developing sensors cheaper, since the materials used are less expensive. The disadvantage, however, is that the amount of noise increases as the number of active components on the chip increases.

## 2.6 SENSITIVITY

Sensitivity is the amount of photocurrent produced by the optical power of a given wavelength [36]. It is measured in amperes per watts (A/W). The sensitivity of a detector is limited by noise currents. Different techniques exist to improve light sensitivity, of which

examples are dedicated manufacturing processes with a limited number of metal layers or thin interconnect layers with thin dielectrics. Another technique makes use of back-side illumination. The Teager Energy Operator [35] provides improved sensitivity.

The aim of all techniques given in section 2.3 is to experiment with different operating environments. Thus the sensitivity can be improved for a given resolution only. To increase the resolution while simultaneously keeping the sensitivity the same, alternative techniques need to be considered.

The photon-generated current ( $i_{PH}$ ) is related to the invasive optical power ( $P_i$ ) by (2.6.1) [37], [38], [46]:

$$i_{PH} = \frac{q}{h\nu} P_i (1 - e^{-\alpha_s w}) (1 - R_f) \quad (2.6.1)$$

where  $\alpha_s$  is the absorption coefficient,  $w$  is the width of the undoped region (in the case of a p-i-n diode) or the width of the base (in the case of an (HBT)) and  $R_f$  is the reflection coefficient defined by the (2.6.2):

$$R_f = \frac{(n - 1)^2 + k^2}{(n + 1)^2 + k^2} \quad (2.6.2)$$

where  $n$  is the refractive index (different values for different radiating wavelengths) and  $k$  is the extinction coefficient defined by (2.6.3):

$$k = \frac{\alpha\lambda}{4\pi}. \quad (2.6.3)$$

The value of  $\lambda$  is defined in (2.4.1). This defines the sensitivity of the pixels and not the detector. The final output sensitivity of a detector is given by (2.6.4):

$$R_{out} = SNR * R_{pixel} \quad (2.6.4)$$

where  $SNR$  is defined by (2.6.5) [37]:

$$SNR_{dB} = \frac{(i_{PH} + i_{DC})^2}{q (i_{PH} + i_{DC}) \tau_{INT} + q^2 (\sigma_{read}^2 + \sigma_{DNSU}^2) + (\sigma_{PRNU} i_{PH} \tau_{INT})^2}. \quad (2.6.5)$$

In (2.6.5),  $i_{PH}$  is the photon-generated current,  $i_{DC}$  is the dark current present,  $\tau_{INT}$  is the integration time,  $\sigma_{read}^2$  is the detector noise,  $\sigma_{DNSU}^2$  is the dark signal non-uniformity noise and  $\sigma_{PRNU}^2$  is the gain FPN.

Practical sensitivity calculations can be done with (2.6.6) [11]:

$$R = \frac{S}{P \times A} \quad (2.6.6)$$

where  $S$  is the signal output of the detector (V or A),  $P$  is the incident radiation intensity ( $W/cm^2$ ) and  $A$  is the sensitive area of the detector ( $cm^2$ ).

### 2.6.1 Noise in sensitivity of detectors

Rearranging the Beert-Lambert law for absorption, the absorption coefficient is given by

$$\alpha = - \frac{\ln\left(\frac{I}{I_o}\right)}{z} \quad (2.6.1.1)$$

where  $\alpha$  is the absorption coefficient ( $cm^{-1}$ ),  $I$  is the light intensity measured after incidence has occurred ( $W/cm^2$ ),  $I_o$  is the light intensity of the original beam ( $W/cm^2$ ) and  $z$  is the distance after the material at which the light intensity is measured (cm). As seen in (2.6.1.1), if the measured light intensity drops, then the absorption coefficient decreases logarithmically given that the distance at which the intensity is measured stays constant.

The inverse of the absorption coefficient is also the distance at which the light intensity is reduced to  $1/e^-$  (~ 36 %) of its original intensity.

When an indirect semiconductor is radiated by waves which exhibit radiation energy larger than the bandgap energy of the material, then the absorption coefficient is related to bandgap energy by (2.6.1.2).

$$\alpha(E) = \alpha_0 \left(\frac{E-E_g}{E_g}\right)^2 \quad (2.6.1.2)$$

This is then related to the photon generated current by (2.6.1.1)

With (2.6.1.2) it is assumed that no noise is present in the system. Since this is not possible in practice, (2.6.1.1) is modified to accommodate noise by adding a noise current parameter with the invasive optical power.

$$i_{PH} = \frac{q}{h\nu} P_i (1 - e^{-\alpha_{sw}}) (1 - R_f) + i_{NOISE} \quad (2.6.1.3)$$

As it can be seen, if noise dominates the system, then a large amount of optical generated current needs to be produced to be able to measure significant photon generated current. There are several contributors to noise ranging from shot noise to flicker noise.

## 2.7 QUANTUM EFFICIENCY

QE is a measure of the conversion quality of incoming photons into conduction electrons. The quality of images produced is directly related to the QE. It is not, however, the only factor, as noise induced in the sensor degrades the SNR, which in turn degrades the quality of the images. The QE of a detector is given in (2.7.1) [11].

$$QE(\eta) = \frac{1240 \text{ Sens}(A/W)}{\lambda} \quad (2.7.1)$$

where the generated current (A) is given in (2.7.2)

$$A = A_0 e^{-\alpha x} \quad (2.7.2)$$

where  $A_0$  is the incident photon flux,  $\alpha$  is a function of the wavelength in use and  $x$  is the depth in the silicon wafer.

$$\eta = K(1 - R) \frac{\Gamma \alpha_{IB}}{\alpha} (1 - e^{-\alpha l}) \quad (2.7.3)$$

where  $\eta$  is the efficiency determined by the absorption coefficient

$K$  is the coupling efficiency due to modal mismatch,

$\Gamma$  is the mode confinement factor,

$\alpha_{IB}$  is the interband absorption,

$\alpha$  is the loss coefficient and

$l$  is the distance of the object from the sensor.

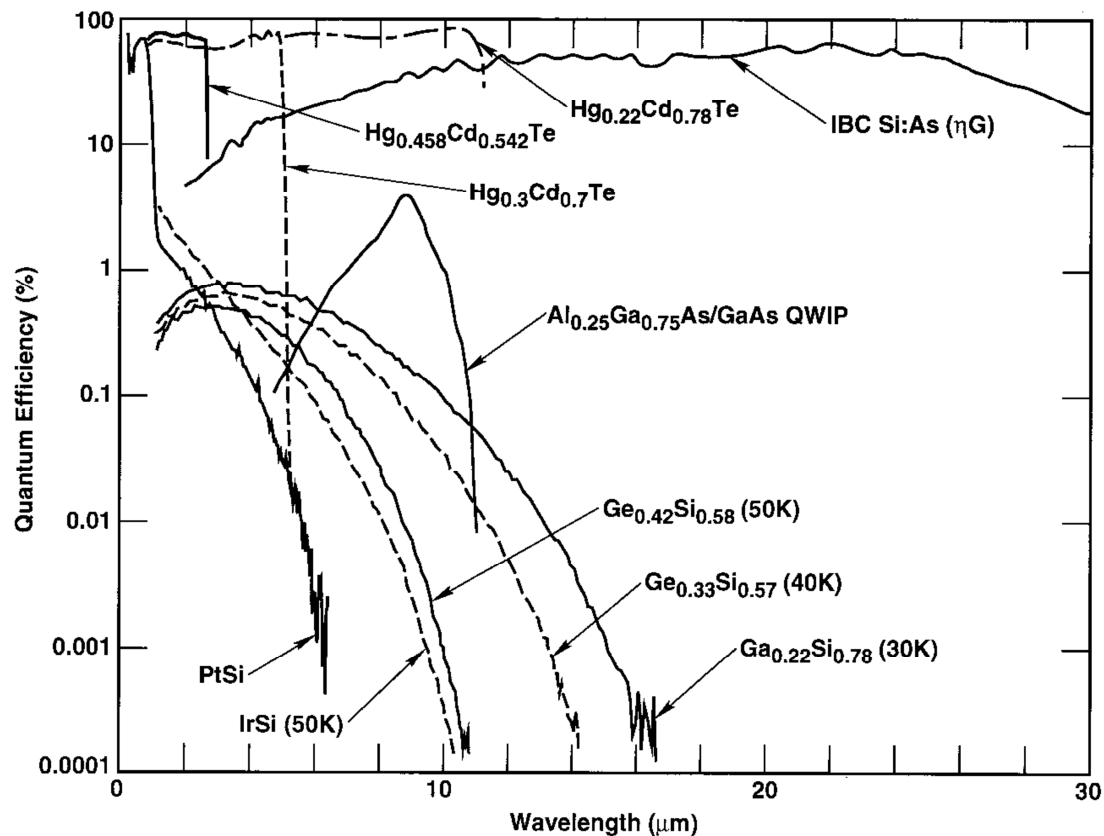
The value of  $\alpha$  is defined by (2.7.4).

$$\alpha = \Gamma \alpha_{IB} + \Gamma \alpha_{FC} + (1 - \Gamma) \alpha_{FCx} + \alpha_s \quad (2.7.4)$$

where  $\alpha_{FC}$ ,  $\alpha_{FCx}$  are the free carrier absorption loss inside and outside the absorption layer and  $\alpha_s$  is the scattering loss.

In quantum well IR detectors, the detectable wavelengths can be modified by changing the quantum well thickness of the barrier heights [30]. Single-photon detectors, however, can only detect wavelengths in the X-ray, ultraviolet, visible and near-IR range [39]. Since the frequency where IR detection takes place is in the THz range, quantum dot detectors can be a feasible solution, but the cost of fabrication can be a problem [40]. Detection of IR beams in SiGe quantum dot detectors is possible [40].

To decide which material would be sufficient for use in a given application, quantum efficiencies are compared with one another. The most important factor that was taken into consideration, together with QE, is the cost of fabrication. Fig. 2.7.1 describes the QE versus wavelength for different detector materials.



**Figure 2.7.1** QE versus wavelength for different materials [11] © [1995] McGraw-Hill

Historically HgCdTe photo detectors have been more popular than photovoltaic detectors [11], [21]. This is due to production capabilities and cost, even though photovoltaic detectors exhibit higher QE, higher detectivity and superior modulation transfer function.

The main problem of HgCdTe photo detectors is the cost of fabrication. In this dissertation, SiGe was used to evaluate the proposed hypothesis. It is evident from Fig. 2.7.1 that SiGe has an acceptable QE at smaller wavelengths and is thus more suitable for BiCMOS IR imaging.

## 2.8 DYNAMIC RANGE

The DR of a sensor used for imaging is defined as the ratio of the pixel saturation level to its signal threshold [11]. It is measured in bits or as a ratio (also in dB). The pixel size and DR are related by (2.8.1).

$$PS \propto DR^2 \quad (2.8.1)$$

where  $PS$  is the pixel size and  $DR$  is the DR of the sensor. Because of this relation, sensors are being developed for a specific frequency range, to maximise the DR for a particular application rather than to develop sensors with a greater DR in a wider frequency band. The latter would produce bulky sensors.

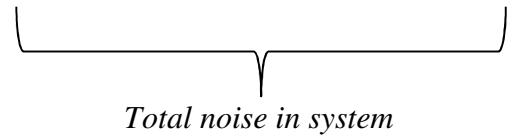
DR is related to noise by (2.8.2) [37]:

$$DR_{dB} = 20 \log \frac{q Q_{well} - i_{DC} \tau_{INT}}{\sqrt{q i_{DC} \tau_{INT} + q^2 (\sigma_{read}^2 + \sigma_{DSNU}^2)}} \quad (2.8.2)$$

where  $Q_{well}$  is the well capacity just before the detector saturates,  $q$  is the charge of an electron ( $1.6 \times 10^{-19}$  C),  $i_{DC}$  is the dark current present,  $\tau_{INT}$  is the integration time,  $\sigma_{read}^2$  is the detector noise and  $\sigma_{DSNU}^2$  is the dark signal non-uniformity noise.

Practically, DR can be calculated using (2.8.3) [41]:

$$DR = \frac{V_{MAX} - V_{DARK}}{\sqrt{V_{NOISE_{DARK}}^2 + 2 \frac{kT}{\alpha q} G_{CPH} + \frac{V_{READOUT_{NOISE}}^2}{A_{TOT}^2}}} \quad (2.8.3)$$


  
 Total noise in system

where  $V_{MAX}$  is the maximum output voltage of the IR detector,

$V_{DARK}$  is the dark voltage output,



$V_{NOISE\_DARK}^2$  is the dark noise voltage,

$k$  is Boltzmann's constant,

$T$  is the temperature (K),

$\alpha$  is a coefficient between 1 and 2.  $\alpha \approx 1$  in hard reset mode and  $\alpha \approx 2$  in soft reset,

$q$  is the charge of an electron,

$G_{C\_PH}$  is the conversion gain of the reset transistor,

$V_{READOUT\_NOISE}^2$  is the readout noise of the detector and

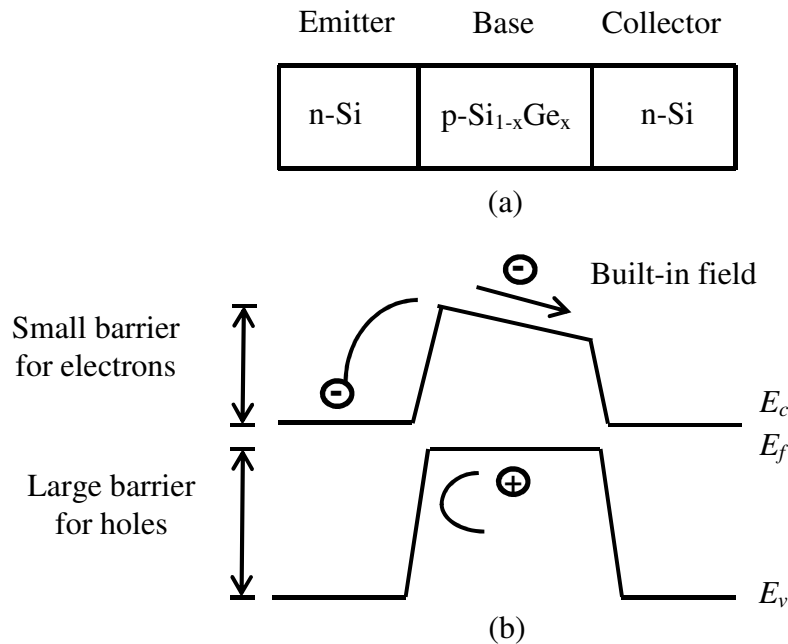
$A_{TOT}$  is the readout circuit gain.

The second term in the denominator is generally considered as the reset noise associated with the detector. Three practical measurements need to be taken in order to compute the DR of an IR detector. The first is the noise of the system when fully operational. This will be the complete numerator in (2.8.3). The second is the voltage output when the system receives no illumination and the third is the voltage output when the system receives illumination. Appropriate de-embedding is needed to obtain accurate values.

## 2.9 INTEGRATED CIRCUIT TECHNOLOGY

Taking into consideration all the necessary requirements and limitations, of which speed and noise are dominant, a suitable material has to be chosen to satisfy the requirements. Of all the available materials, SiGe fulfils most of the criteria, including manufacturing cost. Throughout the past few years, the production cost of SiGe devices has decreased while the capabilities, such as gain, have increased owing to the high common-emitter gain feature, which also aided in the popularity of these devices [33], [42]. Homo-junction detectors are capable of detecting a wide range of wavelengths in the IR band, but are slower compared to hetero-junction detectors.

With the use of HBTs, even more stable sensors can be fabricated because of their low noise capabilities, lower base resistance, high gain and high operating frequency capacity. This increases the carrier mobility of *p*-channel MOS (PMOS) transistors [43]. Fig. 2.9.1 describes the HBT.



**Figure 2.9.1.** Principle of the SiGe HBT: (a) structure, (b) energy band diagram [43]

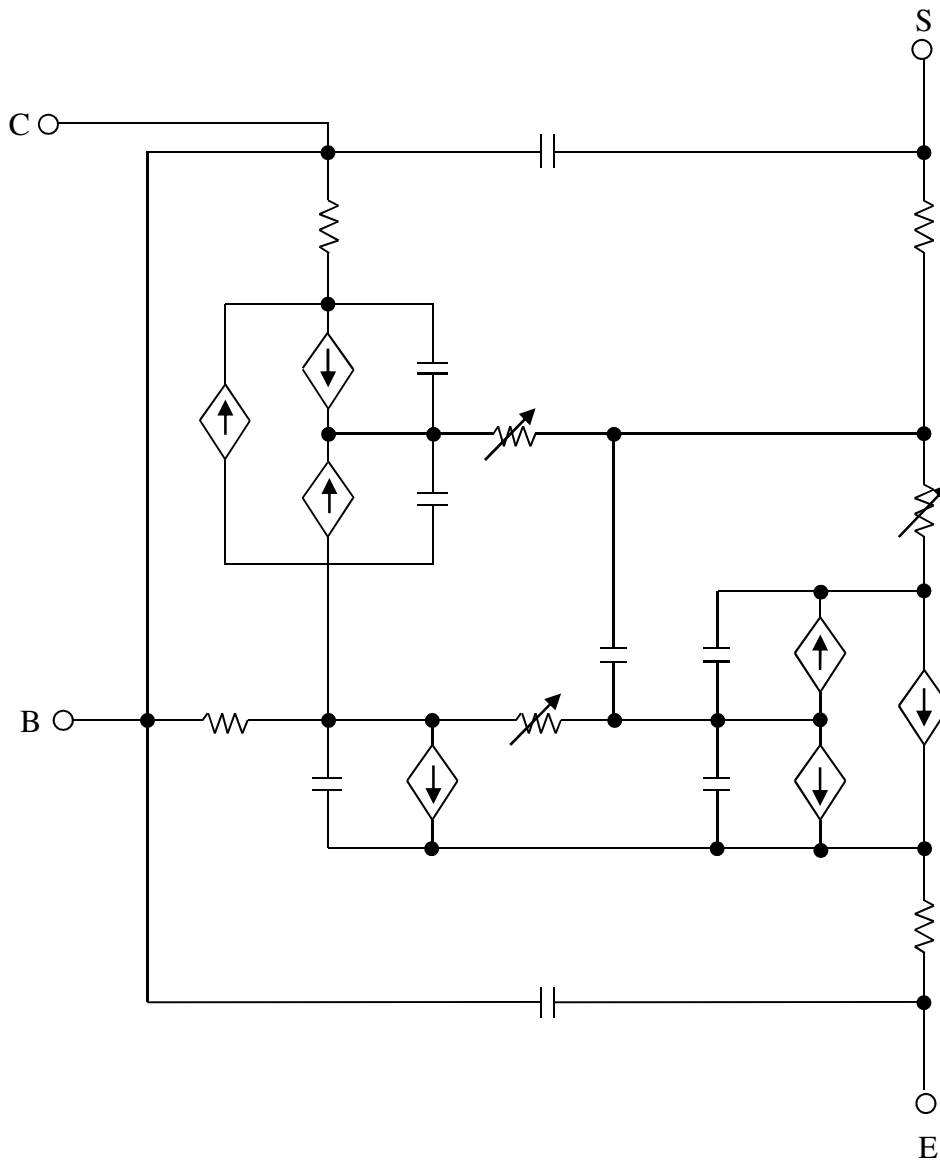
© [2004] IEEE

Fig. 2.9.1 describes the hetero-junction bipolar transistor. The fundamental difference between this transistor and the normal bipolar transistor is that the base is doped with germanium in addition to the *p*-type silicon diffusion.

## 2.10 FABRICATION

Simulation Program with Integrated Circuit Emphasis (SPICE) will be used to verify the functionality of the IC after extensive evaluation has been conducted, before sending it off for fabrication. The fabrication of the IC and the measured results will be compared to the theoretical simulations to validate the hypothesis in question. Since the cost of fabrication is high, this is a critical step in the verification process. The model proposed by [44] was

used for manual calculations. This, however, does not include parasitic elements present in the transistor. Fig. 2.10.1 depicts the VBIC95 model [45].



**Figure 2.10.1** Extract of the VBIC95 model of the bipolar junction transistor (BJT) used for SPICE simulations [45] © [1996] IEEE

Fig. 2.10.1 illustrates the model that is used by SPICE. It includes parasitic parameters not used in manual calculations. The inclusion of the parasitic parameters predicts the behaviour of the transistor. However, manually calculated results can be simulated directly with SPICE with minimal deviations in the calculated results; hence the VBIC95 model and the simplified model [44] will be sufficient for this research.

## 2.11 CONCLUSION

This chapter outlined the literature needed to understand the research conducted in this dissertation. Methods published were briefly discussed to outline the importance of this work. The theories behind the practical measurements of sensitivity, DR and quantum efficiency were discussed. Several types of detectors and their architectures were discussed.

# CHAPTER 3 RESEARCH METHODOLOGY

## 3.1 INTRODUCTION

This chapter outlines the methodology used in this research. It includes all the necessary steps used to verify the hypothesis in question. Information on both the simulators and the equipment used to measure all the necessary quantities are included in this chapter.

## 3.2 JUSTIFICATION OF THE METHODOLOGY

Various detectors have been implemented and are documented in chapter 2. Simulators, such as Cadence Virtuoso, provide only approximate results to the real working prototype. The simulators use models to predict the behaviour of components in software versus the actual behaviour.

To model IR radiation in simulation, an ideal current source is needed in the schematic design. Again, this is only an approximation of the radiation received in view of the imperfect nature of components and other unaccounted effects.

A prototype IC is needed in order to verify the hypothesis in question. The prototype package was mounted on a PCB to enable easy testing and the IC was wire-bonded to the package.

## 3.3 OUTLINE OF THE METHODOLOGY

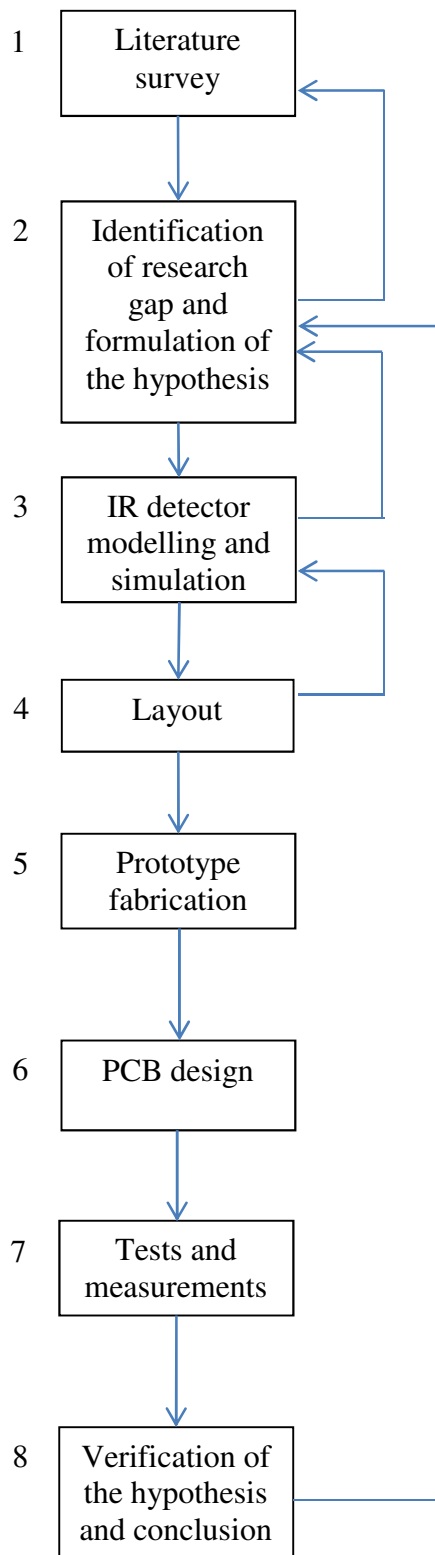
To verify the hypothesis in question, a systematic method was followed to accomplish this with conclusive results. The following list describes the procedures followed in this verification:

- *Theoretical background* – A literature study was conducted to highlight the important factors in previous IR detectors discussed in publications. Several trade-offs were found and incorporated accordingly in the implementation of the prototyped IC for this research.
- *Mathematical design* – Some design equations emanated from the literature study conducted, which were then used to implement this detector. This was needed so

that the detector would be able to function properly under given process specifications. These equations include the design of the clock circuitry, multiplexer (MUX) and transimpedance amplifier (TIA). Some other design equations include the equations to calculate the resulting DR and sensitivity from the noise values obtained, as well as equations used to calculate the DR and sensitivity from experimental measurements.

- *Software-aided design* – The simulation tool Cadence Virtuoso was used to implement the proposed design in software so that testing could be done before the low-level IC was designed.
- *Transistor-level IC design* – The prototype detector layout was done in the 0.35  $\mu\text{m}$  SiGe ams AG process. This design was done with the aid of Cadence Layout GXL.

To conduct research where a prototype IC is needed, an iterative process is followed. Fig. 3.3.1 depicts the flowchart that describes this process graphically.

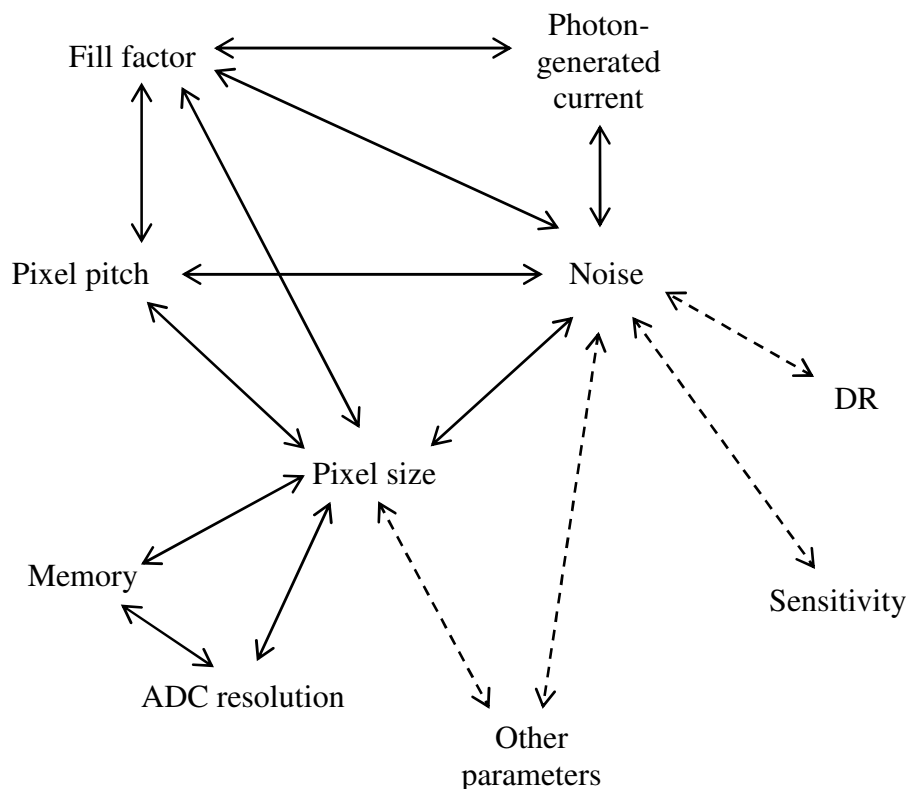


**Figure 3.3.1** Graphical representation of the research methodology

Fig. 3.3.1 shows the methodology that was followed in this research. After a literature survey had been conducted, the research gap was identified and the hypothesis was formulated. After the formulation of the hypothesis, the IR detector was modelled and simulated in software. If there was a flaw in the results or some critical component or parameter was missing, the literature study was reviewed and extended where necessary. Further modelling and simulation were done in the light of the reviewed literature. Much the same iterative method was followed with procedure 4. When the layout was complete, the process continued until the final testing occurred and the hypothesis could be verified.

### 3.4 BICMOS DETECTOR DESIGN METHODOLOGY

The design of BiCMOS detectors constitutes a multi-dimensional design problem where more than one parameter can have an effect on another parameter. There is no set way of designing these detectors, therefore the trade-offs have to be taken into account carefully. Fig 3.4.1 illustrates this problem.



**Figure 3.4.1** Graphical representation of the multidimensional design problem



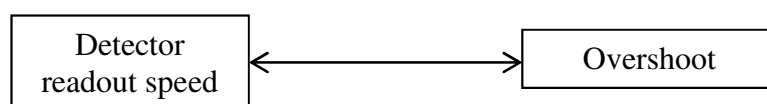
Fig. 3.4.1 shows how the different technical parameters are interlinked in the design of an IR detector. The solid lines indicate the physical parameters, whereas the dashed lines indicate the resulting performance parameters. For instance, an increase in fill factor increases the on-chip noise. This degrades the DR of the detector. However, an increase in the fill factor cannot directly decrease the DR.

One possibility to decrease the amount of noise in an IR detector is to decrease the number of pixel groups. This should decrease the noise component. A decrease in noise exhibits an increase in DR and sensitivity. The amount of increase is not the same in both cases. The number of groups is directly linked to the number of pixels in the detector. Through the literature study conducted in chapter 2, it is possible to decrease the number of groups, while keeping the number of pixels the same. The advantage of this is that the amount of noise is decreased in the system, which in turn increases the DR and sensitivity. The disadvantage of this is that the fill factor will decrease.

### 3.5 PERIPHERAL DESIGN

#### 3.5.1 Overshoot problem

The mathematical design of the detector involves getting the timing right. One trade-off that comes with it is explained in Fig. 3.5.1.



**Figure 3.5.1** Performance trade-off

Fig. 3.5.1 shows that if the detector readout speed is increased, larger unwanted overshoot will be observed at the output. This is due to a spurt of charge that is released as soon as the “switch” is turned on.

#### 3.5.2 Clocking

Since all detectors make use of some kind of MUX to perform the parallel-to-serial conversion, precise clocking is required to ensure that all the data are read out in a clocked

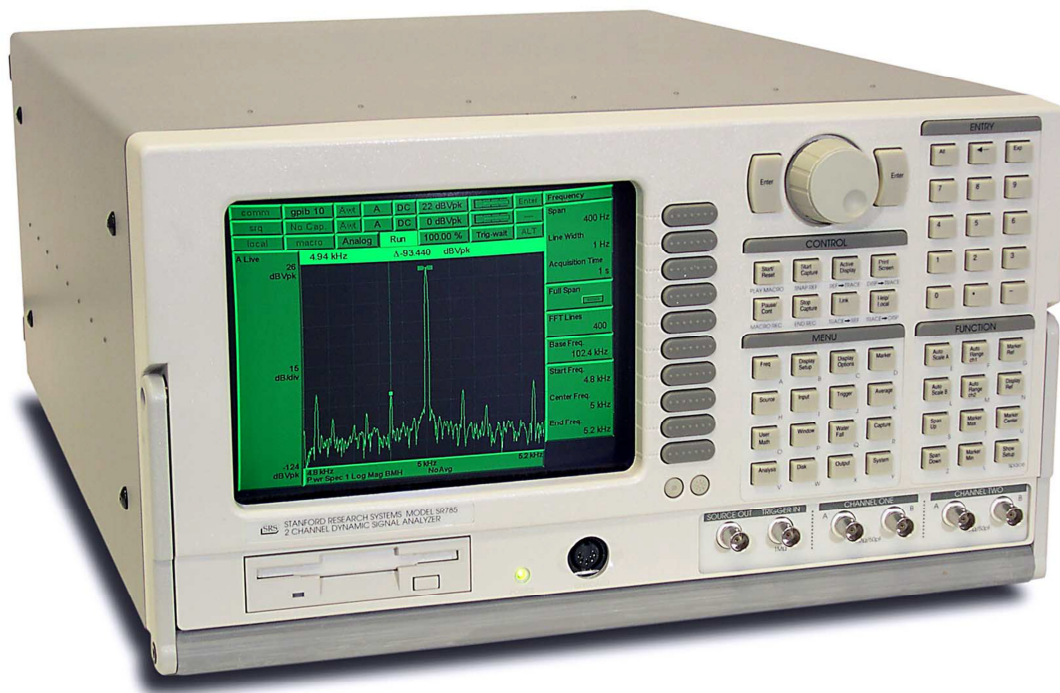
manner. From this, the base clock is derived from the cycle time. This will be explained in more detail in chapter 4.

### 3.6 MEASURING EQUIPMENT AND SETUP

As seen from the literature study in chapter 2, two quantities needed to be measured practically. Firstly, the output noise needed to be measured for all the noise calculations. Secondly, the sensitivity of the detectors in dark and illuminated conditions was needed.

#### 3.6.1 Signal analyser

To perform the noise measurements, the signal analyser model SR785 from Stanford Research Systems<sup>2</sup> was used. The signal analyser is shown in Fig. 3.6.1.1.



**Figure 3.6.1.1** Stanford Research Systems SR785 signal analyser

The SR785 signal analyser shown in Fig. 3.6.1.1 can measure noise up to 102 kHz with an accuracy of 25 parts per million (ppm) from 20 °C to 40 °C. The fast Fourier transform

<sup>2</sup> <http://www.thinksrs.com/products/SR785.htm>

(FFT) spans from 195.3 mHz to 102.4 kHz with a resolution up to 800 lines. A DR of 80 dB is guaranteed with a harmonic distortion of less than -80 dB. The amplitude accuracy of the SR785 analyser is 0.2 dB. The specifications allow for accurate noise measurements in practical circumstances.

### 3.6.2 Monochromator

The DK 480 ½ metre monochromator from Digikröm<sup>3</sup> was used for two reasons. The first was to perform a complete sweep of radiation of the band of interest, which is from 500 nm to 1500 nm, which covers most of the near-IR band. There are other gratings available, which can produce radiation in other bands, but this was not done since it was determined beforehand that this detector will never detect radiation in those bands. This was determined by analysing the expected band gap of the detector used. The second was to illuminate the IR detector with a preselected radiation wavelength and to measure the resulting noise spectra. The DK 480 ½ metre monochromator is shown in Fig. 3.6.2.1.



**Figure 3.6.2.1** Digikröm DK 480 ½ metre monochromator

<sup>3</sup> <http://www.tec-sol.com/products/optic/spectrlprdct/dk480.pdf>

Fig. 3.6.2.1 shows the DK 480 ½ metre monochromator that was used. It exhibits a focal length of 480 mm. The wavelength precision and accuracy are 0.007 nm and 0.3 nm with a 1 200 g/mm grating. The maximum resolution of the monochromator is 0.03 nm and it has a scan speed of 1 - 1200 nm/min.

### 3.6.3 Low noise amplifier

The low noise amplifier (LNA) was needed to amplify the small voltage signals so that the signal analyser and monochromator could measure the voltage signals accurately. The gain that the LNA adds was divided in software to produce an accurate representation of the actual voltage signals. The Stanford Systems SR560 LNA<sup>4</sup> used in the measurements is shown in Fig. 3.6.3.1.



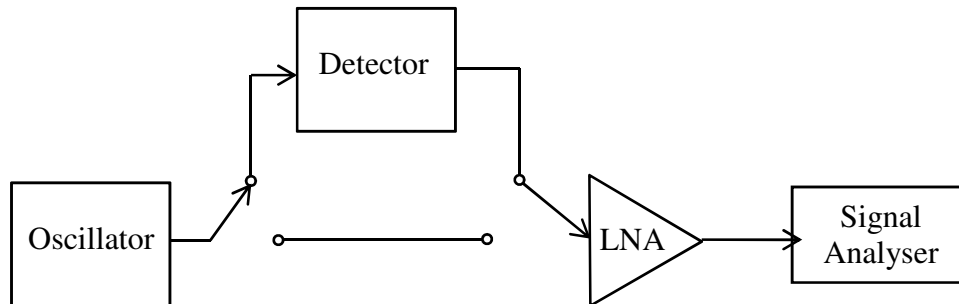
**Figure 3.6.3.1** Stanford Systems SR 560 LNA

Fig. 3.6.3.1 shows the SR 560 LNA used in this research. It exhibits a 4 nV/Hz<sup>1/2</sup> input noise with a 1 MHz bandwidth. The voltage gain is configurable from 1 to 50 000 V/V gain. It exhibits configurable signal filters to filter out certain unwanted signals. The LNA comes with a battery pack, which eliminates the normal AC supply noise voltage spikes when used in battery mode.

<sup>4</sup> <http://www.thinksrs.com/products/SR560.htm>

### 3.6.4 Noise measurement setup

A de-embedding technique was used to measure the noise of the IR detector only. Fig. 3.6.4.1 shows the block diagram of this setup.



**Figure 3.6.4.1** Noise measurement setup

Fig. 3.6.4.1 shows the setup that was used to perform the noise measurements. The noise results were de-embedded to obtain the voltage noise of the IR detector only. The values were subtracted in software to obtain the IR detector voltage noise only. The IR detector voltage noise was first measured with no illumination and then measured with illumination. The illumination was radiated on to the IR detector from the monochromator. The objective of this test was to measure the output noise of the detector under different radiating conditions. The tests, procedure and acceptance criteria of the detector for noise measurements are described in Table V.

TABLE V

THE TEST AND EXPERIMENTAL PROCEDURE FOR THE IR DETECTOR NOISE MEASUREMENTS

Objective	Procedure	Acceptance criteria
Basic noise test: In this test the peripheral circuitry noise measurements in a dark room was obtained which was needed for the one part of the de-embedding process.	Using an oscillator a 2 V square wave input was required at the input. The output was connected to a signal analyser and the results were obtained.	The measured noise should be more than the inherent noise of the cables and measuring equipment which combined should be higher than $6 \text{ pV}/\sqrt{\text{Hz}}$ .
Full system dark room noise test: In this test the noise measurements of the detector in a	A bias voltage of 1.7 V was required at the biasing MOS transistor. A 2 V square wave	The measured noise should be more than the inherent noise of the cables and the measuring

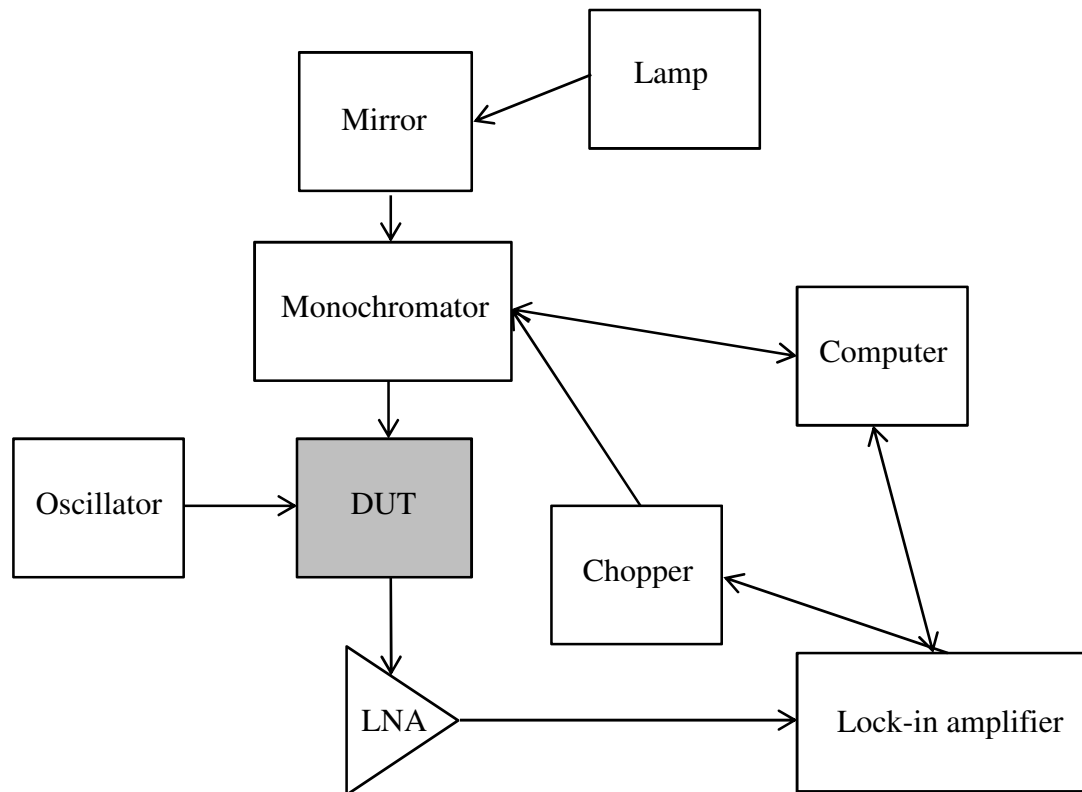
dark room was obtained to complete the noise de-embedding process. input clock was required with the output connected to a signal analyser, and then the results were obtained. equipment which combined should be higher than  $6 \text{ pV}/\sqrt{\text{Hz}}$  plus the noise of the peripheral circuitry noise value in the basic noise test.

Full system detector noise test under illumination: The noise measurements of the detector under illumination were obtained. A bias voltage of 1.7 V was required at the biasing MOS transistor. A 2 V square wave input clock is required with varying incident radiating wavelengths in the IR band. The output was connected to a signal analyser then the results were obtained. The expected noise performance should be the same as that of the dark room test since illumination has no effect on the noise performance.

The measurement procedures described in Table V provide detailed information on how to obtain the correct noise measurements for this detector. This is needed to verify the readout noise reduction, which will improve the DR and sensitivity of BiCMOS IR detectors as shown in (2.6.5) and (2.8.3).

### 3.6.5 Sensitivity measurement setup

Fig. 3.6.5.1 shows the setup or flow that was used to measure the sensitivity.



**Figure 3.6.5.1** Sensitivity measurement setup

Fig. 3.6.5.1 shows the setup that was used to measure the sensitivity of the IR detector. The detector is denoted as the device under test (DUT). The lamp of the system is interchangeable for radiation in different bands. This radiation is reflected from the mirror at an angle to create different radiating wavelengths. This is then passed to the monochromator through a rotating wheel with holes to allow the radiation to fall onto the detector through the slits and break it periodically. The chopper frequency is usually selected at a frequency that does not fall onto the 60 Hz where power supply noise will affect the results. A frequency of 37 Hz was selected owing to the fast response of the SiGe HBTs. The output of the IR detector was fed to the LNA and then fed to the lock-in amplifier. This amplifier tries to lock the output frequency of measurements with the pre-set chopper frequency. The lock-in amplifier also feeds the results to the computer, where these are saved. The computer then feeds the monochromator and chopper module with the pre-set settings.



The objective of this test was to measure the sensitivity of the detector under different radiating conditions. The tests, procedure and acceptance criteria of the detector for sensitivity measurements are described in Table VI.

TABLE VI  
THE TEST AND EXPERIMENTAL PROCEDURE FOR THE IR DETECTOR SENSITIVITY  
MEASUREMENTS

Objective	Procedure	Acceptance criteria
Dark room sensitivity test: Sensitivity measurements of the IR detector in a dark room were obtained with this test. This was needed to verify that the detector in the sensitivity test was indeed responding under illumination.	A bias voltage of 1.7 V was required at the biasing MOS transistor. The detector setup used is described in Fig. 3.6.5.1. in a dark room with a square wave input clock of 2 V applied. The results were then obtained.	The system should produce raw data which can be attributed to noise. A flat response should be observed.
Full system sensitivity test: Sensitivity measurements of the IR detector under IR illumination were obtained with this test.	A bias voltage 1.7 V was required at the biasing MOS transistor. The detector setup used is described in Fig. 3.6.5.1 under varying IR illumination with a square wave input clock of 2 V applied. The results were then obtained.	The system should produce raw data that take on an RC shaped curve. This indicates that the detector is responding as expected. A flat response indicates noise.
Second harmonics test: With this test it was verified whether the second rise in sensitivity is a real response or just second order harmonics under IR illumination.	A bias voltage of 1.7 V was required at the biasing MOS transistor. The detector should be set up as described in Fig. 3.6.5.1 under varying IR illumination with a square wave input clock of 2 V applied. A radiation filter, which filters out any radiation below 1 $\mu\text{m}$ wavelength, was added over the detector and verification was done.	A flat response should be obtained, indicating that the system is indeed measuring harmonics.



The procedure described in Table VI gives detail on how to perform the sensitivity measurements and the acceptance criteria. Using these results, the resulting DR can be calculated as described in section 2.8.

### **3.7 CONCLUSION**

In this chapter the research methodology used to verify the hypothesis in question was explained. The outline of the methodology was given, along with information regarding the modelling, implementation, fabrication and testing of the IR detector.

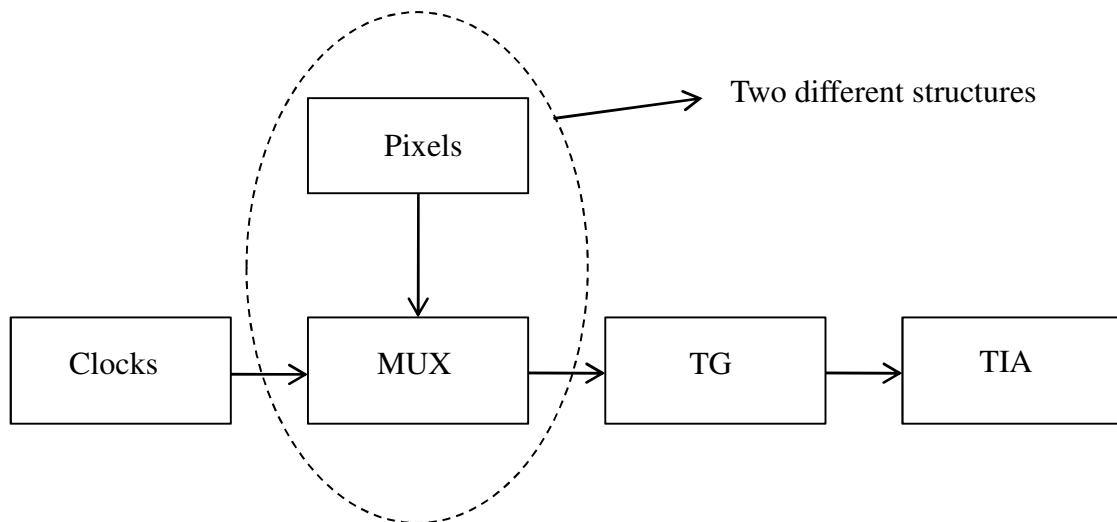
# CHAPTER 4 IR DETECTOR DESIGN AND SIMULATION

## 4.1 INTRODUCTION

In this chapter, the mathematical design underlying the research is explained. Research in the field of microelectronic engineering examines design components as part of the experimental verification of the hypothesis. Two detectors were designed on the same wafer, so that process variations and parasitic capacitances would not play a significant role in the results, since they would be the same.

## 4.2 OVERALL SYSTEM DESIGN

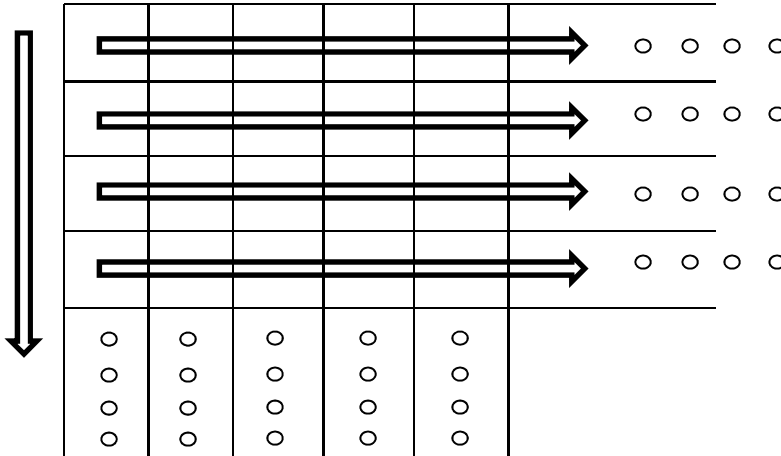
Typical detectors exhibit four distinct subsystems, each with its individual design constraints. Several different features can be added to the detectors, but the fundamental concept remains the same. Fig. 4.2.1 depicts the design of a typical IR detector.



**Figure 4.2.1** Overall system design

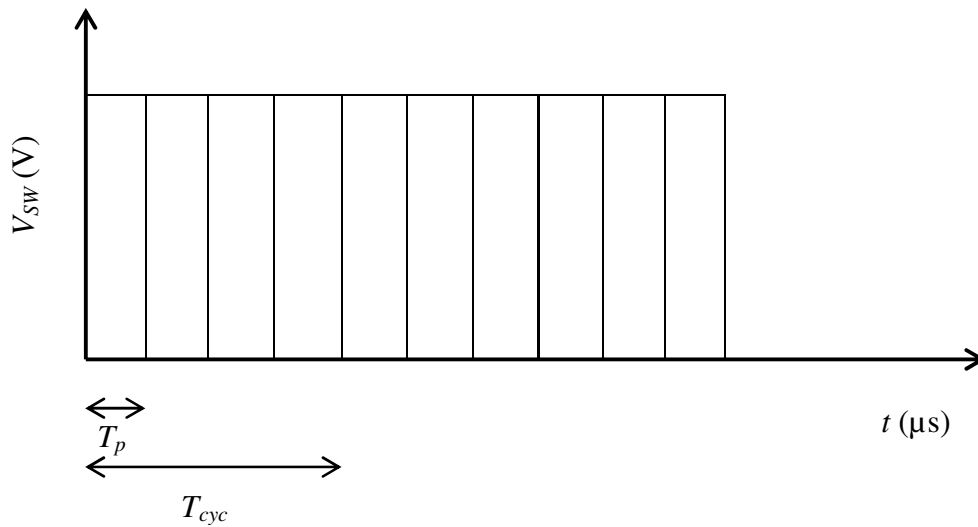
Fig. 4.2.1 shows the subsystems that make up the detector. The typical design of the clock, transmission gate (TG) and TIA are the same. To implement the proposed topology change, the pixel and MUX circuitry will differ slightly.

The classical way to implement these detectors is by means of a sequential scanning technique, which is shown in Fig. 4.2.2.



**Figure 4.2.2** Graphical representation of the sequential scanning technique

In Fig. 4.2.2, each block denotes a pixel. Sequential scanning is a technique through which one pixel at a time is read. Since the need for imaging requires a two-dimensional image, an array needs to be constructed and read out accordingly. There are two different methods of performing the readout. The first one is a pixel-by-pixel readout and the second one is where a row of pixels is switched on and then the pixels are read out sequentially. The latter is preferred because of the simpler clocking circuit in terms of speed. This then requires each row to be switched on sequentially and no two rows must be switched on at the same time. Fig. 4.2.3 depicts this required timing signal.

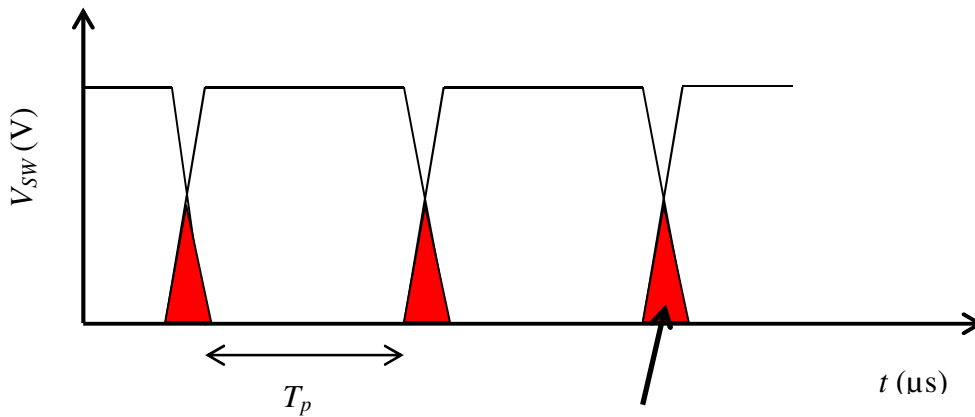


**Figure 4.2.3** Timing signal of the base clock

In Fig. 4.2.3,  $T_{cyc}$  denotes the cycle time of the detector. This is the time it takes to read out the entire array in the detector.  $T_p$  denotes the time one pixel is on. The relevant parameters can be determined by (4.2.1).

$$T_p = \frac{T_{cyc}}{\# \text{ pixels}} \quad (4.2.1)$$

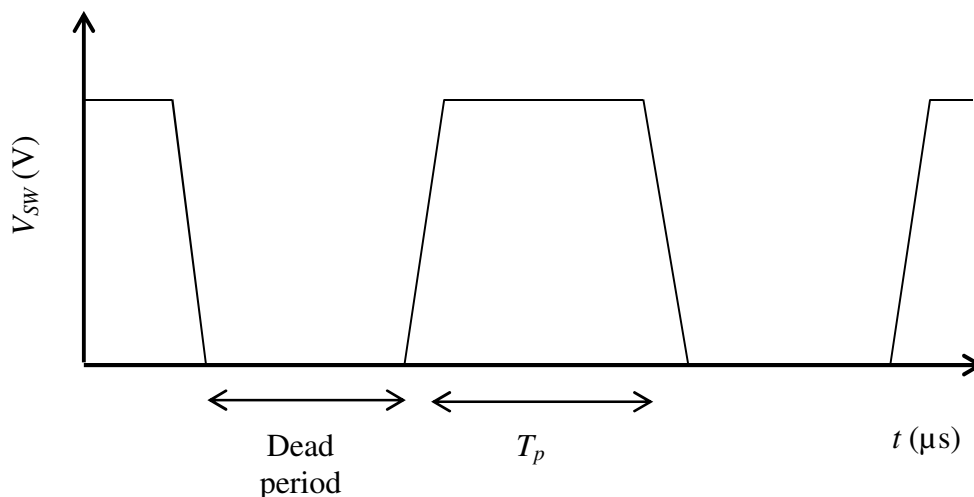
Here it can be seen that the on-time of the pixel and the cycle time are directly proportional. To implement a detector that has a fast cycle time and a large number of pixels, the pixel on-time rapidly becomes small and then parasitics can play a role if gigahertz speeds are required. This is a limiting factor in detector sizes. The complete detector also becomes complex. Since this research is about improving the DR and sensitivity and has no specific requirement for the number of pixels, it was decided to implement four pixels. It was found that when using this method, some unwanted output overshoot occurred and in some cases errors occurred in the output. The reason for that is explained in Fig. 4.2.4.



Double on-time

**Figure 4.2.4** Graphical representation of the multiple switching problem

In any electronic switching circuitry, switching can never occur instantaneously (infinite rising slope). This is due to the finite rise-time that all components exhibit. This will then have the effect of one line in the process of being switched off and another line starting to switch on. There will be a short period where both lines are partially on, which is illustrated in Fig. 4.2.4. This can present problems of certain components switching at the wrong time and can produce errors in the output, especially at high frequencies. One way of overcoming this problem is to have a finite dead period between the switching. This is illustrated in Fig. 4.2.5.


**Figure 4.2.5** Dead period realisation in switching circuitry

As shown in Fig. 4.2.5, the dead period is an inert period between successive switching where no excitation occurs. This dead time allows the different components to settle to

their initial value and no errors or unwanted switching can occur because of the double on-time. The exact time needed for the dead period can change. The shortest time for this is the time it takes for all the components to settle to their initial value. Since improving the DR and sensitivity of IR detectors is the focus of the research and not the switching of the peripheral circuitry, the time for this dead period was chosen to be one pixel on-time long. This can be shorter but it is not crucial. Because of this extra time, (4.2.1) changes to (4.2.2):

$$T_p = \frac{T_{cyc}}{\# pixels \times 2} \quad (4.2.2)$$

This requires a cycle time of twice the original cycle time of the detector. If the same cycle time is required, the base oscillator speed has to be doubled and possible output overshoot problems may occur owing to the ultrafast switching that is required, but the final output signal exhibits reduced noise and errors. For this research, with the choice of four pixels and a cycle time of 1  $\mu$ s, the pixel on-time was found to be 125 ns.

### 4.3 CLOCK CIRCUITRY AND MUX

There are several methods to implement the required clock circuitry. A few considerations have to be kept in mind. The first one is whether to implement the oscillator internally or externally. Internal voltage controlled oscillators occupy a large amount of die area, typically around 1 mm<sup>2</sup> [49] – [52]. Separate circuitry is required to transform these signals to square wave signals. For the IR detector implemented in this research, three different clocks were required to control the input clock, reset pin and the TG pin, which required extra circuitry to realise. External oscillators were chosen, since precise oscillators were readily available and fewer on-chip components were needed, which also reduced the required die area and associated costs.

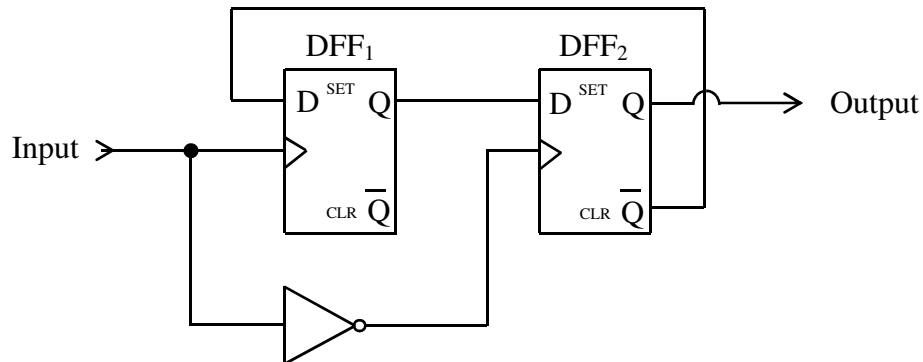
The most common way of implementing a clock signal with a specific duty cycle is to take an oscillating signal, frequency divide it and then take logic circuits to produce the required signal at the specific time. To realise this, a frequency divider and logic circuits are required, each of which will be explained separately.

### 4.3.1 Frequency divider

For this research, square waves are required and therefore only dividers that can divide block-waves will be considered. The most common concept used to perform block-wave frequency divide is with the modified latch-and-hold concept.

#### 4.3.1.1 Modified latch-and-hold

The modified latch-and-hold technique makes use of the well-known D Flip-Flop digital circuit to perform the latch and hold function. Figure 4.3.1.2 shows the topology of the divider circuit.

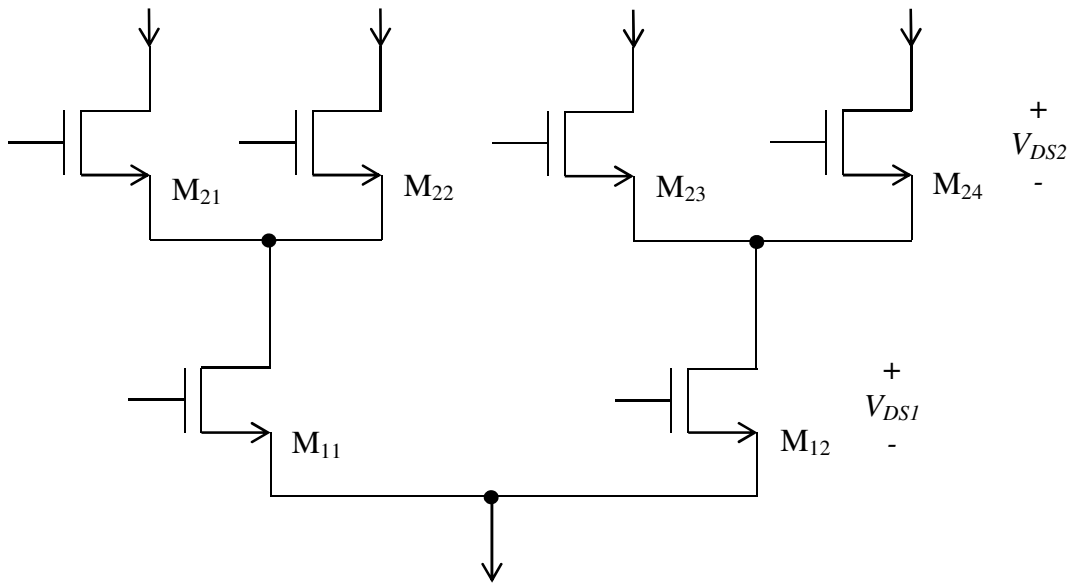


**Figure 4.3.1.2** Modified latch-and-hold circuit

As seen in Fig. 4.3.1.2, the input signal is fed into the clock of the first D Flip-Flop (DFF<sub>1</sub>) and the output is taken at the Q-pin of the second D Flip-Flop (DFF<sub>2</sub>). The output at that pin gives the divided input. The first DFF<sub>1</sub> performs the latch function, while DFF<sub>2</sub> performs the hold function. When the clock reaches the lower limit, the functions are reversed, hence producing the divided signal.

### 4.3.2 Multiplexer

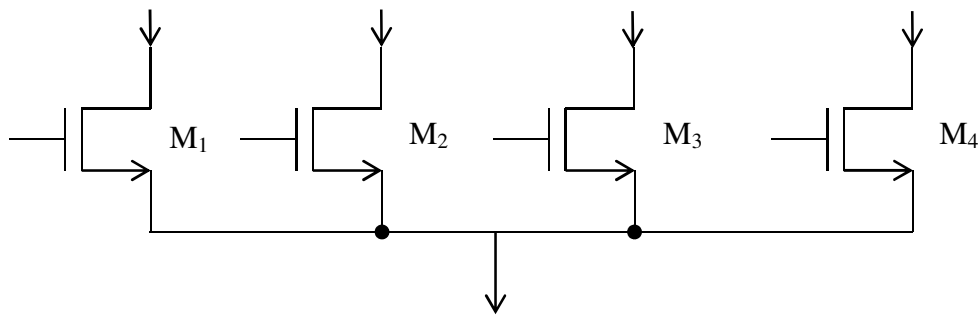
There are two methods of implementing MUX circuits in monolithic devices, both with distinct advantages and disadvantages. Generally it is preferred to implement these circuits with MOS devices, since HBTs have a finite gate current, which increases the complexity of a design. The two methods are explained with the aid of Figs 4.3.2.1 and 4.3.2.2.



**Figure 4.3.2.1** Folded MUX topology

As shown in Fig 4.3.2.1, the folded MUX topology makes use of stacked MOS transistors to guide the particular line to the output. This topology is generally not preferred in monolithic devices, because each MOS device has a  $V_{DS}$  drop, which then requires a larger drop, especially if there are a large number of lines and the total supply is limited to the process. However, with this topology, the clocking circuitry is simple because no complex duty cycle generators are required. Fig. 4.3.2.2 depicts the linear MUX topology.



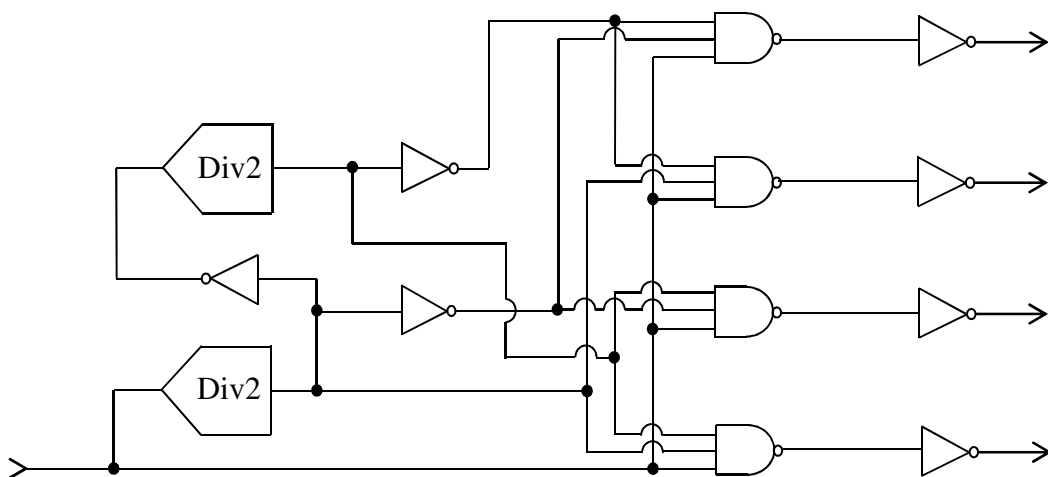


**Figure 4.3.2.2** Linear MUX topology

Fig. 4.3.2.2 shows the linear MUX topology. It comprises multiple MOS devices of which all the sources are connected together. This method is more generally preferred because it has only one  $V_{DS}$  drop from the pixels to the output. This, however, requires more complex clocking circuitry, since each switch needs to be switched on for a portion of the cycle; hence a duty cycle generator is required, which is explained in section 4.3.3.

### 4.3.3 Duty cycle generator

Because of the requirement of the MUX circuit to have a duty cycle generated wave, the clock signal has to produce this wave. The easiest way to generate these waves is with the aid of the frequency divider and some digital logic. The resulting circuit diagram is shown in Fig. 4.3.3.1.



**Figure 4.3.3.1** Duty cycle generator circuit diagram

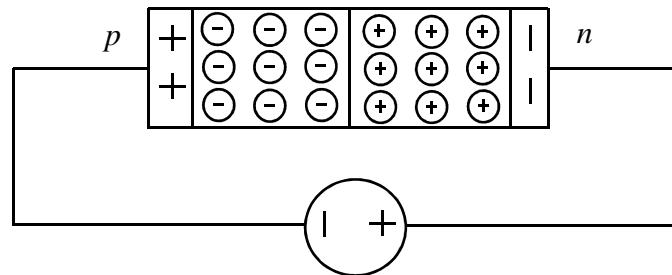
As can be seen in Fig. 4.3.3.1, the incoming clock signal is divided twice and with the use of inverters and NAND gates, the required clock signals are generated. Some die area is

saved and the complexity is reduced by the dead period requirement, as mentioned in section 4.2.

#### 4.4 PIXEL

There are two ways of collecting IR radiation monolithically. The first is by using SiGe reverse-biased diode-connected HBTs and the second by using PPDs. The drawback of PPD is that for the same amount of output current, more PPDs will be required, which will occupy a larger chip area. The advantage of HBTs is that they contain inherent gain not found with PPDs. Nonetheless, it was found that there was sufficient space on the chip and therefore both types were implemented to compare the results.

The reverse-biased diode-connected transistor has a wider depletion region. The base and emitter were shorted such that the  $p-n$  junction is created between the collector and the shorted base and emitter. Fig 4.4.1 illustrates this graphically.

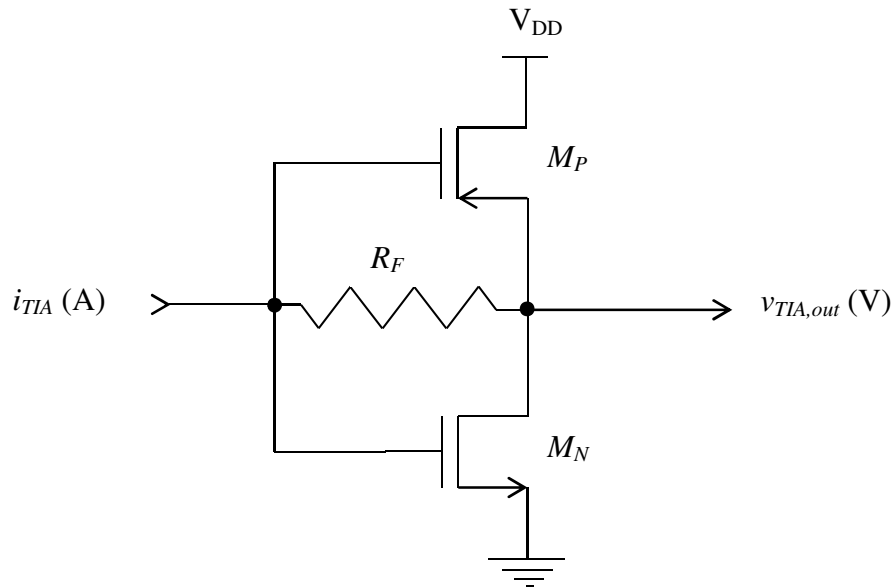


**Figure 4.4.1** Reverse-biased diode

The size of the depletion region is proportional to the applied electric field as shown in Fig.4.4.1. Therefore the applied bias voltage should be just large enough to ensure that avalanche breakdown does not occur. When the diode is externally biased, in this case with incident light, then an electron is released from the  $p$ -type material and is pulled to the  $n$ -type material. This then flows through the external voltage source, hence current flow is generated. The amount of current flow is proportional to the incident light.

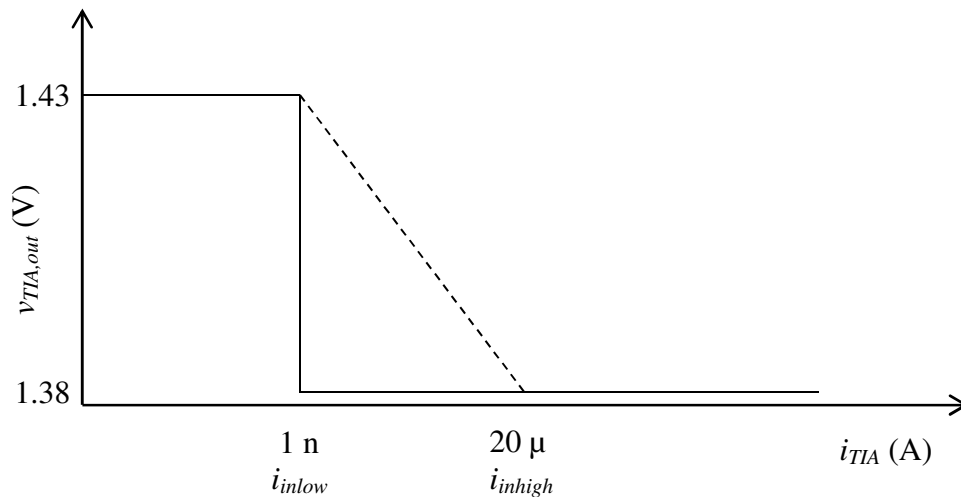
## 4.5 TIA

The detector implemented in this research is a current mediator type detector. This was chosen because of the ease of integration and therefore the system works mainly with currents. Ultimately the output needs to be a voltage for post-processing and hence a TIA was needed. The most common TIA is the inverter type shown Fig. 4.5.1.



**Figure 4.5.1** TIA

As seen in Fig. 4.5.1, the TIA chosen for this research is made up of a classical logic inverter configuration with a feedback resistor. With no feedback resistor, the transfer gain curve has a vertical asymptote in the transition band, whereas with a feedback resistor, there is a finite gain. To maximise the resolution of the detector, the gain must be controllable. Fig. 4.5.2 illustrates this.

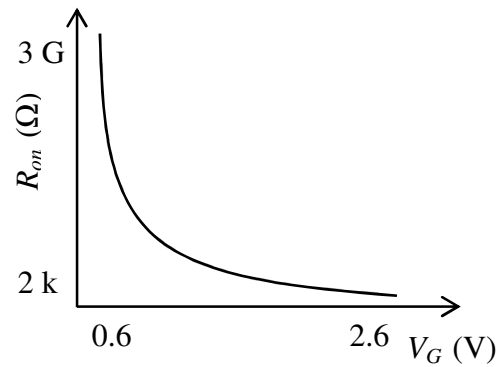


**Figure 4.5.2** Transfer curves for different TIAs

The solid line in Fig. 4.5.2 indicates the transfer curve for the classical inverter, whereas the dashed line indicates the transfer curve for the TIA with resistive feedback. It is of importance that the input current falls between the  $i_{inlow}$  and  $i_{inhigh}$  values, otherwise there will be a loss of information. The TIA used for this research requires the MOS devices to be in the triode region. This requires the  $V_{BIAS}$  input to be at 1.7 V. Appendices B and C provide a discussion on the design and calculated results.

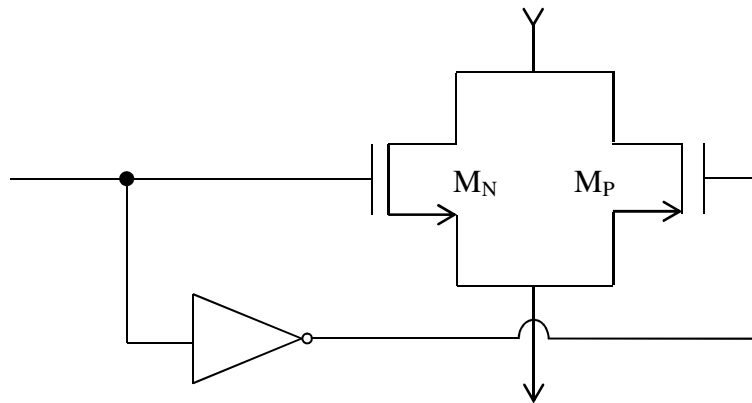
#### 4.6 TRANSMISSION GATE

Generally a MOS device biased in the triode region of operation operates as a switch with adequate performance. However, it was found that in one half of the switching action, unwanted overshoots occurred. The overshoots can be attributed to the on-resistance and inherent output capacitance of the MOS devices. The typical resistance curve for a given gate voltage is shown in Fig.4.6.1.



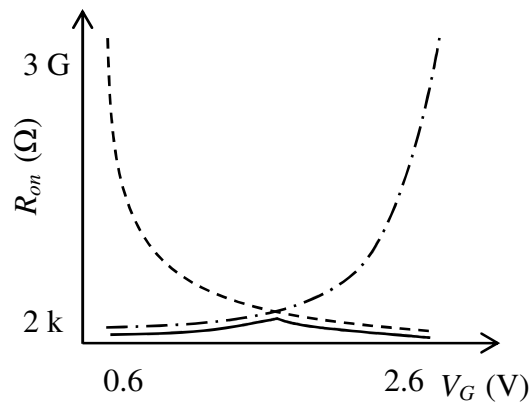
**Figure 4.6.1** On-resistance for a NMOS device in triode region

In the triode region of operation, with a very low gate voltage, any  $n$ -channel MOS (NMOS) device exhibits a high off-resistance (and a low on-resistance with a large gate voltage, as shown in Fig. 4.6.1. This causes sudden unwanted voltage overshoot. The way to overcome this problem is with the aid of TGs. The TG used for this dissertation is shown in Fig. 4.6.2. This overshoot is shown graphically in Figs. 4.8.2.1 and 4.8.2.2.



**Figure 4.6.2** Schematic of a transmission gate

Fig. 4.6.2 shows the schematic diagram to realise a TG. The advantage of using an inverter here is that only one clock is required and not two complementary clocks. The on-resistance curve of the TG is shown in Fig. 4.6.3.

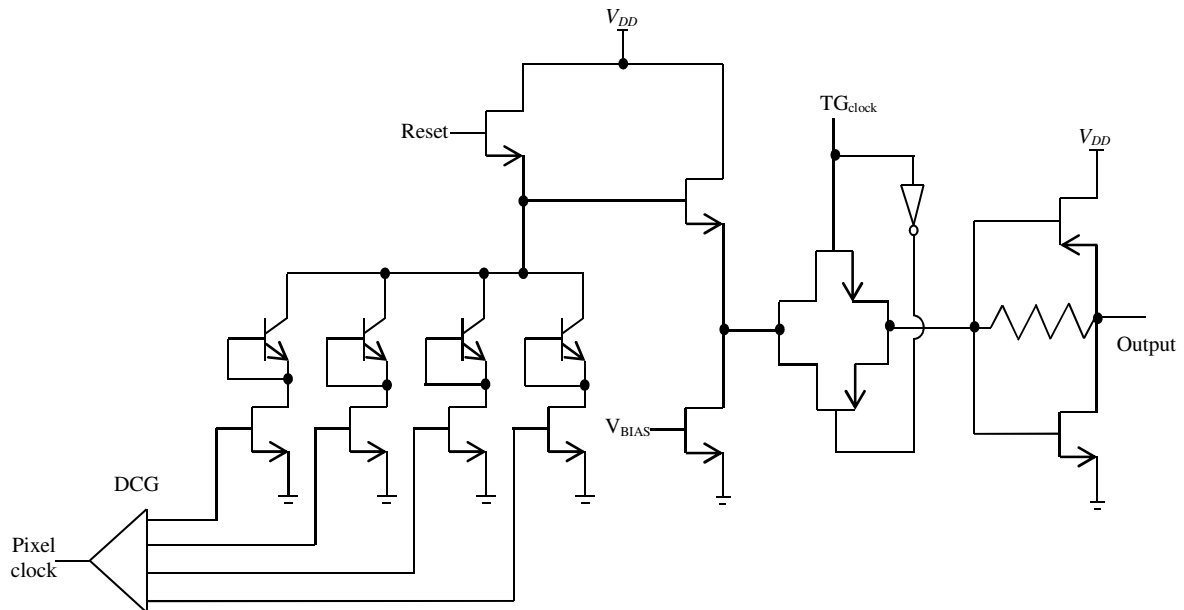


**Figure 4.6.3** On-resistance curve of a transmission gate

In Fig. 4.6.3, the solid line depicts the on-resistance curve for the TG. It is a flatter response as opposed to the sudden drop in resistance. The only real requirement in terms of design here is that both transistors (NMOS and PMOS) must have the same aspect ratio to achieve the flattest response possible.

#### 4.7 OVERALL CIRCUIT

Two different detectors were implemented in the final circuit design. One is the single-pixel-single-amplifier detector and the other is the multiple-pixel-single-amplifier detector. A distinct feature included in both detectors is a bias transistor to achieve the correct biasing levels, as well as an adjustable input clock swing to achieve the best output. That will also decrease the unwanted output overshoot caused by the spurt of charge built up before switching. Fig. 4.7.1 shows the schematic of the multiple-pixel-single-amplifier detector.



**Figure 4.7.1** Multiple-pixel-single-amplifier detector schematic

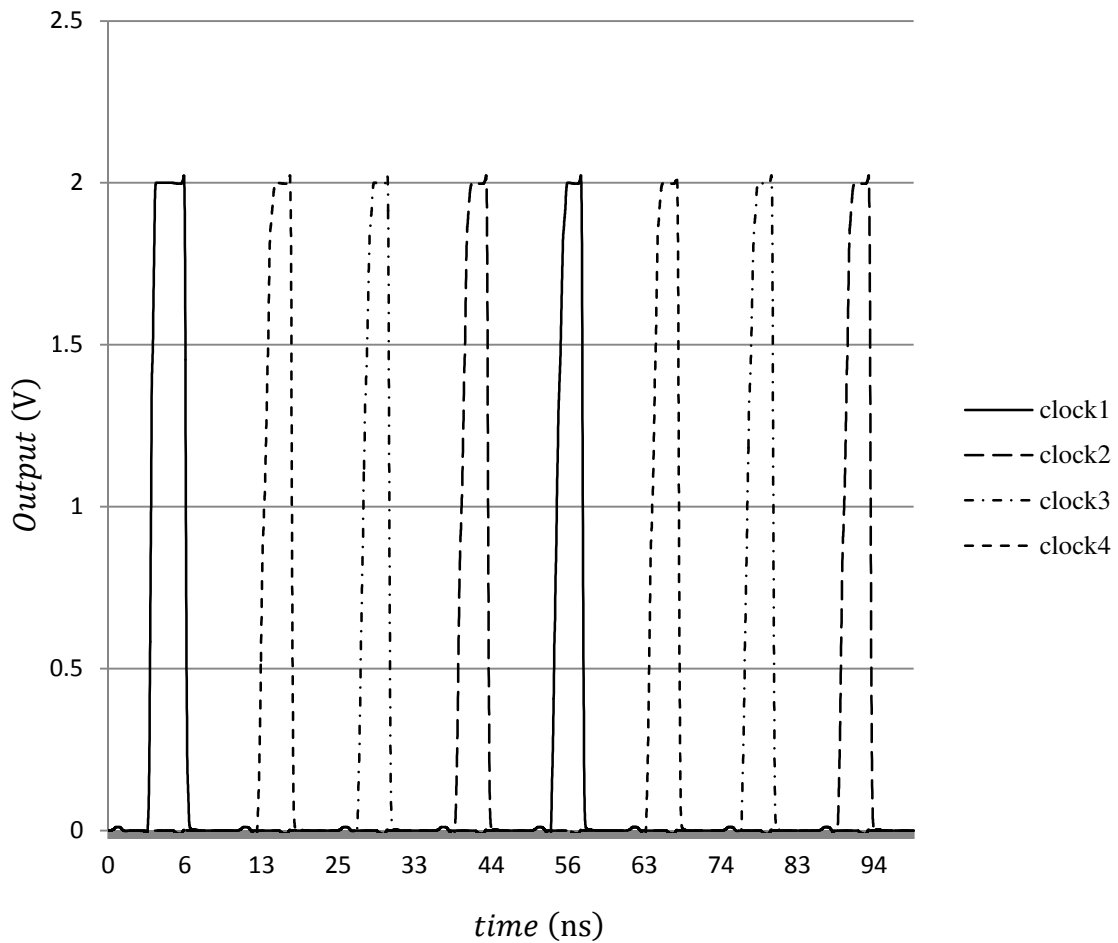
The duty cycle generator denoted by DCG in Fig. 4.7.1 is shown in Fig. 4.3.3.1. Fig. 4.7.1 shows the schematic of the multiple-pixel-single-amplifier detector. The duty cycle generator subsystem circuit diagram is shown in Fig. 4.3.3.1. The full detector requires a small number of components; hence a small wafer area is needed. Pixel clock, Reset,  $TG_{clock}$ ,  $V_{BIAS}$  and Output are input and output pins of the detector.

## 4.8 SIMULATIONS

This section contains the simulations with the aid of Cadence Virtuoso. The duty cycle generator was simulated separately and then the full system. Tables V and VI describe the procedure used to obtain the noise and sensitivity simulation. Since the supply voltage of the process ( $V_{DD} = 3.3$  V) and the transistor gains (for both the HBT and the MOSFETs) are fixed, the design of the detector was based on these fixed values.

### 4.8.1 Duty cycle generator

The duty cycle generator time-domain simulation is shown in Fig. 4.8.1.1.



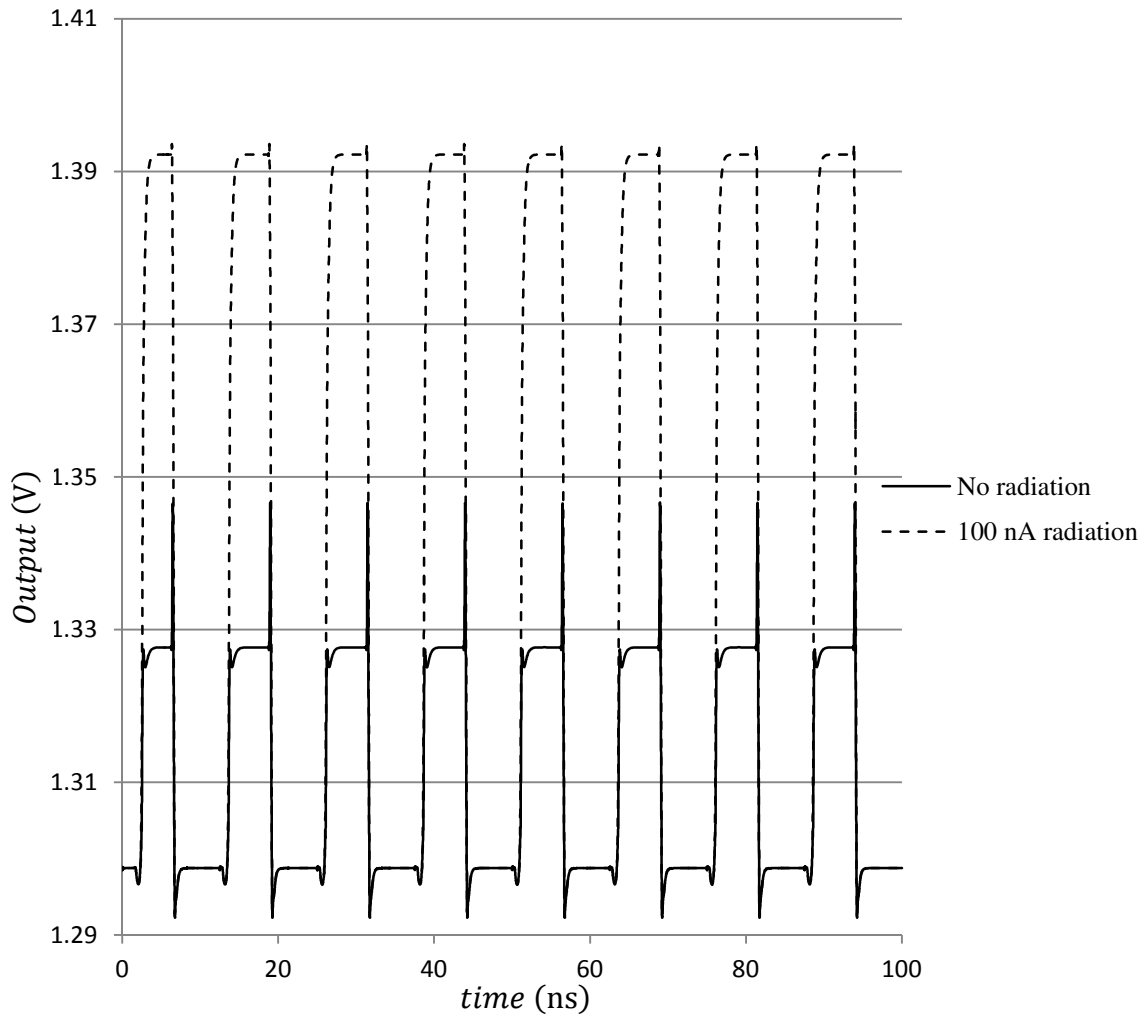
**Figure 4.8.1.1** Duty cycle generator time-domain simulation

Fig. 4.8.1.1 shows the dead periods of the duty cycle generator in between successive switching. This is to ensure correct operation of the MUX. The maximum value of the generator is limited to the supply voltage or the maximum value can be controlled via an external supply, which was done. The purpose of that was to provide the MUX with the best possible clock with minimal voltage spikes.

## 4.8.2 Full system

To simulate the full IR detector to verify the improvement in DR and sensitivity in the time domain, a clock was required but was not implemented in the prototype IC. An external clock in the form of a voltage pulse generator was used for this purpose. The full system simulation is shown in Fig. 4.8.2.1.





**Figure 4.8.2.1** Full system simulation with and without radiation

Fig. 4.8.2.1 shows the full system simulation with and without radiation. To add some radiation, in simulation, a current source needs to be inserted that is directly proportional to the radiation received [47]. This relation is defined by (4.8.2.1).

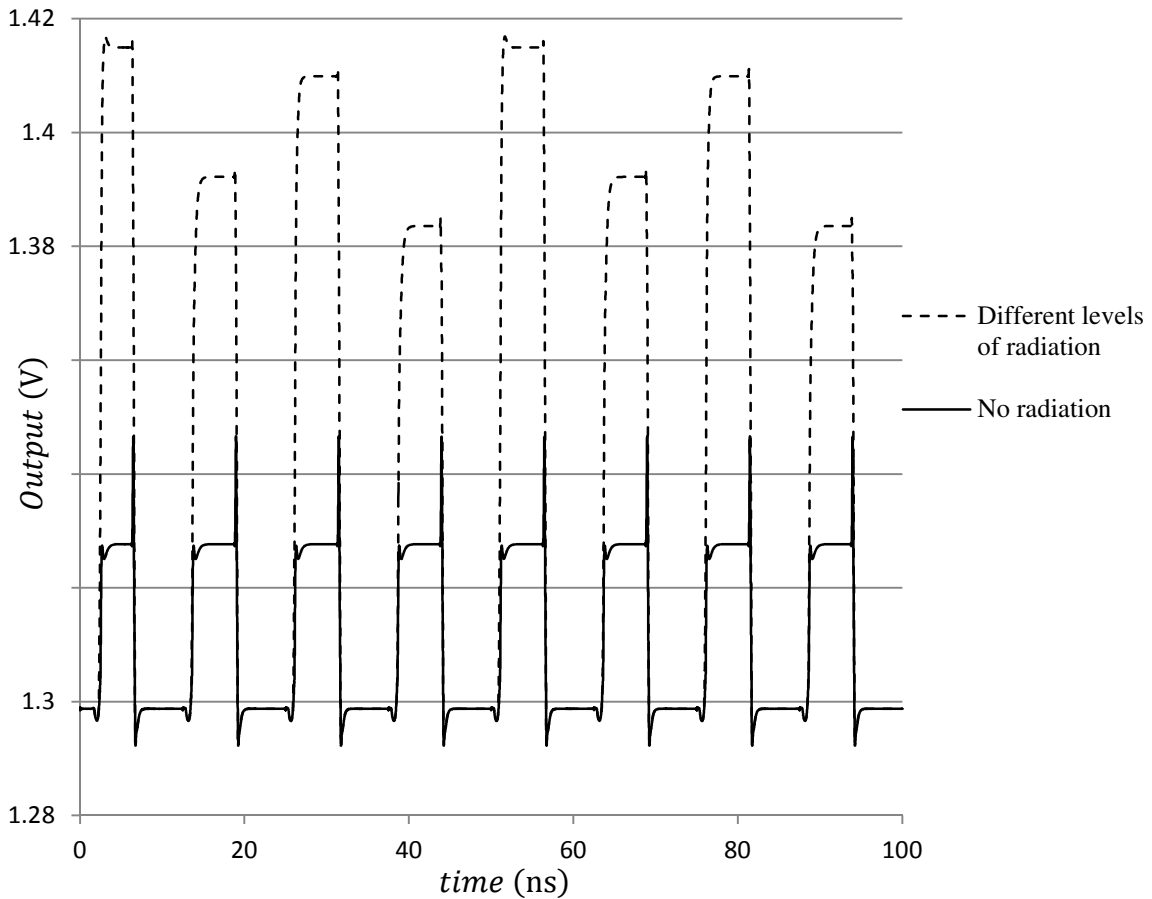
$$i_{ph} = \eta \times q \times \phi \times A \quad (4.8.2.1)$$

where  $\eta$  is the efficiency of the pixel,  $q$  is the charge of an electron ( $1.6 \times 10^{-19}$  C),  $\phi$  is the photon flux ( $\text{W}/\text{cm}^2$ ) and  $A$  is the area of the pixel.

Noticeably when a pixel is read, the output voltage increases accordingly.

To ensure the correct functionality of the IR detector, different levels of radiation were added and the results were observed. In reality this is essential, since the same amount of

radiation will never be present on every pixel, although it may be close. Fig. 4.8.2.2 depicts this simulation.



**Figure 4.8.2.2** Full system with and without different levels of radiation

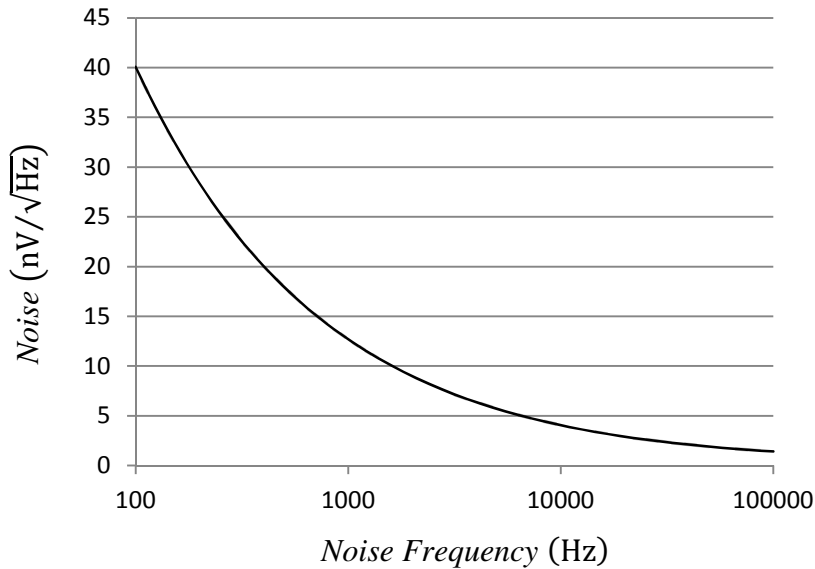
Clearly shown in Fig. 4.8.2.2 is a difference in output voltage level when radiation is present. It was found that this detector can detect radiation generating a current between 50 nA and 500 nA for the given pixel size. Below the value of 50 nA, dark current and noise will be dominant. Above 500 nA the detector will become saturated.

### 4.8.3 Noise simulation

The most common parameters of noise measurements in the application of IR detectors is the output noise and noise figure. Each of these was simulated separately.

### 4.8.3.1 Output noise

Fig. 4.8.3.1.1 depicts the output noise associated with both detectors.

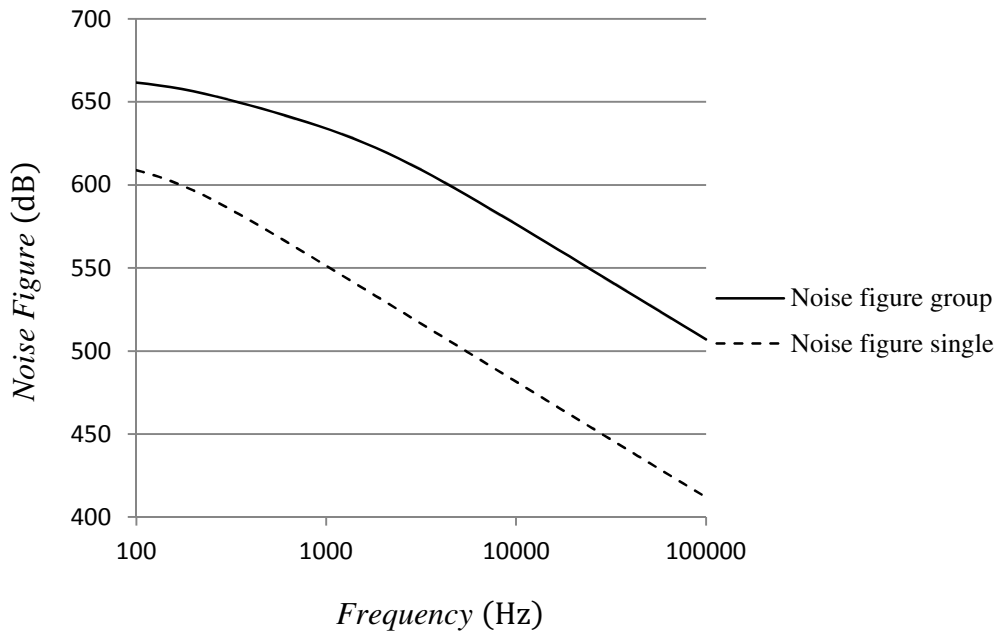


**Figure 4.8.3.1.1** Noise simulation of both detectors

Fig. 4.8.3.1 shows the total output voltage noise present with a  $50 \Omega$  termination at the input. As the input parameters to the simulation remain fixed, the simulation results for the four detectors are identical. This, however, shows the output voltage noise under ideal circumstances.

### 4.8.3.2 Noise figure

Fig. 4.8.3.2.1 shows the noise figure of the detectors.

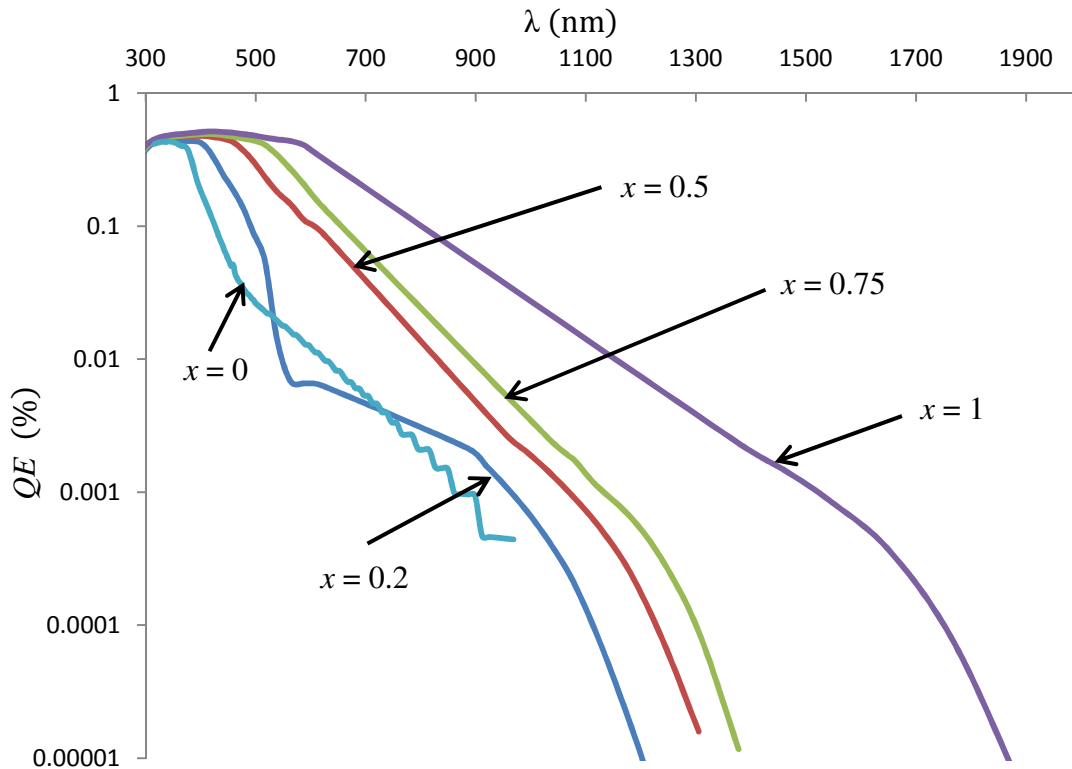


**Figure 4.8.3.2.1** Noise figure of the detector

Fig. 4.8.3.2.1 shows the noise figure simulations of both detector topologies. The results show an increase in noise figure when pixels are grouped together. This can be attributed to the FPN present when pixels are grouped. The advantage of grouping of pixels is the increase in fill factor; however, the noise figure is also increased. The group noise figure of the Si p-i-n diode detector and the diode-connected SiGe HBT IR detector was found to be the same. The same applies for the single-pixel detectors. This is due to the same readout circuitry used for both types of pixel structures. The pixel element noise contribution was negligibly small compared to the noise in the rest of the circuit.

#### 4.8.4 QE

Fig. 4.8.4.1 shows the QE of silicon detectors with different levels of fractions of germanium.



**Figure 4.8.4.1** QE of IR detectors

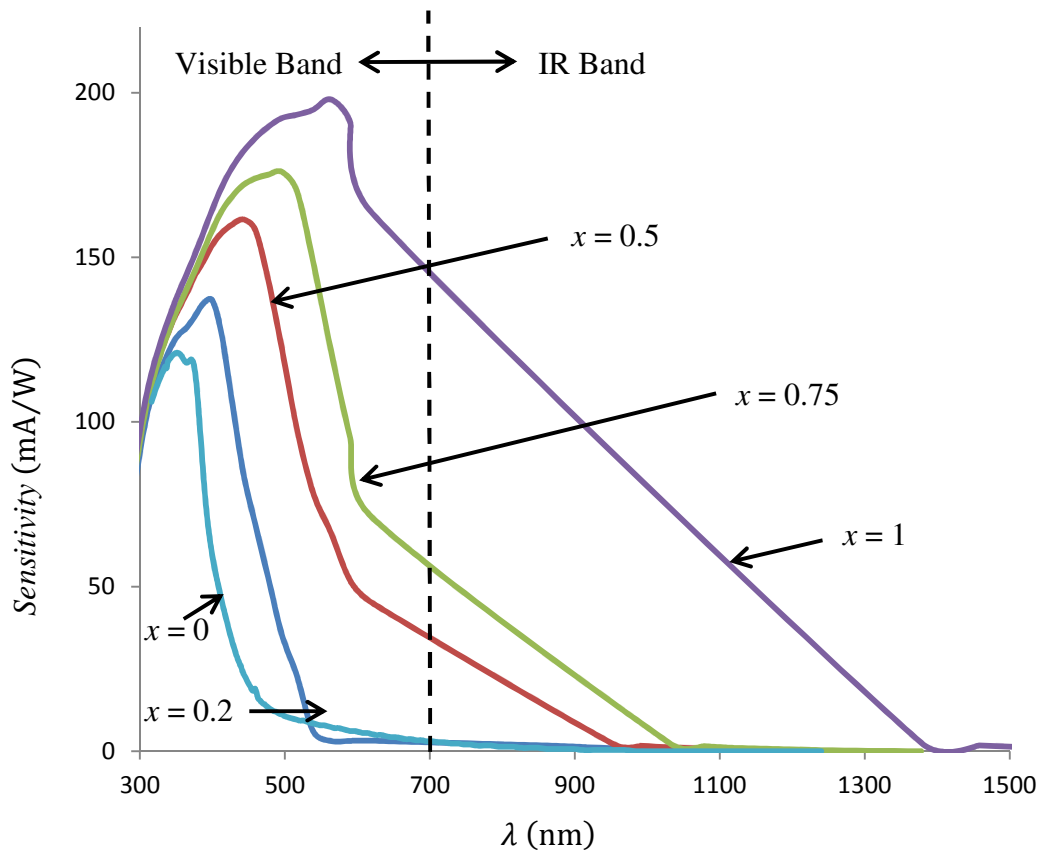
Fig. 4.8.4.1 shows the QE of  $\text{Si}_{1-x}\text{Ge}_x$  detectors with no special pixel structures. Equations (2.6.1) and (2.7.1) together with the experimental absorption coefficients [54] were used to obtain this graph. It shows that the maximum possible QE of SiGe IR detectors are around 0.5 % at 430 nm. Noticeably the detecting band shifts more to the near-IR band as the germanium fraction increases. Post-processing, by making use of amplifiers, can increase the QE of materials significantly. Fig. 4.8.4.1 depicts the QE of the pixel elements only.

The results show that the  $x = 0$  and  $x = 0.2$  curves intersect. Upon further inspection, by using the  $\alpha_0$  values of the respective Ge fractions, it was determined that the lines follow the same trend as shown in Fig. 4.8.4.1. The intersection is likely an instrumental error.

#### 4.8.5 Sensitivity

In Cadence Virtuoso, there is no option to simulate the sensitivity directly. Also, no theoretical model exists of the induced photon current when SiGe HBTs are illuminated. Therefore practical radiation and doped region width values were used, together with

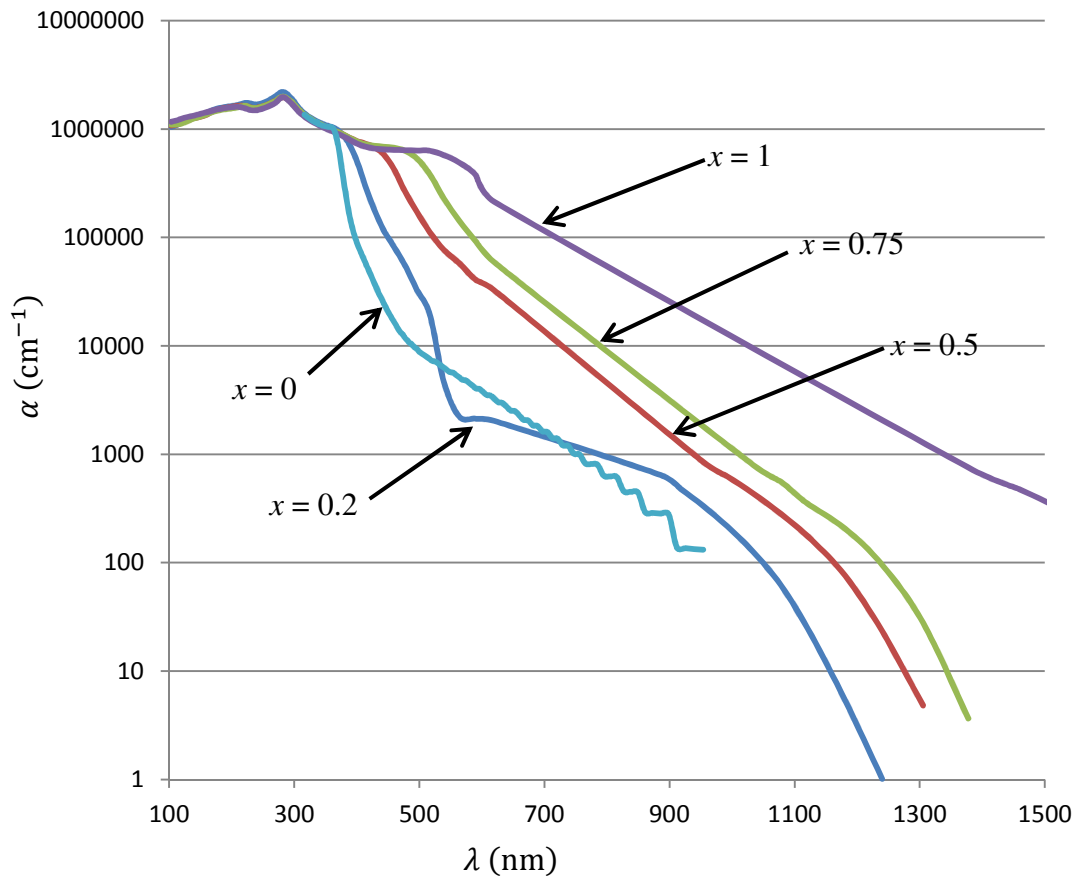
absorption coefficients given in Appendix A. Fig. 4.8.5.1 shows the sensitivity of the detectors.



**Figure 4.8.5.1** Sensitivity of IR detectors

Fig. 4.8.5.1 shows the sensitivity of  $\text{Si}_{1-x}\text{Ge}_x$  detectors. Incident energy of 1 mW and a doped region width of 5  $\mu\text{m}$  were used in the simulation. The sensitivity of a detector increases as the fraction of germanium increases. The detecting band gradually shifts to the IR band as the fraction of germanium increases. This makes SiGe a viable material for IR detection. Noted in Fig. 4.8.5.1 is the straight line in the latter part of every simulation. Usually a sensitivity curve is similar to a resistor-capacitor charge-discharge curve. This straight line is due to the experimental data used to perform this simulation. The absorption coefficients over the band of interest are given in Appendix A.

The absorption coefficients as a function of wavelength are plotted in Fig 4.8.5.2.



**Figure 4.8.5.2** Absorption coefficients as a function of wavelength

Fig. 4.8.5.2 shows the absorption coefficients for Si wafers with different fractions of Ge included according to  $\text{Si}_{1-x}\text{Ge}_x$ . It can be seen that an increase in the Ge fraction exhibits a shift to the IR band. This is the underlying mechanism on which this work is based.

## 4.9 CONCLUSION

This chapter presented the proposed prototype that was used to verify the hypothesis in question. Schematics that were documented and challenges that were found were pointed out and proposed modifications were implemented. The simulation results of the detector are also presented in this chapter. The time domain simulations of the detector performed as expected.

# CHAPTER 5 LAYOUT AND FABRICATION

## 5.1 INTRODUCTION

This chapter describes the layout and fabrication of the detector. Some of the HIT-Kits provided by the foundry were used. Recommendations made by the foundry were strictly followed and common layout practices used in industry, such as the common centroid layout, were adhered to. The Ge fraction could not be selected since this is specific to the particular BiCMOS process.

## 5.2 LAYOUT TECHNIQUES

For the purpose of this research work, symmetrical layout was applied. Symmetrical layout allowed for multiple instances of similar cells which were placed in close proximity to each other, and a balanced approach for signals. This placement approach is preferred so process variations such as non-uniform doping play a less significant role in the outcome. For instance, some of the components were placed in an ABABA format where A and B are different components. For the clock divider, the D Flip-Flops are placed right next to each other to have matched components as far as possible in terms of doping concentration.

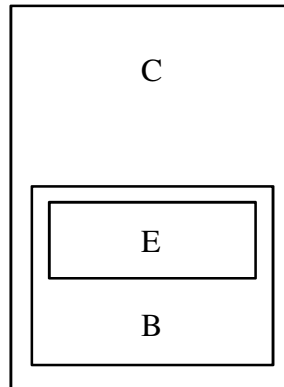
The ams AG 0.35  $\mu\text{m}$  SiGe process has four available metal layers, each with its own current density. The maximum allowable current density is given in the process parameter documentation [55]. Because of a non-disclosure agreement between the author, the university and the selected foundry, specific process or geometrical parameter(s) have been omitted. Simulations show required currents of 20  $\mu\text{A}$ , which is far less than the maximum allowable current. Therefore, in most of the connections, minimum width metal lines were used. The top metal layer was not needed because of the small number of interconnections and lower frequency of operation.

The maximum switching frequency in this prototype is around 80 MHz. This corresponds to an electrical length of larger than 0.01 and therefore transmission line effects did not



play a role. To implement a long wire, the lowest metal layer, was used as far as possible because of the low material resistance it presents.

The ams AG process does not require HBTs to be placed in a common centroid layout although it is recommended in their guidelines and in literature [48]. Fig. 5.2.1 depicts the layout of an HBT, which was used as a pixel in this research.



**Figure 5.2.1** Layout of an HBT in the ams AG process

In Fig. 5.2.1 C, B and E are the collector, base and emitter respectively. The fundamental difference between an HBT and a BJT is explained in section 2.9. For the one detector these HBTs were used as the pixel element.

The TIA requires resistive feedback, as mentioned in chapter 4. Since this detector is a current-mediated mode detector, varying currents will flow through the diode-connected MOS resistor if a MOS device is used as the resistive element and thus change the amplification of the TIA. Therefore MOS devices were not used. The only other option available is on-chip resistors. Generally resistors are not preferred in monolithic devices because of their large size but in some cases one cannot do without these devices where a linear resistive device is needed. Normally the length of the resistor material is directly proportional to the resistance. The TIA requires a resistor of 2 k $\Omega$  for adequate amplification, which will take up a large space in the IR detector. The design of the TIA used in this research is given in Appendix B. Different materials exhibit different sheet resistances, but for the largest sheet resistance a 2 k $\Omega$  resistor will still stretch considerably

and can cause component variations. To overcome this problem, poly resistor layers were used to make turns.

### 5.2.1 HIT-Kits

The foundry supplies standard components and subsystems, which can be used as is. In some cases it is advised to use the HIT-Kits, since these have been optimised for space and performance. The following ams AG HIT-Kit cells were used for this research:

- D Flip-Flop
- Inverter
- NAND2
- NAND3.

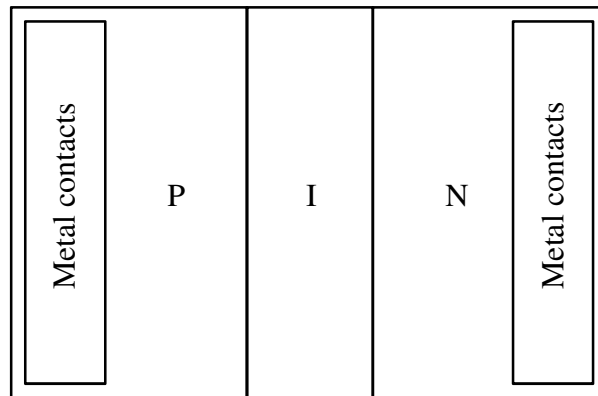
Quite simply, the specific HIT-Kit cell was instanced and the necessary connections were made. A common centroid layout was followed as far as possible.

### 5.2.2 Design Rule Check and Layout versus Schematic

The Cadence Virtuoso program comes with two critical built-in programs, namely Design Rule Check (DRC) and Layout versus Schematic (LVS). To make sure that a specific layout conforms to the design rules specified by the foundry, the DRC was applied to the layout. Not all of the errors and warnings found by the DRC routine can be corrected. For instance, one method that is sometimes used in detector research is to remove the silicon nitride layer on top of the pixel for better coupling, as was the case in this research. A pad layer needs to be put on top of the pixel. The design rules, however, specify the minimum width of the pad layer as well as other layers and viās.

## 5.3 LAYOUT OF PIXELS

The two most common ways of prototyping pixels are with diode-connected BJTs or with p-i-n diodes. Fig. 5.3.1 shows the construction of a p-i-n diode.



**Figure 5.3.1** Construction of a p-i-n diode

In Fig. 5.3.1 it can be seen that the p-i-n diode is made up of five parts, namely two metal contacts, one *p*-type diffusion, one *n*-type diffusion and an intrinsic layer. The intrinsic layer is undoped and therefore has the unique property of capturing light more easily. The undoped region also produces DRC errors but these can be safely ignored.

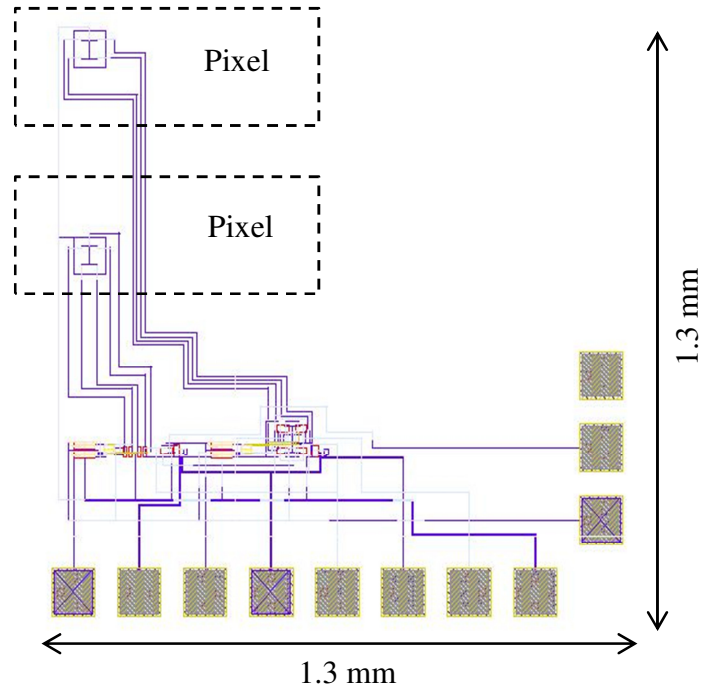
Generally several diodes have to be put in parallel in order to capture a useable amount of incident light, as seen in literature.

#### 5.4 LAYOUT OF PERIPHERAL CIRCUITRY

Since most of the components and subsystems in the *peripheral circuitry* are made up of HIT-Kits, the only real detail to consider is the placement of the subsystems. Generally they are placed in such a manner that fewer wells are needed to reduce the chances of substrate current flow between wells. Proportional to absolute temperature current sources [48] can be placed between wells is one way to avoid this problem. This was not done in this implementation, since all the wells were tied to the same voltage level and were not needed.

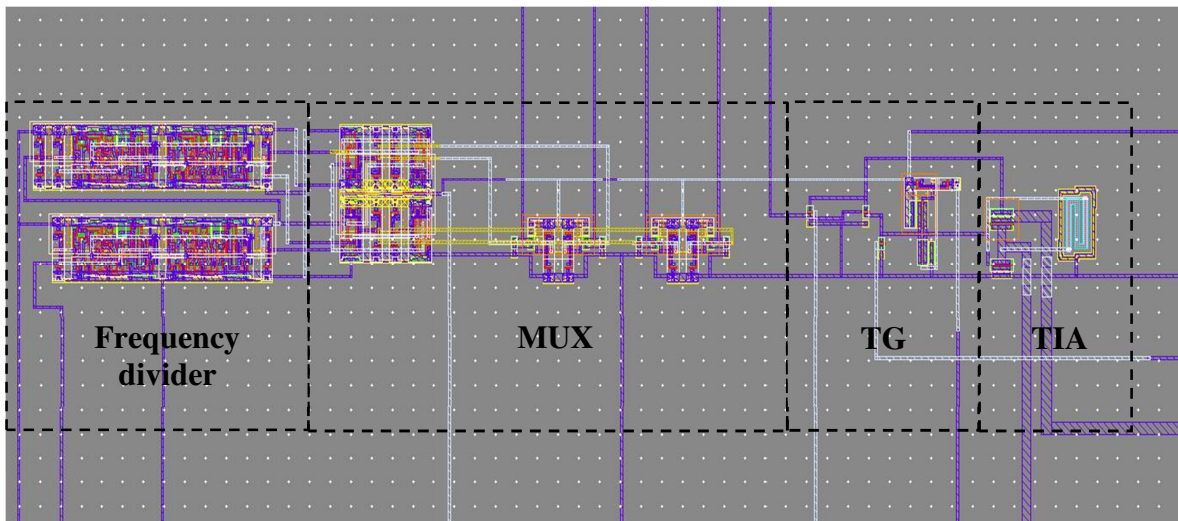
## 5.5 COMPLETE CIRCUIT LAYOUT

All of the above were combined to produce the final layout given in Fig. 5.5.1.

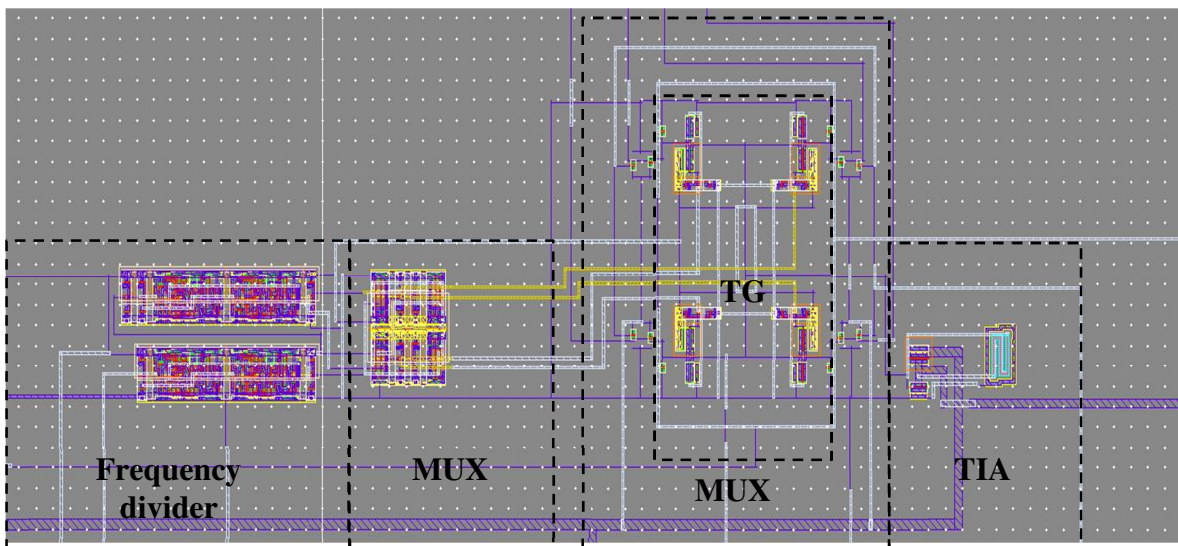


**Figure 5.5.1** Full detector layout

Fig. 5.5.1 shows the final layout of the detector. The pixels were placed 1 mm from the edge so that the pixels are in the centre of the wafer to capture most light. The shape and placement of the detector were decided upon to accommodate two other projects on the multi-project wafer (MPW). Fig. 5.5.2 and Fig. 5.5.3 show the peripheral circuitry in more detail.



**Figure 5.5.2** Peripheral circuitry of the multiple-pixel-single-amplifier near-IR detector

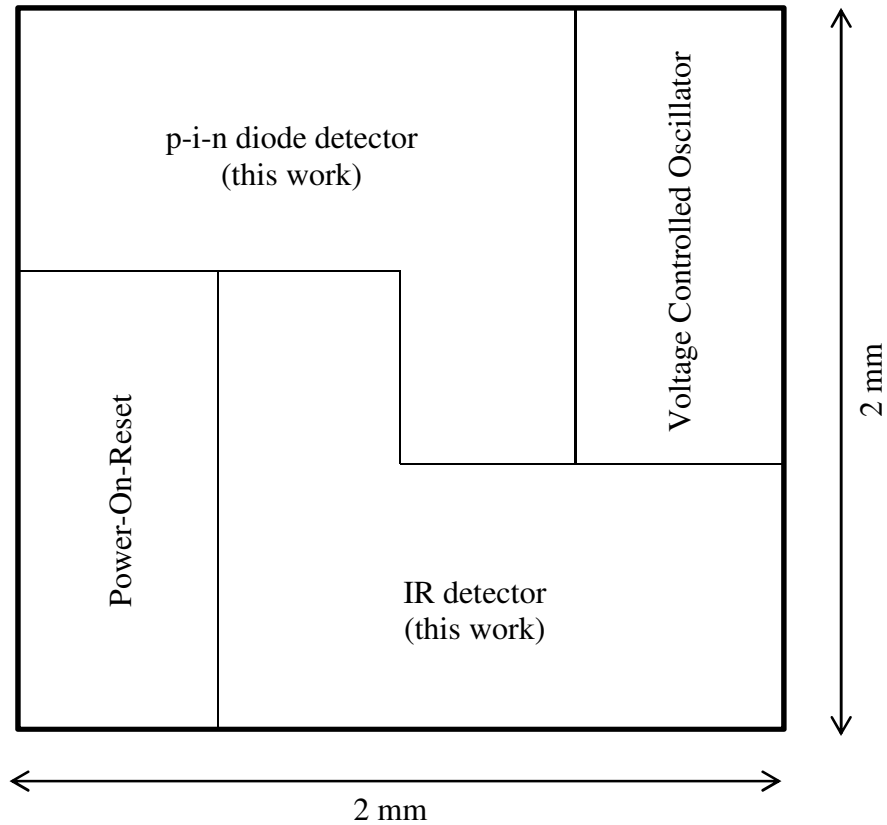


**Figure 5.5.3** Peripheral circuitry of the single-pixel-single-amplifier near-IR detector

Fig. 5.5.2 and Fig. 5.5.3 show the layout of the peripheral circuitry of the multiple-pixel-single-amplifier IR detector and the single-pixel-single-amplifier IR detector respectively. Both IR detectors require the same subsystems; the fundamental difference is the wiring of the respective detectors to realise the single pixel structure as well as the group structure, and the number of components used.

## 5.6 PLACEMENT ON THE CHIP

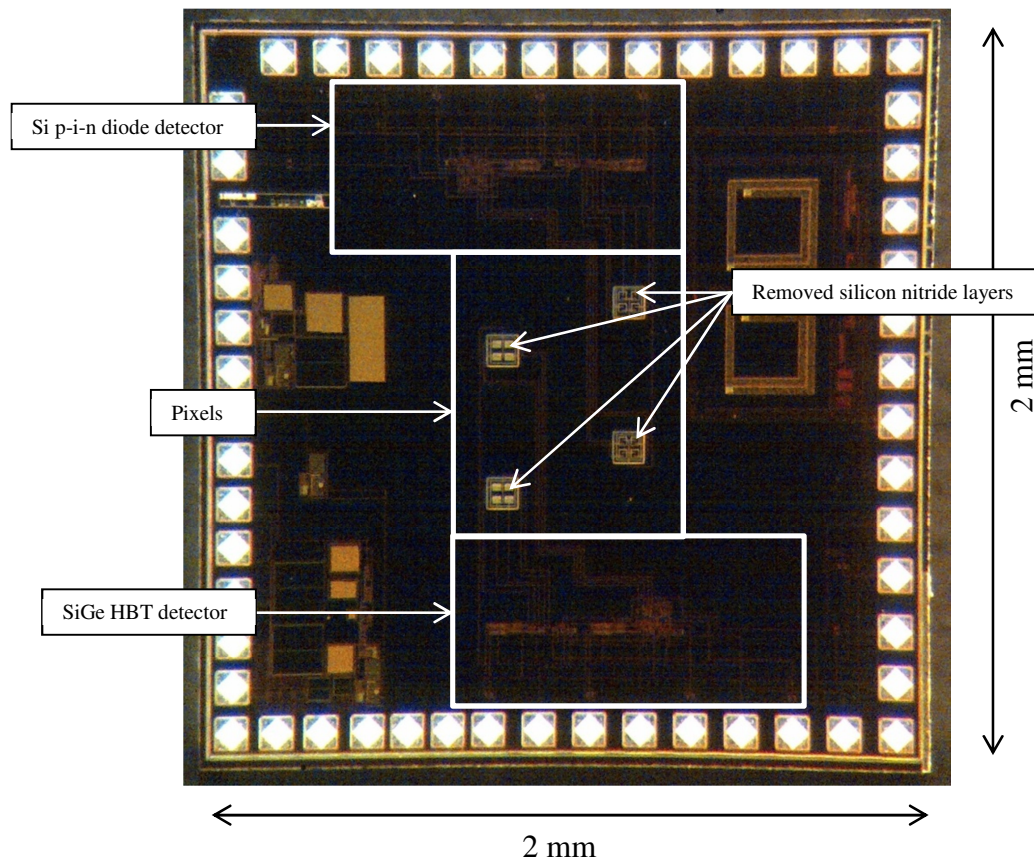
Fig. 5.6.1 depicts the final chip floor plan.



**Figure 5.6.1** Final chip floor plan

Fig. 5.6.1 illustrates the floor plan of the final chip design submitted for fabrication. The pixels were placed in the centre of the shared wafer to capture most light. The other two projects (power-on-reset and voltage controlled oscillator) on this wafer are separate and unrelated to this research. The dimensions of the chip are 2 mm × 2 mm. Fig. 5.6.2 shows the actual chip.





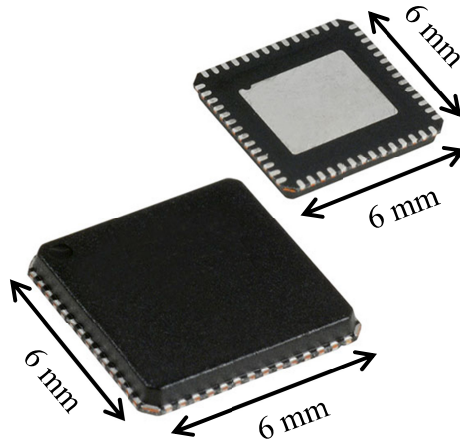
**Figure 5.6.2** Actual chip photograph

Fig. 5.6.2 shows the actual chip photograph of this work together with the other MPW-shared projects. The silicon nitride layer over the pixels was removed for better coupling, which can be seen in Fig. 5.6.2.

## 5.7 PACKAGING

The amount of current that flows through a wire and the frequency of operation of the chip are two key factors in the package choice. Since this work operates at low frequency (<1 GHz) and low power, a 56 pin dual in-line package or a quad flat no-lead (QFN) package will do. The total number of pins is 52, hence the choice of a 56-pin package. The same is true for the power-on-reset project; however, the voltage-controlled oscillator operates at 2.4 GHz. These frequencies require thin interconnects to minimise bond wire inductances. Glass lids are also required for this work, since the detector has to be illuminated to verify correct operation and to perform the required sensitivity measurements. Therefore a QFN package with a glass lid was selected, as this package

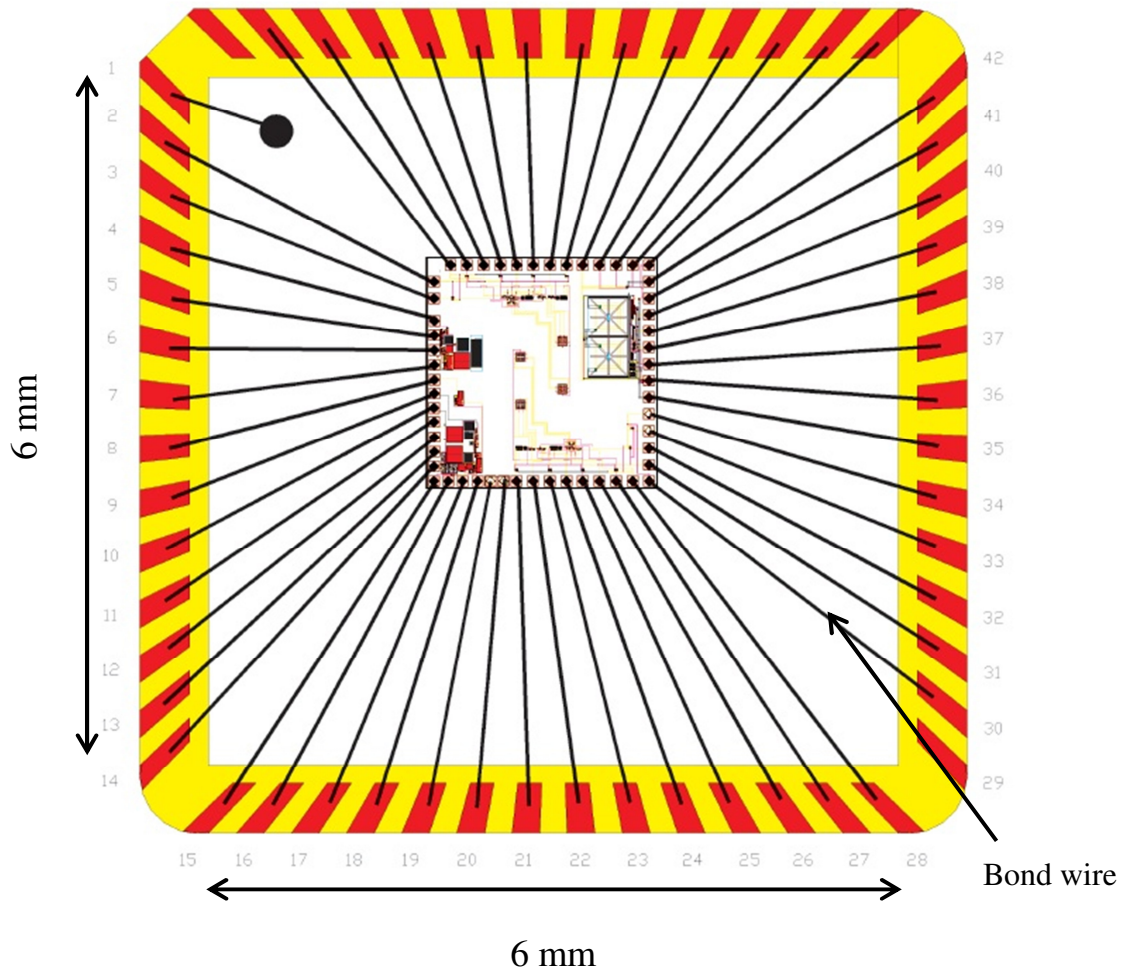
minimises transmission line losses and allows for the exposure required, as shown in Fig 5.7.1 below.



**Figure 5.7.1** QFN package used for the multi-project wafer

Fig. 5.7.1 illustrates the chosen QFN package. The final pin count was 52 and therefore a 56-pin package was used. The unused pins were not connected to any part of the wafer and left floating. Since this work operates at low frequencies, high frequency antenna and capacitive effects for this part of the chip do not pose a problem. To enable better coupling of the radiation, some of the samples were chosen to have a taped glass lid. Because of the size difference of the project wafer and the QFN package, bond wires were needed. Fig 5.7.2 depicts the bonding diagram for this package and wafer.



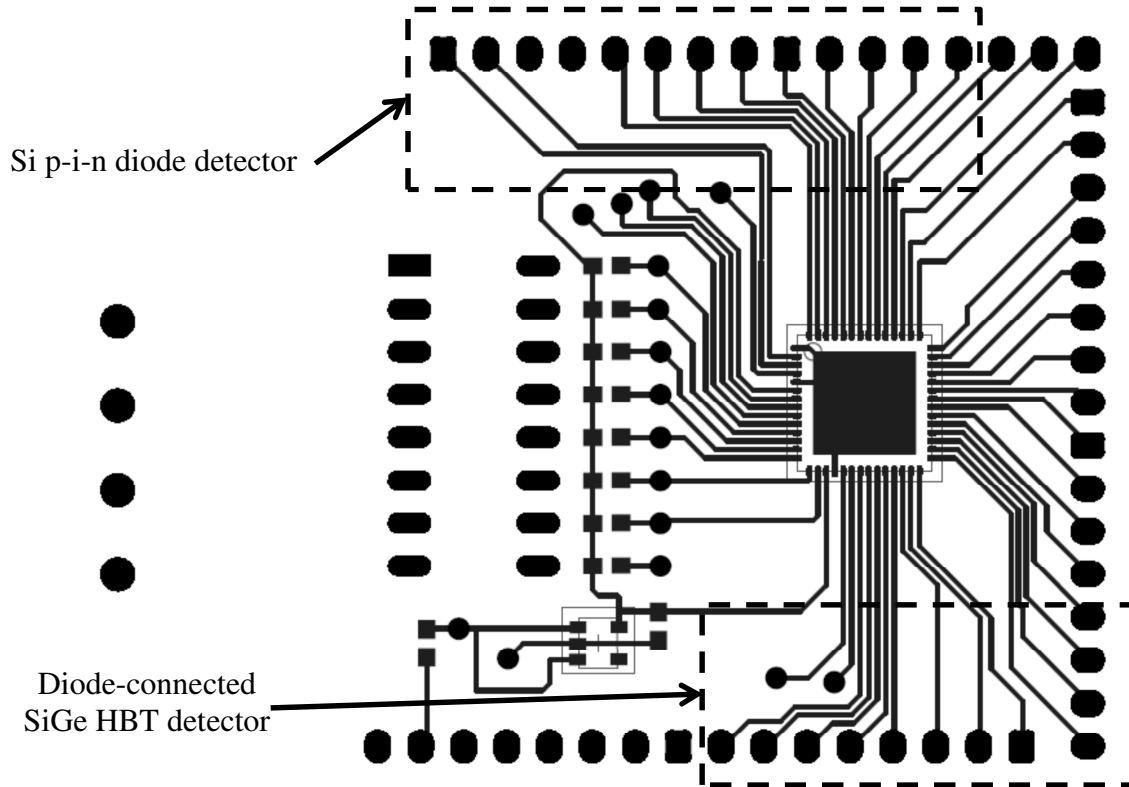


**Figure 5.7.2** Bonding diagram

Fig. 5.7.2 illustrates the bonding diagram of the MPW. The bond pad pitch is 50 μm. The bonding was done by the foundry.

## 5.8 PCB

Fig. 5.8 shows the fabricated PCB used for this research.

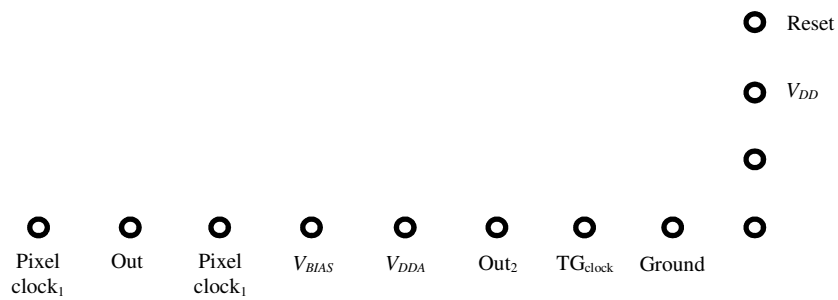


**Figure 5.8.1** Fabricated PCB used for this research

Fig. 5.8.1 shows the PCB used to mount the prototype. The top part is the link to the silicon p-i-n diode detector and the bottom part is the link to the diode-connected SiGe HBT detector. No special matching networks or transmission lines were required, since the work operates at “low” frequency (<1 GHz).

### 5.8.1 Diode-connected SiGe HBT detector pin outputs

Fig. 5.8.1 shows the specific pin outputs for the HBT detector.

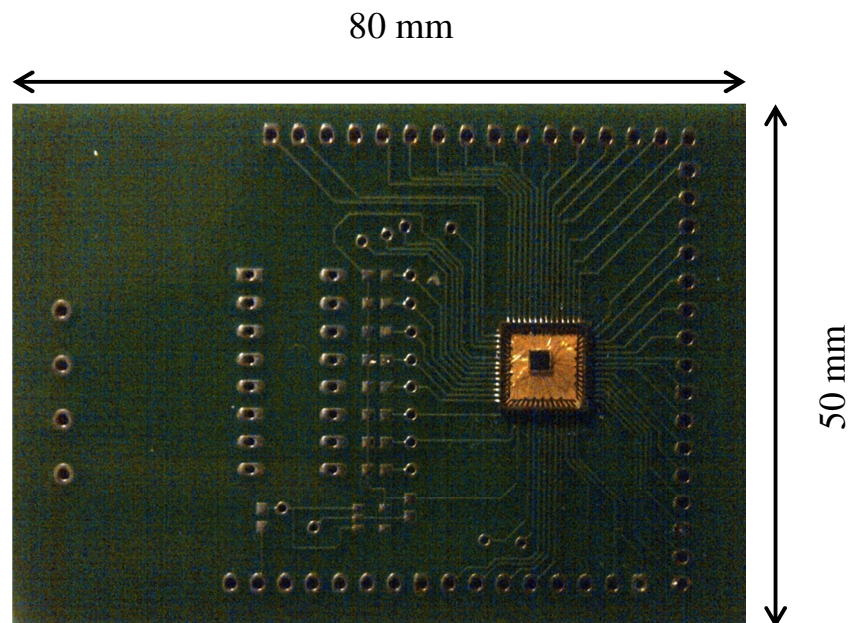


**Figure 5.8.1.1** HBT detector specific pin outs

Fig. 5.8.1.1 shows the specific pin outs on the PCB. These pins were connected to peripheral circuitry by means of single-core wires. The wire lengths were not of great concern in view of the operating frequency, but short wires were used. SMA and other specialised connectors were not needed, since the operating frequency was low (<1 GHz).

## 5.8.2 Actual manufactured PCB

Fig. 5.8.2.1 shows the actual manufactured PCB.

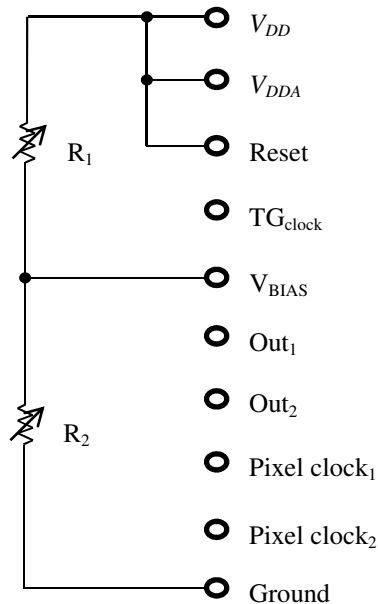


**Figure 5.8.2.1** Actual manufactured PCB

Fig. 5.8.2.1 shows the actual PCB used to perform the required measurements for this research. Not all of the pins seen were used, since some of the pins were linked to the other projects on the MPW.

### 5.8.3 External connections on the PCB.

Fig. 5.8.3.1 shows the external connections made to the PCB to bias the detector correctly.



**Figure 5.8.3.1** External PCB components and connections

Fig. 5.8.3.1 shows the external PCB components used and the pin layout. The rest of the pins were connected to peripherals such as oscillators, oscilloscopes, the monochromator and a signal analyser. Refer to section 3.6.5 for the actual setup. Simulations show that the optimal bias voltage fed into the  $V_{BIAS}$  is 1.7 V. The ratio of the voltage divider used was 0.5 to obtain a bias value of around 1.7 V. Since the value of the current drawn by the terminal,  $V_{BIAS}$ , is negligible in value and the detector should be protected from surge currents, resistor values in the  $k\Omega$  range were chosen.

A battery pack was used to bias the detector in most of the measurements to eliminate power supply voltage spikes produced by the 60 Hz 110 V US supply. In the case where an oscillator was needed, these spikes could not be avoided.

## 5.9 CONCLUSION

This chapter presented the layout of this research and some layout techniques associated with it. The packaging issues were discussed and the appropriate package was chosen. The final floor plan, including the bonding diagram, was also given.

# CHAPTER 6 EXPERIMENTAL RESULTS

## 6.1 INTRODUCTION

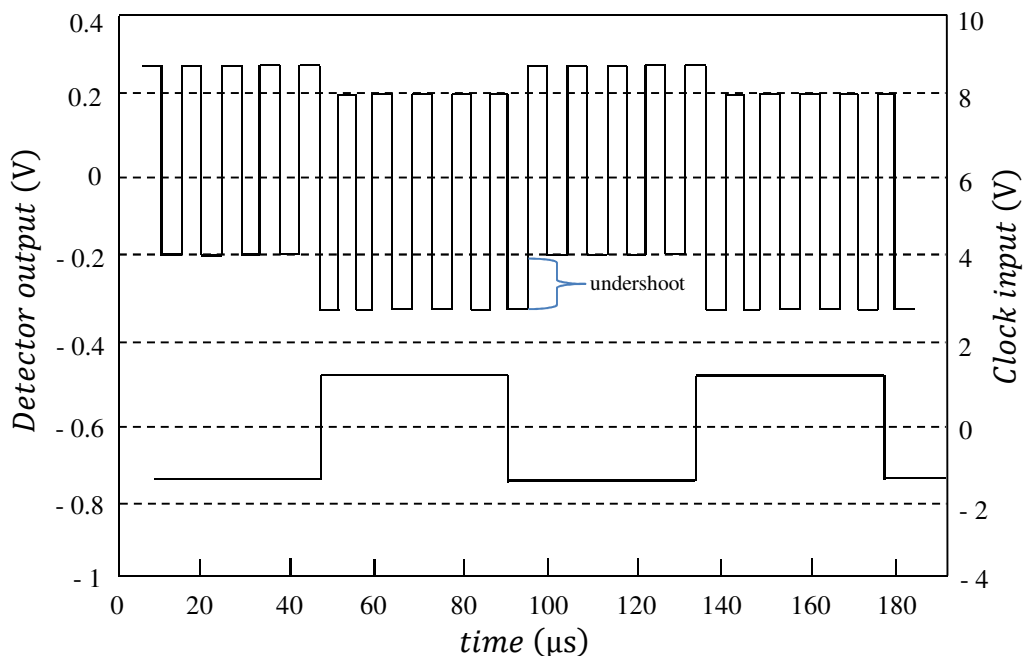
This chapter details the measured results obtained with the experimental implementation of this IR detector. The results were processed as far as possible to obtain a fair comparison to the simulated results in chapter 4. Time-domain, noise, DR and sensitivity results are presented in this chapter. The peripheral circuitry bias MOS transistor was set to 1.7 V to achieve the correct biasing conditions for the TIA. The separate supply pin ( $V_{DD_A}$ ) and the reset pin were connected to the global supply pin ( $V_{DD}$ ).

## 6.2 TIME-DOMAIN

The set of simulations depicted in this section shows the correct functionality of the IR detector.

### 6.2.1 Non-illuminated detector

Figure 6.2.1.1 depicts the time domain response of the IR detector with no illumination.

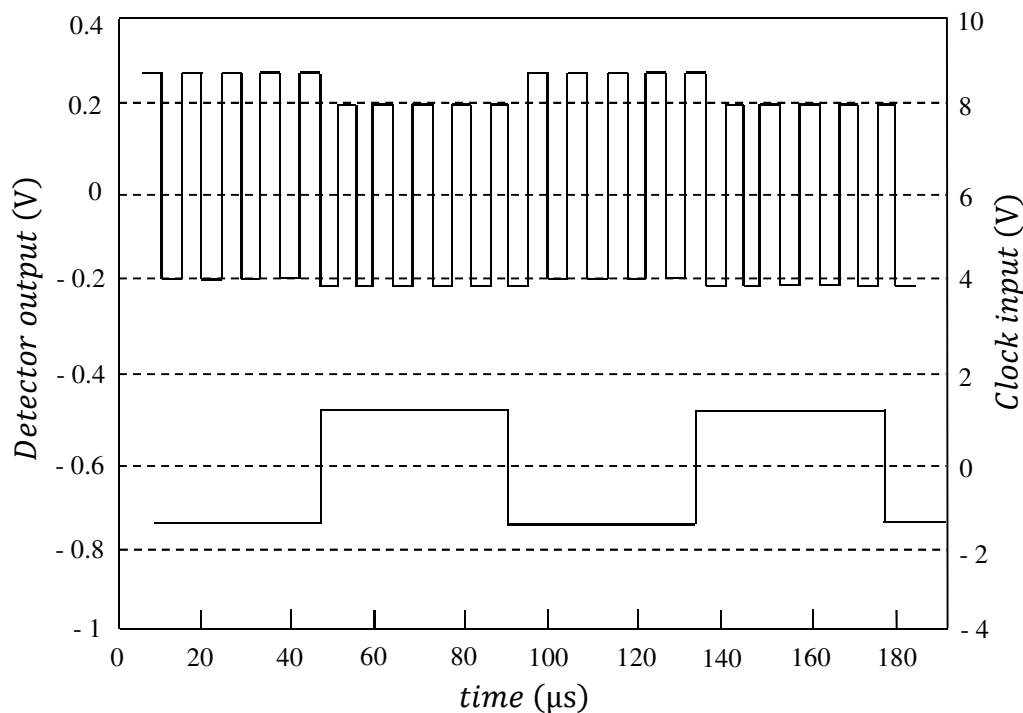


**Figure 6.2.1.1** Time domain response of the IR detector with no illumination (The figure was regenerated from an experimental photograph)

Fig. 6.2.1.1 shows the time domain output of the detector with no illumination. The lower signal is the TG's input signal. The detector should only feed the output through when the voltage input to the TG is high, which was the result. A slight direct current (DC) offset occurs between successive on and off states. Clock feedthrough was also observed, but this can be corrected with better readout circuitry. For this reason, the results presented in this section differ from those presented in section 4.8.2.

## 6.2.2 Illuminated detector

Figure 6.2.2.1 shows the time domain response of the detector when illuminated. The laser used for this experiment was one emitting radiation in the 630 nm to 680 nm band with a power output of 1 mW, which corresponds to an intensity of 31 mW/cm<sup>2</sup>.



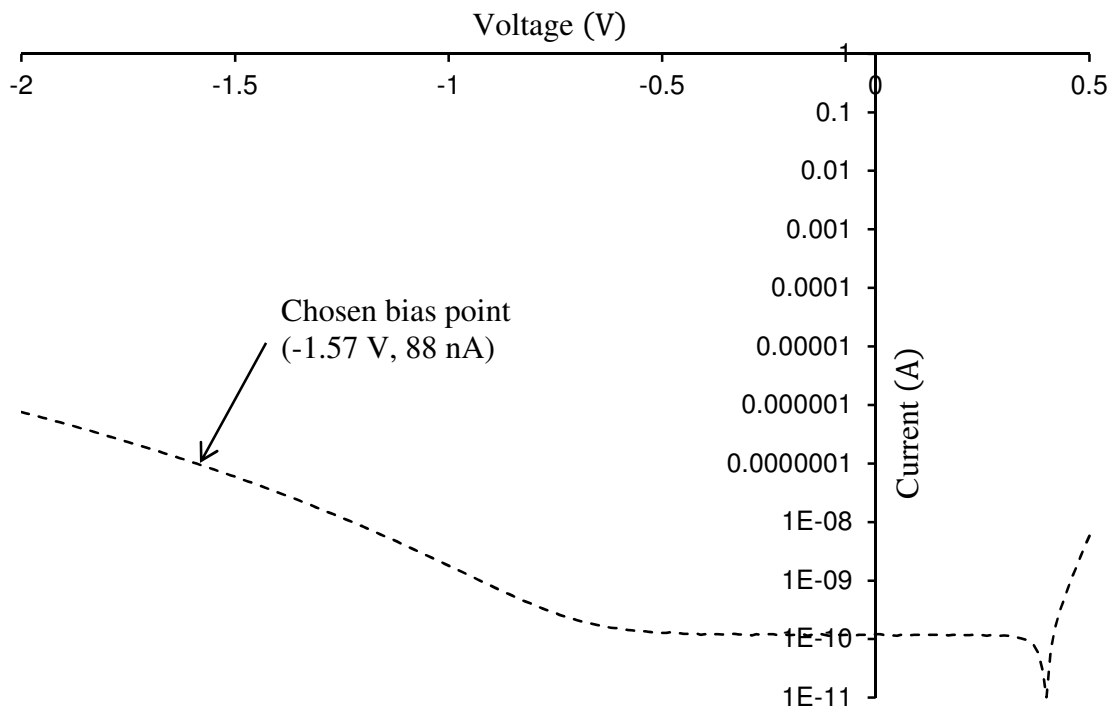
**Figure 6.2.2.1** Time domain response of detector with illumination

Fig. 6.2.2.1 shows the output of the detector when illumination is present. As can be clearly seen, when illumination is present, the bottom part of the output voltage signal increases in value and the total output voltage swing decreases. The undershoot shown in Fig. 6.2.1.1 is reduced. This was expected from the simulations shown in chapter 4. The amount of decrease in the total output voltage swing is a direct representation of the

intensity that the detector receives when illuminated. There is some correlation between these figures and the Figs 4.8.2.1, 4.8.2.2 and 4.8.2.3. The lack of correlation can be attributed to the clock feedthrough (section 4.8.2).

### 6.2.3 HBT I-V

Fig. 6.2.3.1 depicts the current-to-voltage (I-V) curve of a typical HBT of size  $14\ \mu\text{m} \times 6\ \mu\text{m}$ .

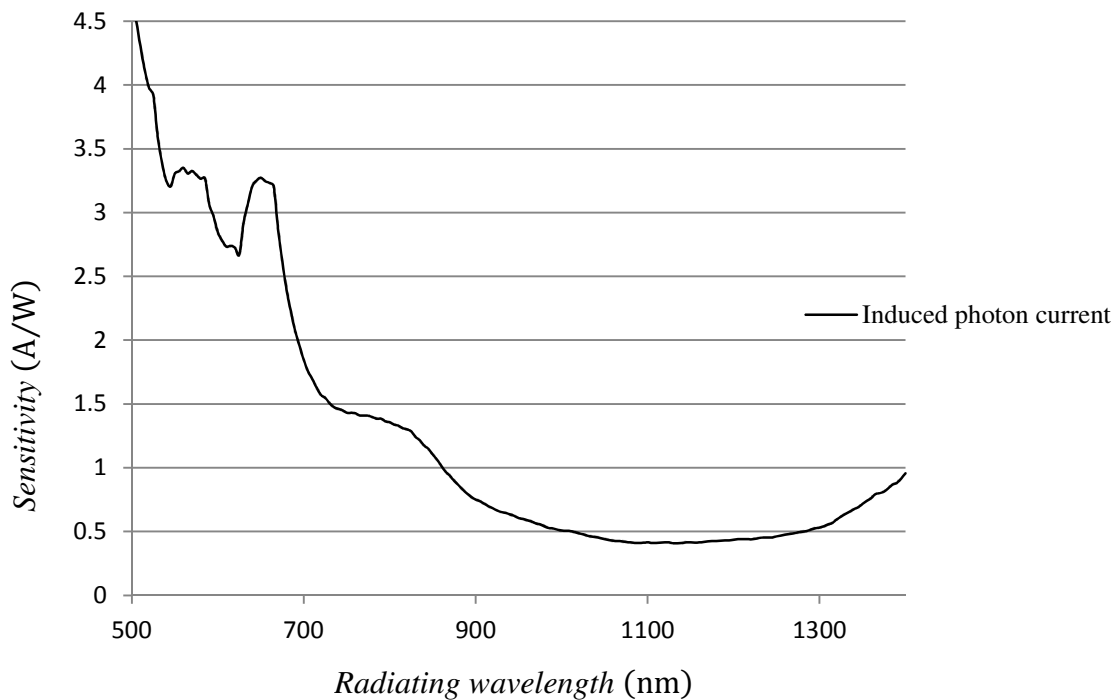


**Figure 6.2.3.1** I-V Curve of a  $14\ \mu\text{m} \times 6\ \mu\text{m}$  diode-connected HBT

Fig. 6.2.3.1 depicts the I-V curve of a diode-connected HBT. A bias voltage of 1.57 V reverse bias was chosen and the resulting load resistance was calculated to be  $2\ \text{M}\Omega$  to perform the required sensitivity measurements.

### 6.2.4 Sensitivity curve of the HBT

Fig. 6.2.4.1 depicts the current sensitivity of the HBTs only.



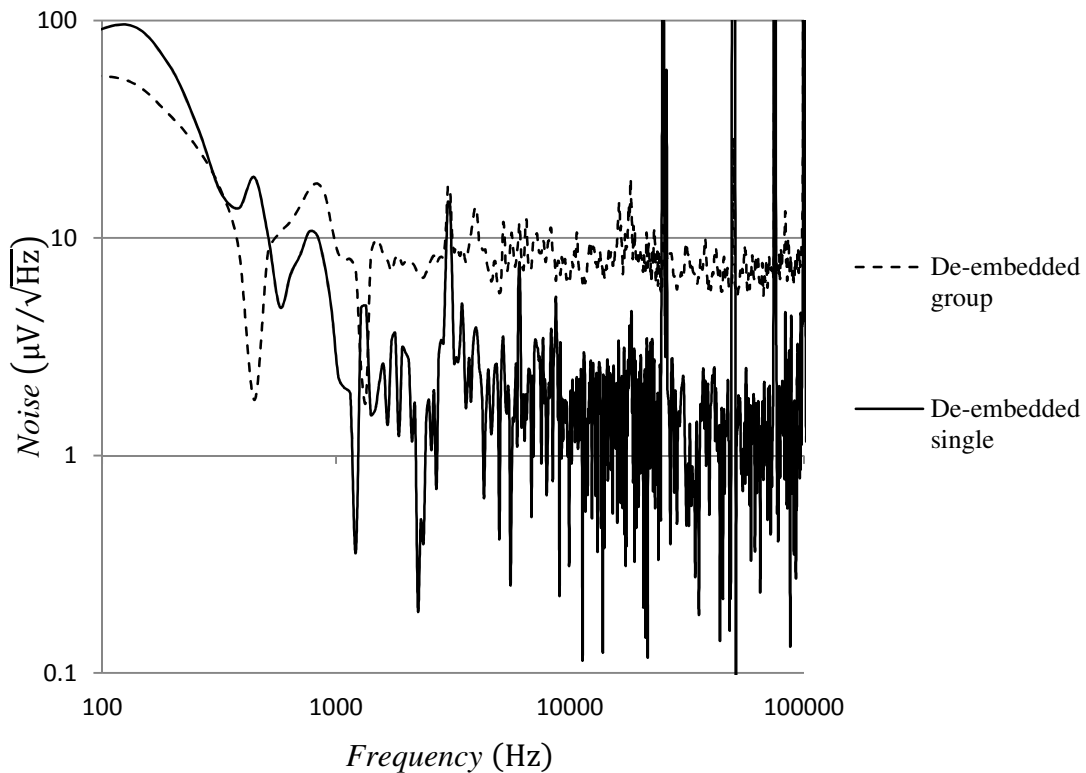
**Figure 6.2.4.1** Current sensitivity as a function of wavelength

Fig. 6.2.4.1 shows the current sensitivity of the HBT pixels only. This was measured by connecting the HBT in a diode connection and inserting this into a simple reverse biasing circuit with a 1 V reverse bias voltage supply and the load resistor of 2 M $\Omega$ . These values were chosen from the I-V curve Fig. 6.2.3.1. This is also a representation of the induced photon current per watt of incident light. The spikes seen between 500 nm and 700 nm are the result of filter changes of the monochromator. The slight change in pattern seen between 700 nm and 900 nm is due to the germanium content in the HBT, which shifts the sensitivity curve, as seen in chapter 4. The rise seen above 1200 nm is the second order harmonics, which produce current at higher wavelengths. This is not as a result of the HBT that is sensitive at higher wavelengths. An arbitrarily selected radiation filter was placed over the detector, filtering out all radiation with a wavelength lower than 1600 nm. No response was observed from the HBT other than the response due to noise in the system.

### 6.3 NOISE

The de-embedded noise values of this IR detector were measured with the setup as shown in chapter 3. Fig. 6.3.1 shows the noise measurement of both detector topologies.





**Figure 6.3.1** De-embedded noise of IR detector

Fig. 6.3.1 shows the resulting output noise voltage of the two different IR detector topologies. The pixels grouped together with one output amplifier exhibit more noise than the pixels with each one a separate output amplifier. This can be attributed to the noise accumulating from each of the other of pixels when one of the pixels is read. The sudden drop from 100 Hz to 800 Hz is due to the system which only settles then. The starting frequency was chosen at 100 Hz because of the noise being generated at higher frequencies where parasitic capacitances influence the noise spectra. This increase in noise is due to the noise being generated from the material itself.

The sudden noise spikes at 20 kHz, 60 kHz, 74 kHz and 100 kHz can be attributed to the noise contribution from the oscillator.

#### 6.4 DYNAMIC RANGE

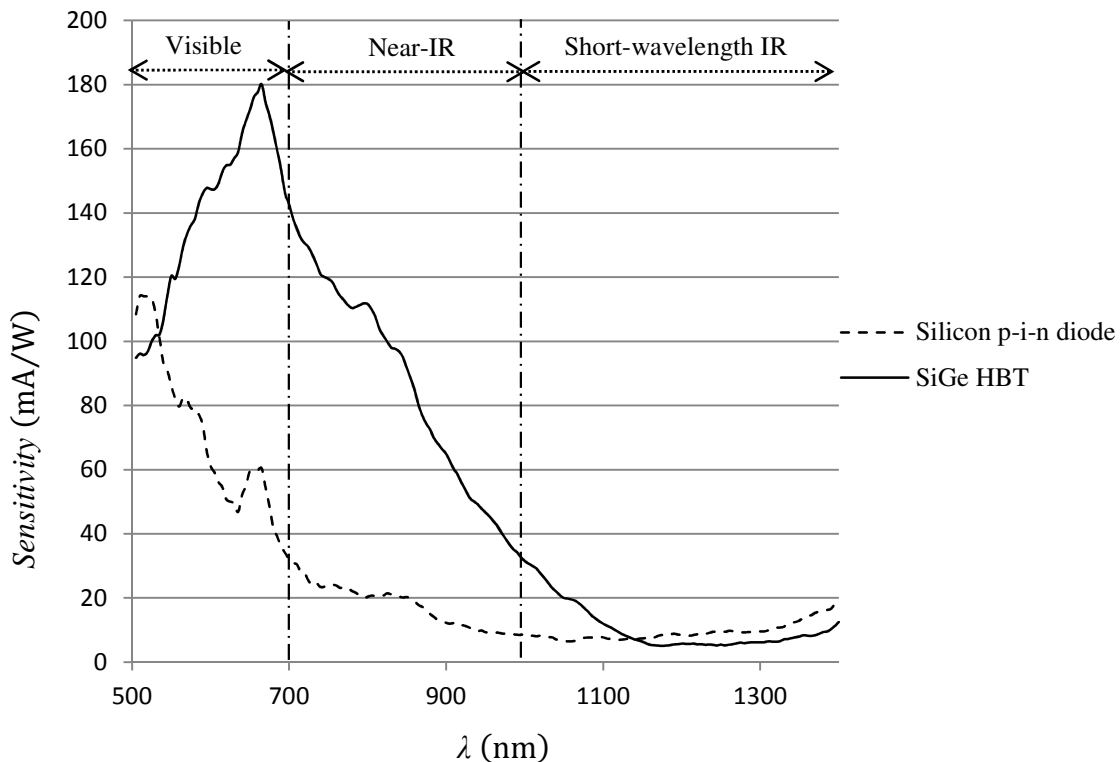
The DR was calculated using (2.8.3) and the measured values are listed below.

- $V_{MAX} - V_{DARK} = 117 \text{ nV}$

- Noise values in Fig. 6.4.1 were used. The total noise is defined in (2.8.3). The reset pin was tied to  $V_{CC}$  and therefore no reset noise was present during measurements. A value of 70 dB was recorded for the DR.

## 6.5 SENSITIVITY

Fig. 6.5.1 shows the sensitivity of the detector.

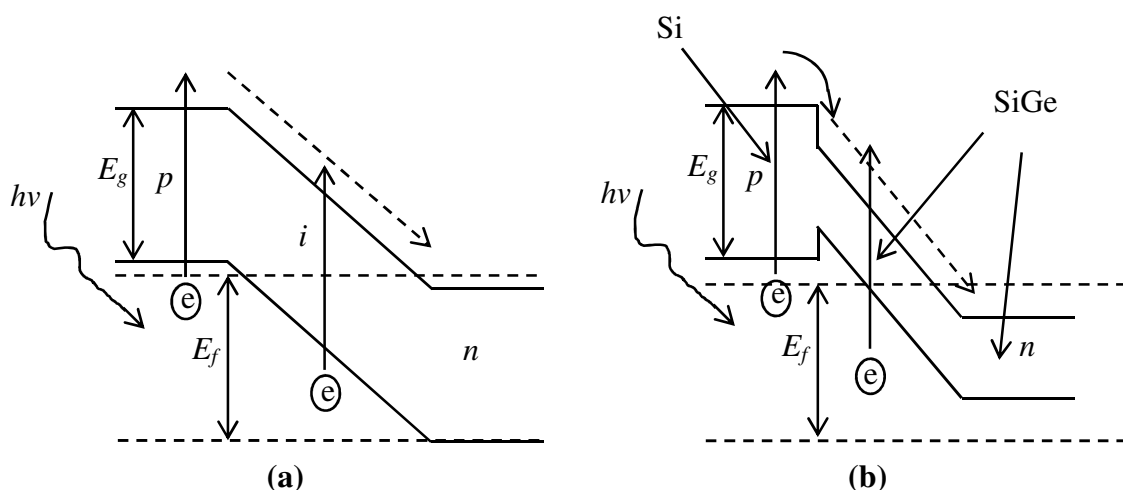


**Figure 6.5.1** Sensitivity curve of the IR detector

Fig. 6.5.1 shows the sensitivity of the IR detector. The visible band of the light spectrum ends at 700 nm where the IR band starts. Fig. 6.5.1 shows that this detector detects a lower band in terms of wavelength in the near-IR range. The other part of this chip contained the same peripheral circuitry, the only difference being that it contains silicon p-i-n diodes instead of SiGe HBTs. The same sweep was performed and the resulting sensitivity curve is given in Fig. 6.5.1. The results show that there is no real response in the IR band. The second rise is the second order harmonics of the visible range. The spikes seen in the silicon p-i-n diode occur (as the HBT pixel measurement shown in Fig. 6.2.4.1) as a result of filter changes. This is not seen in the HBT detector owing to the high gain of the HBTs.

Comparing Fig. 6.5.1 with Fig. 4.8.5.1, it is experimentally verified that the detecting band indeed detects partially in the IR band. Other detectors published in literature shown in Tables I and II show detectors with a sensitivity of 5 kV/W (or 50 mA/W). The results show a maximum sensitivity of 180 mA/W. It also shows improvement in sensitivity and DR. Mapping this figure directly onto Fig. 4.8.5.1 shows that the response obtained is that of Si only. The samples used of which the experimental values were obtained exhibited a Ge fraction in the complete wafer, as opposed to small doping, which was used in this research. Nonetheless, the required shift could be illustrated using the same wafer, which eliminates factors such as these.

This phenomenon of shift in detecting can be explained by the band gap energy curves of both detectors. Figures 6.5.2 (a) and (b) depict the band gap energy curves of both detectors.



**Figure 6.5.2** Band gap diagrams of the (a) silicon p-i-n diode detector and the (b) SiGe diode-connected HBT IR detector

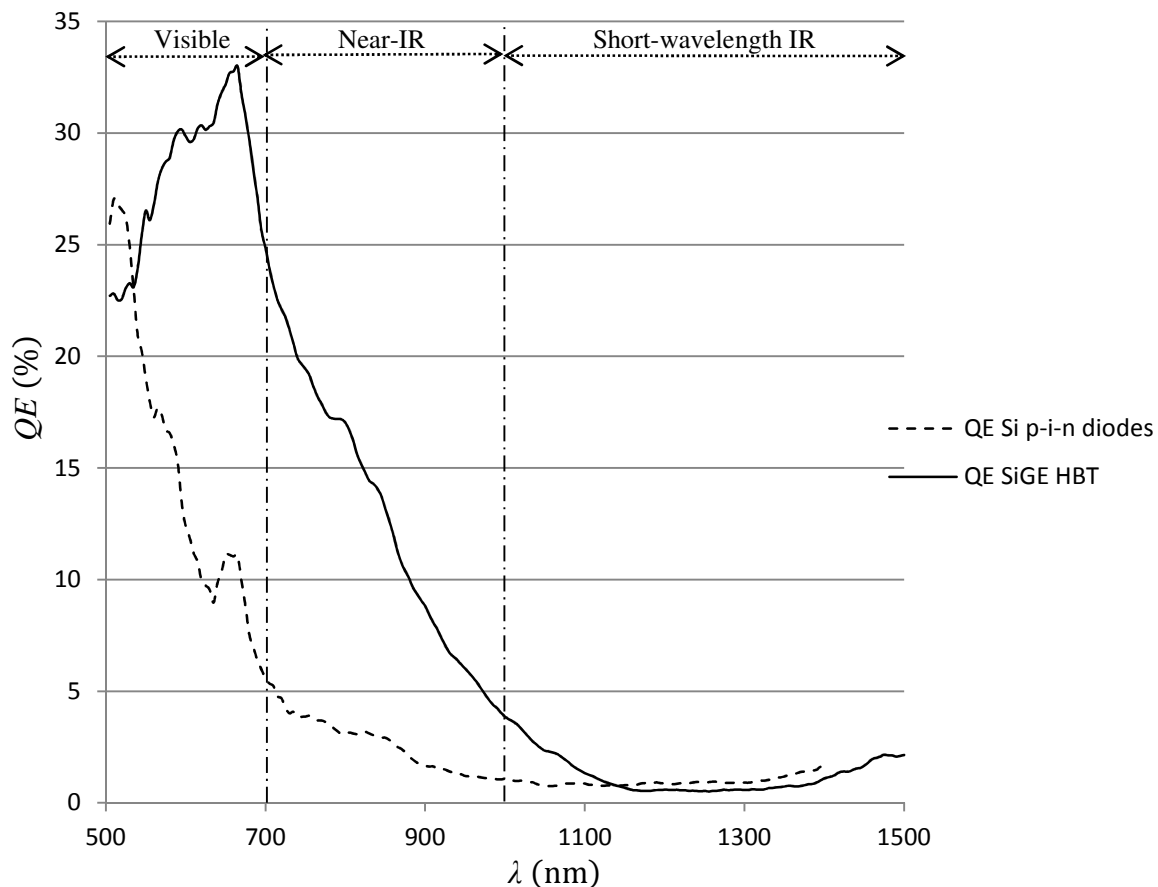
The band gap diagram of a silicon p-i-n diode detector is given in Fig. 6.5.2 (a). The flat band and high band gap energy makes an efficient detector in the visible band. The IR band requires lower photon energy and therefore silicon will not detect in the IR range owing to the lower photon energy available in the IR band. Fig. 6.5.2 (b) shows the band gap diagram of a diode-connected SiGe HBT detector. The added germanium in the base

of the detector lowers the band gap energy and therefore electrons are released with lower photon energy compared to silicon p-i-n diodes.

The results show a shift in detecting band for the SiGe HBT towards the IR range. It still cuts off before the middle of the near-IR band but this shows promising improvements towards IR imaging using SiGe HBT structures.

## 6.6 QE

Fig. 6.6.1 shows the QE of the prototyped detectors.



**Figure 6.6.1** QE versus wavelength of prototyped detectors

Fig. 6.6.1 shows the QE of the prototyped detectors. A maximum QE of 30 % at 665 nm radiation was recorded. The prototyped detector shows comparable performance in the IR band compared to the CCD equivalent of IR detectors. Comparing this to the simulated QE in Fig. 4.8.4.1 shows 100 % correlation in the detecting band but a significant increase in

QE. Fig. 4.8.4.1 shows the QE of the detecting material only (also shown in literature [11]). However Fig. 6.6.1 shows the detecting material QE with *post-processing* with a 30-fold improvement.

## 6.7 CONCLUSION

This chapter presented the measured results of the detector. A shift towards the IR band is shown in the results, which makes the 0.35  $\mu\text{m}$  SiGe BiCMOS viable to develop IR detectors. The results showed improvements in DR, sensitivity and QE compared to previously published work.

# CHAPTER 7 CONCLUSION

## 7.1 INTRODUCTION

This chapter concludes the research conducted and critically evaluates the hypothesis, taking into account the results obtained in the experimental verification. Chapter 1 presented an introduction to this research and the formulation of the hypothesis. Chapter 2 presented a literature study of the fundamental theory needed to understand the characteristics of IR detectors, as well as factors that influence the parameters thereof. The research focussed on improving DR and sensitivity in IR detectors by using SiGe BiCMOS technology instead of CCD technology. The specific application addressed in this research is for the purpose of IR detectors. The research methodology used in this research is presented in chapter 3. This methodology was used to validate the hypothesis in question experimentally. Chapter 4 presented the IR detector design and simulated the IR detector in software, as well as the simulations performed to verify the correct functioning of the IR detector and gaining information on the expected parameters, namely noise, DR and sensitivity. Chapter 5 outlined the layout of the IR detector and the layout considerations that affected the design of the IR detector. Chapter 6 detailed the results obtained by measuring the IR detector's performance in the experimental setup with the signal analyser and monochromator. The comparison of these results to the simulations is also given in this chapter.

## 7.2 VERIFICATION OF THE HYPOTHESIS

The following is a list of findings from this research that verify the hypothesis in question.

- The time and frequency measurements obtained correlated with the simulations in section 4.8 as described in the acceptance criteria column of Tables V and VI. However, these require more processing to eliminate not only the clock feed-through experienced when the TG is off, but also to provide a voltage output signal, which will make the post-processing much easier.
- The increased DR and sensitivity were due to the  $\beta$ -multiplication effect of the Ge doping in the base of the HBT. It is difficult to estimate the germanium doping when comparing Fig. 6.5.1 with Fig. 4.8.5.1 since the measured curve depicts Ge

content only. The simulated results are those of SiGe samples where the Ge content is increased proportionally whereas the measured results are a Si-SiGe combination. Nonetheless it shows the required shift.

- The diode-connected SiGe HBT detector showed improved sensitivity from the end of the visible band to around the middle of the near-IR band. The sensitivity is larger than that of the IR CCD detector in the band of transmission but the IR CCD detector still detects photons in the near to mid-wavelength-IR band, which the SiGe HBT transistor does not do. A shift is exhibited in the radiation band from the visible range, where silicon is most prominent, to the IR range where SiGe HBTs seems to be a viable structure and material for detection.
- The grouping of pixels increases the fill factor of an IR detector, at a cost of increased noise.
- The overall processing of photon-induced current to a voltage output seems to be efficient. An SNR value of 74 dB was obtained.
- The experimental results shown in this dissertation are only for an input clock frequency up to 100 kHz. Above this, significant degradation is seen at the output in the form of a smaller voltage output. The simulations show ideal output at 80 MHz input clock frequency. Other factors that contribute to the input and output ports were not taken into consideration in the simulations, for example input and output matching of the impedances, which could degrade the performance, as well as losses occurring in the processing of the induced photon current.

### 7.3 SHORTCOMINGS

The equations given in literature and the simulations thereof only provide an estimation of the DR and sensitivity of the IR detector. The measured results were used to compare the performance of the IR detector with other results in literature.

The sensitivity measurements were only performed from 500 nm wavelength to 1500 nm. These were the available sources in the laboratory, including at GSU. The calibration curve of only this band was available. Other gratings are available, but the calibration curves are not available.

The reset pin was tied to the supply voltage, since only two oscillators were available. For this IR detector to function properly, three oscillators were needed. The impact of this is that reset noise was not included in the measurements.

A battery of cells was used as the supply with a potentiometer that eliminated the 60 Hz spike (US power supply). The resistor added noise to the detector, which could not be de-embedded.

#### **7.4 POSSIBLE FUTURE WORK**

Better pixel structures can be used to shift the detecting band more towards the IR region. The addition of the germanium doping in the base of the HBT shifts the band to the IR region, but not completely. A possible structure that could be considered is sandwiched SiGe structures, as opposed to the diode-connected SiGe. There are other materials that will detect radiation in the infrared band, but it is very difficult to integrate those materials on-chip with conventional Si technology.

The peripheral circuitry needs be analysed to determine which parameters can be improved to increase the speed of the IR detector. Optimising the structure for this processing should increase the output speed. Further improvements can be made to increase the performance of these detectors by fully optimizing the peripheral circuitry. The gated concept can also be implemented and upscaled to larger arrays.



## REFERENCES

- [1] G. E. Smith, "The invention and early history of the CCD," *Nucl. Instruments Methods Phys. Research, section A*, vol. 607, no. 1, pp. 1-6, Aug 2009.
- [2] B. Rodricks, B. Fowler, C. Liu, J. Lowes, D. Haeffner, U. Lienert and J. Almer, "A CMOS-based large-area high-resolution imaging system for high-energy X-ray applications," *Hard X-Ray, Gamma-Ray, and Neutron Detector Physics X, Proc. of SPIE, The Int. Society for Optical Engineering*, San Diego, vol. 7079, pp. 14, 10 Aug. 2008.
- [3] H. Fan, F. Cui, W-J. Xu, Y-Z. Wu and R-H. Qiu, "Research of noise reduction and non-uniformity correction for CMOS image sensor," *Int. Symp. on Photo-electronic Detection and Imaging, Proc. of SPIE, The Int. Society for Optical Engineering*, San Francisco, vol. 7384, pp. 23, 17 Jun. 2009.
- [4] S. Kawahito, "Circuit and Device Technologies for CMOS Functional Image Sensors," *Proc. of 2006 IFIP Int. Conf. on Very Large Scale Integration*, Nice, pp. 42-47, 16-18 Oct. 2006.
- [5] N. Bassler, "Radiation Damage in Charge-Coupled Devices," *Radiation, Environment and Biophysics*, vol. 49, no. 3, pp. 373-378, 18 Mar. 2010.
- [6] R. Accorsi, "20  $\mu\text{m}$  Resolution Imaging of Soft X-ray Emitters," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 3, pp. 889-897, Jun. 2008.
- [7] H. Lee, T. Madden, P. Fernandez, B. Lee, S. Seifert, J. Weizeorick and M. Molitsky, "Kodak CCD-based Detector for Small Angle X-Ray Scattering," *IEEE Nucl. Sci. Symp. Conf. record*, Orlando, pp.1807-1810, 24 Oct. – 1 Nov. 2009.
- [8] A. Rogalski, "Infrared detectors: status and trends," *Progress in Quantum Electronics*, vol. 27, no. 2-3, pp. 59-210, 23 May 2003.
- [9] S. Eminoglu, M.Y. Tanrikulu and T. Akin, "A Low-Cost 128x128 Uncooled Infrared Detector Array in CMOS Process," *J. of Microelectromech. Syst.*, vol. 17, no. 1, pp. 20-30, Feb. 2008.
- [10] S. Yang, K. Kim, E. Kim, K-B. Baek and S. Kim, "An Ultra Low-Power CMOS Motion Detector," *IEEE Trans. Consum. Electron.*, vol. 55, no. 4, pp. 2425-2430, Nov. 2009.

- 
- [11] M. Bass, *Handbook of Optics, Fundamentals, Techniques and Design*, 2nd ed., vol. 1, *McGraw-Hill Access Engineering*, Sep. 2004.
- [12] A. Theuwissen, “CMOS Image Sensors: State-Of-The-Art and Future Perspectives,” *Proc. of 33rd European Solid-State Device Research Conf.*, Munich, pp. 21 – 27, 11-13 Sep. 2007.
- [13] F. Corsi, M. Foresta, C. Marzocca, G. Mataressa and A. Del Guerra, “Current Mode Front-End Electronics for Silicon Photo-Multiplier Detectors,” *Int. Workshop on Advances in Sensors and Interface*, Bari, pp. 1-6, 26-27 Jun. 2007.
- [14] N. Viarani, N. Liberatore, A. J. Syed, M. Gottardi, N. Massari, C. Corsi and A. Baschiroto, “A 16 cell 80dB Dynamic-Range Auto-Ranging Read-Out Array for Uncooled IR Micro-Bolometers,” *Int. Conf. on Solid-state Sensors, Actuators and Micro-systems*, Lyon, pp. 1361-1364, 10-14 Jun. 2007.
- [15] A. Peizerat, A. Martin, M. Tchagaspanian and V. Nguyen, “Auto-adaptative LSB technique for in-pixel analog to digital conversion,” *Int. Conf. for Sensors, Cameras and Systems for Industrial/scientific Applications IX, Proc. of SPIE, The Int. Society for Optical Engineering*, San Jose, vol. 6816, 29 Jan. 2008.
- [16] R. Yun and V. M. Joyner, “A Monolithically Integrated Phase-Sensitive Optical Sensor for Frequency-Domain NIR Spectroscopy,” *IEEE Sensors J.*, vol. 10, no. 7, pp. 1234-1242, Jul. 2010.
- [17] R. Berger, D. D. Rathman, B. M. Tyrrell, E. J. Kohler, M. K. Rose, R. A. Murphy, T. S. Perry, H. F. Robey, F. A. Weber, D. M. Craig, A. M. Soares, S. P. Vernon and R. K. Reich, “A 64 × 64-Pixel CMOS Test Chip for the Development of Large-Format Ultra-High-Speed Snapshot Imagers,” *IEEE J. of Solid-State Circuits*, vol. 43, no. 9, pp. 1940-1950, Sept. 2008.
- [18] C. Li, F. Gong and P. Wang, “A Low-Power Ultrawideband CMOS Power Detector With an Embedded Amplifier,” *IEEE Trans. on Instrumentation and Measurement*, vol. 59, no. 12, pp. 3270-3278, Dec. 2010.
- [19] F. Schuster, D. Coquillat, H. Videlier, M. Sakowicz, F. Teppe, L. Dussopt, B. Giffard, T. Skotnicki and W. Knap, “Broadband terahertz imaging with highly sensitive silicon CMOS detectors,” *Optics Express*, vol. 19, no. 8, pp. 7827-7832, Apr. 2011.

- 
- [20] M. Fanzhong, Z. Yiqiang, J. Junwei, Q. Ming and W. Gaofeng, “Analysis and Design of a High Performance Infrared Detector Readout Circuit,” *Proc. of the 2009 12th Int. Symp. on Integrated Circuits*, Singapore, pp. 605 – 608, 14-16 Dec. 2009.
- [21] A. Rogalski, “Infrared detectors: an overview,” *Infrared Phys. & Tech.*, vol. 43, no. 3-5, pp.187-210, Jun. 2002.
- [22] R. W. Wagant, “Electro-optics Handbook”, 2nd ed., chapter 16, p. 10. *McGraw-Hill Access Engineering*, 2000.
- [23] M. Perenzoni, N. Massari, D. Stoppa, L. Pancheri, M. Malfatti and L. Gonzo, “A 160 × 120-Pixels Range Camera With In-Pixel Correlated Double Sampling and Fixed Pattern Noise Correction,” *IEEE J. of Solid-State Circuits*, vol. 46, no. 7, pp. 1672-1681, Jul. 2011.
- [24] H. Cheng, B. Choubey and S. Collins, “An Integrating Wide Dynamic Range Image Sensor With a Logarithmic Response,” *IEEE Trans. on Electron Devices*, vol. 56, no. 11, pp. 2423-2428, Nov. 2009.
- [25] V. Gruev, Z. Yang, J. van der Spiegel and R. Ettiene-Cummings, “Current Mode Image Sensor With Two Transistors per Pixel,” *IEEE Trans. on Circuit and Systems I*, vol. 57, no. 6, pp. 1154-1165, Jun. 2010.
- [26] F. Tang and A. Bermak, “A 4T Low-Power Linear-Output Current-Mediated CMOS Image Sensor,” *IEEE Trans. on VLSI Syst.*, vol. 19, no. 9, pp. 1559-1568, Sep. 2011.
- [27] D. Lin, C. Wang and C. Wei, “Quantified Temperature effect in a CMOS Image Sensor,” *IEEE Trans. on Electron Devices*, vol. 57, no. 2, pp. 422-428, Feb. 2010.
- [28] A. G. U. Perera, G. Ariyawansa, M. B. M. Rinzan, M. Stevens, M. Alevli, N. Dietz, S. G. Matsik, A. Asghar, I. T. Ferguson, H. Luo, A. Bezinger and H. C. Liu, “Performance improvements of ultraviolet/infrared dual-band detectors,” *Infrared Phys. & Tech.*, vol. 50, no.2-3, pp. 142-148, Apr. 2007.
- [29] T. Morf, J. Weiss, L. Kull, H. Rothuizen, T. Toifl, M. Kossel, C. Menolfi, G. von Bueren, T. Brunswiler and M. Schmatz, “Antenna coupled far-infrared/THz detector in CMOS,” *Electron. Lett.*, vol. 45, no. 25, pp. 1321-1323, 3 Dec. 2009.

- 
- [30] W-H. Lin, C-C. Tseng, K-P. Chao, S-Y. Kung, S-Y. Lin and M-C. Wu, "Broadband Quantum-Dot Infrared Photodetector," *IEEE Photonics Technol. Lett.*, vol. 22, no. 13, pp. 963-965, 1 Jul. 2010.
- [31] S. G. Chio, T-J. Ha, B-G. Yu, S. P. Jaung, O. Kwon and H-H. Park, "Improvement of uncooled infrared imaging detector by using mesoporous silica as a thermal isolation layer," *Ceramics International*, vol. 34, no. 4, pp. 833-836, May 2008.
- [32] A. Bocci, A. Marcelli, E. Pace, A. Drago, M. Piccinini, M. Cestelli Guidi, A. de Sio, D. Sali, P. Morini and J. Piotrowski, "Fast infrared detector for beam diagnostics with synchrotron radiation," *Nucl. Instruments Methods Phys. Research, section A*, vol. 580, no. 1, pp. 190-193, 21 Sep. 2007.
- [33] C. Peiyi, "Development of SiGe materials and devices," *Int. Conf. on Solid-state and Integrated Circuit Technology*, Shanghai, vol. 1, pp. 570-574, 22-25 Oct. 2001.
- [34] P. Magnan, "Detection of visible photons in CCD and CMOS: A comparative view," *Nucl. Instruments Methods Phys. Research, section A*, vol. 504, nos. 1-3, pp. 199-212, May 2003.
- [35] B. Gosselin and M. Sawan, "An Ultra Low-Power CMOS Automatic Action Potential Detector," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 17, no. 4, pp. 346-353, 11 Aug. 2009.
- [36] D. Litwiller, "CCD vs. CMOS: Facts and fiction," *Photonics Spectra*, vol. 35, no. 1, pp. 154-158, Jan. 2001.
- [37] A. El Gamal and H. Eltoukhy, "CMOS image sensors," *IEEE Circuits and Devices Magazine*, vol. 21, no. 3, pp. 6 – 20, Jun. 2005.
- [38] O. Fidaner, A. K. Okyay, J. E. Roth, R. K. Schaevitz, Y-H. Kuo, K. C. Saraswat, J. S. Harris Jr. and D. A. B. Miller, "Ge – SiGe Quantum-Well Waveguide Photodetectors on Silicon for the Near-Infrared," *IEEE Photonics Tech. Lett.*, vol. 19, no. 20, pp. 1631-1633, 15 Oct. 2007.
- [39] S. Komiyama, "Single-Photon Detectors in the Terahertz Range," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 1, pp. 54-66, Feb. 2011.
- [40] S. Dvorestky, N. Mikhailov, Y.U. Sidorov, V. Shvets, S. Danilov, B. Wittman and S. Ganichev, "Growth of HgTe Quantum Wells for IR to THz Detectors," *J. of Electronic Materials*, vol. 39, no. 7, pp. 918-923, 13 Apr. 2010.

- 
- [41] P. Martin-Gonthier, P. Magnan, F. Corbiere, M. Estribeau, N. Huger and L. Boucher, "Dynamic range optimisation of CMOS image sensors dedicated to space applications," *9<sup>th</sup> Conf. on Sensors, Systems and Next-generation Satellites, Proc. of SPIE, The Int. Society for Optical Engineering*, Florence, vol. 6744, 17 Sep. 2007.
- [42] I. Berbezier and A. Rhonda, "Si/SiGe heterostructures for advanced microelectronic devices," *Phase Transitions*, vol. 81, no. 7-8, pp. 751-772, Jul. 2008.
- [43] F. Schwierz, "SiGe HBTs for Ultra-High Speed Applications," *7<sup>th</sup> Int. Conf. on Solid-state and Integrated Circuit Technology*, Beijing, vol. 3, pp. 2114-2119, 17-21 Oct. 2004.
- [44] H. K. Gummel and H. C. Poon, "An integral charge control model of bipolar transistors," *Bell Labs. Tech. J.*, vol. 49, pp. 827-852, May 1970.
- [45] C. C. McAndrew, M. Dunn, S. Moinian and M. Schröter, "VBIC95, The vertical bipolar inter-company model," *IEEE J. of Solid-State Circuits*, vol. 31, no. 10, pp. 1476-1482, Oct. 1996.
- [46] O. Bazkir, "Quantum efficiency determination of unbiased silicon photodiode and photodiode based trap detectors," *Rev. Adv. Mater. Sci.*, vol. 21, no. 1, pp. 90-98, Jun. 2009.
- [47] K. S. Lai, J. C. Huang and K. Y. J. Hsu, "Design and Properties of Phototransistor and Photodetector in Standard 0.35- $\mu$ m SiGe BiCMOS Technology," *IEEE Trans. on Electron Devices*, vol. 55, no. 3, pp. 774-781, Mar. 2008.
- [48] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analogue Integrated Circuits*, 4<sup>th</sup> Ed, Wiley, John and Sons, Incorporated, Jan. 2001.
- [49] G. Huang and V. Fusco, "60 GHz wide tuning range SiGe bipolar voltage controlled oscillator for high definition multimedia interface and wireless docking applications," *IET Microwaves, Antennas and Propagation*, vol. 5, no. 8, pp. 934-939, Jan. 2011.

- 
- [50] Y-J. Moon, Y-S. Roh, C-Y. Jeong and C-Y. Yoo, "A 4.39-5.26 GHz LC-tank CMOS Voltage-Controlled Oscillator With Small VCO-Gain Variation," *IEEE Microwave and Wireless Components Lett.*, vol. 19, no. 8, pp. 524-526, Aug. 2009.
- [51] C-Y. Yang, C-H. Chang, J-M. Lin and H-Y. Chang, "A 20/40 GHz Dual-Band Voltage-Controlled Frequency Source in 0.13  $\mu\text{m}$  CMOS," *IEEE Trans. on Microwave Theory and Techniques*, vol. 19, no. 8, pp. 2008-2016, Aug. 2011.
- [52] J-J. Kuo, Z-M. Tsai, P-C. Huang, C-C. Chiong, K-Y. Lin and H. Wang, "A Wide Tuning Range Voltage-Controlled Oscillator Using Common-Base Configuration and Inductive Feedback," *IEEE Microwave and Wireless Components Lett.*, vol. 19, no. 10, pp. 653-655, Oct. 2009.
- [53] Y. Chen, M. Du Plessis, "An integrated CMOS optical receiver with clock and data recovery circuit," *Microelectronics Journal*, vol. 37, no. 9, pp. 985-992, Sept. 2006.
- [54] *Optical properties of SiGe and Ge* [online]. Available: <http://www.virginiasemi.com/pdf/Optical%20Properties%20of%20SiGe%20and%20Ge.pdf>.
- [55] ams AG, "0.35  $\mu\text{m}$  CMOS C35 Process Parameters", ENG-182. Available: <http://www.austriamicrosystems.com>.

# APPENDIX A COEFFICIENTS USED IN SIMULATION

Tables A.1 to A.5 show the absorption coefficients and the corresponding band gap energies used to perform the simulation given in Fig. 4.8.4.1 and Fig. 4.8.5.1. Each table represents the absorption coefficients and band gap energies for  $\text{Si}_{1-x}\text{Ge}_x$  where  $x$  was varied. These values were obtained through [54]. The values  $n$  and  $k$  represent the reflection and extinction coefficients respectively.

TABLE A.1  
ABSORPTION COEFFICIENTS FOR  $x = 0$

$E_G$ (eV)	$\lambda$ (nm)	$n$	$k$	$\alpha$ ( $\text{cm}^{-1}$ )
3.92	316.3265306	5.125	3.408	1353860.2
3.9	317.9487179	5.13	3.364	1329562.5
3.88	319.5876289	5.137	3.322	1306229.6
3.86	321.2435233	5.145	3.283	1284240.5
3.84	322.9166667	5.155	3.246	1263187.8
3.82	324.6073298	5.166	3.211	1243059.3
3.8	326.3157895	5.178	3.178	1223842.9
3.78	328.042328	5.192	3.147	1205526.4
3.76	329.787234	5.207	3.117	1187716.6
3.74	331.5508021	5.223	3.098	1174197.6
3.72	333.3333333	5.241	3.063	1154723.8
3.7	335.1351351	5.26	3.039	1139516.5
3.68	336.9565217	5.282	3.107	1158716.7
3.66	338.7978142	5.305	2.998	1111990
3.64	340.6593407	5.332	2.981	1099642.6
3.62	342.5414365	5.361	2.966	1088097.7
3.6	344.4444444	5.395	2.955	1078073
3.58	346.3687151	5.433	2.946	1068818.5
3.56	348.3146067	5.478	2.942	1061404.3
3.54	350.2824859	5.531	2.942	1055441.4
3.52	352.2727273	5.595	2.947	1051262
3.5	354.2857143	5.675	2.957	1048835.9
3.48	356.3218391	5.78	2.97	1047427.3
3.46	358.3815029	5.919	2.977	1043862.1
3.44	360.4651163	6.101	2.962	1032598.9
3.42	362.5730994	6.321	2.896	1003720.6
3.4	364.7058824	6.557	2.756	949612.25

TABLE A.1

ABSORPTION COEFFICIENTS FOR  $x = 0$ 

$E_G$ (eV)	$\lambda$ (nm)	$n$	$k$	$\alpha$ (cm <sup>-1</sup> )
3.38	366.8639053	6.77	2.531	866955.94
3.36	369.047619	6.921	2.238	762057.14
3.34	371.257485	6.986	1.914	647853.16
3.32	373.4939759	6.969	1.598	537654.19
3.3	375.7575758	6.888	1.317	440441.16
3.28	378.0487805	6.769	1.081	359325.23
3.26	380.3680982	6.63	0.889	293702.43
3.24	382.7160494	6.483	0.735	241335.12
3.22	385.0931677	6.337	0.614	200360.65
3.2	387.5	6.197	0.519	168308.29
3.18	389.9371069	6.064	0.446	143730.9
3.16	392.4050633	5.94	0.39	124893.51
3.14	394.9044586	5.827	0.347	110419.89
3.12	397.4358974	5.725	0.313	98966.249
3.1	400	5.632	0.286	89849.55
3.08	402.5974026	5.547	0.263	82090.829
3.06	405.2287582	5.47	0.243	75355.66
3.04	407.8947368	5.399	0.226	69625.801
3.02	410.5960265	5.332	0.209	63964.853
3	413.3333333	5.27	0.194	58980.869
2.98	416.1073826	5.211	0.179	54057.689
2.96	418.9189189	5.155	0.166	49795.257
2.94	421.7687075	5.101	0.153	45585.523
2.92	424.6575342	5.05	0.141	41724.404
2.9	427.5862069	5.001	0.13	38205.82
2.88	430.5555556	4.954	0.12	35023.691
2.86	433.5664336	4.909	0.11	31882.098
2.84	436.6197183	4.865	0.102	29356.663
2.82	439.7163121	4.823	0.095	27149.441
2.8	442.8571429	4.782	0.087	24686.838
2.78	446.0431655	4.743	0.081	22820.124
2.76	449.2753623	4.705	0.075	20977.732
2.74	452.5547445	4.669	0.07	19437.338
2.72	455.8823529	4.634	0.065	17917.212
2.7	459.2592593	4	0.061	16690.978
2.68	462.6865672	4.567	0.057	15480.958
2.66	466.1654135	4.535	0.053	14287.153
2.64	469.6969697	4.505	0.05	13377.104
2.62	473.2824427	4.475	0.048	12744.732
2.6	476.9230769	4.447	0.045	11856.979



TABLE A.1

ABSORPTION COEFFICIENTS FOR  $x = 0$ 

$E_G$ (eV)	$\lambda$ (nm)	$n$	$k$	$\alpha$ (cm <sup>-1</sup> )
2.6	476.9230769	4.447	0.045	11856.979
2.58	480.620155	4.419	0.043	11242.848
2.56	484.375	4.393	0.041	10636.825
2.54	488.1889764	4.367	0.04	10296.317
2.52	492.0634921	4.342	0.038	9704.481
2.5	496	4.318	0.037	9374.1071
2.48	500	4.295	0.035	8796.4594
2.46	504.0650407	4.272	0.034	8476.2197
2.44	508.1967213	4.251	0.033	8160.0336
2.42	512.3966942	4.23	0.032	7847.9011
2.4	516.6666667	4.209	0.031	7539.8224
2.38	521.0084034	4.189	0.03	7235.7973
2.36	525.4237288	4.17	0.03	7174.9923
2.34	529.9145299	4.151	0.029	6877.0477
2.32	534.4827586	4.133	0.028	6583.1567
2.3	539.1304348	4.116	0.027	6293.3195
2.28	543.8596491	4.099	0.026	6007.5359
2.26	548.6725664	4.082	0.025	5725.806
2.24	553.5714286	4.065	0.025	5675.1351
2.22	558.5585586	4.05	0.024	5399.4857
2.2	563.6363636	4.034	0.023	5127.8899
2.18	568.8073394	4.019	0.022	4860.3479
2.16	574.0740741	4.004	0.022	4815.7575
2.14	579.4392523	3.99	0.021	4554.2959
2.12	584.9056604	3.976	0.02	4296.888
2.1	590.4761905	3.962	0.019	4043.5338
2.08	596.1538462	3.949	0.019	4005.0239
2.06	601.9417476	3.936	0.018	3757.7502
2.04	607.8431373	3.923	0.017	3514.5301
2.02	613.8613861	3.91	0.017	3480.0739
2	620	3.898	0.016	3242.9344
1.98	626.2626263	3.886	0.015	3009.8484
1.96	632.6530612	3.874	0.015	2979.4459
1.94	639.1752577	3.863	0.014	2752.4405
1.92	645.8333333	3.851	0.013	2529.4888
1.9	652.6315789	3.84	0.013	2503.14
1.88	659.5744681	3.83	0.012	2286.2687
1.86	666.6666667	3.819	0.011	2073.4512
1.84	673.9130435	3.809	0.011	2051.156
1.82	681.3186813	3.798	0.01	1844.4189

TABLE A.1

ABSORPTION COEFFICIENTS FOR  $x = 0$ 

$E_G$ (eV)	$\lambda$ (nm)	$n$	$k$	$\alpha$ (cm <sup>-1</sup> )
1.8	688.8888889	3.788	0.01	1824.1506
1.78	696.6292135	3.779	0.009	1623.494
1.76	704.5454545	3.769	0.009	1605.2525
1.74	712.6436782	3.76	0.008	1410.6764
1.72	720.9302326	3.75	0.008	1394.4618
1.7	729.4117647	3.741	0.007	1205.9662
1.68	738.0952381	3.733	0.007	1191.7784
1.66	746.9879518	3.724	0.006	1009.3633
1.64	756.097561	3.715	0.006	997.20231
1.62	765.4320988	3.707	0.005	820.86776
1.6	775	3.699	0.005	810.73359
1.58	784.8101266	3.691	0.005	800.59942
1.56	794.8717949	3.683	0.004	632.3722
1.54	805.1948052	3.675	0.004	624.26486
1.52	815.7894737	3.668	0.004	616.15753
1.5	826.6666667	3.66	0.003	456.03764
1.48	837.8378378	3.653	0.003	449.95714
1.46	849.3150685	3.646	0.003	443.87664
1.44	861.1111111	3.639	0.002	291.86409
1.42	873.2394366	3.632	0.002	287.81042
1.4	885.7142857	3.625	0.002	283.75676
1.38	898.5507246	3.619	0.002	279.70309
1.36	911.7647059	3.612	0.001	137.82471
1.34	925.3731343	3.606	0.001	135.79788
1.32	939.3939394	3.6	0.001	133.77104
1.3	953.8461538	3.594	0.001	131.74421
1.28	968.75	3.588	0.001	129.71737
1.26	984.1269841	3.582	0	0
1.24	1000	3.576	0	0
1.22	1016.393443	3.571	0	0
1.2	1033.333333	3.565	0	0
1.18	1050.847458	3.56	0	0
1.16	1068.965517	3.555	0	0
1.14	1087.719298	3.55	0	0
1.12	1107.142857	3.545	0	0
1.1	1127.272727	3.54	0	0
1.08	1148.148148	3.535	0	0
1.06	1169.811321	3.531	0	0
1.04	1192.307692	3.526	0	0
1.02	1215.686275	3.522	0	0
1	1240	3.517	0	0

TABLE A.2

ABSORPTION COEFFICIENTS FOR  $x = 0.2$ 

$E_G$ (eV)	$\lambda$ (nm)	$n$	$k$	$\alpha$ (cm <sup>-1</sup> )
12	103	0.64	0.86	1045846.3
11	113	0.62	0.98	1092463.5
10	124	0.6	1.16	1175563.7
9	138	0.6	1.4	1276905.4
8	155	0.66	1.69	1370139.8
7	177	0.77	2.18	1546474.3
6	207	1.18	2.71	1647816
5.6	221	1.28	3.07	1742266.5
5.4	230	1.43	3.15	1723822.3
5.2	238	1.49	3.19	1681056.1
5	248	1.5	3.4	1722808.9
4.8	258	1.6	3.75	1824150.6
4.6	270	1.87	4.29	1999877.1
4.4	282	2.7	4.93	2198304.1
4.2	295	4.18	4.53	1928127.2
4	310	4.48	3.69	1495803.5
3.8	326	4.6	3.3	1270824.9
3.6	344	4.77	3.07	1120028.5
3.5	354	4.92	3.01	1067634.8
3.4	364	5.21	2.95	1016457.2
3.3	376	5.57	2.71	906298.81
3.2	386	5.91	2.26	732903.16
3.1	400	6.07	1.62	508938.01
3	413	5.87	0.99	300984.84
2.9	428	5.53	0.62	182212.37
2.8	443	5.22	0.41	116340.27
2.7	459	4.99	0.3	82086.776
2.6	477	4.79	0.21	55332.567
2.5	496	4.63	0.13	32936.052
2.4	517	4.49	0.08	19457.606
2.3	539	4.37	0.02	4661.7181
2.2	564	4.27	0.01	2229.5174
2.1	590	4.18	0.01	2128.1757
2	620	4.1	0.01	2026.834
1.4	886	3.74	0.00453	642.70905
1.35	919	3.72	0.00348	476.1033
1.3	954	3.7	0.00253	333.31285
1.25	992	3.68	0.00171	216.61788
1.2	1033	3.67	0.00104	126.47444
1.15	1078	3.65	0.00053	61.767765
1.1	1127	3.64	0.00019	21.180415
1.05	1181	3.63	0.00005	5.3204392
1	1240	3.61	0.00001	1.013417

TABLE A.3  
 ABSORPTION COEFFICIENTS FOR  $x = 0.5$ 

$E_G$ (eV)	$\lambda$ (nm)	$n$	$k$	$\alpha$ (cm <sup>-1</sup> )
12	103	0.77	0.88	1070168.3
11	113	0.75	0.99	1103611.1
10	124	0.72	1.15	1165429.5
9	138	0.73	1.37	1249543.1
8	155	0.77	1.63	1321495.7
7	177	0.85	2.12	1503910.8
6	207	1.23	2.68	1629574.5
5.6	221	1.32	2.88	1634438.9
5.4	230	1.39	2.89	1581538.5
5.2	238	1.4	2.97	1565121.2
5	248	1.43	3.17	1606265.9
4.8	258	1.54	3.48	1692811.7
4.6	270	1.77	3.89	1813408.4
4.4	282	2.41	4.42	1970893.4
4.2	295	3.56	4.17	1774898.5
4	310	3.9	3.53	1430944.8
3.8	326	4.03	3.17	1220762.1
3.6	344	4.15	2.95	1076248.8
3.5	354	4.23	2.88	1021524.3
3.4	365	4.34	2.8	964772.97
3.3	376	4.41	2.7	902954.53
3.2	388	4.6	2.58	836677.06
3.1	400	4.69	2.47	775973.39
3	413	4.82	2.41	732700.48
2.9	428	5.06	2.32	681826.95
2.8	443	5.38	2.06	584538.92
2.7	459	5.62	1.56	426851.23
2.6	477	5.51	1.01	266123.3
2.5	496	5.26	0.68	172280.89
2.4	517	5.03	0.46	111881.24
2.3	539	4.83	0.33	76918.349
2.2	564	4.65	0.26	57967.452
2.1	590	4.5	0.19	40435.338
2	620	4.39	0.16	32429.344
1.3	954	3.94	0.00644	848.4327
1.25	992	3.91	0.00494	625.78499
1.2	1033	3.89	0.00359	436.58004
1.15	1078	3.86	0.00241	280.86852
1.1	1127	3.84	0.00145	161.64001
1.05	1181	3.83	0.00071	75.550236
1	1240	3.81	0.00023	23.308591
0.95	1305	3.79	0.00005	4.8137307

TABLE A.4

 ABSORPTION COEFFICIENTS FOR  $x = 0.75$ 

$E_G$ (eV)	$\lambda$ (nm)	$n$	$k$	$\alpha$ (cm <sup>-1</sup> )
12	103	0.85	0.9	1094490.3
11	113	0.84	0.99	1103611.1
10	124	0.8	1.13	1145161.2
9	138	0.8	1.36	1240422.4
8	155	0.83	1.64	1329603.1
7	177	1.02	2.08	1475535.1
6	207	1.27	2.58	1568769.5
5.6	221	1.28	2.89	1640114
5.4	230	1.34	2.87	1570593.6
5.2	238	1.33	2.96	1559851.4
5	248	1.35	3.17	1606265.9
4.8	258	1.45	3.47	1687947.3
4.6	270	1.67	3.89	1813408.4
4.4	282	2.3	4.46	1988729.5
4.2	295	3.46	4.21	1791923.9
4	310	3.8	3.58	1451213.1
3.8	326	3.92	3.22	1240017
3.6	344	4.03	2.98	1087193.7
3.5	354	4.09	2.89	1025071.3
3.4	365	4.18	2.8	964772.97
3.3	376	4.27	2.7	902954.53
3.2	388	4.34	2.57	833434.13
3.1	400	4.36	2.45	769690.2
3	413	4.36	2.38	723579.73
2.9	428	4.4	2.39	702399.31
2.8	443	4.5	2.42	686691.35
2.7	459	4.72	2.45	670375.34
2.6	477	5.07	2.39	629737.31
2.5	496	5.45	2.11	534577.46
2.4	517	5.72	1.57	381855.52
2.3	539	5.6	0.98	228424.19
2.2	564	5.33	0.64	142689.11
2.1	590	5.11	0.43	91511.554
2	620	4.93	0.29	58778.185
1.2	1033	4.11	0.00657	798.97795
1.15	1078	4.09	0.00478	557.07532
1.11	1117	4.06	0.00322	362.2155
1.05	1181	4.04	0.00193	205.36895
1	1240	4.02	0.00094	95.261197
0.95	1305	4	0.00029	27.919638
0.9	1378	3.98	0.00004	3.6483011

TABLE A.5

ABSORPTION COEFFICIENTS FOR  $x = 1$ 

$E_G$ (eV)	$\lambda$ (nm)	$n$	$k$	$\alpha$ (cm <sup>-1</sup> )
12	103	0.74	0.96	1167456.4
11	113	0.74	1.08	1203939.4
10	124	0.75	1.25	1266771.2
9	138	0.78	1.45	1322509.2
8	155	0.83	1.73	1402569.1
7	177	1	2.14	1518098.6
6	207	1.37	2.63	1599172
5.6	221	1.29	2.73	1549311.9
5.4	230	1.3	2.73	1493979.3
5.2	238	1.28	2.82	1486074.7
5	248	1.29	3.02	1530259.6
4.8	258	1.36	3.31	1610116.9
4.6	270	1.52	3.72	1734159.1
4.4	282	2.14	4.42	1970893.4
4.2	295	3.34	4.04	1719565.9
4	310	3.61	3.43	1390408.1
3.8	326	3.7	3.09	1189954.2
3.6	344	3.78	2.87	1047062.4
3.5	354	3.84	2.78	986054.73
3.4	365	3.9	2.7	930316.79
3.3	376	3.97	2.6	869511.77
3.2	388	4.02	2.47	801004.78
3.1	400	4.02	2.34	735132.68
3	413	3.98	2.26	687096.72
2.9	428	3.94	2.25	661254.58
2.8	442	3.94	2.29	649802.97
2.7	459	3.99	2.35	643013.08
2.6	477	4.09	2.42	637641.97
2.5	496	4.25	2.5	633385.62
2.4	517	4.54	2.59	629940
2.3	539	4.99	2.46	573391.33
2.2	564	5.27	2.2	490493.82
2.1	590	5.71	1.76	374558.92
2	620	5.62	1.05	212817.57
0.9	1377	4.2	0.00826	753.37419
0.85	1459	4.18	0.00554	477.21806
0.8	1550	4.15	0.00325	263.48842
0.75	1653	4.13	0.0015	114.00941
0.7	1771	4.12	0.00032	22.70054
0.65	1908	4.1	0.00002	1.3174421

# APPENDIX B TRANSIMPEDANCE AMPLIFIER DESIGN

The final subsystem in the implementation of the IR detector is the TIA as discussed in section 4.5. This appendix describes the design of this subsystem. Although this is not directly part of the research, it is required for the experimental verification.

Fig. 4.5.1 shows the components that make up the TIA, which consist of an NMOS, PMOS and a resistor. Typically it is aimed to design for a  $Q$  factor of 0.85. Experimentally this value is almost never obtained. For this TIA, the closed-loop transfer function is given in (B.1) [53].

$$A_{CL} = \frac{V_{OUT}}{I_{IN}} = \frac{A(j\omega)R_F}{-\omega^2 C_{IN}R_F C_{OUT}R_{OUT} + j\omega(C_{IN}R_F + C_{OUT}R_{OUT}) + \frac{1 - A(j\omega)^2 R_F}{A(j\omega)R_F}} \quad (B.1)$$

where  $C_{IN}$ ,  $C_{OUT}$  is the input and output capacitance respectively,

$R_{OUT}$ ,  $R_F$  is the feedback and output resistance respectively,

$A(s)$  is the open-loop transfer function.

$A(s)$  is given in (A.2) [53].

$$A(j\omega) = \frac{R_F(g_{m1} + g_{m2})(g_{ds1} + g_{ds2})^{-1}}{(1 + j\omega C_{IN}R_F)(1 + j\omega C_{OUT}R_{OUT})} \quad (B.2)$$

where  $g_m$  and  $g_{ds}$  are the gate-source and the drain-source transconductance respectively.

The quality factor for this TIA is given in (A.3) [53].

$$Q = \frac{\sqrt{A(j\omega)C_{IN}R_F C_{OUT}R_{OUT}}}{C_{IN}R_F + C_{OUT}R_{OUT}} \quad (B.3)$$

Table B.I shows the results obtained by using equations (B.1 – B.3). Other parameters that have a direct influence on these equations are defined and used in well-known equations, like the drain current flowing through the transistor for a specific gate voltage. Using

parameter extraction, values of 0.44 V and -0.38 V were obtained for the threshold voltage of the NMOS and PMOS devices respectively. These were subsequently used in all calculations.

TABLE BI  
TIA DESIGN RESULTS

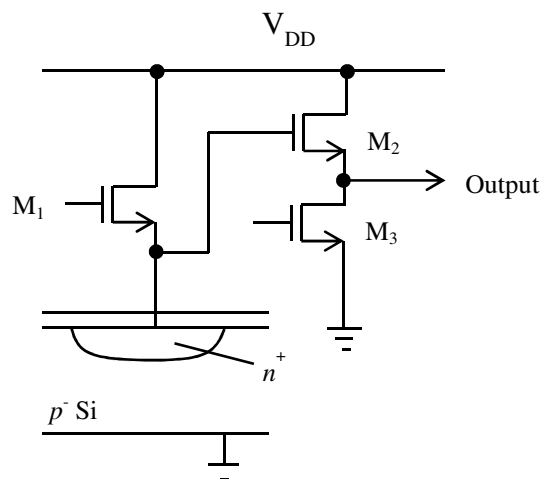
$\frac{W_P}{L_P}$	$\frac{W_N}{L_N}$	$\tau_{plh} (ns)$	$\tau_{phl} (ns)$	OF (MHz)	$R_F (k\Omega)$	$ A(s) $	$ A(cl) $	Q
$\frac{15 \mu m}{0.35 \mu m}$	$\frac{5 \mu m}{0.35 \mu m}$	1.2	1	80	2	141	151	1.16
$\frac{5 \mu m}{0.35 \mu m}$	$\frac{1.67 \mu m}{0.35 \mu m}$	0.6	0.5	80	6	144	147	0.81
$\frac{5 \mu m}{0.35 \mu m}$	$\frac{1.67 \mu m}{0.35 \mu m}$	0.6	0.5	80	2	135	145	1.38
$\frac{15 \mu m}{0.35 \mu m}$	$\frac{5 \mu m}{0.35 \mu m}$	0.6	0.5	80	3	152	159	0.69
$\frac{15 \mu m}{0.35 \mu m}$	$\frac{5 \mu m}{0.35 \mu m}$	0.6	0.5	80	1	135	156	1.17
$\frac{15 \mu m}{0.35 \mu m}$	$\frac{5 \mu m}{0.35 \mu m}$	0.6	0.5	80	2	147	158	0.84
$\frac{15 \mu m}{0.35 \mu m}$	$\frac{5 \mu m}{0.35 \mu m}$	0.6	0.5	100	2	119	126	0.75

In Table B.I, the OF denotes the operating frequency of the system. These results confirm some of the tradeoffs mentioned in Fig. 3.4.1. Based on these results, the best values to use are the second last set of values. These give the best performance with the least amount of die area required and were subsequently used for this research.



# APPENDIX C DETECTOR READOUT CIRCUIT DESIGN

The detector itself contains peripheral circuitry that has to process the data (which in this case are the captured photons) and transform these into a useable signal. Using well-known equations for the different currents and voltages, an acceptable design can be obtained as discussed in section 4.7, keeping in mind performance and fill-factor. Fig. C.1 depicts the readout circuit used in this research.



**Figure C.1** Detector readout circuit

Fig. C.1 shows the components in a typical readout circuit used in this research. It consists of a pixel element (usually a photodiode) and the MOS devices biased in different regions of operation. Transistor  $M_1$  operates in the triode region whereas transistors  $M_2$  and  $M_3$  operate in the linear region. The results for various aspect ratios are given in Table C.I.

TABLE C.I

## DETECTOR READOUT CIRCUIT DESIGN RESULTS

$W_1$ ( $\mu\text{m}$ )	$W_2$ ( $\mu\text{m}$ )	$V_{S1}$ (V)	$V_{S2}$ (V)	$I_{D2}$ ( $\mu\text{A}$ )	$V_{G3}$ (V)
1	1	2.41	1.458	11	1.7
2	2	2.425	1.457	13.7	1.9
4	4	2.58	1.455	15.2	2

All the values given in Table C.1 are for a photon generated current of 100 nA ( $I_{DI}$ ). The results show that by choosing a width for M1 and M2 equal to 1  $\mu\text{m}$ , the best performance and smallest fill factor are obtained. M3's aspect ratio is chosen sufficiently large such that no current limiting occurs. For this research it was chosen to be 5  $\mu\text{m}$  wide. The length of all MOSFETs was chosen to be 0.35  $\mu\text{m}$ .