AN INVESTIGATION INTO AN ALL-OPTICAL 1x2 SELF-ROUTED OPTICAL SWITCH USING PARALLEL OPTICAL PROCESSING

by

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KEYWORDS

All-optical packet switching; parallel processing; optical switching; optical packet switched networks; optical networks; optical header processing; optical inverter

SUMMARY

A unique all-optical 1x2 self-routed switch is introduced. This switch routes an optical packet from one input to one of two possible outputs. The header and payload are transmitted separately in the system, and the header bits are processed in parallel thus increasing the switching speed as well as reducing the amount of buffering required for the payload. A 1x2 switching operation is analysed and a switching ratio of up to 14dB is obtained.

The objective of the research was to investigate a unique all-optical switch. The switch works by processing the optical bits in a header packet which contains the destination address for a payload packet. After the destination address is processed the optical payload packet gets switched to one of two outputs depending on the result of the optical header processing.

All-optical packet switching in the optical time domain was accomplished by making use of all-optical parallel processing of an optical packet header. This was demonstrated in

experiments in which a three bit parallel processing all-optical switching node was designed, simulated and used to successfully demonstrate the concept.

The measure of success that was used in the simulated experiments was the output switching ratio, which is the ratio between the peak optical power of a high bit at the first output and the peak optical power of a high bit at the second output. In all experimental results the worst case scenario was looked at, which means that if there was any discrepancy in the peak value of the output power then the measurement's minimum/maximum value was used that resulted in a minimum value for the switching ratio.

The research resulted in an optical processing technique which took an optical bit sequence and delivered a single output result which was then used to switch an optical payload packet. The packet switch node had two optical fibre inputs and two optical fibre outputs. The one input fibre carried the header packet and the other input fibre carried the payload packet. The aim was to switch the payload packet to one of the two output fibres depending on the bit sequence within the header packet. Also only one unique address (header bit sequence) caused the payload packet to exit via one of the outputs and all the other possible addresses caused the payload packet to exit via the other output. The physical configuration of the all-optical switches in the parallel processing structure of the switching node determined for which unique address the payload packet would exit via a different output than when the address was any of the other possible combinations of sequences.

Only three Gaussian shaped bits were used in the header packet at a data rate of 10 Gbps and three Gaussian shaped bits in the payload packet at a data rate of 40 Gbps, but in theory more bits can be used in the payload packet at a decreased bit length to increase throughput. More bits can also be used in the header packet to increase the number of addresses that can be reached.

In the simulated experiments it was found that the payload packet would under most circumstances exit both outputs, and at one output it would be much larger than at the other

output (where it was normally found to be suppressed when compared to the other output's optical power).

The biggest advantage of this method of packet-switching is that it occurs all-optically, meaning that there is no optical to electronic back to optical conversions taking place in order to do header processing. All of the header processing is done optically. One of the disadvantages is that the current proposed structure of the all-optical switching node uses a Cross-Gain Modulator (XGM) switch which is rather expensive because of the Semiconductor Optical Amplifier (SOA). In this method of packet-switching the length of the payload packet cannot exceed the length of one bit of the header packet. This is because the header processing output is only one header bit length long and this output is used to switch the payload packet. Thus any section of the payload packet that is outside this header processing output window will not be switched correctly.

ONDERSOEK NA TEN VOLLE OPTIESE 1x2 SELF GEREGULEERDE OPTIESE SKAKELAAR DEUR GEBRUIK TE MAAK VAN PARALLELE PROSESSERING

deur

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SLEUTELWOORDE

Optiese pakkie skakeling; parallele prosessering; optiese skakeling; optiese pakkie skakel netwerke; optiese netwerke; optiese hoof prosessering; optiese omkeerder

OPSOMMING

'n Unieke 1X2 ten volle optiese self gereguleerde skakelaar is voorgestel. Die skakelaar skakel 'n optiese pakkie vanaf een inset na een van twee moontlike uitsette. Die pakkie se adres en die informasie pakkie is apart in die stelsel gehou, en die adres bisse is in parallel verwerk wat die skakel spoed verhoog en ook die buffer grootte wat benodig word vir die data pakkie verlaag het. 'n 1X2 Skakel operasie word geanaliseer en 'n skakel verhouding van tot 14dB is bereik.

Die objektief van die navorsing was om 'n unieke ten volle optiese skakelaar te ondersoek. Die skakelaar werk deur die optiese seine in 'n adres pakkie opties te verwerk. Die adres pakkie bevat die adres van die bestemming vir 'n informasie pakkie. Nadat die bestemmings adres verwerk is word die informasie pakkie na een van twee uitsette geskakel na aanleiding van die resultaat van die optiese hoof verwerking.

Optiese pakkie skakeling is in die optiese tyd omgewing bereik deur gebruik te maak van optiese parallel prosessering van 'n optiese adres pakkie. Dit was gedemonstreer deur

eksperimente waarin ‘n drie bis parallele prosessering optiese skakel node ontwikkel, gesimuleer en suksesvol gedemonstreer was.

In die eksperimente was die sukses van die pakkie skakelaar was gemeet aan die uitset skakel verhouding. Die uitset skakel verhouding is die verhouding tussen die maksimum optiese sterkte van ‘n hoog sein by die eerste uitset en die maksimum optiese sterkte van ‘n hoog sein by die tweede uitset. In all die eksperimentele resultate is daar gekyk na die slegste situasie wat beteken dat as daar enige onduidelikheid in die maksimum waarde van die uitset krag was dan was die lesing se minimum/maksimum waarde gebruik wat ‘n minimum waarde vir die skakel verhouding tot gevolg sou hê

Die navorsing het gelei tot ‘n optiese verwerkings tegniek wat ‘n optiese bis sekwensie as inset neem en ‘n enkele uitset as resultaat lewer wat dan gebruik was om ‘n optiese informasie pakkie te skakel. Die pakkie skakel node het twee optiese vesel insette en twee optiese vesel uitsette. Die een inset vesel dra die adres pakkie en die ander inset vesel dra die informasie pakkie. Die mikput was om die informasie pakkie na een van die twee uitset vesels te skakel na aanleiding van die sein sekwensie binne die hoof pakkie. Slegs een unieke adress (adres pakkie sekwensie) het daartoe gelei dat die informasie pakkie by een van die uitsette uitgestuur is, vir all die ander moontlike adresse is die informasie pakkie by die teenoorgestelde uitset uitgestuur. Die fisiese konfigurasie van die optiese skakelaars in die parallele prosesserings struktuur van die skakel node het bepaal vir watter unieke adres die informasie pakkie by ‘n ander uitset sou uitkom as vir enige van die ander adres kombinasies.

Slegs drie Gaussies gevormde bisse was in die adres pakkie gebruik teen ‘n data spoed van 10 Gigagrepe per sekonde en drie Gaussies gevormde bisse was gebruik in die data pakkie teen ‘n informasie spoed van 40 Gigagrepe per sekonde, maar teoreties kan meer bisse kan gebruik word in die informasie pakkie teen ‘n verkorte bis lengte om die data deurset syfer te verhoog. Meer bisse kan ook in die adres pakkie gebruik word om die aantal adresse wat ge-adresseer kan word te vergroot.

Daar is in die gesimuleerde eksperimente gevind dat die informasie pakkie onder meeste omstandighede by beide uitset vesels sou uitkom, en dat die optiese krag baie groter by die een uitset sou wees as by die ander (waar dit normaalweg onderdruk was in vergelyking met die ander uitset).

Die grootste voordeel van hierdie metode van pakkie skakeling is dat dit ten volle in die optiese arena plaasvind wat beteken dat daar geen optiese na elektroniese terug na optiese omskakelings plaasvind om adres verwerking te doen nie. Die adres pakkie word slegs in die optiese arena verwerk. ‘n Nadeel van die huidige voorgestelde struktuur is dat die optiese skakel node ‘n Kruis Versterkings Modulator skakelaar gebruik wat die duurder alternatief is as gevolg van die gebruik van ’n Halfgeleier Optiese Versterker . In hierdie metode van pakkie skakeling kan die informasie pakkie se lengte nie langer as die lengte van een adres pakkie bis wees nie. Dit is omdat die adres verwerkings uitset is slegs een adres pakkie bis lank is en hierdie uiset word gebruik om die informasie pakkie te skakel. Dus sal enige gedeelte van die informasie pakkie wat buite hierdie adres pakkie uitset venster val nie korrek ge-skakel word nie.

List of abbreviations

AU	Arbitrary Units
CPMZ	Colliding Pulse Mach-Zehnder
CW	Continuous Wave
dB	decibel
FWHM	Full Width Half Maximum
Gbps	Gigabit per second
GUI	Graphical User Interface
InP	Indium Phosphide
MEMS	Micro-electro-mechanical Systems
MZI	Mach-Zehnder Interferometer
NOLM	Nonlinear Optical Loop Mirror
OADMs	optical add drop multiplexers
OSA	Optical Spectrum Analyzer
OTDM	Optical Time-Division Multiplexing
OXCs	optical cross-connects
PBS	Polarization Beam Splitter
PDA	Photonic Design Automation
PPS	Photonic Packet Switched
PTDS	Photonic Transmission Design Suite
SMZ	Symmetric Mach-Zehnder
SOA	Semiconductor Optical Amplifier
SONET	Synchronous Optical Network
SDH	Synchronous Digital Hierarchy
TDM	Time Division Multiplexing
TM	Trademark
TOAD	Terahertz Optical Asymmetric Demultiplexer
WDM	Wavelength Division Multiplexing
XGM	Cross-gain Modulator
XPM	Cross Phase Modulation

CONTENTS

Chapter 1

INTRODUCTION

1. BACKGROUND

There are two generations of optical networks. In the first generation optics was essentially used for transmission and to provide capacity. Optical fibre provided lower bit error rates and higher capacities than copper cables. All the network functions (management, switching, buffering, etc.) were handled by electronics. Examples of these first generation networks are SONET (Synchronous Optical Network) and the SDH (Synchronous Digital Hierarchy). In second generation networks some of the routing, switching, and intelligence is moving into the optical layer [1].

In an all-optical network, data is carried from its source to its destination in optical form, without undergoing any optical-to-electrical conversions along the way to do management, switching, buffering, regeneration or any other network function. Presently research into all-optical photonic networks concentrates on two major areas: WDM (Wavelength-Division Multiplexing) and OTDM (Optical Time-Division Multiplexing) (see Aleksić *et al.* [2]). WDM uses the wavelength characteristics of light to enable routing and management of optical networks and increase the capacity of optical networks. WDM systems are widely deployed today in long-haul and undersea networks and are being deployed in metro networks as well. OTDM tries to approach the functionality of electronic TDM computer networks by using the individual bits of an optical packet header to enable packet management of the network. The latter is done because an ideal network would have the throughput of current all-optical networks and the functionality of current packet switched electronic networks. These optical packet-switched networks are called Photonic Packet Switched (PPS) networks and the aim of a PPS network is to provide the same services that electronic packet-switched networks provide, but at much higher speeds.

Currently WDM enjoys the lion's share of the research efforts because the fundamental technologies used in WDM networks are largely commercially available. The big disadvantage of OTDM is the difficulty of doing optical signal processing and this deficiency has led to research in OTDM focussing on the serial processing of optical

packet headers. Routing and switching tasks are already implemented in WDM networks by the use of optical cross-connects (OXCs) [3] and optical add drop multiplexers (OADMs) [4]. Aleksić *et al.* [2] discuss the current trends and advantages of OTDM systems. The advantages include simple management and control, the provision of a truly flexible bandwidth on demand service, packet switching or self-routing of a packet, scalability in number of users (packet address space), the use of statistical multiplexing, the ability to provide quality of service, the use of digital regeneration, digital buffering, coding and encryption, and the potential to provide flexible bandwidth on demand at burst rates of 100Gb/s at a signal wavelength.

Mahoney *et al* [5] discuss the need for optical packet switching and states that the bandwidth efficiency associated with optical packet switched networks will be able to economically support the increased demand for capacity in telecommunication networks where circuit switched optical networks will not meet future requirements. Mahoney *et al* [5] also states that pure optical packet switching in which packet header recognition and control are achieved in an all-optical manner is still many years away. In this approach the payload is routed in the optical domain, but the label processing and switch control takes place in the electronic domain. In this investigation the header (also referred to as label) is processed in the optical domain and thus no electronic processing takes place anywhere during the course of routing the payload.

Calabretta *et al* [6] discuss a novel all-optical header processing technique that utilizes a header pre-processor to separate the payload from the header and subsequently the header is processed by two Terahertz Optical Asymmetric Demultiplexers (TOAD) which acts as switches for the optical payload. This method can distinguish between a large number of header patterns. The address information is encoded by the time difference between the leading edges of two header pulses, thus not in the pattern itself. Thus the more addresses there are to distinguish between the longer the header packet needs to be. As such the addition of one additional header bit (irrespective of its position) would mean a constant increase in number of addresses that can be processed. In the parallel processing method used in this investigation the addition of one additional header bit would double the number of addresses that can be processed.

Optical packet switched networks have also been demonstrated in the Wavelength Division Multiplexing (WDM) domain by combining packet switching with WDM transmission techniques [7]. The goal is to shift most of the switching functionality into the optical domain permitting the switching capability of IP-routers together with the capacity of WDM transmission. The focus in this investigation has been on the optical time domain as opposed to WDM technologies because of the time domain nature of the header processing technique employed.

Glesk *et al.* [8] uses a TOAD device to demonstrate all-optical ultra fast single bit packet routing. The limitation of this device is that only two addresses are possible because of the single header bit which has to be used in order to facilitate ultra-fast (250 Gbps) operation of the device. In this investigation the parallel processing nature of the device facilitates a number of addresses depending on the number of header bits processed and thus the header processing architecture in the device.

2. AIM

This research investigation aims to provide a unique all-optical 1x2 self routed optical switch for PPS networks that is scalable, has the potential for reduced cost, is fluid, has a good switching ratio, and has the potential for increased throughput. The motivations for researching optical packet switching are that optical packet switches hold the potential for realizing higher capacities than electronic routers, and optical packet switching can improve the bandwidth utilization within the optical layer [9].

3. OUTLINE

The crux of any packet-switched network is the switching node. This also holds true for the all-optical packet-switched network where one of the most important ingredients is the optical switch node. The idea behind an optical packet-switch is to create a node with much higher capacities than can be envisioned with electronic packet-switching. Such a node will take an incoming packet, read its header and optically switch it to the appropriate optical output port. Additional functions like contention and buffering are also important, but this investigation will aim to only provide a unique all-optical switch which can be used in optical packet-switched networks. The problem addressed in this investigation is the

difficulty of optical computing to perform processing of the optical packet header in the optical time domain.

In this investigation parallel optical signal-processing is utilized by implementing a novel optical parallel processing technique, which brings all the advantages that parallel processing enjoys over serial processing. The parallel processing will be applied to the optical destination addresses in a header packet.

To introduce the concept of the all-optical packet switch two types of networks are discussed here. In both network architectures there are packet switch nodes which switch optical packets to their destinations. The only difference between the networks is the node link structure. The first network architecture has a single link between two nodes on which a single optical packet is transported. The network architecture is shown in figure 1.1 below.

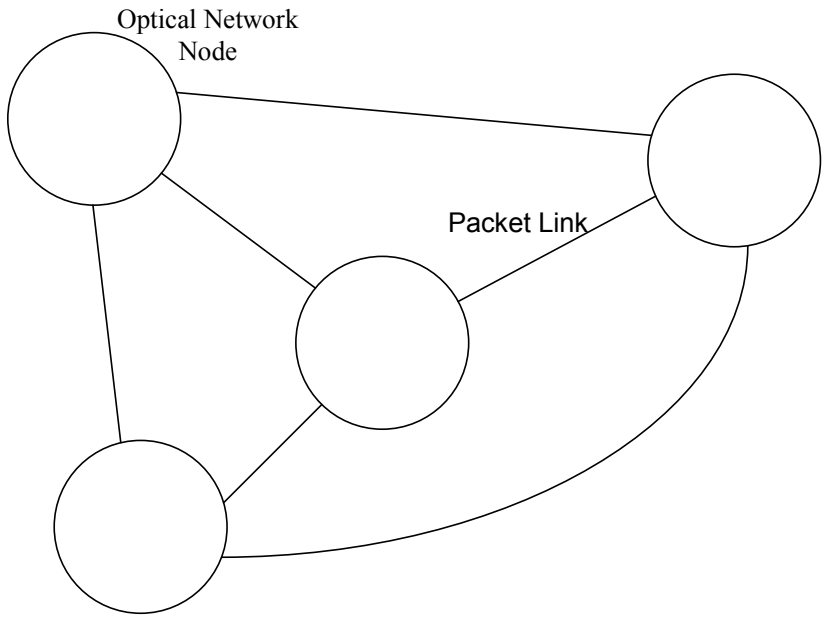

Figure 1.1

Architecture of a simple optical packet-switched network with single links on which packets are transported between nodes. The packets that get transported between the nodes of the network consist of header bits and the payload bits.

In the network architecture of figure 1.1 above the links between the nodes consist of single fibres. These links carry one optical packet consisting of header bits and payload bits on the same link. The header bits are used by the nodes to determine where to switch the packet, and the payload bits contain the data that needs to get to the destination. In this network architecture the packet switch will have to split the header and payload bits, process the header bits and then switch the packet to the correct output link based on the header processing result.

The second network architecture has two links between network nodes as shown in figure 1.2 below.

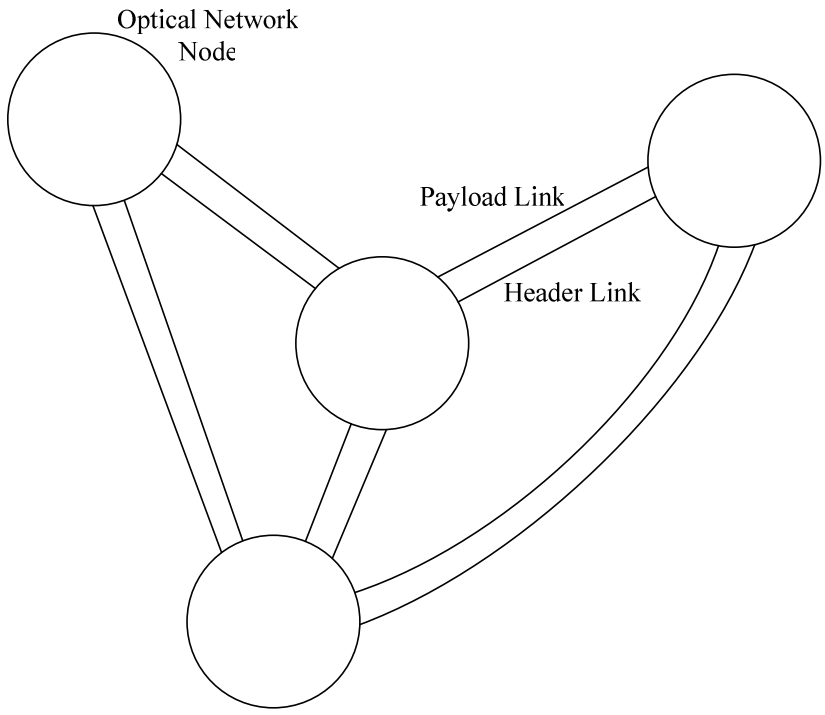

Figure 1.2

Architecture of a simple optical packet-switched network with two links between nodes. On one link the packet header gets transported and on the other link the packet payload gets transported between nodes.

In the network architecture of figure 1.2 above the links between the nodes consist of two fibres. One of the fibres carries the packet header and the other fibre carries the payload packet. Each node accepts the header and payload packets on separate input fibres. In this network architecture the packet switch does not have to split the header and payload bits, it

only has to process the header bits and then switch the packet payload to the correct output link.

In the configuration that is used in this investigation the packet header and packet payload are accepted at separate input fibres. The self routed switch proposed in this investigation can be used in both network architectures shown above. If the proposed packet switch is used in the network architecture of figure 1.1 the header and payload bits can be separated before they enter the packet switch, although this is not absolutely necessary as will be discussed in chapter 2. Methods for separating the header and payload bits will also be discussed.

The rest of this chapter is divided up into two sections. The overview section will expand on a conceptual overview of what the research is all about. The approach section will focus on the most important choices of components for an optical packet-switched network node.

4. OVERVIEW

A conceptual block diagram of the architecture of the proposed all-optical packet-switch is shown in figure 1.3 below.

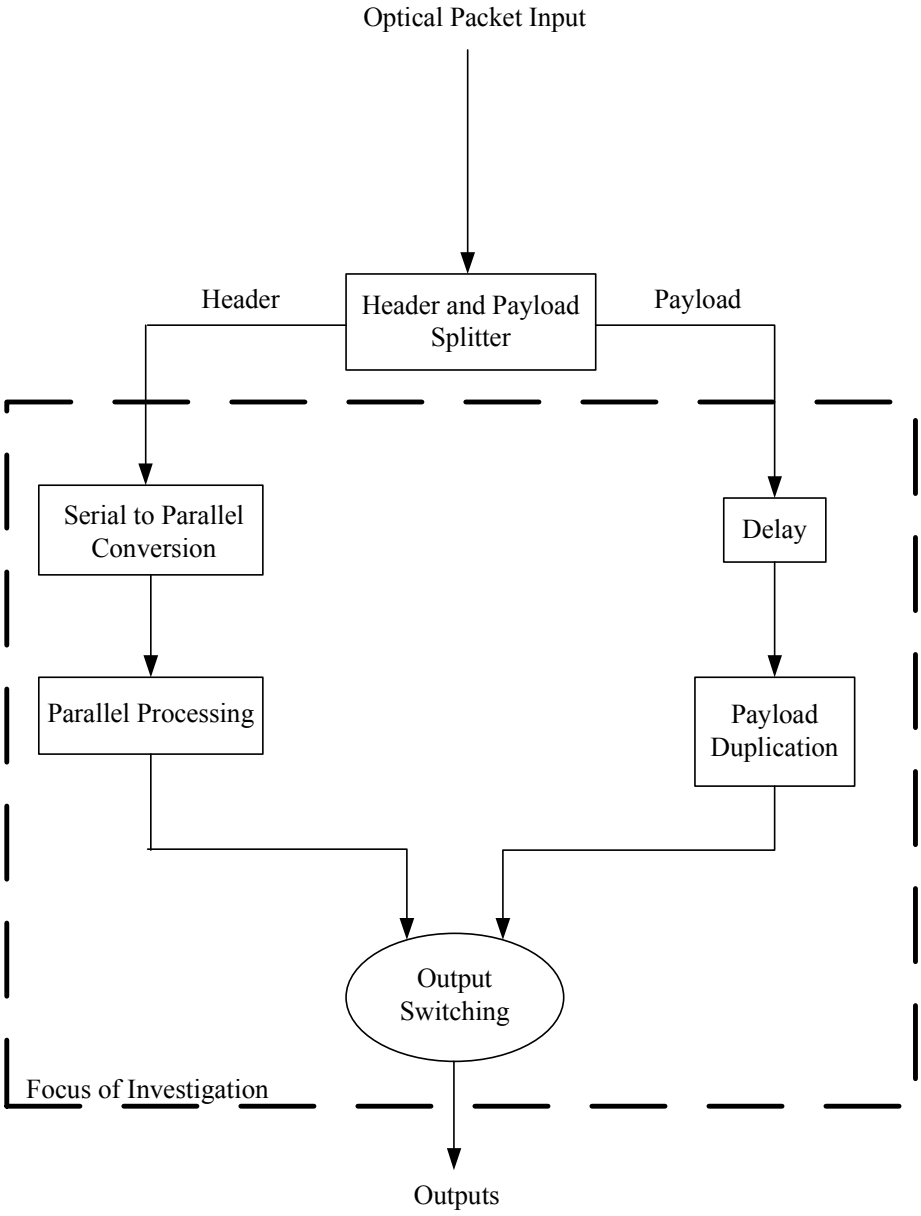

Figure 1.3

A Conceptual overview of the packet switching architecture to be investigated.

The proposed packet-switch accepts the header and payload packets on different input fibres. The focus of this investigation is shown in figure 1.3 as the striped block. The header and payload splitter is shown here for completeness.

In figure 1.3 the optical header bits enter the packet switch on the left and the optical payload bits enter the packet switch on the right. While the payload bits get delayed as they enter the packet switch, the header bits are converted from series to parallel. After the conversion the header bits are processed in their parallel state two bits at a time. The output

of the parallel processing is then fed to the output switches where the payload meets up with the parallel processing output. The payload then gets switched to the correct output fibre according to the parallel processing output. The output switching function consists of two optical switches. The first switch has as its inputs the processing output and a duplicate of the payload packet. The second switch has as its input an inverted version of the processing output and a duplicate of the payload. Thus the output switching function will need an inverting function and two switching functions. Possible inverters and switches are discussed in section 2 of this chapter. A more detailed description of the exact structure of the self routed switch used in this investigation will be given in chapter 2.

5. APPROACHES

Optical parallel processing solutions to all-optical packet routing have been proposed in the form of Optical Neural Networks [10], [11]. The disadvantage of the neural network approach is that the training of the neural network needs to be supervised and often happens in the electronic domain.

The crux of this investigation's parallel optical processing technique will be the nonlinear optical threshold function. In this research investigation a nonlinear optical threshold function will be used extensively and thus different options will be looked at and discussed in the following paragraphs.

A typical ideal nonlinear switching function is shown in figure 1.4 below.

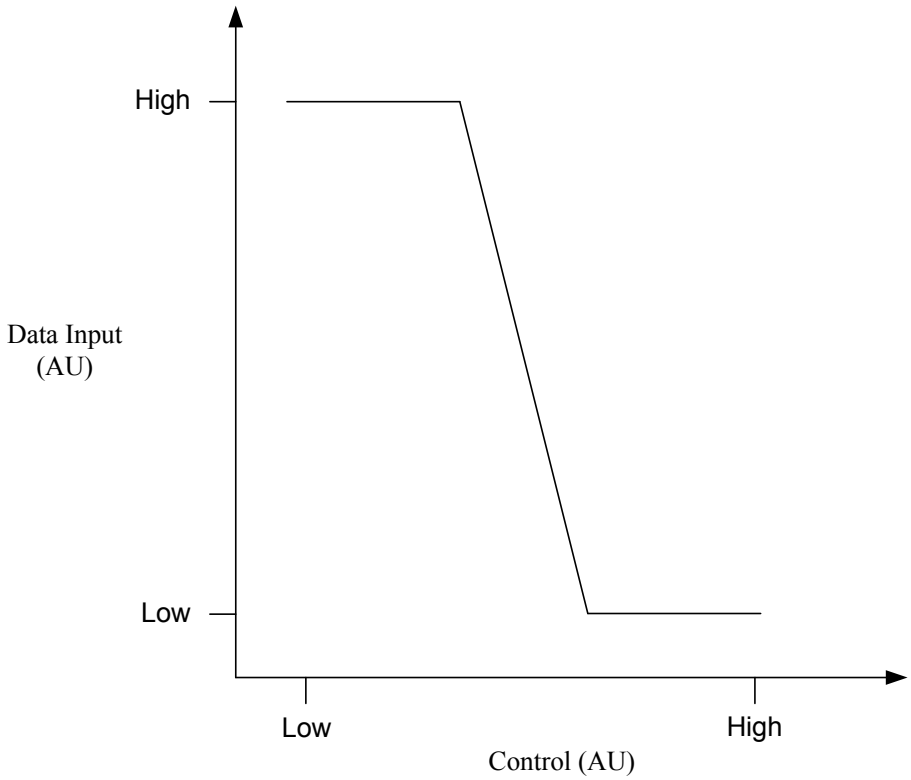

Figure 1.4

Typical ideal nonlinear function that is used for switching in arbitrary units (AU).

The nonlinear threshold function is where the processing takes place. In figure 1.4 it can be seen that when the control signal is low (or zero) the output is equal to the data signal. In this case the data signal is high (or one) and thus the output is also high. If instead the data signal was low then the output would also be low when the control signal is low. When the control signal is high the data signal gets suppressed and the output is low whether the data signal is high or not.

Some nonlinear threshold functions for optical networks include the interaction between coupled lasers [10], gain competition between lasing modes in a shared gain medium [12], InP based switch exploiting carrier induced refractive index change [13], [14], optical Stark effect in multiple quantum well structures [15], and the Kerr effect [16], [17]. A nonlinear optical device that has been used extensively is the Nonlinear Optical Loop Mirror (NOLM) by induced phase delay [14]. The NOLM device works on the principle of light-intensity induced nonlinear refractive index change in dispersion-shifted polarization maintaining fibre. The NOLM device approach to optical switching is attractive because of its passive nature and its all-optical demultiplexing nature. Unfortunately the long loop

fibre that has to be used in the NOLM makes it very sensitive to environmental and especially acoustic disturbances.

Another approach to the routing of an optical packet header is by using a self-routing all-optical switch [18]. This approach uses a specific index of refraction profile in a dispersion flattened fibre. It routes optical pulses based on their respective optical input intensities. Optical switching is also achieved using bandedge nonlinearities in semiconductor waveguides [19]. Semiconductor optical switching devices have been constructed using Semiconductor Optical Amplifiers in a Mach-Zehnder Interferometer (MZI) optical modulator configuration [20]. Three nonlinear optical switch geometries are shown in figures 1.5, 1.6 and 1.7 [21]. These nonlinearities are based on a resonant excitation in an active or passive Semiconductor Optical Amplifier (SOA). The advantage of using a SOA as a nonlinear optical device is that it requires low control pulse energy compared to the control pulse required when using passive devices as the nonlinear optical device. All three switches in figures 1.5, 1.6 and 1.7 use control pulses to briefly introduce a differential phase shift between interfering pulses to switch them to the output port. In all three the duration of the switching window is determined by the offset Δx.

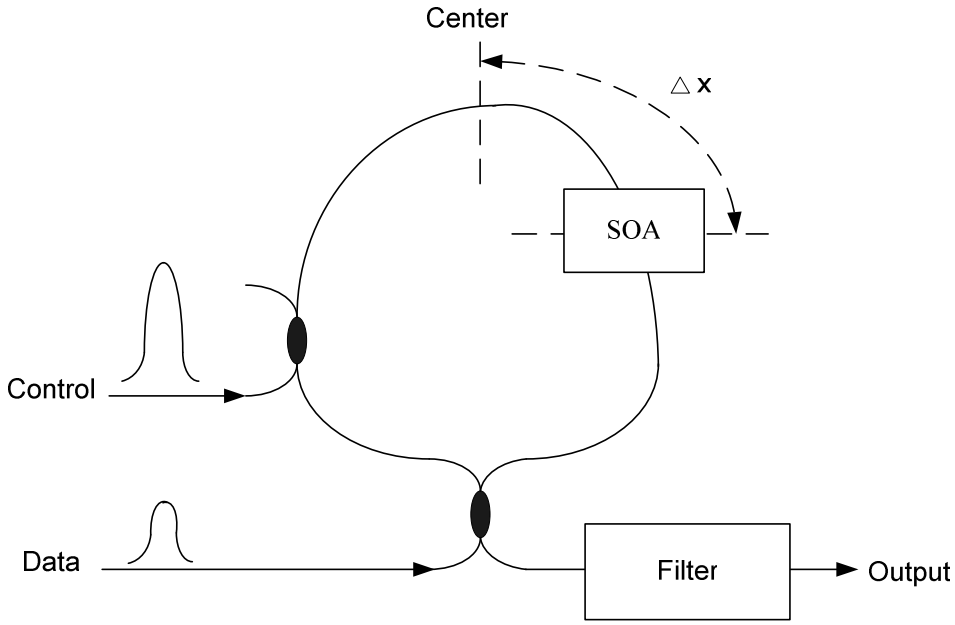

Figure 1.5

A Terahertz Optical Asymmetric Demultiplexer (TOAD) switch geometry.

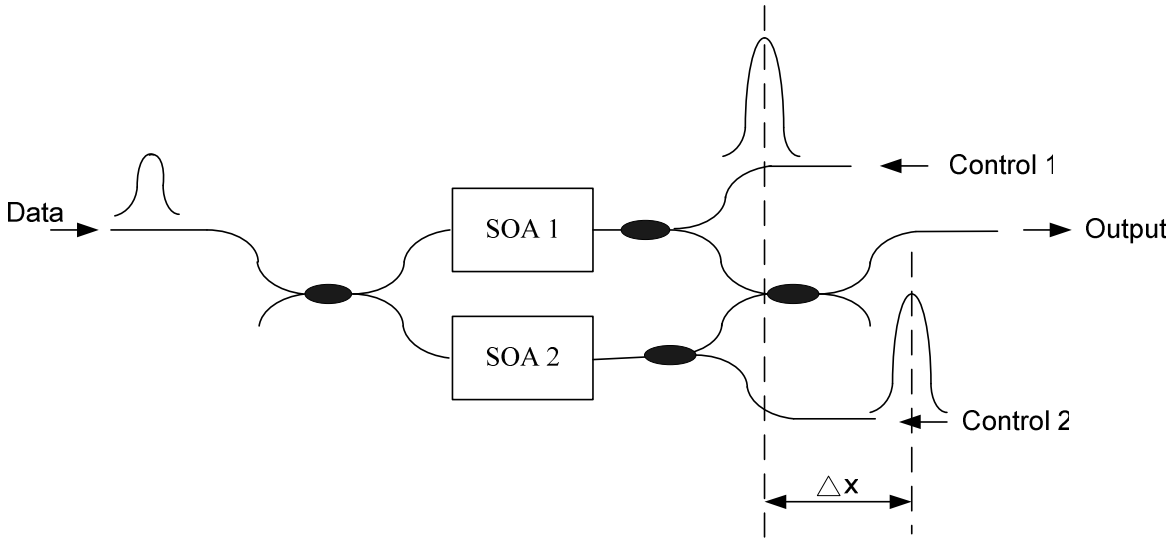

Figure 1.6

A Colliding Pulse Mach-Zehnder (CPMZ) switch geometry.

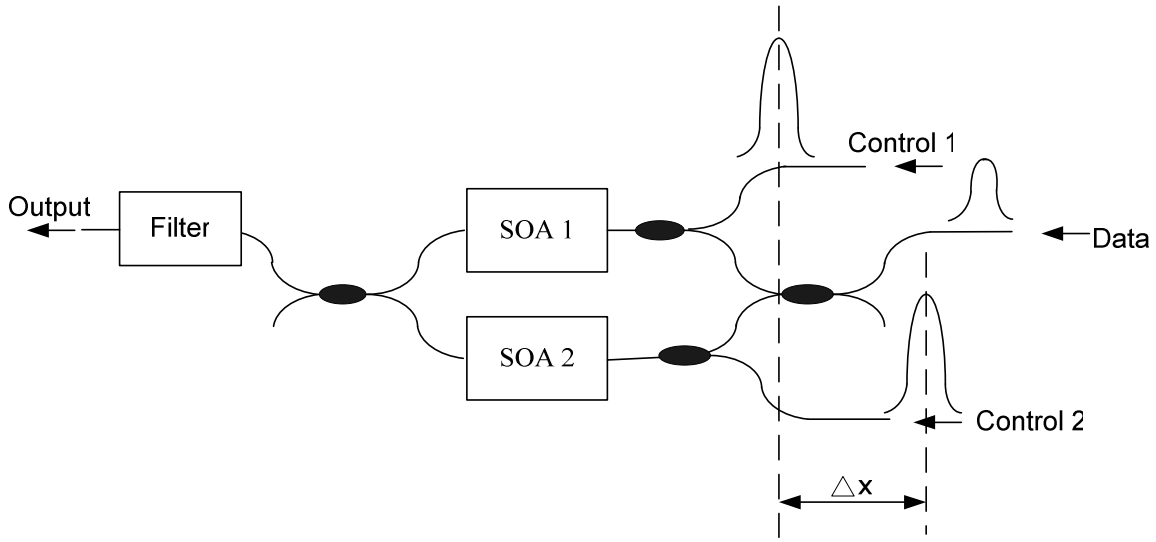

Figure 1.7

A Symmetric Mach-Zehnder (SMZ) switch geometry.

Of all three switch geometries shown in figures 1.5, 1.6 and 1.7 above the SMZ switch exhibits the best performance in terms of the minimum switching window width and output peak-to-peak amplitude. The optical switching node proposed in this research consists of a SOA in a Cross-gain Modulator (XGM) configuration.

One of the key components in optical signal processing technology is the semiconductor optical amplifier and because it is used in the XGM configuration of the switching node a discussion of the working of a SOA is necessary here in order to understand the operation of the XGM switch geometry. The SOA can be used as an optical amplifier in its linear region of operation, and in its saturation region of operation the SOA can be used in optical signal processing applications like time-domain multiplexing systems [22]. All optical amplifiers increase the power level of incident light through a stimulated emission process. Free carriers are created when an electron receives enough energy to bridge the bandgap energy of the semiconductor active layer and reach the valence band energy level. Both a hole and an electron are then created. When an optical signal enters a SOA active area it depletes some of the free carriers that are present by the process of stimulated emission in which the electrons recombine with the holes and emit photons of the same energy as the incident photons that caused the stimulated emission. The incident optical signal also creates free carriers by the process of absorption in the SOA active area. When an optical saturating signal is injected into a SOA active area the carrier density in the active layer reaches a steady state value after some time. If a short pulse is then injected into the SOA cavity after the saturating signal it depletes some of the carriers via stimulated emission after which the optical saturating signal's photons as well as the applied electric field creates carriers.

An analysis of the operation of an Semiconductor Laser Amplifier as an on/off gate is done by Ehrhardt *et al.* [23]. This forms the basis of the Cross-gain Modulator (XGM) used in this investigation.

Carrier recovery is regarded as the re-creation of electrons and holes that are available for amplification after a data pulse depleted some of the original carriers. The SOA carrier dynamics permit behavior such as high speed switching [24], [25] and clock division. Carrier recombination processes within the SOA cavity limit the speed of optical signal processing. For instance when two short pulses enter a SOA in quick succession then the first pulse would receive the normal amount of amplification, but the second pulse would receive less amplification because the first pulse's photons depleted the available carriers and the carriers couldn't recover fast enough to provide enough amplification depending on the time between the pulses and the SOA biasing current. The carrier recovery time is also

referred to as the carrier lifetime. The effective carrier lifetime within a SOA cavity is dependent on stimulated absorption in the presence of two energy levels. To decrease the recovery time of a SOA after a short optical pulse has passed through it, the SOA cavity can be pumped with a CW optical saturating signal, which is also called an optical holding beam.

Another attractive optical-switch alternative is the Kerr-switch. The refractive index of many optical materials has a weak dependence on optical intensity I (equal to the optical power (P) per effective area (A_{eff}) in the fibre) given by

$$n = n_0 + n_2 I = n_0 + n_2 \frac{P}{A_{eff}}, \qquad (1.1)$$

where n_0 is the ordinary refractive index of the material and n_2 is the nonlinear index coefficient. The nonlinearity in the refractive index is known as the Kerr nonlinearity and this nonlinearity can be found at the heart of many optical switching devices. This nonlinearity produces a carrier-induced phase modulation of the propagating signal, which is called the Kerr effect [26]. The Kerr effect approach to optical switching is attractive because of its passive nature and its all-optical switching prospect. A polarization independent Kerr-switch using a polarization diversity loop [16] has the advantages of being polarization independent, non-interferometric, using standard dispersion shifted fibre, and being insensitive to acoustical disturbances. This type of Kerr effect optical switch is inherently more stable than the NOLM device mentioned above. An experimental setup using the Kerr-switch as a demultiplexer is shown in figure 1.8 below [16].

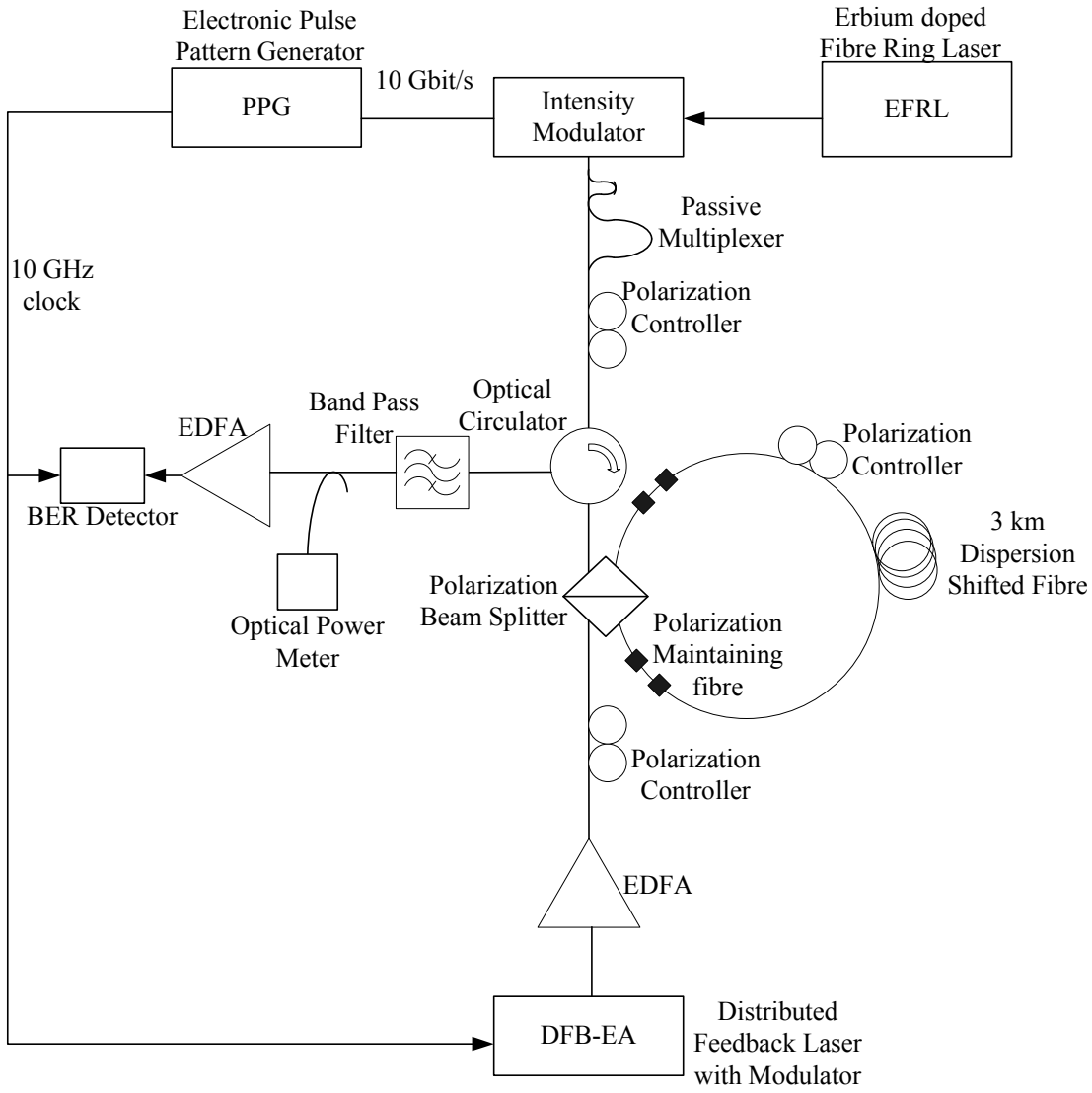

Figure 1.8

An experimental setup to test the structure of a polarization independent Kerr-effect switch [16]. Standard dispersion shifted fibre is used which is insensitive to acoustical disturbances.

The Kerr-switch works by feeding data and control signals into a polarization beam splitter (PBS) which splits the incoming light into its orthogonal polarization components. If the wavelength separation between the control and data signals is appropriate the difference in polarization angles between the data and control signal will be 45^0, which is required for maximum Kerr effect. When the data copropagates with an intense control pulse its polarization state will change nonlinearly due to cross phase modulation (XPM) from the control pulse. If the polarization state of the data signal is rotated 90^0 it will be reflected back to one of the input terminals of the PBS and retrieved by the circulator. The control

pulse polarization state at the input of the PBS should be oriented so that an equal amount of control power enters both ends of the loop fibre to achieve polarization independence of the input data [16].

The only other optical processing function that is used in the research investigation is the optical inverter. It is used in the output switching function as discussed in section 1 of this chapter. The optical inverter that is used in this research investigation is a modified version of the XGM optical switch discussed above. It is explained in chapter 2. One possible other choice for an optical inverter is discussed here.

An all-optical inverter with 1 picojoule switching energy is shown in figure 1.9 [27].

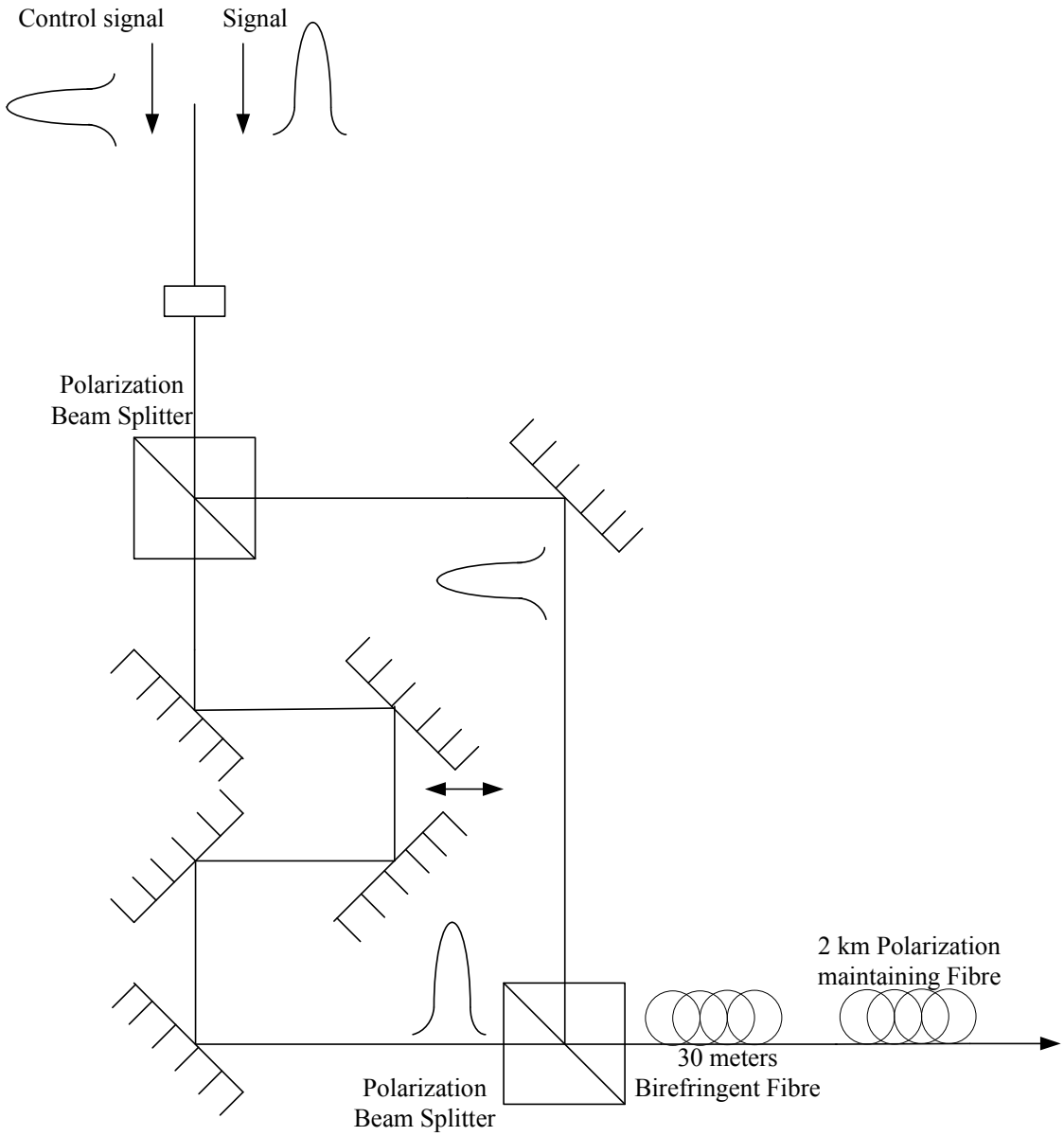

Figure 1.9

An experimental setup to test the structure of an optical inverter [22]. It uses Polarization Beam Splitters, mirrors, birefringent fibre, and polarization maintaining fibre. The control signal and the data signal have to be orthogonally polarized.

The inverter consists of a time domain chirp switch architecture which is divided into a nonlinear chirper followed by soliton dispersive delay line. In the absence of a data signal the control pulse propagates through and arrives at the output in the clock window. By adding the data signal it chirps (frequency shifts) the control pulse and the shift transforms into a time change ΔT after propagating in the dispersive section. The nonlinear chirper is realized by the moderately birefringent fibre and the soliton dispersive delay line corresponds to a long polarization maintaining fibre. A disadvantage of the optical inverter

shown in figure 1.9 is that the control signal and the data signal have to be orthogonally polarized.

There are also some other optical switch technologies that are worth mentioning here. In mechanical switches the switching function is performed by some mechanical means. One such a mechanical switch uses a mirror arrangement whereby the switching state is controlled by moving a mirror in and out of the optical path. Another type of mechanical switch bends or stretches a directional coupler in the interaction region and thus switches light from an input port between different output ports [28]. In terms of optical switches Micro-electro-mechanical systems (MEMS) refers to mini movable mirrors fabricated in silicon. These mirrors are deflected from one position to another using a variety of electronic actuation techniques [29], [30]. Another type of optical switch uses a planar waveguide approach where the switch actuation is based on fluid in a crossover point is heated and an air bubble is formed. This air bubble breaks the index matching, and as a result, the light is now reflected at that crossover point [31]. Liquid crystal cells offer another way for realizing small optical switches. These switches typically make use of polarization effects to perform the switching function. By applying a voltage to a liquid crystal cell the polarization of the light passing through the cell can be rotated or not and combined with passive polarization beam splitters and combiners it can yield a polarization independent switch [27], [28]. Some of these technologies promise to enable a very scalable, cost effective switching element along with reducing the need for optical to electrical to optical conversions. These attributes will drive the value of photonic networks [34], [35].

The new generation of optical networks requires intelligence in order to aid a wide range of functionalities in the optical domain. Network intelligence enables a wide range of new networking capabilities ranging from mesh networking to optical packet interworking [36]. Signal processing in high speed OTDM networks [37] will become important with the amount of internet traffic doubling every 100 days [38]. WDM packet routing [39] might also be an important alternative to signal processing for high speed packet-switched networks. WDM packet routing can also be used in conjunction with time domain signal processing in high-speed networks.

Chapter 2

STRUCTURE AND MATERIALS

The purpose of this investigation is to determine the feasibility of a unique all-optical switching node. To do this the investigation focussed on a three bit parallel processing architecture for the all-optical switching node. The structure of the proposed three bit parallel processing all-optical switching node is shown in figure 2.1 below.

It must be stressed here that although this research investigation focussed on a three bit parallel processing architecture (meaning it can only process three header bits at a single point in time) the concept can be further extended to process more than three header bits. The more header bits there are to process in parallel the more optical switches are necessary and the more complex the system becomes. Therefore three header bits were chosen in this research investigation because of the ease of illustration of processing three bits. For illustrative purposes a possible four bit parallel processing architecture is shown in Appendix B.

In the optical packet switching node of figure 2.1 below there are two optical fibre inputs and two optical fibre outputs. The one input is where the packet header enters (which contains the packet payload address). This packet header is then processed optically to determine to which one of the outputs the packet payload (which enters at the other input) should be routed to. In the setup of figure 2.1 the packet header and packet payload are accepted at separate input fibres. Thus in the network where this packet switch is used either the header and payload packets are separated before they reach the packet-switch, or the network architecture is of such a nature that the header and payload packets are separated throughout the entire network. The header and payload packets can easily be separated by utilizing two different wavelengths, wavelength filters and a splitter.

The header and payload don't necessarily have to be separated. If a large enough delay period is inserted into the original packet between the header and payload (to allow for transient effects created by the header packet in the output switches to die out) this packet

consisting of first the header packet and then the payload packet can then be fed to both inputs of the optical switch. The nature of the timing designed into the packet-switch in figure 2.1 above will then ensure that the payload packet gets switched. In this case the header packet will propagate to the next node even if the payload packet gets suppressed at the node.

In figure 2.1 the optical header packet input is split by a 3 dB splitter, dividing it into two copies of the original packet while the payload packet is delayed by two header bit length delays before being split and fed to the output switches. The header and payload packets consist of two different bit-rates (one for the header and one for the payload). A one constitutes optical power and a zero is indicated by zero optical power. One of the outputs of the splitter (one of the optical header packets) is delayed by one bit header length whilst the other is fed to the data input port of the first optical switch in the parallel processing architecture.

The header bits get split and delayed so that they can be processed via the XGM switches two at a time. The last two bits get processed first and their subsequent output gets inserted into the data input port of another XGM switch together with a delayed version of the first bit. The optical bit-sequence in the header packet that results in a unique routing output can be seen as constituting the individual addresses of a subnet or workstation. The bit sequences responsible for a specific routing output is determined by the physical XGM switch setup in the parallel header processing structure. Each header bit is 100 ps long (10 Gbps bit-rate FWHM) and each payload bit is 25 ps long (40 Gbps bit-rate FWHM). In this research investigation Gaussian shaped header and payload packages were simulated.

In figure 2.2 the payload packet that is received as input is delayed by roughly 250 ps (Refer to figure A.10 in Appendix A) before reaching the data input port of the XGM of the first output. Thus the first output's time window that is looked at in the experiments of Chapter 4 is between 250 ps and 340 ps (the length of the window being equal to the length of the payload packet). In figure 2.2 it can be seen that the packet payload input encounters two delays in its path from the input to the data input port of the second output's XGM. The first delay is the 250 ps and the second delay is 1.05 ns (Refer to figure A.10 in

Appendix A). Thus the second output's time window that is looked at in the experiments of Chapter 4 is between 1.3 ns and 1.39 ns.

The first delay of 250 ps was introduced because the payload packet has to appear at the first output's XGM switch during the time that the parallel header processing appears at the control input port of the same XGM switch, and the parallel processing output only appears at the control input of the first output's XGM switch after all three the header bits were processed. In this case the full header bit length is taken as 80 ps and thus the headers appear at the control input port of the first output's XGM switch at 240 ps. The payload packet input is given an additional 10 ps (resulting in 250 ps) delay because of transients that occurs as a result of the parallel processing output appearing at the control input. The second delay of 1.05 ns (resulting in a total delay of 1.3 ns) was introduced in the payload packet's path to the data input port of the second output's XGM switch because the parallel processing output (which only appears after 240 ps) is delayed by an additional 1.05 ns to cater for the big initial transient that occurs in the inverter because of the step response it gets from the CW laser at start-up (refer to figure 2.3 for a schematic of the setup of the inverter).

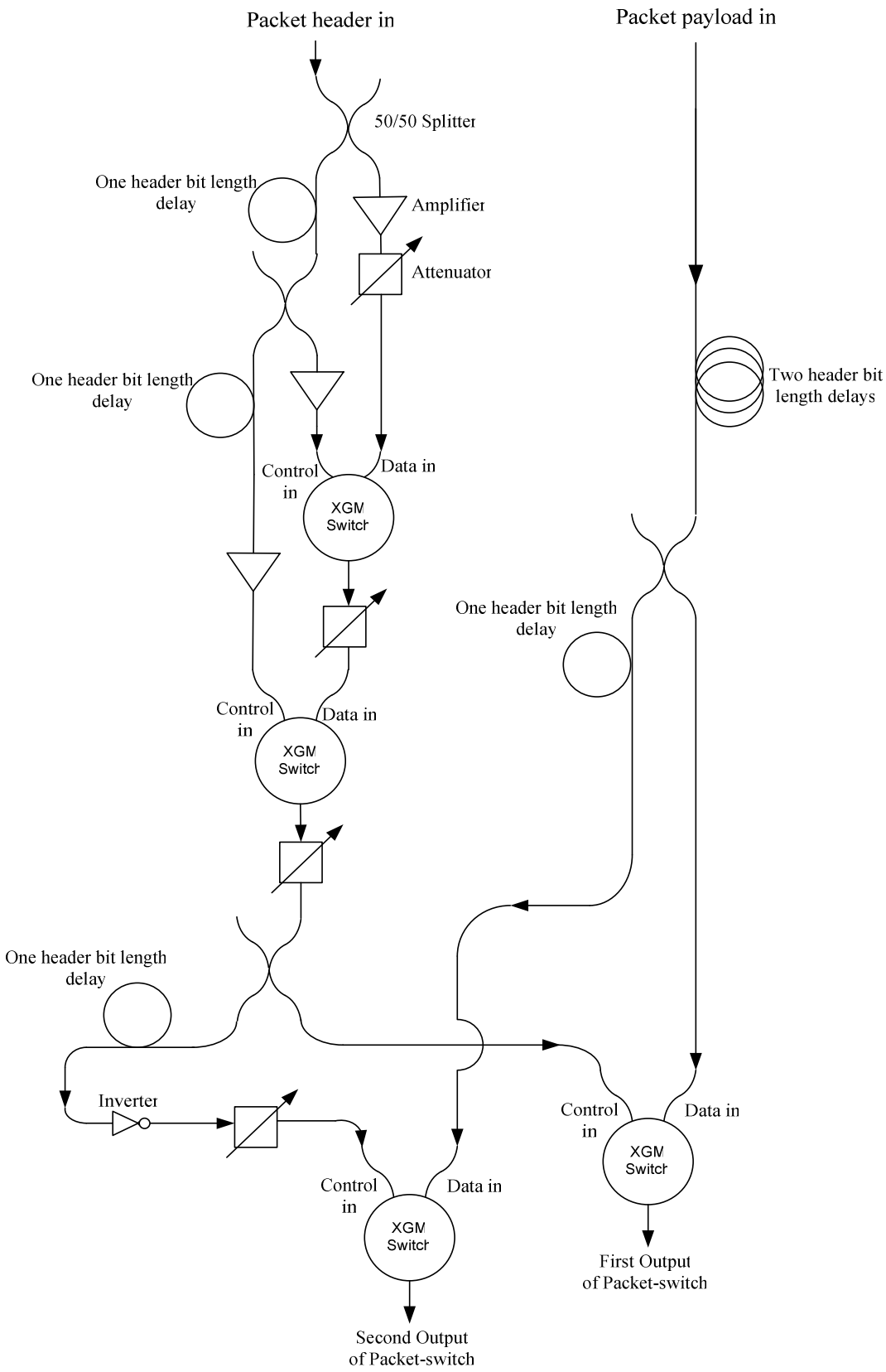

Figure 2.1

An optical switching node using a unique three bit parallel processing technique and output switches.

The basic building block used in the switching node is the XGM switch which is shown in figure 2.2 below. This switch is used as the nodes in the parallel processing architecture, as the crux of the optical inverter shown in figure 2.3, and as the payload gates at the respective outputs. The output of the parallel processing structure is split and one version is fed into an inverter of which the output enters the control input port of an XGM switch in order to suppress or amplify a version of the payload packet. The other version of the split parallel processing output is fed directly into the control input port of another XGM switch in order to suppress or amplify another version of the payload packet oppositely to the first output switch.

The packet switching node of figure 2.1 can be made to process more header bits by adding more XGM switches in parallel in the same fashion as the two XGM switches were linked in figure 2.1. In figure 2.1 the first two XGM switches, which the packet header encounters, combines to build the three bit parallel processing architecture.

The structure of the XGM switches used in the switching nodes in figure 2.1 above is shown in figure 2.2 below. Refer to chapter 1 for a description of the operation of the SOA that is used as the building block of the XGM switch in figure 2.2.

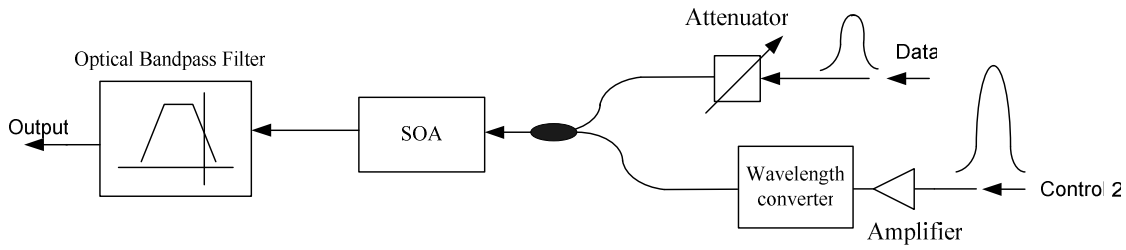

Figure 2.2

Structure of the cross-gain modulator which is the basic building block of the inverter and the switching node.

In figure 2.2 above the wavelength converter changes the wavelength of the control input to a wavelength that gets filtered out by the optical bandpass filter so that only the data input is present at the output fibre of the switch. The structure of the optical inverter used in the structure of the switching node in figure 2.1 above is shown in figure 2.3 below.

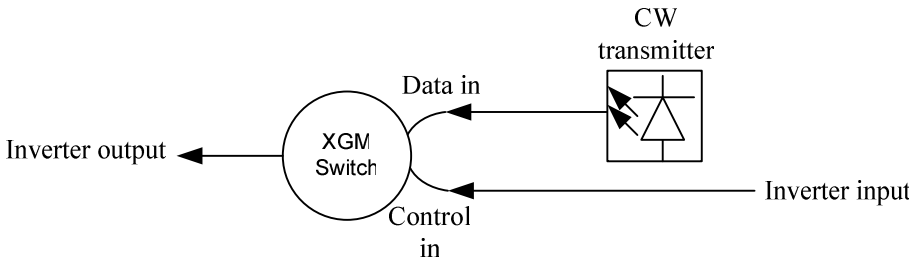

Figure 2.3

Structure of an optical inverter which is built using the optical switch of figure 2.2 and a CW transmitter.

In the inverter of figure 2.3 the output of the inverter is an amplified version of the CW input signal when there is no signal present at the inverter input. When a signal appears at the inverter's input it depletes the free carriers in the active area of the SOA in the switch geometry and as a result the inverter's output power decreases because there aren't many free carriers left to amplify the CW input signal via the process of amplified stimulated emission. Thus in summary when no signal is present at the inverter's input a large optical signal is present at the inverter's output, and when a signal is present at the inverter's input the inverter's output signal becomes smaller. The function of the inverter is to suppress one of the packet outputs so that a payload packet will appear at only one of the packet switch outputs.

The input/output table for the XGM structure of figure 2.2 is shown in table 2.1 below.

Table 2.1

This table shows all the combinations of logical inverter input and inverter CW data input resulting in a specific logical output for the cross-gain modulator switch structure of figure 2.2. A logical one indicates the presence of an optical signal where a logical zero indicates the absence of an optical signal.

Control input	Data Input	Output
0	0	0
0	1	1
1	0	0
1	1	0

From table 2.1 it can be seen that only when the data input signal is present and the control input signal is absent will there be an output signal present. Using table 2.1 an input/output

table can be created for the inverter structure of figure 2.4. This input/output table is shown in table 2.2 below.

Table 2.2

This table shows all the combinations of logical control input and data input resulting in a specific logical output for the cross-gain modulator switch structure of figure 2.2. A logical one indicates the presence of an optical signal where a logical zero indicates the absence of an optical signal.

Inverter input (Control input)	CW Input (Data input)	Inverter Output
0	1	1
1	1	0

In table 2.3 below the information in tables 2.1 and 2.2 is used in the structure of figure 2.1 to predict at which output of the switching node the packet payload will exit.

Table 2.3

This table shows all the combinations of header input sequences and the corresponding switching node output that the payload packet exits (as labeled in figure 2.1). A logical one indicates the presence of an optical signal where a logical zero indicates the absence of an optical signal.

Header input sequence	Switching node output
000	First
001	Second
010	First
011	First
100	First
101	First
110	First
111	First

Figure 2.4 shows the typical application envisaged for the optical switching node of figure 2.1.

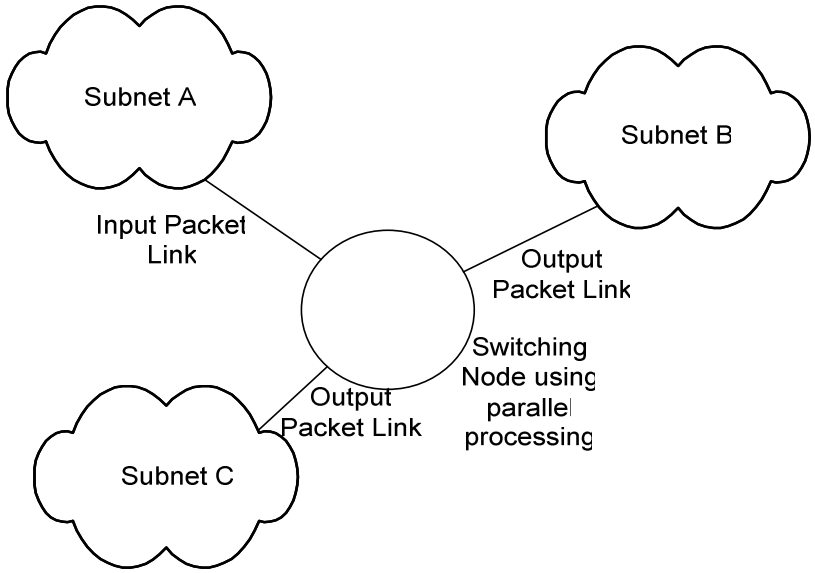

Figure 2.4

Typical application envisaged for the optical switching node of figure 2.1.

In figure 2.4 the optical switching node receives an optical packet with a header bit sequence at 10 Gbps and a payload at 40 Gbps from subnet A. It processes the header sequence of the packet and switches the packet payload to either subnet C or subnet D depending on the header bit sequence.

Chapter 3

METHOD

In order to ascertain the feasibility of the three bit all-optical packet switch of figure 3.1 different simulated experiments were conducted (refer to Chapter 4 for the results). The basic functional layout of the simulated experiments is shown in figure 3.1 below.

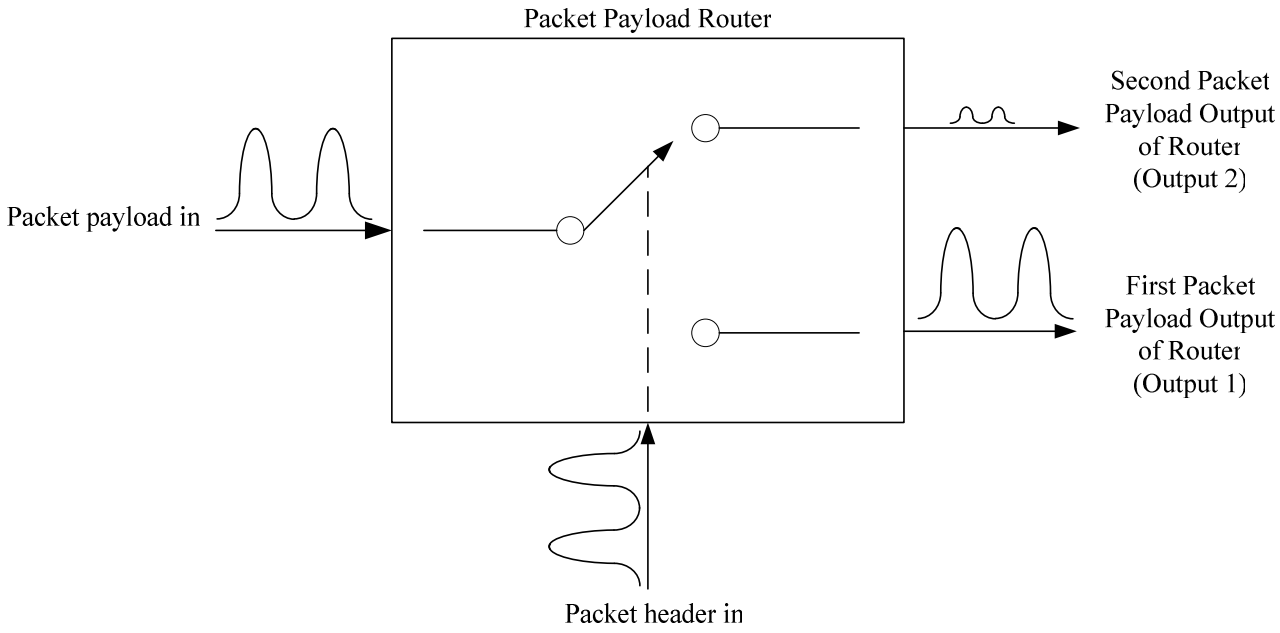

Figure 3.1

Basic functional layout of the simulated experiments. The packet header determines at which output the packet payload should exit. The packet payload switching node that is used can be seen in figure 2.1. Output 1 of this figure corresponds to the First Output of Figure 2.1 and Output 2 of this figure corresponds to the Second Output of Figure 2.1.

In figure 3.1 the packet header determines at which output the packet payload should exit. Only one unique sequence of packet header optical bits will result in the packet payload exiting at one of the outputs (e.g. output 1) of the switching node and being attenuated at the other (e.g. output 2). For all other sequences of packet header optical bits the packet payload will exit at the opposite output (e.g. output 2) and be attenuated at the other output

(e.g. output 1). The packet payload switching node that is used in figure 3.1 can be seen in figure 2.1, and Output 1 of figure 3.1 corresponds to the First Output of Figure 2.1 and Output 2 of figure 3.1 corresponds to the Second Output of Figure 2.1.

In the simulated experiments different header and payload input sequence combinations were tested and both outputs analysed. Each simulated experiment consisted of a three bit header input at 10 Gbps (i.e. each header bit was effectively a 50 ps FWHM gaussian pulse) and a three bit packet payload input at 40 Gbps (i.e. each payload bit was effectively an 8 ps FWHM gaussian pulse). The configuration of the parallel processing determined what header sequences resulted in what output switching situations (i.e. at which output the packet payload was suppressed and at which output the packet payload was amplified). Only two header bit sequences (101 and 001) were simulated with all eight possible three bit payload combinations because they showed all the possible outcomes clearly. The other six header bit sequences (000, 010, 011, 100, 110 and 111) all had the same effect as the 101 header bit sequence and were thus just simulated with a payload sequence of 111 for completeness. There were only two possible types of results. The first possible type of result was that the payload was suppressed (relative to the other output of the switching node) at Output 2 (measured on OSA 4 in figure A.11) and amplified (relative to the other output of the switching node) at Output 1 (measured on OSA 5 in figure A.11). The second possible type of result was that the payload was suppressed (relative to the other output of the switching node) at Output 1 and amplified (relative to the other output of the switching node) at Output 2. Only one payload bit sequence (111) was simulated with all eight of the different header bit sequences to illustrate the concept. By looking at the functional layout as shown in figure 3.1 and comparing it with the structural layout in figure 2.1 it can be seen that the SOAs in the switches will only need to operate at the header bit-rate of 10 Gbps. This is because only the first two switches have 10 Gbps signals as inputs and thus have to change state at this bit-rate. At the output switches the header processing block's output is at 10 Gbps and this signal effects a change of state in the output switches which results in a steady state for the payload bit-rate of 40 Gbps. Thus the 40 Gbps payload only sees saturation or gain at the output switches for the period that it passes through the output switches. The header processing output arrives at the output switches, effects a change to saturation or gain in the switches and then when the change has been effected and has stabilized the payload packet arrives and either passes through the switches or not depending on the change effected by the header processing output. From the fact that the parallel header processing output is only as long as an individual header bit and the fact

that the header processing output effects a change in the output switches which effects the payload packet when it reaches the individual output switches it can be concluded that the common length of the individual header bits determine the length of the payload packet i.e. the total payload packet length can only be smaller than the total length of a single bit of the header so as to also allow for the time it takes to effect a change in the output switches. Therefore a longer header bit length will enable larger payload packets. Larger payload packets can also be obtained by increasing the payload packet length.

In all of the experiments both the header and the payload wavelength was 1554 nm (193.1 THz). In the switches the header's wavelength gets converted to 193.2 THz at the control input but stays at 193.1 THz at the data input. The XGM output filter then only lets the 193.1 THz data input through and filters out the wavelength converted control input at 193.2 THz (refer to figure 2.2).

Table 3.1 below shows all the simulated experiments that were carried out (in terms of the changing input parameters) and their character allocation used to identify them in section 1.1 to section 1.8 of chapter 4.

Table 3.1

All the combinations of header input bit sequence and payload input bit sequence that was simulated and their respective character allocations. A 1 indicates a relatively large optical power and a 0 indicates an insignificantly small optical power.

Experiment character	Header input sequence (at 10 Gbps)	Payload input sequence (at 40 Gbps)
A	000	111
B	001	000
B	001	001
B	001	010
B	001	011
B	001	100
B	001	101
B	001	110
B	001	111
C	010	111
D	011	111
E	100	111
F	101	000

F	101	001
F	101	010
F	101	011
F	101	100
F	101	101
F	101	110
F	101	111
G	110	111
H	111	111

From figure 3.1 it can be seen that there were only two input parameters, namely packet header and packet payload bit sequences. All other parameters in the experiment were constant and were determined by a combination of simple calculations and experimental trial and error.

The success of the routing was measured by the switching ratio. The switching ratio is a power ratio between the first output of the switching node and the second output of the switching node. This ratio is given by

$$\alpha = \frac{P_1}{P_2}, \tag{3.1}$$

where α is the switching ratio, P_1 is the maximum optical power for a one bit at the first output of the switching node (Output 1) and P_2 is the maximum optical power for a one bit at the second output of the switching node (Output 2). In dB the switching ratio will look as follows

$$\alpha_{dB} = 10\left(\log\left[\frac{P_1}{P_2}\right]\right). \tag{3.2}$$

From equation 3.2 it can be seen that when P_1 is larger than P_2 the switching ratio would be positive, and that when P_2 is larger than P_1 the switching ratio would be negative. Thus in abstract terms a negative switching ratio would indicate that the payload packet exited at the second output (Output 2) and a positive switching ratio would indicate that the payload packet exited at the first output (Output 1).

As can be seen from equation 3.1 the switching ratio is dependant on the optical power of a one bit at the first and second outputs of the switching node. By looking at figure A.10 and A.11 and summing all the delays it can be seen that the payload packet will appear at OSA

4 (Output 2) after 1,3 ns. This happens because there is a 250 ps delay and a 1,05 ns delay in the light path from the packet payload input to the second output of the switching node. Thus in the experiments the measurements for three optical payload bits at the second output of the switching node was taken during a period which included the 1,3 ns to 1,4 ns window in order to include zero to one and one to zero gradients. This will be referred to as the output switching window for output 2. By using the same method the output switching window of first output of the switching node was determined to be 250 ps to 350 ps. This output switching window for each output is calculated by adding up all the delays between the packet payload input and the specific packet payload output in figures A.10 and A.11 (the reasons for these delays were given in Chapter 2). The reason the two output windows differ is because the input header bits follow different paths to the output switches (switch 3 and switch 4 in figure A.11). The main reason behind the difference in time delay between the two header bit paths is the 1,05 ns delay introduced prior to the inverter. This delay was introduced in order to allow the inverter time to stabilize. This initial oscillation of the inverter output is the result of the initial step input of the CW laser that feeds the data input of the inverter. As such this initial oscillation does not have to be catered for when the device has been in operation for some time and thus in practice the output windows can both be 250 ps to 350 ps.

The 250 ps delay was inserted into the light path of the packet payload to enable the packet header to completely pass through the parallel processing before the output of the parallel processing and the packet payload meet at the input to XGM switch at the first output of the switching node. The 1,05 ns delay was inserted into the light path of the split version of the packet payload to enable the inverter to reach a saturated state before the packet payload reached the input to the XGM switch at the second output of the switching node.

Appendix A shows the diagrams that were created in VPItransmissionMaker^{TM} in order to execute the above-mentioned experiments. VPIsystems^{TM} provides VPItransmissionMaker^{TM} which is an optical fibre communication system simulation package. VPItransmissionMaker^{TM} allows the designer of an optical network or component to decide the trade-off between simulation speed and accuracy. It has the ability to simulate the electrical and the optical domain; it can simulate a Wavelength Division Multiplexing (WDM) optical network, an OTDM network, or a simple analogue optical channel.

VPItransmissionMaker™ is a fourth generation Photonic Design Automation (PDA) tool. The first generations of PDA tools were largely proprietary modules devised to tackle discrete specialist design tasks, such as semiconductor lasers and optical waveguides. The second generation allowed many components to be interconnected to form circuit and system models, but were limited to a single signal format, best suited for a particular scale of problem.

The third generation was Photonic Transmission Design Suite (PTDS). This included multiple signal modes and representations to allow many types of simulation tasks to be represented efficiently by mapping the problem onto an optimum set of signal types. The power of PTDS was that all types of signal could be represented in a single simulation environment. Signal representations could be mapped onto a problem both spatially and spectrally.

The reason VPItransmissionMaker™ was chosen as the design tool in this research investigation was that it contains the features of PTDS as well as the additional features of co-simulation capabilities, a tailored Graphical User Interface (GUI), and an extensive library. A co-simulation capability indicates the capability to integrate third party tools and tailored models alongside a comprehensive library of component and system models. The extensive library consists of photonic modules covering the latest photonic technologies over several levels of abstraction, from detailed physical models, to black box, measured and data sheet models. Appendix A also discusses more details about the VPItransmissionMaker™ architecture that was created for this research investigation.

Chapter 4

SIMULATION RESULTS

This section contains the results obtained in the simulated experiments indicated in table 3.1. The results consisted of two time vs. optical power graphs (one for each output of the switching node) as well as one time vs. optical power graph for the packet payload input which gave the resultant output graphs. In each sub-section the first graph shows the optical power vs. time at the packet payload input (refer to figure 2.1), the second and third (sequentially) graphs show the optical power vs. time at the respective outputs of the switching node. Each sub-section has a constant gaussian header sequence input.

1. RESULTS

1.1 Simulated experiment A

In this experiment the header bit sequence was absent (i.e. a header bit sequence of 000). Figure 4.1 shows the payload input power versus time for a 111 payload bit sequence.

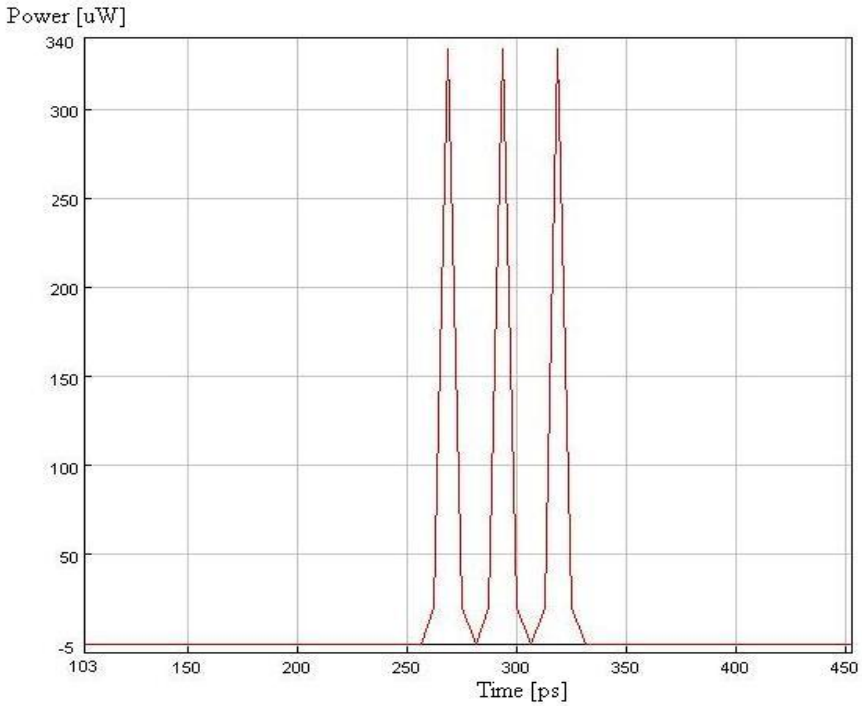

Figure 4.1

This figure shows the payload input power vs time for a 111 payload bit sequence (as seen on OSA 1 in figure A.10) .

Figure 4.2 shows the output power versus time (as seen on OSA 5 at the output of XGM switch 3 in figure A.11) when the header bit sequence is absent and the payload input bit sequence is 111. This is the first output of the optical switching node (output 1).

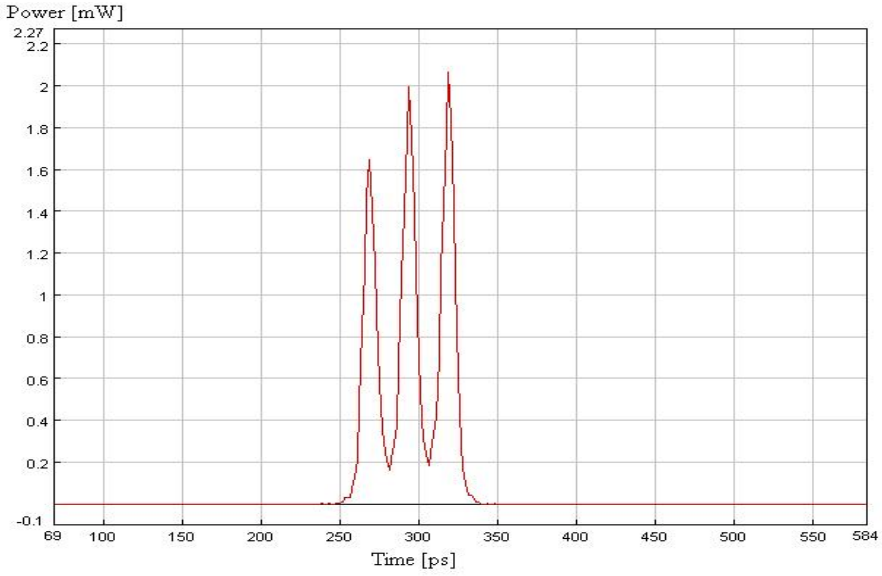

Figure 4.2

This figure shows the output power versus time at output 1.

Figure 4.3 shows the output power versus time (as seen on OSA 4 at the output of XGM switch 4 in figure A.11) for the same input sequences. This is the second output of the optical switching node (output 2).

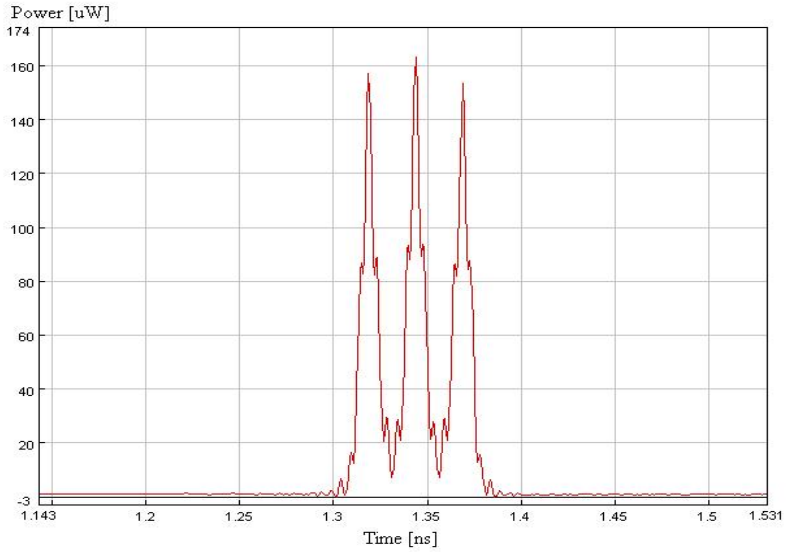

Figure 4.3

This figure shows the output power versus time at output 2.

By comparing figure 4.2 with figure 4.3 it can be seen that the payload got amplified to about 1.6 mW at output 1 and that at output 2 the payload amplification was suppressed and the payload stayed at roughly 160 μW. Thus from equation 3.1 the switching ratio is

$$\alpha = \frac{1.6mW}{160\mu W}, \tag{4.1}$$

$$\therefore \alpha = 10, \tag{4.2}$$

$$\therefore \alpha = 10\text{dB}. \tag{4.3}$$

1.2 Simulated experiment B

In this experiment the header packet was a 001 bit sequence. Figure 4.4 shows the payload input power versus time for a 001 payload bit sequence.

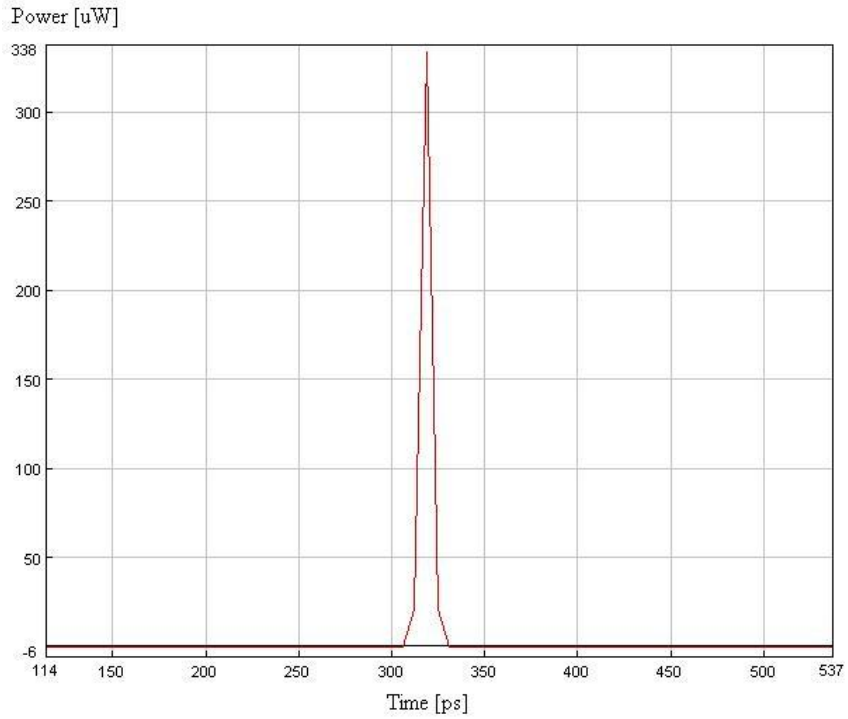

Figure 4.4

This figure shows the payload input power versus time for a 001 payload bit sequence.

Figure 4.5 shows the output power versus time at output 1 when the header bit sequence is 001 and the payload input bit sequence is 001.

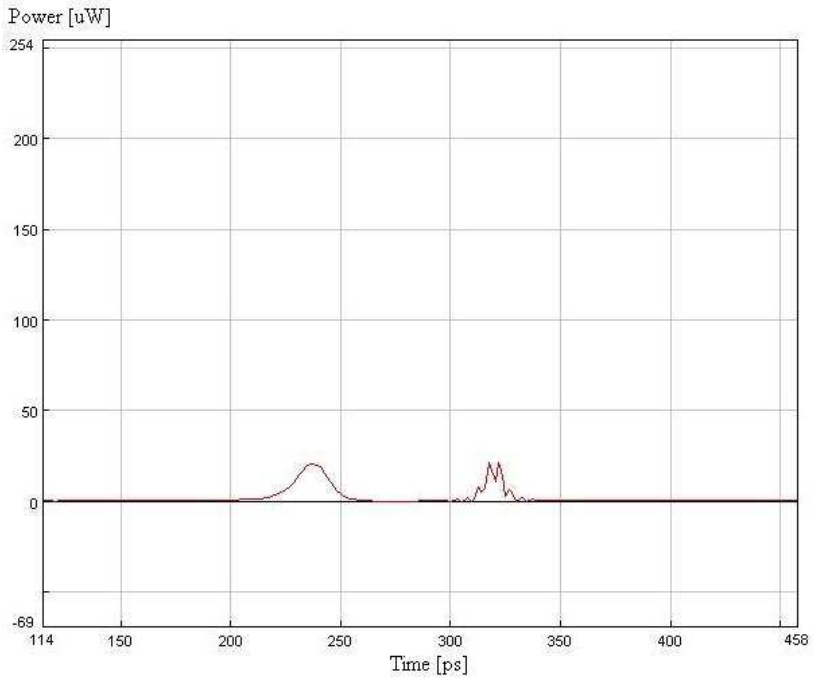

Figure 4.5

This figure shows the output power versus time at output 1.

Figure 4.6 shows the output power versus time at output 2 when the header bit sequence is 001 and the payload input bit sequence is 001.

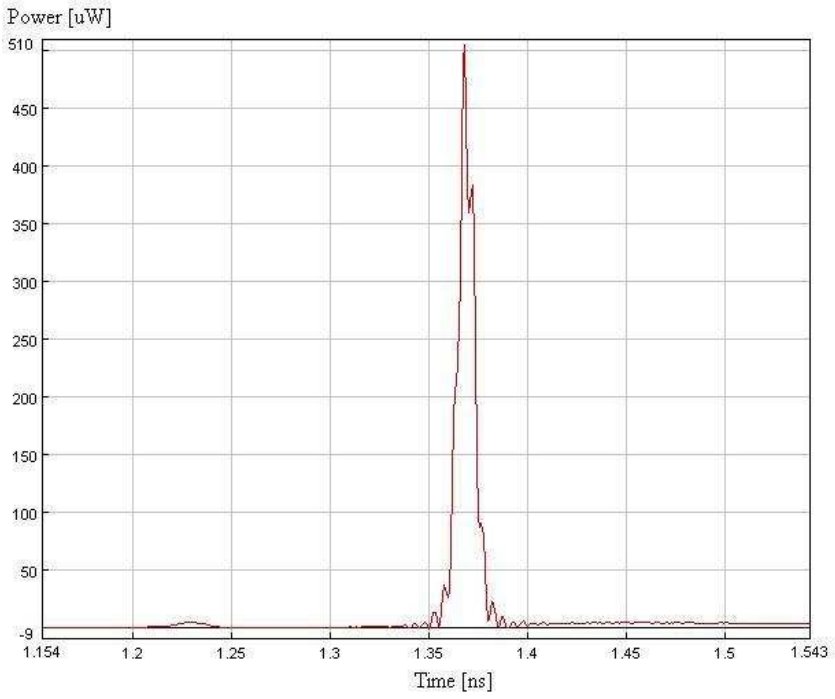

Figure 4.6

This figure shows the output power versus time at output 2

By comparing figure 4.5 with figure 4.6 it can be seen that the payload got amplified to about 510 µW at output 2 and that at output 1 the payload amplification was suppressed and the payload output reached a peak at roughly 20 µW. Thus from equation 3.1 the switching ratio is

$$\alpha = \frac{20\mu W}{510\mu W}, \tag{4.4}$$

$$\therefore \alpha = 0.04, \tag{4.5}$$

$$\therefore \alpha = -14.1\text{dB}. \tag{4.6}$$

Figure 4.7 shows the payload input power versus time for a 010 payload bit sequence.

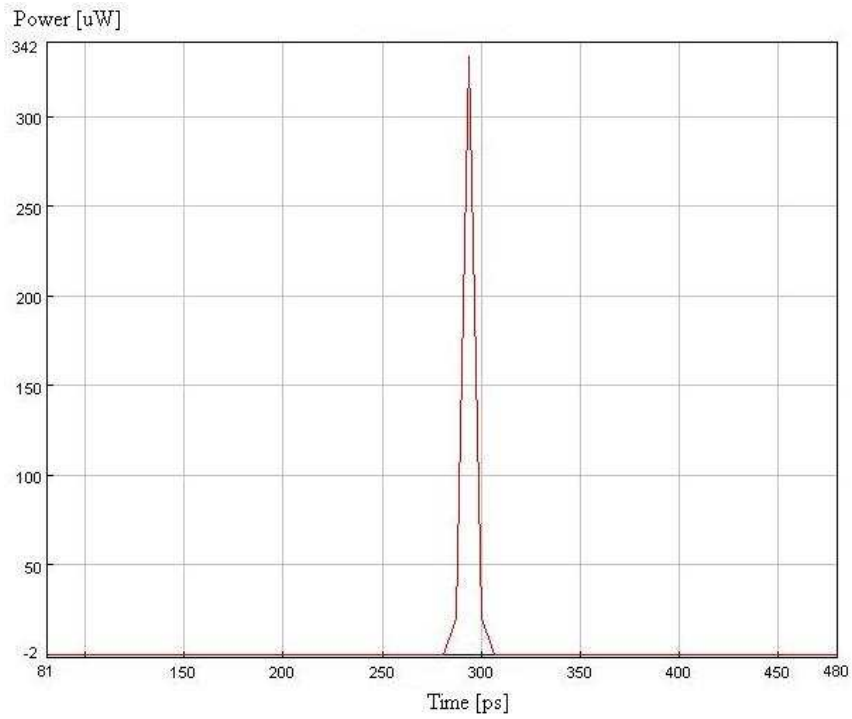

Figure 4.7

This figure shows the payload input power versus time for a 010 payload bit sequence.

Figure 4.8 shows the output power versus time at output 1 when the header bit sequence is 001 and the payload input bit sequence is 010.

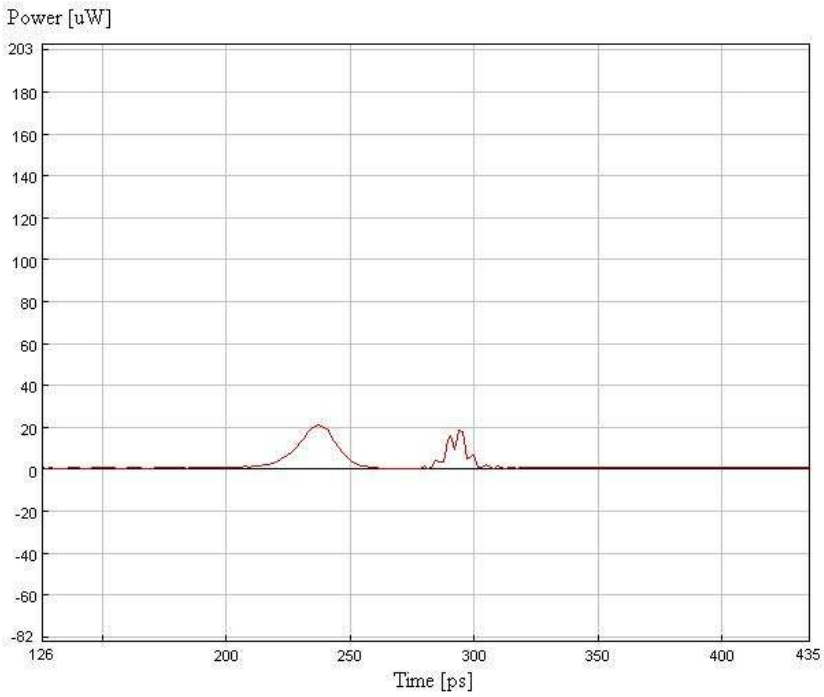

Figure 4.8

This figure shows the output power versus time at output 1.

Figure 4.9 shows the output power versus time at output 2 when the header bit sequence is 001 and the payload input bit sequence is 010.

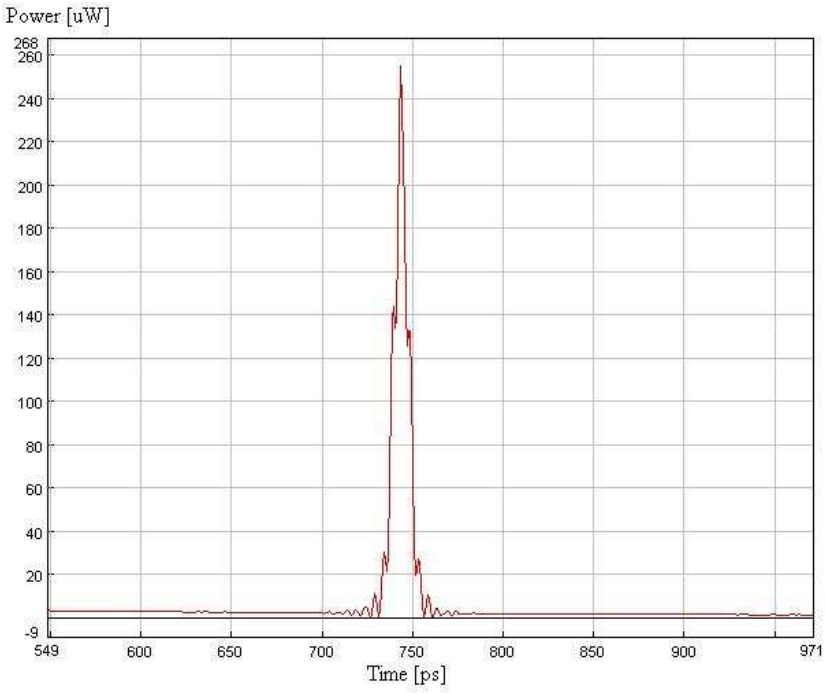

Figure 4.9

This figure shows the output power versus time at output 2.

By comparing figure 4.8 with figure 4.9 it can be seen that the payload got amplified to about 255 uW at output 2 and that at output 1 the payload amplification was suppressed and the payload output reached a peak at roughly 20 µW. Thus from equation 3.1 the switching ratio is

$$\alpha = \frac{20\mu W}{255\mu W}, \tag{4.7}$$

$$\therefore \alpha = 0.08, \tag{4.8}$$

$$\therefore \alpha = -10.7\text{dB}. \tag{4.9}$$

Figure 4.10 shows the payload input power versus time for a 011 payload bit sequence.

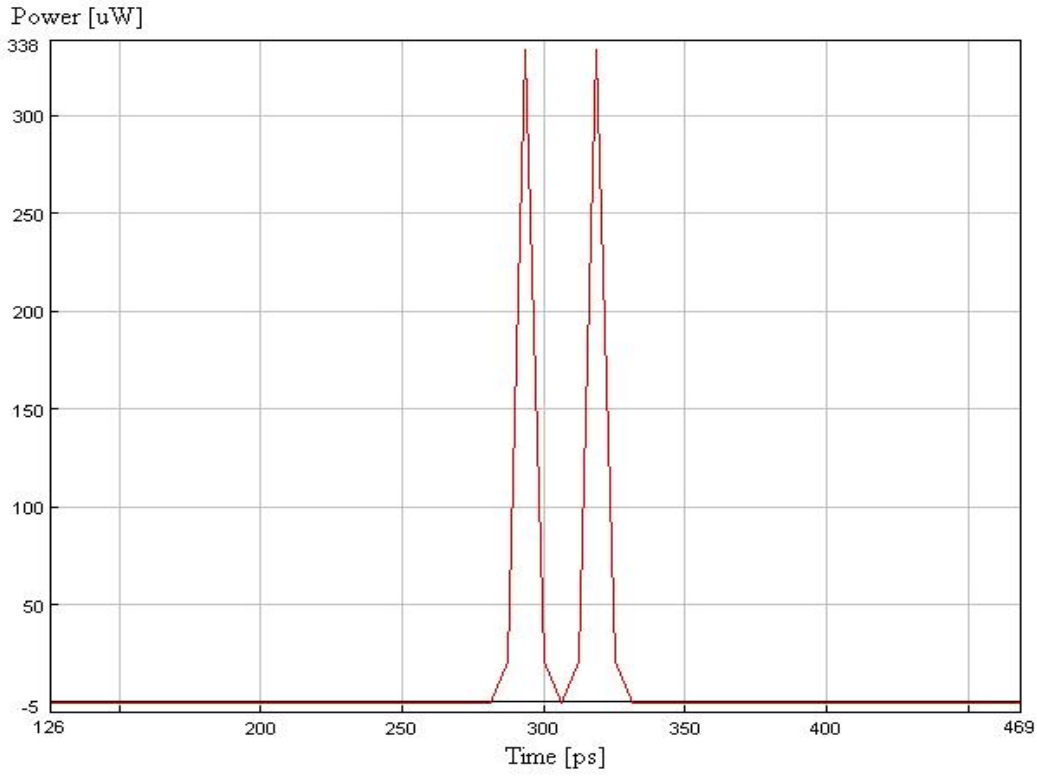

Figure 4.10

This figure shows the payload input power versus time for a 011 payload bit sequence.

Figure 4.11 shows the output power versus time at output 1 when the header bit sequence is 001 and the payload input bit sequence is 011.

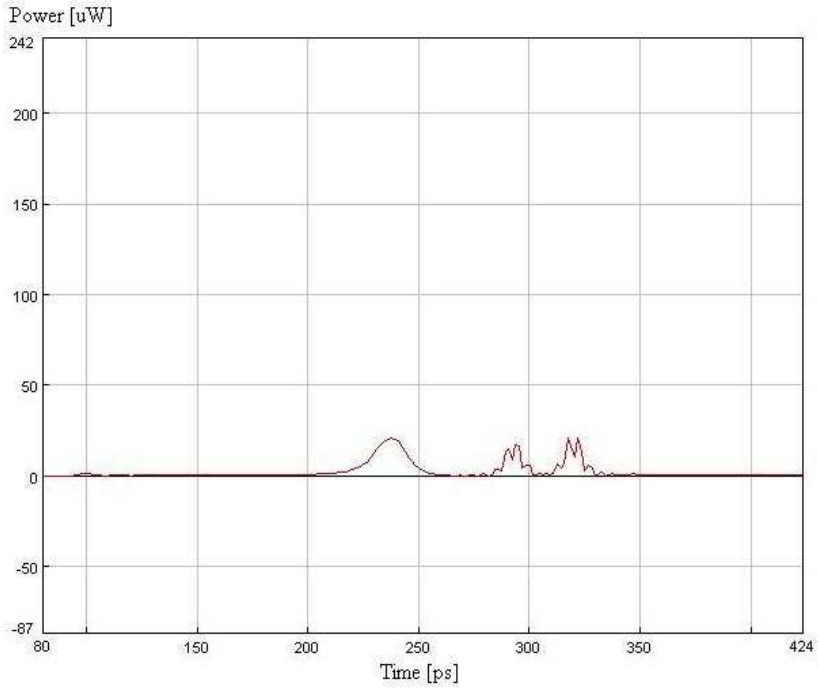

Figure 4.11

This figure shows the output power versus time at output 1

Figure 4.12 shows the output power versus time at output 2 when the header bit sequence is 001 and the payload input bit sequence is 011.

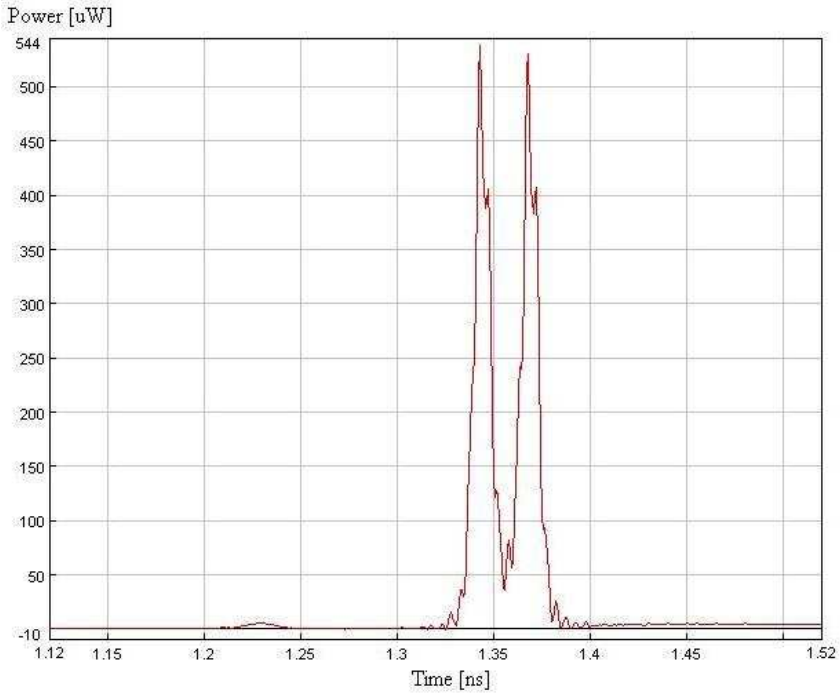

Figure 4.12

This figure shows the output power versus time at output 2.

By comparing figure 4.11 with figure 4.12 it can be seen that the payload got amplified to about 540 µW during the initial spike at output 2 and that at output 1 the payload amplification was suppressed and the payload output reached a peak at roughly 20 µW. Thus from equation 3.1 the switching ratio is

$$\alpha = \frac{20\mu W}{540\mu W}, \tag{4.10}$$

$$\therefore \alpha = 0.04, \tag{4.11}$$

$$\therefore \alpha = -14.3\text{dB}. \tag{4.12}$$

Figure 4.13 shows the payload input power versus time for a 100 payload bit sequence.

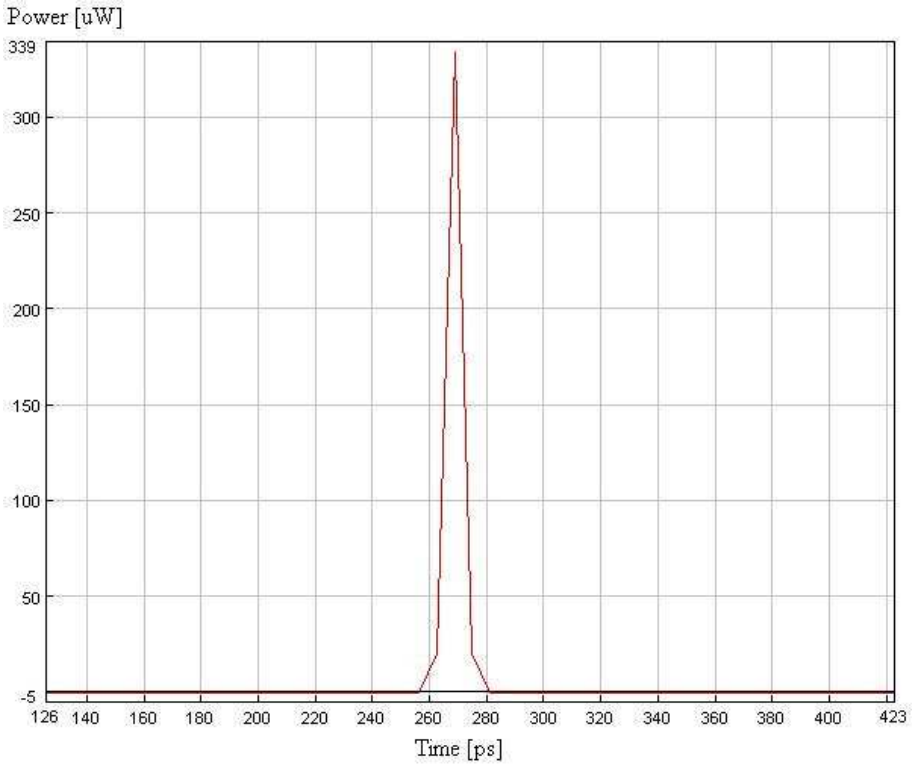

Figure 4.13

This figure shows the payload input power versus time for a 100 payload bit sequence.

Figure 4.14 shows the output power versus time at output 1 when the header bit sequence is 001 and the payload input bit sequence is 100.

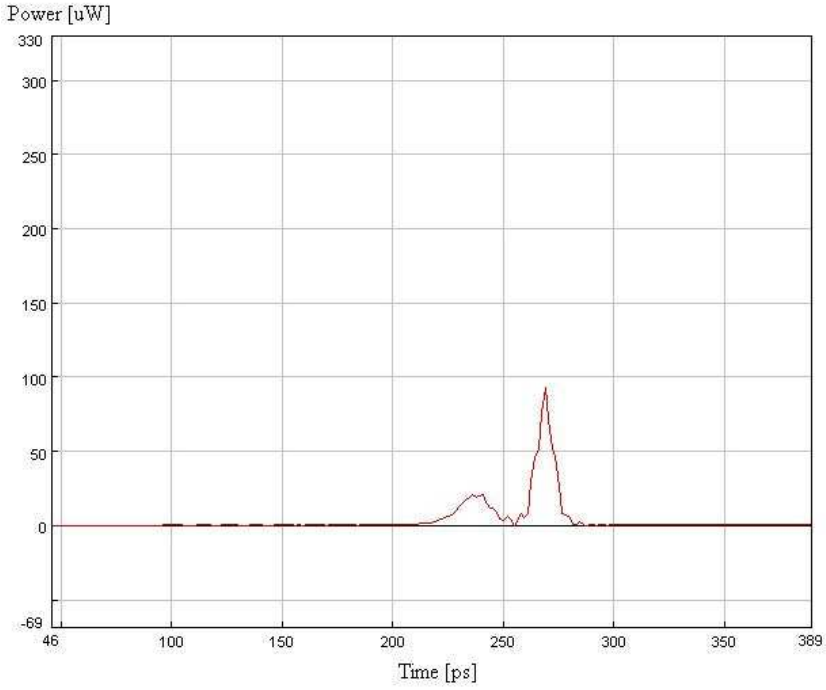

Figure 4.14

This figure shows the output power versus time at output 1.

Figure 4.15 shows the output power versus time at output 2 when the header bit sequence is 001 and the payload input bit sequence is 100.

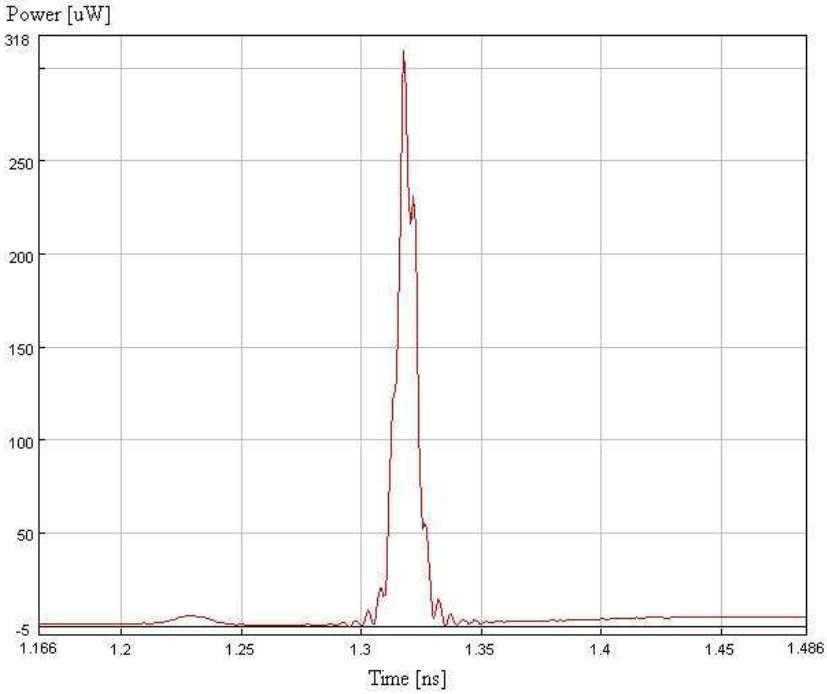

Figure 4.15

This figure shows the output power versus time at output 2.

By comparing figure 4.15 with figure 4.14 it can be seen that in the worst case scenario the payload got amplified to about 310 μW during the initial spike at output 2 and that at output 1 the payload amplification was more suppressed and the payload output reached a peak at roughly 90 μW. Thus from equation 3.1 the switching ratio is

$$\alpha = \frac{90\mu W}{310\mu W}, \tag{4.13}$$

$$\therefore \alpha = 0.29, \tag{4.14}$$

$$\therefore \alpha = -5.4\text{dB}. \tag{4.15}$$

Figure 4.16 shows the payload input power versus time for a 101 payload bit sequence.

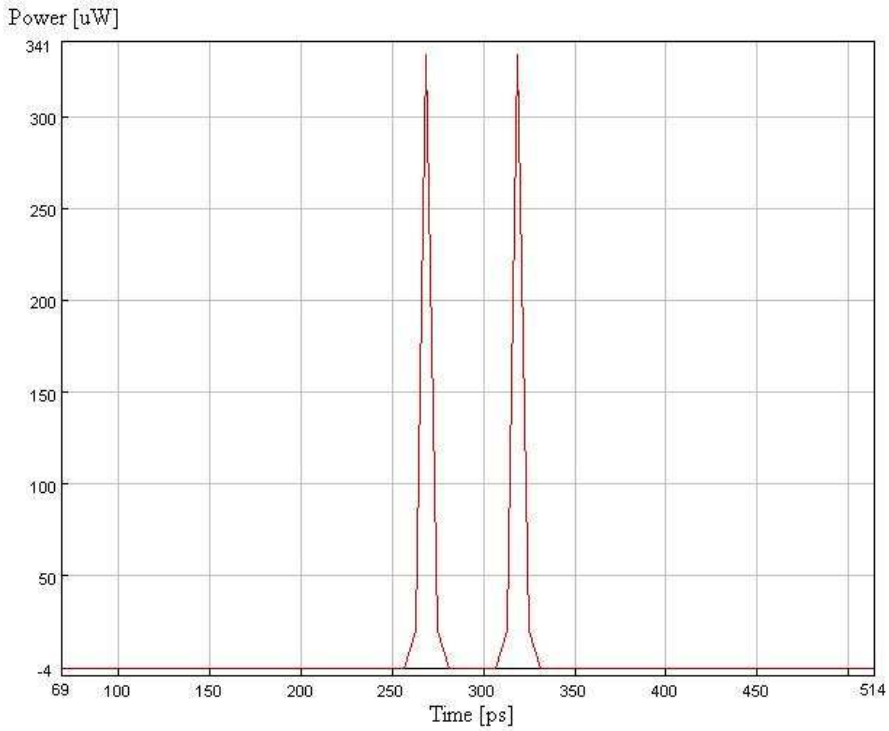

Figure 4.16

This figure shows the payload input power versus time for a 101 payload bit sequence.

Figure 4.17 shows the output power versus time at output 1 when the header bit sequence is 001 and the payload input bit sequence is 101.

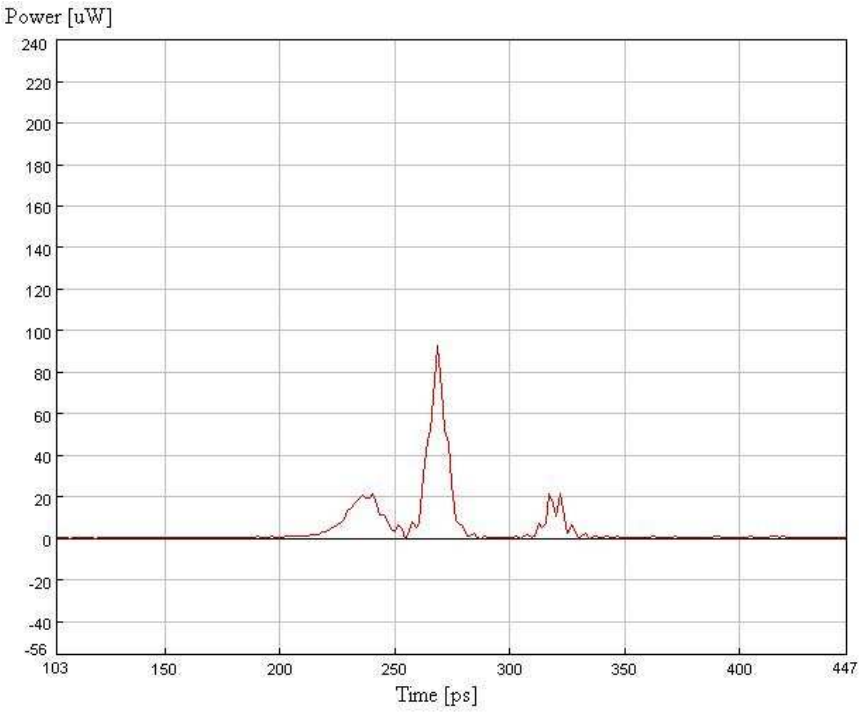

Figure 4.17

This figure shows the output power versus time at output 1

Figure 4.18 shows the output power versus time at output 2 when the header bit sequence is 001 and the payload input bit sequence is 101.

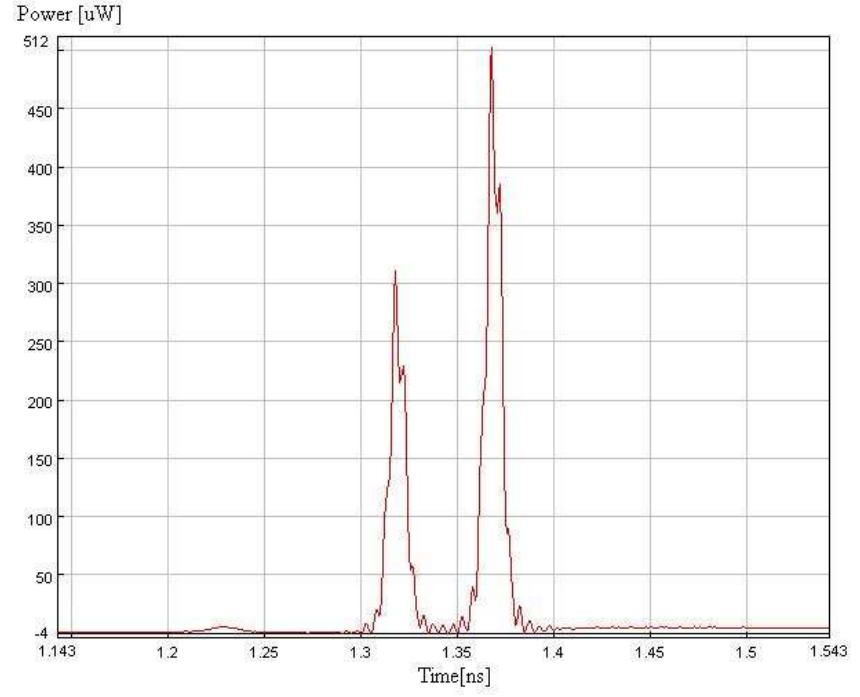

Figure 4.18

This figure shows the output power versus time at output 2.

By comparing figure 4.17 with figure 4.18 it can be seen that the first of the payload bits got amplified to about 300 μW during the initial spike at output 2 and that at output 1 the amplification of the first bit was more suppressed and the payload output reached a peak at roughly 90 μW. Thus from equation 3.1 the switching ratio for the first bit in the payload is

$$\alpha = \frac{90\mu W}{300\mu W}, \tag{4.16}$$

$$\therefore \alpha = 0.30, \tag{4.17}$$

$$\therefore \alpha = -5.2\text{dB}. \tag{4.18}$$

Figure 4.19 shows the payload input power versus time for a 110 payload bit sequence.

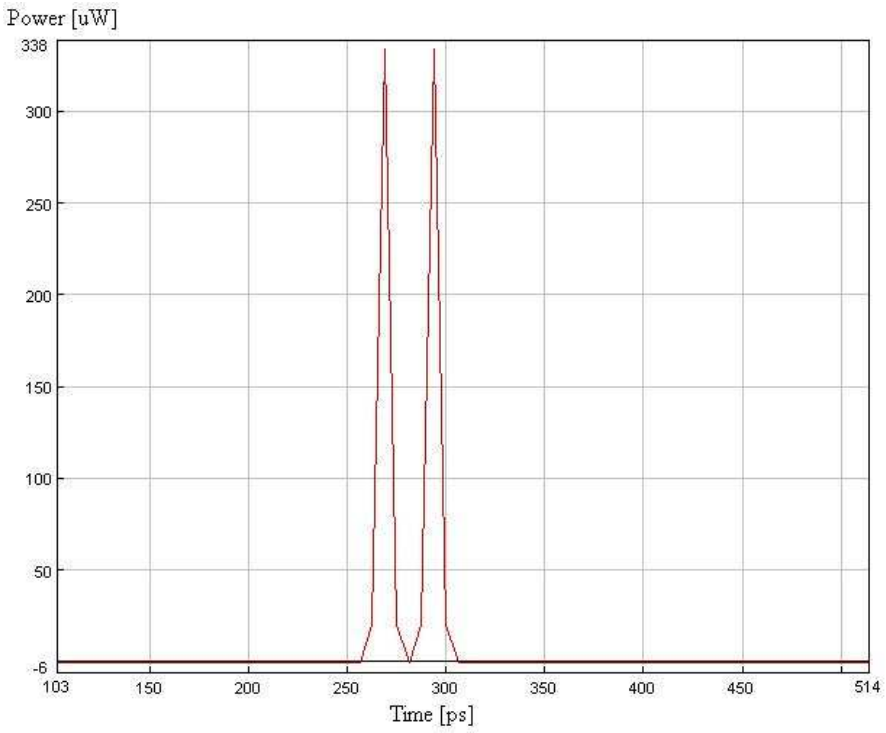

Figure 4.19

This figure shows the payload input power versus time for a 110 payload bit sequence.

Figure 4.20 shows the output power versus time at output 1 when the header bit sequence is 001 and the payload input bit sequence is 110.

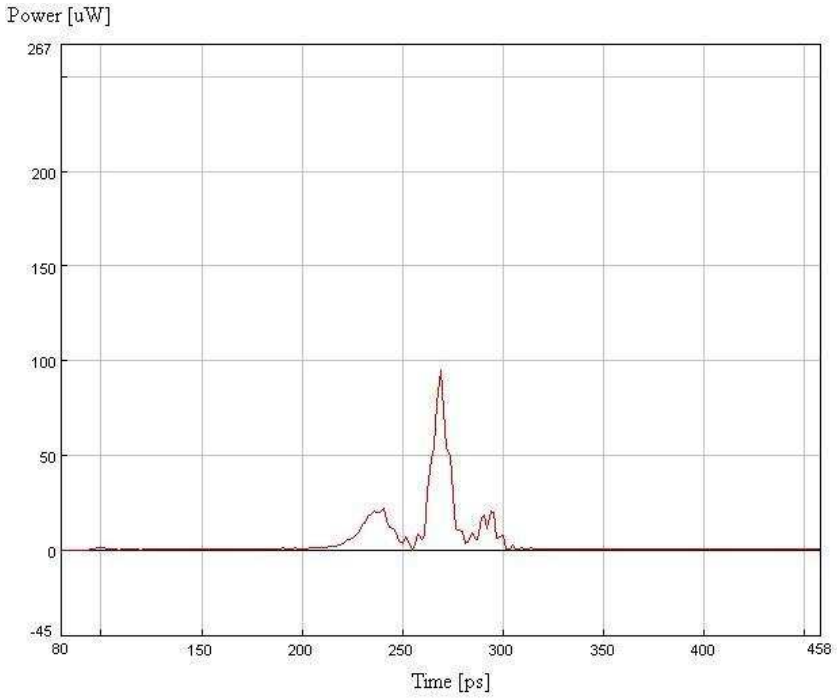

Figure 4.21

This figure shows the output power versus time at output 1.

Figure 4.22 shows the output power versus time at output 2 when the header bit sequence is 001 and the payload input bit sequence is 110.

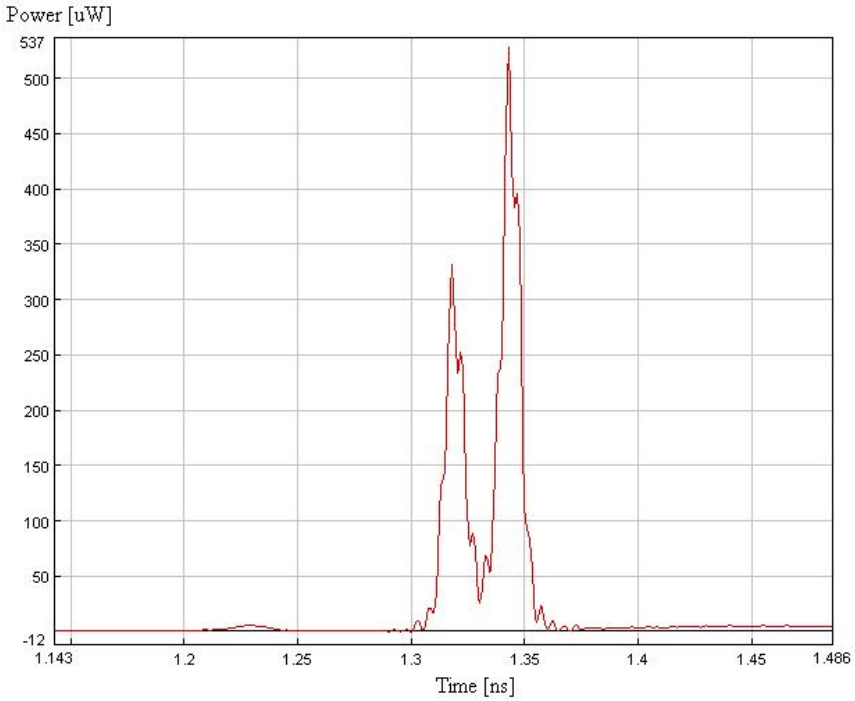

Figure 4.22

This figure shows the output power versus time at output 2.

By comparing figure 4.21 with figure 4.22 it can be seen that in the worst case scenario the payload got amplified to 330 µW at output 2 and that at output 1 the payload amplification was more suppressed and the payload output reached a peak at roughly 95 µW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{90\mu W}{330\mu W}, \tag{4.19}$$

$$\therefore \alpha = 0.27, \tag{4.20}$$

$$\therefore \alpha = -5.6\text{dB}. \tag{4.21}$$

Figure 4.23 shows the payload input power versus time for a 111 payload bit sequence.

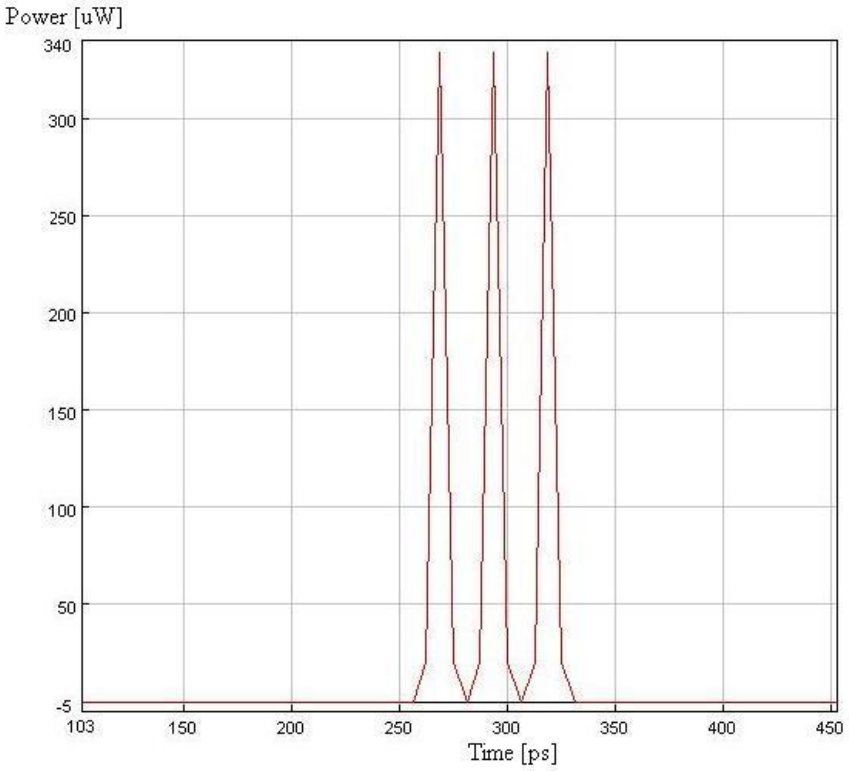

Figure 4.23

This figure shows the payload input power versus time for a 111 payload bit sequence.

Figure 4.24 shows the output power versus time at output 1 when the header bit sequence is 001 and the payload input bit sequence is 111.

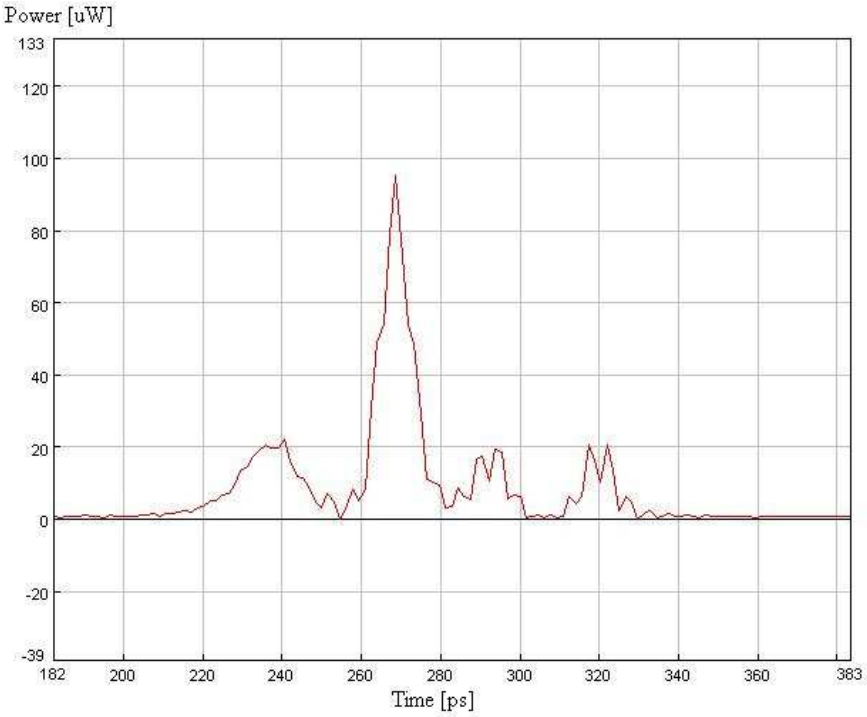

Figure 4.24

This figure shows the output power versus time at output 1.

Figure 4.25 shows the output power versus time at output 2 when the header bit sequence is 001 and the payload input bit sequence is 111.

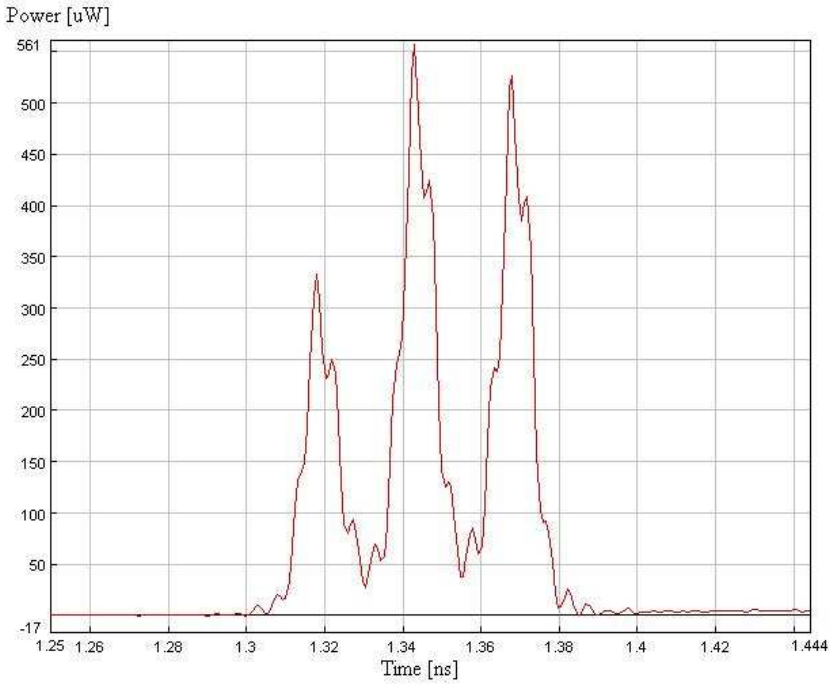

Figure 4.25

This figure shows the output power versus time at output 2.

By comparing figure 4.24 with figure 4.25 it can be seen that in the worst case scenario the payload got amplified to 330 μW at output 2 and that at output 1 the payload amplification was more suppressed and the payload output reached a peak at roughly 95 μW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{95\mu W}{330\mu W}, \tag{4.22}$$

$$\therefore \alpha = 0.29, \tag{4.23}$$

$$\therefore \alpha = -5.4\text{dB}. \tag{4.24}$$

1.3 Simulated experiment C

In this experiment the header packet is a 010 bit sequence. Figure 4.26 shows the output power versus time at output 1 when the header is a 010 bit sequence and the payload input is a 111 bit sequence (as shown in figure 4.1).

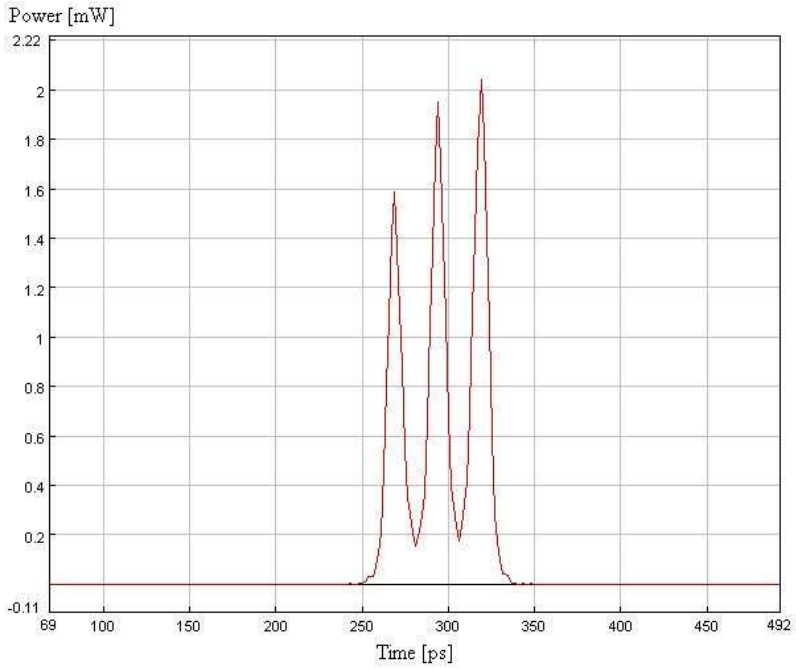

Figure 4.26

This figure shows the output power versus time at output 1.

Figure 4.27 shows the output power versus time at output 2 when the header is a 010 bit sequence and the payload input is a 111 bit sequence.

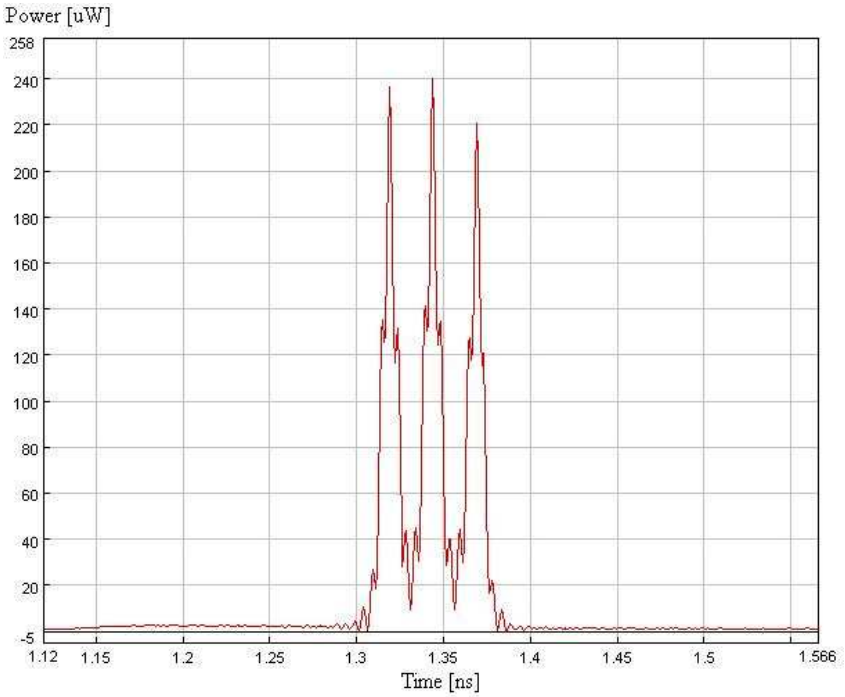

Figure 4.27

This figure shows the output power versus time at output 2.

By comparing figure 4.27 with figure 4.26 it can be seen that in the worst case scenario the payload got amplified to 1.6 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 240 µW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{1.6mW}{240\mu W}, \tag{4.25}$$

$$\therefore \alpha = 6.7, \tag{4.26}$$

$$\therefore \alpha = 8.2\text{dB}. \tag{4.27}$$

1.4 Simulated experiment D

In this experiment the header packet is a 011 bit sequence. Figure 4.28 shows the output power versus time at output 1 when the header is a 011 bit sequence and the payload input is a 111 bit sequence (as shown in figure 4.1).

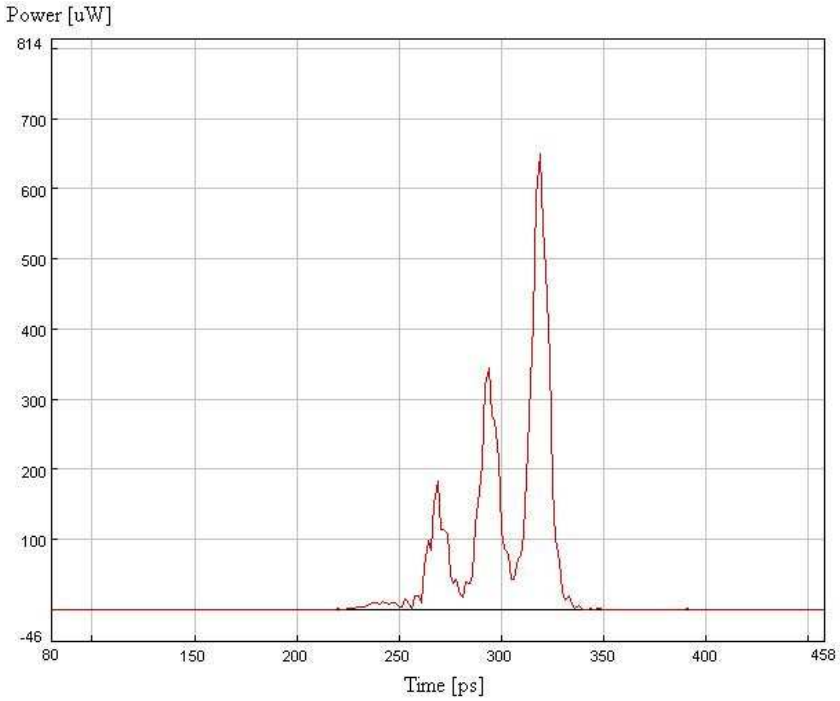

Figure 4.28

This figure shows the output power versus time at output 1.

Figure 4.29 shows the output power versus time at output 2 when the header is a 011 bit sequence and the payload input is a 111 bit sequence.

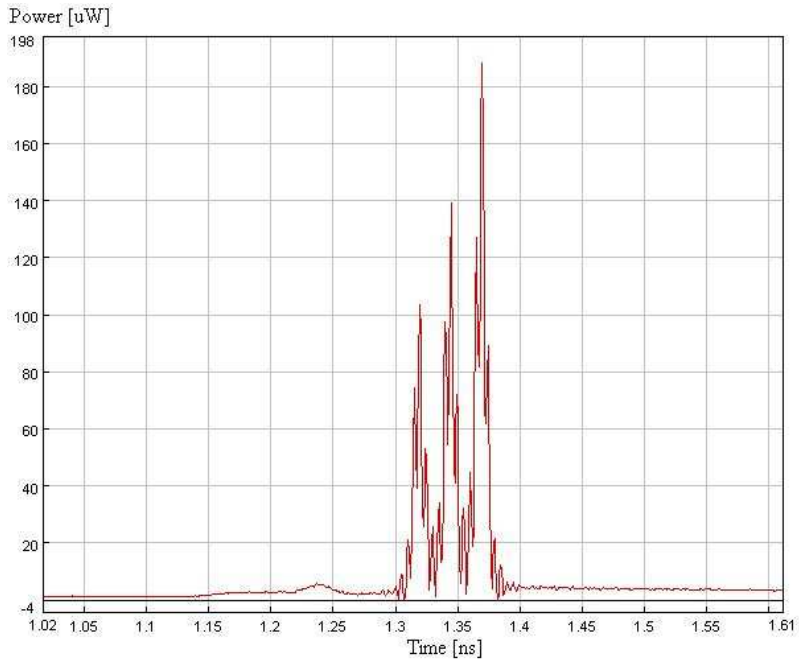

Figure 4.29

This figure shows the output power versus time at output 2.

By comparing figure 4.29 with figure 4.28 it can be seen that in the worst case scenario the payload got amplified to around 190 μW at output 1 and that at output 2 the payload amplification output reached a peak at roughly 190 μW as well. It must be noted here that the distortion is substantial at output 2 as can be seen in figure 4.29. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{190\mu W}{190\mu W}, \tag{4.28}$$

$$\therefore \alpha = 1, \tag{4.29}$$

$$\therefore \alpha = 0\text{dB}. \tag{4.30}$$

1.5 Simulated experiment E

In this experiment the header packet is a 100 bit sequence. Figure 4.30 shows the output power versus time at output 1 when the header is a 100 bit sequence and the payload input is a 111 bit sequence (as shown in figure 4.1).

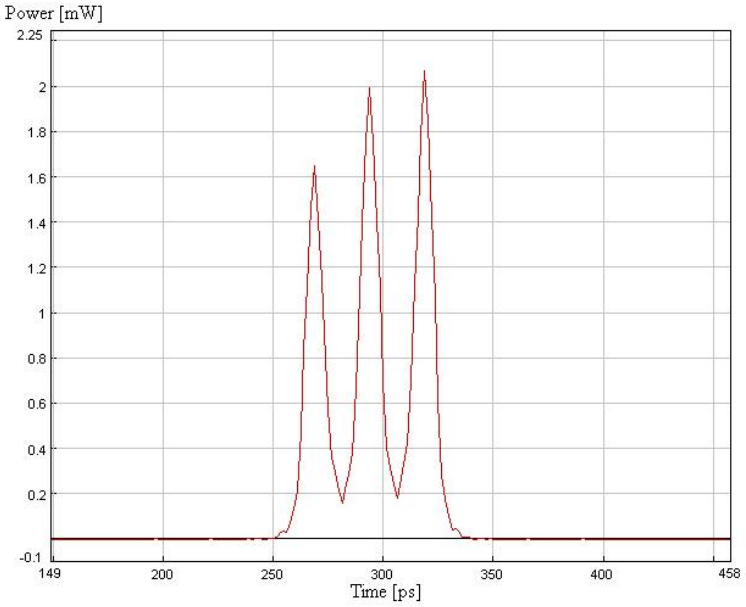

Figure 4.30

This figure shows the output power versus time at output 1.

Figure 4.31 shows the output power versus time at output 2 when the header is a 100 bit sequence and the payload input is a 111 bit sequence.

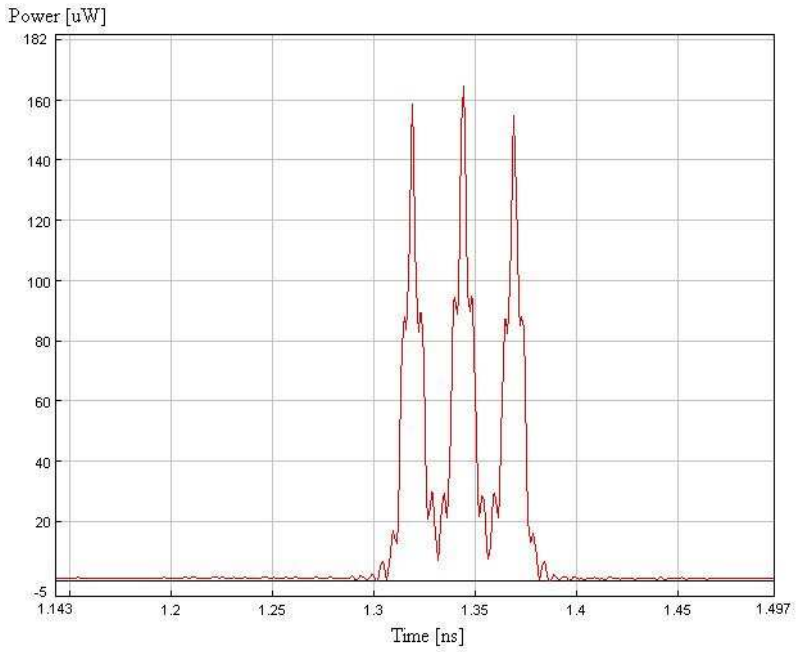

Figure 4.31

This figure shows the output power versus time at output 2.

By comparing figure 4.30 with figure 4.31 it can be seen that in the worst case scenario the payload got amplified to at least 1.6 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 160 μW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{1.6mW}{160\mu W}, \tag{4.31}$$

$$\therefore \alpha = 10, \tag{4.32}$$

$$\therefore \alpha = 10\text{dB}. \tag{4.33}$$

1.6 Simulated experiment F

In this experiment the header packet is a 101 bit sequence. Figure 4.32 shows the output power versus time at output 1 when the header is a 101 bit sequence and the payload input is a 001 bit sequence.

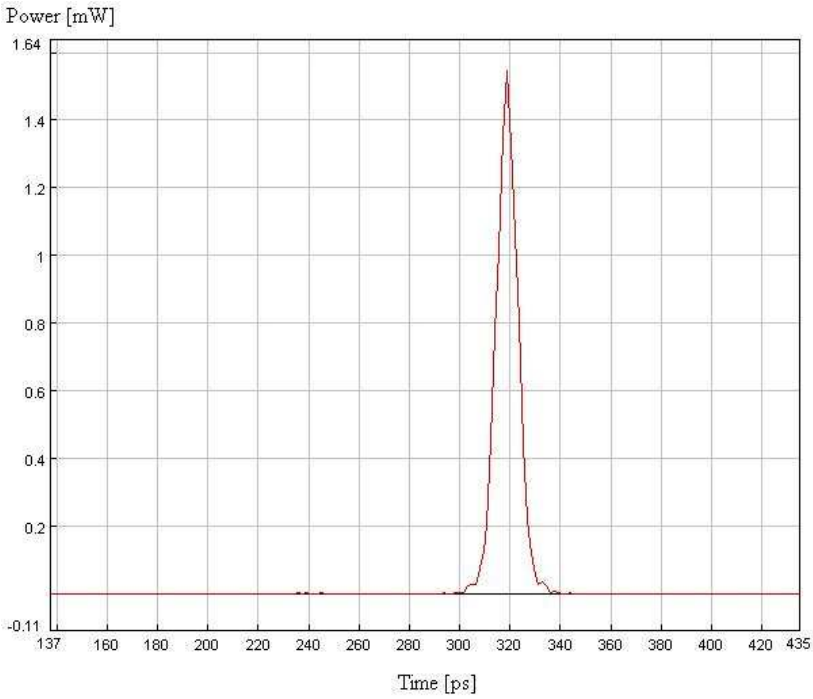

Figure 4.32

This figure shows the output power versus time at output 1.

Figure 4.33 shows the output power versus time at output 2 when the header is a 101 bit sequence and the payload input is a 001 bit sequence.

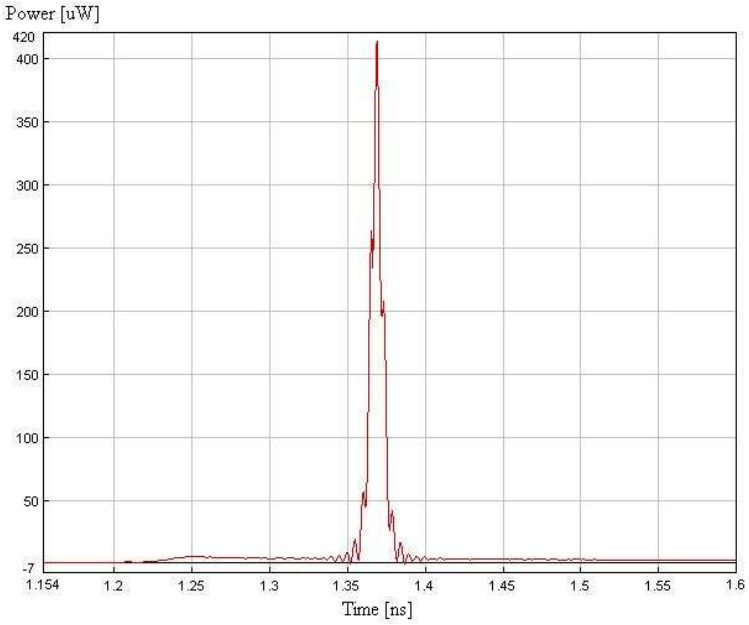

Figure 4.33

This figure shows the output power versus time at output 2.

By comparing figure 4.32 with figure 4.33 it can be seen that in the worst case scenario the payload got amplified to at least 1.55 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 410 µW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{1.55mW}{410\mu W}, \tag{4.34}$$

$$\therefore \alpha = 3.8, \tag{4.35}$$

$$\therefore \alpha = 5.8\text{dB}. \tag{4.36}$$

Figure 4.34 shows the output power versus time at output 1 when the header is a 101 bit sequence and the payload input is a 010 bit sequence.

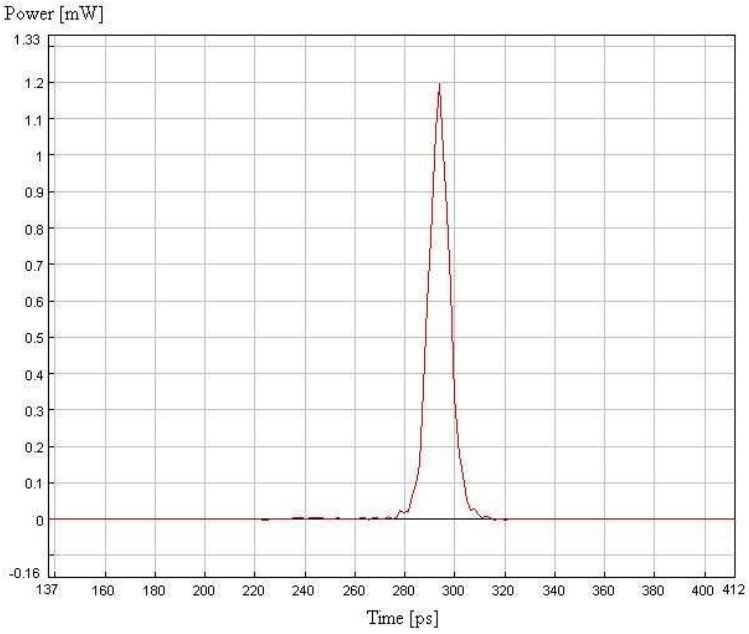

Figure 4.34

This figure shows the output power versus time at output 1.

Figure 4.35 shows the output power versus time at output 2 when the header is a 101 bit sequence and the payload input is a 010 bit sequence.

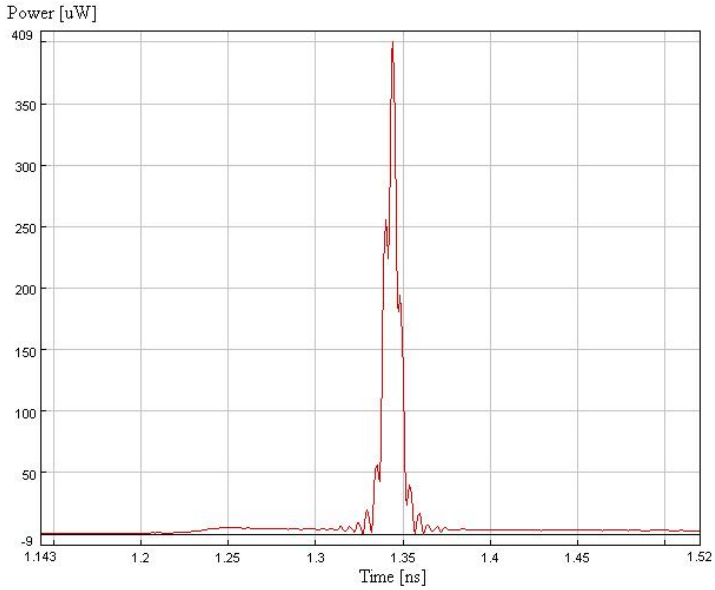

Figure 4.35

This figure shows the output power versus time at output 2.

By comparing figure 4.34 with figure 4.35 it can be seen that in the worst case scenario the payload got amplified to at least 1.2 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 400 μW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{1.2mW}{400\mu W}, \tag{4.37}$$

$$\therefore \alpha = 3, \tag{4.38}$$

$$\therefore \alpha = 4.8\text{dB}. \tag{4.39}$$

Figure 4.36 shows the output power versus time at output 1 when the header is a 101 bit sequence and the payload input is a 011 bit sequence.

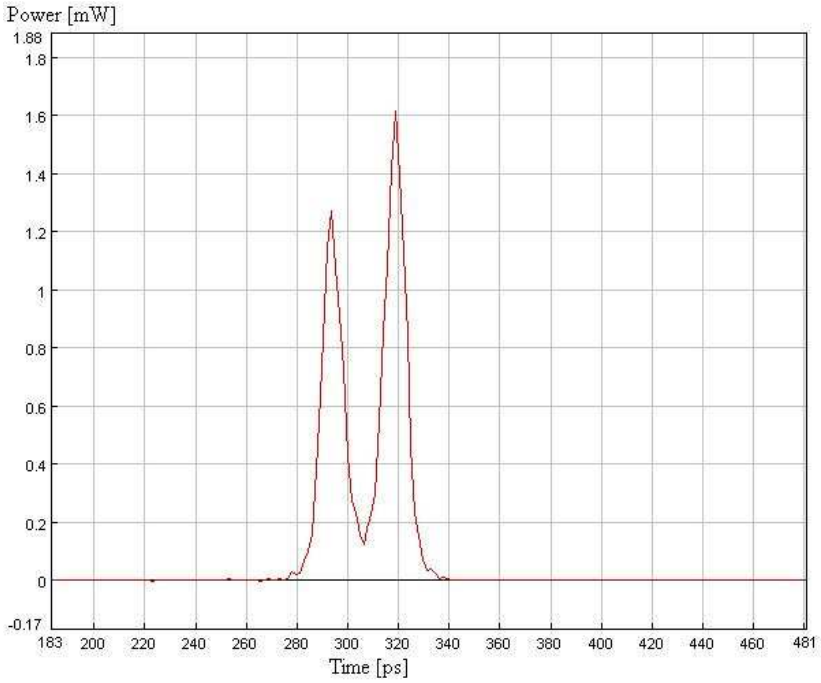

Figure 4.36

This figure shows the output power versus time at output 1.

Figure 4.37 shows the output power versus time at output 2 when the header is a 101 bit sequence and the payload input is a 011 bit sequence.

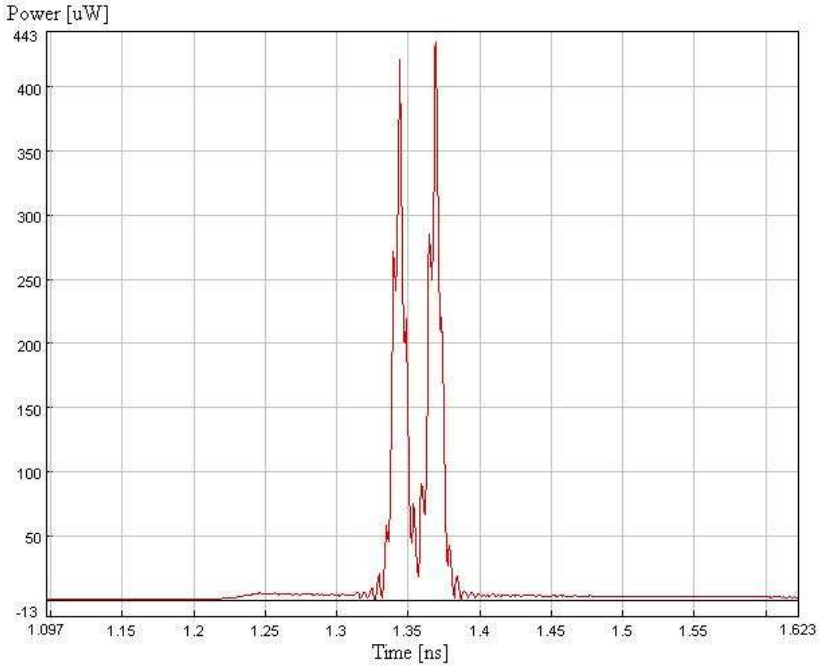

Figure 4.37

This figure shows the output power versus time at output 2.

By comparing figure 4.37 with figure 4.36 it can be seen that in the worst case scenario the payload got amplified to at least 1.25 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 440 µW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{1.25mW}{440\mu W}, \tag{4.40}$$

$$\therefore \alpha = 2.8, \tag{4.41}$$

$$\therefore \alpha = 4.5\text{dB}. \tag{4.42}$$

Figure 4.38 shows the output power versus time at output 1 when the header is a 101 bit sequence and the payload input is a 100 bit sequence.

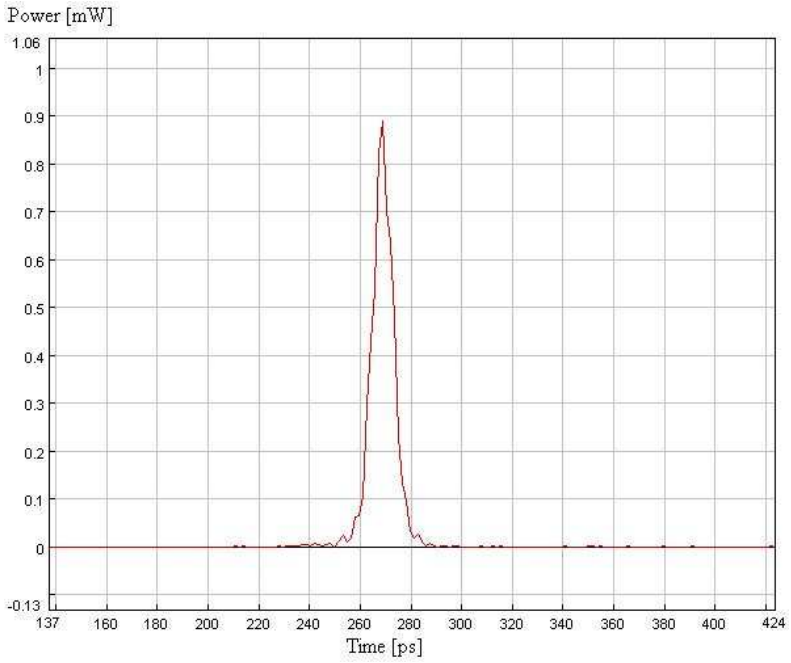

Figure 4.38

This figure shows the output power versus time at output 1.

Figure 4.39 shows the output power versus time at output 2 when the header is a 101 bit sequence and the payload input is a 100 bit sequence.

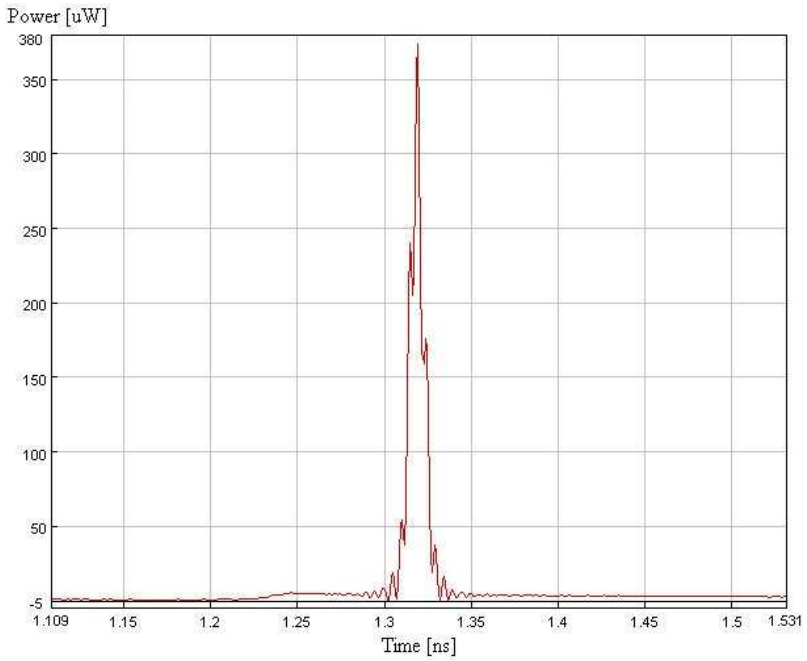

Figure 4.39

This figure shows the output power versus time at output 2.

By comparing figure 4.39 with figure 4.38 it can be seen that in the worst case scenario the payload got amplified to at least 0.9 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 375 μW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{0.9mW}{375\mu W}, \tag{4.43}$$

$$\therefore \alpha = 2.4, \tag{4.44}$$

$$\therefore \alpha = 3.8\text{dB}. \tag{4.45}$$

Figure 4.40 shows the output power versus time at output 1 when the header is a 101 bit sequence and the payload input is a 101 bit sequence.

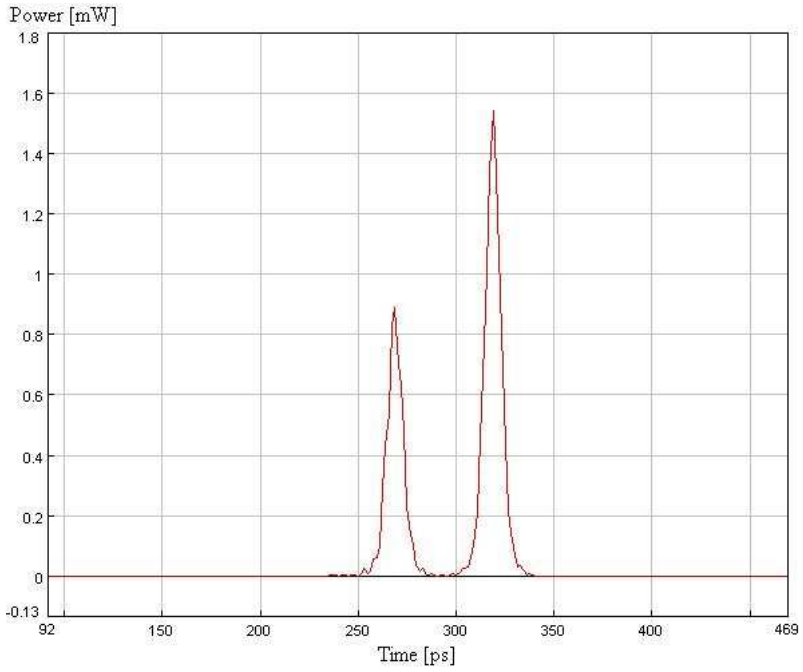

Figure 4.40

This figure shows the output power versus time at output 1.

Figure 4.41 shows the output power versus time at output 2 when the header is a 101 bit sequence and the payload input is a 101 bit sequence.

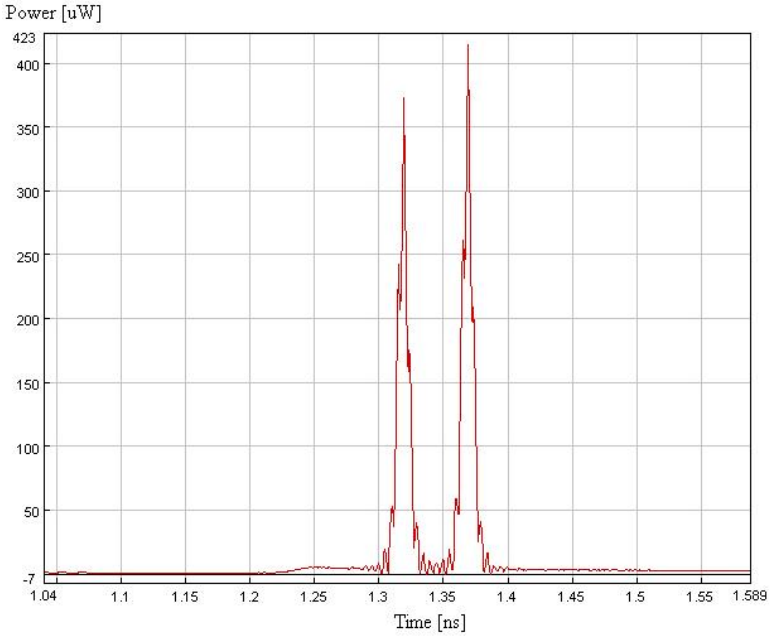

Figure 4.41

This figure shows the output power versus time at output 2.

By comparing figure 4.41 with figure 4.40 it can be seen that in the worst case scenario the payload got amplified to at least 0.9 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 420 µW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{0.9mW}{420\mu W}, \tag{4.46}$$

$$\therefore \alpha = 2.1, \tag{4.47}$$

$$\therefore \alpha = 3.3\text{dB}. \tag{4.48}$$

Figure 4.42 shows the output power versus time at output 1 when the header is a 101 bit sequence and the payload input is a 110 bit sequence.

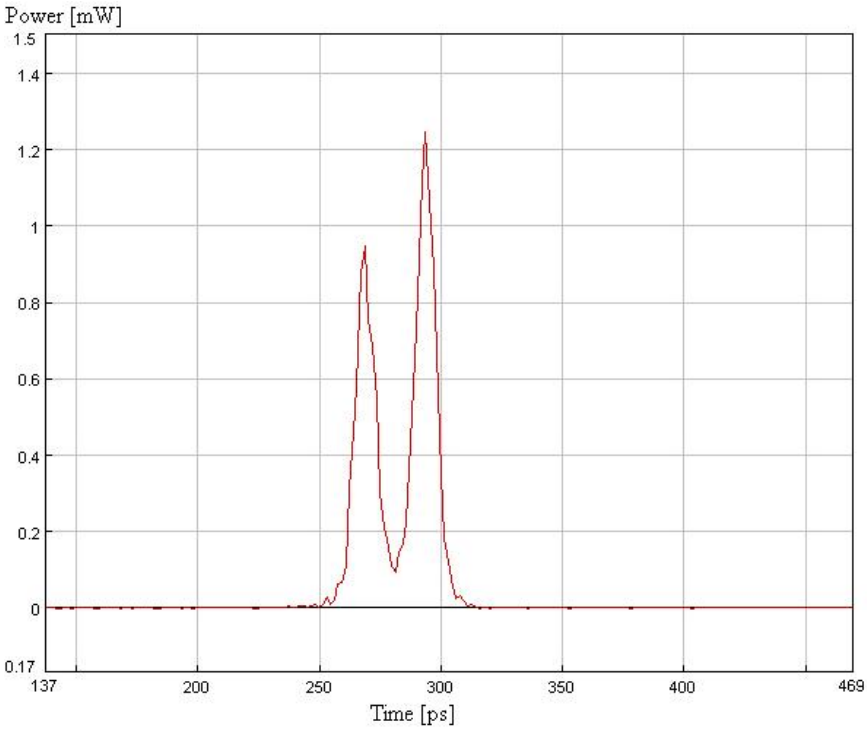

Figure 4.42

This figure shows the output power versus time at output 1.

Figure 4.43 shows the output power versus time at output 2 when the header is a 101 bit sequence and the payload input is a 110 bit sequence.

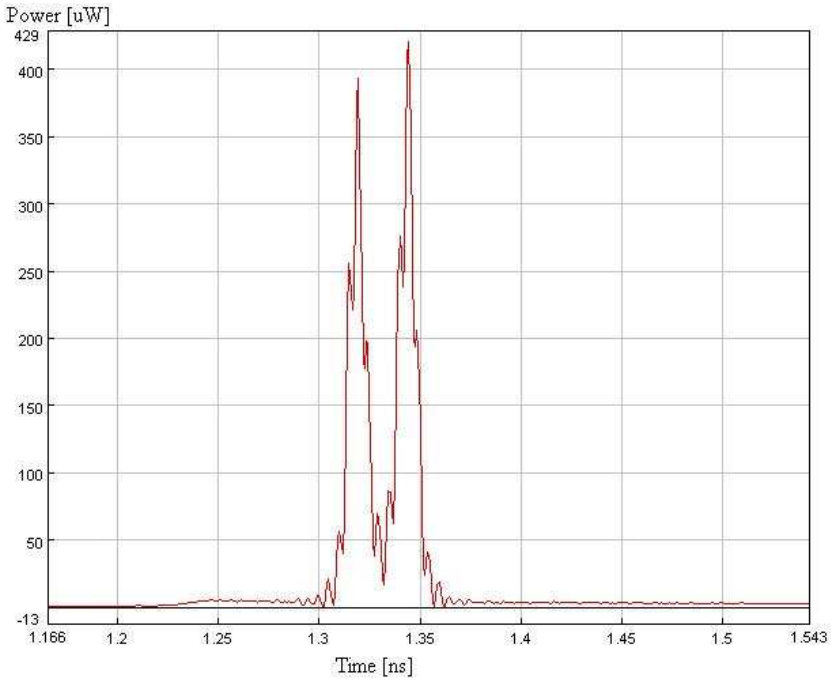

Figure 4.43

This figure shows the output power versus time at output 2.

By comparing figure 4.43 with figure 4.42 it can be seen that in the worst case scenario the payload got amplified to at least 0.95 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 420 μW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{0.95mW}{420\mu W}, \tag{4.49}$$

$$\therefore \alpha = 2.3, \tag{4.50}$$

$$\therefore \alpha = 3.5\text{dB}. \tag{4.51}$$

Figure 4.44 shows the output power versus time at output 1 when the header is a 101 bit sequence and the payload input is a 111 bit sequence.

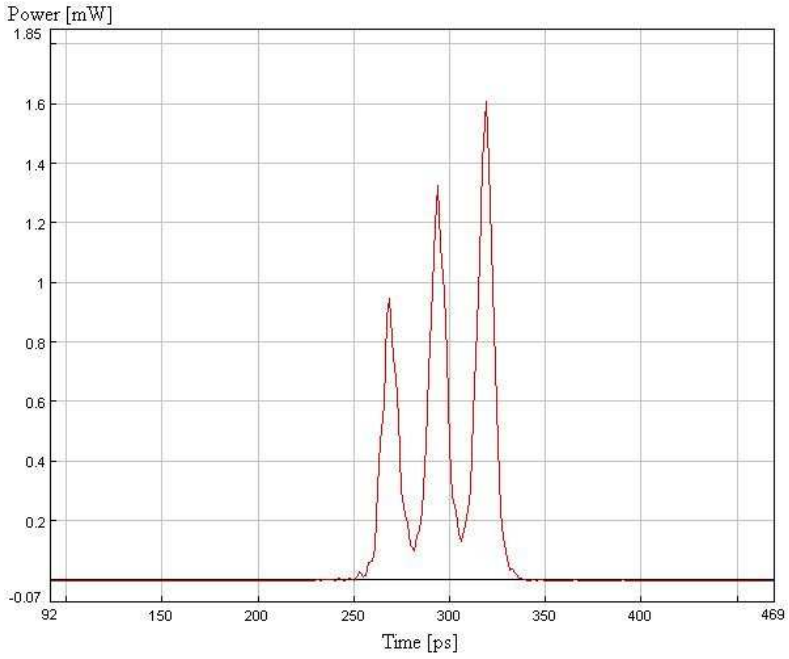

Figure 4.44

This figure shows the output power versus time at output 1.

Figure 4.45 shows the output power versus time at output 2 when the header is a 101 bit sequence and the payload input is a 111 bit sequence.

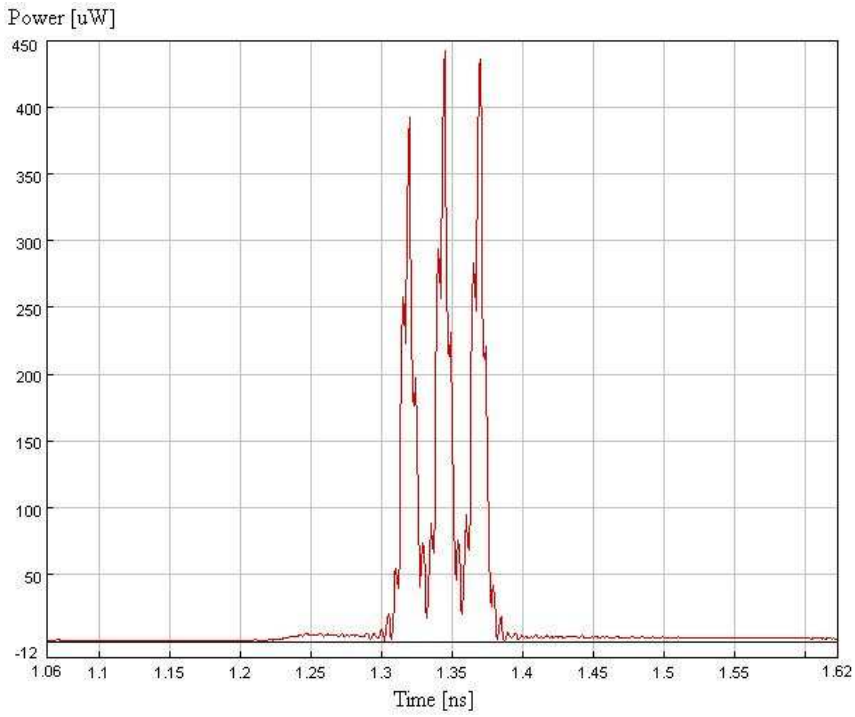

Figure 4.45

This figure shows the output power versus time at output 2.

By comparing figure 4.45 with figure 4.44 it can be seen that in the worst case scenario the payload got amplified to at least 0.95 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 445 μW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{0.95mW}{445\mu W}, \tag{4.52}$$

$$\therefore \alpha = 2.1, \tag{4.53}$$

$$\therefore \alpha = 3.3\text{dB}. \tag{4.54}$$

1.7 Simulated experiment G

In this experiment the header packet is a 110 bit sequence. Figure 4.46 shows the output power versus time at output 1 when the header is a 110 bit sequence and the payload input is a 111 bit sequence.

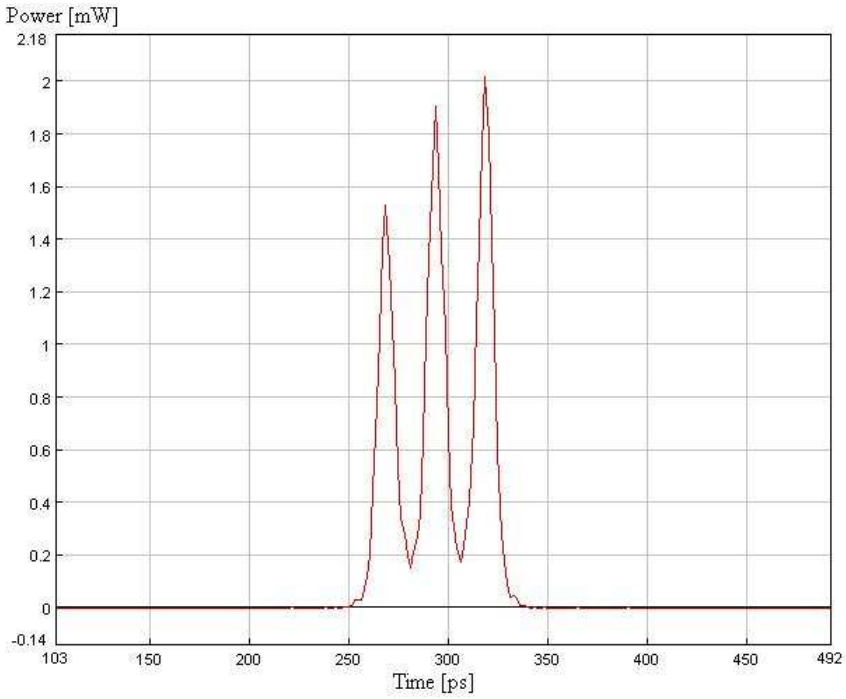

Figure 4.46

This figure shows the output power versus time at output 1.

Figure 4.47 shows the output power versus time at output 2 when the header is a 110 bit sequence and the payload input is a 111 bit sequence.

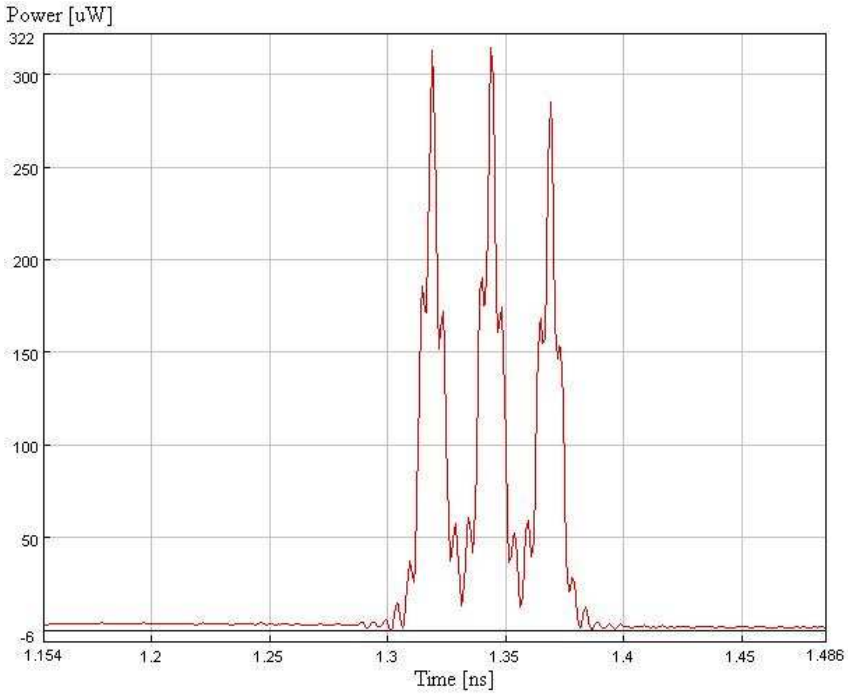

Figure 4.47

This figure shows the output power versus time at output 2.

By comparing figure 4.47 with figure 4.46 it can be seen that in the worst case scenario the payload got amplified to at least 1.5 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 320 μW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{1.5mW}{320\mu W}, \tag{4.55}$$

$$\therefore \alpha = 4.7, \tag{4.56}$$

$$\therefore \alpha = 6.7\text{dB}. \tag{4.57}$$

1.8 Simulated experiment H

In this experiment the header packet is a 111 bit sequence. Figure 4.48 shows the output power versus time at output 1 when the header is a 111 bit sequence and the payload input is a 111 bit sequence.

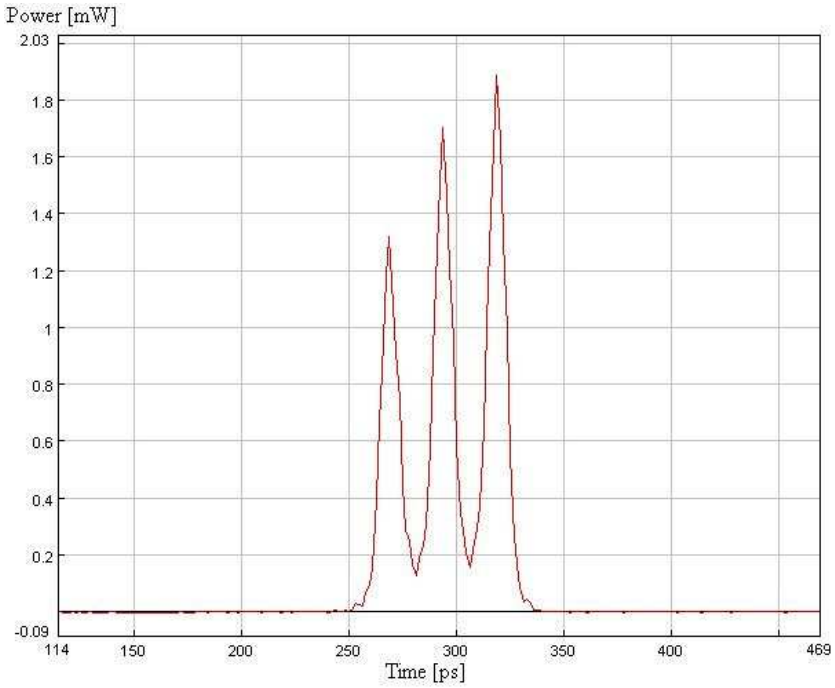

Figure 4.48

This figure shows the output power versus time at output 1.

Figure 4.49 shows the output power versus time at output 2 when the header is a 111 bit sequence and the payload input is a 111 bit sequence.

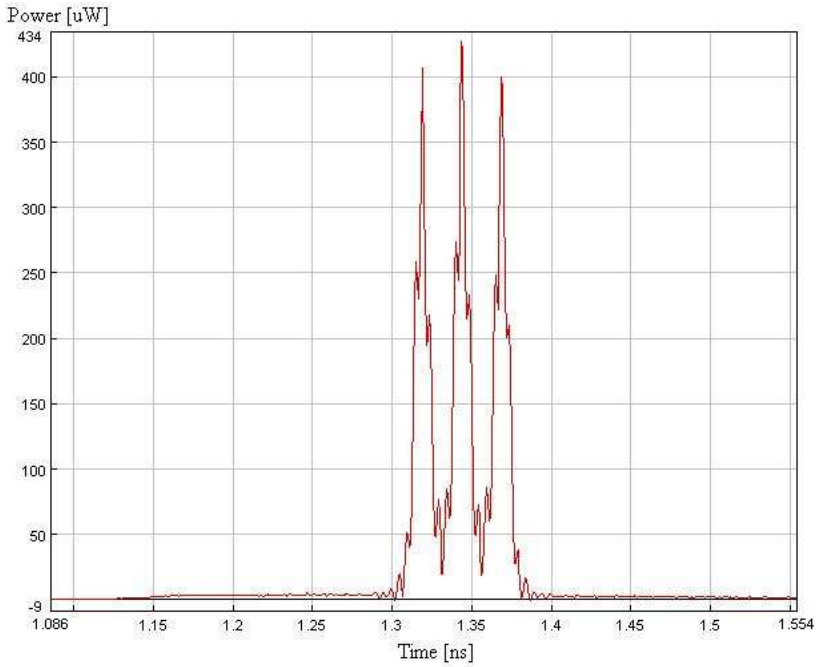

Figure 4.49

This figure shows the output power versus time at output 2.

By comparing figure 4.49 with figure 4.48 it can be seen that in the worst case scenario the payload got amplified to at least 1.3 mW at output 1 and that at output 2 the payload amplification was more suppressed and the payload output reached a peak at roughly 430 mW. Thus from equation 3.1 the worst case switching ratio is

$$\alpha = \frac{1.3mW}{430\mu W}, \tag{4.58}$$

$$\therefore \alpha = 3.0, \tag{4.59}$$

$$\therefore \alpha = 4.8\text{dB}. \tag{4.60}$$

Chapter 5

DISCUSSION AND CONCLUSION

A unique all-optical self routing switch is introduced. The objective of all-optical packet routing by way of all-optical header processing of the optical bits in an all-optical header packet (the destination address) was achieved. It was illustrated by successfully simulating a three bit parallel processing all-optical switching node. The header and payload packets were transmitted separately in the system, and the header bits were processed in parallel thus increasing the switching speed as well as reducing the amount of buffering required for the payload. A 1x2 switching operation is analysed and a switching ratio of up to 14dB is obtained.

The research resulted in an optical routing processing technique which took an optical bit sequence and delivered a single output result which was then used to switch an optical packet payload. The switching node had two optical fibre inputs and two optical fibre outputs. The one input fibre carried the header packet, which contained the destination address for the payload packet, and the other input fibre carried the payload packet, which contained the data. The aim was to switch the payload packet to one of the two output fibres depending on the bit sequence within the header packet. Also only one unique address (header bit sequence) caused the payload packet to exit via one of the outputs and all the other possible addresses caused the payload packet to exit via the other output. Figure 5.1 below functionally illustrates the results that were achieved in the simulated experiments. To prove the concept only three bits were used in the header packet and three bits in the payload packet, but in theory more bits can be used in the payload packet at a decreased bit length to increase throughput. More bits can also be used in the header packet to increase the number of addresses that can be reached. Refer to Appendix B for the design detail of a theoretical four bit all-optical packet-switch.

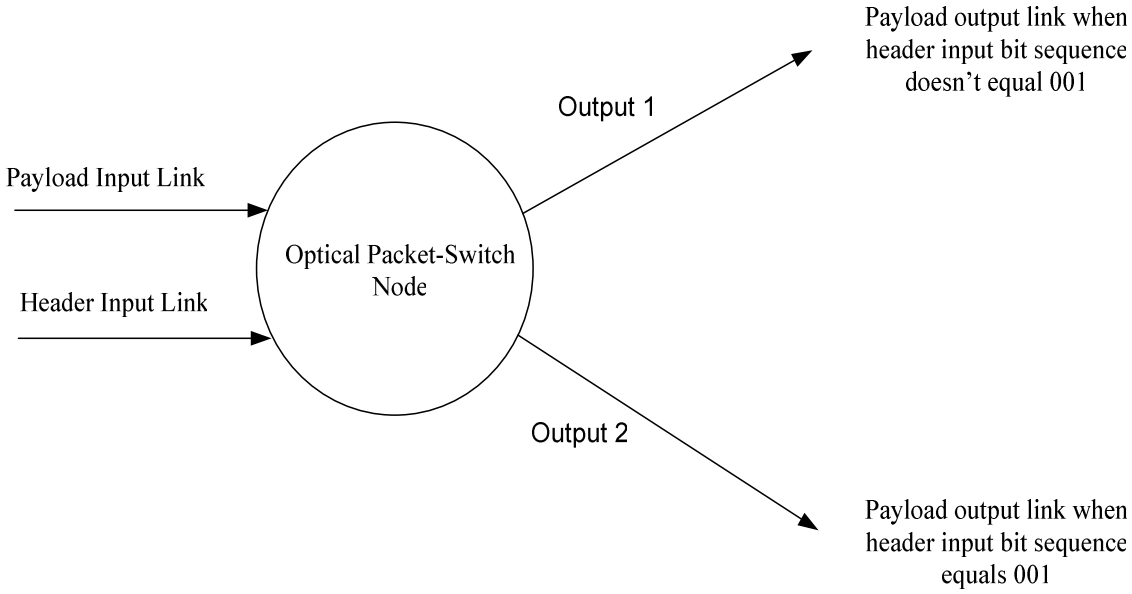

Figure 5.1

Functional illustration of the results achieved in the simulated experiments.

The physical configuration of the all-optical switches in the parallel processing structure of the switching node determined for which unique address the payload packet would exit via a different output than when the address was any of the other possible combinations of sequences.

It was found that the payload packet would under all circumstances exit both outputs, but that at one output it would be much larger than at the other output (where it was normally found to be suppressed when compared to the original payload packet input optical power). This difference in optical powers at the two output fibres was referred to as the switching ratio and was used to determine the success of the switching node for the different header sequences and payload sequences. In this investigation the switching ratio was calculated based on the maximum values of the gaussian pulses, but the Full Width Half Maximum (FWHM) values could also have been used to calculate the switching ratios.

The VPItransmissionMaker^{TM} simulation package had difficulty in simulating the Kerr-effect switch. This was because the package was unable to work with the values of nonlinear index coefficient (refer to equation 1.1) necessary to do optical switching with. It

was therefore not simulated in this research proposal. The results obtained in the simulated experiments are summarized in table 5.1 below.

Table 5.1

This table shows all the combinations of header input bit sequence and payload input bit sequence that was simulated and their respective worst case switching ratios. A 1 indicates a relatively large optical power and a 0 indicates an insignificantly small optical power. N.A. indicates Not Applicable

Experiment character	Header input sequence (at 10 Gbps)	Payload input sequence (at 40 Gbps)	Worst case switching ratio (dB)
A	000	111	10
B	001	000	N.A.
B	001	001	-14.1
B	001	010	-10.7
B	001	011	-14.3
B	001	100	-5.4
B	001	101	-5.2
B	001	110	-5.6
B	001	111	-5.4
C	010	111	10
D	011	111	0
E	100	111	10
F	101	000	N.A
F	101	001	5.8
F	101	010	4.8
F	101	011	4.5
F	101	100	3.8
F	101	101	3.3
F	101	110	3.5
F	101	111	3.3
G	110	111	6.7
H	111	111	4.8

Although the worst case switching ratio is 0 dB in simulated experiment D (011 header and 111 payload) this switching ratio can be avoided by not utilizing the 011 header bit sequence , thus restricting the number of potential addresses to 7 instead of 8, or by increasing the width of the header bits, thus increasing the available switching window and decreasing the effect of any transients produced by the parallel processing on the first of the three payload bits. Another method to avoid the 0 dB switching ratio in experiment D is by inserting a slight delay in front of the data input of the first output's XGM switch (refer

to figure 2.1), thus also limiting the effect of any transients on the first of the payload bits. This conclusion is made because by comparing figures 4.28 and 4.29 it can be seen that the worst case switching ratio is obtained by comparing the first bit in output 1 with the last bit of output 2 via equation 3.1, but that the last bit in output 1 is roughly 460 μW higher than the concurrent first bit of the same output and, compared to output 2 where the last bit is only about 90 μW higher than the first bit, the conclusion can be made that the switching window is more effective during the second and third bits of output 1 than during the first and that thus a slight delay in output 1's XGM payload input would have the same positive effect on the switching ratio as increasing the switching window by increasing the header bit widths (thus decreasing the header bit rate).

In table 5.1 it can be seen that only when the header input sequence was equal to 001 was the switching ratio negative. This means that the payload packet only exited via output 2 when the header bit sequence was equal to 001. For all other values of the header bit sequence the switching ratio was positive and the payload packet thus exited via output 1.

The SOA used in the simulated experiments is a very important component when trying to determine the maximum switching speed. The SOA's recovery rate will determine how long after one packet was processed can the next packet be processed. This is because as long as the SOA's free carriers are being replenished it cannot process another header package. The SOA's recovery rate can be brought down by pumping a CW optical signal into the SOA. This CW signal should however not have such large optical powers that it saturates the SOA.

The throughput can be increased by decreasing the payload packet bit length (i.e. increasing its bit-rate), inserting more payload packet bits or decreasing the bit-rate of the payload packet (i.e. increasing its bit length). Additionally more payload bits can be added if the header bit-rate is slower (i.e. header bits are longer). This is as a result of the length of the switch window (the window where the individual output XGMs are prepared to correctly process the payload bits) being determined by the length of the parallel processing output because the parallel processing output in turn feeds the control inputs of both of the output XGMs and the parallel processing output is equal in length to the length of the header bits.

The type of architecture that was investigated here for an optical packet-switch has the potential to be scalable, meaning that the architecture could in principle be modified to process a larger number of header bits, and as such it will be able to send packets to a larger number of destinations. Thus this type of architecture could theoretically be used to switch packets in large optical networks with a multitude of destinations, but additional Signal to Noise Ratio measurements will have to be made in order to verify the actual scalability of this type of architecture.

In the structure designed in this investigation the 001 header sequence resulted in the payload packet exiting at a different output than all of the other possible header sequences, this header bit sequence (001) will be referred to as the switch sequence. By changing the structure of the parallel processing architecture a different header sequence can fulfill the switch sequence role. Appendix C shows possible header processing architectures for a 100 switch sequence and a 110 switch sequence respectively. Thus the parallel processing architecture proposed in this investigation is very fluid (i.e. it can change with the change in switching node demand). Thus by changing the architecture's parallel processing configuration the packet can be routed to a different output with the same header as previously.

The potential for propagation of the full packet (including the header bit sequence) exists because of the parallel processing output which can be used to control the header bit sequence throughput and addition in front of the payload packet (refer to Appendix D for a possible configuration utilizing this methodology).

Thus in conclusion a novel all-optical parallel processing three bit switching node structure has been proposed and the results verified. The advantages of the architecture proposed and investigated here includes potential for scalability, fluidity, switching ratio, the potential for realizing higher capacities than electronic routers, the possibility to improve the bandwidth utilization within the optical layer, and the potential for increased throughput.

REFERENCES

[1] R. Ramaswami, K.N. Sivarajan, *Optical Networks: A practical perspective*, second edition, Academic Press, San Diego, pg. 12, 2002.

[2] S. Aleksić, V. Krajinović, K. Bengi, An overview on Technologies for Access Nodes in Ultra-Fast OTDM Photonic Networks, *Photonic Network Communications*, Vol. 3, Numbers 1/2, pp. 75, January-June 2001.

[3] S. Johanson, Transport network involving a reconfigurable WDM network layer – A European demonstration, *Journal of Lightwave Technology*, Vol. 14, pp. 1341-1348, June1996.

[4] T. Miyakawa *et. al.*, An experiment of optical add-drop multiplexer using fibre grating and its limiting factor, *Tech. Digest OECC'96*, paper17B3-5, Chiba, Japan, July 1996.

[5] M.J.O'Mahoney, *et al*, The application of optical packet switching in future communication networks, *IEEE Communications Magazine,* pp. 128-135, 2001.

[6] N. Calabretta, *et al*, Ultrafast Asynchronous Multioutput All-Optical Header Processor. *IEEE Photonics Technology Letters,* Vol. 16, No. 4, pp. 1182-1184, Apr. 2004.

[7] C. Guillemot, *et al*, Transparent Optical Packet Switching: The European ACTS KEOPS Project Approach, *Journal of Lightwave Technology*, Vol. 16, No. 12, pp. 2117-2134, Dec. 1998.

[8] I Glesk, KI Kiang and PR Prucnal, Demonstration of ultra-fast all-optical packet router, *ELECTRONICS LETTERS*, Vol. 3, No. 9, pp. 794-795, Apr. 1997.

[9] R. Ramaswami, K.N. Sivarajan, *Optical Networks: A practical perspective*, second edition, Academic Press, San Diego, pp. 616, 2002.

[10] MT Hill, EEE Frietman, H de Waardt and HJS Dorren, All fiber-optic neural network using coupled SOA based ring lasers, *IEEE Transactions on Neural Networks*, Vol. 13, No. 6, pp. 1504-1513, Nov 2002.

[11] EEE Frietman, MT Hill and GD Khoe, A Kohonen neural network controlled all-optical switching node system, *International Journal of Computer Research*, Vol. 10, No. 2, pp. 251-267, 2001.

[12] S.B. Colack, J.J.H.B. Schleipen and C.T.H. Leidenbaum, Neural network using longitudinal modes of an injection laser with external feedback, *IEEE Transactions on Neural Networks*, Vol. 7, pp. 1389-1400, Nov. 1996.

[13] K Ishida, H Nakamura, H Matsumura, T Kadoi and H Inoue, InGaAsP/InP optical switches using carrier induced refractive index change, *Appl. Phys. Lett.,* 50, pp. 141-142, 1987.

[14] Y. Guo, C.K. Kao, E.H. Li, K.S. Chiang, *Nonlinear Photonics: Nonlinearities in Optics, Optoelectronics and Fiber Communications*, Chinese University Press, Hong Kong, pp. 207-208, 2002.

[15] TV Dolgova, MG Martemyanof, AA Fedyanin and OA Aktsipetrof, Microcavity enhancement of nonlinear response of one-dimensional photonic crystals based on porous silicon, *Proc. QELS 2001*, pp. 157.

[16] BE Olsson and PA Andrekson, Polarization independent Kerr-Switch using polarization diversity loop, *Proc. ECOC'98*, Madrid, pp. 185-186, Sept 1998.

[17] M. Asobe, T. Kanamari, H. Itoh and T. Kaino, Ultrafast and efficient optical Kerr effects in chalcogenide glass fibers and the application in all-optical switching, Nonlinear Optics: Materials, Fundamentals and Applications, NLO'94 IEEE, pp. 306-308, July 1994.

[18] MJ Potasek and T Campbell, All-optical switch using multi-terabit/sec pulses, *CLEO'01 Technical Digest*, Summaries of papers presented at the Conference on Lasers and Electro-Optics, pp. 180-181, May 2001.

[19] RV Penty, Picosecond optical switching using near bandedge nonlinearities in semiconductor waveguides, *IEE Colloquium on Ultra-Short Optical Pulses*, pp. 6/1-6/4, Nov 1993.

[20] K Morito, J Leuthold and H Melchior, Dynamic analysis of MZI-SOA all optical switches for balanced switching, *ECOC'97*, Conference Publication no. 448, pp. 81-84, Sept 1997.

[21] P. Toliver, R.J. Runser, I. Glesk, and P.R. Prucnal, Comparison of three nonlinear optical switch geometries, *Technical Digest of CLEO 2000*, paper CWD2, San Francisco, California, pp. 254-255, May 2000.

[22] Manning, R. J. & Ellis, A.D. *et. al.* (1997), "Semiconductor laser amplifiers for ultrafast all-optical signal processing", *Journal of the Optical Society of America B*, vol. 14, no. 11, pp. 3204-3216.

[23] A. Ehrhardt, *et al*, Semiconductor Laser Amplifier as Optical Switching Gate, *Journal of Lightwave Technology*, Vol. 11, No. 8, pp. 1287-1295, Aug. 1993.

[24] Hill, M.T. & Srivatsa, A. *et. al.* (2001), "1x2 Optical packet switch using all-optical header processing", *Electronics Letters*, vol. 37, no. 12, pp. 774-775.

[25] Srivatsa, A. & d. Waardt, H. *et. al.* (2001), "All-optical serial header processing based on two-pulse correlation", *Electronics Letters*, vol. 37, no. 4, pp. 234-235.

[26] G. Keiser, *Optical Fiber Communications*, third edition, McGraw-Hill, Singapore, pp. 496, 2000.

[27] MN Islam, CE Soccolich, CJ Chen, KS Kim, JR Simpson and UC Paek, All-optical inverter with one picojoule switching energy, *ELECTRONICS LETTERS*, Vol. 27, No. 2, pp. 130-132, Jan 1991.

[28] N. Kashima, *Passive Optical Components for Optical Fiber Transmission,* Artech House, Boston, 1995.

[29] A. Neukermans and R. Ramaswami, MEMS technology for optical networking applications, *IEEE Communications Magazine,* 36(12):62-69, Jan. 2001.

[30] L.Y. Lin, E.L. Goldstein, R.W. Tkach, Free-spaced micromachined optical switches with submillisecond switching time for large-scale optical cross-connects. *IEEE Photonics Technology Letters,* 10(4):525-528, Apr. 1998.

[31] J.E. Fouquet, Compact optical cross-connect switch based on total internal reflection in a fluid-containing planar lightwave circuit, *OFC 2000 Technical Digest*, pp. TuM1-1-TuM1-4, 2000.

[32] K. Y. Wu, J.Y. Liu, Liquid-crystal space and wavelength routing switches, *Proceedings of Lasers and Electro-Optics Society Annual Meeting,* pp. 28-29, 1996.

[33] J.S. Patel, Y. Silberberg, Liquid crystal and grating-based multiple-wavelength cross-connect switch, *IEEE Photonics Technology Letters*, 7(5): 514-516, May 1995.

[34] J. Gruber, *et al*, The Photonic Switch/Cross-Connect (PSX) – It's Role in Evolving Optical Networks, AMTC, Vol. 1, San Diego, CA, July 17-20, 2000, pp. 101-114.

[35] J. Gruber and R. Ramaswami, Moving Toward All-Optical Networks, Lightwave Mag., pp. 60-68, Dec. 22, 2000.

[36] J. Gruber, *et al*, Architectures for the Optical Internet, NFOEC 2001, Baltimore, MD, 8-12 July, 2001.

[37] P.R. Prucnal, *et al*, Signal Processing in high speed OTDM networks, Proceedings of ECOC '98, pp. 17-19, 20-24 September, 1998, Madrid, Spain.

[38] L. Margherio, *et al*, *The Emerging Digital Economy*, U.S. Department of Commerce, 1998.

[39] Q. Yang, *et al*, WDM Packet Routing for High-Capacity Data Networks, *Journal of Lightwave Technology*, Vol. 19, No. 10, pp. 1420-1426, Oct. 2001.

Appendix A: Technical Diagrams

1. INTRODUCTION

VPIsystems™ provides VPItransmissionMaker™ which is an optical fibre communication system simulation package. VPItransmissionMaker™ is a Photonic Design Automation (PDA) tool that assists development by:

- reducing the need for physical experimenting with virtual prototyping
- familiarizing designers with next generation technology before commercial availability
- stimulating innovation by expanding design resources and possibilities

VPItransmissionMaker™ allows the designer of an optical network or component to decide the trade-off between simulation speed and accuracy. It has the ability to simulate the electrical and the optical domain; it can simulate a Wavelength Division Multiplexing (WDM) optical network, an OTDM network, or a simple analogue optical channel. The levels that can be designed with VPItransmissionMaker™ include designs at the network architecture level or the component level. VPItransmissionMaker™ is an open architecture fourth generation PDA tool with a comprehensive library of photonic component and system models.

VPItransmissionMaker™ was the optical software package used to determine the feasibility of the three-bit parallel processing all-optical switching node. VPItransmissionMaker™ works at three different levels namely stars, galaxies and universes. A star is an individual component model, a galaxy is an interconnected collection of components with ports to other levels, and a universe is a collection of stars and galaxies with no interconnection to higher levels. Stars and galaxies were used in the simulated experiments. A star is shown in figure A.1 together with some additional information, and a galaxy is shown in figure A.2 together with some additional information. A universe is also shown in figure A.3 even though it wasn't used as such.

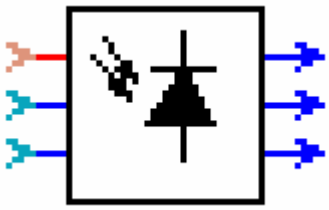

Figure A.1

A typical icon representing a star in VPItransmissionMaker™.

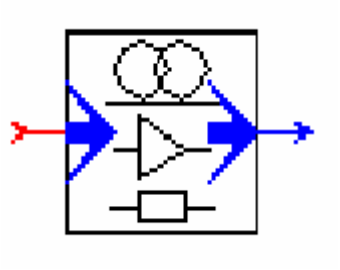

Figure A.2

The icon representing a galaxy in VPItransmissionMaker™.

Figure A.3

The icon representing a universe in VPItransmissionMaker™.

2. XGM SWITCH

Figure A.4 shows the XGM switch of figure 2.2 as it is constructed in VPItransmissionMaker™. Figures A.5 and A.6 shows an increased resolution of the left and right halves of figure A.1 respectively.

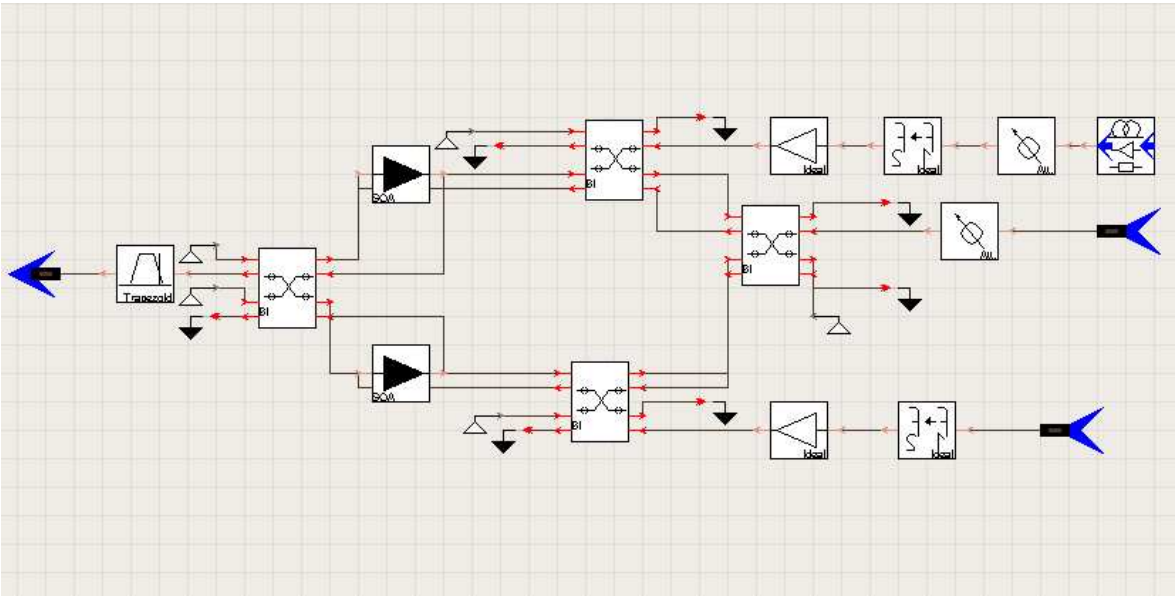

Figure A.4

The Cross-Gain Modulator configuration of figure 2.2 as it is constructed in VPItransmissionMaker™.

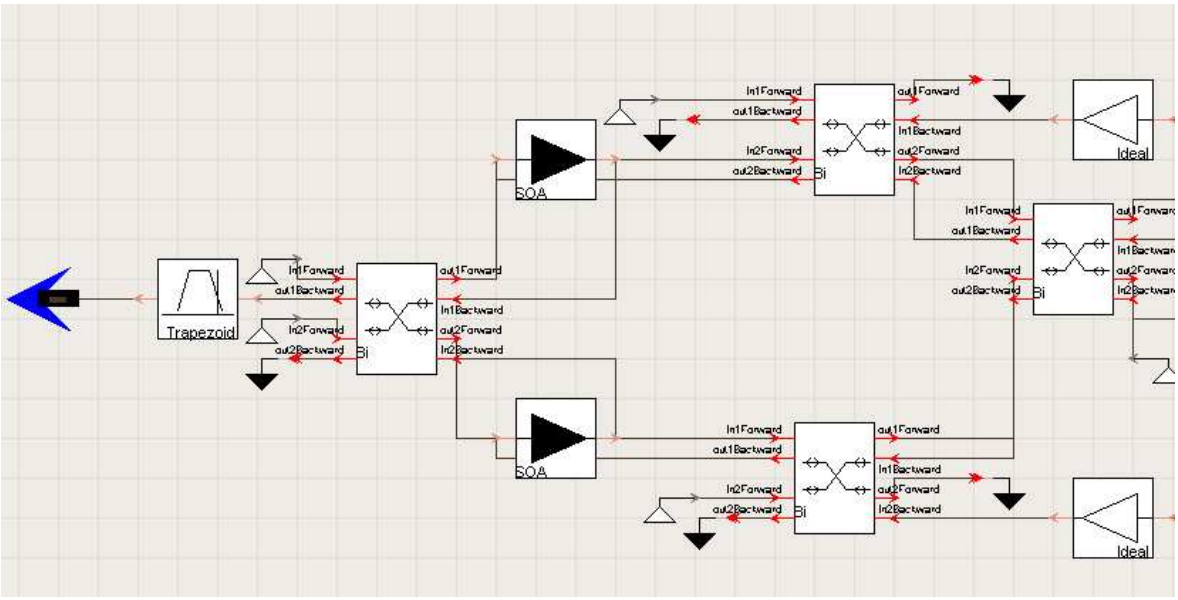

Figure A.5

An increased resolution of the left half of the Cross-Gain Modulator configuration of figure 2.2 as it is constructed in VPItransmissionMaker™.

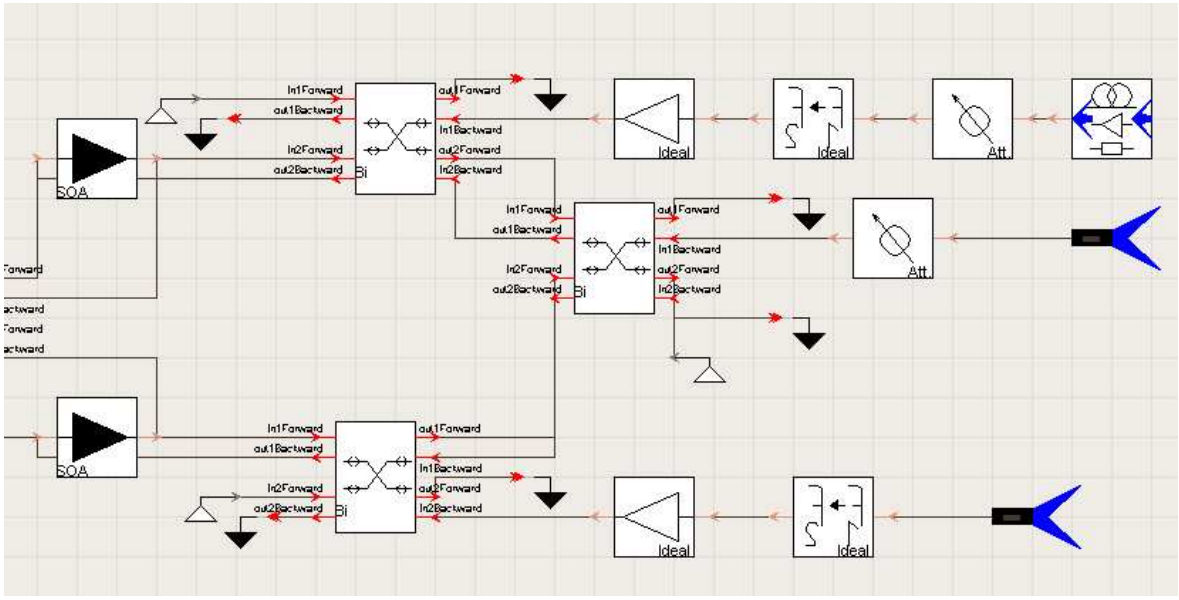

Figure A.6

An increased resolution of the right half of the Cross-Gain Modulator configuration of figure 2.2 as it is constructed in VPItransmissionMaker™.

As can be seen in figure 2.2 the SMZ optical switch uses three inputs (control 1, control 2 and a data input). In figure A.4 and figure 2.2 the use of only two inputs is apparent. This is because the SMZ switch of figure 1.3 was slightly modified in order to use only two inputs. This was done by making the control 1 input a constant "1" input (i.e. it is constantly outputting 1 mW). This makes the SMZ switch dynamics only dependant on the other two inputs. All of the inputs to the simulations were controlled by text files in which 1's and 0's indicate the wanted input bit sequences. Each input (e.g. constant 1, header input and payload input) has its own text file specifying a bit sequence. The constant one for control one is generated by a galaxy and is shown in figure A.7 below.

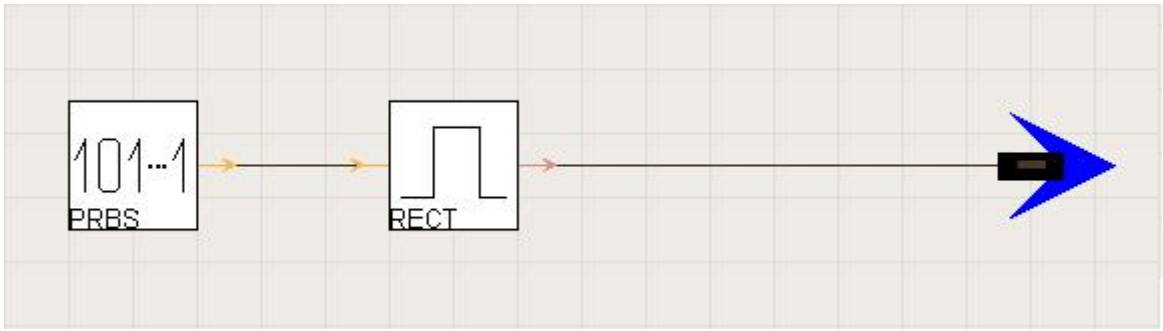

Figure A.7

The VPItransmissionMaker™ galaxy used in the SMZ switch to generate a continuous wave optical signal for the control 1 input.

3. OPTICAL INVERTER

The structure of the optical inverter as shown in figure 2.4 is generated by a VPItransmissionMaker™ galaxy which is shown in figure A.8.

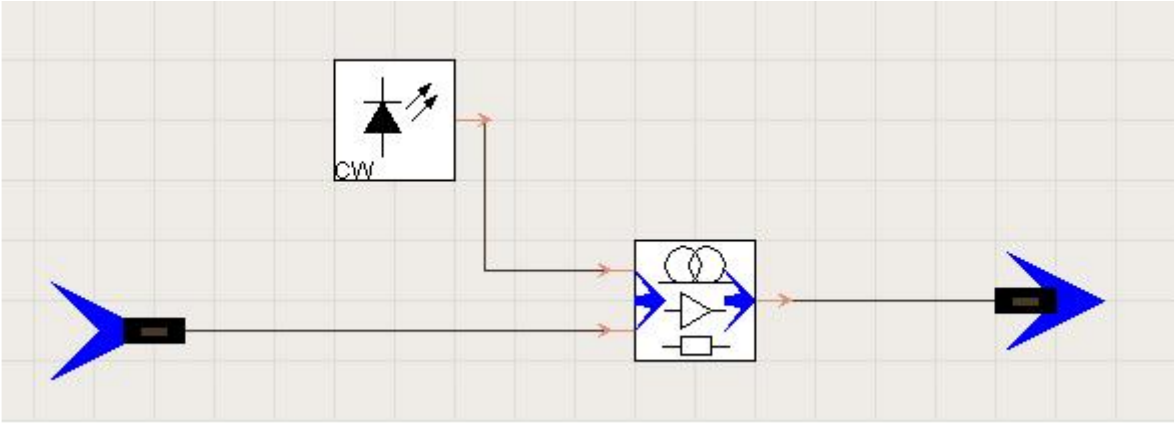

Figure A.8

The all-optical inverter created in VPItransmissionMaker™ which uses the SMZ switch galaxy of figure A.1 and figure 2.2.

4. SWITCHING NODE

The structure of the three-bit parallel processing all-optical switching node is shown in figure A.9.

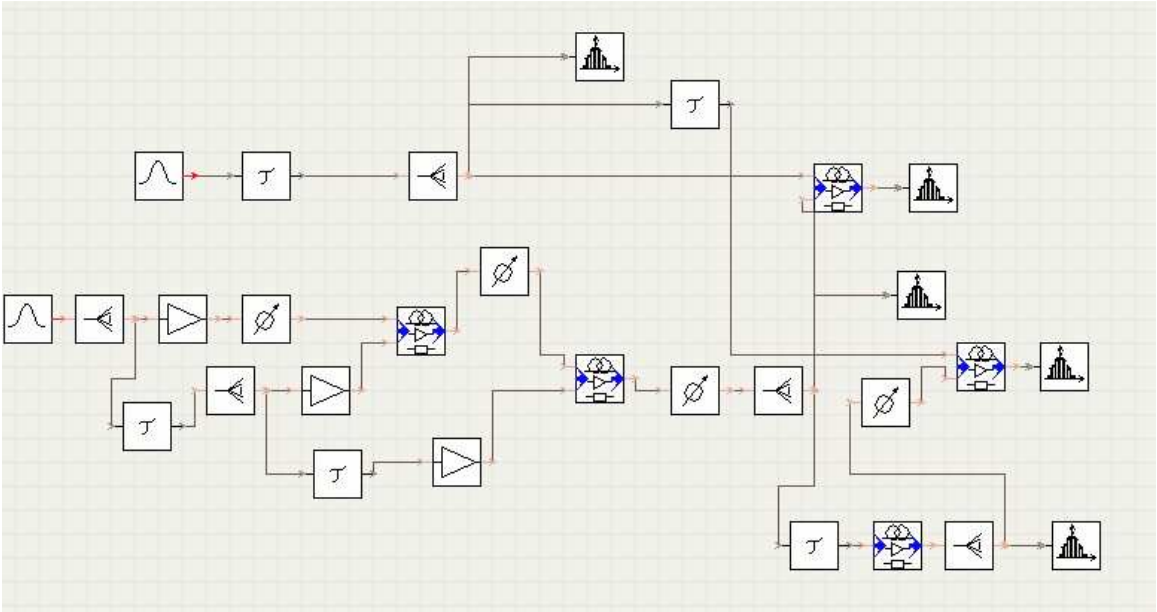

Figure A.9

A three-bit parallel processing all-optical switching node created in VPItransmissionMaker™ which uses the XGM switch galaxy.

Figure A.10 and A.11 shows an increased resolution of the left and right halves of figure A.9 respectively.

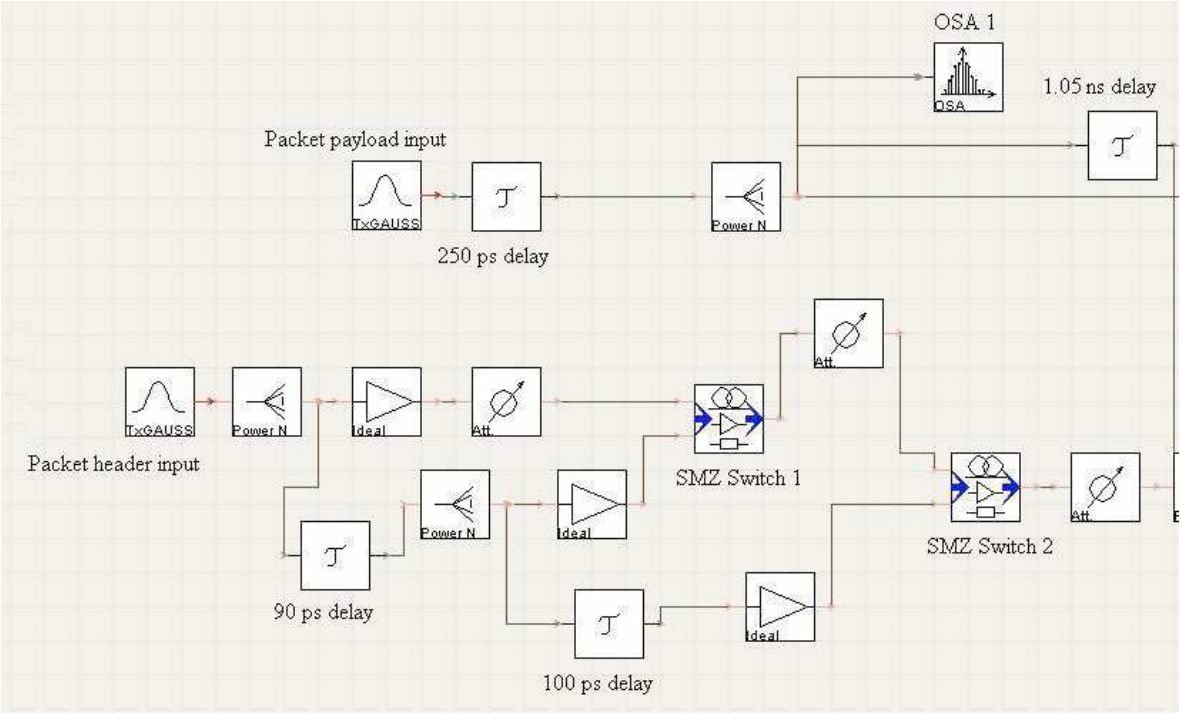

Figure A.10

An increased resolution of the left half of the three bit parallel processing all-optical switching node structure of figure A.9.

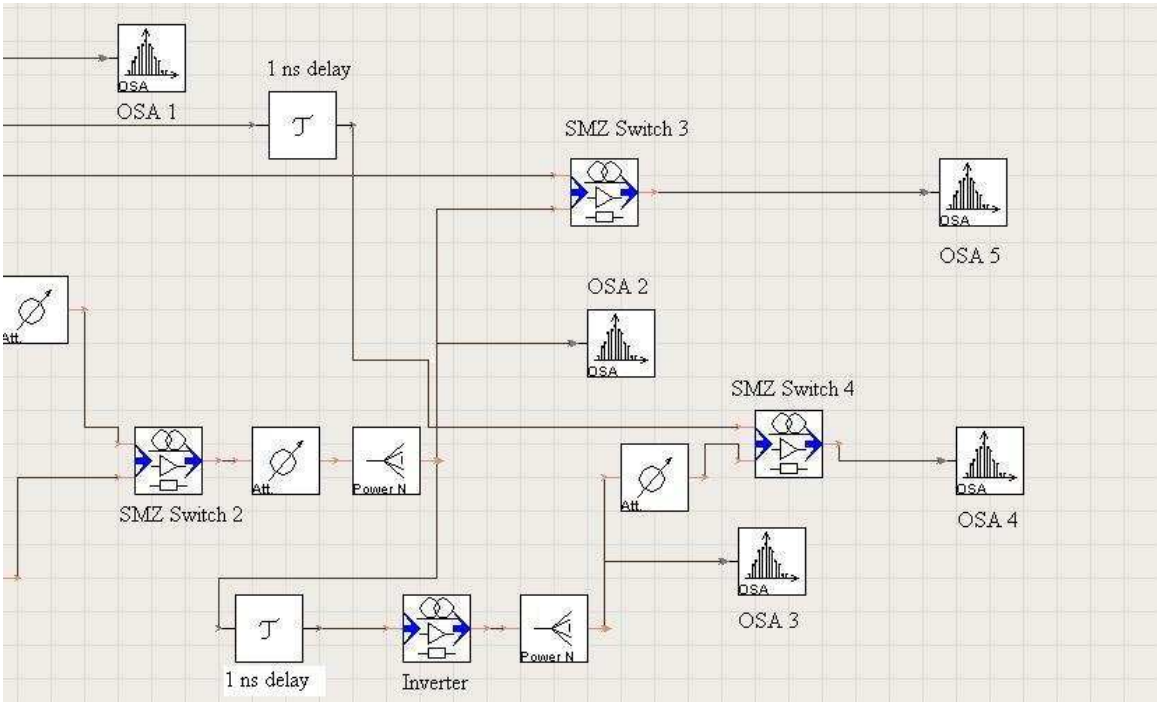

Figure A.11

An increased resolution of the right half of the switching node structure of figure A.9.

The following components are used in the simulations of the structures indicated above. A bit sequence generator which is shown in figure A.12 below.

Figure A.12

A controlled bit sequence generator which receives the bit sequence from a text file.

The bit sequence generator used the text file as input and generated the appropriate signal for the optical rectangle generator. An optical rectangle generator is shown in figure A.13 below.

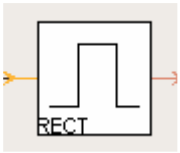

Figure A.13

An optical rectangle generator which receives the bit sequence from bit sequence generator and produces optical rectangles at its output.

An optical splitter is shown in figure A.14 below ad is used to split the incoming optical power into N required outputs.

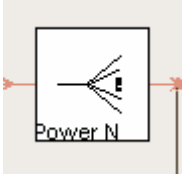

Figure A.14

A 1xN optical splitter used to split an optical signal equally to N different optical outputs.

An optical amplifier is shown in figure A.15 below. The exact type of amplifier used is irrelevant, but an EDFA sufficed.

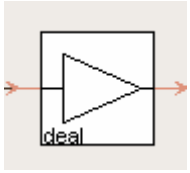

Figure A.15

An optical amplifier.

An Optical Spectrum Analyzer was used to measure the results and an example of the icon representing one is shown in figure A.16 below.

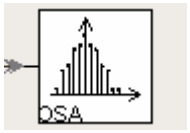

Figure A.16

An OSA used to measure the output results obtained in the simulated experiments.

Attenuators were used to fine-tune the different optical powers to obtain the desired results and an example of the icon used to represent an attenuator in the simulations is shown in figure A.17 below.

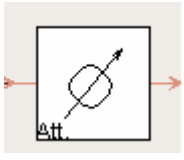

Figure A.17

An attenuator used to fine-tune optical powers in the simulations.

Optical delays were used in the experiments to correlate the different signals with each other and an example of an optical delay icon used in the simulations is shown in figure A.18 below.

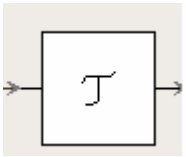

Figure A.18

An optical delay icon used to delay optical signals in the simulations.

A figure of the SOAs used in the simulations is shown in figure A.19 below.

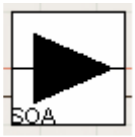

Figure A.19

A SOA used in the simulations as the active device.

An optical coupler used in the experiments is shown in figure A.20 below.

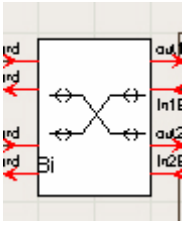

Figure A.20

An optical coupler use din the experiments.

The icon used to do the frequency shifting inside the optical switches is shown in figure A.21 below.

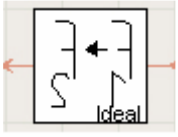

Figure A.21

An optical frequency (wavelength) converter used in the experiments.

The icon used to generate the Gaussian optical pulses for the header input and the payload input is shown in figure A.22 below.

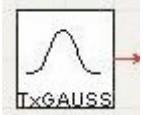

Figure A.22

A Gaussian pulse generator used in the experiments.

Appendix B: Possible Four Bit Parallel Processing Architecture

The structure of a possible four bit parallel processing all-optical switching node is shown in figure B.1.

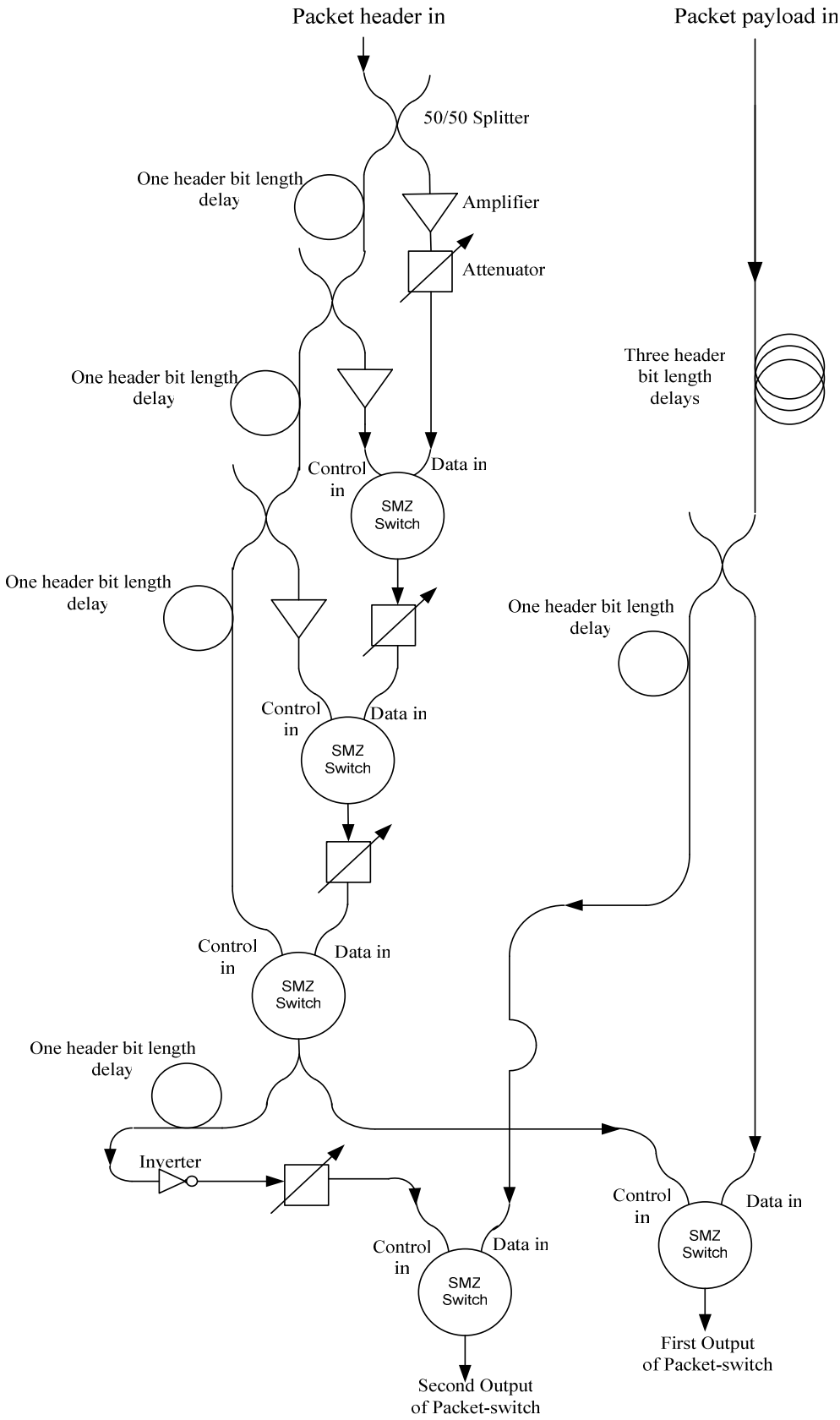

Figure B.1

An optical switching node using a unique four bit parallel processing technique and output switches.

Appendix C: Header Processing Architecture for Alternative Switching Sequences

The structure of a possible three bit parallel processing architecture for a 010 switch sequence is shown in figure C.1.

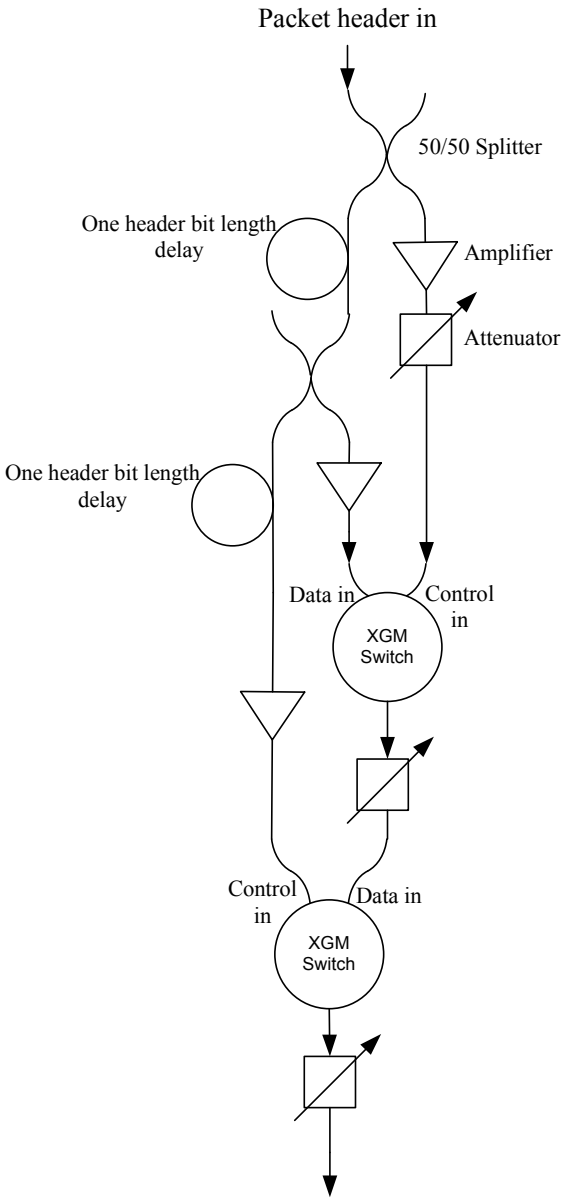

Figure C.1

Parallel processing architecture for a 010 switch sequence. The architecture differs from the original of figure 2.1 in the top XGM switch inputs. The Data in input for the top XGM switch is the delayed input from the packet header in.

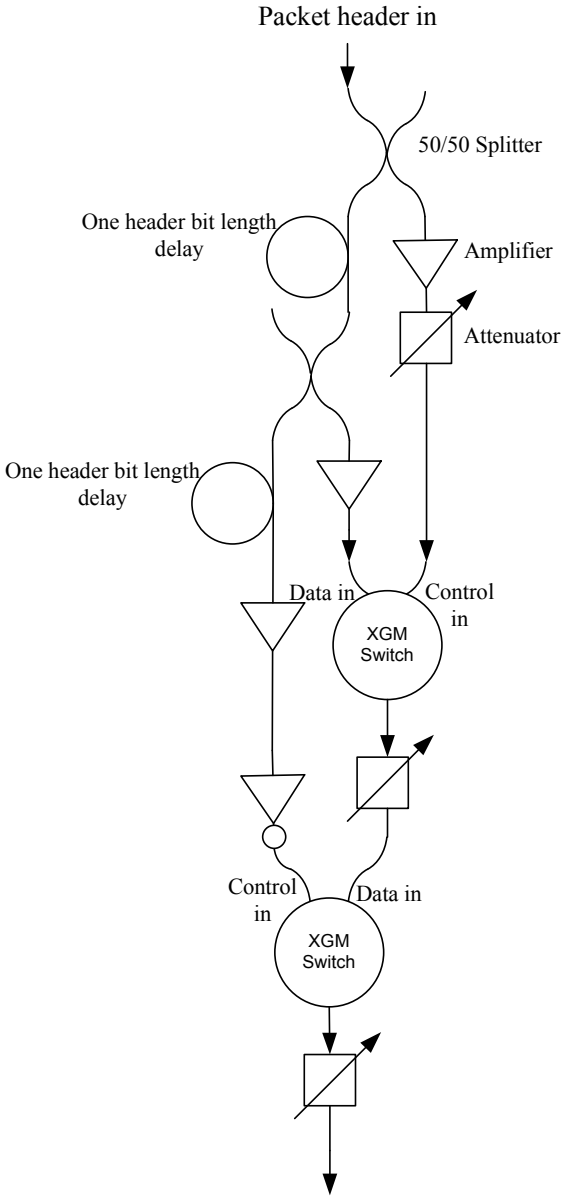

Figure C.2

Parallel processing architecture for a 110 switch sequence. The architecture differs from the original of figure 2.1 in the top XGM switch inputs. The Data in input for the top XGM switch is the delayed input from the packet header in and the bottom XGM switch has its control input inverted.

Appendix D: Architecture Including Headers in Outputs

The structure of a possible three bit parallel processing architecture that inserts the header packet (which was input to the node) in front of the payload packets before they exit the node is shown in figure D.1.

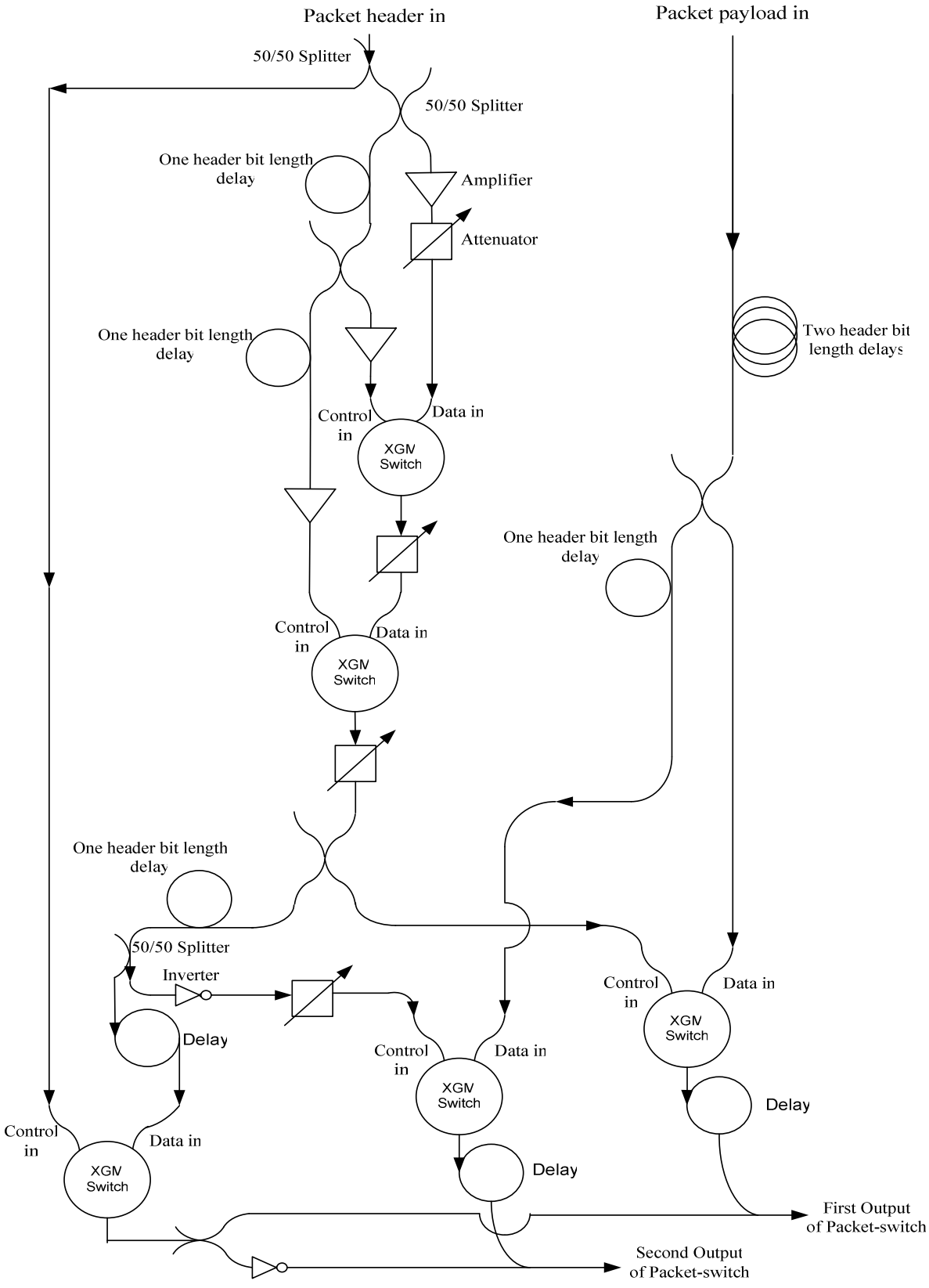

Figure D.1

Parallel processing architecture for a switch where the outputs payload packets are reconciled with the original header packets that resulted in the specific switch sequence.