DSSS COMMUNICATION LINK EMPLOYING COMPLEX SPREADING SEQUENCES

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By

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Submitted in partial fulfillment of the requirements for the degree

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FORM A

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SUMMARY

DSSS COMMUNICATION LINK EMPLOYING COMPLEX SPREADING SEQUENCES

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Master of Engineering (Electronics)

The present explosion in digital communications and multi-user wireless cellular networks has urged a demand for more effective modulation methods, utilizing the available frequency spectrum more efficiently. To accommodate a large number of users sharing the same available frequency band, one requirement is the availability of large families of spreading sequences with excellent AC and CC properties. Another requirement is the availability of sets of orthogonal basis functions to extend capacity by exploiting all available degrees of freedom (e.g., temporal, frequency and spatial dimesions), or by employing orthogonal multi-code operation in parallel, such as used in the latest 3GPP and 3GPP2 Wide-band Code Division Multiple Access (WCDMA) modulation standards by employing sets of orthogonal Walsh codes to improve the overall data throughput capacity. The generic Direct Sequence Spread Spectrum (DSSS) transmitter developed in this dissertation has originally been designed and implemented to investigate the practicality and usefulness of complex spreading sequences, and secondly, to verify the concept of non-linearly interpolated root-of-unity (NLI-RU) filtering. It was found that both concepts have a large potential for application in point-to-point, and particularly micro-cellular Wireless Local Area Networks (WLANs) and Wireless-Local-Loop (WLL) environments. Since then, several novel concepts and subsystems have been added to the original system, some of which have been patented both locally and abroad, and are outlined below. Consequently, the ultimate goal of this research project was to apply the principles of the generic DSSS transmitter and receiver developed in this study in the implementation of a WLL radio-frequency (RF)-link, and particularly towards the establishment of affordable wireless multimedia services in rural areas. The extended coverage at exceptionally low power emission levels offered by the new design will be particularly useful in rural applications. The proposed WLL concept can for example also be utilized to add a unique mobility feature to for example existing Private Automatic Branch Exchanges (PABXs). The proposed system will in addition

offer superior teletraffic capacity compared to existing micro-cellular technologies, e.g., the Digital European Cordless Telephony (DECT) system, which has been consider by Telkom for employment in rural areas. The latter is a rather outdated interim standard offering much lower spectral efficiency and capacity than competitive CDMA-solutions, such as the concept analyzed in this dissertation, which is based on the use of unique large families of spectrally well confined (i.e., band-limited) constant envelope (CE) complex spreading sequences (CSS) with superior correlation properties. The CE characteristic of the new spreading sequences furthermore facilitates the design of systems with superior power efficiency and exceptionally robust performance characteristics (much less spectral re-growth) compared to existing 2G and 3G modulation standards, in the presence of non-linear power amplification. This feature allows for a system with larger coverage for a given performance level and limited peak power, or alternatively, longer battery life for a given maximum communication distance and performance level, within a specified fixed spreading bandwidth. In addition, the possibility to extend the concept to orthogonal multi-code operation provides for comparable capacity to present 3G modulation standards, while still preserving superior power efficiency characteristics in non-linear power amplification. Conventional spread spectrum communication systems employ binary spreading sequences, such as Gold or Kasami sequences. The practical implementation of such a system is relatively simple. The design and implementation of a spread-spectrum communication system employing complex spreading sequences is however considerable more complex and has not been previously presented, nor been implemented in hardware. The design of appropriate code lock loops for CSS has led to a unique design with 3dB performance advantage compared to similar loops designed for binary spreading sequences. The theoretical analysis and simulation of such a system will be presented, with the primary focus on an efficient hardware implementation of all new concepts proposed, in the form of a WLL RF-link demonstrator.

Keywords:

Multi-Dimensional Direct Sequence Spread Spectrum (MD-DSSS), Families of Complex Spreading Sequences (CSS), Non-linearly Interpolated Root-of-Unity (NLI-RU) filtering, Complex Code Lock Loop (CCLL), Peak-to-Average Power Ratio (PAPR), PAPR Complementary Cumulative Distribution Function (CCDF), power and spectrally efficient modulation technique, DSSS Wireless RF Link.

OPSOMMING

DSSS COMMUNICATION LINK EMPLOYING COMPLEX SPREADING SEQUENCES

deur

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Die huidige ontploffing in syferkommunikasie- en multi-gebruiker draadlose sellulêre dienste het die aanvraag na meer effektiewe modulasiemetodes, asook die meer effektiewe gebruik van frekwensiespektrum, sterk laat toeneem. Ten einde ’n groot aantal gelyktydige medegebruikers van dieselfde spektrum moontlik te maak, word die beskikbaarheid van groot families spreisekwensies met uitstekende outokorrelasie- (OK) en kruiskorrelasie- (KK) eienskappe benodig. ’n Verdere vereiste is die beskikbaarheid van stelle ortogonale basisfunksies waarmee die stelselkapasiteit uitgebrei kan word, deur die eksploitering van alle moontlike beskikbare vryheidgrade (dws, temporale, frekwensie en ruimtelike dimensies), of deur die aanwending van veelvuldige ortogonale kodes (spreisekwensies) in parallel, soos byvoorbeeld in die jongste 3GPP en 3GPP2 Wyeband Kode-Divisie Multi-Toegang (WKDVT of ’WCDMA’) modulasiestandaarde gebruik word, deur van stelle ortogonale Walsh codes gebruik te maak om die resultante data-deursettempo te verbeter. Die generiese DSSS-sender wat in hierdie verhandeling ontwikkel word, is oorspronklik ontwerp en geïmplementeer om eerstens die realiseerbaarheid en bruikbaarheid van komplekse spreisekwensies te ondersoek, en om tweedens die konsep van ’n nie-lineêre eenheidswortelfiltertegniek te verifieer en te evalueer. Dit is bevind dat beide konsepte ’n groot potensiaal vir aanwending in punt-tot-punt, en spesifiek mikro-sellulêre draadlose lokale-area netwerke (DLAN of ’WLAN’) en draadlose lokale-lus (DLL of ’WLL’) toepassings toon. Sederdien was die hoofoogmerk van hierdie verhandeling om die generiese sender en ontvanger wat uit hierdie navorsings- en ontwikkelingsprogram voortgevloei het, in die implementering van een tipiese WLL RF-skakel aan te wend, en spesifiek vir die aanwending daarvan as syferkommunikasiemedium in plattelandse gebiede. Die besondere groot dekking teen buitengewone lae drywingsuitsetvlakke wat deur die nuwe ontwerp moontlik gemaak word, maak dit uiters geskik vir aanwending in hierdie gebiede. Dieselfde konsepte kan byvoorbeeld ook in ’WLL’-toepassings aangewend word, waardeur ’n mobiele dimensie aan bestaande statiese

private outomatiese taksentrales (POTS of ’PABXs’) verleen kan word. Die voorgestelde stelsel sal ook verbeterde televerkeerskapasiteit in vergelyking met bestaande mikro-sellulêre tegnieke bied, soos bv die DECT-stelsel, wat deur Telkom oorweeg is vir gebruik in plattelandse gebiede. Laasgenoemde is tans ’n betreklik verouderde interim-standaard met baie laer spektrale effektiwiteit en kapasiteit as kompeterende CDMA-oplossings, as bv die modulasie-konsep wat in hierdie verhandeling voorgestel word. Laasgenoemde is gebaseer op die gebruik van groot families unieke konstante-omhulling (KO) komplekse spreisekwensies (KSS) met goeie spektrale konsentrasie (dws, bandbeperk), sowel as met uitstekende korrelasie-eienskappe. Die KO-eienskappe van hierdie nuwe spreisekwensies maak verder die ontwerp van stelsels met verbeterde drywingseffektiwiteit en buitengewone robuuste werkverrigtingseienskappe moontlik, met veel minder spektrale groei in vergelyking met bestaande 2G en 3G modulasiestandaade in die teenwoordigheid van nie-lineêre drywingsversterking. Hierdie eienskappe maak stelsels met groter radiodekking vir ’n gegewe werkverrigtingspeil moontlik, of alternatiewelik, ’n langer batteryleeftyd vir ’n gegewe maksimum kommunikasie-afstand en werkpeil, binne ’n gespesifiseerde (vaste) spreibandwydte. Hierby bied die moontlikheid om die modulasietegniek na veelvuldige kodes uit te brei, vergelykbare kapasiteit met huidige 3G modulasiestandaarde, terwyl die superieure drywingseffektiwiteitskarakteristieke in die teenwoordigheid van nie-lineêre drywingsversterking gehandhaaf word. Die analise en ontwerp van konvensionele sprei-spektrum tegnieke wat van binêre spreisekwensies, soos Gold en Kasami, gebruik maak, is relatief eenvoudig. Die ontwerp en realisering van ’n spreispektrum-stelsel wat van komplekse spreisekwensies gebruik maak, is egter aansienlik komplekser, en is na die beste wete van die skrywer nog nie voorheen aangebied, of in hardeware gerealiseer nie. Die ontwerp van geskikte kode-sluit-lusse (KSL) vir gebruik met komplekse spreisekwensies het gelei tot ’n unieke ontwerp met ’n 3 dB werkverrigtingsvoorsprong relatief tot soortgelyke lusse vir binêre spreisekwensies. Die teoretiese ontwerp, simulasie en implementering van sodanige stelsel word in hierdie verhandeling aangebied, met die primêre fokus op die effektiewe en ekonomiese implemtering van al die onderliggende substelsels wat die volledige prototiepe WLL RF-skakel uitmaak.

Sleutelwoorde:

Multi-Dimensionele Direkte-Sekwensie Sprei-Spektrum (MD-DSSS), Families Komplekse Spreisekwensies (KSS), Nie-Lineêr Geïnterpoleerde Eenheidswortel filters, Komplekse Kode-Sluit-Lus (KKSL), Piek-tot-Gemiddelde Drywingsverhouding (PGDV), Komplementêre Kumulatiewe Distribusie-Funksie (KKDF), drywings- en spektraal-effektiewe modulasietegniek, DSSS Draadlose RF-verbinding.

To God Almighty

for all the opportunities and His grace

and

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my late Father, my Mother, Brother, family

and my family in law

who supported me through my years of study.

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CONTENTS

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PART I

OVERVIEW OF THE DSSS COMMUNICATION SYSTEM

CHAPTER ONE
INTRODUCTION AND OVERVIEW

This chapter provides an overview of the DSSS communication system employing complex spreading sequences presented in this dissertation. The first sections of this chapter give an introduction as well as the main objectives of the dissertation. This is followed by the outline of the dissertation illustrated by a schematic representation. The contributions of this research and development are discussed and the chapter is then concluded with an overview of a generic DSSS system.

1.1 OVERVIEW OF THE GENERIC DSSS SYSTEM

The use of DSSS techniques in communication systems has grown considerably over the past decade. This is because CDMA is considered a promising technique to obtain high spectral and power efficiency (low fading margin) in multiple-access applications, such as for example in personal communication networks (PCN), in addition to its well-known merits in the field of secure communications. A DSSS system employing complex spreading sequences may include several additional advantages [1], [2], [3], such as offering a perfectly constant envelope output signal, including the possibility to generate a SSB DSSS signal with theoretically up to $6dB$ more PG than offered by conventional DSB systems, while still exhibiting comparable auto and improved cross correlation properties compared to any other (binary) DSSS schemes presently employed [4].

This dissertation describes the theoretical analysis [5–8] of a novel DSSS transmitter and receiver structure employing complex spreading sequences. The structure is generic in the sense that it can be employed in many different ways, i.e., in a balanced QPSK

configuration [1] or in a normal dual-channel QPSK configuration [2] by using most of the common multi-amplitude multi-phase (QAM) modulation strategies. The output signal of the transmitter is generated by means of complex multiplication of the input data, the complex spreading sequences and the quadrature carriers and by finally taking the real part of the result. The receiver structure is responsible for demodulation and despreading of the received DSSS signal. Diversity is built into the system by utilizing a balanced mode of operation. In the balanced mode of operation, when either the in-phase or quadrature-phase components of the signal is eliminated during transmission, the original data can still be recovered from the remaining signal component.

A description of the complex spreading sequences with their properties will be given, as well as simulation results of the system employing these complex sequences [9]. The simulation results will include both the double side band (DSB) and single side band (SSB) cases, which both provides constant output signal envelopes [10]. Another advantage of using chirp-like complex spreading sequences is the fact that they can be band limited by means of novel mod-π or analytical mod-2π root-of-unity filtering processes, while still maintaining a perfectly constant envelope output signal.

The theoretical analysis will then be used as a basis for the practical implementation of the system. A brief description of the operation of the practical system will be given, as well as practical results obtained from a generic hardware implementation of the DSSS communication link.

The DSSS system provides a choice of data rates by selecting different families and lengths of spreading sequences for a given chip rate and transmission bandwidth. A minimum PG of at least 10 dB is maintained throughout, although PGs of more than 30 dB are feasible. The proposed DSSS system may be readily expanded to serve a multi-user CDMA-DSSS environment. This is however not incorporated into this dissertation, but left as a future exercise.

1.2 MAIN OBJECTIVES

The main objective of this dissertation is the hardware implementation of a prototype two-dimensional (QPSK) DSSS baseband modem employing complex spreading sequences, including all synchronisation subsystems necessary to achieve coherent DSSS

[1] Balanced operation implies that the input data stream is duplicated on the in-phase (I) and quadrature phase (Q) branches prior to modulation onto quadrature carriers.
[2] Dual-channel operation implies that the incoming data is serial-to-parallel converted into two quadrature half rate symbol streams prior to quadrature modulation.

communication. Although the modulation principles presented may be extended to more than two dimensions, this will be specifically reserved for future research. A detailed design and analysis of the DSSS system are two of the primary objectives of this study. The study will mostly focus on the performance of the system in the AWGN channel, although some simulation results will be presented to illustrate the operation of the system under fading channel conditions, as well as in the presence of a number of users sharing the same bandwidth. Multi-user detection, cancellation and RAKE-combining have however been explicitly excluded from the hardware design as a result of the complexity of the project as it stands. These aspects are also the objectives of a companion dissertation. Some multi-user results under various Rayleigh-fading mobile channel conditions will nevertheless be presented for comparison purposes, where appropriate. The implementation of the new DSSS communication system involved the analysis and design of unique synchronization loops for code tracking and carrier phase estimation, as a result of the use of complex spreading sequences. Extensive analytical analysis and theoretical as well as simulation results will be presented to verify correct operation of all subsystems, as well as the complete DSSS system, including the RF-link. The latter subsystem

The dissertation objectives can be summarized as follows:

- Theoretical design and analysis of a DSSS communication system employing complex spreading sequences.
- Simulation of a DSSS wireless communication link employing complex spreading sequences.
- Design of implementation structures for the transmitter and receiver of a DSSS communication system with complex spreading sequences, employing appropriate (FPGA) implementation technologies.
- Design and realisation of implementation technologies for the synchronization of timing (code, bit and frame synchronisation) and carrier frequency and phase estimation of a DSSS communication system employing complex spreading sequences.
- Simulation and prototype hardware performance evaluation of the DSSS system under typical AWGN and some fading mobile channel conditions, including power saturation effects.

1.3 DISSERTATION OUTLINE

Figure 1.1 contains a schematic representation of this dissertation.

The dissertation is outlined as follows:

PART I gives an overview of the DSSS communication system in Chapter 1.

A theoretical analysis is presented in *PART II* and is consisting of Chapter 2 to Chapter 6. Chapter 2 gives the theoretical background of SS systems. Chapter 3 describes the complex spreading sequences and their properties, e.g. auto and cross-correlation properties. The analysis of the DSSS transmitter is presented in Chapter 4. Both balanced QPSK and a conventional dual channel QPSK transmitter structures have been investigated, employing unique combinations of the real and imaginary parts of the complex spreading sequences. The DSSS receiver is analyzed in Chapter 5. Different receiver structures were investigated in the search for an optimum configuration for the proposed DSSS communication system, employing complex spreading sequences. The receiver structures have been designed to demodulate and despread transmitter signals corresponding to the balanced and dual-channel transmitter configurations, respectively. In Chapter 6 the synchronization of the DSSS communication system is investigated. Code acquisition, code tracking and carrier synchronization techniques for best system performance are described. Synchronization structures for code acquisition and code tracking as well as carrier tracking and data demodulation are investigated and designed by using a coherent approach for a DSSS system employing complex spreading sequences. A combined coherent Decision-Directed Costas Carrier Recovery Loop (DD-CCRL) and Coherent Decision-Directed Complex Delay-Lock-Loop (DD-CDLL) synchronization scheme for a DSSS communication system, originally proposed by De Gaudenzi for systems using binary spreading sequences, have been generalized and extended to include systems employing binary and/or complex spreading sequences. The advantages offered by this unique code locking scheme are also discussed.

PART III presents the DSSS system simulation. Simulation of the complete complex DSSS communication system, as designed and analyzed in Chapters 4, 5 and 6, were done prior to hardware implementation, in order to evaluate and verify correctness of the theoretical design. In Chapter 7 the simulation of the DSSS transmitter, employing complex spreading sequences, is done. In Chapter 8 the simulation of the receiver with all corresponding results are presented. The decision-directed complex Costas carrier recovery loop, decision-directed complex DLL as well as the acquisition circuitry are also simulated to perform a fully independent receiver structure responsible for code acquisition, carrier

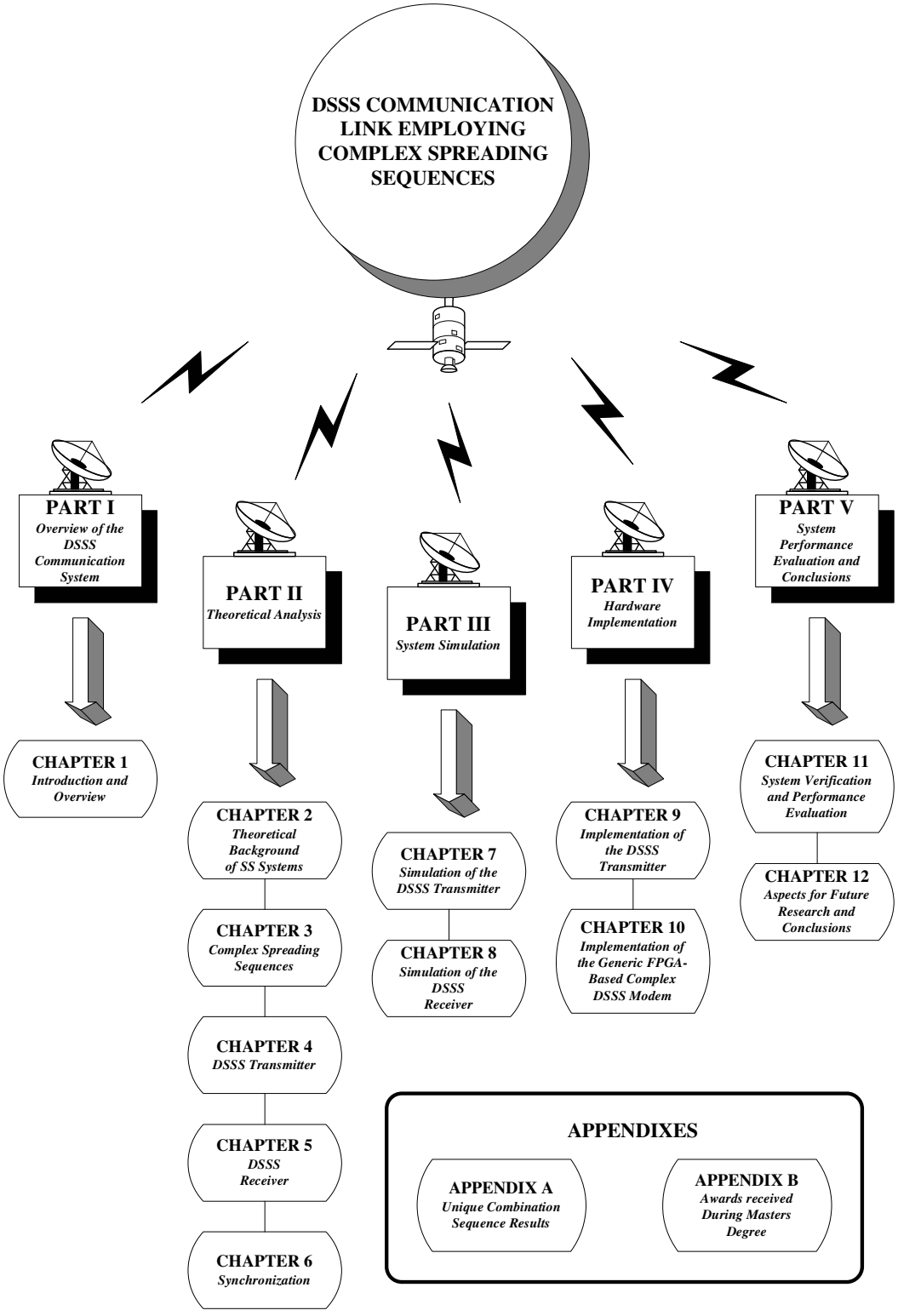

FIGURE 1.1: Schematic representation of the dissertation outline

recovery and code tracking. Results related to these loop structures are also given.

PART IV contains the hardware implementation of the DSSS system. Chapter 9 gives the design approach and hardware transmitter structures used, as well as results obtained with this transmitter module. The transmitter module was the first prototype version built to illustrate the practical implementation of complex spreading sequences. The results obtained with the hardware transmitter module correlated very well with the theory and simulations. The system was also upgraded to a more advanced version on FPGA technology and is also described in detail. In Chapter 10 the final FPGA-based complex DSSS modem is presented, which is a great improvement in terms of technology relative to the structures described in Chapter 9. In Chapter 10 the aforementioned theoretical structures and schemes were implemented in hardware by utilizing Altera's FPGA technology. IF sampling principles were applied at the receiver and implemented on FPGA using VHDL programming software, resulting in a number of advantages compared to analog down-conversion and carrier tracking. The hardware results of the complex DSSS communication system are presented in this chapter. Complete system specifications are presented, as well as a brief description of the operation of the DSSS system.

PART V gives a system performance evaluation and conclusion. Chapter 11 presents the system verification and performance evaluation. This chapter compares the system performances of the balanced and dual channel DSSS QPSK modulation configurations, employing a class of constant-envelope root-of-unity (CE-RU) filtered complex spreading sequences, with conventional Nyquist filtered QPSK modulated CDMA systems employing binary spreading sequences. A verification and performance evaluation of the balanced and dual channel DSSS QPSK system employing CSS are presented in terms of bit error rate performance, spectral and power efficiency, transmitter output peak-to-average power ratio (PAPR), etc. The comparison is also done in non-linear power amplification and is based on Complementary Cumulative Probability Density Function Peak-to-Average Power Ratio (CCDF-PAPR) measurements, as well as the amount of spectral regrowth experienced when the power amplifier is driven close to the so-called 1dB saturation point. Simulation as well as hardware results are presented to illustrate the superiority of the new complex-spreaded WCDMA modulation schemes over conventional methods in terms of spectral and power efficiency in the presence of non-linear power amplification. Chapter 12 gives the aspects for future research and concludes with the main objectives of the dissertation. In this chapter the ultimate goal of this research project is given, that was to design and develop a generic DSSS modem employing complex spreading sequences (CSS). This objective has been achieved

with the establishment of a prototype WLL RF-link, providing the required vehicle and test bed to verify and illustrate all the principles and concepts formulated, e.g., the concept of linear root-of-unity filtering and its realisation in hardware.

Appendix A and B presents the results of the unique combination sequences as well as the awards received during Masters degree, respectively.

1.4 TYPICAL APPLICATIONS OF THE PROPOSED NEW DSSS COMMUNICATION SYSTEM

The generic DSSS communication system presented in this dissertation may typically form the heart of both limited coverage ('small-area') as well as large coverage ('wide-area') applications. In a small-area application, the system may coexist with other services with minimum interference, due to its small footprint (micro- to pico-cellular, i.e., for example, in 100m radius application scenarios), exceptionally low emission power levels and the fact that DSSS is in effect a low-probability-of-intercept (LPI) concept (i.e., will cause minimum interference with co-users in the same frequency band), while it is capable of suppressing in-band interference by virtue of its inherent Spreading or Processing Gain (PG) (which may be in access of 30dB, depending on the available bandwidth).

Possible secondary small-area applications that has already been touched on in the introduction, is the application of the proposed concepts as a semi-mobile extension to existing PABX technologies, giving the latter 'fixed' services an extra mobility dimension whereby the users are allowed to roam about within a predefined coverage area (typically micro-cellular, such as would be found within a building). The same Wireless-Local-Loop (WLL) concept could naturally be applied in a host of other applications, such as in cases where temporary telecommunications must be established over a limited period of time (e.g., at conferences, sport events etc.). Another major small or wide-area application could be in remotely situated rural areas where both small and densely populated communities could be given affordable local multimedia telecommunication services (including digital speech, data and video), via standard interfaces and high capacity links (e.g., microwave, satellite link, optical fibre) to not only the PSTN, but also to existing cellular and Internet infrastructures. The development of such an affordable multimedia CDMA product is presently the topic of an NRF-supported research and development (R&D) programme. In addition, a two-dimensional application of the novel DSSS techniques presented in this dissertation, have found application in a ultra-high distance telemetry control link, which has

to date outperformed all other competing solutions in this field of application.

Moreover, an extension of the proposed new modulation technique to more than four dimensions would allow the establishment of WLAN 'last-mile' access systems, whereby customers may be offered multimedia broadband Internet access. One way to achieve the latter goal is to use techniques similar to that of WiMax, utilising a novel multi-dimensional configuration (using more than four dimensions) with interesting similarities to OFDM modulation schemes (but with significantly better power efficiency and superior performance), to realise a form of IP-based broadband WLAN service, which may render an alternative to present 2 and 3G wireless cellular services. Since the proposed multi-dimensional modulation concept may be extended to offer very high data throughput rates at practically the performance of a conventional QPSK modulation system, it may even be considered for application in fourth generation (4G) wireless cellular applications.

The proposed micro-cellular system, incorporating the generic DSSS transmitter, will not only be easy to deploy, but also relatively efficient in terms of power (i.e., battery) requirements, due to its near constant envelope (i.e., instantaneous power) output. The latter advantage will obviously have a direct impact on terminal costs, due to the reduced transmitter power requirements of the handsets, compared to for example contending existing TDMA techniques. Since the power source and high power amplifier subsystems may contribute as much as 20% of the total handset cost, significant savings may be incurred by employing the DSSS system with complex spreading proposed in this dissertation. The unique multidimensional DSSS modulation scheme offers flexible data rates within relatively small spreading bandwidths, while maintaining high processing gains - the necessary ingredients to provide for 'service-on-demand' multi-media requirements.

1.5 MAIN CONTRIBUTIONS

The advantages and applications outlined above are based on major contributions that evolved from this research and prototype hardware development, including the following:

- Unique upwards-expandable multi-dimensional transmitter and receiver configurations are proposed employing complex spreading sequences.
- Novel carrier synchronization techniques are presented, in order to overcome the presence of unwanted interference terms in the process of achieving carrier phase estimation in the presence of complex spreading.

- Similarly, dedicated code tracking loops have been proposed, designed and analyzed, capable of tracking the chip timing of the desired received DSSS signal's complex spreading code.

- The superior performance (compared to existing binary DSSS systems) of the latter synchronisation subsystems, including the complex detection process, can be attributed to using unique combinations of the real and imaginary parts of the complex spreading sequence allocated to individual users.

- The proposed new generic DSSS system is sufficiently versatile to allow the use of either binary or complex spreading sequences.

- One major contribution is the use of families of Non-Linearly-Interpolated Root-of-Unity (NLI-RU) filtered complex spreading sequences capable of producing constant-envelope Double-Side-Band (DSB), as well as Single-Side-Band (SSB) DSSS outputs. To the author's knowledge, no comparable constant-envelope results have ever before been produced for SSB modulation systems.

- Sequences (binary as well as complex) may be pre-NLI-RU-filtered before being downloaded to the DSSS transmitter. Surprisingly tightly filtered output signals can be obtained by employing the NLI-RU filtering method, requiring only mild additional bandlimiting to meet RF-mask requirements in most cases.

- NLI-RU filtered complex spreading sequences exhibit perfectly constant envelope, even with SSB modulation, giving systems employing these sequences a definite power efficiency advantage compared to non-constant envelope schemes.

- The generic DSSS transmitter is very flexible in terms of data rate, spreading sequence length and Processing Gain (PG). Not only can different multi-phase as well as multi-amplitude modulation techniques be very easily implemented, but the system may be easily adapted to serve a host of variable data rate ('service-on-demand') applications, some of which have been outlined above.

- Lastly, the above mentioned subsystems have been implemented in reprogrammable FPGA hardware, resulting in the generation of considerable intellectual property (IP) in the form of additional DSSS/CDMA VHDL functional core software.

1.5.1 List of Publications

- F.E. Marx and L.P. Linde, ”DSP implementation of a generic DSSS transmitter employing complex or binary spreading sequences”, *COMSIG’95*, pp 75-80, 16 November 1995.

- F.E. Marx and L.P. Linde, ”DSP implementation of a generic DSSS transmitter”, in *Elektron, Journal of the South African Institute of Electrical Engineers*, pp 20-22, March, 1996.

- F.E. Marx and L.P. Linde, ”Theoretical analysis and practical implementation of a balanced DSSS transmitter and receiver employing complex spreading sequences”, in *Proceedings of AFRICON’96*, pp 402-407, University of Stellenbosch, Stellenbosch, 22-24 September, 1996.

- F.E. Marx, M. Snyman, M. Drewes, R. Milton and F.M. Ragghianti, ”Measurements for digital telecoms channels”, in *Elektron, Journal of the South African Institute of Electrical Engineers*, pp 47-49, April, 1998.

- F.E. Marx and L.P. Linde, ”A combined coherent carrier recovery and decision-directed delay-lock-loop scheme for DS/SSMA communication systems employing complex spreading sequences”, in *Proceedings of the IEEE International Symposium on Spread Spectrum Techniques and Applications, ISSSTA’98*, Sun City, South Africa, September 1998.

- F.E. Marx and L.P. Linde, ”A combined coherent carrier recovery and decision-directed delay-lock-loop scheme for DS/SSMA communication systems employing complex spreading sequences”, *The Transactions of the SAIEE Special Issue: CDMA Technology Changing the face of wireless access*, Vol. 89, No. 3., pp 131-139, September 1998.

- F.E. Marx and L.P. Linde, ”Four Dimensional Modem Employing Complex Spreading Sequences”, in *Proceedings of AFRICON’99*, pp 221-226, Cape Technicon, Cape Town, September, 1999.

- F.E. Marx and L.P. Linde, ” A Novel Four Dimensional Modem for Wireless Multimedia Communications”, in *Proceedings of the IFAC Conference on Technology transfer in Developing Countries: Automation in Infrastructure Creation, IFAC DECOM - TT 2000*, pp 212-217, Pretoria, South Africa, July 2000.

- L.P. Linde, F.E. Marx and W.R. Malan, "Power and spectral efficiency of a family of constant-envelope root-of-unity filtered complex Spreading Sequences in WCDMA non-linear power amplification", in *Proceedings of AFRICON'02*, pp 395-400, George, South Africa, October, 2002.

- J.F. Pienaar, L.P. Linde and F.E. Marx, "Realization of multi-level partial response modem in reconfigurable logic", in *Proceedings of AFRICON'02*, pp 167-172, George, South Africa, October, 2002.

- L.P. Linde and F.E. Marx, "Power and spectral efficiency performance of a family of WCDMA-modulated constant envelope root-of-unity filtered complex spreading sequences in non-linear power amplification", *The Transactions of the SAIEE: Research Journal of the South African Institute of Electrical Engineers*, Vol. 94, No. 4., pp 57-67, December 2003.

1.5.2 List of Patents

- L.P. Linde and F.E. Marx, "Multi-Dimensional Spread Spectrum Modem", South African Complete Patent no. 2000/2645, 30 January 2002. (Earliest priority claimed: ZA 99/1136, dated 26-02-1999).

- L.P. Linde and F.E. Marx, "Multi-Dimensional Spread Spectrum Modem", United States Complete Patent no. 6,744,807, 1 June 2004.

1.5.3 List of Awards

- F.E. Marx and L.P. Linde, SABS design institute awards, 1996.

- F.E. Marx, Special Merit Award of the SAIIPL, 1996.

- L.P. Linde, D.J. van Wyk, B. Westra, F.E. Marx and W.H. Büttner, SABS design institute awards, 1997.

1.5.4 Potential Applications and Products

The new DSSS technology presented in this dissertation, has already found several practical and real-world applications, some of which are mentioned below.

- The generic DSSS transmitter has firstly been used by the CSIR in a channel sounding application to measure the delay-spread profile of typical wireless communication channels at different carrier frequencies. Such a wideband DSSS transmitter can be used in various similar applications, e.g. in different types of channel sounding, accurate distance and signal path delay measurements, radar applications and many more.

- As a second example, an appropriately adapted version of the wireless DSSS communication system was in fact employed in a specialised commercial application. The particular application comprised a long distance ($>$ 200 km) ultra wide-band DSSS equivalent of the prototype DSSS system, capable of meeting all the stringent requirements specified for this particular project, including low probability of interception (LPI) operation and synchronisation in the presence of adverse (sub-zero dB SNR) conditions. Since the DSSS communication link used the technology and principles presented in this dissertation, it therefore serves as a realistic test bed and confirms and verifies the analysis and evaluation results presented in this dissertation.

PART II

THEORETICAL ANALYSIS

CHAPTER TWO

FUNDAMENTAL CONCEPTS AND THEORETICAL BACKGROUND OF SPREAD-SPECTRUM SYSTEMS

2.1 INTRODUCTION

Spread-spectrum modulation was originally developed for military applications where resistance to jamming (interference) is of primary importance. However, there are civilian applications that may also benefit from the unique characteristics of spread-spectrum modulation. For example, it can be used to provide multipath rejection in a ground-based mobile radio environment. Another application is in multiple-access communication in which a number of independent users are required to share a common channel without an external synchronizing mechanism. Every user is allocated his own spreading code and coexists in a common spreading bandwidth with multiple other users. The unique properties of the spreading code make it possible to extract the transmitted data from the composite multi-user environment at the reference user's receiver. Thus, the system also provides a form of secure communication in a hostile environment such that the transmitted signal is not easily detected or recognized by unwanted listeners.

2.2 BASIC PRINCIPLES OF DSSS

In a DSSS communication system, [11], [12], [13], [14], the spectrum spreading is accomplished before transmission through the use of a spreading code that is independent of the data sequence. The same spreading code is used in the receiver (operating in synchronism with the transmitter) to despread the received signal so that the original data

may be recovered. The information-bearing signal is multiplied by a spreading code so that each information bit is divided into a number of small time increments. These small time increments are commonly referred to as chips. In this process the narrow bandwidth of the information-bearing signal is spread over a wide bandwidth with a factor L which equals the length of the spreading sequence. The two fundamental types of spread-spectrum systems are direct-sequence (DS) and frequency-hop (FH) spread-spectrum.

In order to classify as a spread-spectrum modulation technique, two criteria must be satisfied:

- The transmission bandwidth must be much larger than the information bandwidth.
- The resulting spread radio-frequency bandwidth must have no direct relation with the information signal bandwidth, i.e., it should be the result of a spreading process in which the spreading sequence or code is totally uncorrelated with the information signal.

Spread-spectrum communication techniques may be very useful in solving different communication problems. The amount of performance improvement that is achieved through the use of spread-spectrum, relative to an unspread system, is described in terms of a so-called processing gain (PG) factor. In spread-spectrum modulation an information-bearing signal is transformed into a transmission signal with a much larger bandwidth. The transformation is achieved by encoding (spreading) the information bearing signal with a spreading code signal that is independent of the data signal. This process spreads the power of the original data signal over a much broader bandwidth, resulting in a lower power spectral density than the unspread information signal. When the spectral density of the resultant SS signal starts to merge with or fall below the background noise level, the DSSS communication signal enters a state of low visibility or perception, making it hard to locate or intercept. This communication mode is commonly referred to as low probability of interception (LPI), and offers a form of security, which has previously been exploited for military applications, but are presently increasingly applied to a host of commercial applications. The PG of the spread-spectrum system can be defined as the ratio of transmission bandwidth to information bandwidth,

$$PG = \frac{B_T}{B_B} = \frac{T_b}{T_c} = \frac{R_c}{R_b} = L \tag{2.1}$$

where B_T is the transmission bandwidth, B_B the bandwidth of the information-bearing signal, T_b is one bit period of the data signal, T_c is one chip period of the spreading code, R_c

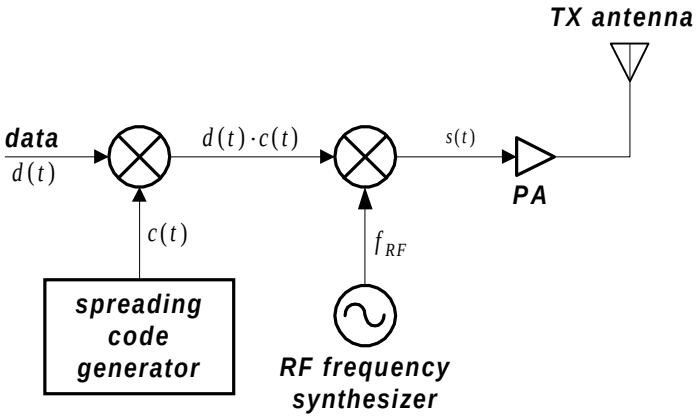

FIGURE 2.1: Conceptual block diagram of a DSSS transmitter

is the chip rate of the spreading sequence, R_b is the bit rate of the data signal and L is the length of the spreading code.

The receiver correlates the received signal with a synchronously generated replica of the spreading code signal to recover the original information-bearing signal. This implies that the receiver must know the spreading sequence or code used to spread or spread-spectrum modulate the data.

The basic spreading process in a direct sequence spread-spectrum system is illustrated in the conceptual block diagram of a DSSS transmitter in Figure 2.1. The information-bearing signal, $d(t)$, is multiplied by the spreading code, $c(t)$, and modulated onto a RF carrier frequency to obtain a final spread output signal, $s(t)$,

$$s(t) = d(t) \cdot c(t) \cdot \cos(2\pi f_{RF} t) \tag{2.2}$$

where f_{RF} is the RF carrier frequency.

The basic DSSS despreading process is shown in the conceptual block diagram of a DSSS receiver depicted in Figure 2.2. The incoming signal is received by the RF front-end, consisting of basically a noise reject bandpass filter, a LNA and a mixer to down-convert the RF signal to IF. This IF DSSS signal is despread and bandpass filtered, whereafter the despread signal is demodulated by means of a BPSK demodulator to recover the original information-bearing signal, $d(t)$. The relevant time domain signals of the spreading and despreading processes are displayed in Figure 2.3, while Figure 2.4 depicts the frequency spectra of these signals.

In the case of a high-power narrow-band interference or jamming signal, the interference

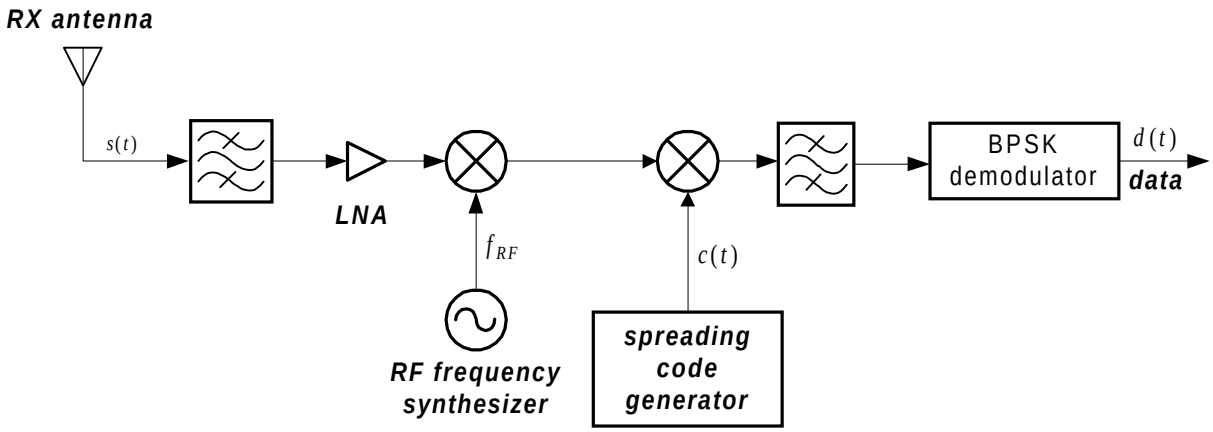

FIGURE 2.2: Conceptual block diagram of a DSSS receiver

or jamming signal is added to the spread data signal in the radio channel. In the despreading process at the receiver, the spread data signal is despread to its original narrow bandwidth and bandpass filtered to the double sideband information bandwidth, while the interference or jammer signal is spread by a factor equal to the spreading sequence length L, resulting in a low density wideband interference signal. Since only a portion of this low-density interference or jammer signal may fall within the actual information band after despreading, the interference power will be significantly reduced compared to the original full-power interference case.

Below are a number of alternative ways whereby spread-spectrum signals may be generated, namely:

- Direct-sequence spread-spectrum.
  The information-bearing signal is multiplied directly by a fast spreading code signal.
- Frequency hopping spread-spectrum.
  The carrier frequency at which the information-bearing signal is transmitted is rapidly changed according to the spreading code signal.
- Time hopping spread-spectrum.
  The information-bearing signal is not transmitted continuously. Instead the signal is transmitted in short bursts where the times of the bursts are decided by the spreading code signal.
- Chirp modulation.

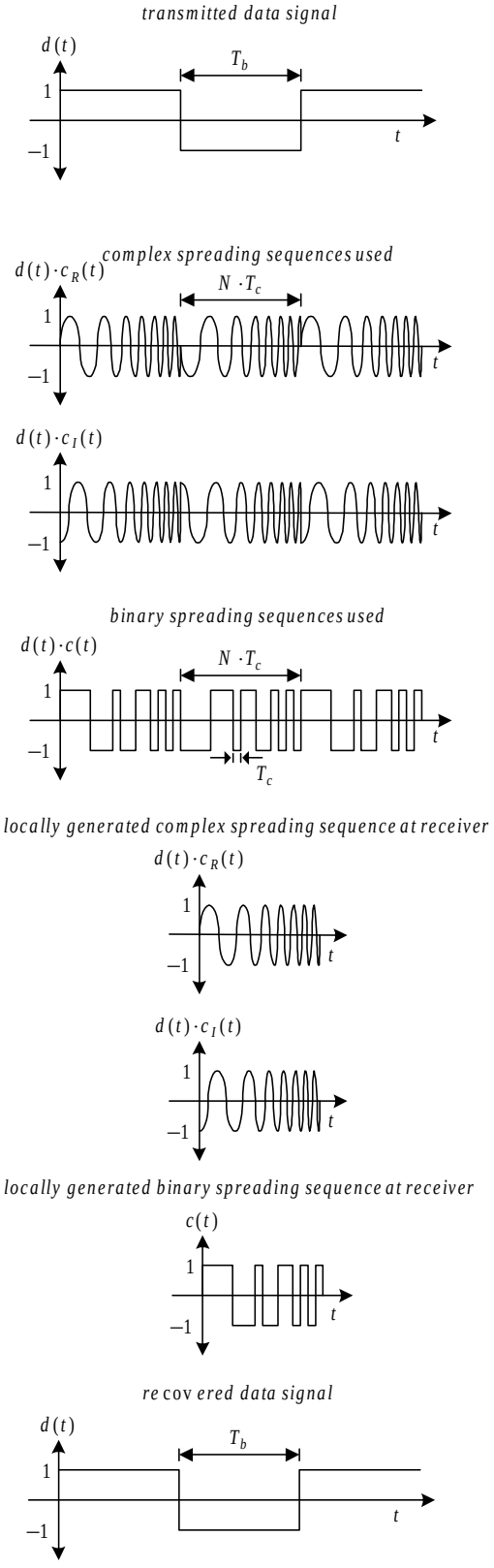

FIGURE 2.3: Signals in the time domain demonstrating the spreading-despreading process

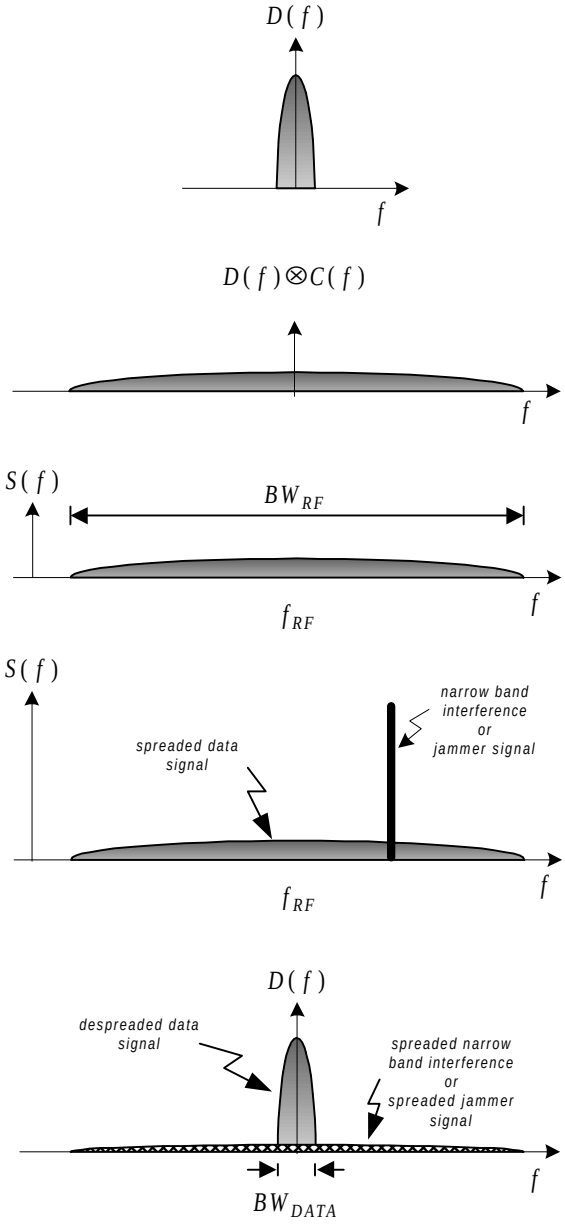

FIGURE 2.4: Signals in the frequency domain demonstrating the spreading-despreading process

This kind of spread-spectrum modulation is almost exclusively used in military radars. The radar continuously transmits a low power signal whose frequency is linearly varied (swept) over a wide range.

- Hybrid modulation.
  By combining two or more of the above mentioned spread-spectrum modulation techniques the advantages of both of the constituent techniques may be gained, and possible disadvantages may be overcome.

2.3 WHY SPREAD SPECTRUM ?

2.3.1 Advantages of DSSS

- Enhanced security and privacy in communications:
  The transmitted signal can only be despread and the data recovered if the spreading code is known to the receiver.

- Protection against multipath interference:
  In a radio channel there are more than one path between a transmitter and receiver. Due to reflections and refractions a signal will be received from a number of different paths. The signals of the different paths are all copies of the transmitted signal but with different amplitudes and phases. Adding these signals at the receiver will be constructive at some frequencies and destructive at others. In the time domain, this results in a dispersed signal. Spread-spectrum modulation combats this multipath interference and may in fact resolve it if the differential multipath delays are larger than the chip period. In such a case multipath diversity may be exploited by employing maximal ratio combining techniques such as provided by so-called RAKE receiver mechanisms.

- Low probability of intercept (LPI):
  Spread spectrum complicates the signal detection problem of a surveillance receiver by virtue of a larger frequency band to be monitored as well as a lower power spectral density of the signal to be detected in the spectrum-spreading process.

- Interference rejection and immunity:
  Cross-correlating the code signal with a narrowband signal will spread the power of the narrowband signal thereby reducing the interfering power in the information

bandwidth. This is illustrated in Figure 2.4, where it is assumed that narrowband interference is intensionally or non-intensionally added to the spread-spectrum signal during transmission. At the receiver the spread-spectrum signal is despread while the interference signal is spread, making it appear as background noise compared to the despread information signal. The overall effect is to gain a processing advantage for the DSSS-modulated information signal with respect to the narrowband interfering signal, making the DSSS signal more immune to interference.

- Low power density spectra:
  The power of the data information signal is spread over the total available spreading bandwidth of the DSSS communication system during the spreading process. This results in a much lower power spectral density compared to the corresponding narrowband modulation case, offering the advantage of low probability of detection and interception.

- High resolution ranging:
  In radar applications, ranging resolution is determined by the code rate (chip length) and code length (number of chips per code). The code repetition rate and length also determine the maximum unambiguous range. Ranging has been the most prominent and certainly the best known use of spread spectrum systems. Position location systems, such as for example the Global Positioning System (GPS), uses spread-spectrum principles to provide services such as vehicle location and tracking.

- Code division multiplexing for code division multiple access applications:
  If multiple users transmit a spread-spectrum signal at the same time in the same frequency band, the receiver will still be able to distinguish between the users provided each user has a unique spreading code with sufficiently low cross-correlation with other spreading codes. Correlating the received signal with a spreading code signal from a certain user will then only despread the signal of that user, while the other spread-spectrum signals will remain spread over a large bandwidth. Thus, within the information bandwidth, the power of the desired user will be much larger than the interfering power of the other users (interferers), provided that there are not too many simultaneous users, allowing the desired signal to be recovered (despread and extracted) with a minimum specified quality of service (QoS). It is exactly this interference rejection ability of a spread-spectrum system that facilitates multiple access services, i.e., co-existence of multiple users in the same communication band

and thus, efficient sharing of limited spectrum resources. For this reason, this synchronous form of spectrum sharing is often called spread-spectrum multiple-access (SSMA) or code-division multiple-access (CDMA), [15].

- Elimination of frequency planning in SS CDMA:
  The basic principle of cellular telecommunications is the ability to reuse available channel frequencies over a particular geographical area. In analog and TDMA-based systems every frequency cannot be reused in every cell, because such practice would cause unmanageable interference. The available frequencies must be utilised according to a well planned frequency reuse scheme over a number of cells and carefully coordinated to avoid interference with each other. In a CDMA system, all the users on a certain carrier share the same RF spectrum. The same RF carrier frequency is used in every cell site and in every sector of a sectorized cell site, resulting in a universal frequency reuse pattern. It is this unique universal frequency reuse strategy that gives CDMA its very large capacity increase over analog and TDMA-based technologies and eliminates the need for frequency planning.

- Improves spectral efficiency and capacity:
  CDMA provides larger spectral efficiency and system capacity than analog and TDMA-based systems, [16], by virtue of a larger channel/carrier reuse factor per coverage area. The universal frequency reuse strategy of CDMA has allowed mobile systems to achieve up to 20 times more capacity than first generation (1G) analog systems (FM/FDMA), and 4 to 6 times capacity increase over existing second generation (2G) digital TDMA or FDMA systems, [17].

- Voice activity detection:
  Voice activity detection , [15], is another variable which helps to increase the capacity of a CDMA system. CDMA takes advantage of voice activity gain through its use of variable rate vocoders. The principle behind the variable rate vocoder is to have it run at high speed, providing the best speech quality, only when voice activity is detected. When no voice activity is detected, the vocoder will drop its encoding rate. The variable rate vocoder uses up channel capacity only as needed. Since the level of interference created by all of the users directly determines system capacity, CDMA network capacity is maximized because the voice activity detection reduces the noise level in the system. In a typical phone conversation, a person is actively talking only about 35% of the time. The other 65% is spent listening to the other party, or is spent

in silence when neither party is speaking. This implies that system capacity could be increased by 65% using voice activity detection.

2.4 CAPACITY OF A CDMA SYSTEM

In a CDMA communication system, the capacity is interference limited, while it is bandwidth limited in FDMA and TDMA systems. Thus, the capacity of a CDMA system, [18], [17], [19], [13], [14], [11], will increase with a reduction of interference. As the number of users decrease, the interference level decreases and the link performance for each user increases. TDMA is a time-dimension-limited system in which there can be no additional users when all the time slots have been assigned. As the number of users increase, there is no interference caused by one mobile radio to the reception of another mobile radio at the cell cite. The number of users will increase until the number of time slots is exhausted. There after it is not possible to increase the number of users. Spread spectrum communication systems can tolerate some interference and the introduction of each additional active user raises the overall level of total interference to the base station receivers. The number of CDMA channels allowed in a star network depends on the total level of interference that can be tolerated by the CDMA system. Based on the fact that the CDMA system is limited by interference, spread spectrum CDMA systems place a greater premium on good overall mobile radio and system design than conventional narrowband FDMA and TDMA multiple-access radio systems.

Given the following assumptions for a digital cellular CDMA communication system:

- Power control is employed such that all uplink (mobile-to-base station) signals at the cell site are received with the same signal power level.
- All users are spread over the same total available bandwidth B_T.
- The interference between radios is modelled as Gaussian noise.
- Each user has a required bit error probability that defines a required E_b/N_o.
- A cell has a total number of M users.

For a single cell site with power control, all reverse link signals are received with the same power level. Thus composite uplink received signal at the base site will consist of the desired signal with power P_S and $M-1$ interfering users, each also of power P_S. The signal-to-noise (interference) power ratio can be written as

$$SNR = \frac{P_S}{(M-1)P_S} = \frac{1}{M-1} \tag{2.3}$$

The bit energy-to-noise density ratio is obtained by dividing the signal power P_S by the information bit rate, R_b, and dividing the noise (interference) by the total spreading bandwidth or transmission bandwidth, B_T. Thus the bit energy-to-noise density ratio is

$$E_b/N_o = \frac{P_S/R_b}{(M-1)P_S/B_T} = \frac{B_T/R_b}{M-1} = \frac{PG}{M-1} \tag{2.4}$$

By solving 2.4 for M, the capacity of the cell in terms of channels/transmission bandwidth B_T is found, given by

$$M = 1 + \frac{PG}{E_b/N_o} \cong \frac{PG}{E_b/N_o} \tag{2.5}$$

for M large, and with the assumption that each interferer is transmitting continuously.

The required E_b/No depends on how much error correction coding is used and how well the radio is designed, for a given bit error probability. According to Shannon's limit in AWGN, error free communication is possible for

$$E_b/N_o = ln2 = 0.69 = -1.59dB \tag{2.6}$$

and thus for this Shannon limit

$$M = 1.44 \times PG. \tag{2.7}$$

Spread spectrum systems can have more users per cell than traditional systems, which are limited by the number of dimensions, such as available frequency bands (FDMA) or time slots (TDMA). With practical CDMA systems, it may be difficult to accommodate this many users in a single cell, but TDMA and FDMA systems, however, use only up to 20 percent of this theoretical capacity to ensure the practical isolation between non-interfering channels.

The interference at the base station will come from both within a cell, as well as from outside the cell. The interference coming from outside the cell can be accounted for by a factor f, and then Equation 2.5 becomes

$$M = \frac{PG}{E_b/N_o} f \tag{2.8}$$

The capacity of a CDMA system can be extended by lowering the level of interference. There are several methods of decreasing the interference level in a CDMA communication system, i.e., voice activity and data applications, [20], antenna sectorisation, frequency reuse, power control and multibeam antennas.

CHAPTER THREE

COMPLEX SPREADING SEQUENCES

3.1 INTRODUCTION

In a CDMA system the capacity is limited by the amount of MUI present. Every user in the CDMA system uses it's own unique spreading sequence. At the receiver the user performs a correlation between the received signal and his spreading sequence, stored or generated at the receiver. The received signal consists of the sum of the spreading sequence of the reference user and the spreading sequences of all other users. During the despreading process in the receiver, both an **A**uto-**C**orrelation (AC) and a **C**ross-**C**orrelation (CC) function are performed. The value of the CC is not necessarily zero and therefore the spreading sequences of the other users generate noise in the process of signal detection. This noise is known as multi-user-interference (MUI) and is directly proportional to the number of users in the CDMA system.

Thus, the spreading sequences used in a CDMA system must have certain correlation properties to ensure a large capacity and high performance of the system. Two of the most important properties of spreading sequences are their AC and CC characteristics. The AC function must have a high peak at zero-shift, while the off-peak values of the AC and all the values of the CC functions have to be very small. For the ideal case these off-peak AC values and the CC values must be zero. These properties are summarized in equation 7.5.16, p733 in [21], and will be used to evaluate the sequences described below.

In [22] a complete performance analysis of direct sequence spread-spectrum multiple-access (DS/SSMA) communications with deterministic complex (non-binary and polyphase) signature sequences has been done. The probability of bit error (PBE)

performance of different types of complex sequences is compared to that of Gold sequences. In the calculation of the PBE the computational upper and lower bounding technique and the Gaussian approximation method have been used. The general outcome of the analysis was that both the correlation characteristics and the performance of the complex spreading sequences are better than that of binary Gold sequences.

The maximum value of the out-of-phase periodic auto correlation and periodic cross correlation C_{max} functions has been derived by [23] and [24] for families of spreading sequences of size M, sequence length L, and is given by

$$C_{max} = \begin{cases} \sqrt{2(L+1)}+1, & Goldsequences, L = 2^r - 1, rodd \\ \sqrt{L+\sqrt{2(L+1)}+2}, & nearoptimal4\phi sequences, L = 2^r - 1, rodd \\ \sqrt{L}, & FZCsequences, Loddprime \end{cases} \quad (3.1)$$

Zadoff-Chu complex spreading sequences have the best possible periodic correlations when the sequence length L is an odd prime.

3.2 SPREADING CODES

The complex spreading sequences used in this dissertation are derived from the family of **Z**adoff-**C**hu (ZC) sequences [9], which is a sub-class of the **G**eneral-**C**hirp-**L**ike (GCL) sequences. The rth ZC sequence is defined by

$$a(r,k) = \begin{cases} W_L^{\frac{k^2}{2}+qk} & ; Leven \\ W_L^{\frac{k(k+1)}{2}+qk} & ; Lodd \end{cases} \quad (3.2)$$

here W_L denotes a complex Lth root-of-unity, defined as

$$W_L = e^{-j\frac{2\pi r}{L}} \quad (3.3)$$

where $j = \sqrt{-1}$, r is any integer relatively prime to L, $k = 0, 1, 2, \ldots, L-1$, denoting the primary values of the sequence, and q is any integer. The family size equals $N = m - 1$ of length $L = m^2$. The real and imaginary parts of a typically eight times over-sampled sequence, with $r = 1$ and $L = 121$, is illustrated in Figure 3.1.

For an odd value of m, the unfiltered sequence exhibit perfect periodic CC properties, i.e., the peak AC values and the peak secondary AC values fall below the so-called Welch bound, which is commonly used as a figure of merit in the evaluation of correlation properties of families of spreading sequences.

To prevent spectral overlap in a communication system it is necessary to filter these spreading sequences. The filtering process must be chosen in such a way that the correlation characteristics of the spreading signal are not adversely affected. The ZC sequences consist only of the samples generated by Equation 3.2 and the values interpolated by the filtering process do not form part of the spreading sequence. Thus, the absolute phase difference between successive samples is not very important and any values can be chosen as interpolation values, as long as the primary values of the original ZC sequence do not change. The value of the absolute phase difference between successive samples can be reduced modulo π, and the resulting phase difference can then be linearly interpolated on the unit circle. All the samples are taken from the unit circle and the filtered sequence thus have a constant envelope. This filtering technique is described in detail in [25].

The double sided bandwidth of the filtered ZC spreading sequence, for all the possible values of r, can be calculated as

$$BW = \frac{f_{sample}}{samples\ per\ chip}\ [Hz] \tag{3.4}$$

The real and imaginary parts of the root-of-unity filtered complex spreading sequence 1 and 6 of length, $L = 121$, and samples per chip, $spc = 8$, are depicted in Figures 3.1 and 3.4, while the real vs. imaginary parts of sequence 1 and 6 are shown in Figures 3.2 and 3.5, respectively. The power spectral densities (PSD) for sequence 1 and sequence 6 are shown in Figures 3.3 and 3.6, respectively.

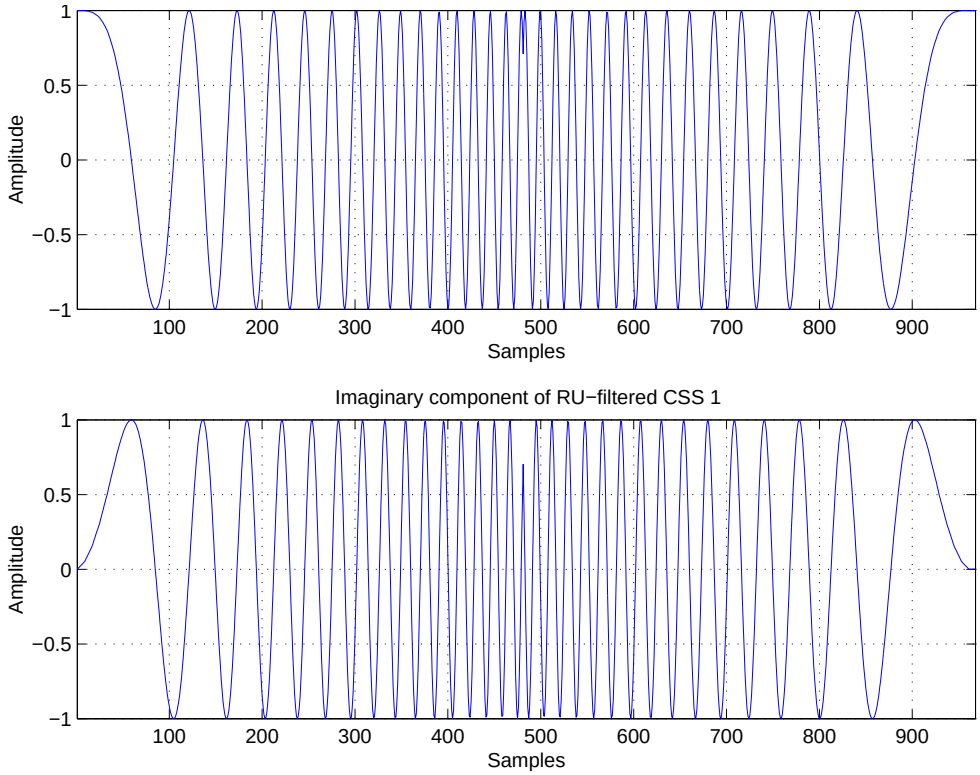

FIGURE 3.1: The Real, (a), and Imaginary, (b), part of complex spreading sequence 1. $(L = 121, RU filtered, spc = 8)$

3.2.1 Correlation Bounds

Sets of periodic sequences with good correlation properties are required for a variety of engineering applications, and much effort has been spent on design techniques for such sequences. It can be observed generally that if the set of sequences has good AC properties, then the CC properties are not very good. On the other hand, if the set of sequences has good CC properties, then the AC properties are not very good. A compromise has therefore to be made between the AC and CC properties of a particular family of spreading sequences for a specific application.

There is considerable literature on singular signals with good AC function, but little on sets of signals with good CC [26]. A lower bound to the maximum CC value for a family of complex spreading sequences was first derived by Welch [26]. Around the same time, Sidelnikov [27] derived a lower bound on the maximum value of CC of such sequences. Both Welch and Sidelnikov bounds have since been used extensively in the design and analysis of sequences for CDMA [26], [28], [29], [30], [31] and [32]. The criteria for DS-SSMA signal design are the minimization of the absolute value of the periodic and aperiodic cross-correlation (CC) between the signals. This criteria for sequence selection

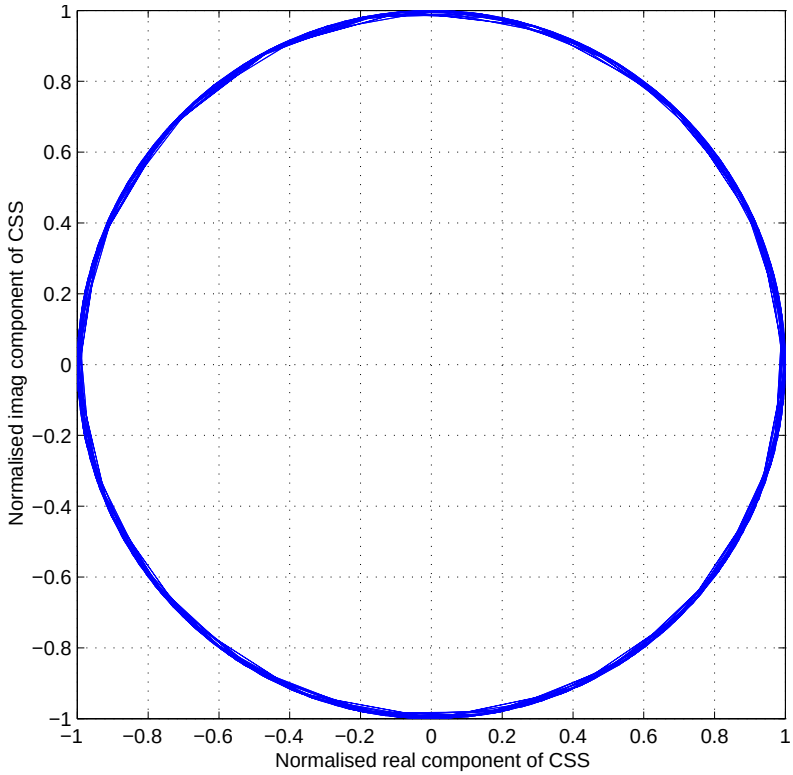

FIGURE 3.2: Real vs. Imaginary part of complex spreading sequence 1. $(L = 121, RU filtered, spc = 8)$

may not correspond to any DS-SSMA network performance measure, but it can be argued that a signal set which optimizes the network performance has to have small periodic and aperiodic CC values for all relative sequence shifts. The rule is to find good signals among the signal sets with small values of periodic and aperiodic CC.

The Welch's and Sidelnikov's lower bounds have been used as a benchmark for testing the merit of complex valued sequences. In general Welch's bound applies to complex vectors in general with no constraints on their sequence elements, whereas Sidelnikov's bound applies only to complex root of unity sequences with constant envelope [33].

3.2.1.1 The Welch Bound

The Welch bound [26] (normalised with respect to L) for the periodic case is defined as

$$\theta_{p(max)} \geq \sqrt{\frac{N-1}{L \cdot N - 1}} \tag{3.5}$$

It can be seen that for large L and a fixed value of N, Equation 3.5, becomes

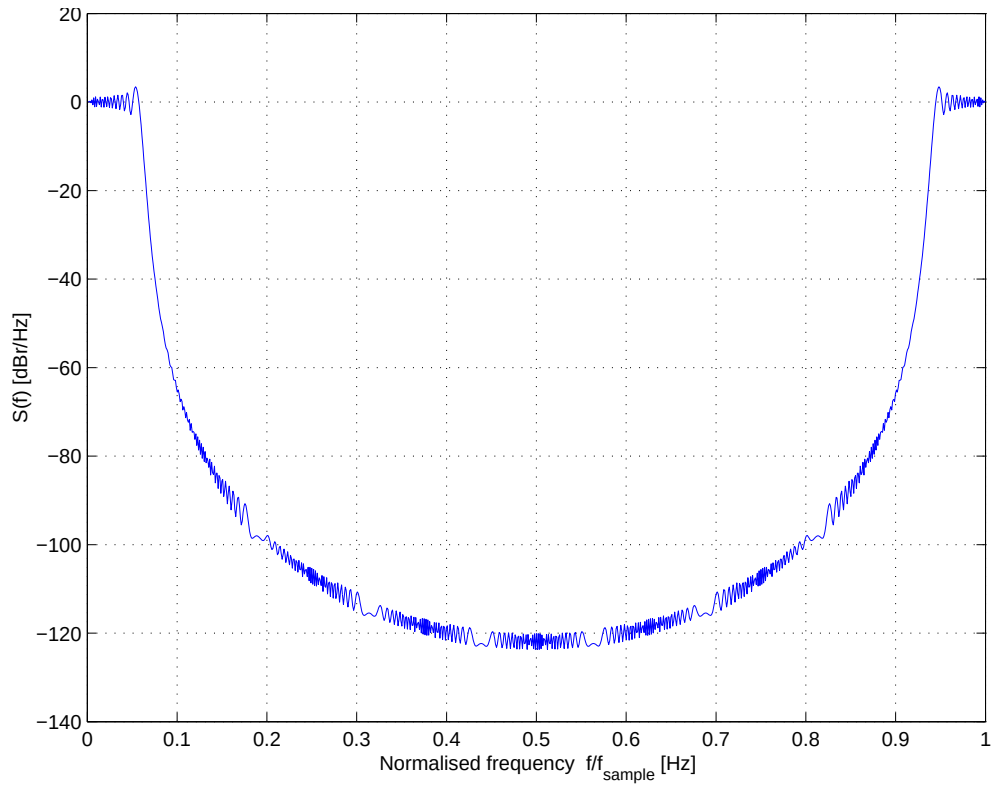

FIGURE 3.3: Power spectral density (PSD) of complex spreading sequence 1. $(L = 121, RU filtered, spc = 8)$

$$\theta_{p(max)} = \frac{1}{\sqrt{L}} \tag{3.6}$$

whereas the aperiodic case (normalised with respect to L) is given as

$$\theta_{a(max)} \geq \sqrt{\frac{N-1}{N(2L-1)-1}} \tag{3.7}$$

where N and L denote family size and sequence length, respectively.

3.2.1.2 The Sidelnikov Bound

The Sidelnikov bound (normalised with respect to L) states that for any $N \geq L$

$$\theta_{p(max)} > \frac{\sqrt{2 \cdot L - 2}}{L} \tag{3.8}$$

According to [31], Welch's bound is tighter than Sidelnikov's bound by the factor of $\sqrt{2}$, for large family sizes N. In recent years several researchers have tried to improve on the Welch's and Sidelnikov's bounds [30] and [32]. Since large family sizes are needed for CDMA applications, the work reported is mainly concentrated on improving Welch's and

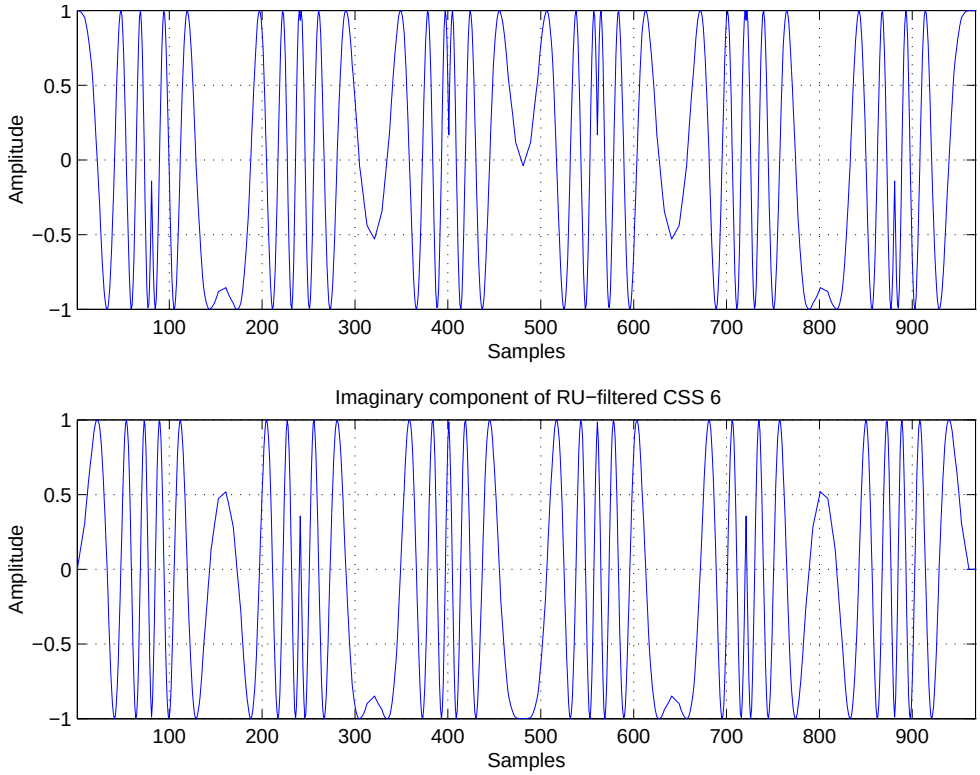

FIGURE 3.4: The Real, (a), and Imaginary, (b), part of complex spreading sequence 6. $(L = 121, RU filtered, spc = 8)$

Sidelnikov's bound for the case when N is larger than L. It is not possible to achieve N greater than L for the complex GCL sequences under consideration, with the exception of Quadri-phase sequences. Therefore, the comparison will be made on the basis of Welch's bound, which is usually treated as a lower bound on the maximum correlation values., i.e., it is considered to be a fundamental bound on the sum of the squares of the magnitudes of the inner products between the codes.

The bounds described above do not allow the design of correlation value and N independently. They rather dictate the limits within which all the code designs must lie. Since the design margin is very restrictive, the implication of these bounds for CDMA system designers is that it might be difficult to achieve new families of spreading sequences with large family sizes with good correlation properties [33].

In [23], it has been shown that the maximum magnitude of the periodic auto correlation (PAC) and periodic cross correlation (PCC) functions are related through an inequality, providing the lower bound on the maxima if the value of the other is specified.

$$\left\{\frac{\theta_c^2}{L}\right\} + \frac{L-1}{L(N-1)} \cdot \left\{\frac{\theta_a^2}{L}\right\} \geq 1 \tag{3.9}$$

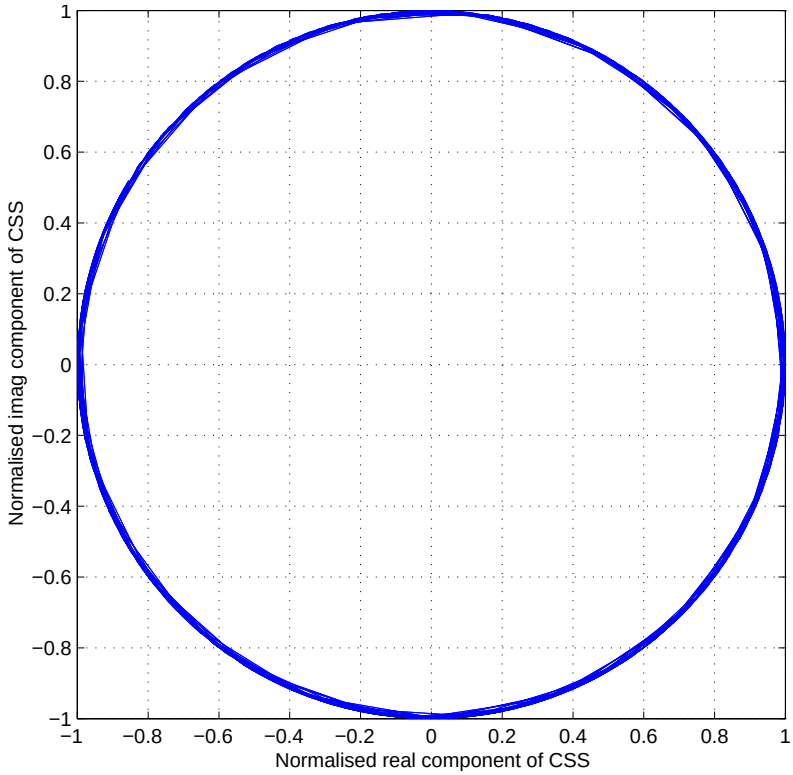

FIGURE 3.5: Real vs. Imaginary part of complex spreading sequence 6. $(L = 121, RU filtered, spc = 8)$

where L is the sequence length, N the family size, θ_a the maximum periodic AC peak and θ_c the maximum periodic CC peak.

When we substitute the maximum magnitude of the PAC, i.e., $\theta_a = 0$ in Equation 3.9, the lower bound for the maximum magnitude of the PCC is given by $\frac{1}{\sqrt{L}}$, which corresponds to Welch's bound, i.e., Equation 3.6.

Similarly maximum AAC and ACC function magnitudes are related through an inequality providing the lower bound on the maxima if the value of the other is specified

$$\frac{2L-1}{L}\left(\frac{C_c^2}{L}\right) + \frac{2(L-1)}{L(N-1)} \cdot \left(\frac{C_a^2}{L}\right) \geq 1 \tag{3.10}$$

where L again denotes the sequence length and N the family size, C_a the maximum secondary aperiodic AC peak and C_c the maximum aperiodic CC peak.

It has been shown in [23] that the lower bound on C_c, if C_a is given, is

$$\frac{C_{max}^2}{L^2} = max\left\{\frac{C_a^2}{L^2}, \frac{C_c^2}{L^2}\right\} \geq \frac{N-1}{2LN-N-1} \tag{3.11}$$

which is a result due to Welch [26], i.e., Equation 3.7.

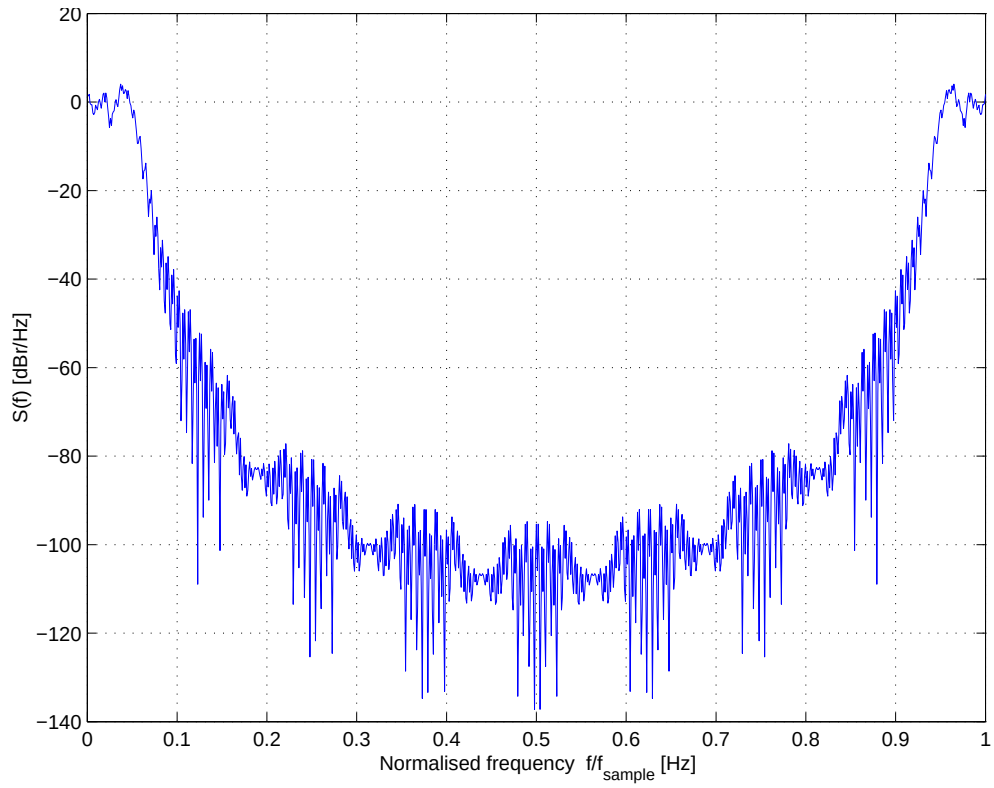

FIGURE 3.6: Power spectral density (PSD) of complex spreading sequence 6. $(L = 121, RU filtered, spc = 8)$

3.2.2 Autocorrelation Function

The sequence $\{s_k\}$ of length L has periodic AC function, $R_{ss}[l]$, given as

$$R_{ss}[l] = \sum_{k=0}^{L-1} s[k] \cdot s^*[k+l]_{mod\,L} \tag{3.12}$$

where * denotes the complex conjugate, the index $[k+l]$ is computed modulo L, and the time shift is l.

Thus for the ZC sequences, the periodic AC function is

$$R_{ss}[l] = \sum_{k=0}^{L-1} W_L^{\frac{k(k+1)}{2}} \cdot W_L^{\frac{-(k+l)_{mod\,L}\,((k+l)_{mod\,L}+1)}{2}} \tag{3.13}$$

for $q = 0$ and L odd.

The periodic AC functions for the ZC sequences 1 and 6, for a length of 121, can be seen in Figures 3.7, 3.8 and Figures 3.9, 3.10, respectively.

For a sequence s_k of length L the aperiodic AC function is defined as

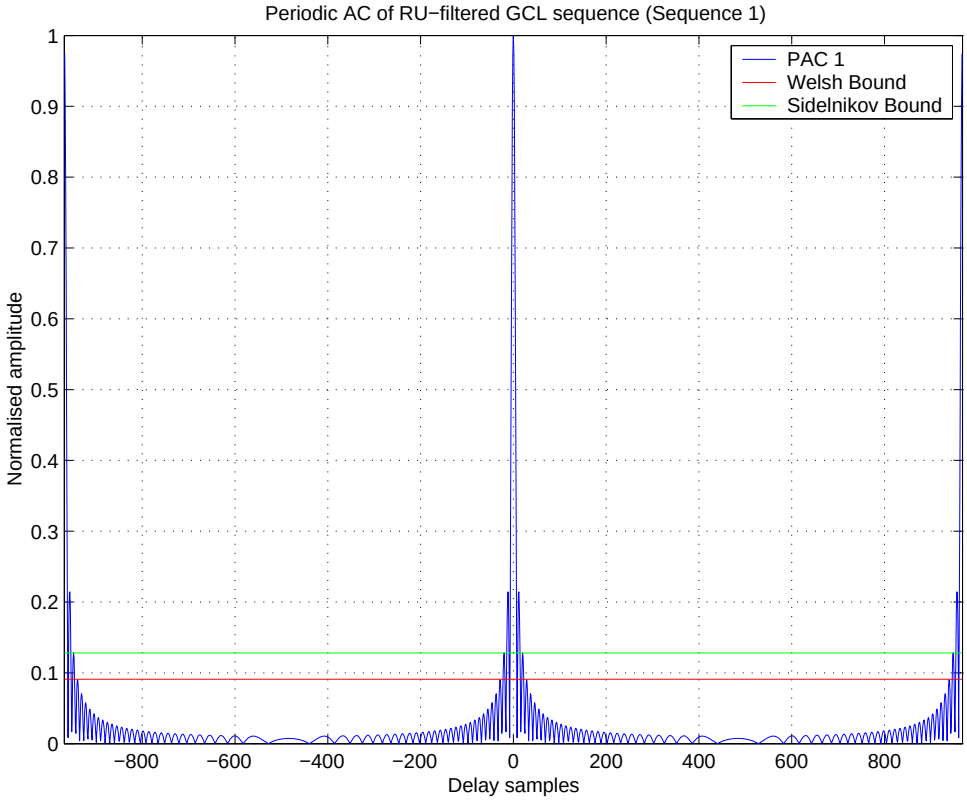

FIGURE 3.7: Periodic Auto Correlation (PAC) function of complex spreading sequence 1. $(L = 121, RUfiltered, spc = 8)$

$$R_{ss}[l] = \int_{-\infty}^{\infty} s[l] \cdot s^*[t+l]\, dl \tag{3.14}$$

where * denotes the complex conjugate and the time shift is l.

In discrete time notation the aperiodic AC function can be expressed as

$$R_{ss}[l] = \begin{cases} \sum_{k=0}^{L-1-l} s[l] \cdot s^*[k+l] & ;0 \leq l \leq L-1 \\ \sum_{k=0}^{L-1+l} s[k-l] \cdot s^*[k] & ;1-L \leq l < 0 \\ 0 & ;\mid l \mid \geq L \end{cases} \tag{3.15}$$

For ZC sequences the aperiodic AC function is

$$R_{aa}[l] = \begin{cases} \sum_{k=0}^{L-1-l} W_L^{\frac{k(k+1)}{2}} \cdot W_L^{\frac{-(k+1)(k+l+1)}{2}} & ;0 \leq l \leq L-1 \\ \sum_{k=0}^{L-1+l} W_L^{\frac{(k-l)(k-l+1)}{2}} \cdot W_L^{\frac{-k(k+l)}{2}} & ;1-L \leq l < 0 \\ 0 & ;\mid l \mid \geq L \end{cases} \tag{3.16}$$

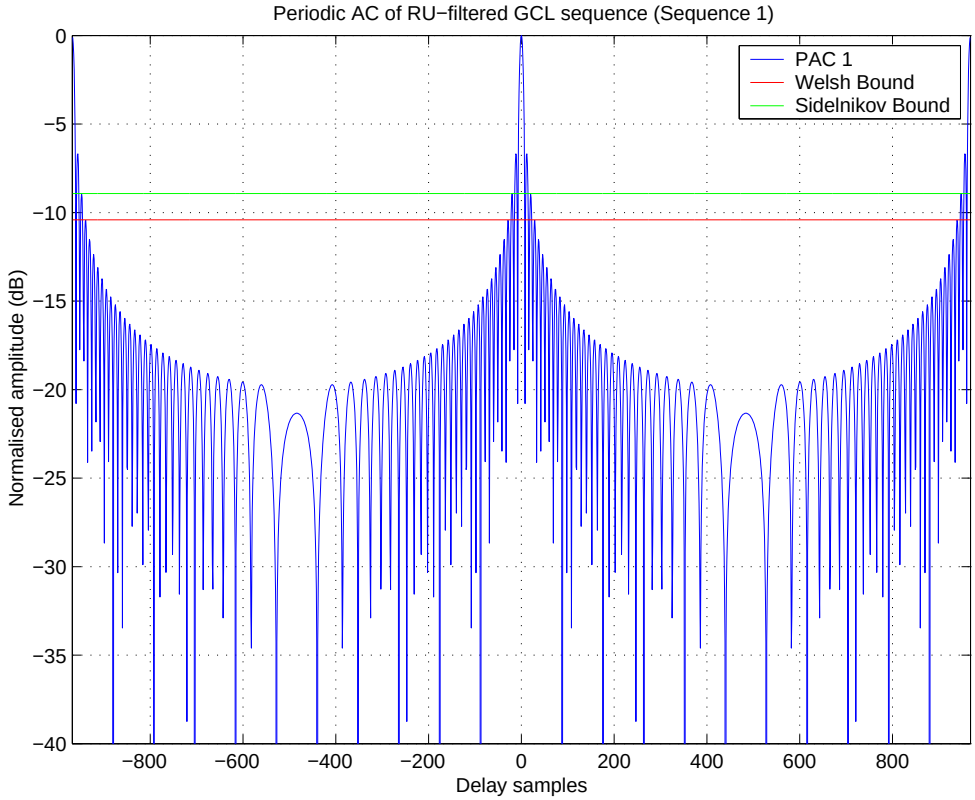

FIGURE 3.8: Periodic Auto Correlation (PAC) function of complex spreading sequence 1 in decibels. $(L = 121, RU filtered, spc = 8)$

for $q = 0$ and L odd.

The aperiodic AC functions for the ZC sequences 1 and 6, for a length of 121, can be seen in Figures 3.11, 3.12 and Figures 3.13, 3.14, respectively.

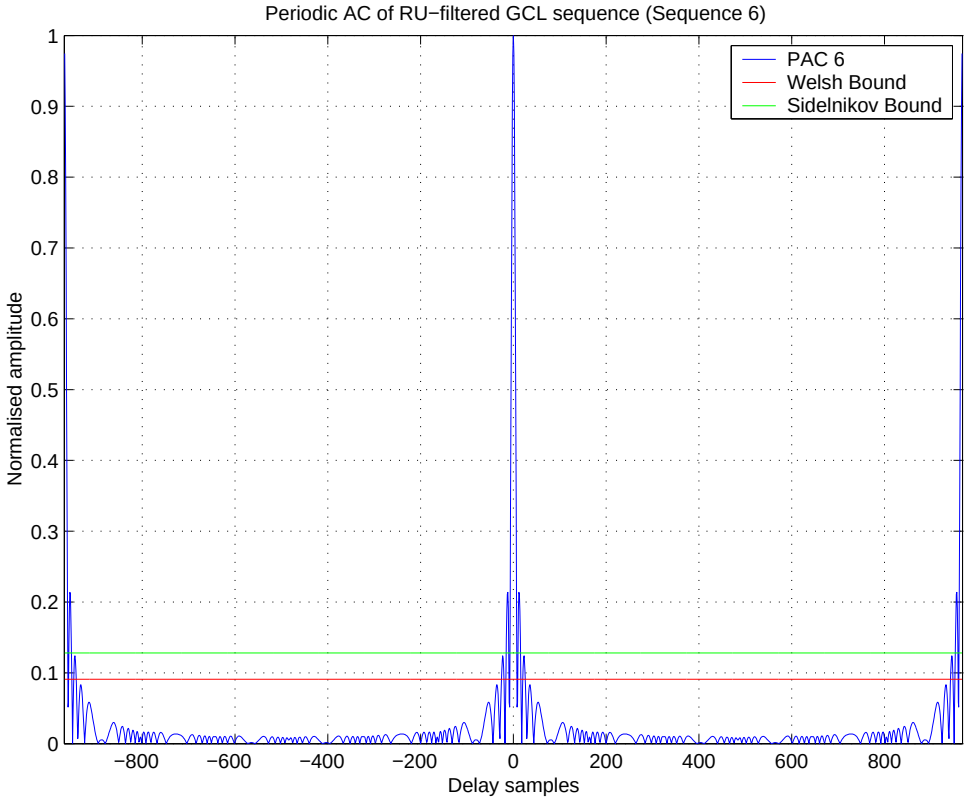

FIGURE 3.9: Periodic Auto Correlation (PAC) function of complex spreading sequence 6. $(L = 121, RUfiltered, spc = 8)$

3.2.3 Cross Correlation Function

The CC function shows the correspondence between two signals at different time shifts. The periodic CC function between any two sequences s_k and u_k, both of length L, is defined as

$$R_{su}[l] = \sum_{k=0}^{L-1} s[k] \cdot u^*[(k+l)_{modL}] \tag{3.17}$$

where $*$ denotes the complex conjugate, the index $(k + l)$ is computed modulo L, and the time shift is l.

Thus for the ZC sequence the periodic CC function is

$$R_{ab}[l] = \sum_{k=0}^{L-1} W_{L_a}^{\frac{k(k+1)}{2}} \cdot W_{L_a}^{\frac{-(k+l)_{modL}((k+l)_{modL}+1)}{2}} \tag{3.18}$$

for $q = 0$ and L odd.

The periodic cross correlation functions between spreading code number 1 and 6 are shown in Figures 3.15 and 3.16.

The aperiodic CC function between any two sequences s_k and u_k, both of length L, in discrete time notation is defined as

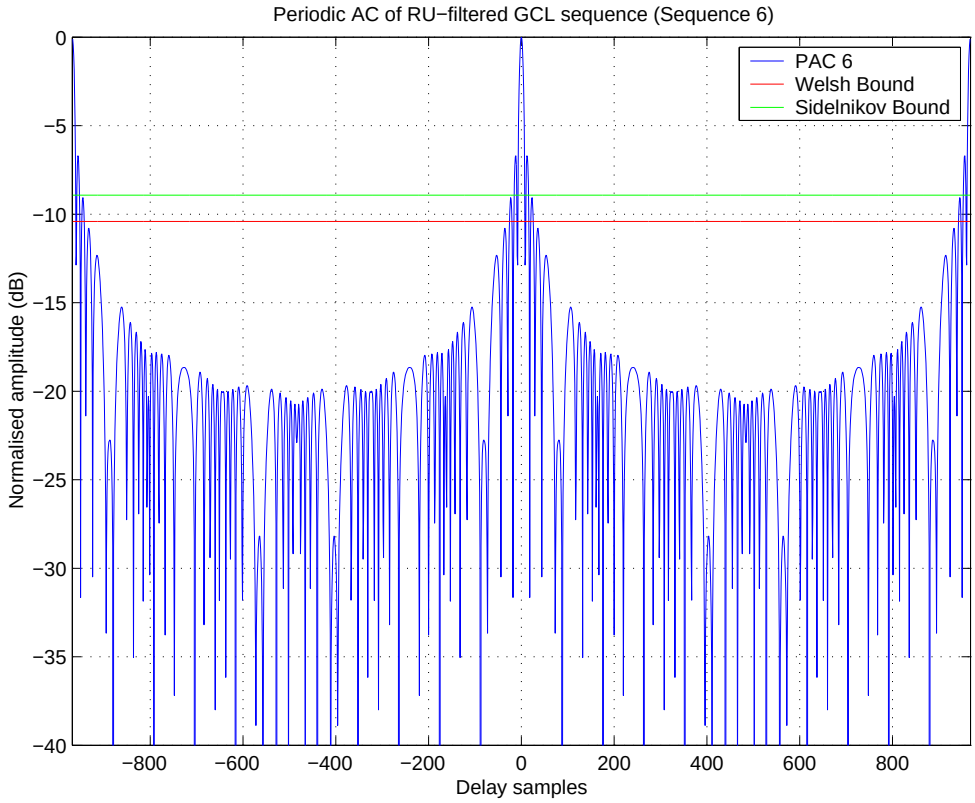

FIGURE 3.10: Periodic Auto Correlation (PAC) function of complex spreading sequence 6 in decibels. $(L = 121, RU\,filtered, spc = 8)$

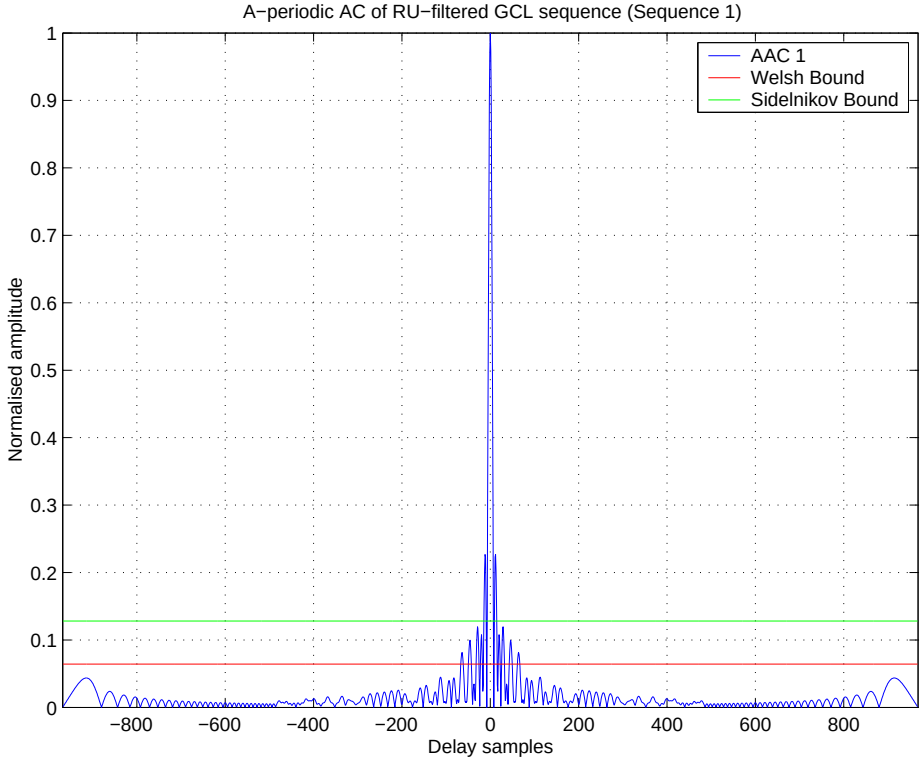

FIGURE 3.11: Aperiodic Auto Correlation (AAC) function of complex spreading sequence 1. $(L = 121, RU\,filtered, spc = 8)$

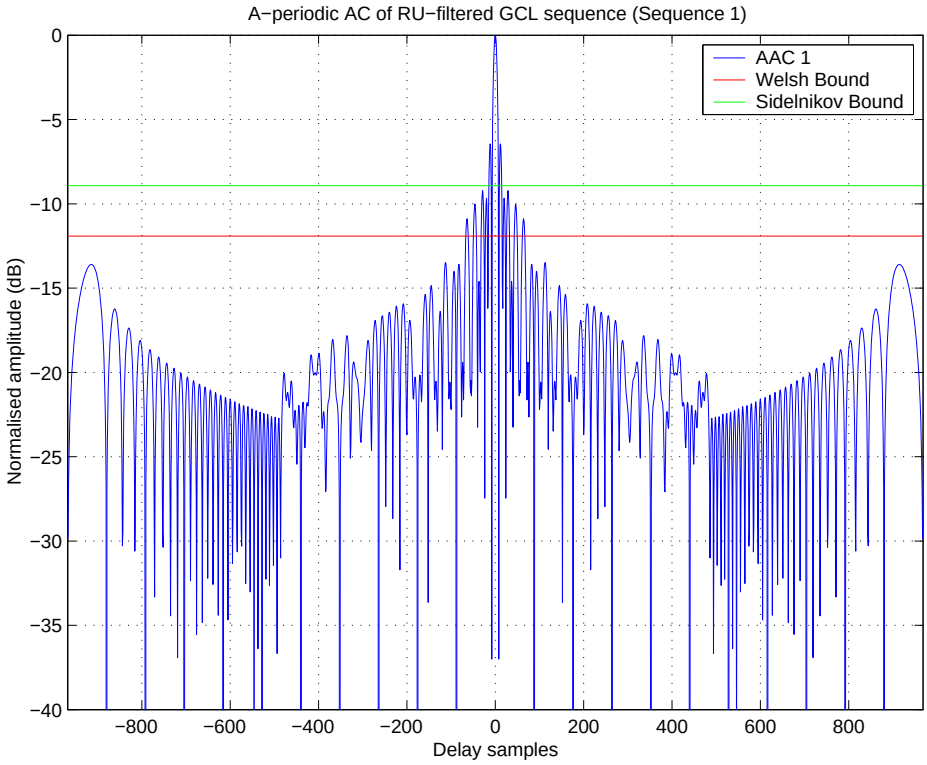

FIGURE 3.12: Aperiodic Auto Correlation (AAC) function of complex spreading sequence 1 in decibels. $(L = 121, RU filtered, spc = 8)$

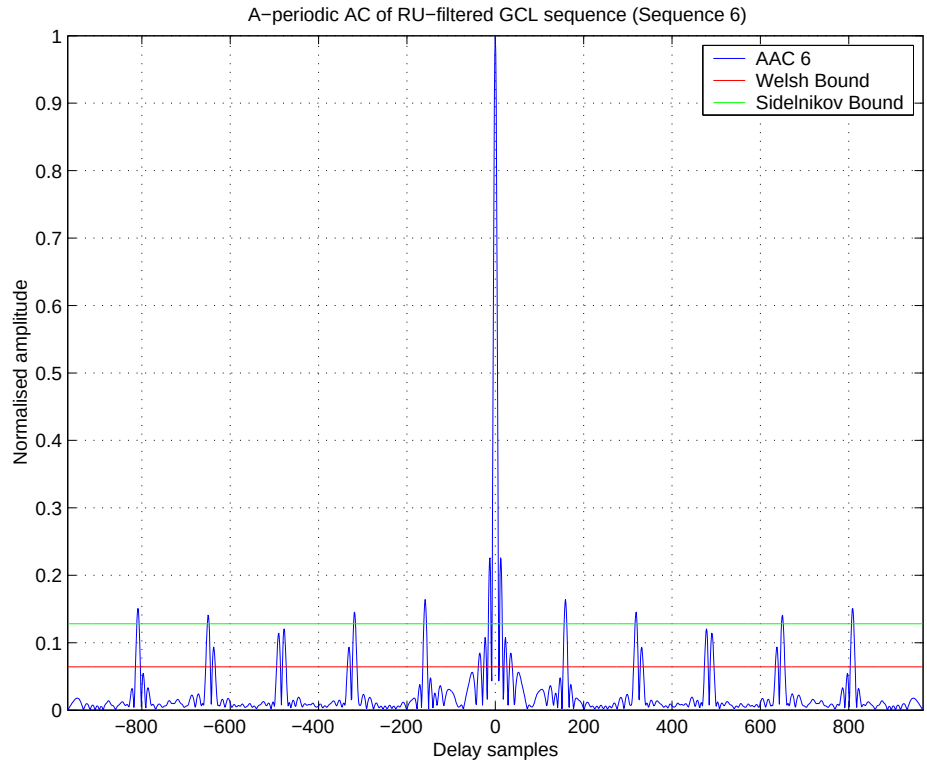

FIGURE 3.13: Aperiodic Auto Correlation (AAC) function of complex spreading sequence 6. $(L = 121, RU filtered, spc = 8)$

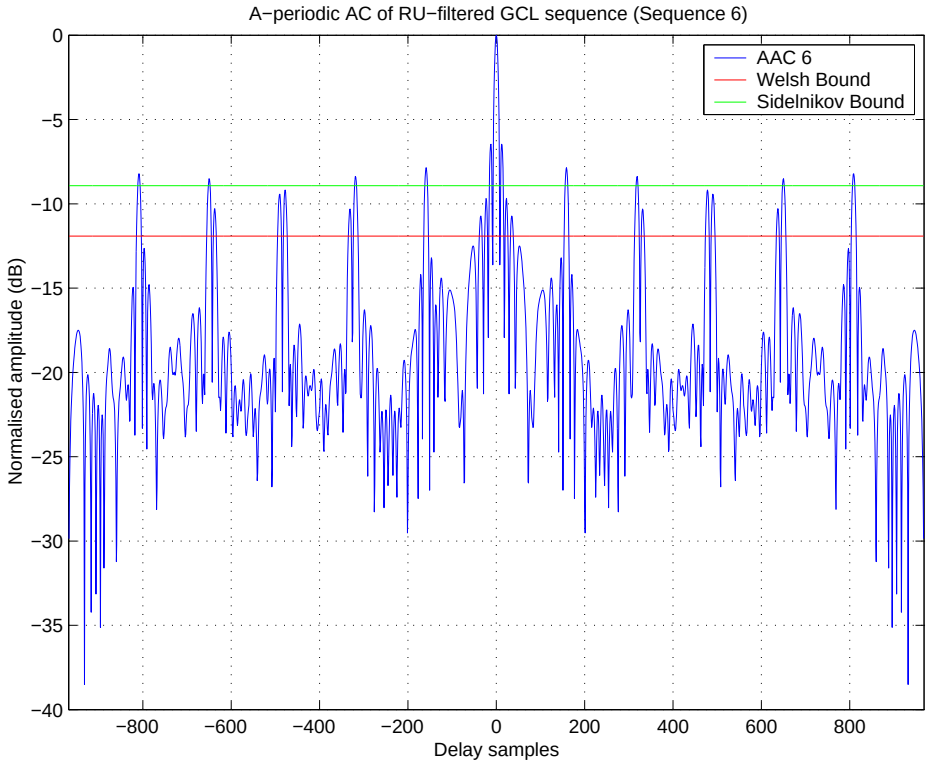

FIGURE 3.14: Aperiodic Auto Correlation (AAC) function of complex spreading sequence 6 in decibels. $(L = 121, RU filtered, spc = 8)$

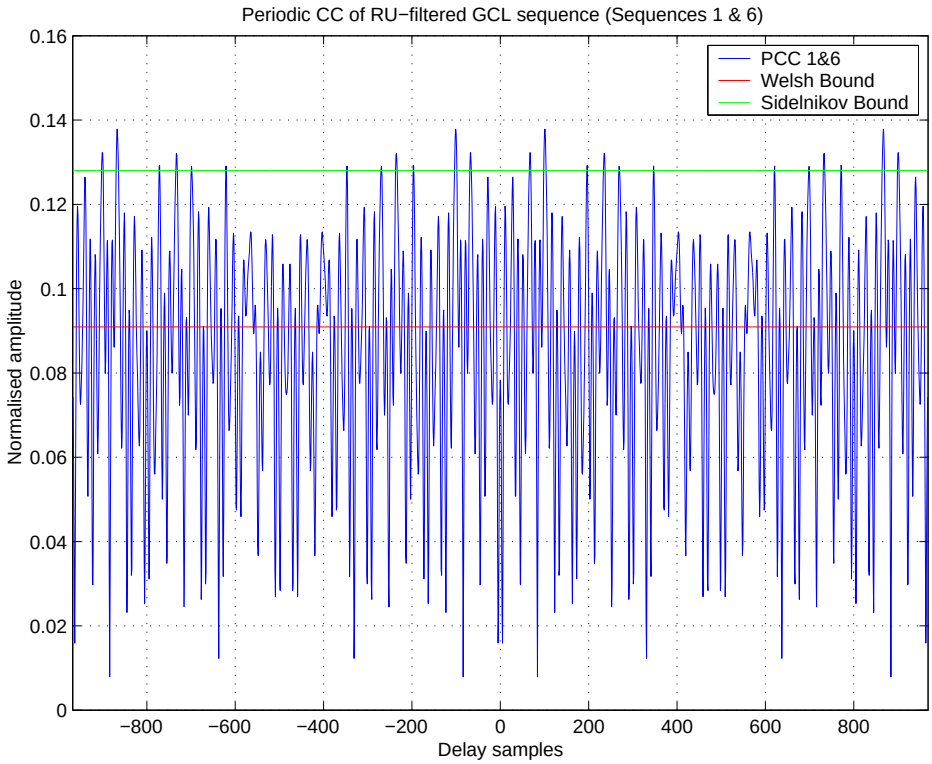

FIGURE 3.15: Periodic Cross Correlation(PCC) function between complex spreading sequences 1 and 6. $(L = 121, RU filtered, spc = 8)$

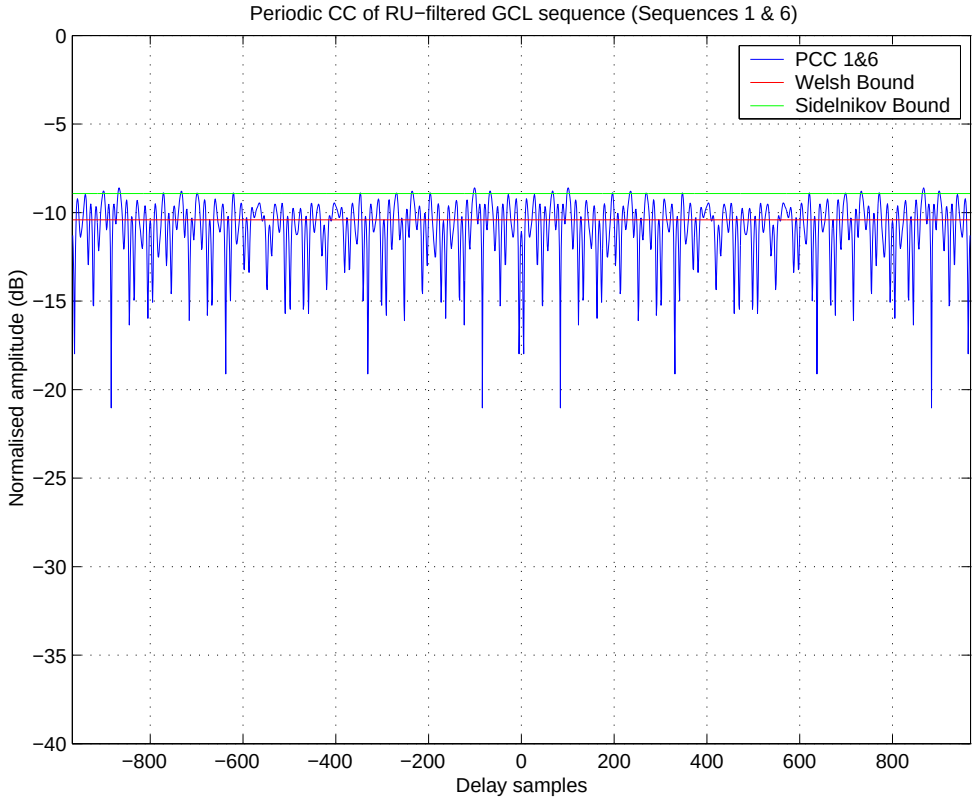

FIGURE 3.16: Periodic Cross Correlation(PCC) function between complex spreading sequences 1 and 6 in decibels. $(L = 121, RUfiltered, spc = 8)$

$$R_{su}[l] = \begin{cases} \sum_{k=0}^{L-1-l} s[l] \cdot u^*[k+l] & ; 0 \leq l \leq L-1 \\ \sum_{k=0}^{L-1+l} s[k-l] \cdot u^*[k] & ; 1-L \leq l < 0 \\ 0 & ; \mid l \mid \geq L \end{cases} \tag{3.19}$$

where * denotes complex conjugate and the time shift is l.

For the ZC sequences the aperiodic CC function is

$$R_{ab}[l] = \begin{cases} \sum_{k=0}^{L-1-l} W_{L_a}^{\frac{k(k+1)}{2}} \cdot W_{L_b}^{\frac{-(k+1)(k+l+1)}{2}} & ; 0 \leq l \leq L-1 \\ \sum_{k=0}^{L-1+l} W_{L_a}^{\frac{(k-l)(k-l+1)}{2}} \cdot W_{L_b}^{\frac{-k(k+l)}{2}} & ; 1-L \leq l < 0 \\ 0 & ; \mid l \mid \geq L \end{cases} \tag{3.20}$$

for $q = 0$ and L odd.

The aperiodic cross correlation functions for the ZC sequences are depicted in Figures 3.17 and 3.18.

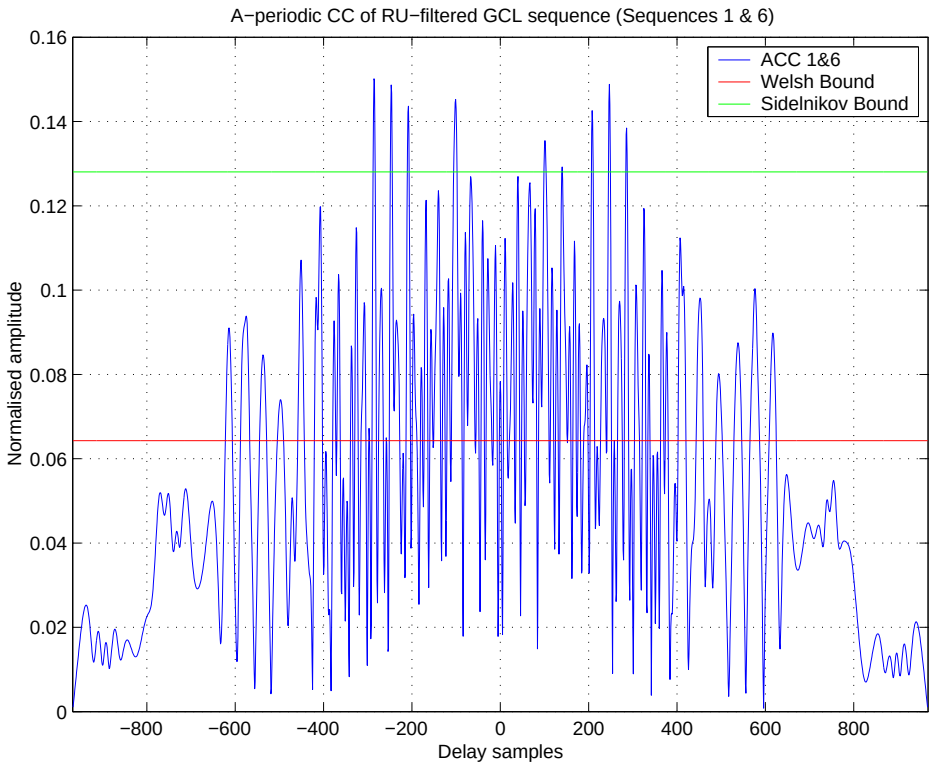

FIGURE 3.17: Aperiodic Cross Correlation(PCC) function between complex spreading sequences 1 and 6. $(L = 121, RU filtered, spc = 8)$

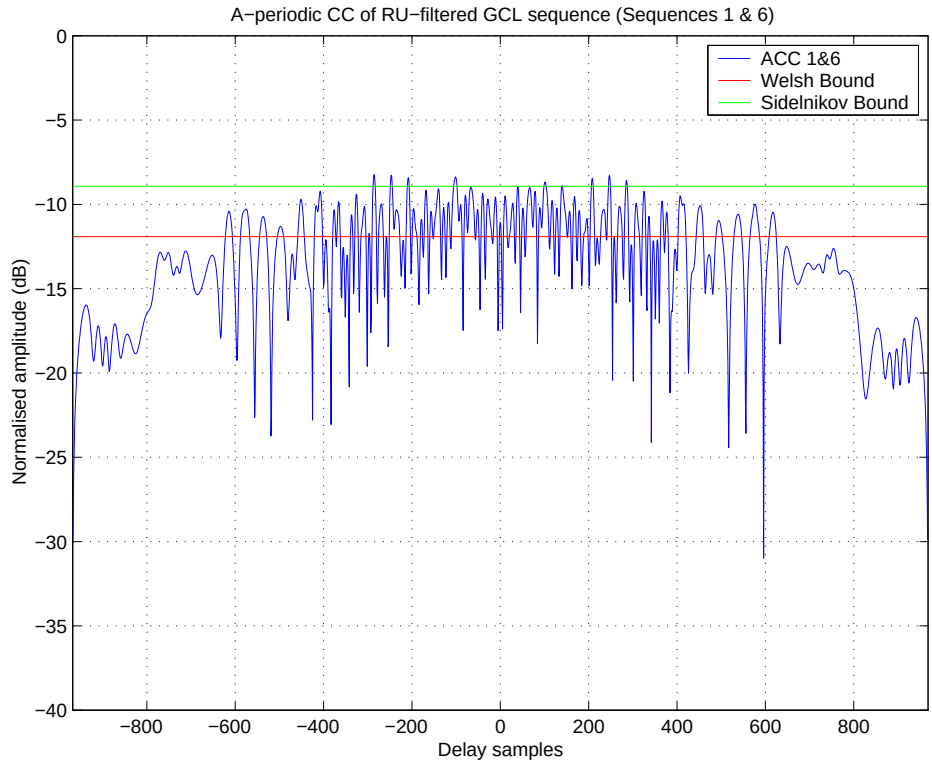

FIGURE 3.18: Periodic Cross Correlation(PCC) function between complex spreading sequences 1 and 6 in decibels. $(L = 121, RU filtered, spc = 8)$

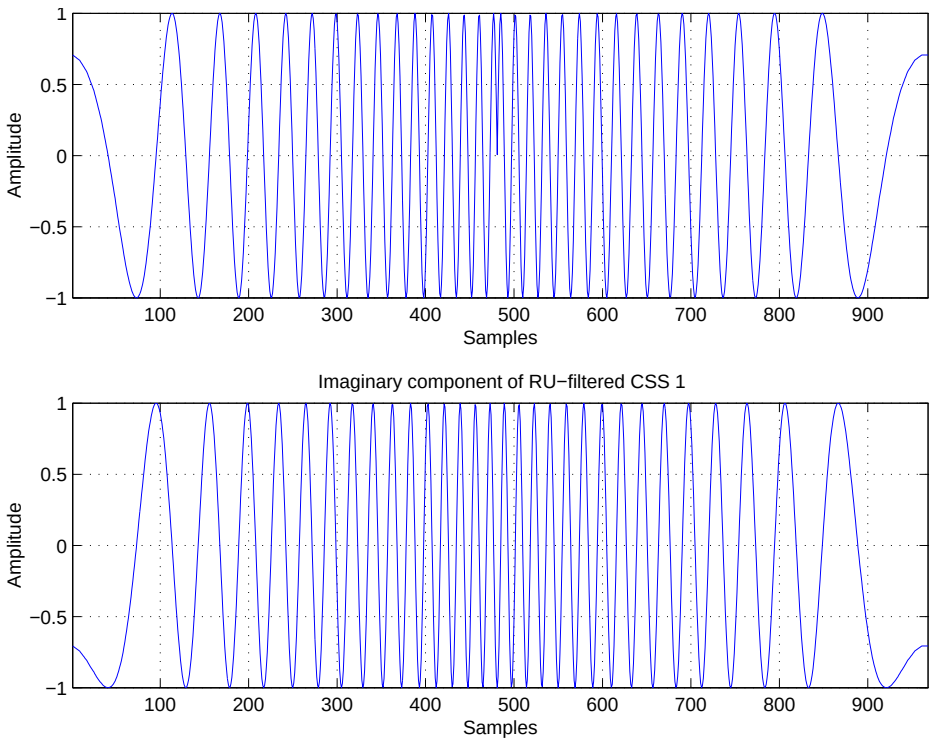

FIGURE 3.19: The Real, (a), and Imaginary, (b), part of the unique combination of CSS 1. $(L = 121, RU filtered, spc = 8)$

Unique combinations of the real and imaginary parts of the complex spreading sequences are used

$$C_{r_1 comb} = C_{r_1} - C_{i_1} \tag{3.21}$$

$$C_{i_1 comb} = -C_{r_1} - C_{i_1} \tag{3.22}$$

and is shown in Figure 3.19.

The same for complex spreading sequence 6

$$C_{r_6 comb} = C_{r_6} - C_{i_6} \tag{3.23}$$

$$C_{i_6 comb} = -C_{r_6} - C_{i_6} \tag{3.24}$$

and is depicted in Figure 3.20.

The auto- and cross correlation functions of these unique combinations are practically identical to the standard Zadoff-Chu correlation functions and are therefore presented in APPENDIX A.

Opperman sequences are closely related to Zadoff-Chu sequences. These sequences are briefly discussed in [34], [35], [36] and [37] for further interest.

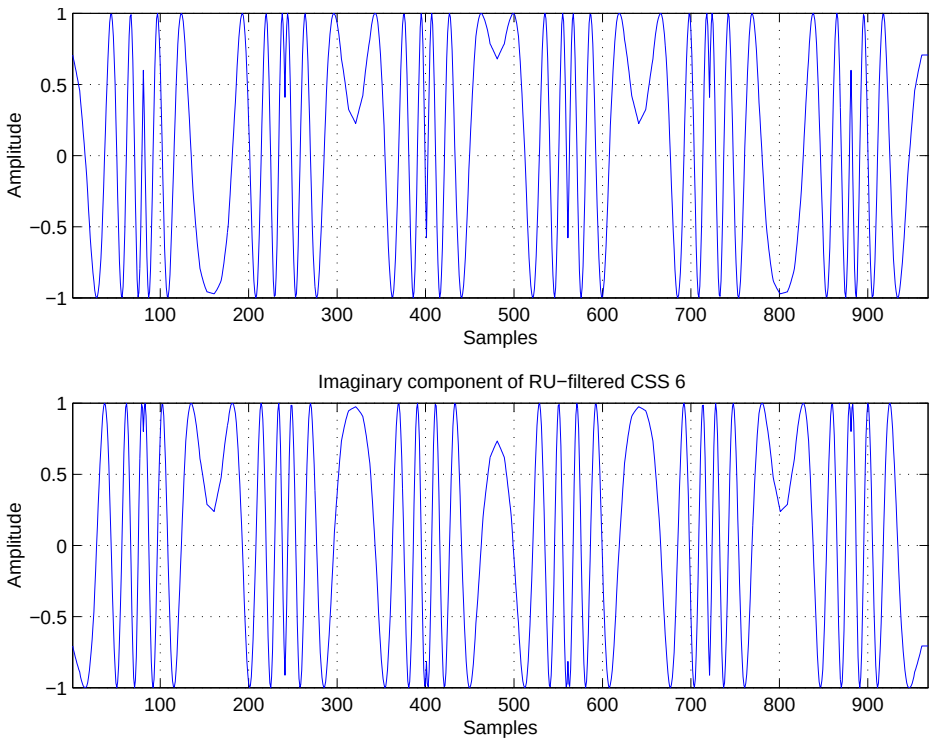

FIGURE 3.20: The Real, (a), and Imaginary, (b), part of the unique combination of CSS 6. $(L = 121, RU filtered, spc = 8)$

3.2.4 Bit Error Probability

In a spread spectrum system the total bit energy is not affected except for its distribution after frequency spreading. In an AWGN environment the spread spectrum modulation provides no gain and thus, the bit error probability will be the same as that of a narrow band system with the same type of modulation scheme. For a BPSK modulated spread spectrum, in an environment which is free of MUI, the average probability of a bit error for equally likely signals is,

$$\begin{aligned} P_e &= \tfrac{1}{2} erfc\left[\sqrt{\tfrac{\alpha^2 E_b}{2 \cdot N_o}(1-\rho_r)}\right] \\ &= Q\left[\sqrt{\tfrac{\alpha^2 E_b}{N_o}(1-\rho_r)}\right] \end{aligned} \tag{3.25}$$

as also given in [21], where α is the channel attenuation, E_b is the energy per bit, N_o the AWGN power spectral density and ρ_r is the correlation coefficient.

By the Central Limit Theorem, in an MUI environment, it is expected that for a large number of users, the MUI will have approximately a Gaussian distribution. With this approximation a simplistic expression is given in [22] for the probability of bit error in a MUI environment. This bit error probability is

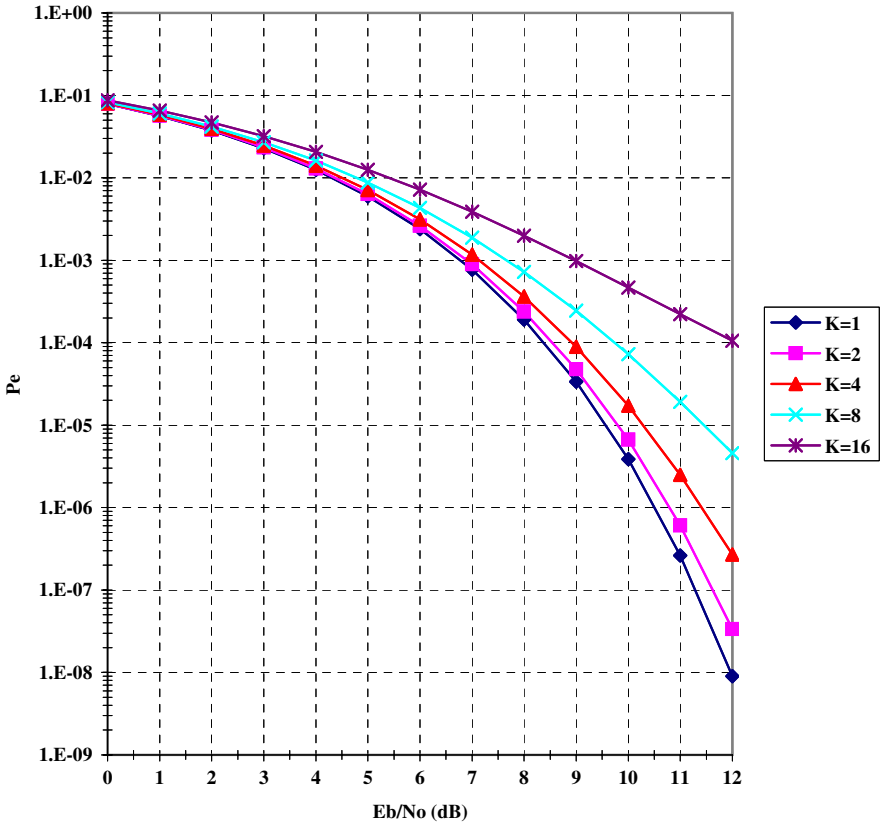

FIGURE 3.21: Bit error probability vs Eb/No for a BPSK/QPSK communication system in an MUI environment for a different number of users.

$$P_e = Q\left[SNR\right] \tag{3.26}$$

where

$$SNR \cong \left[\frac{K-1}{3 \cdot L} + \frac{1}{2}\left(\frac{E_b}{N_o}\right)^{-1}\right]^{-\frac{1}{2}} \tag{3.27}$$

where K is the number of users, L the spreading sequence length, E_b the energy per bit and N_o is the AWGN power spectral density. The bit error probability for a different number of users is depicted in Figure 3.21.

CHAPTER FOUR
DSSS TRANSMITTER

4.1 INTRODUCTION

The power efficiency of the HPA at the transmitter is one of the critical parameters in designing a wireless digital communication system. A constant envelope transmitter output signal requires no input power back-off from the $1dB$ compression point of the HPA, and thus utilizes the power amplifier optimally, ensuring high power efficiency in the transmitter. The balanced as well as the dual channel QPSK transmitters produce constant envelope (CE) outputs, by utilization of the constant envelope non-linearly-interpolated root-of-unity (CE NLI RU) filtered complex spreading sequences (CSS) described in Chapter 3.

Both balanced QPSK and a conventional dual channel QPSK transmitter structures have been investigated, employing unique combinations of the real and imaginary parts of the complex spreading sequences. Utilizing these unique combinations of complex spreading codes in the spreading and despreading processes, ensures optimal operation of the overall system. This advantage will become clear from the theoretical analysis. The theoretical analysis will be done for both balanced and dual-channel quadrature DSSS transmitter structures.

4.2 BALANCED QPSK DSSS TRANSMITTER

In the case of the balanced DSSS transmitter the data on the in-phase (I) and quadrature (Q) branches are identical. The serial incoming data is represented as a complex value and all multiplications in the transmitter are complex. Figure 4.1 shows the block diagram of the complex representation of the balanced DSSS transmitter. The theoretical analysis that

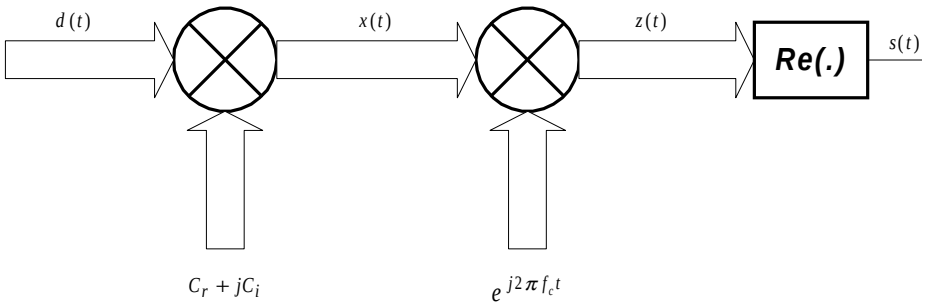

FIGURE 4.1: Block diagram of the balanced DSSS transmitter using complex notation

follows refers to this block diagram.

The input data can be represented as a complex value, namely

$$d(t) = d_1(t) + jd_1(t) \tag{4.1}$$

where $j = \sqrt{-1}$ and $d_1(t)$ denotes the serial input data at bit rate $f_b = \frac{1}{T_b}[bits/s]$, and T_b represents one bit period of a single data bit.

The complex data, $d(t)$ is then spread by multiplying $d(t)$ with a complex spreading sequence $c(t)$, where

$$c(t) = C_r + jC_i \tag{4.2}$$

and Cr denotes the real part of the complex spreading sequence, and Ci denotes the imaginary part of the complex spreading sequence.

The multiplication between $d(t)$ and $c(t)$ results in $x(t)$, i.e.

$$\begin{aligned} x(t) &= d(t) \cdot c(t) \\ &= [d_1(t) + jd_1(t)] \cdot [C_r + jC_i] \\ &= d_1(t) \cdot [C_r - C_i] + jd_1(t) \cdot [C_r + C_i] \end{aligned} \tag{4.3}$$

$x(t)$ is then modulated onto a carrier $e^{j2\pi f_c t}$, where f_c is the carrier frequency, to obtain the modulated signal, $z(t)$,

$$\begin{aligned} z(t) &= x(t) \cdot e^{j2\pi f_c t} \\ &= \{d_1(t) \cdot [C_r - C_i] + jd_1(t) \cdot [C_r + C_i]\} \cdot e^{j2\pi f_c t} \\ &= \{d_1(t) \cdot [C_r - C_i] \cdot cos(2\pi f_c t) - d_1(t) \cdot [C_r + C_i] \cdot sin(2\pi f_c t)\} \\ &\quad + j\{d_1(t) \cdot [C_r - C_i] \cdot sin(2\pi f_c t) + d_1(t) \cdot [C_r + C_i] \cdot cos(2\pi f_c t)\} \end{aligned} \quad (4.4)$$

The final output signal, $s(t)$, of the DSSS transmitter is obtained by taking the real part of $z(t)$, giving

$$\begin{aligned} s(t) &= Re\{z(t)\} \\ &= d_1(t) \cdot [C_r - C_i] \cdot cos(2\pi f_c) - d_1(t) \cdot [C_r + C_i] \cdot sin(2\pi f_c t) \end{aligned} \quad (4.5)$$

$s(t)$ can be represented in complex notation as

$$s(t) = Re\{u_1 \cdot e^{j2\pi f_c t}\} + Re\{ju_2 \cdot e^{j2\pi f_c t}\} \quad (4.6)$$

where

$$u_1(t) = d_1(t) \cdot [C_r - C_i] \quad (4.7)$$

and

$$u_2(t) = d_1(t) \cdot [C_r + C_i] \quad (4.8)$$

Figure 4.2 depicts an equivalent structure for the balanced DSSS transmitter shown in Figure 4.1.

The envelope of the balanced QPSK DSSS transmitter output signal can be written as

$$\begin{aligned} e(t) &= \sqrt{(x_1^2(t) + x_2^2(t))} \\ &= \sqrt{(d_1(t) \cdot [C_r - C_i])^2 + (d_1(t) \cdot [-C_r - C_i])^2} \\ &= \sqrt{(d_1^2(t) \cdot [C_r - C_i]^2) + (d_2^1(t) \cdot [-C_r - C_i]^2)} \\ &= \sqrt{(C_r C_r - 2C_r C_i + C_i C_i) + (C_r C_r + 2C_r C_i + C_i C_i)} \\ &= \sqrt{2} \cdot \sqrt{C_r^2 + C_i^2} \\ &= \sqrt{2} \end{aligned} \quad (4.9)$$

where $d_1^2(t) = 1$ and $C_r^2 + C_i^2 = 1$.

Equation 4.9 shows that the envelope of the output signal of the balanced QPSK DSSS transmitter is constant and the phase trajectory of the output is restrained to only traverse the unit circle.

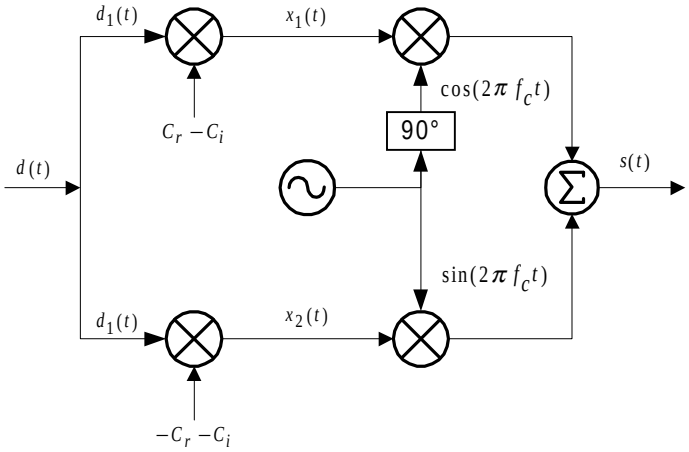

FIGURE 4.2: Block diagram of the balanced DSSS transmitter using real notation, suitable for direct implementation

4.3 DUAL CHANNEL QPSK DSSS TRANSMITTER

The dual channel QPSK transmitter has independent parallel data streams on the in-phase and quadrature branches. A direct realization is depicted in Figure 4.3.

Firstly the incoming serial data is converted into two parallel streams, $x_1(t)$ and $x_2(t)$, respectively. These two parallel data streams are then spread by means of unique combinations of complex spreading sequences, C_I and C_Q, as defined in Chapter 3.

$$x_1(t) = d_1(t) \cdot [C_r - C_i] \tag{4.10}$$

and

$$x_2(t) = d_2(t) \cdot [-C_r - C_i] \tag{4.11}$$

$x_1(t)$ and $x_2(t)$ are then modulated onto cosine and sine carriers and summed to form the final output signal, $s(t)$, of the dual channel QPSK DSSS transmitter, which can be written as:

$$\begin{aligned} s(t) &= x_1(t) \cdot \cos(2\pi f_c t) + x_2(t) \cdot \sin(2\pi f_c t) \\ &= d_1(t) \cdot [C_r - C_i] \cdot \cos(2\pi f_c t) \\ &+ d_2(t) \cdot [-C_r - C_i] \cdot \sin(2\pi f_c t) \end{aligned} \tag{4.12}$$

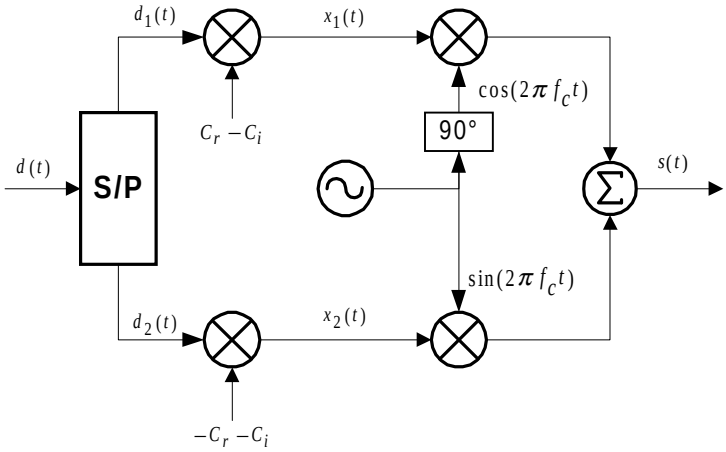

FIGURE 4.3: Block diagram of the QPSK DSSS transmitter

The envelope of the dual channel DSSS QPSK output signal can be written as:

$$\begin{aligned} e(t) &= \sqrt{(x_1^2(t) + x_2^2(t))} \\ &= \sqrt{(d_1(t) \cdot [C_r - C_i])^2 + (d_2(t) \cdot [-C_r - C_i])^2} \\ &= \sqrt{(d_1^2(t) \cdot [C_r - C_i]^2) + (d_2^2(t) \cdot [-C_r - C_i]^2)} \\ &= \sqrt{(C_r C_r - 2C_r C_i + C_i C_i) + (C_r C_r + 2C_r C_i + C_i C_i)} \\ &= \sqrt{2} \cdot \sqrt{C_r^2 + C_i^2} \\ &= \sqrt{2} \end{aligned} \tag{4.13}$$

where $d_1^2(t) = 1$, $d_2^2(t) = 1$ and $C_r^2 + C_i^2 = 1$.

The dual channel DSSS QPSK transmitter's output signal exhibits a constant envelope, as can be deducted from Equation 4.13.

CHAPTER FIVE
DSSS RECEIVER

5.1 INTRODUCTION

Different receiver structures were investigated in the search for an optimum configuration for the proposed DSSS communication system, employing complex spreading sequences. The receiver structures have been designed to demodulate and despread transmitter signals corresponding to the balanced and dual-channel transmitter configurations, respectively, as described in Chapter 4. The following sections give a detailed analysis of these receiver structures. In the theoretical analysis presented in this chapter only the effects of AWGN will be taken into account. The corresponding effects of phase and timing errors will be addressed in the synchronization section in Chapter 6.

5.2 BALANCED QPSK DSSS RECEIVER

A block diagram of the balanced DSSS receiver structure is depicted in Figure 5.1 and the theoretical analysis that follows refers to this block diagram.

The received signal, $r(t)$, at the input of the balanced DSSS receiver, can be written as

$$r(t) = d_1(t) \cdot C_I \cdot \cos(2\pi f_c t) + d_1(t) \cdot C_Q \cdot sin(2\pi f_c t) + n(t) \tag{5.1}$$

where C_I and C_Q are the data-synchronous in-phase and quadrature-phase combinations of the real and imaginary parts of the CSS, respectively. $n(t)$ denotes bandlimited AWGN with double-sided power spectral density $N_o/2$, which can be written as

$$n(t) = n_c(t)\cos(2\pi f_c t) - n_s(t)\sin(2\pi f_c t) \tag{5.2}$$

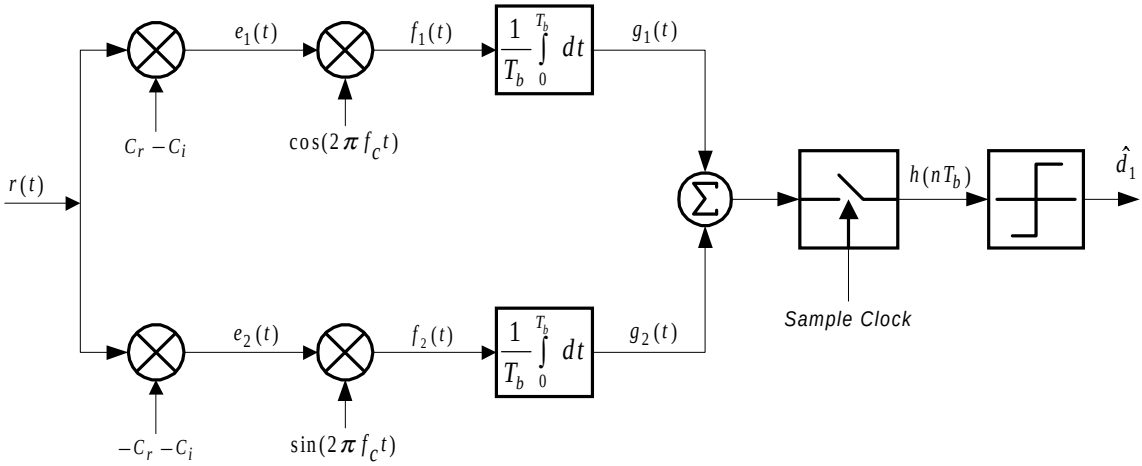

FIGURE 5.1: Block diagram of the balanced DSSS receiver

The incoming signal is split into two parallel branches which are despread with the unique complex spreading sequence combinations, C_I and C_Q. These despread in-phase and quadrature branches are then demodulated with the recovered cosine and sine carriers, to obtain $f_1(t)$ and $f_2(t)$, respectively.

Consider $f_1(t)$:

$$\begin{aligned} f_1(t) &= r(t) \cdot C_I \cos(2\pi f_c t)) \\ &= \frac{1}{2} d_1(t) \cdot C_I C_I \cdot [1 + \cos(4\pi f_c t)] + \frac{1}{2} d_1(t) \cdot C_Q C_I \cdot \sin(4\pi f_c t) \\ &+ \frac{1}{2} n_c(t) C_I \cdot [1 + \cos(4\pi f_c t)] - \frac{1}{2} n_s(t) C_I \cdot \sin(4\pi f_c t) \end{aligned} \tag{5.3}$$

and $f_2(t)$:

$$\begin{aligned} f_2(t) &= r(t) \cdot C_Q \sin(2\pi f_c t)) \\ &= \frac{1}{2} d_1(t) \cdot C_I C_Q \cdot \sin(4\pi f_c t) + \frac{1}{2} d_1(t) \cdot C_Q C_Q \cdot [1 - \cos(4\pi f_c t)] \\ &+ \frac{1}{2} n_c(t) C_Q \cdot \sin(4\pi f_c t) - \frac{1}{2} n_s(t) C_Q \cdot [1 - \cos(4\pi f_c t)] \end{aligned} \tag{5.4}$$

In order to eliminate the high frequency components of the mixing process, both branch signals are integrate-and-dumped to obtain $g_1(t)$ and $g_2(t)$,

$$g_1(t) = \frac{1}{2T_b} \int_0^{T_b} \{d_1(t) \cdot C_I C_I + n_c(t) C_I\}\, dt \tag{5.5}$$

$$g_2(t) = \frac{1}{2T_b} \int_0^{T_b} \{d_1(t) \cdot C_Q C_Q - n_s(t) C_Q\}\, dt \tag{5.6}$$

With $d_1(t) \in \{-1; 1\}$,

$$\omega_{c_I}(t) = \frac{1}{2T_b} \int_0^{T_b} n_c(t) C_I \, dt, \tag{5.7}$$

$$\omega_{s_Q}(t) = \frac{1}{2T_b} \int_0^{T_b} n_s(t) C_Q \, dt \tag{5.8}$$

Thus,

$$g_1(t) = \frac{d_1(t)}{2T_b} \int_0^{T_b} C_I C_I \, dt + \omega_{c_I}(t) \tag{5.9}$$

and

$$g_2(t) = \frac{d_1(t)}{2T_b} \int_0^{T_b} C_Q C_Q \, dt - \omega_{s_Q}(t) \tag{5.10}$$

Both branches, $g_1(t)$ and $g_2(t)$ can be summed because of the balanced structure at the transmitter, yielding identical data on both branches, whereafter a sample-and-hold operation is performed (at time instants $t = nT_b$ for $n = 0, 1, 2, ...$), to obtain

$$\begin{aligned} h(nT_b) &= \frac{1}{T_b} d_1(nT_b) \int_0^{T_b} \{C_r C_r + C_i C_i\} \, dt + \omega_{c_I}(nT_b) - \omega_{s_Q}(nT_b) \\ &= \frac{N}{T_b} d_1(nT_b) + \omega_{c_I}(nT_b) - \omega_{s_Q}(nT_b) \end{aligned} \tag{5.11}$$

where it is assumed that there is zero time shift between the incoming spreading codes and the despreading codes at the receiver. Finally, signal detection is performed on $h(nT_b)$ to recover the original data, $\hat{d_1}$.

5.3 DUAL CHANNEL QPSK DSSS RECEIVER

The block diagram of the dual channel QPSK DSSS receiver structure is shown in Figure 5.2 and the theoretical analysis that follows refers to this block diagram.

The received signal, $r(t)$, at the input of the DSSS QPSK receiver can be written as

$$r(t) = d_1(t) \cdot C_I \cdot cos(2\pi f_c) + d_2(t) \cdot C_Q \cdot sin(2\pi f_c t) + n(t) \tag{5.12}$$

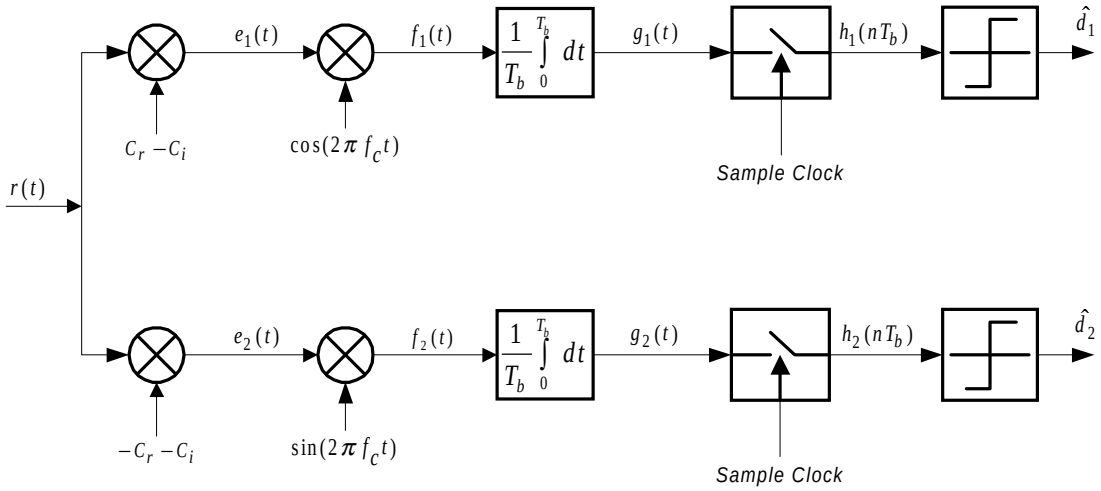

FIGURE 5.2: Block diagram of the QPSK DSSS receiver

where C_I and C_Q are the data-synchronous in-phase and quadrature-phase combinations of the real and imaginary parts of the CSS, respectively. $n(t)$ denotes bandlimited AWGN with double-sided power spectral density $N_o/2$, and can be written as

$$n(t) = n_c(t)\cos(2\pi f_c) - n_s(t)\sin(2\pi f_c t) \tag{5.13}$$

The incoming signal is split into two parallel branches, despread with C_I and C_Q and multiplied with the recovered cosine and sine carriers, to obtain $f_1(t)$ and $f_2(t)$, respectively.

This yields

$$\begin{aligned} f_1(t) &= r(t)\cdot C_I\cos(2\pi f_c t)) \\ &= \frac{1}{2}d_1(t)\cdot C_I C_I\cdot[1+\cos(4\pi f_c t)] + \frac{1}{2}d_2(t)\cdot C_Q C_I\cdot\sin(4\pi f_c t) \\ &+ \frac{1}{2}n_c(t)C_I\cdot[1+\cos(4\pi f_c t)] - \frac{1}{2}n_s(t)C_I\cdot\sin(4\pi f_c t) \end{aligned} \tag{5.14}$$

and

$$\begin{aligned} f_2(t) &= r(t)\cdot C_Q\sin(2\pi f_c t)) \\ &= \frac{1}{2}d_1(t)\cdot C_I C_Q\cdot\sin(4\pi f_c t) + \frac{1}{2}d_2(t)\cdot C_Q C_Q\cdot[1-\cos(4\pi f_c t)] \\ &+ \frac{1}{2}n_c(t)C_Q\cdot\sin(4\pi f_c t) - \frac{1}{2}n_s(t)C_Q\cdot[1-\cos(4\pi f_c t)] \end{aligned} \tag{5.15}$$

In order to eliminate the high frequency components, both branch signals are

integrate-and-dumped to obtain $g_1(t)$ and $g_2(t)$,

$$g_1(t) = \frac{1}{2T_b}\int_0^{T_b} d_1(t)\cdot C_I C_I\,dt + \frac{1}{2T_b}\int_0^{T_b} n_c(t)C_I\,dt \tag{5.16}$$

$$g_2(t) = \frac{1}{2T_b}\int_0^{T_b} d_2(t)\cdot C_Q C_Q\,dt - \frac{1}{2T_b}\int_0^{T_b} n_s(t)C_Q\,dt \tag{5.17}$$

With $d_1(t) \in \{-1;1\}$, $d_2(t) \in \{-1;1\}$,

$$\omega_{c_I}(t) = \frac{1}{2T_b}\int_0^{T_b} n_c(t)C_I\,dt, \tag{5.18}$$

$$\omega_{s_Q}(t) = \frac{1}{2T_b}\int_0^{T_b} n_s(t)C_Q\,dt \tag{5.19}$$

Note that at zero time shift,

$$\frac{1}{T_b}\int_0^{T_b} C_I C_I\,dt \approx \frac{N}{T_b} \tag{5.20}$$

and

$$\frac{1}{T_b}\int_0^{T_b} C_Q C_Q\,dt \approx \frac{N}{T_b} \tag{5.21}$$

Equation 5.16 and 5.17 reduces to

$$g_1(t) = \frac{Nd_1(t)}{2T_b} + \omega_{c_I}(t) \tag{5.22}$$

and

$$g_2(t) = \frac{Nd_2(t)}{2T_b} - \omega_{s_Q}(t) \tag{5.23}$$

$g_1(t)$ and $g_2(t)$ are then sample-and-hold at time instants $t = nT_b$ for $n = 0, 1, 2, ...$, to obtain

$$h_1(nT_b) = \frac{Nd_1(nT_b)}{2T_b} + \omega_{c_I}(nT_b) \tag{5.24}$$

$$h_2(nT_b) = \frac{Nd_2(nT_b)}{2T_b} - \omega_{s_Q}(nT_b) \tag{5.25}$$

Signal detection is performed on $h_1(nT_b)$ and $h_2(nT_b)$ to recover the original data signals, $\hat{d}_1$ and $\hat{d}_2$, after which a parallel-to-serial conversion is done to recover an estimate of the original serial data stream, $\hat{d}(t)$.

CHAPTER SIX
SYNCHRONIZATION

6.1 INTRODUCTION

In a spread-spectrum communication link several levels of synchronization have to be maintained between the transmitter and the receiver. These synchronization subsystems can be subdivided into temporal and carrier synchronization classes. The initial time synchronization subsystem is responsible for the determination of the initial code phase of the received spread-spectrum signal, and the corresponding process is called *code acquisition*. The function of second temporal synchronisation phase is to maintain code synchronization after initial code acquisition has been accomplished, and is called *code tracking*. Carrier synchronization comprises *initial carrier acquisition* and *carrier phase tracking*. All of these above mentioned components of synchronization needs to function jointly and optimally to deliver a spread-spectrum system with reliable performance. The synchronization of a DSSS communication system employing complex spreading sequences will be investigated and designed in this chapter, constituting one of the main novel contributions of this dissertation, apart of the hardware implementation of the complete system.

A DSSS system requires excellent synchronization for code acquisition, code tracking and carrier synchronization to ensure best system performance and to minimize multi-user interference. Code tracking loops and demodulation receiver structures for spread-spectrum systems can be categorised in coherent and non-coherent tracking loops and receiver structures. Coherent receiver loops make use of received carrier phase information, whereas non-coherent receiver loops do not. In this DSSS communication system, employing complex spreading sequences, synchronization structures for code acquisition and code

tracking as well as carrier tracking and data demodulation will be investigated and designed by using a coherent approach. The reason for utilizing coherent detection and tracking loop structures is because of the advantage in system performance of the coherent receiver compared to the non-coherent receiver structures.

A combined coherent Decision-Directed Costas Carrier Recovery Loop (DD-CCRL) and Coherent Decision-Directed Complex Delay-Lock-Loop (DD-CDLL) synchronization scheme for a DSSS communication system, originally proposed by De Gaudenzi et al [8] for systems using binary spreading sequences, have been generalized and extended to include systems employing binary and/or complex spreading sequences. In addition to its versatility, other major advantages offered by this unique code locking scheme are that it eliminates the problem of arm imbalance by obviating the need for squaring devices in the loop structure. The absence of the latter leads to improved tracking ability. The new structure also facilitates simplified hardware by requiring only two loop correlators in stead of four, such as required for non-coherent DLL schemes in the case of complex spreading sequences. This simplified structure is obtained through the novel use of composite signals in the spreading, despreading and code locking processes, which leads to effective cancellation of unwanted cross product interference terms, generated in the said processes.

6.2 GLOBAL RECEIVER STRUCTURE

The global DSSS synchronization scheme is depicted in Figure 6.1. The receiver synchronization structure consists of three modules running in parallel. These modules are the acquisition circuitry [38], shown in Figure 6.4, consisting of a coherent Decision-Directed Costas Carrier-Recovery-Loop (DD-CCRL), shown in Figures 6.2 and 6.3, and a novel coherent Decision-Directed Complex Delay-Lock-Loop (DD-CDLL) depicted in Figures 6.5 and 6.9, for the balanced QPSK and dual channel QPSK configurations, respectively. Initial synchronization is performed by the acquisition circuitry. Prior to acquisition the transmit and receive complex sequence generators are not in synchronism, that is, the zero reference time positions of the complex spreading sequences are not aligned. In order to achieve code locking, a course sliding correlation [38] is first performed on the in-phase and quadrature phase branches. The outputs of the sliding correlators are then used to determine when the spreading code and the despreading code are aligned within one chip period. During the initial synchronization time the coherent DD-CDLL is in an open loop free running mode. Once the alignment of the spreading

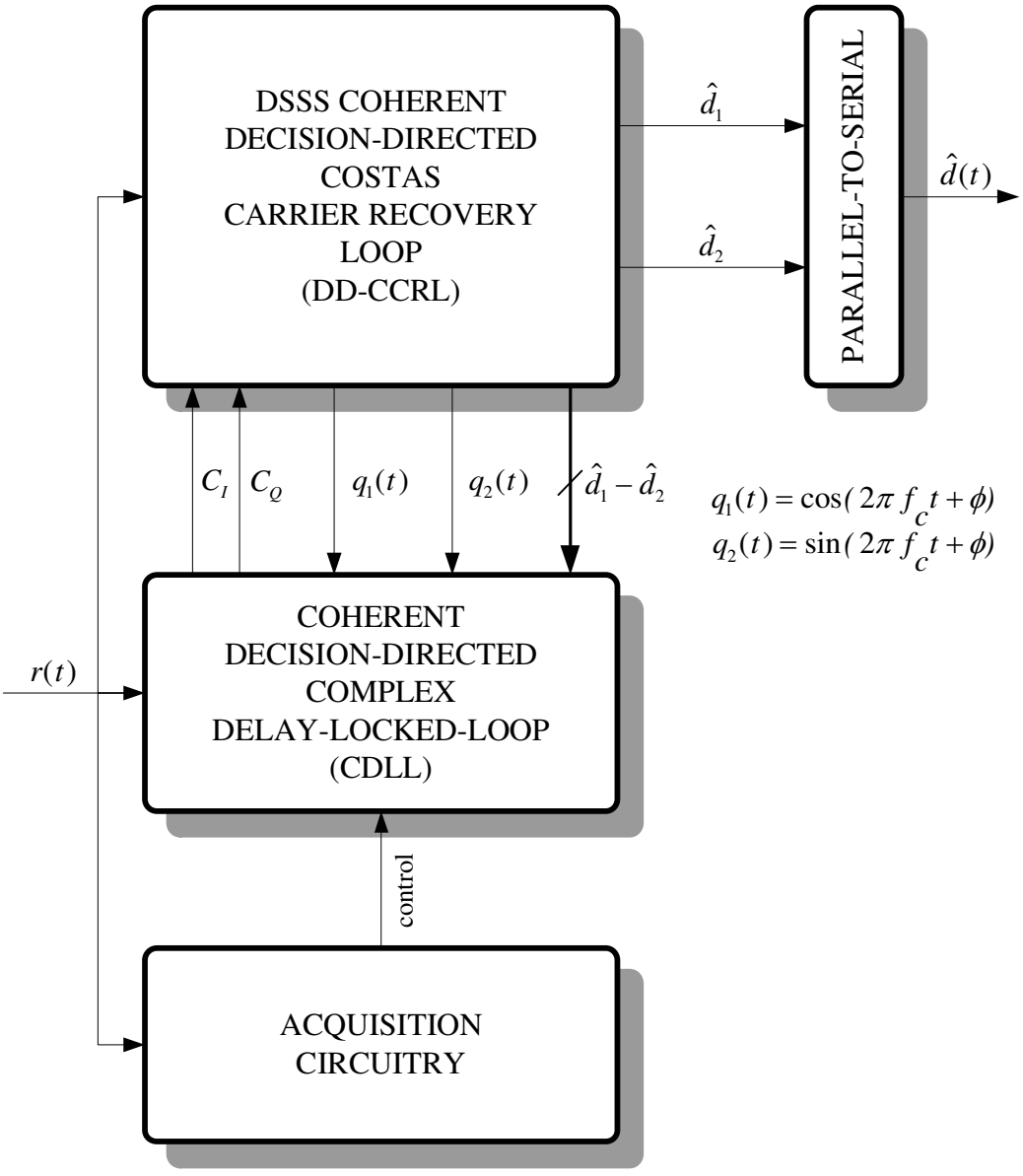

FIGURE 6.1: Block diagram of the global DSSS receiver structure

and despreading codes are detected to be within one chip period, the coherent DD-CDLL is switched to a closed loop mode for code tracking. Consequently, the receiver complex spreading sequence generator is aligned to within one chip period with the transmitted spreading sequence.

The operation of the coherent DD-CDLL commences immediately after course synchronization (acquisition) has been achieved. Code tracking or fine synchronization is performed by the coherent DD-CDLL. The coherent DD-CDLL provides the synchronized punctual composite signals of the real and imaginary parts of the CSS to the DD-CCRL to perform carrier tracking. The same punctual composite signals are also fed to the despreading and data detection subsystems, to facilitate recovery of the original data streams. The received DSSS signal is correlated with composite signals, consisting of the difference between the early and late replicas of unique combinations of the real and imaginary parts of a CSS, on the in-phase and quadrature phase branches, respectively. The correlation results are converted to baseband by means of the recovered cosine and sine carriers, provided by the DD-CCRL. The data modulation on the two branches is eliminated by means of the decisions made in the DD-CCRL and then combined to derive a proper loop error signal to drive the Numerically Controlled Code Generator (NCCG). The major advantage of this unique structure of the coherent DD-CDLL is that it eliminates the problem of arm imbalance. It simplifies and reduces the hardware that would have been required to realise four correlators, to the hardware required to implement only two correlators, and also improves the tracking capabilities of the loop, because of the absence of squaring devices (commonly found in non-coherent DLL schemes).

The DD-CCRL provides recovered sine and cosine carriers to demodulate the incoming signal to a specific intermediate frequency (IF). Despreading of the incoming signal forms part of the DD-CCRL. Despreading is also done by means of the same unique combinations of real and imaginary parts of the complex spreading sequences used at the transmitter, ensuring optimal performance through the elimination of unwanted cross product interference terms. Data decisions are made on the despreaded in-phase and quadrature branches and are used to eliminate the data modulation on the despreaded branches to generate an error signal for controlling the NCO that provides the recovered quadrature carriers.

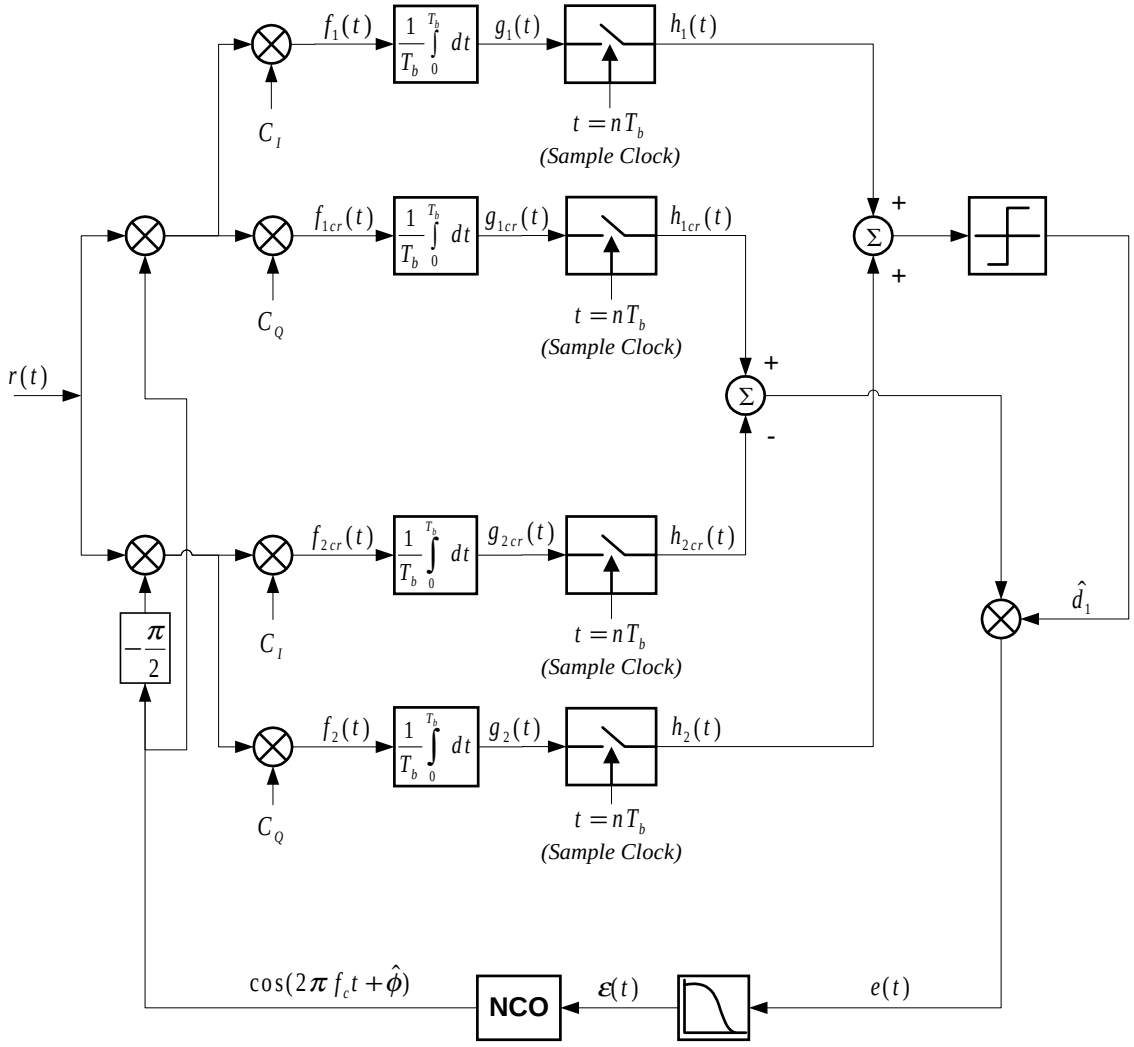

FIGURE 6.2: Block diagram of the Balanced QPSK Coherent Complex Decision-Directed Costas Carrier Recovery Loop

6.3 CARRIER AND PHASE SYNCHRONIZATION

In this section the coherent DD-CCRLs will be analyzed for both the balanced QPSK and dual channel QPSK DSSS communication systems.

6.3.1 Balanced QPSK Coherent Complex Decision-Directed Costas Carrier Recovery Loop

Figure 6.2 shows the block diagram of the coherent complex DD-CCRL used for carrier tracking in the balanced QPSK DSSS configuration.

With reference to Figure 6.2, the input signal $r(t)$, on a specific IF at the input of the

balanced QPSK DSSS receiver, can be written as

$$r(t) = d_1(t) \cdot C_I \cdot \cos(2\pi f_c t + \phi) - d_1(t) \cdot C_Q \cdot sin(2\pi f_c t + \phi) + n(t) \tag{6.1}$$

where C_I and C_Q are the data-synchronous in-phase and quadrature-phase combinations of the real and imaginary parts of the CSS, respectively. $n(t)$ denotes bandlimited AWGN with double-sided power spectral density $N_o/2$, which can be written as

$$n(t) = n_c(t)\cos(2\pi f_c t + \phi) - n_s(t)\sin(2\pi f_c t + \phi) \tag{6.2}$$

The incoming signal is demodulated with an estimate of the incoming quadrature carriers and despread with synchronized despreading sequences to produce a despread baseband signal, as well as high frequency components on the in-phase and quadrature branch, given by

$$\begin{aligned} f_{1cr}(t) &= \frac{d_1(t)C_I C_Q}{2}\left[\cos(4\pi f_c t + \phi + \hat{\phi}) + \cos(\phi - \hat{\phi})\right] \\ &- \frac{d_1(t)C_Q C_Q}{2}\left[\sin(4\pi f_c t + \phi + \hat{\phi}) + \sin(\phi - \hat{\phi})\right] \\ &+ \frac{n_c(t)C_Q}{2}\left[\cos(4\pi f_c t + \phi + \hat{\phi}) + \cos(\phi - \hat{\phi})\right] \\ &- \frac{n_s(t)C_Q}{2}\left[\sin(4\pi f_c t + \phi + \hat{\phi}) + \sin(\phi - \hat{\phi})\right] \end{aligned} \tag{6.3}$$

on the in-phase branch and

$$\begin{aligned} f_{2cr}(t) = &- \frac{d_1(t)C_I C_I}{2}\left[\sin(4\pi f_c t + \phi + \hat{\phi}) - \sin(\phi - \hat{\phi})\right] \\ &+ \frac{d_1(t)C_I C_Q}{2}\left[\cos(\phi - \hat{\phi}) - \cos(4\pi f_c t + \phi + \hat{\phi})\right] \\ &- \frac{n_c(t)C_I}{2}\left[\sin(4\pi f_c t + \phi + \hat{\phi}) - \sin(\phi - \hat{\phi})\right] \\ &+ \frac{n_s(t)C_I}{2}\left[\cos(\phi - \hat{\phi}) - \cos(4\pi f_c t + \phi + \hat{\phi})\right] \end{aligned} \tag{6.4}$$

on the quadrature branch.

In order to eliminate the high frequency components and conclude the despreading process, both branch signals are integrate-and-dumped to obtain $g_1(t)$ and $g_2(t)$, respectively:

$$g_{1cr}(t) = \frac{d_1(t)\cos(\phi - \hat{\phi})}{2T_b}\int_0^{T_b} C_I C_Q dt$$

$$
\begin{aligned}
& - \frac{d_1(t)\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_Q C_Q dt \\
& + \frac{\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} n_c(t) C_Q dt \\
& - \frac{\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} n_s(t) C_Q dt
\end{aligned} \tag{6.5}
$$

$$
\begin{aligned}
g_{2cr}(t) &= \frac{d_1(t)\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_I dt \\
&+ \frac{d_1(t)\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_Q dt \\
&+ \frac{\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} n_c(t) C_I dt \\
&+ \frac{\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} n_s(t) C_I dt
\end{aligned} \tag{6.6}
$$

Noting that $d_1(t) \in \{-1; 1\}$ and

$$\omega_{c_I}(t) = \frac{1}{2T_b}\int_0^{T_b} n_c(t) C_I \, dt, \tag{6.7}$$

$$\omega_{c_Q}(t) = \frac{1}{2T_b}\int_0^{T_b} n_c(t) C_Q \, dt, \tag{6.8}$$

$$\omega_{s_I}(t) = \frac{1}{2T_b}\int_0^{T_b} n_s(t) C_I \, dt \tag{6.9}$$

$$\omega_{s_Q}(t) = \frac{1}{2T_b}\int_0^{T_b} n_s(t) C_Q \, dt \tag{6.10}$$

equations 6.5 and 6.6 can be written as

$$
\begin{aligned}
g_{1cr}(t) &= \frac{d_1(t)\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_Q dt \\
&- \frac{d_1(t)\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_Q C_Q dt
\end{aligned}
$$

$$+ \quad \omega_{cQ}(t)\cos(\phi-\hat{\phi})$$

$$- \quad \omega_{sQ}(t)\sin(\phi-\hat{\phi}) \tag{6.11}$$

and

$$\begin{aligned} g_{2cr}(t) &= \frac{d_1(t)\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_I dt \\ &+ \frac{d_1(t)\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_Q dt \\ &+ \omega_{cI}(t)\sin(\phi-\hat{\phi}) \\ &+ \omega_{sI}(t)\cos(\phi-\hat{\phi}) \end{aligned} \tag{6.12}$$

The outputs of the integrate-and-dump blocks are sample-and-hold at optimum time instants at the end of each integration period (i.e., at time instants $t = nT_b$ for $n = 0, 1, 2, ...$).

The quadrature samples are subtracted from the in-phase samples and the result is multiplied by the data decision, $\hat{d}_1$, provided by the despreading and data detection processes. This is done to produce an DD-CCRL error signal without any data modulation. This concept is based on a decision-directed method and has the advantage of eliminating the additional noise from the tracking loop caused by data modulation (so-called data-dependent noise). The error signal is given by

$$\begin{aligned} e(nT_b) = &- \frac{1}{2T_b}\int_0^{T_b}\left[C_I C_I + C_Q C_Q\right]dt \cdot \sin(\phi-\hat{\phi}) \\ &+ \left[\omega_{cQ}(nT_b) - \omega_{sI}(nT_b)\right]\sin(\phi-\hat{\phi}) \\ &- \left[\omega_{sI}(nT_b) + \omega_{sQ}(nT_b)\right]\cos(\phi-\hat{\phi}) \end{aligned} \tag{6.13}$$

Equation 6.13 can be simplified by substituting C_I and C_Q with the combinations of the real and imaginary parts of the CSS as defined in Chapter 3. Thus, 6.13 can be written as

$$\begin{aligned} e(nT_b) = &- \frac{1}{2T_b}\int_0^{T_b} 2\left[C_r^2 + C_i^2\right]dt \cdot \sin(\phi-\hat{\phi}) \\ &+ \left[\omega_{cQ}(nT_b) - \omega_{sI}(nT_b)\right]\sin(\phi-\hat{\phi}) \\ &- \left[\omega_{sI}(nT_b) + \omega_{sQ}(nT_b)\right]\cos(\phi-\hat{\phi}) \end{aligned} \tag{6.14}$$

where

$$\begin{aligned} \frac{1}{2T_b}\int_0^{T_b} 2\left[C_r^2 + C_i^2\right] dt &= \frac{2LT_c}{2T_b} \\ &= \frac{2T_b}{2T_b} \\ &= 1 \end{aligned} \tag{6.15}$$

L denotes the spreading sequence length and T_c the chip period of the CSS.

By substituting 6.15 into 6.23, the error signal can be written as

$$\begin{aligned} e(nT_b) = &- \sin(\phi - \hat{\phi}) \\ &+ \left[\omega_{cQ}(nT_b) - \omega_{sI}(nT_b)\right]\sin(\phi - \hat{\phi}) \\ &- \left[\omega_{sI}(nT_b) + \omega_{sQ}(nT_b)\right]\cos(\phi - \hat{\phi}) \end{aligned} \tag{6.16}$$

where it is assumed that there is zero time shift between the incoming spreading codes and the despreading codes at the receiver. The produced error signal is low-pass filtered and used to control the NCO to recover the quadrature carriers.

It is important to note that the complex despreading codes C_I and C_Q are used in the DD-CCRL to despread the quadrature and in-phase branch, respectively, which is the exact opposite of the despreading and data detection processes. This is to ensure that auto correlation terms will be formed as a result of the product with the DD-CCRL error signal, as shown in 6.13, otherwise a cross correlation term will emerge as a result of the product with the DD-CCRL error signal, which would be very small and would nevertheless lead to insufficient carrier tracking capability.

6.3.2 Dual Channel QPSK Coherent Complex Decision-Directed Costas Carrier Recovery Loop

The block diagram of the coherent complex DD-CCRL used for carrier tracking in the dual channel QPSK DSSS configuration, is depicted in Figure 6.3.

The input of the dual channel QPSK DSSS receiver is given as

$$r(t) = d_1(t)\cdot C_I \cdot \cos(2\pi f_c t + \phi) - d_2(t)\cdot C_Q \cdot sin(2\pi f_c t + \phi) + n(t) \tag{6.17}$$

where all the symbols are as defined in the previous section.

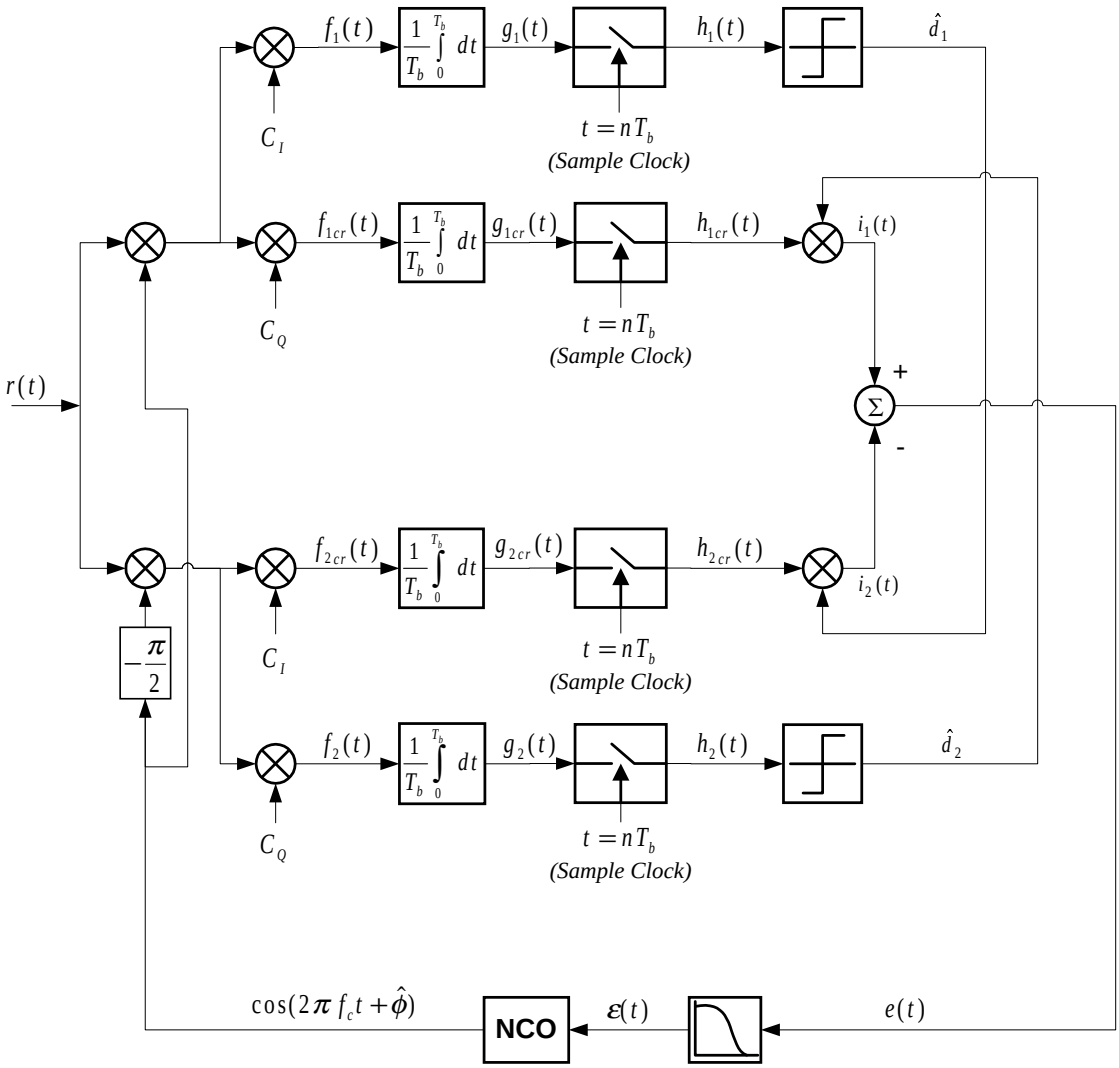

FIGURE 6.3: Block diagram of the dual channel QPSK Complex Decision-Directed Costas Carrier Recovery Loop

Following a similar derivation as that used for the balanced QPSK DSSS system, after elimination of the high frequency components and despreading, the in-phase and quadrature branch signals are integrate-and-dumped to yield $g_1cr(t)$ and $g_2cr(t)$, respectively:

$$\begin{aligned} g_{1cr}(t) &= \frac{d_1(t)\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_Q dt \\ &- \frac{d_2(t)\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_Q C_Q dt \\ &+ \frac{\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} n_c(t) C_Q dt \\ &- \frac{\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} n_s(t) C_Q dt \end{aligned} \tag{6.18}$$

$$\begin{aligned} g_{2cr}(t) &= \frac{d_1(t)\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_I dt \\ &+ \frac{d_2(t)\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_Q dt \\ &+ \frac{\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} n_c(t) C_I dt \\ &+ \frac{\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} n_s(t) C_I dt \end{aligned} \tag{6.19}$$

By applying the same definitions used for the balanced QPSK DSSS configuration, equations 6.18 and 6.19 can be written as

$$\begin{aligned} g_{1cr}(t) &= \frac{d_1(t)\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_Q dt \\ &- \frac{d_2(t)\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_Q C_Q dt \\ &+ \omega_{cQ}(t)\cos(\phi-\hat{\phi}) \\ &- \omega_{sQ}(t)\sin(\phi-\hat{\phi}) \end{aligned} \tag{6.20}$$

and

$$\begin{aligned} g_{2cr}(t) &= \frac{d_1(t)\sin(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_I dt \\ &+ \frac{d_2(t)\cos(\phi-\hat{\phi})}{2T_b}\int_0^{T_b} C_I C_Q dt \end{aligned}$$

$$+ \quad \omega_{cI}(t)\sin(\phi - \hat{\phi})$$

$$+ \quad \omega_{sI}(t)\cos(\phi - \hat{\phi}) \tag{6.21}$$

The integrate-and-dump outputs are sample-and-hold at optimum time instants at the end of each integration period (at time instants $t = nT_b$ for $n = 0, 1, 2, ...$).

The sampled in-phase and quadrature branches are cross multiplied by the data decisions, $\hat{d}_2$ and $\hat{d}_1$, made on the quadrature and in-phase branches, respectively, in the despreading and data detection processes, to eliminate the data modulation on the branches. These results are used to form the DD-CCRL error signal by subtracting the quadrature samples from the in-phase samples. This is also based on a decision-directed method and has the advantage of eliminating the additional noise from the tracking loop caused by data modulation. The error signal is given by

$$\begin{aligned} e(nT_b) = & - \frac{1}{2T_b}\int_0^{T_b} [C_I C_I + C_Q C_Q]\, dt \cdot \sin(\phi - \hat{\phi}) \\ & + [\omega_{cQ}(nT_b) - \omega_{sI}(nT_b)]\sin(\phi - \hat{\phi}) \\ & - [\omega_{sI}(nT_b) + \omega_{sQ}(nT_b)]\cos(\phi - \hat{\phi}) \end{aligned} \tag{6.22}$$

which is the same as for the balanced QPSK DSSS system, and 6.22 can in the same manner be simplified to

$$\begin{aligned} e(nT_b) = & - \sin(\phi - \hat{\phi}) \\ & + [\omega_{cQ}(nT_b) - \omega_{sI}(nT_b)]\sin(\phi - \hat{\phi}) \\ & - [\omega_{sI}(nT_b) + \omega_{sQ}(nT_b)]\cos(\phi - \hat{\phi}) \end{aligned} \tag{6.23}$$

where it is assumed that there is zero time shift between the incoming spreading codes and the despreading codes at the receiver. The resultant error signal is low-pass filtered and used to control the NCO to recover the quadrature carriers.

It is also important to note that the composite despreading codes C_I and C_Q are used in the DD-CCRL to despread the quadrature and in-phase branch, respectively, which is exactly opposite to the despreading and data detection processes. The reason for this is to ensure that auto correlation terms will be formed in the product with the DD-CCRL error

signal, as shown in Equation 6.22, otherwise a cross correlation term would be present in the product with the DD-CCRL error signal, resulting in a very small error signal that would jeopardize the carrier tracking process.

6.4 SPREADING CODE SYNCHRONIZATION

The majority of papers on code synchronization loops design for DSSS communication systems concentrate on non-coherent schemes employing binary spreading sequences. These loop structures comprise early and late arm structures with squaring devices which are very prone to arm imbalance effects. In this dissertation a combined coherent carrier recovery and Decision-Directed Delay-Lock-Loop (DD-DLL) synchronization scheme for complex DSSS communication systems are proposed. The novelty of the technique lies in the fact that it extends the structure proposed by de Gaudenzi et al [8] to enable synchronization of systems employing both binary and complex spreading sequences. Typical advantages include features such as less sensitivity to arm imbalance problems due to the elimination of squaring devices, improved tracking capability and simplified hardware by requiring only two correlators in stead of four in the DD-CDLL structure. The simplified loop structures are the direct result of the novel use of unique combinations of the real and imaginary parts of the spreading codes used in both the spreading, demodulation/despreading and code tracking processes and leads to the elimination of unwanted cross product interference terms when employing complex spreading sequences. The loop response is analyzed analytically and its performance verified through computer simulation when employing both binary as well as new families of complex Non-Linearly Interpolated Root-of-Unity (NLI-RU) filtered complex spreading sequences, including a subclass of Analytical Bandlimited Complex (ABC) spreading sequences [4].

6.4.1 Code Acquisition

Prior to acquisition, the unique combinations of complex spreading codes, generated at the transmitter and receiver, are not in synchronism. In order to achieve code locking, a course sliding correlation [38] is first performed on the in-phase and quadrature phase branches. The modulus of these two results are combined and provided as input to a threshold detector.

The outputs of the integrators on the in-phase and quadrature phase branches at the

receiver are given by

$$g_1(t) = \frac{1}{2T_b} d_1(t) \int_0^{T_b} C_I C_I(t - T_d)\, dt + \omega_{c_I}(t) \tag{6.24}$$

and

$$g_2(t) = \frac{1}{2T_b} d_1(t) \int_0^{T_b} C_Q C_Q(t - T_d)\, dt - \omega_{s_Q}(t), \tag{6.25}$$

respectively, as defined in Chapter 5. Assume that there is a time shift $T_d = iT_c$ between the received spreading codes and the local reference spreading codes in the receiver, where $i = 0, 1, 2, \ldots$ and T_c is one chip duration. The signals $g_1(t)$ and $g_2(t)$ are sampled-and-hold and summed. The absolute value of this summed result, illustrated in Figure 6.4, is compared with a predetermined threshold.

The output of the threshold detector controls the clock driving the complex spreading sequence generator. It controls the clock in such a way that when the threshold is not exceeded, the clock is disabled for one clock cycle at the end of the punctual spreading sequence pattern. During the initial synchronization time the coherent DD-CDLL is in an open loop free running mode. Once the threshold is exceeded, the clock is enabled and the coherent DD-CDLL is switched to a closed loop mode. The end result is that the local receiver complex spreading sequence generator will be aligned to within one chip period with the transmitted spreading sequence, yielding *code lock*.

6.4.2 Code Tracking

6.4.2.1 Balanced Complex Decision-Directed Delay-Lock-Loop

Figure 6.5 shows the block diagram for the balanced complex decision-directed DLL synchronization scheme.

The incoming signal $r(t)$ to the coherent CDLL, shown in Figure 6.5, can be modelled as

$$\begin{aligned} r(t) \quad = \quad & \sqrt{P} d(t - T_d) C_I(t - T_d) \cos(2\pi f_c t + \phi) \\ & + \sqrt{P} d(t - T_d) C_Q(t - T_d) \sin(2\pi f_c t + \phi) \\ & + n(t) \end{aligned} \tag{6.26}$$

where P is the average power of the signal, $d(t)$ is the binary data stream, $C_I(t)$ and $C_Q(t)$ is the data-synchronous in phase and quadrature phase combinations of the real and imaginary

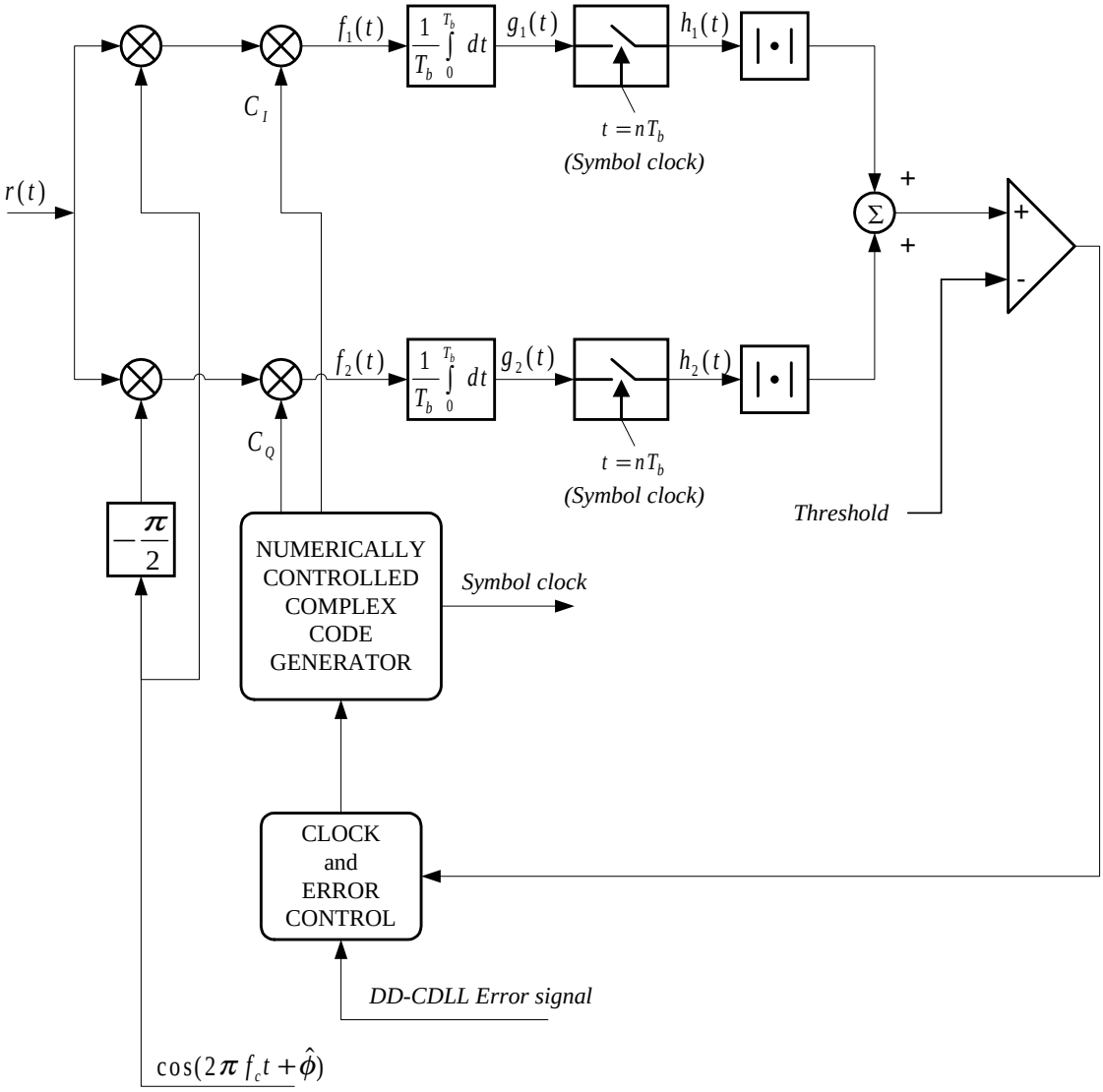

FIGURE 6.4: Block diagram of the acquisition circuitry.

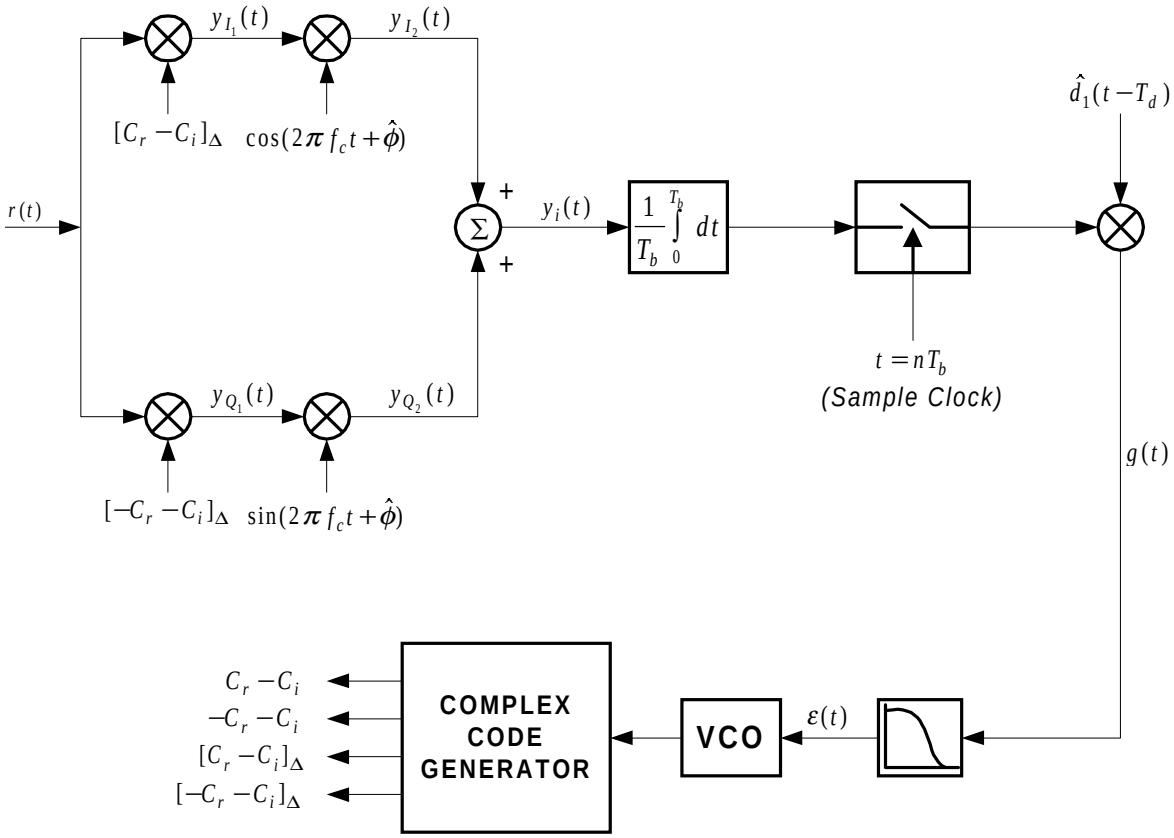

FIGURE 6.5: Block diagram of the Balanced Complex Decision-Directed Delay Lock Loop

parts of complex spreading codes, repectively. T_d is the transmission delay, f_c is the carrier frequency, ϕ is the initial carrier phase and $n(t)$ is **A**dditive **W**hite **G**aussian **N**oise (AWGN) with double-sided power spectral density (PSD) $\frac{N_0}{2}$. We also assume that

$$d(t) = \sum_{i=-\infty}^{\infty} d_i q(t - iT_b) \tag{6.27}$$

where $\{d(t)\}$ are symbols selected from the alphabet $\{-1, +1\}$, and $q(t)$ is the NRZ pulse with bit duration T_b. The spreading codes have a chip duration of T_c seconds.

The code generator produces four sets of spreading code combinations. The first two are variable delay replicas of the combinations used at the transmitter and the second two are composite signals, which can be defined as

$$C_I(t - T_d) = C_r(t - T_d) - C_i(t - T_d) \tag{6.28}$$

and

$$C_Q(t - T_d) = -C_r(t - T_d) - C_i(t - T_d) \tag{6.29}$$

$$\begin{aligned} C_{I\Delta}(t-\hat{T}_d) = [C_r(t - \hat{T}_d - \Delta) - C_i(t - \hat{T}_d - \Delta)] \\ -[C_r(t-\hat{T}_d+\Delta) - C_i(t-\hat{T}_d+\Delta)] \end{aligned} \tag{6.30}$$

and

$$\begin{aligned} C_{Q\Delta}(t - \hat{T}_d) = [-C_r(t-\hat{T}_d-\Delta) - C_i(t-\hat{T}_d-\Delta)] \\ -[-C_r(t-1\hat{T}_d+\Delta) - C_i(t-\hat{T}_d+\Delta)] \end{aligned} \tag{6.31}$$

where Δ is a fixed time shift and $\hat{T}_d$ is the estimated transmission code delay. We can now decompose the AWGN $n(t)$ in Equation (11.1) into its in-phase and quadrature components

$$n(t) = n_c(t)\cos(2\pi f_c t+\phi) - n_s(t)\sin(2\pi f_c t+\phi) \tag{6.32}$$

where $n_c(t)$ and $n_s(t)$ are two mutually independent white Gaussian processes with PSD N_0.

The incoming signal $r(t)$ is divided into an in-phase and quadrature phase branch at the input of the coherent CDLL. Firstly we consider the in-phase branch. At the output of the

first mixer, where the incoming signal is multiplied by $C_{I\Delta}(t-\hat{T}_d)$, we have

$$\begin{aligned} y_{I_1}(t) &= r(t)C_{I\Delta}(t-\hat{T}_d) \\ &= \sqrt{\frac{P}{2}}d(t-T_d)C_I(t-T_d)C_{I\Delta}(t-\hat{T}_d) \\ &\quad \cos(2\pi f_c t+\phi) \\ &+ \sqrt{\frac{P}{2}}d(t-T_d)C_Q(t-T_d)C_{I\Delta}(t-\hat{T}_d) \\ &\quad \sin(2\pi f_c t+\phi)+\omega_{cI\Delta}(t)\cos(2\pi f_c t+\phi) \\ &- \omega_{sI\Delta}(t)\sin(2\pi f_c t+\phi) \end{aligned} \tag{6.33}$$

where

$$\omega_{cI\Delta}(t) = n_c(t)C_{I\Delta}(t-\hat{T}_d) \tag{6.34}$$

and

$$\omega_{sI\Delta}(t) = n_s(t)C_{I\Delta}(t-\hat{T}_d) \tag{6.35}$$

Assume now that the recovered carrier can be represented as

$$c_1(t) = 2\cos(2\pi f_c t+\hat{\phi}) \tag{6.36}$$

where $\hat{\phi}$ is the estimated carrier phase. Thus, at the output of the second mixer we have

$$\begin{aligned} y_{I_2}(t) &= \sqrt{\frac{P}{2}}d(t-T_d)C_I(t-T_d)C_{I\Delta}(t-\hat{T}_d) \\ &\quad [\cos(4\pi f_c t+\phi+\hat{\phi})+\cos(\phi-\hat{\phi})] \\ &+ \sqrt{\frac{P}{2}}d(t-T_d)C_Q(t-T_d)C_{I\Delta}(t-\hat{T}_d) \\ &\quad [\sin(4\pi f_c t+\phi+\hat{\phi})+\sin(\phi-\hat{\phi})] \\ &+ \omega_{cI\Delta}(t)[\cos(4\pi f_c t+\phi+\hat{\phi})+\cos(\phi-\hat{\phi})] \\ &- \omega_{sI\Delta}(t)[\sin(4\pi f_c t+\phi+\hat{\phi}) \\ &+ \sin(\phi-\hat{\phi})] \end{aligned} \tag{6.37}$$

In the same way we can determine the output of the second mixer of the quadrature phase

branch as

$$\begin{aligned} y_{Q_2}(t) &= \sqrt{\frac{P}{2}} d(t-T_d) C_I(t-T_d) C_{Q\Delta}(t-\hat{T}_d) \\ &\quad [\sin(4\pi f_c t + \phi + \hat{\phi}) - \sin(\phi - \hat{\phi})] \\ &+ \sqrt{\frac{P}{2}} d(t-T_d) C_Q(t-T_d) C_{Q\Delta}(t-\hat{T}_d) \\ &\quad [-\cos(4\pi f_c t + \phi + \hat{\phi}) + \cos(\phi - \hat{\phi})] \\ &+ \omega_{cQ\Delta}(t)[\sin(4\pi f_c t + \phi + \hat{\phi}) - \sin(\phi - \hat{\phi})] \\ &- \omega_{sQ\Delta}(t)[-\cos(4\pi f_c t + \phi + \hat{\phi}) \\ &+ \cos(\phi - \hat{\phi})] \end{aligned} \tag{6.38}$$

After summation of these two branches, and the integration over one bit period ($T_b = LT_c$), where L is the complex spreading sequence length, we obtain the following signal

$$\begin{aligned} y_i(t) &= \sqrt{2P}\frac{1}{T_b}\int_0^{Tb} d(t-T_d)\{C_I(t-T_d)C_{I\Delta}(t-\hat{T}_d) \\ &+ C_Q(t-T_d)C_{Q\Delta}(t-\hat{T}_d)\}\cos(\phi-\hat{\phi})dt \\ &+ \sqrt{2P}\frac{1}{T_b}\int_0^{Tb} d(t-T_d)\{C_Q(t-T_d)C_{I\Delta}(t-\hat{T}_d) \\ &- C_I(t-T_d)C_{Q\Delta}(t-\hat{T}_d)\}\sin(\phi-\hat{\phi})dt \\ &+ \frac{1}{T_b}\int_0^{Tb}\{\omega_{cI\Delta}(t)-\omega_{sQ\Delta}(t)\}\cos(\phi-\hat{\phi})dt \\ &- \frac{1}{T_b}\int_0^{Tb}\{\omega_{sI\Delta}(t)+\omega_{cQ\Delta}(t)\}\sin(\phi-\hat{\phi})dt \end{aligned} \tag{6.39}$$

The unique combinations of the real and imaginary parts of the complex spreading sequence, at the transmitter and receiver, as well as the unique structure of the system, are responsible for the required output signal. This output signal is without any cross terms between the real and imaginary parts of the complex spreading sequence, which will induce a lot of code noise into the system.

The following two terms from equation (6.39) can be simplified as follows

$$\begin{aligned} & C_I(t-T_d)C_{I\Delta}(t-\hat{T}_d) + C_Q(t-T_d)C_{Q\Delta}(t-\hat{T}_d) \\ = \; & 2C_r(t-T_d)C_r(t-\hat{T}_d-\Delta) \\ - \; & 2C_r(t-T_d)C_r(t-\hat{T}_d+\Delta) + 2C_i(t-T_d) \\ & C_i(t-\hat{T}_d-\Delta) - 2C_i(t-T_d)C_i(t-\hat{T}_d+\Delta) \end{aligned} \tag{6.40}$$

and by inspection

$$\begin{aligned} & C_Q(t-T_d)C_{I\Delta}(t-\hat{T}_d) \\ & -C_I(t-T_d)C_{Q\Delta}(t-\hat{T}_d) = 0 \end{aligned} \tag{6.41}$$

Using equations (6.40) and (6.41) to replace the terms in equation (6.39), we get

$$\begin{aligned} y_i(t) &= \sqrt{2P}\frac{1}{T_b}\int_0^{Tb} d(t-T_d)[2C_r(t-T_d) \\ &\quad C_r(t-\hat{T}_d-\Delta)-2C_r(t-T_d)C_r(t-\hat{T}_d+\Delta) \\ &+ 2C_i(t-T_d)C_i(t-\hat{T}_d-\Delta)-2C_i(t-T_d) \\ &\quad C_i(t-\hat{T}_d+\Delta)]\cos(\phi-\hat{\phi})dt+\omega_\Delta(t) \end{aligned} \tag{6.42}$$

where

$$\begin{aligned} \omega_\Delta(t) &= \frac{1}{T_b}\int_0^{Tb}\{[\omega_{cI\Delta}(t)-\omega_{sQ\Delta}(t)]\cos(\phi-\hat{\phi}) \\ &- [\omega_{sI\Delta}(t)+\omega_{cQ\Delta}(t)]\sin(\phi-\hat{\phi})\}dt \end{aligned} \tag{6.43}$$

If all the details relative to the data demodulation process which is performed by successive despreading, integrate-and-dump and sample-and-hold operations on the received signal, are skipped $\hat{d}(t-T_d)$ may be assumed as the estimated data stream. By using $\hat{d}(t-T_d)$ we have

$$\begin{aligned} g(t) &= \sum_{i=-\infty}^{\infty}\{\sqrt{2P}\frac{1}{T_b}\int_0^{Tb} d(t-T_d)\hat{d}(t-T_d) \\ &\quad [2C_r(t-T_d)C_r(t-\hat{T}_d-\Delta) \\ &- 2C_r(t-T_d)C_r(t-\hat{T}_d+\Delta) \\ &+ 2C_i(t-T_d)C_i(t-\hat{T}_d-\Delta) \\ &- 2C_i(t-T_d)C_i(t-\hat{T}_d+\Delta)]\cos(\phi-\hat{\phi})dt \\ &+ \omega_\Delta(t)\}h(t-iT_b) \end{aligned} \tag{6.44}$$

To find the final expression of the open-loop error signal $e(t)$ as input signal to the VCO, which drives the complex code generator at the receiver, after the loop filter $f(t)$, we can retain only the DC component of the error signal in equation (6.44) and also neglect the self-noise contribution.

By using $P_e(\varepsilon)$, the BER of the BPSK data demodulator can be determined, when a fixed normalized code timing error ε is present, namely

$$\varepsilon \equiv \frac{T_d-\hat{T}_d}{T_c} \tag{6.45}$$

the DC component can be defined as

$$\begin{aligned} M &= \langle E\{d(t-T_d)\hat{d}(t-T_d)\}\rangle \\ &= 1-2P_e \\ &= 1-2Q[R_c(\varepsilon T_c)\sqrt{\frac{2E_b}{N_0}}\cos(\phi-\hat{\phi})] \end{aligned} \tag{6.46}$$

where

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{(\frac{-y^2}{2})}dy \tag{6.47}$$

The normalised auto-correlation peak $R_c(\varepsilon T_c)$ is shown in Figure 6.6. The DC value of $d(t-T_d)\hat{d}(t-T_d)$ would be one in the absence of bit errors. Since the BER is P_e, one regenerated bit every $\frac{1}{P_e}$ bits in $\hat{d}(t)$ will have the incorrect sign. On time averaging the product, $d(t-T_d)\hat{d}(t-T_d)$, the average amplitude is in effect reduced by the amount $2P_e$. Thus $g(t)$ can be written as

$$\begin{aligned} g(t) &= \{\sqrt{2P}\frac{1}{T_b}\int_0^{Tb}(1-P_e)X(t,T_d,\Delta)\cos(\phi-\hat{\phi})dt\} \\ &\quad \otimes f(t) + \omega_{\Delta}(t)\hat{d}(t)\otimes f(t) \end{aligned} \tag{6.48}$$

where

$$\begin{aligned} X(t,T_d,\Delta) &= 2C_r(t-T_d)C_r(t-\hat{T}_d-\Delta) \\ &- 2C_r(t-T_d)C_r(t-\hat{T}_d+\Delta) \\ &+ 2C_i(t-T_d)C_i(t-\hat{T}_d-\Delta) \\ &- 2C_i(t-T_d)C_i(t-\hat{T}_d+\Delta) \end{aligned} \tag{6.49}$$

Define the average autocorrelation function as

$$\begin{aligned} R_c(\tau) &\equiv \frac{1}{NT_c}\int_0^{NT_c} c(t)c(t+\tau)d\tau \\ &= \frac{1}{T_b}\int_0^{T_b} c(t)c(t+\tau)d\tau \end{aligned} \tag{6.50}$$

Thus,

$$\frac{1}{T_b}\int_0^{T_b} X(t,T_d,\Delta)dt = R_c(-\Delta+\varepsilon T_c) - R_c(\Delta+\varepsilon T_c) \tag{6.51}$$

where

$$R_c(-\Delta+\varepsilon T_c) \equiv R_r(-\Delta+\varepsilon T_c) + R_i(-\Delta+\varepsilon T_c) \tag{6.52}$$

and

$$R_c(\Delta+\varepsilon T_c) \equiv R_r(\Delta+\varepsilon T_c) + R_i(\Delta+\varepsilon T_c) \tag{6.53}$$

The final error signal, $e(t)$, is therefore

$$\begin{aligned} e(t) &= \sqrt{2P}(1-P_e)[R_c(-\Delta+\varepsilon T_c)-R_c(\Delta+\varepsilon T_c)] \\ &\quad \cos(\phi-\hat{\phi})\} \otimes f(t)+\omega_\Delta(t)\hat{d}(t)\otimes f(t) \end{aligned} \tag{6.54}$$

The error function $V(\varepsilon)$ can be defined as

$$V(\varepsilon) = R_c(-\Delta+\varepsilon T_c) - R_c(\Delta+\varepsilon T_c) \tag{6.55}$$

and the normalised error function is depicted in Figure 6.7. By defining the following

$$N(t) \equiv \omega_\Delta(t)\hat{d}(t) \tag{6.56}$$

$$\eta \equiv \frac{d}{d\varepsilon}\left[R_c(-\Delta+\varepsilon T_c) - R_c(\Delta+\varepsilon T_c)\right] \mid \varepsilon = 0 \tag{6.57}$$

$$M_0 \equiv M(0) = 1 - 2Q\left[\sqrt{\frac{2E_b}{N_0}}\cos(\phi-\hat{\phi})\right] \tag{6.58}$$

and

$$S(\varepsilon) \equiv \frac{1}{\eta M_0}\left[R_c(-\Delta+\varepsilon T_c) - R_c(\Delta+\varepsilon T_c)\right] M(\varepsilon) \tag{6.59}$$

the error signal $e(t)$ can be written as

$$\begin{aligned} e(t) &= \sqrt{2P}\eta M_0 \cos(\phi - \hat{\phi}) \\ &\quad \left[S(\varepsilon) + \frac{N(t)}{\sqrt{2P}\eta M_0 \cos(\phi - \hat{\phi})} \right] \otimes f(t) \end{aligned} \tag{6.60}$$

The normalised error characteristic (NEC), $S(\varepsilon)$, of the loop is shown in Figure (6.7), for different values of $\frac{E_b}{N_0}$.

The stochastic differential equation which describes the dynamic behaviour is given by

$$\begin{aligned} \frac{d\varepsilon(t)}{dt} &= Ke(t) \\ &= K\sqrt{2P}\eta M_0 \cos(\phi - \hat{\phi}) \\ &\quad \left[S(\varepsilon) + \frac{N(t)}{\sqrt{2P}\eta M_0 \cos(\phi - \hat{\phi})} \right] \otimes f(t) \end{aligned} \tag{6.61}$$

where K denotes the voltage controlled oscillator (VCO) sensitivity. In the following derivations and expressions the assumption is made that the recovered carrier phase error is negligible, i.e. $\phi - \hat{\phi} \approx 0$, and thus $\cos(\phi - \hat{\phi}) \approx 1$.

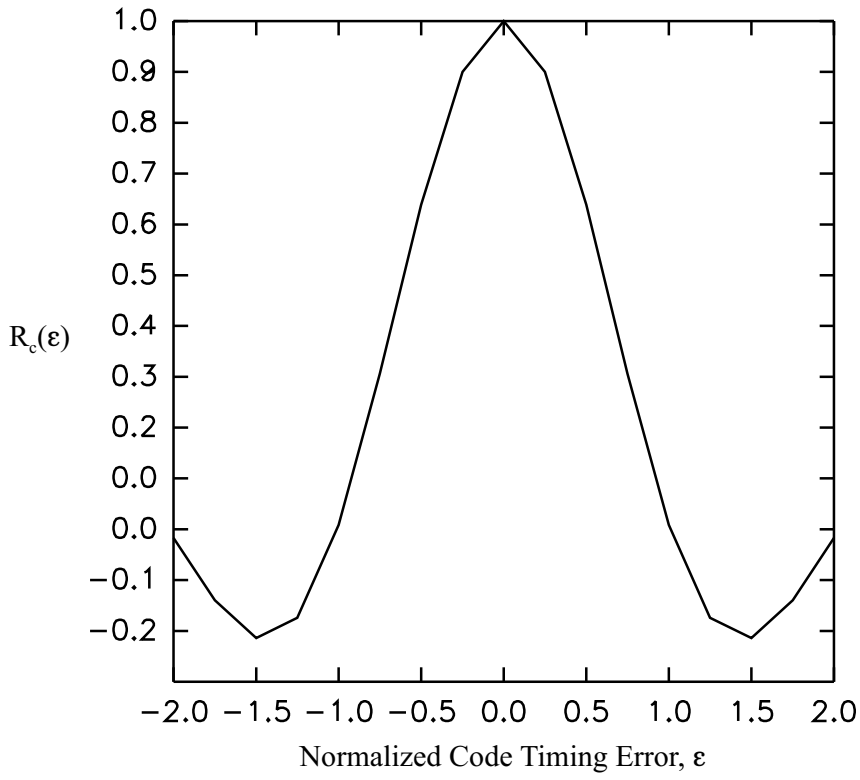

FIGURE 6.6: Normalised autocorrelation peak, $R_c(\varepsilon T_c)$

In the presence of a high signal-to-noise ratio in the loop, $S(\varepsilon)$ can be replaced by its linear equivalent in the neighborhood of $\varepsilon = 0$ and equation (6.61) becomes

$$\begin{aligned}\frac{d\varepsilon(t)}{dt} &= Ke(t) \\ &= K\sqrt{2P}\eta M_0 \cos(\phi - \hat{\phi}) \\ &\quad \left[\varepsilon + \frac{N(t)}{\sqrt{2P}\eta M_0 \cos(\phi - \hat{\phi})}\right] \otimes f(t)\end{aligned} \tag{6.62}$$

The loop transfer function $H(s)$ is defined in [39] as

$$H(s) = \frac{K\sqrt{2P}\eta M_0 F(s)}{s + K\sqrt{2P}\eta M_0 F(s)} \tag{6.63}$$

Assume that a second order passive low pass loop filter of the form

$$F(s) = \frac{s\tau + 1}{s(\tau_1 + \tau_2) + 1)} \tag{6.64}$$

is used. Then the loop transfer function of the tracking loop becomes

$$H(s) = \frac{K\sqrt{2P}\eta M_0 \frac{s\tau_1 + 1}{\tau_1 + \tau_2}}{s^2 + s\frac{1 + K\sqrt{2P}\eta M_0 \tau_2}{\tau_1 + \tau_2} + \frac{1 + K\sqrt{2P}\eta M_0}{\tau_1 + \tau_2}} \tag{6.65}$$

From this expression it can be shown that the natural frequency of the loop, ω_n, is

$$\omega_n = (\frac{K\sqrt{2P}\eta M_0}{\tau_1 + \tau_2})^{\frac{1}{2}} \tag{6.66}$$

and the damping factor, ζ

$$\zeta = \frac{1}{2}(\frac{K\sqrt{2P}\eta M_0}{\tau_1 + \tau_2})^{\frac{1}{2}}(\tau_2 + \frac{1}{K\sqrt{2P}\eta M_0}) \tag{6.67}$$

The same mathematical derivation can be followed for the dual channel QPSK as for the case of the balanced QPSK configuration, as described above. The decision-directed complex delay-locked loop (DD-CDLL) for the dual channel QPSK configuration is depicted in Figure 6.9.

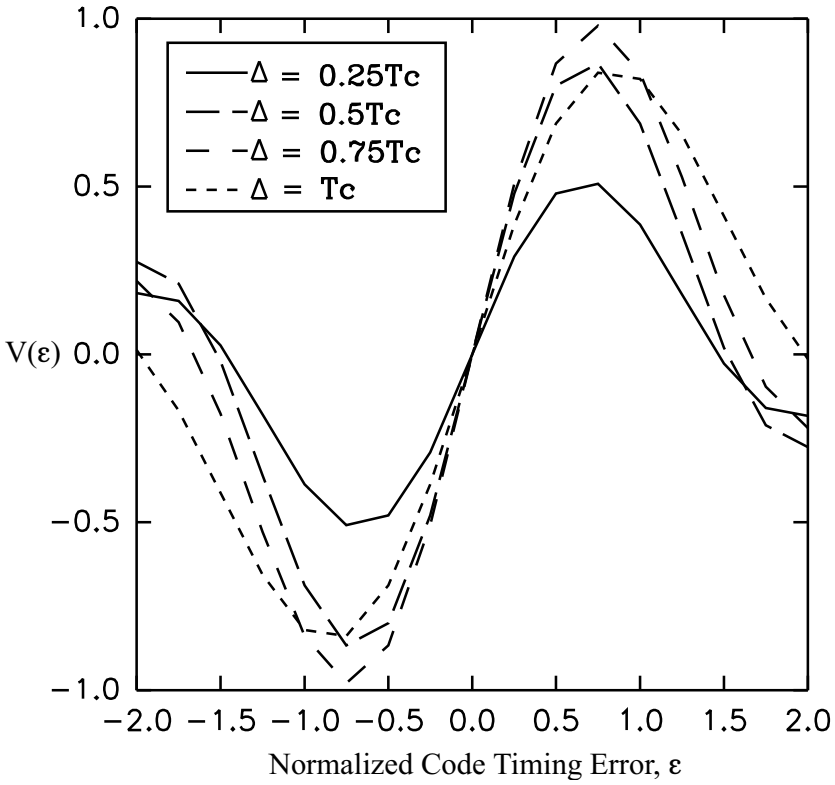

FIGURE 6.7: Normalised error characteristic S-curve for the CDLL

6.5 TIMING RECOVERY

The Decision-Directed Delay-Lock-Loop (DD-DLL) is used, as described in the previous sections, to synchronize the complex spreading sequences, used at the DSSS transmitter and receiver, within one chip period with the accuracy of fractions of a sample. By controlling the global system clock of the receiver by means of the DD-CDLL error signal, code tracking as well as symbol timing are achieved. A complete complex spreading sequence length fits one symbol time period and thus no additional symbol timing recovery is needed.

6.6 CARRIER PHASE AND CODE SYNCHRONISATION: CONCLUSION

Code tracking is performed by means of the coherent Decision-Directed Delay-Lock-Loop (DD-DLL), while the coherent DD-CCRL is responsible for carrier phase tracking. These two synchronisation loops are fully integrated and functions as one combined synchronisation loop. These two interconnected synchronisation loops use mutual synchronisation estimates to perform near optimum carrier phase and code tracking (the

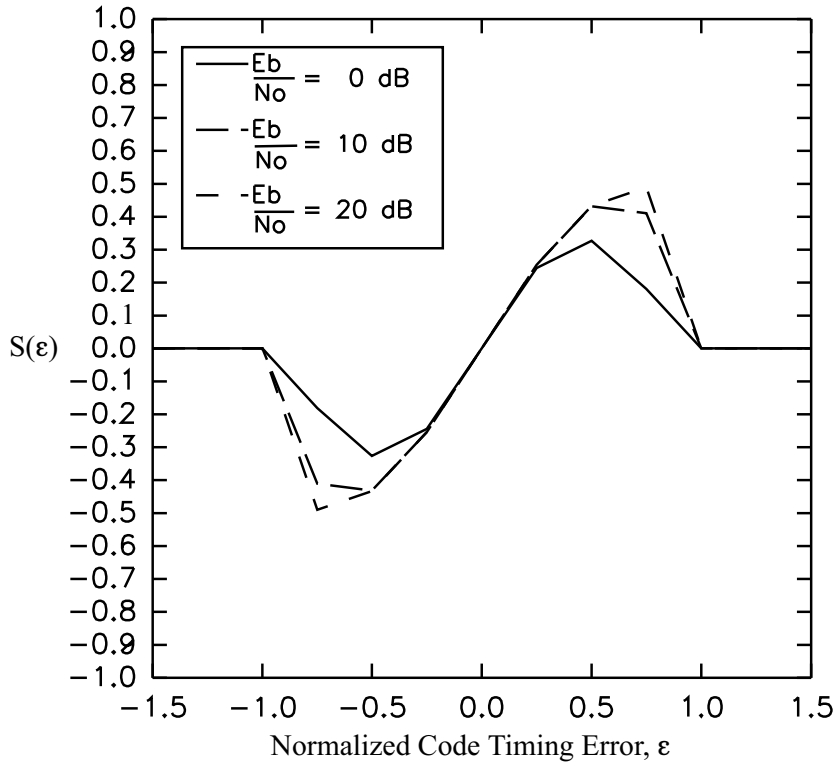

FIGURE 6.8: Normalized error characteristic S-curve for the CDLL for different E_b/N_0 values for $\triangle = 0.75T_c$

optimality of this principle is explained in [21] p.333). The tracking of the carrier phase and the spreading sequence are dependent on each other. This concept is illustrated in Figure 6.10, where the x-axis represents the code timing error in terms of samples, the y-axis represents the carrier phase error and the periodic auto-correlation (PAC) is plotted on the z-axis. A maximum optimum auto-correlation is only obtained with a zero code offset and multiples of 180^o of the carrier phase error. A similar result has been obtained from measurements on the hardware prototype of the DSSS system in Chapter 10 - refer Figures 10.21 and 10.22. It is the function of the combined synchronisation loop to maintain the receiver at this optimum operating point.

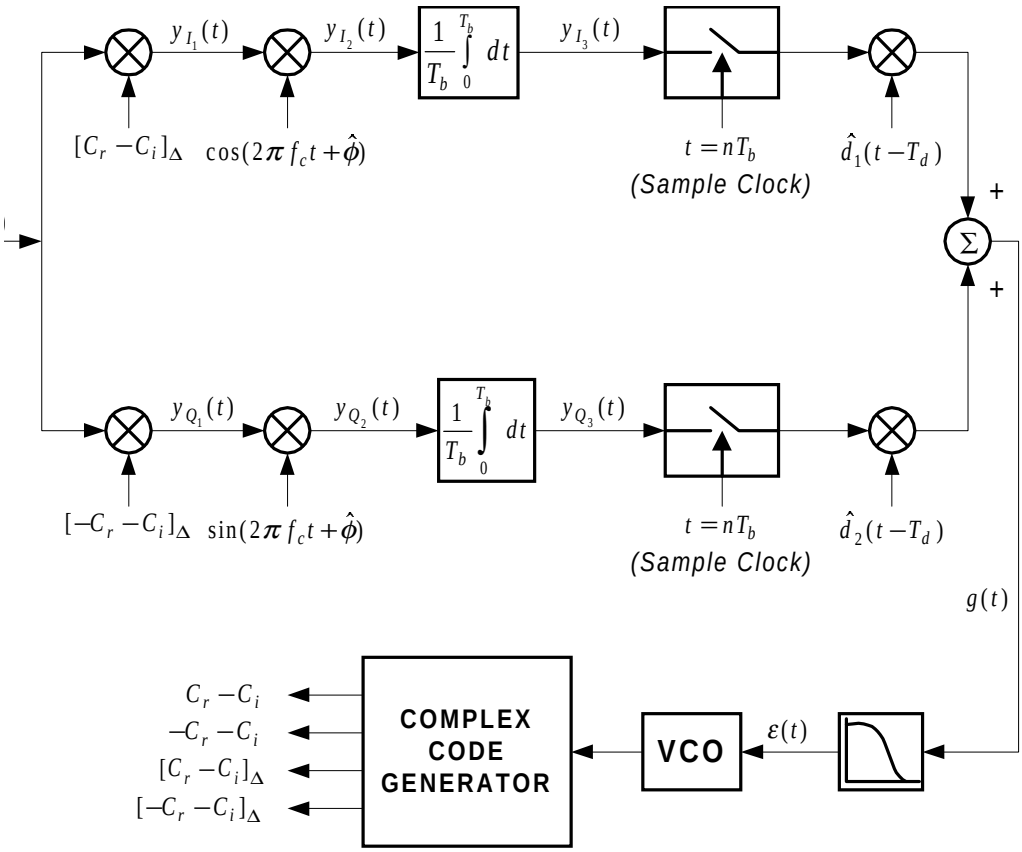

FIGURE 6.9: Block diagram of the Balanced Complex Decision-Directed Delay Lock Loop

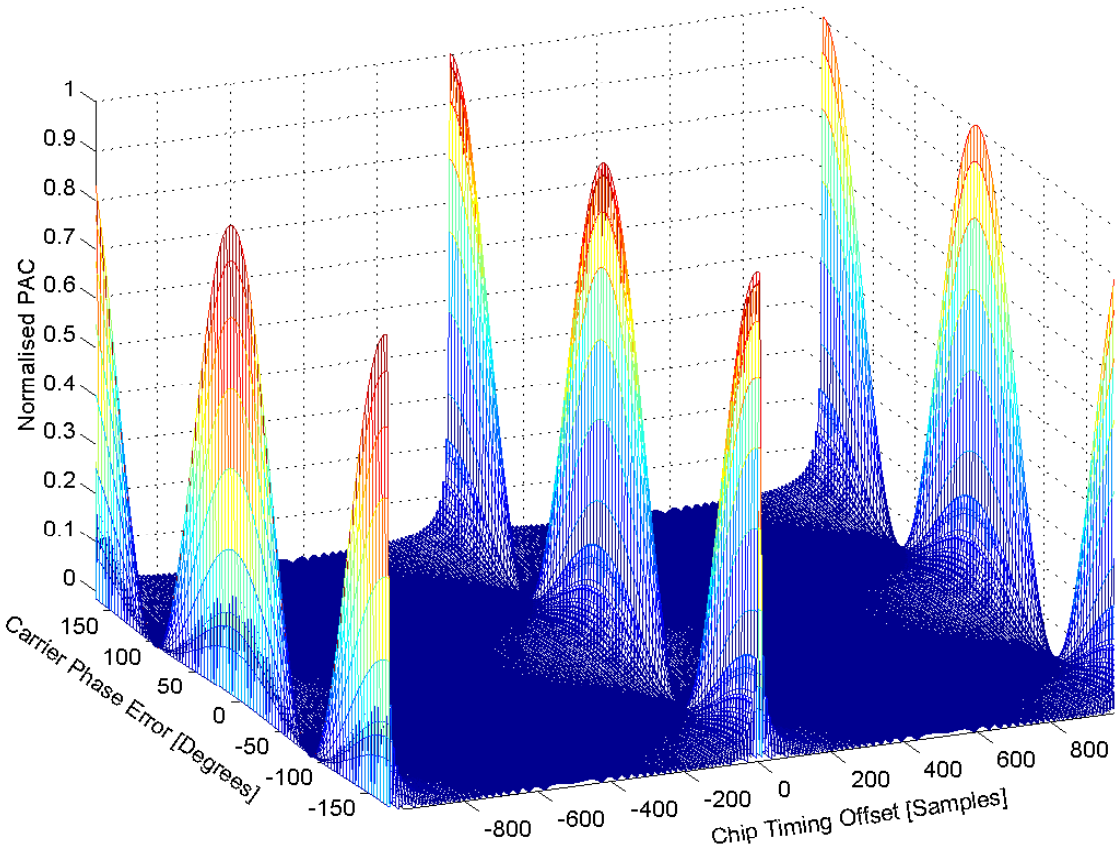

FIGURE 6.10: Illustration of the combination of carrier phase and chip timing synchronisation

PART III

SYSTEM SIMULATION

CHAPTER SEVEN

SIMULATION OF THE DSSS TRANSMITTER

7.1 INTRODUCTION AND DESCRIPTION

Simulation of the complete complex DSSS communication system, prior to hardware implementation, in order to evaluate and verify correctness of the theoretical design, is absolutely essential and of inestimable value during the realisation phases of the project. To enhance the operation of the overall system, modifications of the structures as well as fine tuning of certain parameters can be achieved with relatively ease using the simulation platform.

The complete DSSS system employing complex spreading sequences, designed and analyzed in Chapters 4, 5 and 6, was simulated in C++. This chapter presents the results obtained for the transmitter part. Figure 7.1 shows the block diagram of the complete simulation setup. The complete setup consists of a data source supplying random bipolar data, a DSSS modulator that spreads this data with a complex spreading sequence, an AWGN source that provides noise samples to be added to the output of the modulator, a DSSS demodulator, responsible for the demodulation and despreading of the data signal and a BER meter to measure the bit error performance of the system. The spreading sequence length, L, the prime value, r, and samples-per-symbol, sps, are parameters that can be adjusted at the DSSS modulator and demodulator, while the average, μ, and the variance, σ^2, are adjustable parameters in the AWGN source. The last two parameters are used to calibrate the AWGN source to ensure the correct E_b/N_o value required to measure the bit error performance of the system.

The simulated DSSS transmitter is illustrated in Figure 7.2. The results presented are for

the balanced as well as the dual channel QPSK configurations. The results presented show the temporal characteristics (time signals) as well as the the corresponding frequency spectra at different points in the transmitter.

7.2 SIMULATION RESULTS AND DISCUSSION

In this simulation complex spreading sequences were used as discussed in Chapter 3. The real and imaginary parts of a DSB complex spreading sequence, with a length of 121, are shown in Figure 7.3 in (a) and (b), respectively. The unique derived combinations of the real and imaginary parts of the CSS, $C_r - C_i$ and $-C_r - C_i$, discussed previously, are shown in Figure 7.4 in (a) and (b), respectively, with a length of $L = 121$. Figure 7.5, (a) and (b), presents the real and imaginary parts of a SSB CSS, respectively, while Figure 7.6, (a) and (b), presents the unique combinations of the real and imaginary parts of the SSB CSS, $C_r - C_i$ and $-C_r - C_i$, respectively. Both cases are for a spreading sequence length of 121. All of these sequences in Figures 7.3 to 7.6 are filtered by interpolating on the unit circle, as described in [10].

These unique combinations of the real and imaginary parts of the CSS are used in the transmitter for spreading the data signals on the in-phase and quadrature phase branches. The DSB CSS are used for spreading in both the balanced QPSK and normal dual channel QPSK configuration, while the SSB CSS are used only in the balanced QPSK configuration to produce a SSB transmitter output signal. Figure 7.7 shows the in-phase and quadrature phase branch signals in a balanced QPSK configuration spreaded with the unique combinations C_1 and C_2 of the DSB CSS, respectively. Figure 7.8 shows the same two branch signals where the data are spreaded with the unique combinations C_1 and C_2 of the SSB CSS, respectively. Figures 7.9 and 7.10 show the PSD of the spreaded branch signals for the DSB CSS C_1 and C_2 respectively, while Figures 7.11 and 7.12 depict the PSD for same two branch signals for the case of SSB CSS. In Figures 7.13 and 7.14 the time signals of the spreaded branch signals, modulated onto the quadrature carrier, are shown for the DSB and SSB CSS, respectively, while Figures 7.15, 7.16, 7.17 and 7.18 show the PSD of these signals. The final output signal of the transmitter, when using DSB CSS for spreading, is illustrated in Figure 7.19. Only one sideband remains, compared to the DSB case in Figure 7.19, when the SSB CSS are used for spreading on the two branch signals, and is presented in Figure 7.20. In the case

of SSB CSS spreading, the spectra on the two quadrature carriers, are DSB but produces a SSB output signal when they are added. This is because the one branch signal is the Hilbert transform of the other and thus produces a SSB output signal when they are summed.

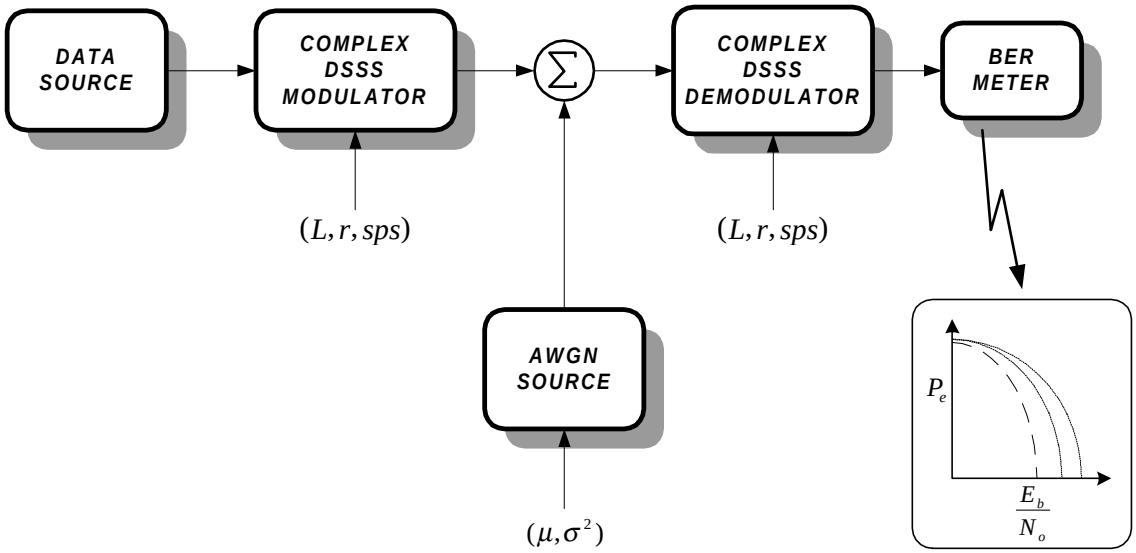

FIGURE 7.1: Block diagram of the complete simulation setup

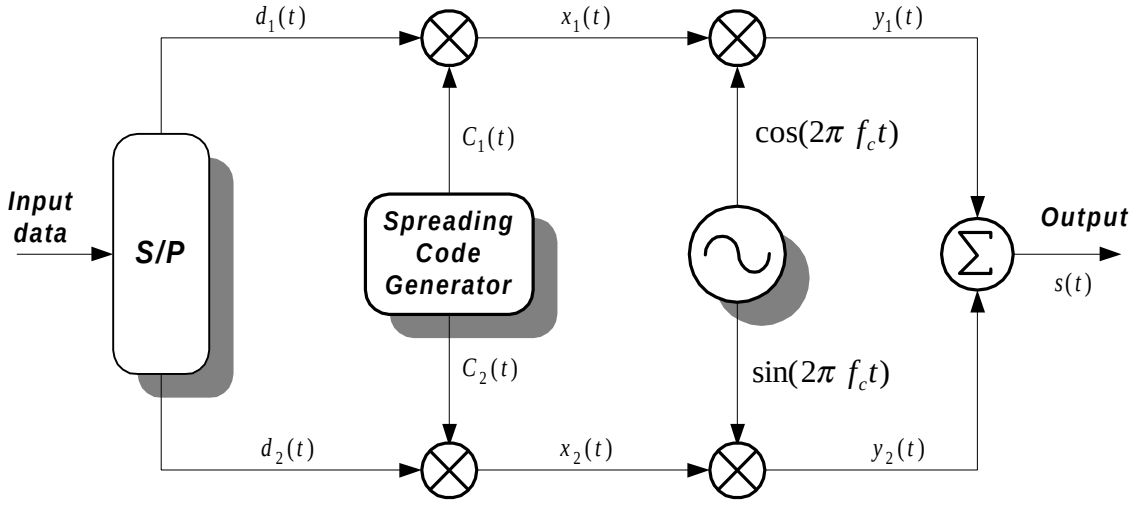

FIGURE 7.2: Block diagram of the transmitter structure used in the simulation

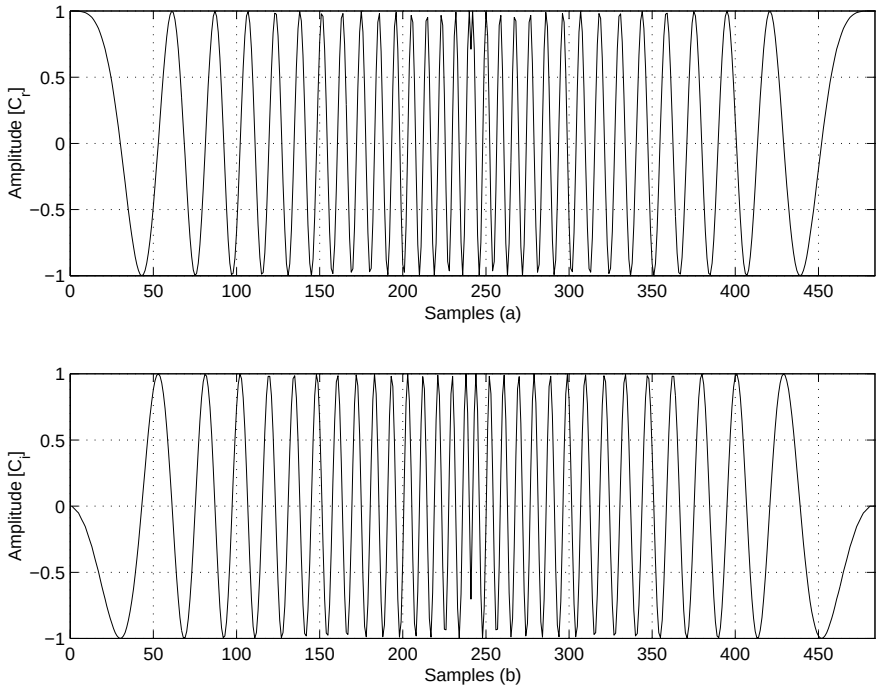

FIGURE 7.3: Real part of the DSB CSS in (a) and imaginary part of the DSB CSS in (b) with L=121, sps=4 and r=1

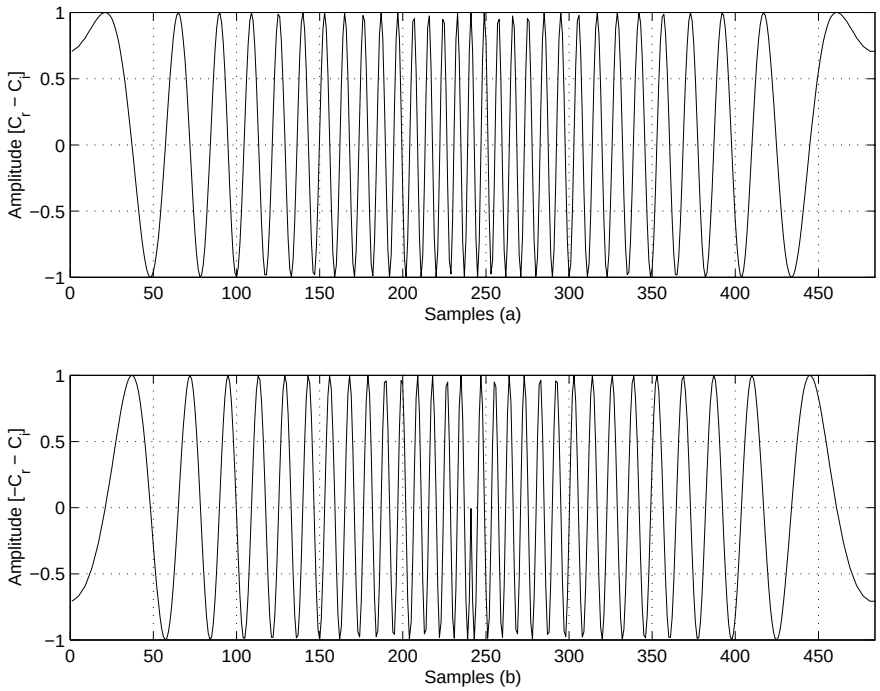

FIGURE 7.4: Unique combinations of the real and imaginary parts of the DSB CSS. $[C_r - C_i]$ in (a) and $[-C_r - C_i]$ in (b) with L=121, sps=4 and r=1

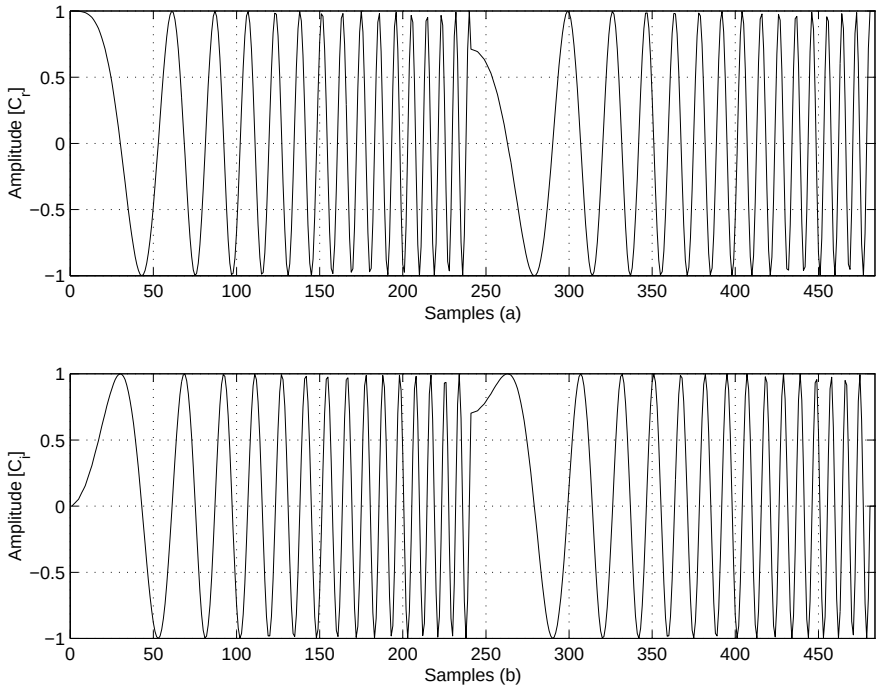

FIGURE 7.5: Real part of the SSB CSS in (a) and imaginary part of the SSB CSS in (b) with L=121, sps=4 and r=1

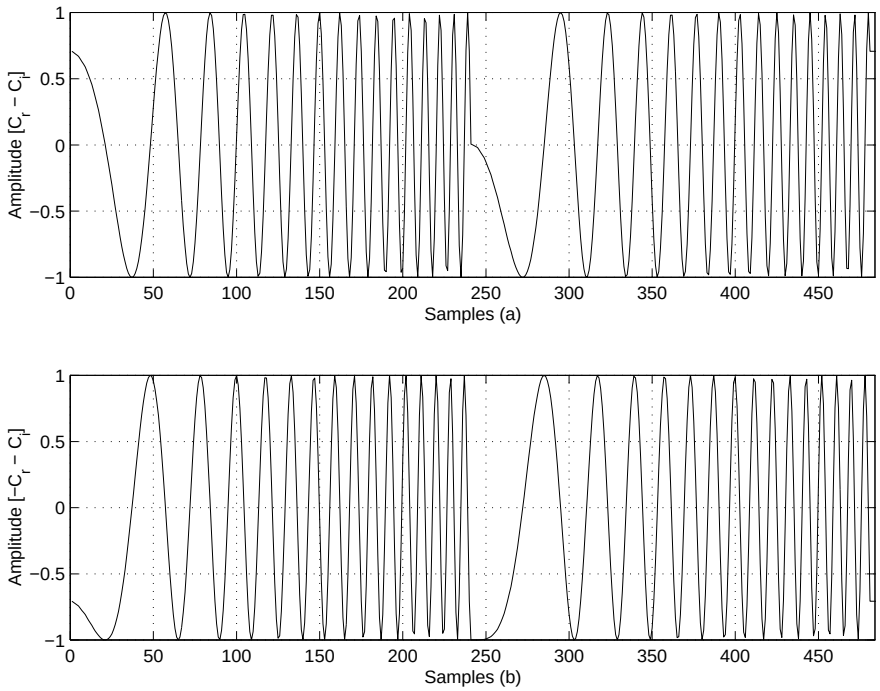

FIGURE 7.6: Unique combinations of the real and imaginary parts of the SSB CSS. $[C_r - C_i]$ in (a) and $[-C_r - C_i]$ in (b) with L=121, sps=4 and r=1

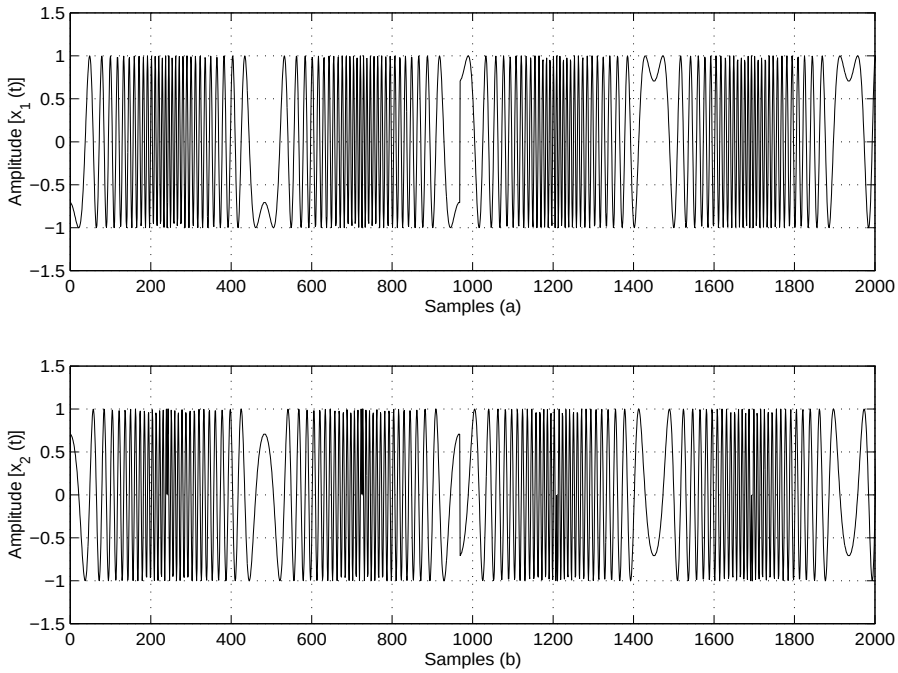

FIGURE 7.7: Data stream on in-phase branch spreaded with DSB CSS combination: $[C_r - C_i]$ in (a) and data stream on quadrature-phase branch spreaded with DSB CSS combination: $[C_r - C_i]$ in (b). (L=121, sps=4 and r=1)

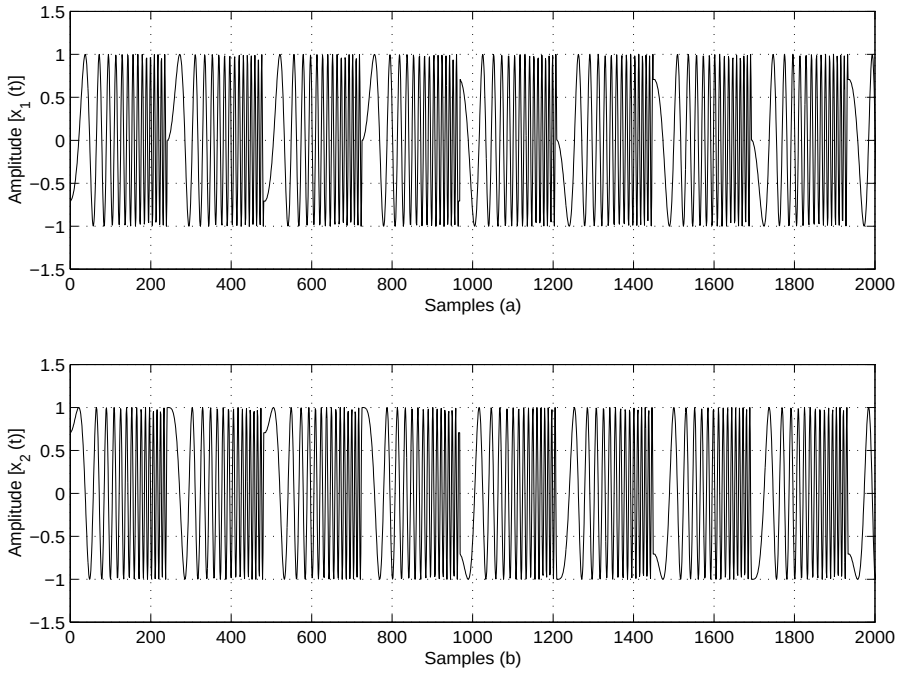

FIGURE 7.8: Data stream on in-phase branch spreaded with SSB CSS combination: $[C_r - C_i]$ in (a) and data stream on quadrature-phase branch spreaded with SSB CSS combination: $[C_r - C_i]$ in (b). (L=121, sps=4 and r=1).

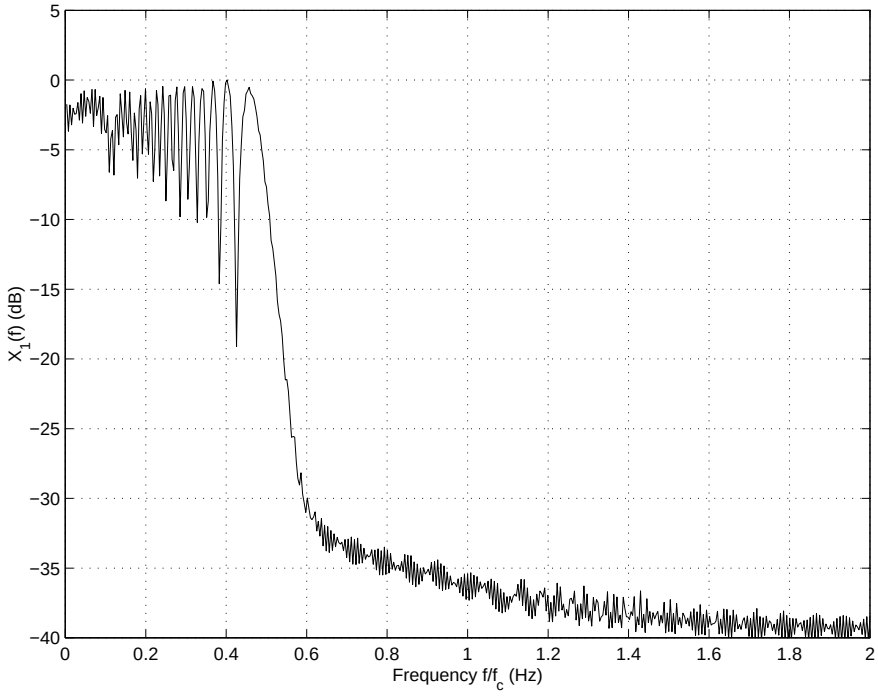

FIGURE 7.9: PSD of the in-phase branch at the transmitter after spreading of the data signal with the DSB complex unique combination spreading code C_1 (L=121,sps=4,r=1).

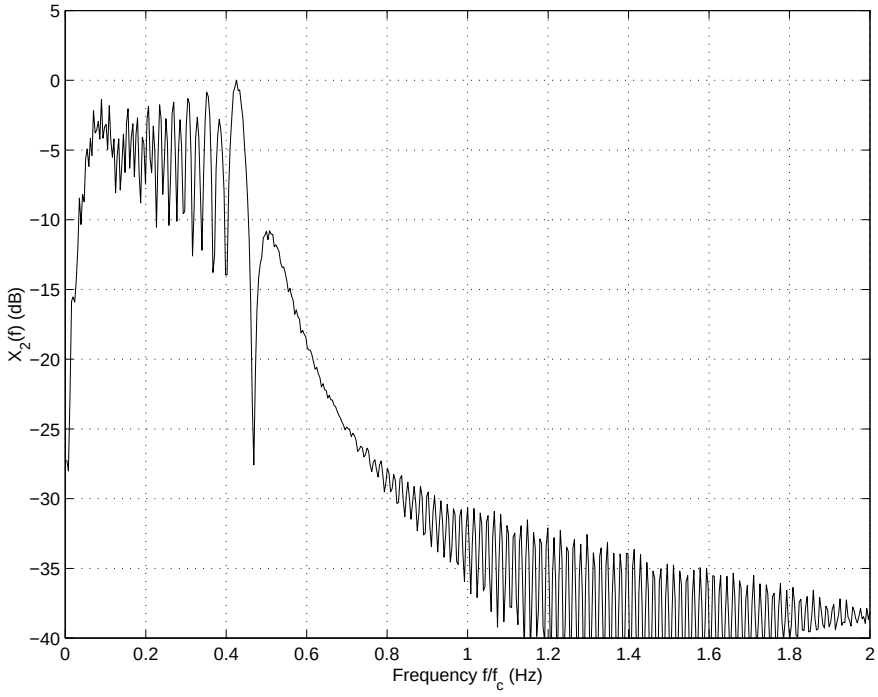

FIGURE 7.10: PSD of the quadrature-phase branch at the transmitter after spreading of the data signal with the DSB complex unique combination spreading code C_2 (L=121,sps=4,r=1).

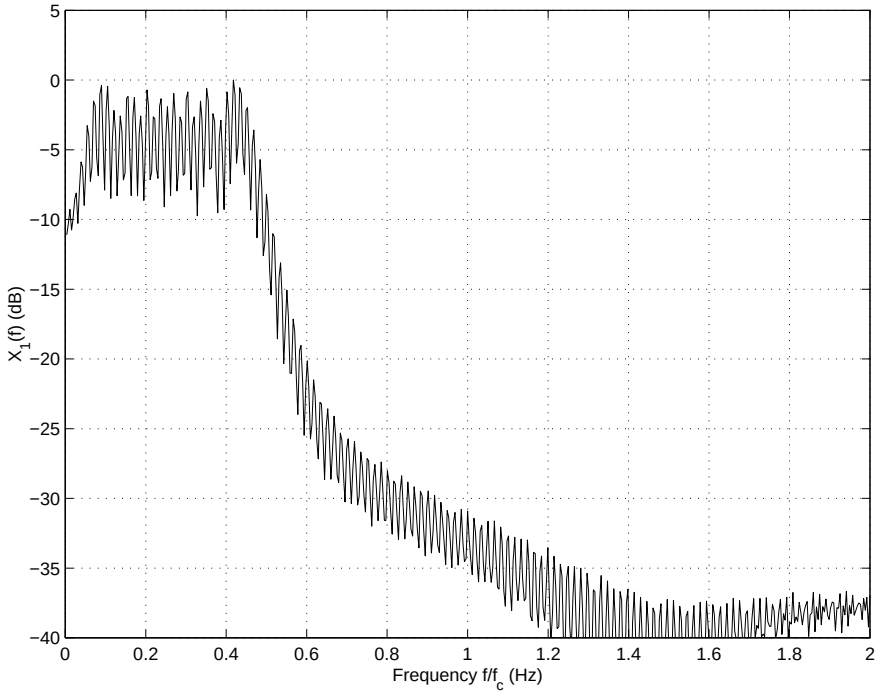

FIGURE 7.11: PSD of the in-phase branch at the transmitter after spreading of the data signal with the SSB complex unique combination spreading code C_1 (L=121,sps=4,r=1).

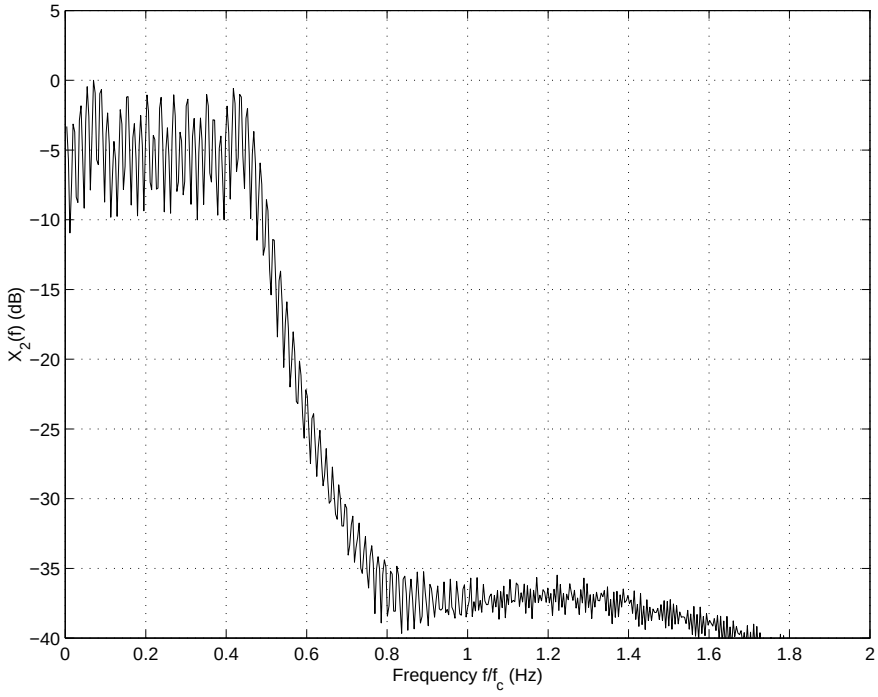

FIGURE 7.12: PSD of the quadrature-phase branch at the transmitter after spreading of the data signal with the SSB complex unique combination spreading code C_2 (L=121,sps=4,r=1).

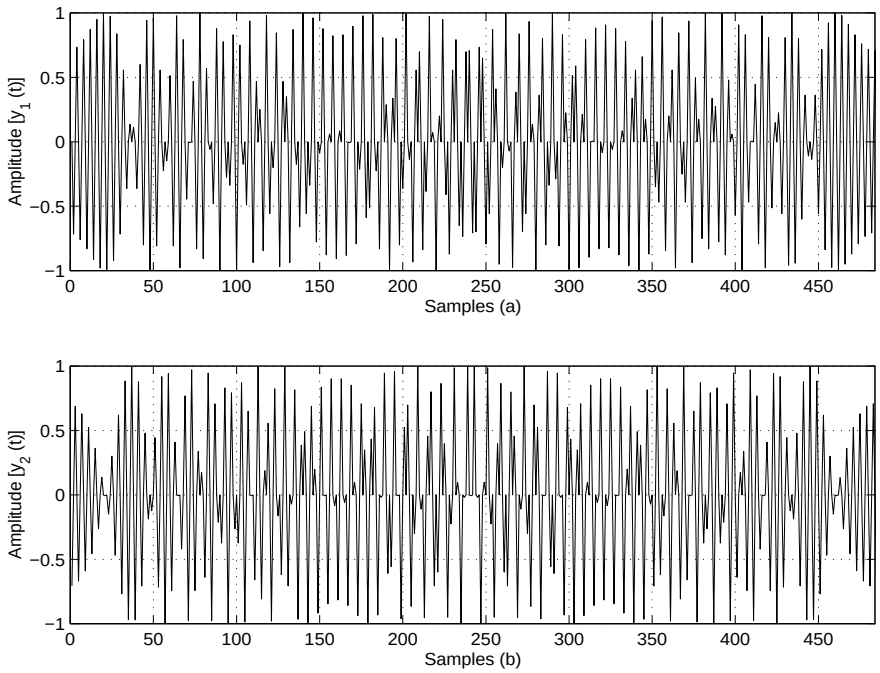

FIGURE 7.13: In-phase branch in (a) and quadrature phase branch in (b) at the transmitter after modulation of the DSB spreaded data signal onto the cosine and sine carriers, respectively (L=121,sps=4,r=1).

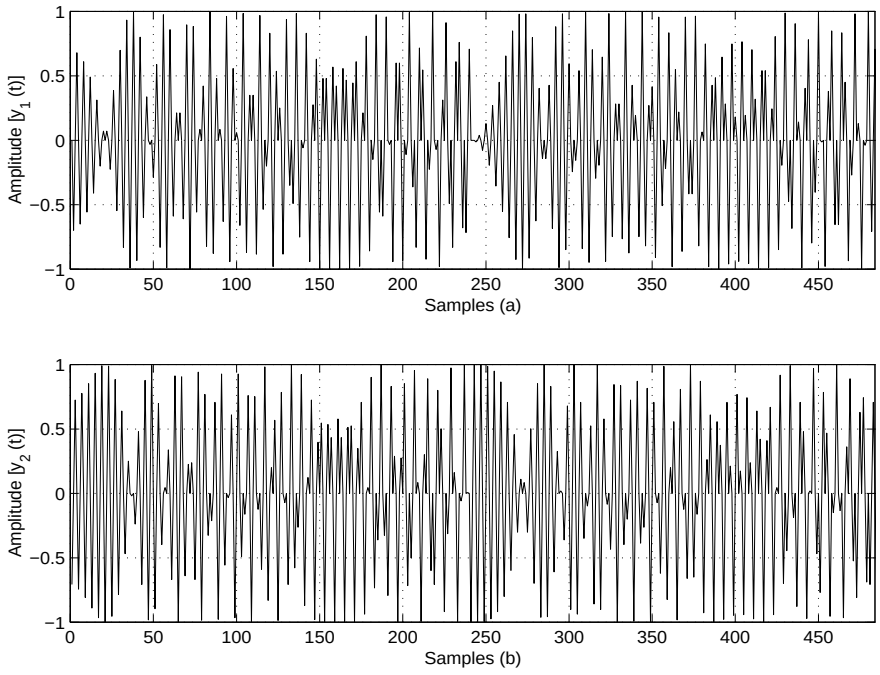

FIGURE 7.14: In-phase branch in (a) and quadrature phase branch in (b) at the transmitter after modulation of the SSB spreaded data signal onto the cosine and sine carriers, respectively (L=121,sps=4,r=1).

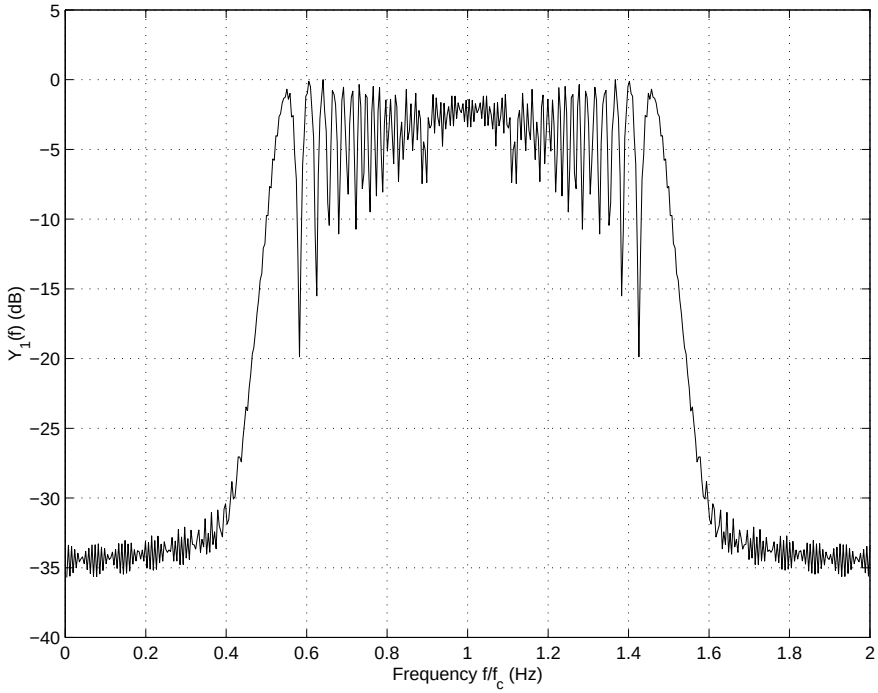

FIGURE 7.15: PSD of the in-phase branch at the transmitter after modulation of the DSB spreaded data signal onto the cosine carrier (L=121,sps=4,r=1).

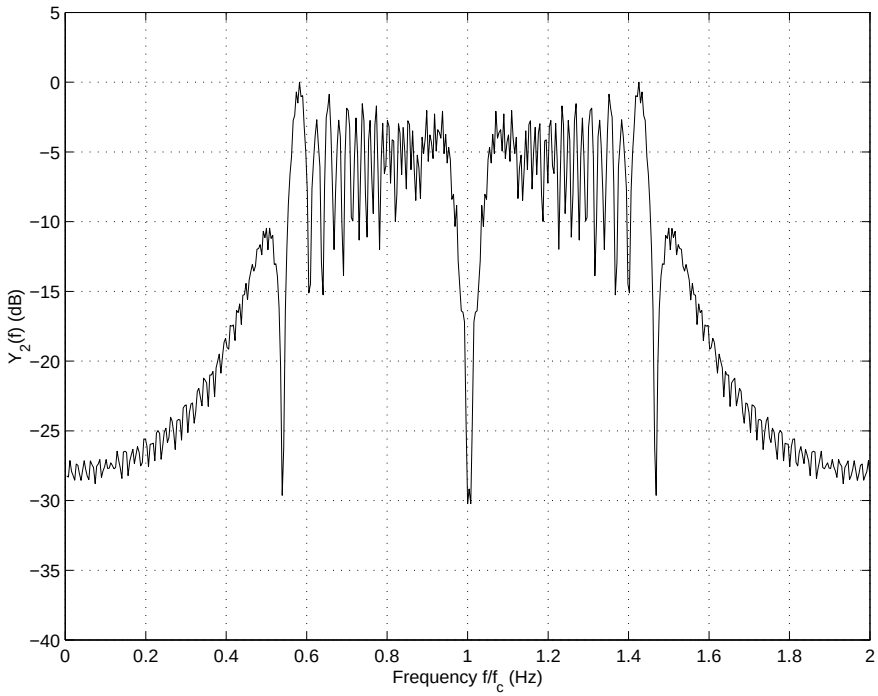

FIGURE 7.16: PSD of the quadrature phase branch at the transmitter after modulation of the DSB spreaded data signal onto the sine carrier (L=121,sps=4,r=1).

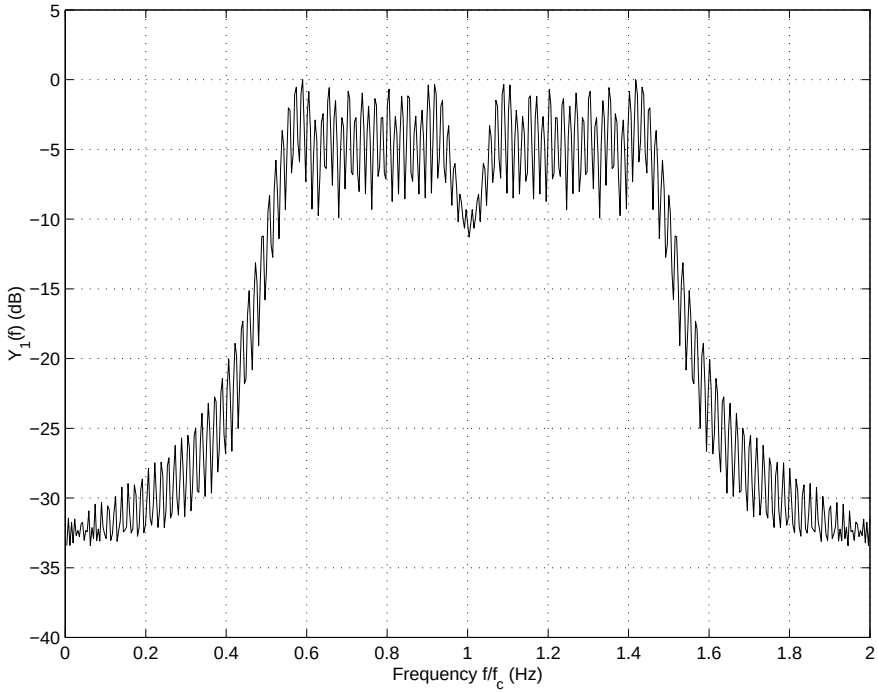

FIGURE 7.17: PSD of the in-phase branch at the transmitter after modulation of the SSB spreaded data signal onto the cosine carrier (L=121,sps=4,r=1).

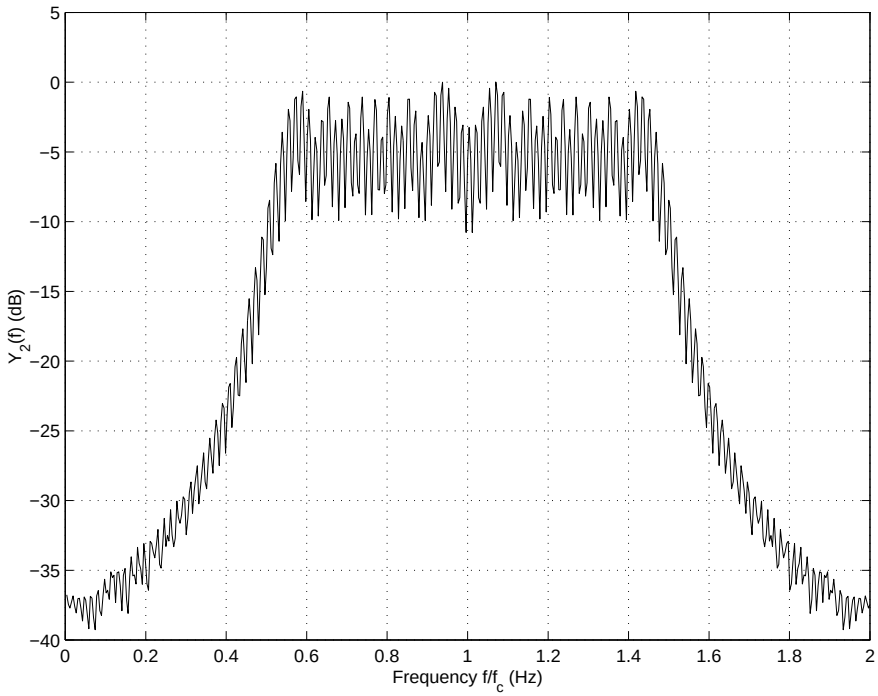

FIGURE 7.18: PSD of the quadrature phase branch at the transmitter after modulation of the SSB spreaded data signal onto the sine carrier (L=121,sps=4,r=1).

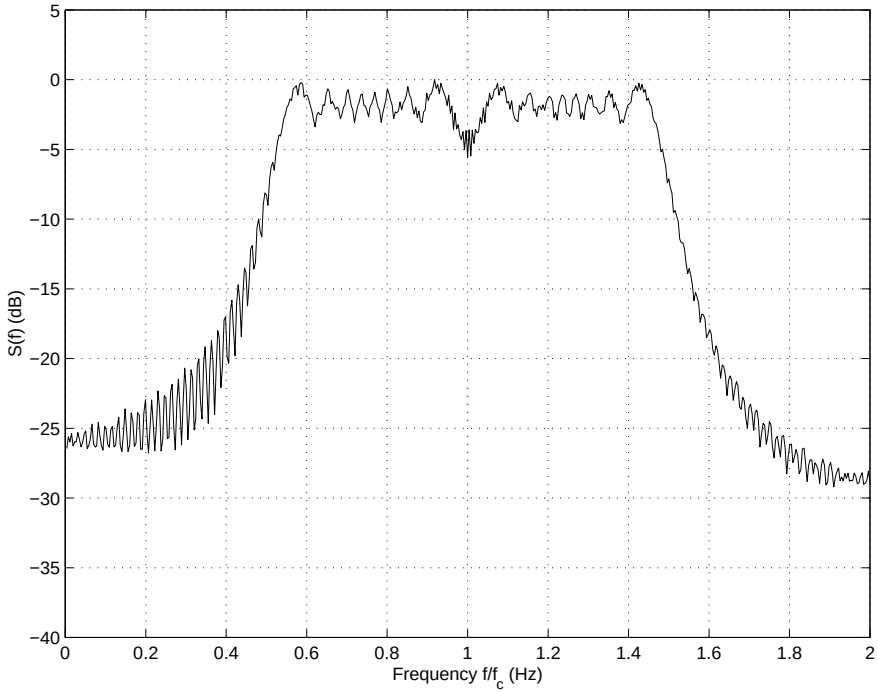

FIGURE 7.19: PSD of the final output of the DSSS transmitter when using DSB CSS in the case of balanced and QPSK (L=121,sps=4,r=1)

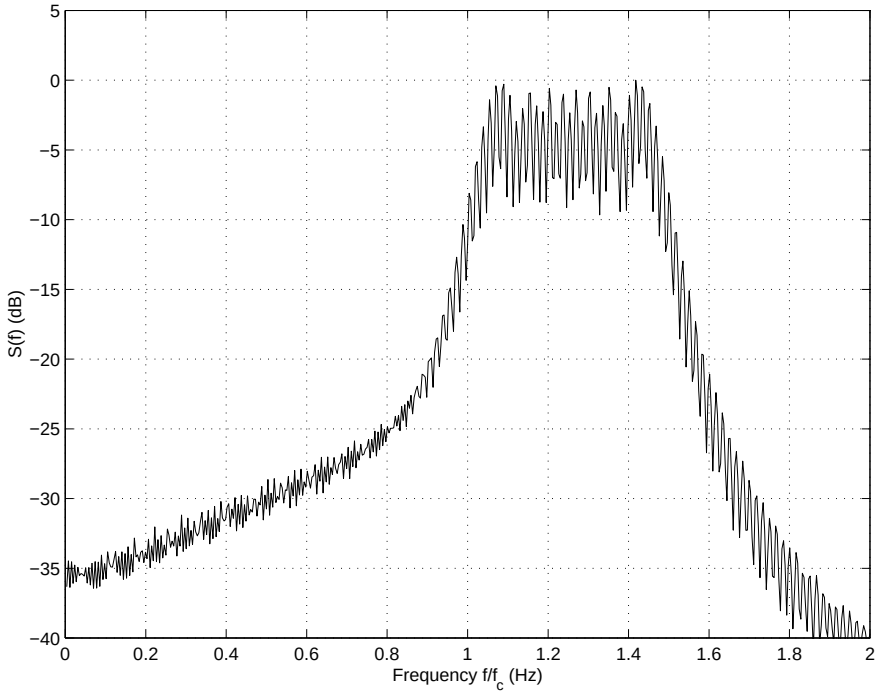

FIGURE 7.20: PSD of the final output of the DSSS transmitter when using SSB CSS in the case of balanced QPSK (L=121,sps=4,r=1)

CHAPTER EIGHT

SIMULATION OF THE DSSS RECEIVER

8.1 INTRODUCTION AND DESCRIPTION

The theoretically analysed DSSS receiver structures, which form the complete complex DSSS system, have been simulated in C++. Figure 7.1 presents a block diagram of the complete simulated system. The simulation of the receiver with all corresponding results are presented in this chapter. Figure 8.1 shows the block diagram of the receiver for the case of the balanced QPSK as well as the normal QPSK configuration. The receiver consists of two multipliers in parallel, despreading the incoming signal with the receiver's replica of spreading codes C_1 and C_2, which are the same synchronized unique combinations used in the transmitter, provided by the VCCG module in the complex DLL subsystem. These despreaded signals are then demodulated with the recovered quadrature sine and cosine carriers and then integrate-and-dumped to produce $g_1(t)$ and $g_2(t)$, respectively. For the case of the balanced QPSK configuration, $g_(t)$ and $g_2(t)$ are summed and sampled, whereafter a decision is made to recover the original data. For the dual channel QPSK configuration, the two parallel signals, $g_1(t)$ and $g_2(t)$, are sampled separately, whereupon decisions are made based on these samples, in order to recover the original two data streams. The following figures will illustrate the signals at different points throughout the receiver structure for both configurations, as well as for the cases where DSB and SSB CSS are used in the spreading and despreading processes.

The decision-directed complex Costas carrier recovery loop, decision-directed complex DLL as well as the acquisition circuitry are also simulated to perform a fully independent receiver structure responsible for code acquisition, carrier recovery and code tracking.

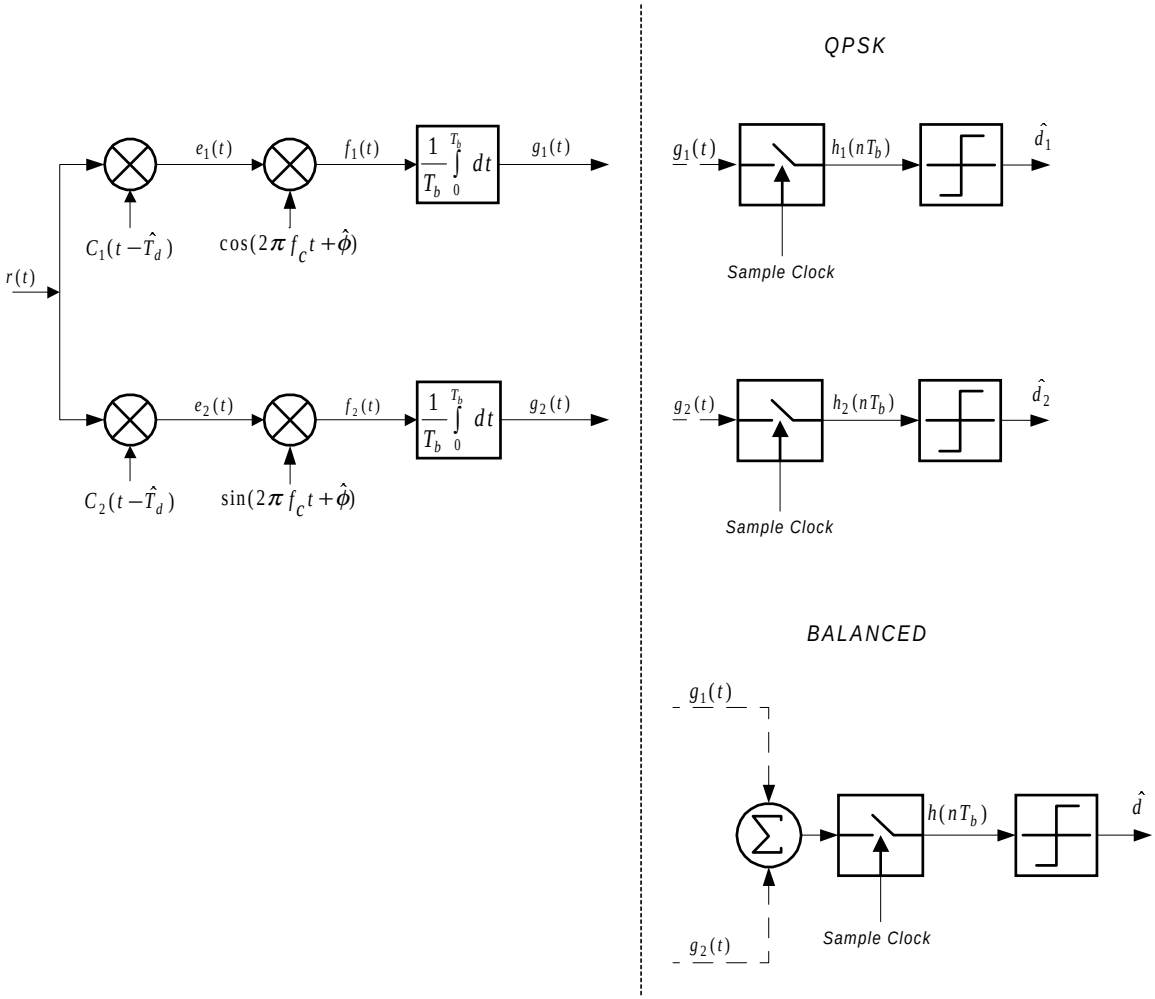

FIGURE 8.1: Block diagram of the receiver structure used in the simulation

Results related to these loop structures will also be given in this chapter.

8.2 SIMULATION RESULTS AND DISCUSSION

The two branch signals after despreading, $e_1(t)$ and $e_2(t)$, are shown in Figure 8.2 for the case of DSB CSS and Figure 8.3 shows the case for SSB CSS. The spectra for these despreaded signals are shown in Figures 8.4 and 8.5 for the DSB CSS and in Figures 8.6 and 8.7 for SSB CSS. It can be seen in Figures 8.4, 8.5, 8.6 and 8.7 that the despreaded signals are still modulated onto the carrier signal and that the bandwidth is much narrower than that of the spreaded output signal at the transmitter. The recovered carriers, cosine and sine, are now used to demodulate the two branch signals to obtain $f_1(t)$ and $f_2(t)$, respectively, and is shown in Figure 8.8 for DSB CSS, and in Figure 8.9 for SSB CSS. The spectra for these despreaded demodulated signals are presented for DSB CSS in Figures 8.10 and 8.11 and in Figures 8.12 and 8.13 for SSB CSS. The length of the CSS, from which the unique despreading code combinations is generated, is $L = 121$, with 4 samples per chip and $r = 1$. In this case the processing gain of the system equald $10log(121) = 20.83dB$.

The in-phase and quadrature branch signals, after integrate-and-dump operation, are shown in Figure 8.14, for DSB CSS, while Figure 8.15 shows the case using SSB CSS. In the case of DSB CSS, the PSD of the in-phase branch signal is depicted in Figure 8.16 and for the quadrature branch in Figure 8.17. The PSDs for the in-phase and quadrature branch signals, using SSB CSS, are depicted in Figures 8.18 and 8.19, respectively.

In Figure 8.20 the PSD of the incoming signal, with $Eb/No = 10dB$, is shown, using DSB CSS, and in Figure 8.21 using SSB CSS. By despreading these signals with the unique spreading sequence combination C_1 in the case of DSB CSS, a PSD is obtained as show in Figure 8.22, and with unique combination C_2 the PSD shown in Figure 8.23 is obtained. When the SSB CSS input signal is despread with the unique combinations C_1 and C_2, respectively, the PSD of the in-phase branch is as depicted in Figure 8.24 and the PSD of the quadrature branch as in Figure 8.25, with $Eb/No = 10dB$.

Figure 8.26 shows the in-phase and quadrature branch signal after integrate-and-dump operation in the case of DSB CSS and at $Eb/No = 10dB$, while Figure 8.27 shows the integrate-and-dump output of the in-phase and quadrature branches when using SSB CSS.

The PSD of the incoming signal, with $Eb/No = 20dB$, is shown in Figure 8.28 when using DSB CSS. Figures 8.29 and 8.30 depicts the PSDs of the incoming signal with a $Eb/No = 30dB$, for the DSB and SSB cases, respectively.

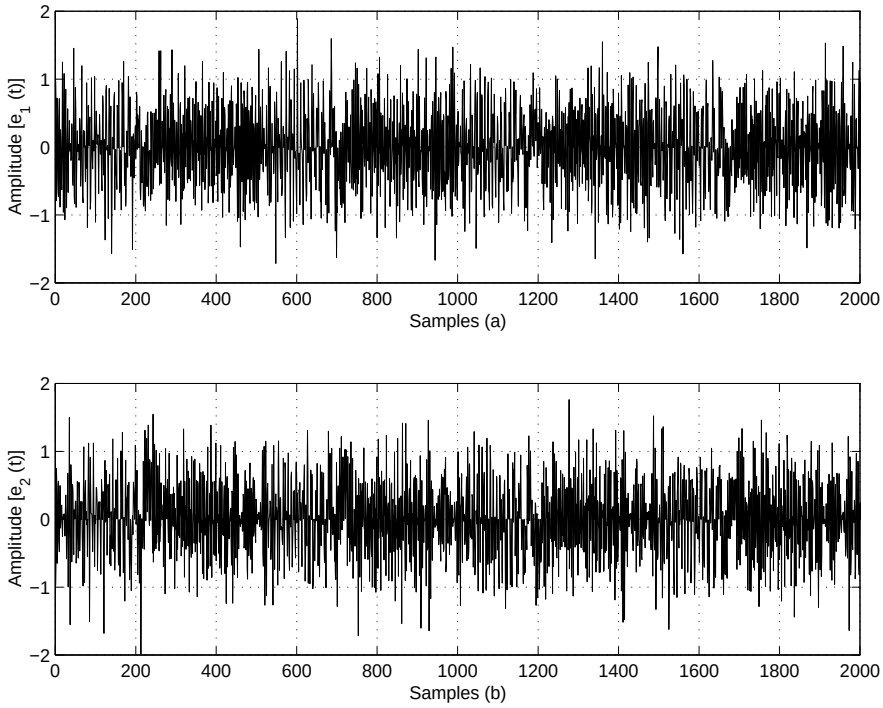

FIGURE 8.2: Incoming signal despreaded with unique combination C_1 in (a) and with C_2 in (b) for the case of DSB CSS (L=121, sps=4 and r=1).

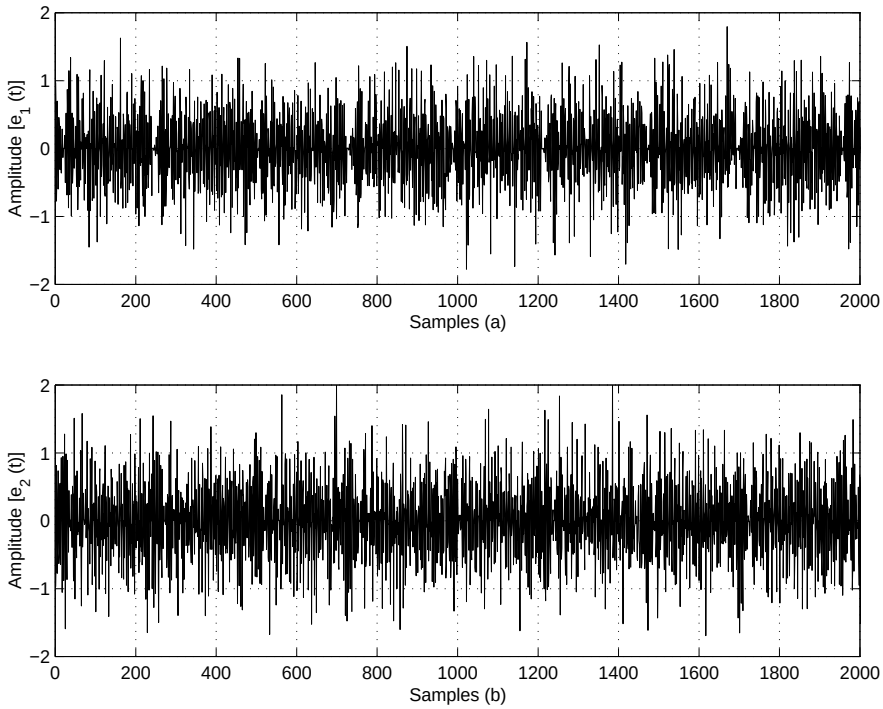

FIGURE 8.3: Incoming signal despreaded with unique combination C_1 in (a) and with C_2 in (b) for the case of SSB CSS (L=121, sps=4 and r=1).

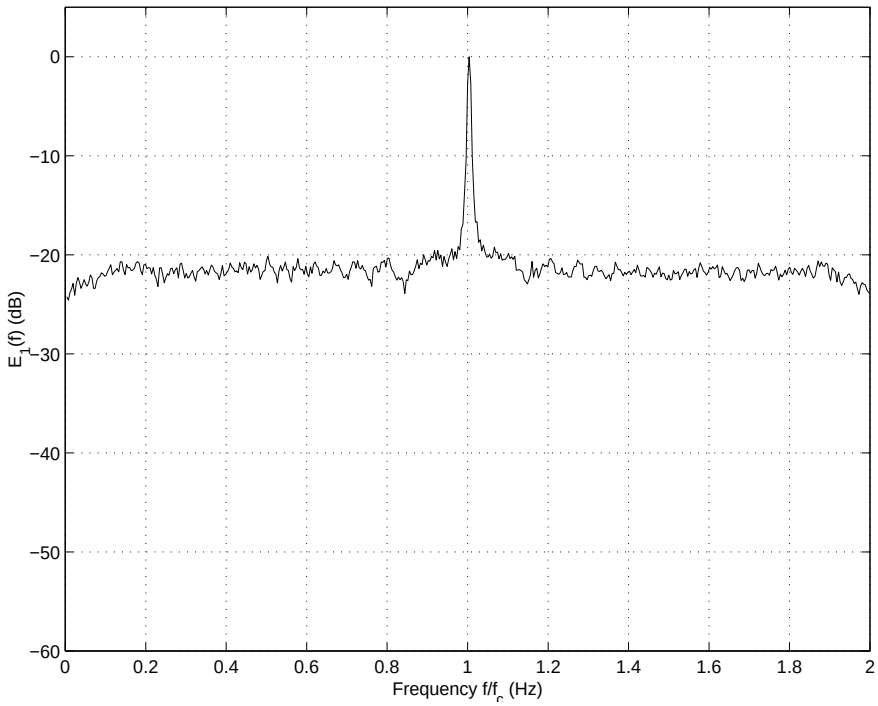

FIGURE 8.4: PSD of the incoming signal despreaded with the unique combination C_1 for the case of DSB CSS (L=121, sps=4 and r=1).

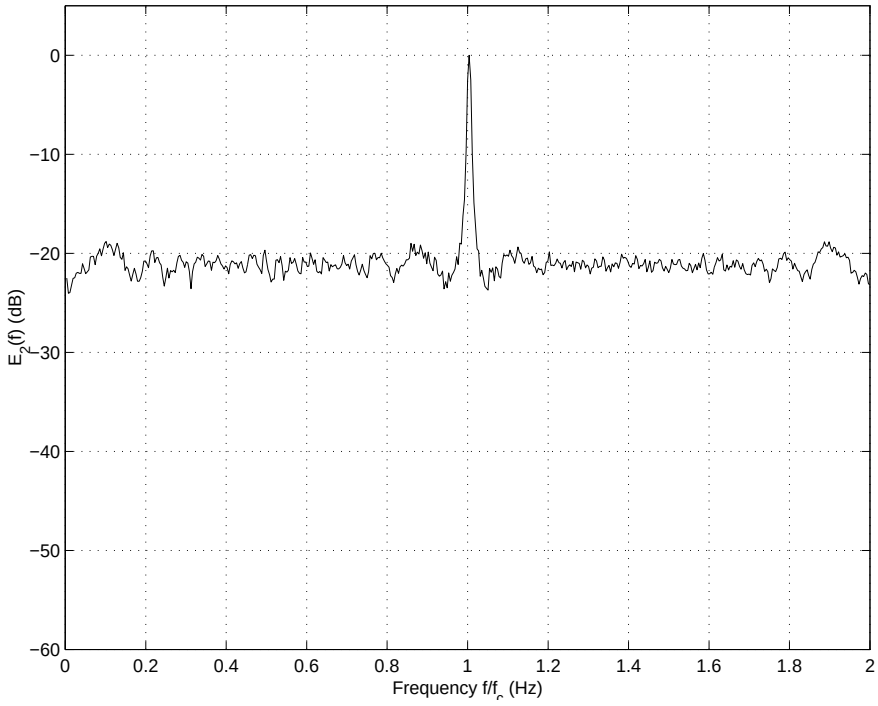

FIGURE 8.5: PSD of the incoming signal despreaded with the unique combination C_2 for the case of DSB CSS (L=121, sps=4 and r=1).

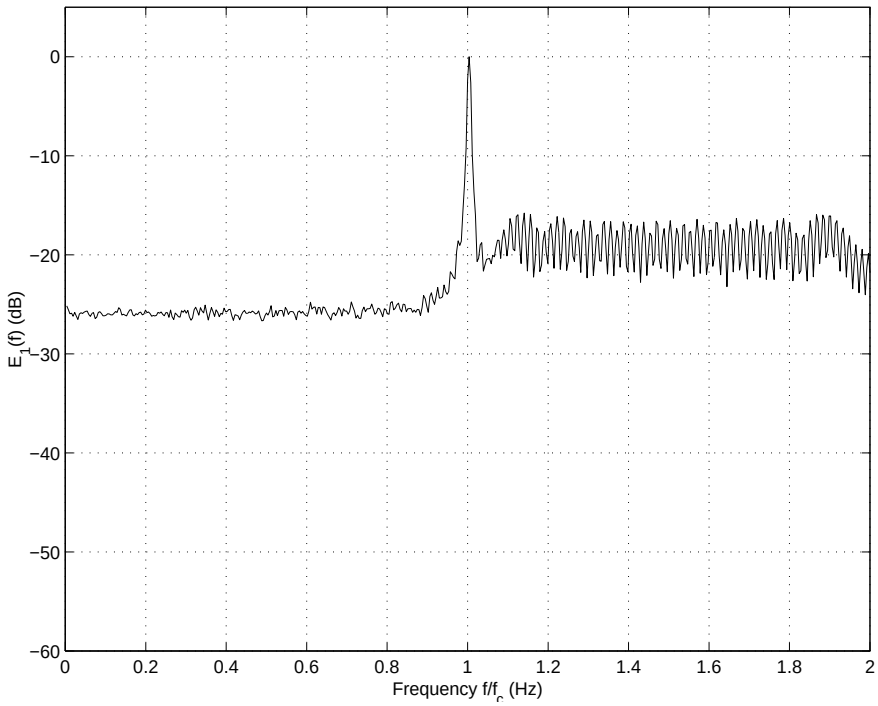

FIGURE 8.6: PSD of the incoming signal despreaded with the unique combination C_1 for the case of SSB CSS (L=121, sps=4 and r=1).

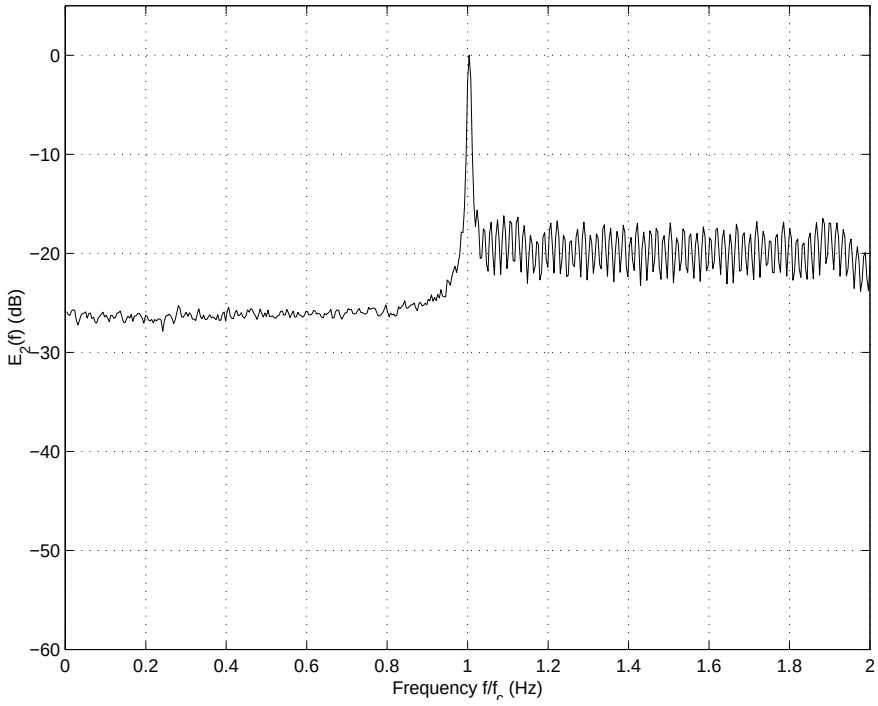

FIGURE 8.7: PSD of the incoming signal despreaded with the unique combination C_2 for the case of SSB CSS (L=121, sps=4 and r=1).

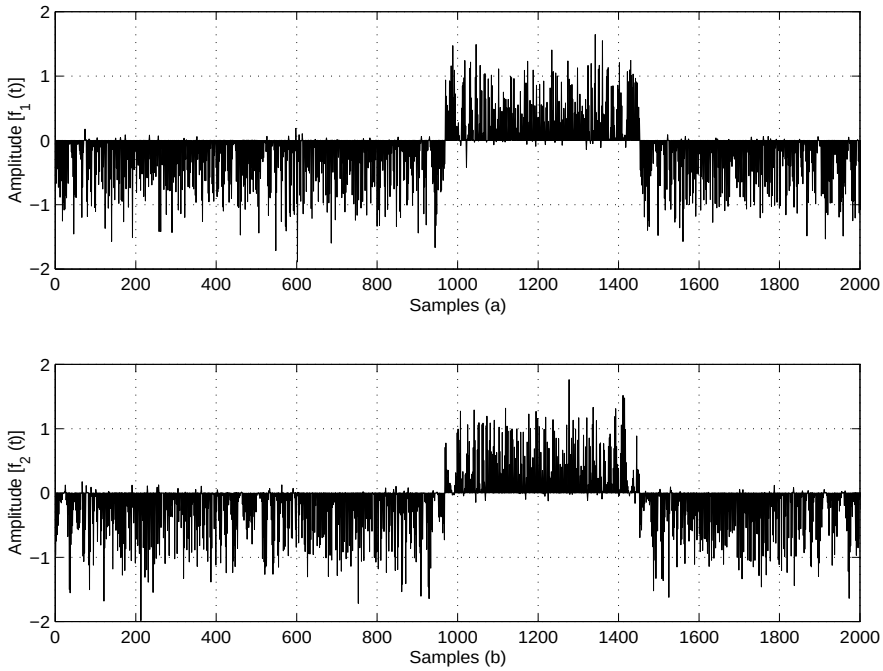

FIGURE 8.8: In-phase branch signal after despreading with DSB CSS C_1 and demodulation with the recovered cosine carrier in (a) and quadrature phase branch signal after despreading with DSB CSS C_2 and demodulation with the recovered sine carrier in (b) (L=121,sps=4,r=1).

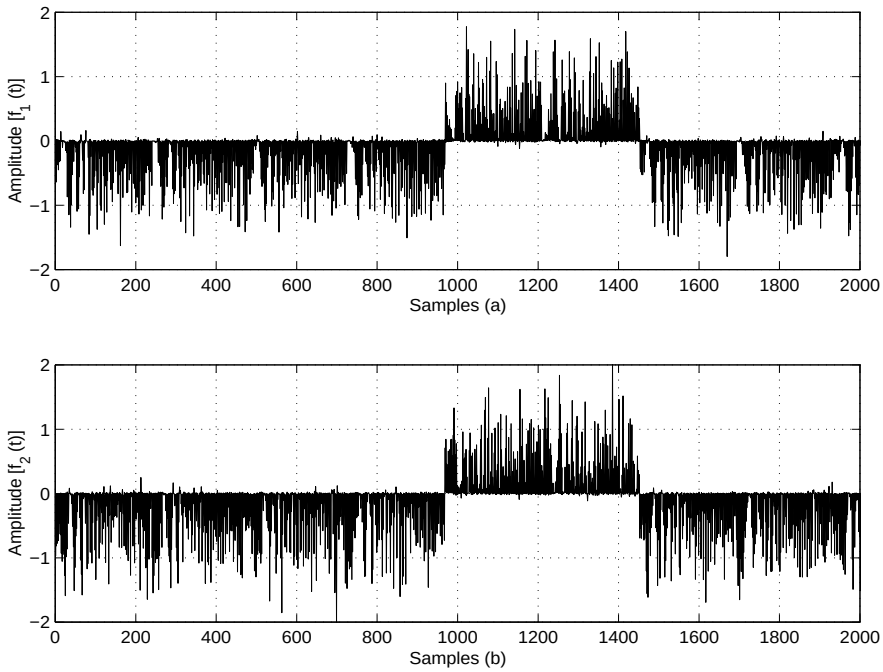

FIGURE 8.9: In-phase branch signal after despreading with SSB CSS C_1 and demodulation with the recovered cosine carrier in (a) and quadrature phase branch signal after despreading with SSB CSS C_2 and demodulation with the recovered sine carrier in (b) (L=121,sps=4,r=1).

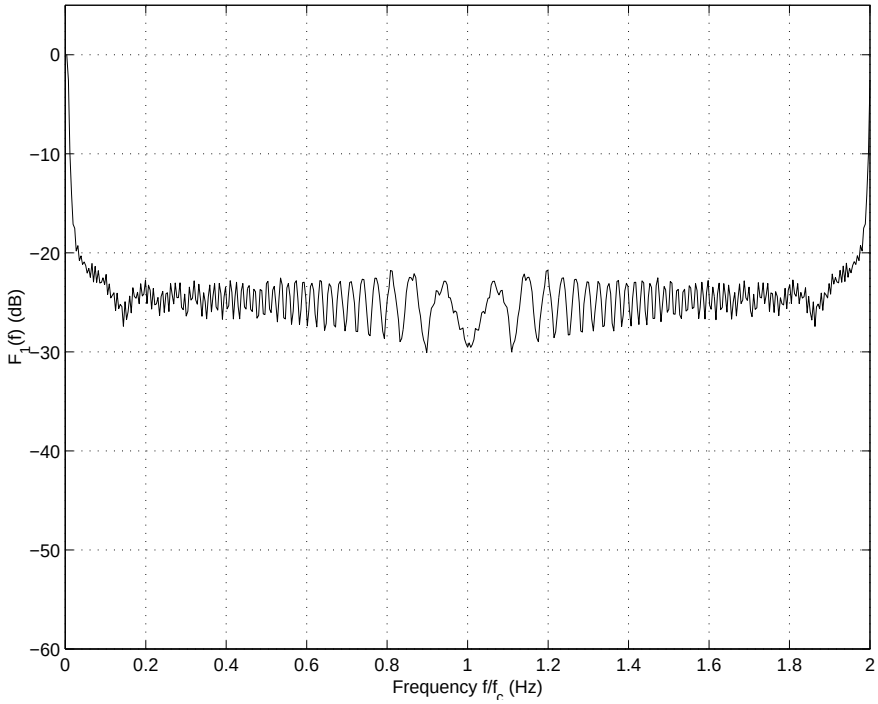

FIGURE 8.10: PSD of the in-phase branch signal after despreading with DSB CSS C_1 and demodulation with the recovered cosine carrier (L=121,sps=4,r=1).

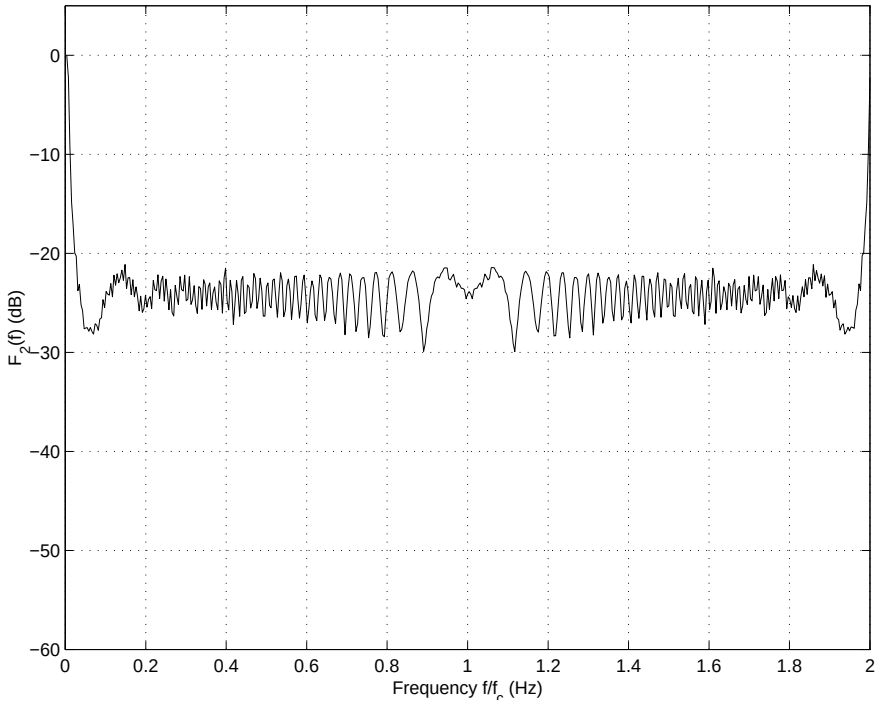

FIGURE 8.11: PSD of the quadrature phase branch signal after despreading with DSB CSS C_2 and demodulation with the recovered sine carrier (L=121,sps=4,r=1).

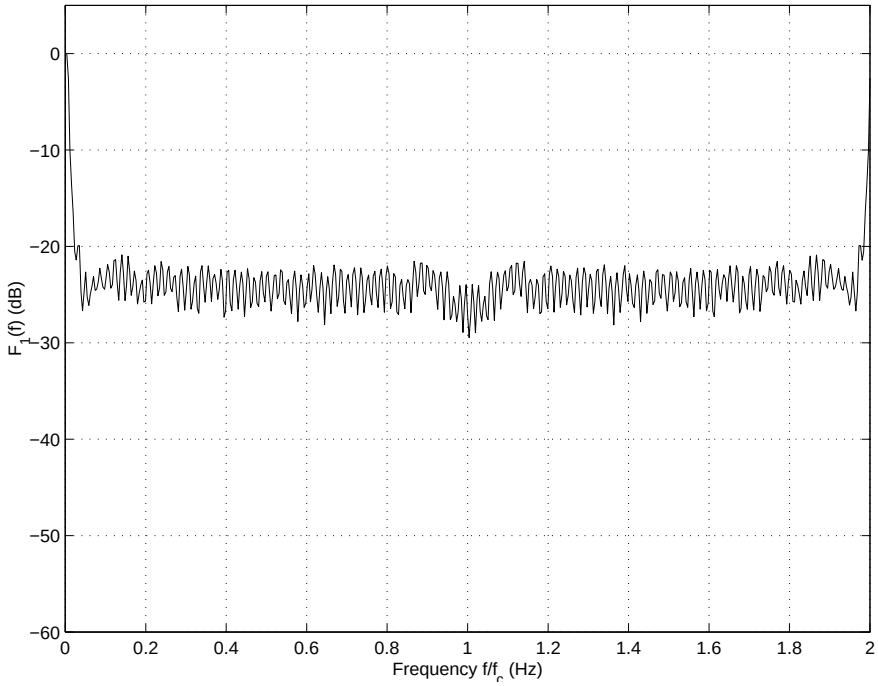

FIGURE 8.12: PSD of the in-phase branch signal after despreading with SSB CSS C_1 and demodulation with the recovered cosine carrier (L=121,sps=4,r=1).

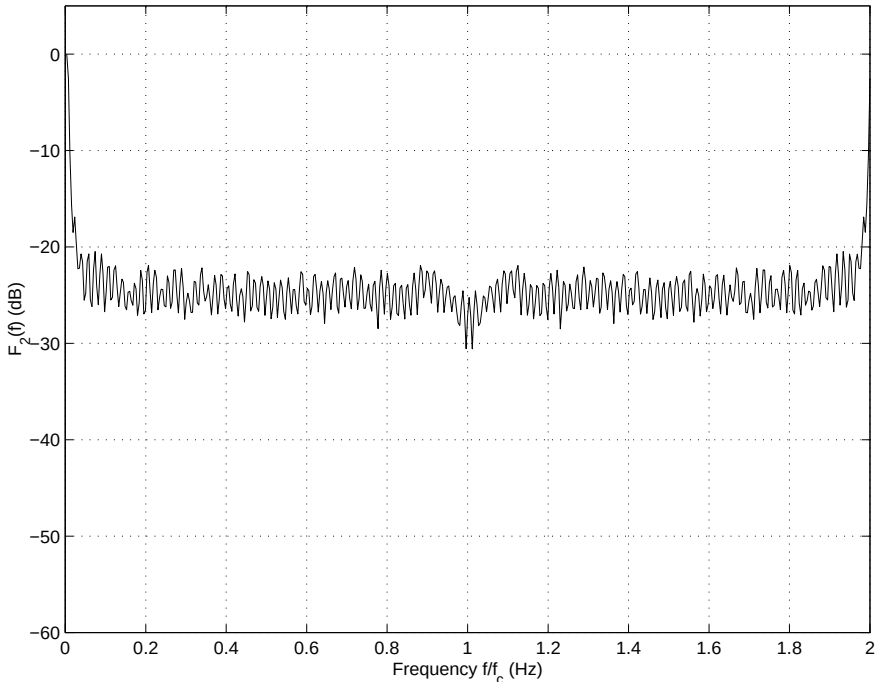

FIGURE 8.13: PSD of the quadrature phase branch signal after despreading with SSB CSS C_2 and demodulation with the recovered sine carrier (L=121,sps=4,r=1).

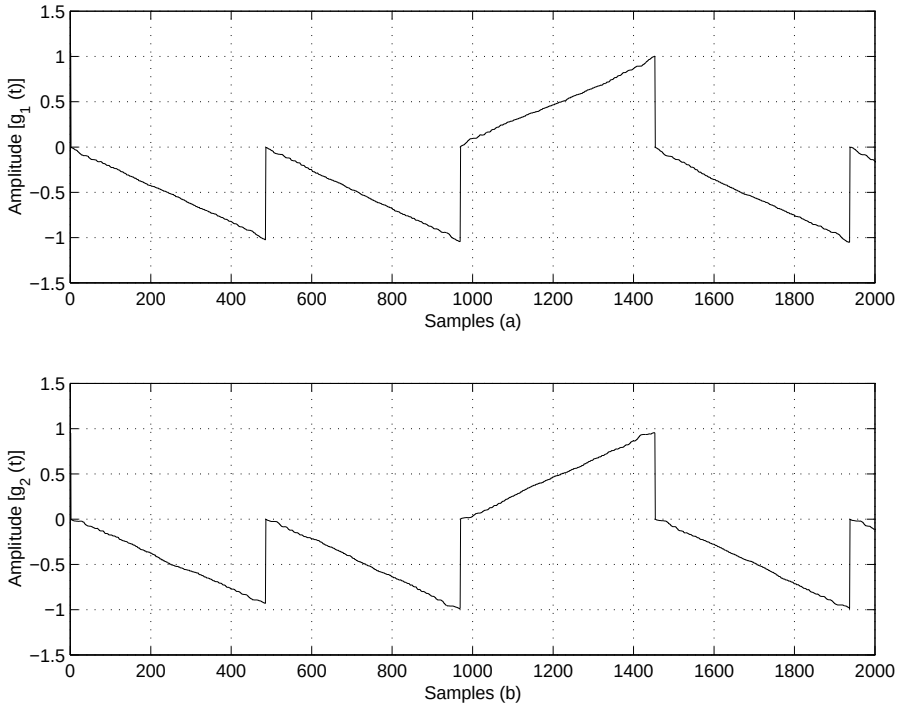

FIGURE 8.14: In-phase branch signal after integrate-and-dump operation in (a) and quadrature phase branch signal after integrate-and-dump operation in (b) for the case of DSB CSS.

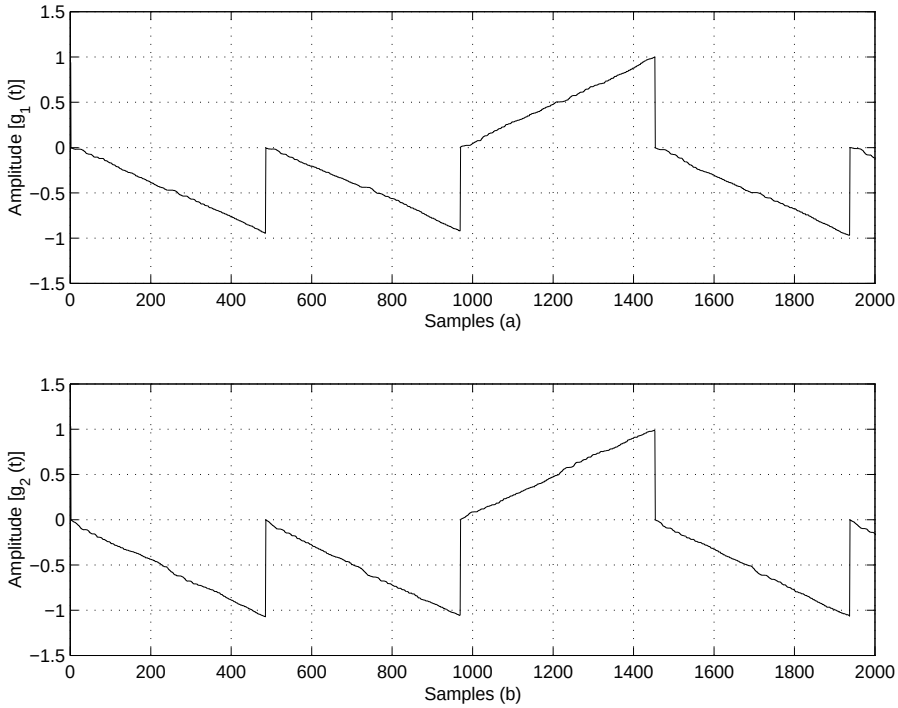

FIGURE 8.15: In-phase branch signal after integrate-and-dump operation in (a) and quadrature phase branch signal after integrate-and-dump operation in (b) for the case of SSB CSS.

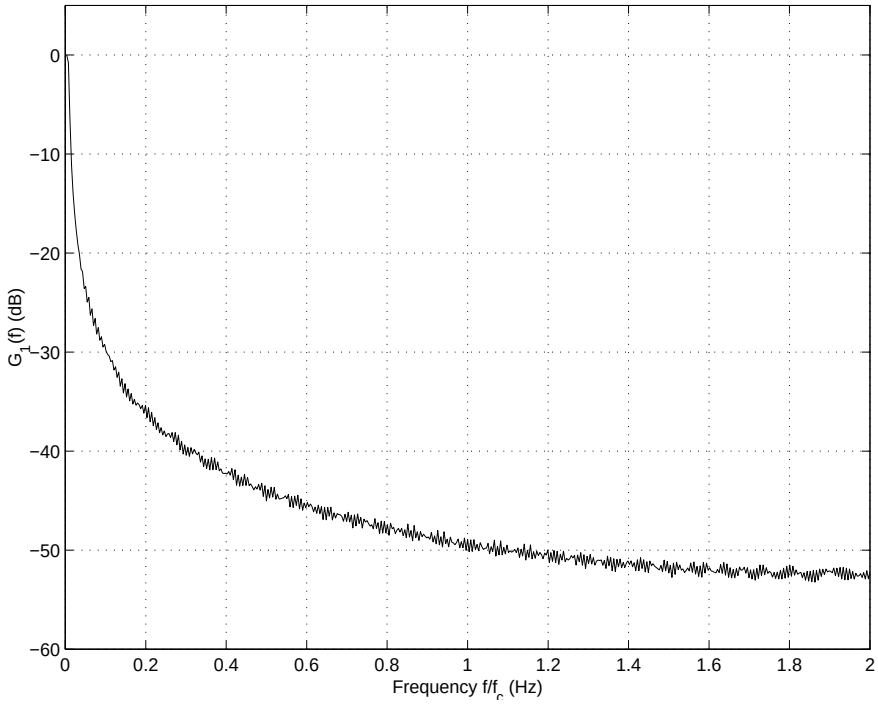

FIGURE 8.16: PSD of the in-phase branch signal after integrate-and-dump operation for the case of DSB CSS.

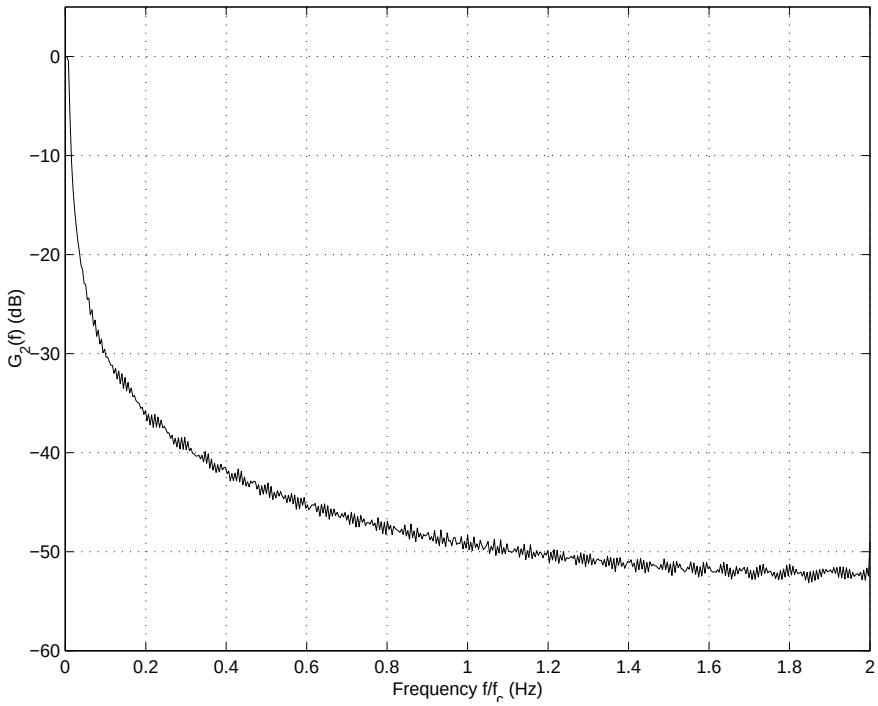

FIGURE 8.17: PSD of the quadrature phase branch signal after integrate-and-dump operation for the case of DSB CSS.

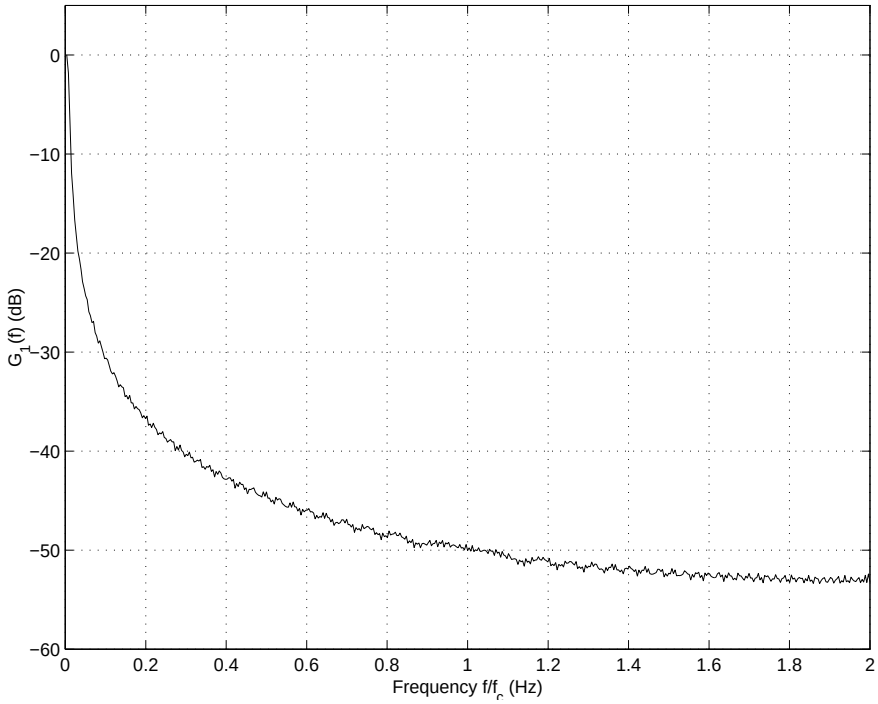

FIGURE 8.18: PSD of the in-phase branch signal after integrate-and-dump operation for the case of SSB CSS.

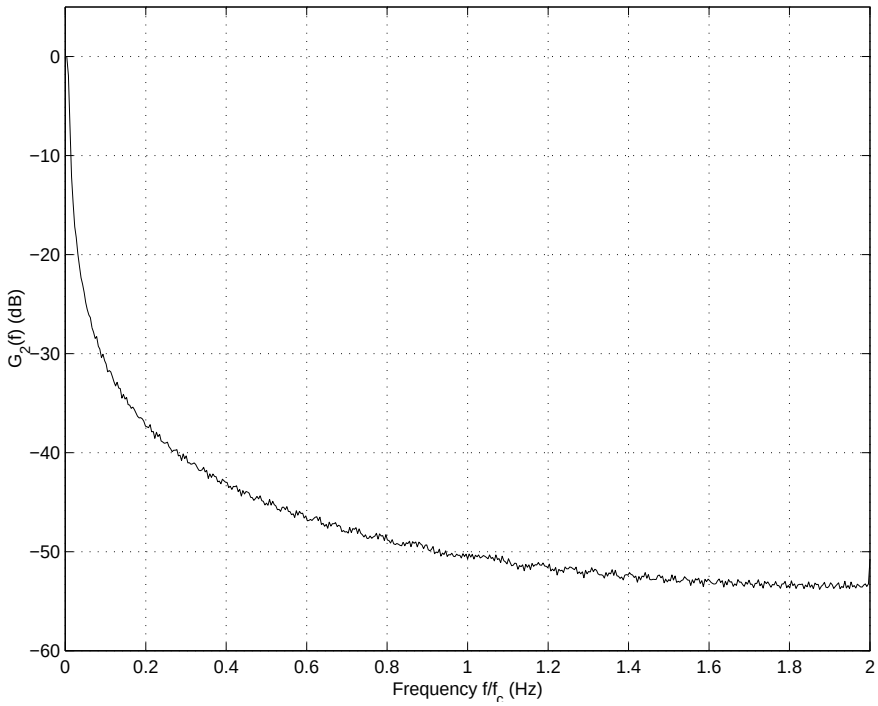

FIGURE 8.19: PSD of the quadrature phase branch signal after integrate-and-dump operation for the case of SSB CSS.

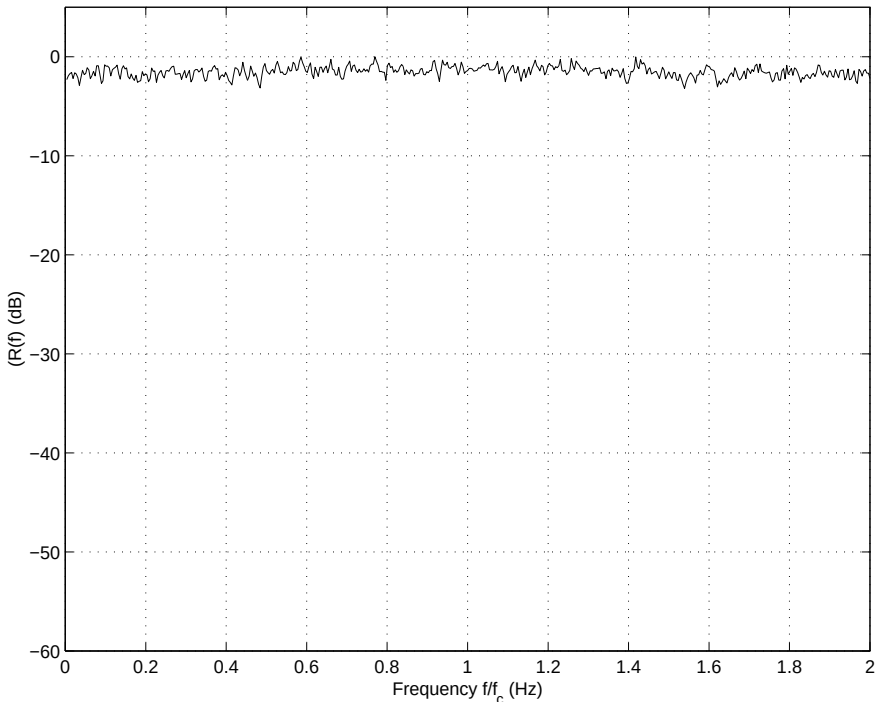

FIGURE 8.20: PSD of the incoming signal with a $Eb/No = 10dB$ and by using DSB CSS, (L=121,sps=4,r=1)

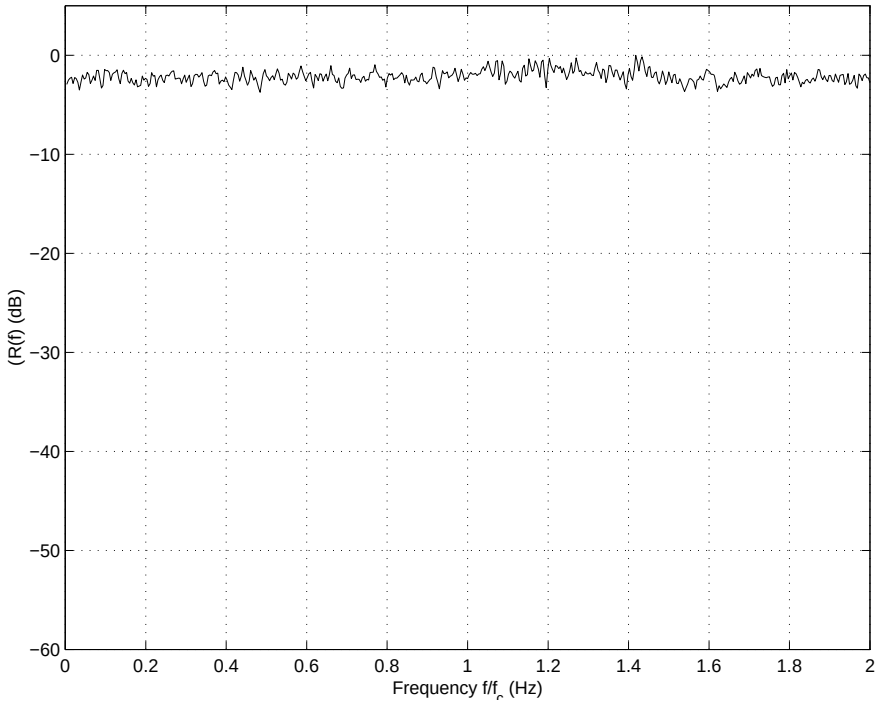

FIGURE 8.21: PSD of the incoming signal with a $Eb/No = 10dB$ and by using SSB CSS, (L=121,sps=4,r=1)

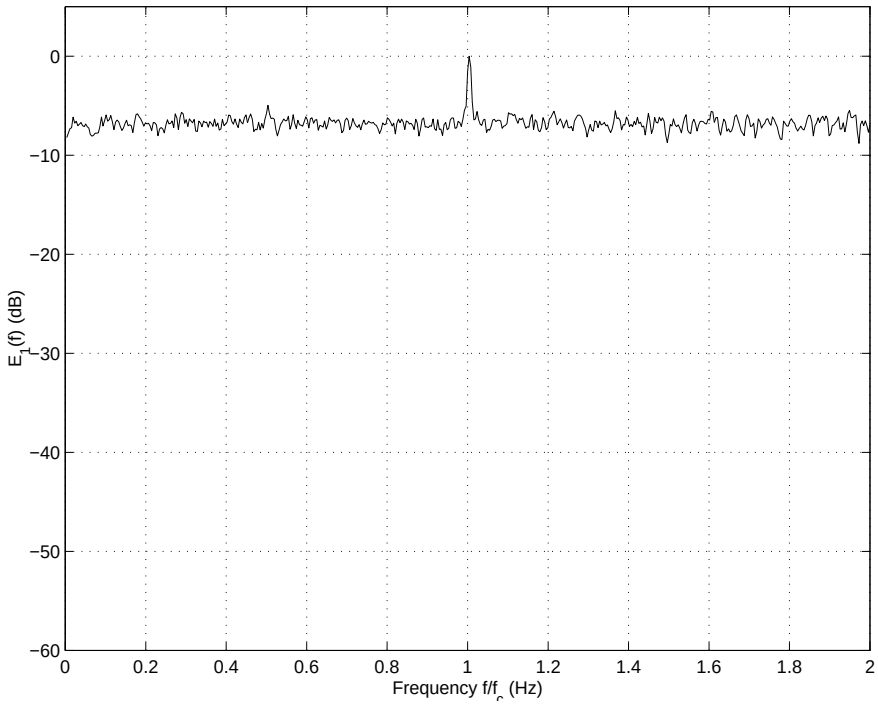

FIGURE 8.22: PSD of the incoming signal despreaded with the unique combination C_1 for the case of DSB CSS and at a $Eb/No = 10dB$, (L=121, sps=4 and r=1).

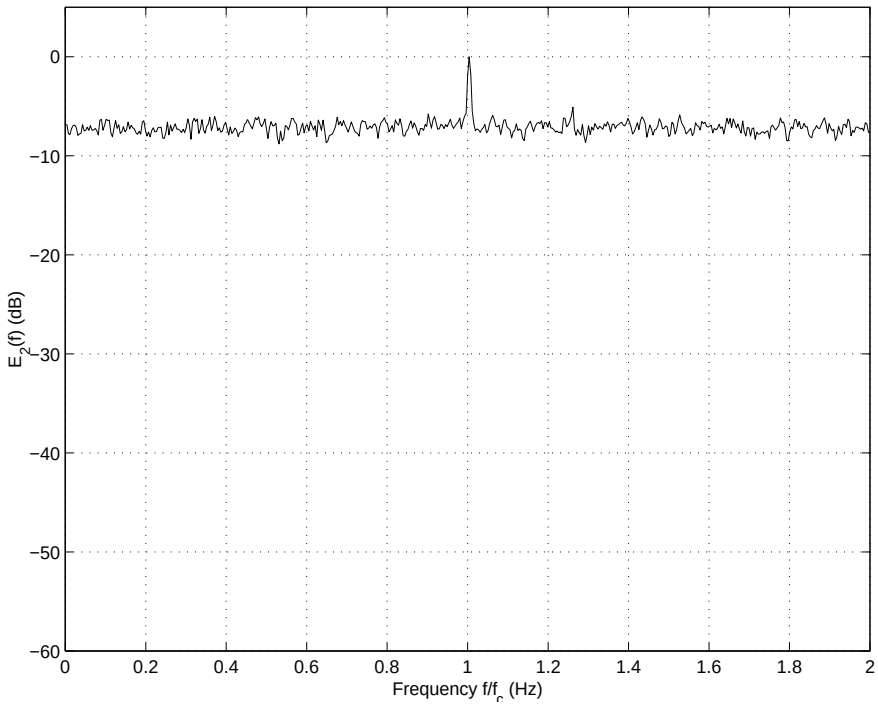

FIGURE 8.23: PSD of the incoming signal despreaded with the unique combination C_2 for the case of DSB CSS and at a $Eb/No = 10dB$, (L=121, sps=4 and r=1).

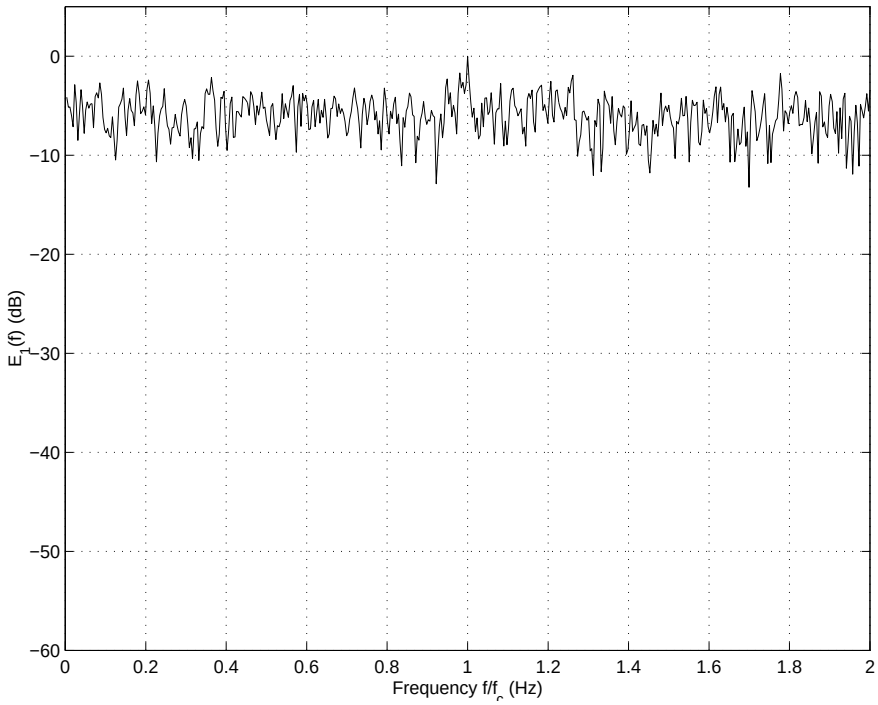

FIGURE 8.24: PSD of the incoming signal despreaded with the unique combination C_1 for the case of SSB CSS and at a $Eb/No = 10dB$, (L=121, sps=4 and r=1)

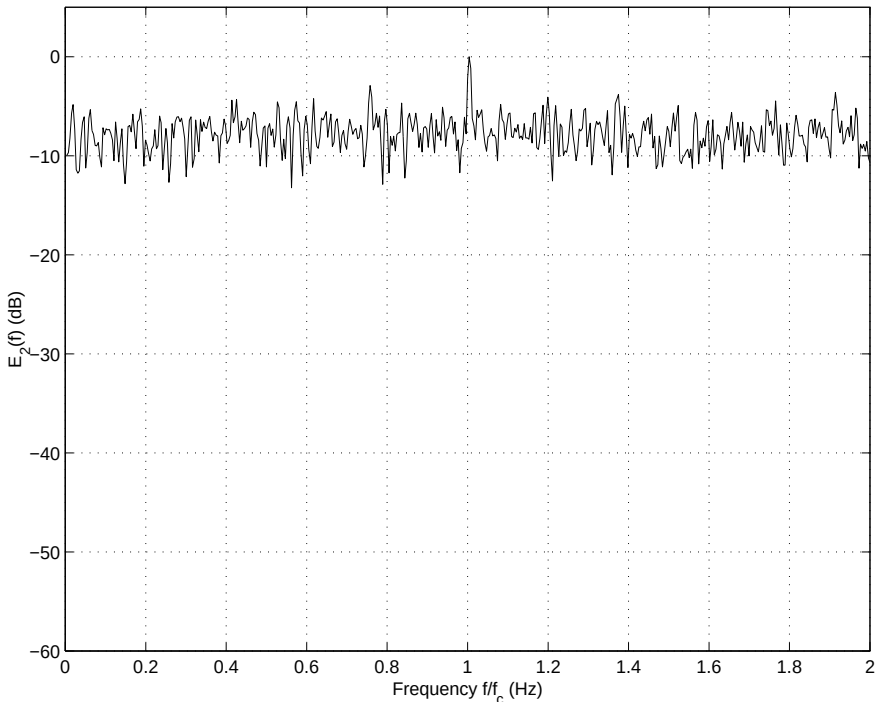

FIGURE 8.25: PSD of the incoming signal despreaded with the unique combination C_2 for the case of SSB CSS and at a $Eb/No = 10dB$, (L=121, sps=4 and r=1)

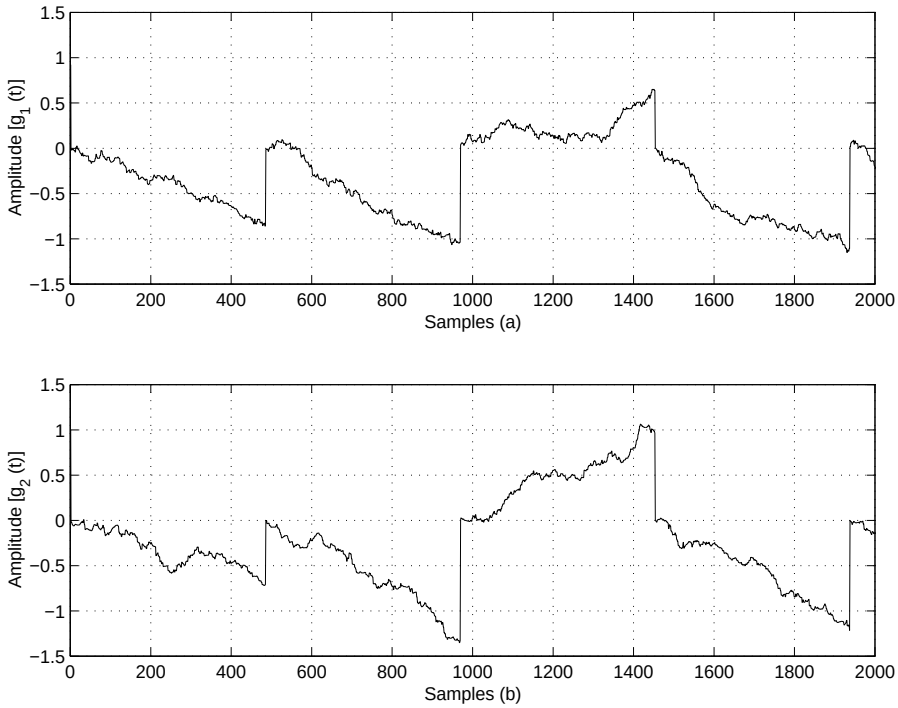

FIGURE 8.26: In-phase branch signal after integrate-and-dump operation in (a) and quadrature phase branch signal after integrate-and-dump operation in (b) for the case of DSB CSS and at $Eb/No = 10dB$, (L=121, sps=4 and r=1).

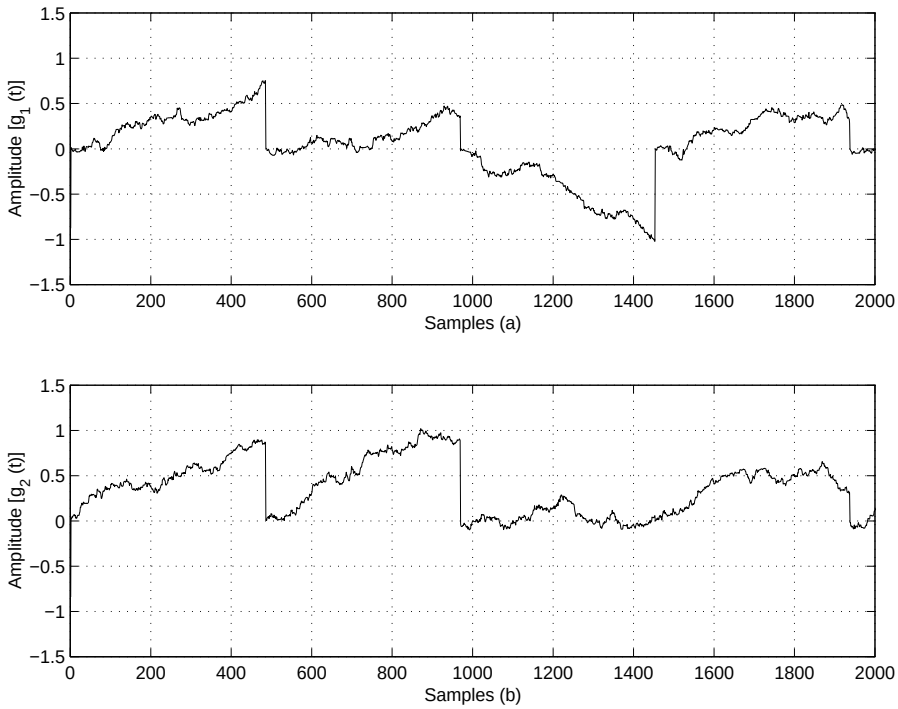

FIGURE 8.27: In-phase branch signal after integrate-and-dump operation in (a) and quadrature phase branch signal after integrate-and-dump operation in (b) for the case of SSB CSS and at $Eb/No = 10dB$, (L=121, sps=4 and r=1).

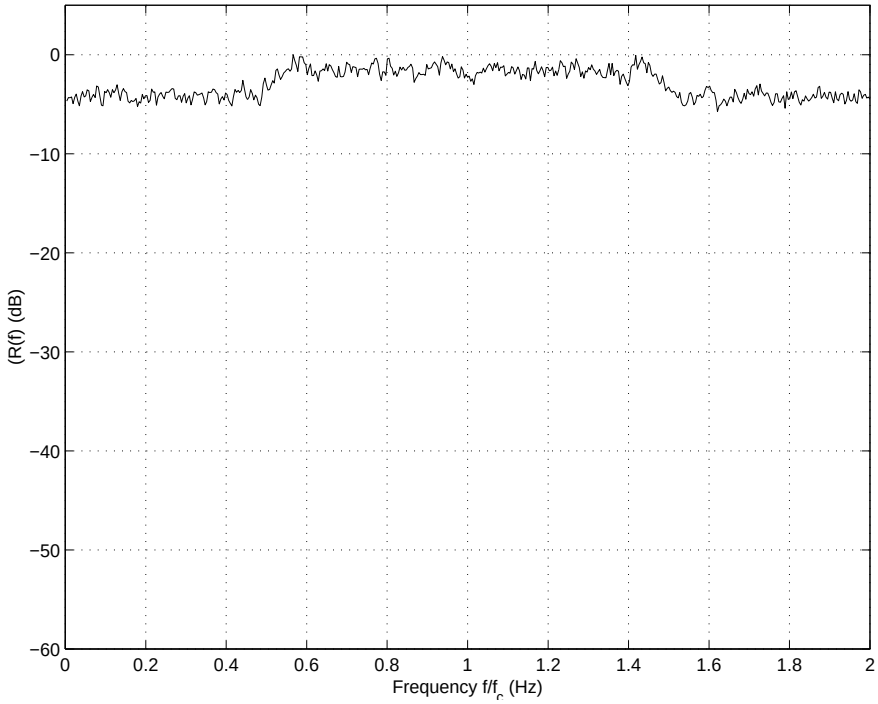

FIGURE 8.28: PSD of the incoming signal with a $Eb/No = 20dB$ and by using DSB CSS, with L=121, sps=4 and r=1

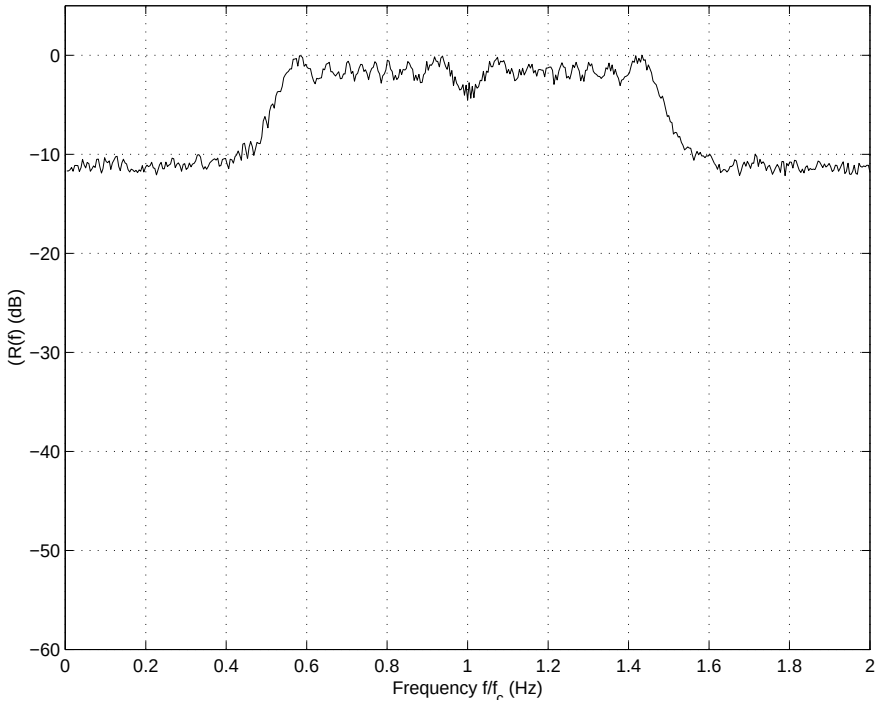

FIGURE 8.29: PSD of the incoming signal with a $Eb/No = 30dB$ and by using DSB CSS, with L=121, sps=4 and r=1

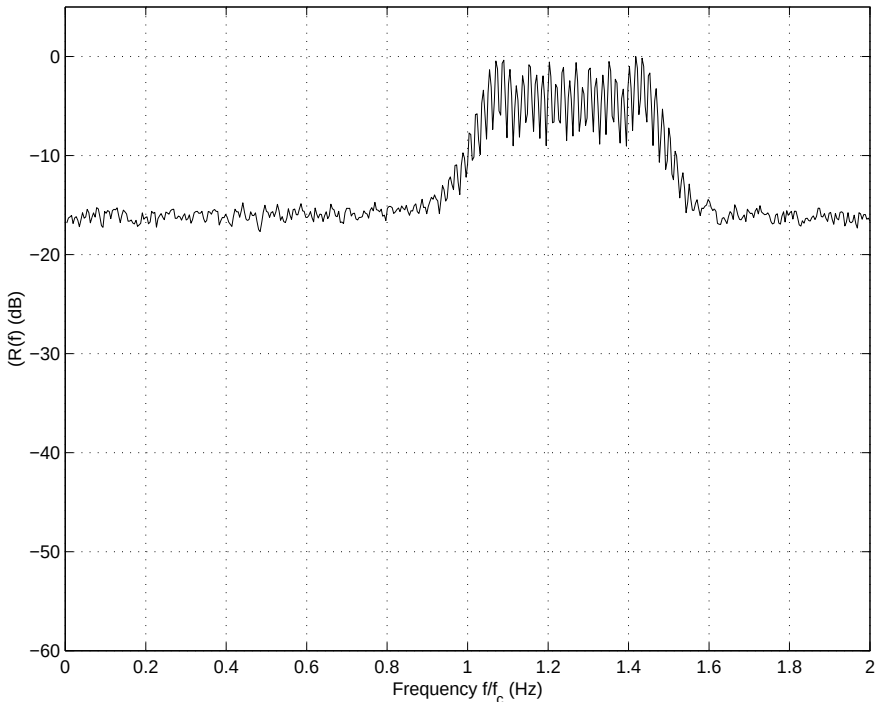

FIGURE 8.30: PSD of the incoming signal with a $Eb/No = 30dB$ and by using SSB CSS, with L=121, sps=4 and r=1

PART IV

HARDWARE IMPLEMENTATION

CHAPTER NINE

IMPLEMENTATION OF THE DSSS TRANSMITTER

9.1 INTRODUCTION

The success by which the theoretical analysis and simulation of the DSSS transmitter have been performed and the promising results obtained in Chapter 7, motivated the implementation of the transmitter in hardware. The same approach that has been followed with the theoretical analysis and simulation, was applied in the implementation of the hardware DSSS transmitter. This chapter gives the design approach and hardware transmitter structures used, as well as results obtained with this transmitter module. The transmitter module was the first prototype version built to illustrate the practical implementation of complex spreading sequences. The results obtained with the hardware transmitter module correlated very well with the theory and simulations. The system was also upgraded to a more advanced version using FPGA technology and will also be described in detail in this chapter. In Chapter 10 the final FPGA-based complex DSSS modem is presented, which is a great improvement in terms of technology relative to the structures described in this chapter.

9.2 HARDWARE DESCRIPTION

In contrast with DSSS communication systems using binary spreading sequences [6, 40], the spreading sequences employed in the DSSS systems described in this dissertation are complex, resulting in an increased implementation complexity when discrete logic components and memory devices are utilised. Memory devices are needed to implement the complex spreading sequences (CSS), by storing sampled pre-filtered replicas of the complex

spreading sequences. The generation of complex spreading sequences is subsequently accomplished by reading the sequences from memory in real time. In contrast, in a conventional binary DSSS system, the binary Gold or Kasami spreading sequences are generated using simple shift register devices with feedback. It is nevertheless shown in Chapter 10 that the complexity problem experienced with CSS can be largely overcome by using reprogrammable FPGA technology.

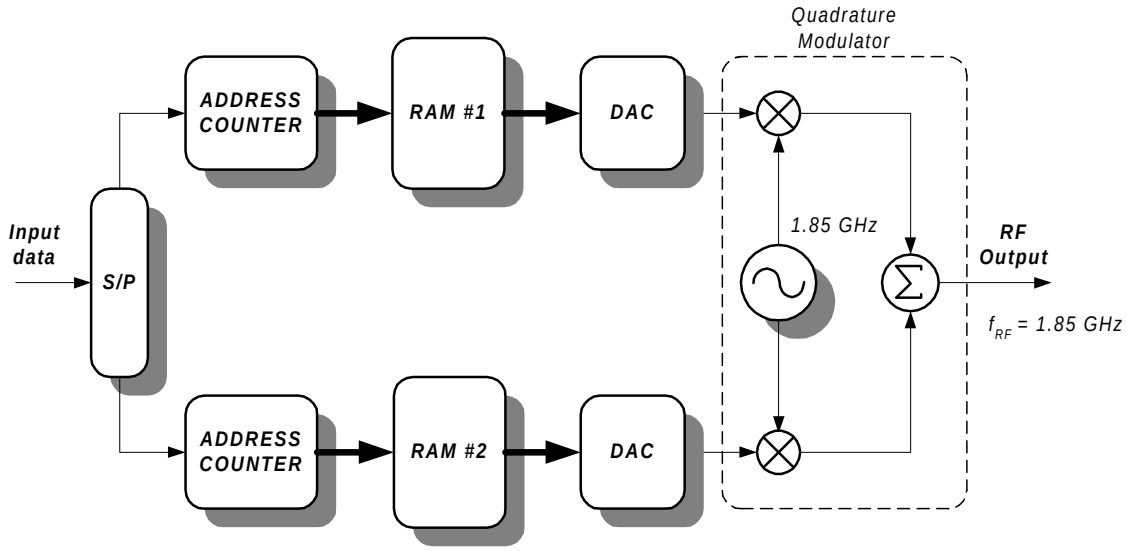

FIGURE 9.1: Block diagram of the hardware implementation of the complex DSSS transmitter

The transmitter, illustrated in Figure 9.1, consists of a serial-to-parallel converter producing two parallel data streams at the symbol rate (half the bit rate) for the case of the dual channel QPSK configuration and two identical data streams at the bit rate for the balanced QPSK configuration. These data streams are inputs to two address counters and are used as the most significant bits in the addresses supplied to two blocks of SRAMs. The data bits are used to select between different RAM blocks for the representation of "$1s$" and "$0s$", where different replicas of the spreading sequences are stored. Thus, different replicas of the spreading sequences are read out of the RAMs, representing "$1s$" and "$0s$", respectively, corresponding to the occurrence of "$1s$" and "$0s$" on the two branches, to accomplish the direct sequence spreading process. The digital outputs of the RAMs are converted to analog signals by means of digital-to-analog converters (DACs) to form the baseband in-phase and quadrature-phase branches. These baseband signals are fed into a quadrature modulator to be modulated onto cosine and sine RF carriers (at typically 1.85

GHz), whereafter they are combined with a zero-degree combiner to produce the final output signal of the complex DSSS transmitter. Figure 9.2 shows the complex DSSS transmitter hardware implementation.

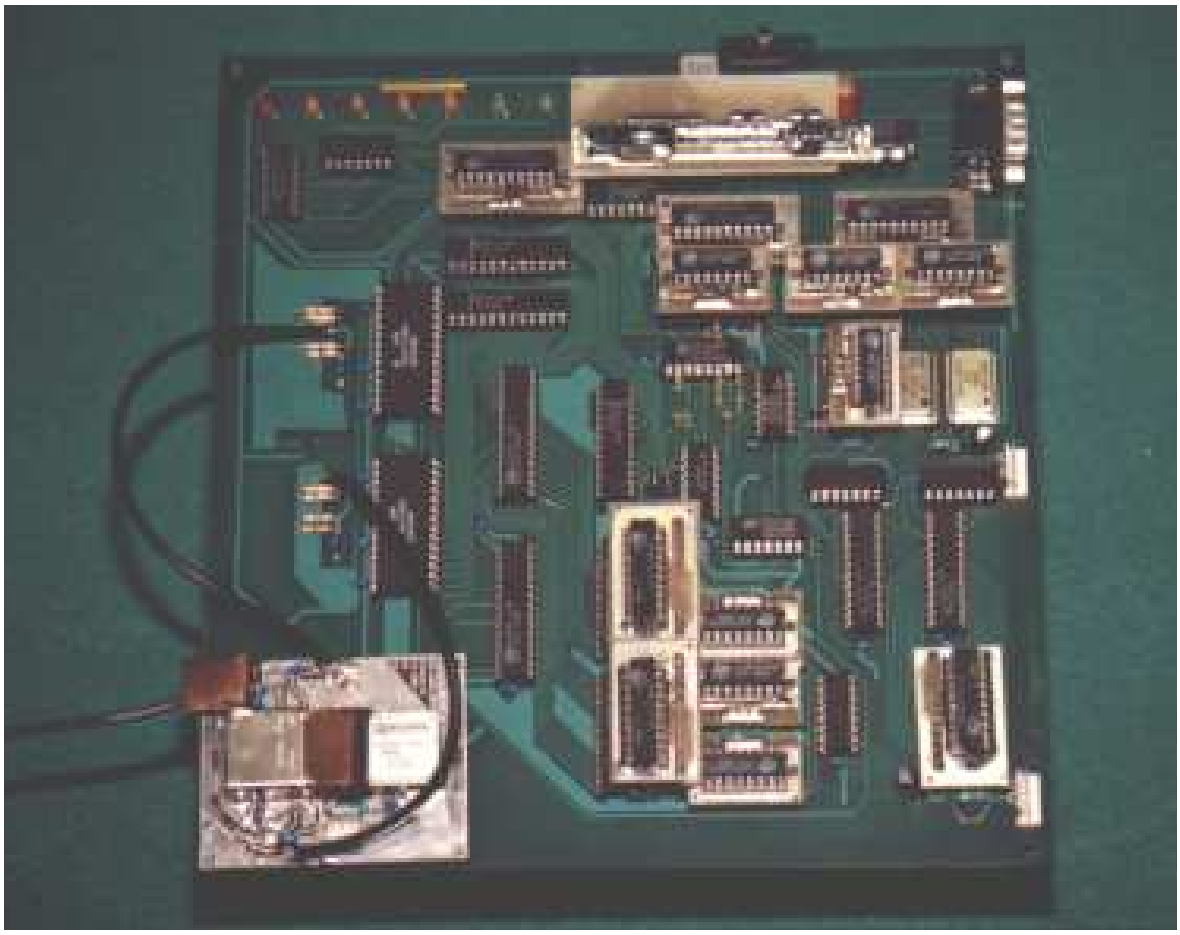

FIGURE 9.2: Complex DSSS transmitter hardware (First hardware version).

System control is achieved by means of a computer (PC) connected to a micro-controller (DS2250T). The board setup is done in software on the PC and then down-loaded to the micro-controller. The complex spreading sequences, used in the spreading process, are also initially down-loaded from the PC to the SRAMs of the transmitter board under the control of the micro-controller. Figure 9.3 shows a typical hardware setup for down-loading the setup configuration and spreading sequences. The length of the spreading sequence is chosen to equal the length of one data bit in the balanced QPSK configuration, or equal to one symbol in the dual channel QPSK configuration. The sampling clock on the board is used to clock the address counters, SRAMs and DACs, while the sampling clock is divided by a factor $S = spc * L$ to produce the data symbol clock, where spc represents the number of samples per chip in the sampled system and L the spreading sequence length. This symbol clock

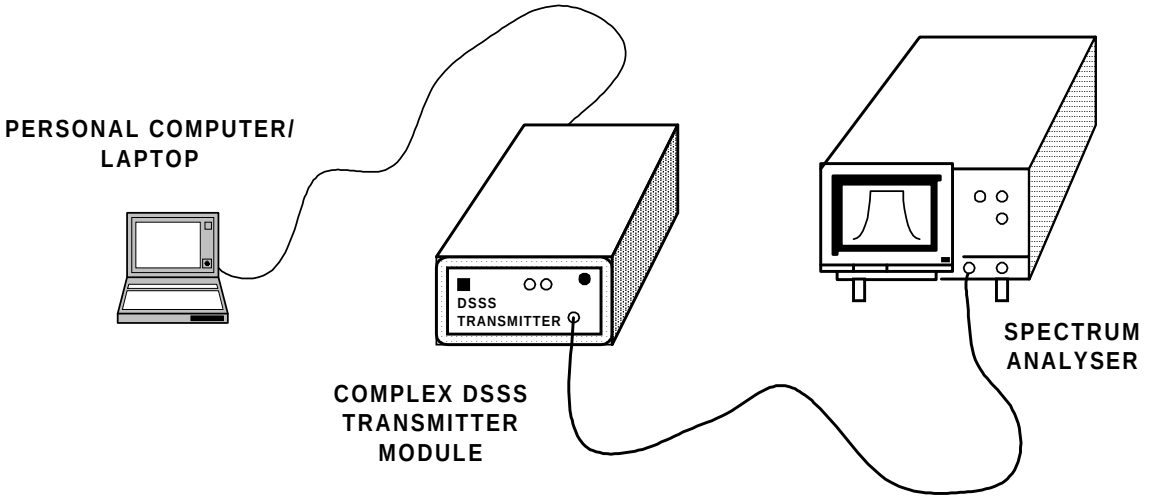

FIGURE 9.3: Hardware during down-loading of setup configuration and spreading sequences (First hardware version).

is used to clock the data latch in the input stage. It is also necessary to produce a double frequency clock to clock the data into the serial-to-parallel (S/P) converter in the case of the dual channel QPSK configuration, whereafter the clock is divided by two to clock the parallel I and Q symbol streams after S/P conversion of the input data. The complex DSSS transmitter unit, used in this setup, can be seen in Figure 9.4.

Using analytical complex spreading sequences, generated as described in Chapter 3, a SSB output signal is obtained, resulting in a 50% saving in bandwidth compared to DSB binary phase shift keying (BPSK). Since the latter two systems support identical data throughput, a 3dB processing gain (PG) advantage is obtained with the SSB system relative to the BPSK system. The 3dB PG can either be achieved by doubling the data rate of the SSB relative to the BPSK system, or by using double length spreading sequences for the same data rate and identical bandwidths. However, compared to the DSB dual channel (QPSK) transmitter configuration, the balanced quadrature configuration used to obtain the SSB result leads to a reduction of data throughput rate by a factor of two. The 50% bandwidth advantage of the balanced SSB system is thus neutralised by the factor of two reduction in data throughput rate relative to the dual channel (QPSK) system, resulting in 0dB PG advantage overall, i.e., the two systems potentially have identical performance. Any differences in performance will therefore be due to differences in cross-correlation properties between the two families of spreading sequences employed in each case, namely the analytically bandlimited complex (ABC) sequences used in the SSB case, and the generalised chirp-like (GCL) sequences used in the DSB case (refer [25] for details). It should be finally noted

FIGURE 9.4: The complex DSSS transmitter unit (First hardware version).

that the output signals produced by all the aforementioned systems exhibit perfectly constant envelopes (CE), which is a unique result in the SSB case. The CE SSB feature is achieved through a unique combination of a balanced QPSK structure and the use of ABC CSS.

The transmitter not only facilitates the use of binary or complex spreading sequences, but the sequences can be pre-filtered before they are down-loaded to the transmitter board. This feature makes it possible to use any type of filtering which can be implemented in software. For example in the case of binary spreading sequences, filters with different roll-off factors, like the Nyquist filter, can be easily implemented. The latter is not always that simple to implement in practice, and the results are more ideal as would ever be the case for conventional lumped hardware systems. The results illustrating this concept can be seen in section 9.3 of this chapter.

The balanced QPSK and dual channel QPSK DSSS transmitter configurations can, with minor modifications, be extended to also generate $\pi/4$-QPSK, 8-PSK or 7x1-PSK modulation formats [21, 41–43]. The signal constellations for these modulation configurations are shown in Figure 9.5. When either $\pi/4$-QPSK, QPSK, 8-PSK or 7x1-PSK mode is selected, the incoming data is firstly serial-to-parallel converted. This is followed by combinational logic (precoder) to Gray and differentially encode the serial-to-parallel converted data into symbols which are then appropriately mapped onto the selected M-PSK

signal constellation in the following way: The output of the precoder is used to control logic which generates the starting address of a pair of spreading sequences. These spreading sequences are weighted by scale factors corresponding with the X and Y -coordinates of the signal constellation point, onto which the symbol to be transmitted, is to be mapped. The mapping is accomplished by reading the selected pair of spreading sequences from the SRAMs under control of the micro-controller.

The real and imaginary parts of the spreading sequence can be pre-modulated onto cosine and sine carriers at an intermediate frequency, f_{IF}, (usually chosen to be equal to the chip frequency, f_{chip}), before they are stored in RAM. This is done by multiplying the four times over-sampled real and imaginary components of the complex spreading sequence by repetitive $(1, 0, -1, 0)$ and $(0, 1, 0, -1)$ sequences, respectively, constituting the cosine and sine modulation processes, [44–46]. This modulation method produces an IF output signal at a quarter of the sampling frequency. No unwanted spectral components are generated by means of this modulation method and thus less filtering is required.

Figure 9.6 shows version 2 of the DSSS transmitter module, which also includes parts of the receiver.

9.2.1 TRANSMITTER SPECIFICATIONS

In this section f_{sample} denotes the sampling frequency at which the system is clocked, f_{chip} the chip frequency, spc the number of samples per chip and L the length of the spreading sequence. For the chirp-like sequences the (DSB) transmission bandwidth on the carrier is

$$\begin{aligned} B_T &= \frac{f_{sample}}{spc} \\ &= f_{chip} \quad [Hz] \end{aligned} \tag{9.1}$$

It should be noted that the spectral shaping obtainable with the NLI-RU filtered GCL CSS approaches that of a Nyquist filter with roll-off factor $\alpha = 0$ for sufficiently long sequence lengths L. Since Nyquist filters with $\alpha = 0$ are hard to realise in practice, realistic Nyquist bandwidths equal that defined in Equation 9.1, multiplied by the factor $(1 + \alpha)$, giving the NLI-RU filtering process an α bandwidth advantage compared to conventional Nyquist applications.

The data rate, f_b, depends on the available spreading bandwidth B_T, the chosen family of spreading sequences and the spreading sequence length, L, within a specific family, the

maximum spreading sequence length being limited to $L_{max} = 1024$ for this system.

$$f_b = \frac{f_{chip}}{L} \quad [bps] \tag{9.2}$$

The primary system specifications are summarized in Table 9.1.

PARAMETER	SPECIFICATION
Modulation Technique	Balanced/Dual channel QPSK DSSS
Spreading Sequences	Families of binary (Gold/Kasami) or complex (GCL)
Sequence Lengths	L (selectable up to 1023 - see Tables 9.2 and 9.3)
Data rate	f_b (selectable - see Tables 9.2 and 9.3)
Processing Gain	$PG = 10logL$ (see Tables 9.2 and 9.3)
Chip rate	$f_{chip} = 12.5Mchips/s$
Samples per chip	$spc = 4$
Sampling frequency	$f_{sample} = 50MSPS$
RF Carrier frequency	$f_{RF} = 1.85GHz$
Transmission bandwidth	$B_T = 12.5MHz(DSB) or B_T = 6.25MHz(SSB)$

TABLE 9.1: Complex DSSS transmitter specifications.

The typical data rates and processing gains achievable by the DSSS transmitter module is given in Tables 9.2 and 9.3 (other options are also available and can be obtained through simple software adjustments).

CODE LENGTH	PROCESSING GAIN [dB]	DATA RATE [kbps]
63	17.99	198.41
127	21.04	98.43
255	24.07	49.02
511	27.08	24.46
1023	30.10	12.22

Table 9.2: PGs and data rates obtainable with Gold and Kasami (binary) spreading sequences at a chip rate of $f_{chip} = 12.5Mchips/s$.

CODE LENGTH	PROCESSING GAIN [dB]	DATA RATE [kbps]
49	16.90	255.10
121	30.83	82.64
169	22.28	73.96
289	24.61	43.25
361	25.58	34.63
529	27.23	23.63
841	29.25	14.86
961	29.83	13.00

Table 9.3: PGs and data rates obtainable with General Chirp-Like (GCL) spreading sequences at a chip rate of $f_{chip} = 12.5 Mchips/s$

9.3 PRACTICAL HARDWARE RESULTS

For comparative purposes, Figure 9.7 depicts the spectrum of the output of the DSSS transmitter when using Nyquist filtered binary (Gold) spreading sequences of length 511, modulated onto a $1.85\ GHz$ RF carrier. Figure 9.8 shows the output spectrum of the DSSS transmitter, modulated onto a $1.85\ GHz$ RF carrier, for the case where DSB root-of-unity filtered complex spreading sequences (RU-CSS) of length 529 were used for spreading. Figure 9.9 shows the spectrum of the output of the DSSS transmitter when non-linearly-interpolated root-of-unity filtered complex spreading sequences (NLI-RU-CSS, $N = 529$), [4], are used. Note that, the bandwidth of the output of the balanced SSB DSSS transmitter, using ABC NLI-RU-CSS, is only half of that produced by the dual channel DSB DSSS transmitter, using GCL NLI-RU-CSS. The data throughput rate of the former system is however two times lower than the latter system, resulting in identical processing gains, as explained in section 9.2.

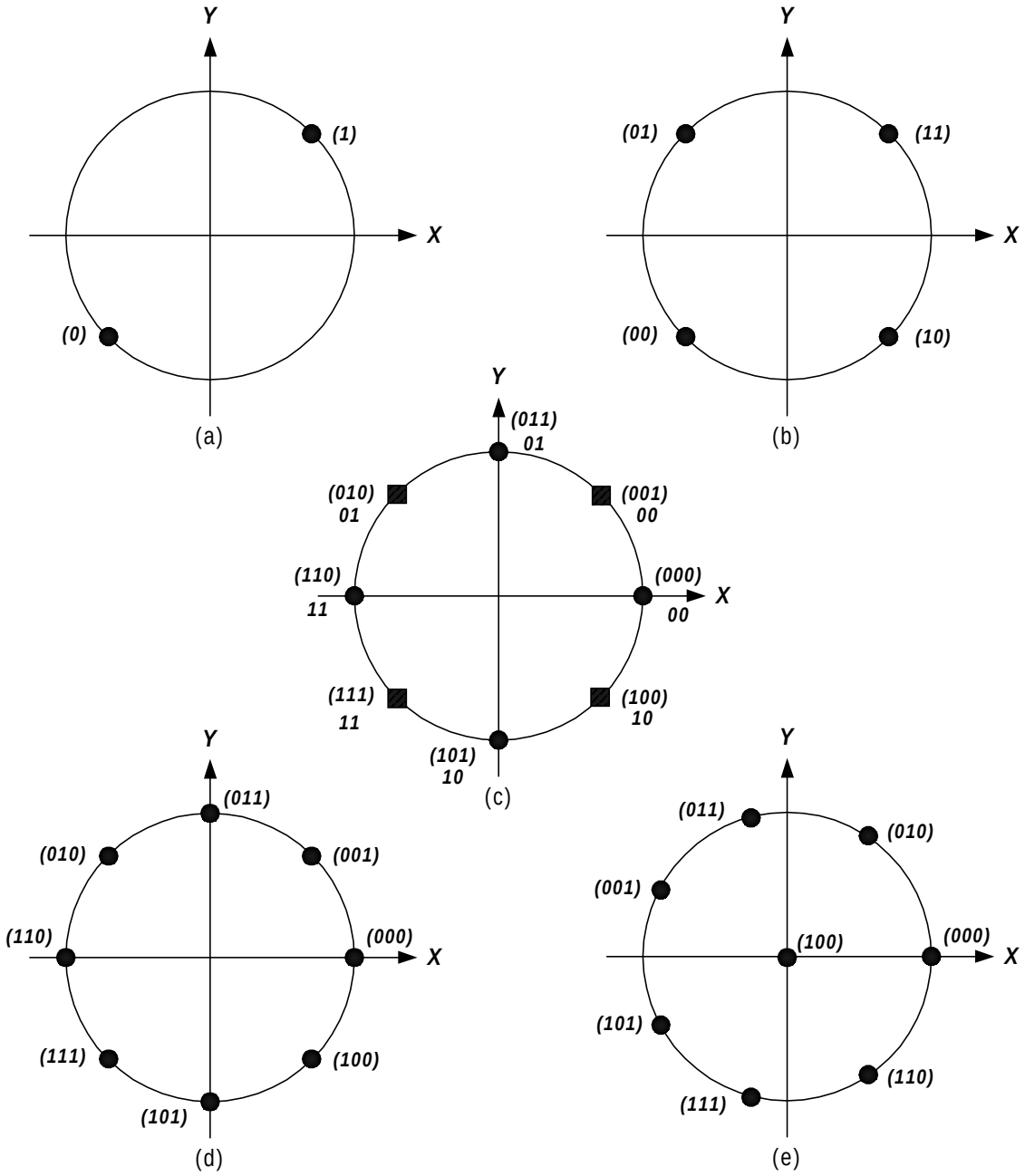

FIGURE 9.5: Signal constellations for the different modulation schemes: (a) Balanced QPSK, (b) Dual channel QPSK, (c) $\pi/4 - QPSK$, (d) 8-PSK and (e) 7x1-PSK.

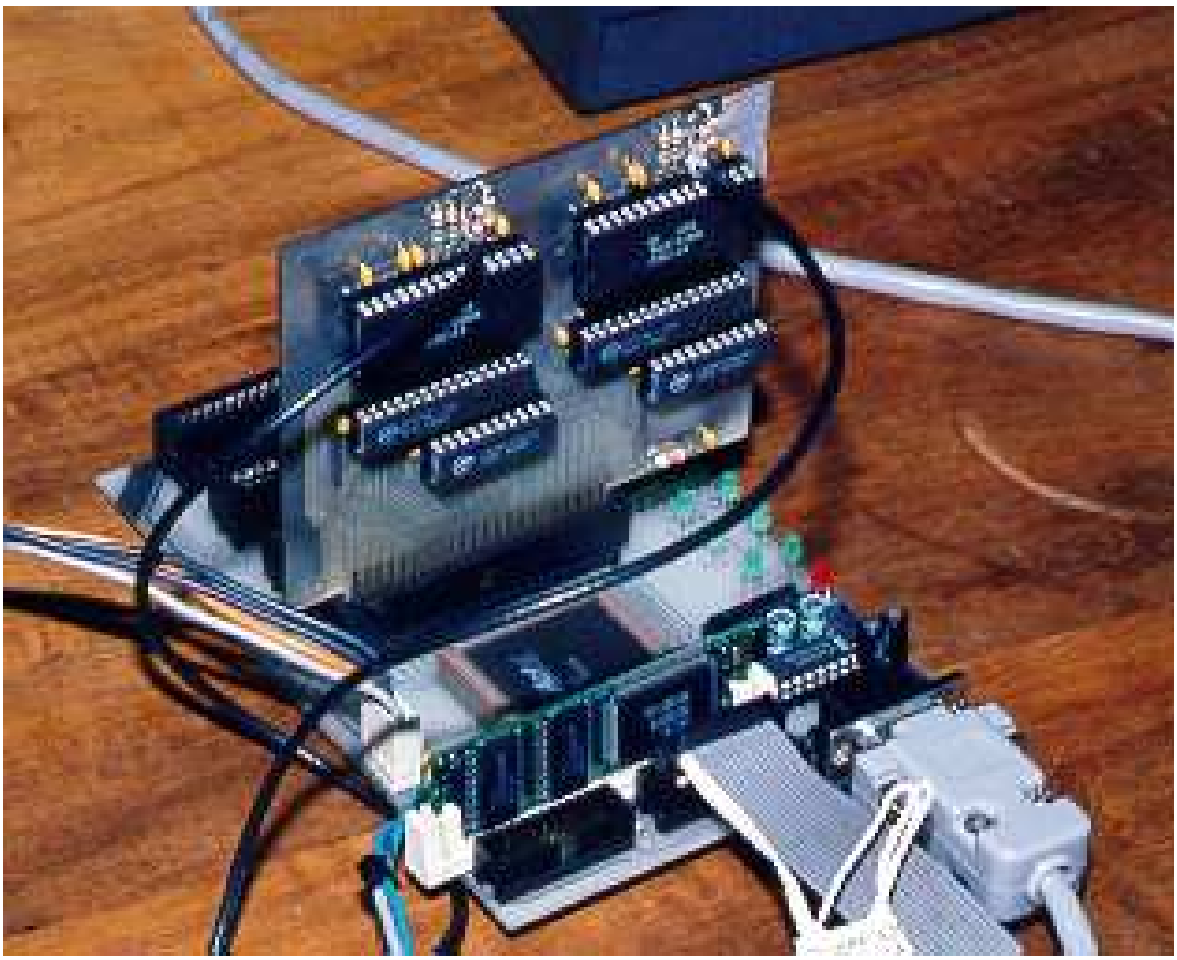

FIGURE 9.6: Second hardware version of the DSSS transmitter, including parts of the receiver.

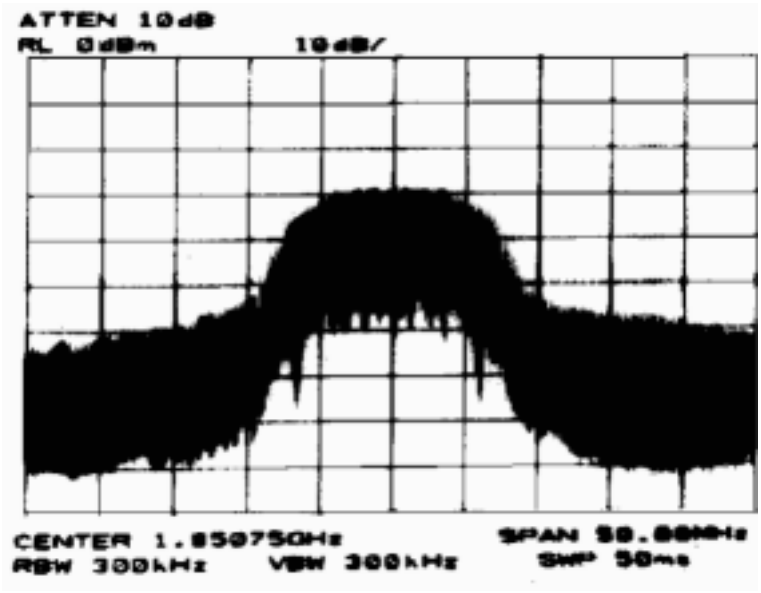

FIGURE 9.7: Spectrum of the output of the DSSS transmitter using binary (Gold) spreading sequences of length 511.

9.4 TYPICAL APPLICATIONS

As an example of the versatility and applicability of the proposed DSSS transmitter, it may be mentioned that the hardware prototype has been used in a channel sounding application to measure the delay-spread profile of various communication channels, including DECT and GSM (i.e., at different carrier frequencies). Other applications include various types of channel sounding, accurate distance and signal path delay measurements, radar applications and more.

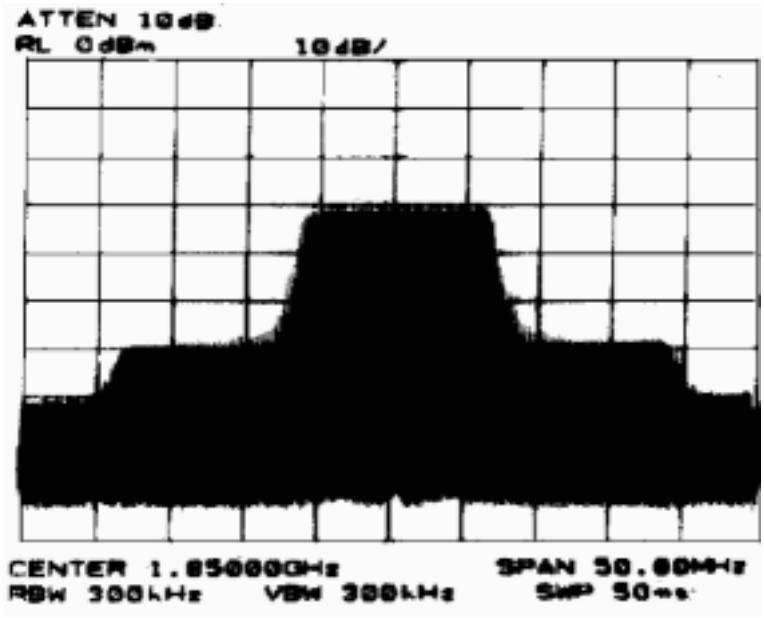

FIGURE 9.8: Spectrum of the output of the DSSS transmitter, modulated onto a $1.85\ GHz$ RF carrier, for the case where DSB root-of-unity filtered complex spreading sequences (RU-CSS) of length 529 were used.

[htb]

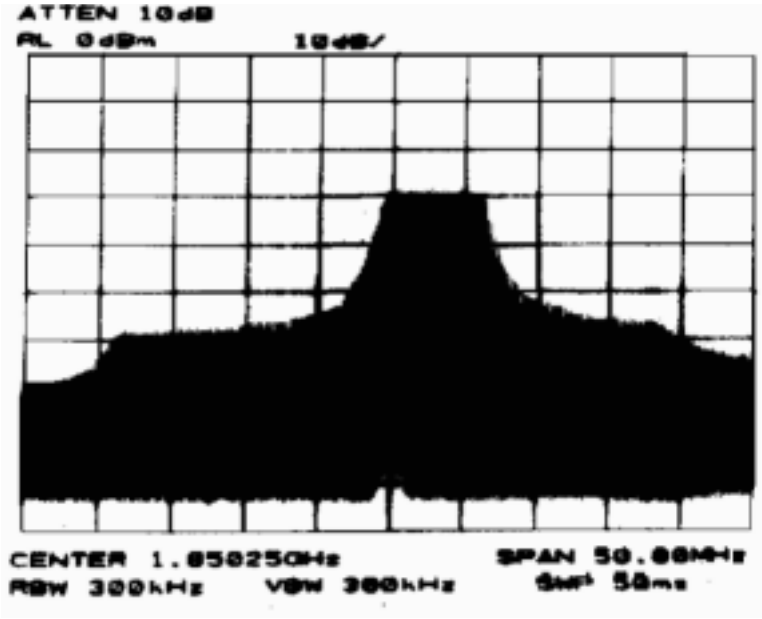

FIGURE 9.9: Spectrum of the output of the DSSS transmitter, modulated onto a $1.85\ GHz$ RF carrier, for the case where SSB non-linearly-interpolated root-of-unity filtered complex spreading sequences (NLI-RU-CSS) of length 529 were used.

CHAPTER TEN

IMPLEMENTATION OF THE GENERIC FPGA-BASED COMPLEX DSSS MODEM

10.1 INTRODUCTION

The results of the previous chapters serve to illustration the power and value of a simulation platform. The simulation results, presented in Chapter 8, is of inestimable value and will be used as a baseline in the implementation of the DSSS modem. The aforementioned theoretical structures and schemes were implemented in hardware by utilizing Altera's FPGA technology. In the initial design of the complex DSSS transmitter and receiver, most of the baseband processing was done by means of Altera's FPGA technology in VHDL. The rest of the system, and particularly the IF and RF subsystems, was realised with analog components. IF sampling principles were applied at the receiver and implemented on FPGA using VHDL programming software, resulting in a number of advantages compared to analog down-conversion and carrier tracking. The hardware results of the complex DSSS communication system are presented in this chapter. Complete system specifications are presented, as well as a brief description of the operation of the DSSS system.

10.2 HARDWARE DESCRIPTION

10.2.1 DSSS Modem Module

10.2.1.1 Hardware Design of DSSS Modem, Version One

The block diagram of the first hardware designed version of the complete DSSS modem is depicted in Figure 10.2. In this version of the DSSS modem, most of the IF, RF, carrier recovery, down-conversion, filtering, etc. were done by means of external hardware components, while the baseband processing is done inside the FPGA. On the transmit side the digital-to-analog converted DAC) baseband in-phase and quadrature data branches are modulated onto a $70\ MHz$ IF carrier frequency by means of a quadrature modulator. The IF is then up-converted to an RF frequency of $2.4415\ GHz$, which falls within one of the Industrial, Scientific and medical (ISM) frequency bands. On the receive side the received signal is first bandpass filtered and amplified by means of a low noise amplifier (LNA), whereafter it is again band pass filtered. The $2.4415\ GHz$ RF signal is down-converted to a $70\ MHz$ IF frequency, bandpass filtered and automatic gain controlled (AGC). This $70\ MHz$ IF signal is quadrature down-converted to provide baseband in-phase and quadrature branches, which are analog-to-digital converted. A quadrature down-converter with a voltage controlled oscillator (VCO) and external tank circuit, was used for the final down-conversion stage as well as for part of the carrier recovery loop. The phase detector, etc. parts of the carrier recovery loop were done inside the baseband processing block in FPGA. A DAC is used for conversion of the carrier recovery error signal to an analog signal to control the external VCO in the carrier recovery loop. The data spreading and despreading are done inside the FPGA as part of the baseband processing. The data source can be a voice codec or any other external device that generates data to be transmitted, as illustrated in Figure 10.2. Hardware boards developed to implement the first few versions of the DSSS communication system are shown in Figure 10.1.

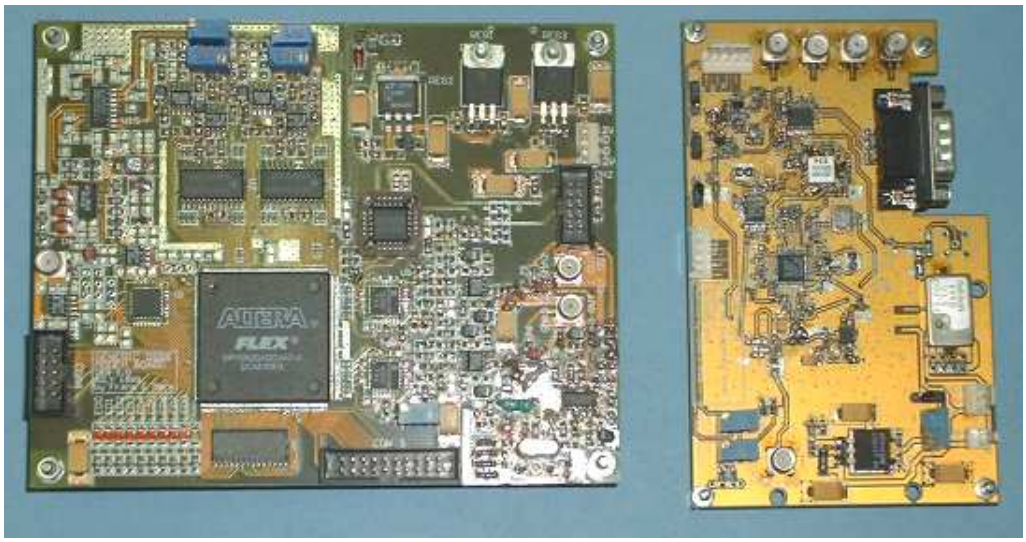

FIGURE 10.1: Hardware boards of the first design version of the DSSS modem. The FPGA board with the baseband processing on the left and the IF/RF board on the right.

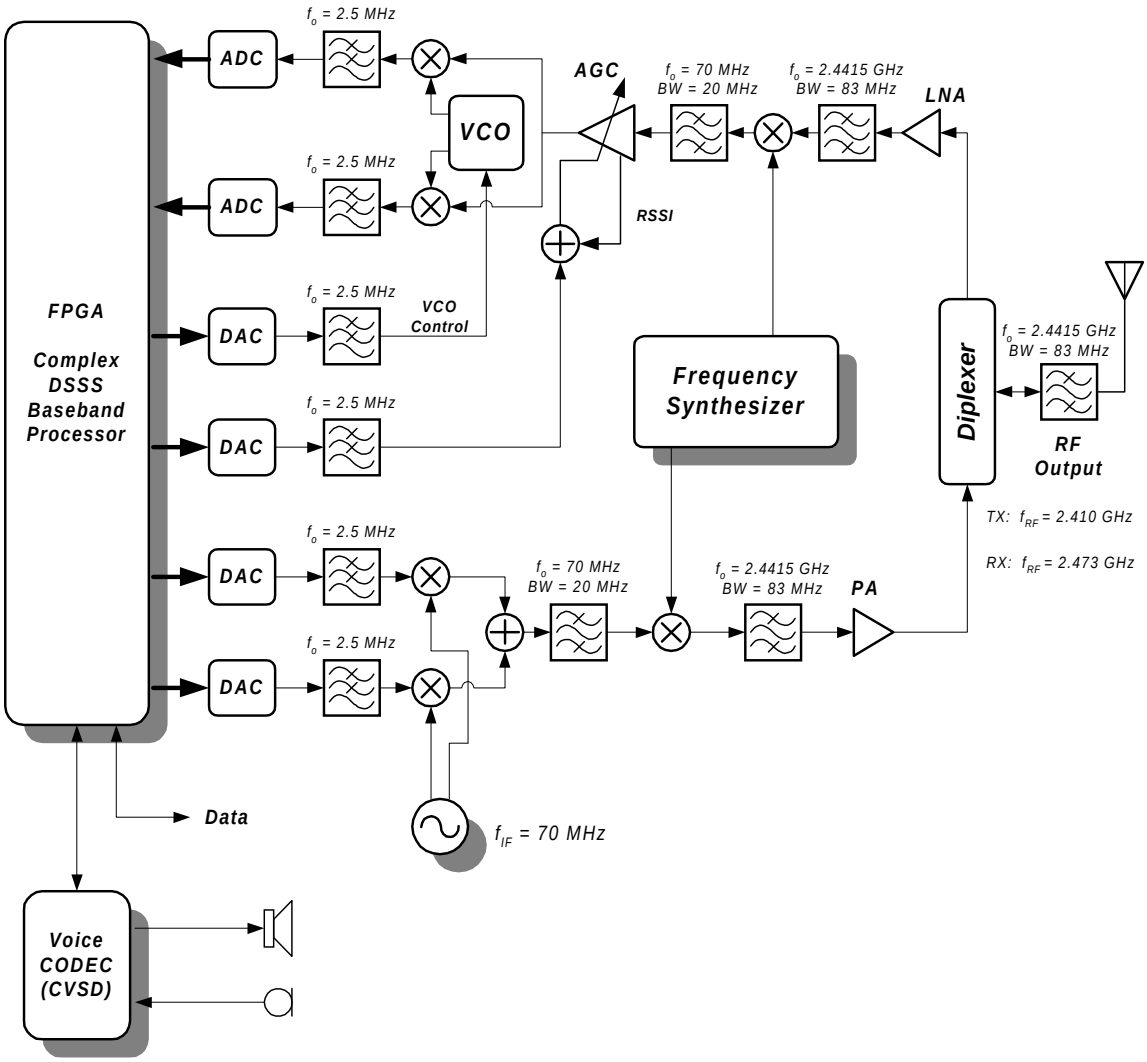

FIGURE 10.2: Block diagram of the first designed hardware implementation of the complex DSSS modem structure.

10.2.1.2 Hardware Design of the DSSS Modem Employing CSS: Final Version

The final design and implementation of the DSSS modem, consisting of the transmitter and receiver blocks, are shown in Figures 10.3 and 10.4, respectively. The hardware setup of the final DSSS modem is depicted in Figure 10.7.

Two generic FPGA based DSP platforms were developed on which the DSSS modem was implemented. The FPGA development boards each consist of four $20K600E$ FPGA chips. The FPGA development platform has a system clock of $80\ MHz$. This system clock is used to clock all the FPGAs, on the board as well as the DACs and ADCs needed to establish communication to and from the DSSS modem.

The DSSS modem structure consists of a voice CODEC, complex DSSS baseband processor, IF section and RF section. The complex DSSS baseband processor contains the DSSS transmitter core software, receiver, code acquisition, code tracking, IF sampling, numerically controlled oscillator (NCO), carrier phase tracking, automatic gain control (AGC), interfacing with the data source and voice CODEC as well as the overall setup and control of the DSSS modem module. The interfacing with the IF section and control signals is done by means of ADC and DAC circuitry.

10.2.1.3 DSSS Modem Transmitter Module

The DSSS transmitter, shown in Figure 10.3, accepts binary data as input. These data bits, are firstly differentially encoded and then spread using composite complex spreading sequences. The spreading block, differential encoding, spreading code generator, code control and clock generators forms part of the DSSS baseband processor. This baseband processor runs at a system / sample clock speed of $80\ MHz$. The baseband in-phase and quadrature phase branches, generated at the transmitter, are converted to analog signals by means of two DACs. These analog signals are then lowpass filtered, modulated onto an $850\ MHz$ cosine and sine RF frequency and summed, by means of a quadrature modulator. The lowpass filtering following the DACs does not perform shaping, but eliminates unwanted frequency components due to sampling. This RF output is bandpass filtered, amplified and finally transmitted via an antenna.

10.2.1.4 DSSS Modem Receiver Part

With reference to Figure 10.4, the signal received from the antenna is amplified by a low noise amplifier (LNA), bandpass filtered at a RF centre frequency of $850\ MHz$

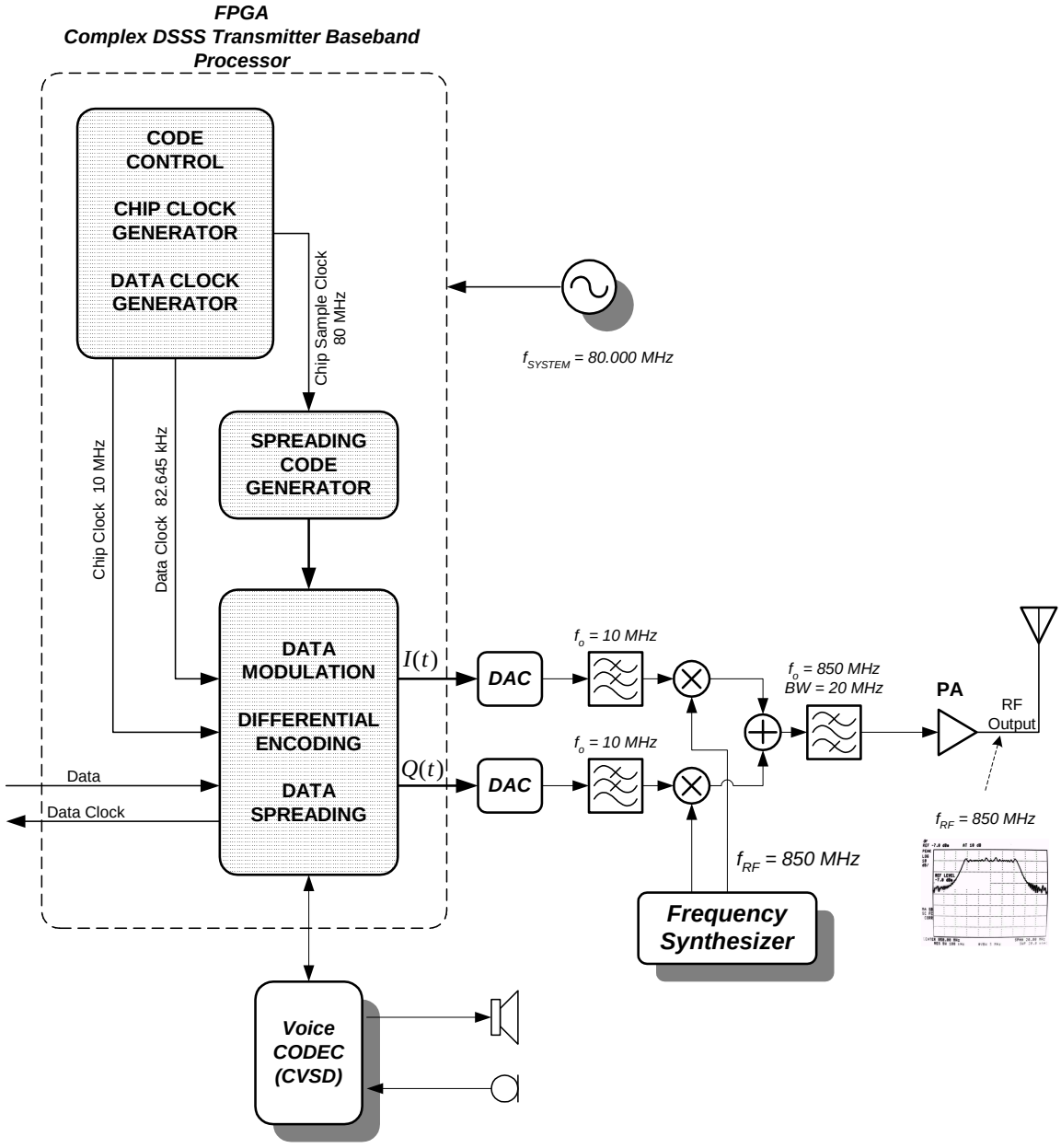

FIGURE 10.3: Block diagram of the final hardware implementation of the transmitter part of the DSSS modem employing CSS.

down-converted to $70\ MHz$ IF frequency. The $70\ MHz$ IF signal is passed through a bandpass SAW filter to eliminate all noise and interference power outside the relevant spreaded data bandwidth. The $70\ MHz$ IF is again down-converted to a secondary IF frequency of $16\ MHz$, which is low enough to be IF-sampled at a sampling rate of $80\ Msps$. Automatic gain control (AGC) is also performed on this IF-signal to ensure full range quantization on the ADC input. The control signal of the AGC is generated by using the measured average voltage level of the sampled IF signal, which is compared to a pre-specified reference level, in order to control the gain of the AGC amplifier. This enables a full range voltage input signal to be delivered to the ADC.

In the complex DSSS baseband processor FPGA the sampled $16\ MHz$ IF signal is down-converted to a baseband in-phase and quadrature branch, by means of a quadrature demodulation block. The quadrature local oscillator (LO) is provided by a numerically controlled oscillator (NCO), which forms part of a decision-directed Costas carrier-recovery-loop (DD-CCRL). A decision-directed complex delay-locked-loop (DD-CDLL) operates in parallel with the DD-CCRL, to track the received and locally generated spreading codes to within one chip period. The punctual complex spreading codes generated by the DD-CDLL are used in the DD-CCRL in the despreading process of the data. The recovered quadrature carriers, provided by the DD-CCRL, are used in the DD-CDLL to demodulate the incoming IF signal into two quadrature baseband branches, despreaded by the unique composite signals, to produce an error signal as described in Chapters 5 and 6. The combination of these two synchronization blocks, operating as jointly as one combined unit, in effect achieves a dual diversity gain, and provides superior performance compared to two independent tracking loops, controlled by two separate tracking error signals, as illustrated by Proakis in [21] p.333. An illustration of how the periodic autocorrelation function is affect by the combined code tracking and carrier recovery operation is illustrated in paragraph 6.6 Figure 6.10.

The spreading code acquisition operates in parallel with the combined synchronization block. The function of the acquisition process is to ensure alignment of the received and locally generated spreading codes within one chip period. This coarse code synchronization forms part of the initial synchronization phase. After this initial acquisition phase, the DD-CDLL swithes over into closed-loop operation mode for fine and accurate code tracking.

The numerically controlled chip clock generator (NCCCG), controlled by the DD-CDLL, drives the complex spreading code generator. The complex spreading code generator produces the two punctual combinations of complex spreading sequences, used in the data

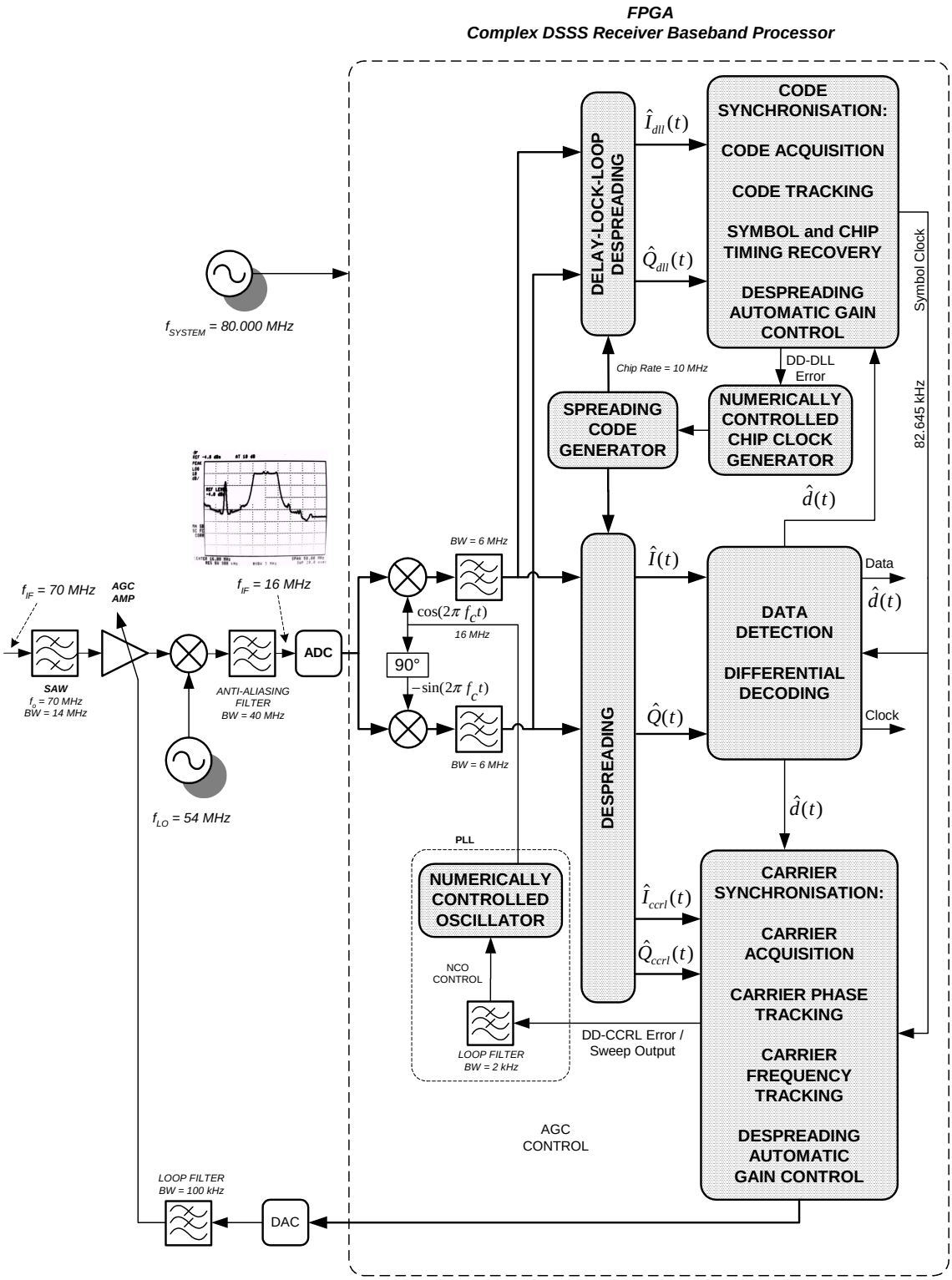

FIGURE 10.4: Block diagram of the hardware implementation of the final receiver of the DSSS modem employing CSS.

despreading process. It also produces the composite pair of combinations of complex spreading sequences, used by the DD-CDLL to generate the control error signal for controlling the NCCCG. The DD-CDLL automatically recovers the symbol timing by fine tracking the spreading code within one chip period.

10.2.2 Voice CODEC Module

A voice CODEC, as depicted in Figure 10.5, digitally encodes the incoming voice signal from a microphone, which is automatic gain controlled. It also decodes the received data and provides an analog signal, which is amplified to drive a speaker.

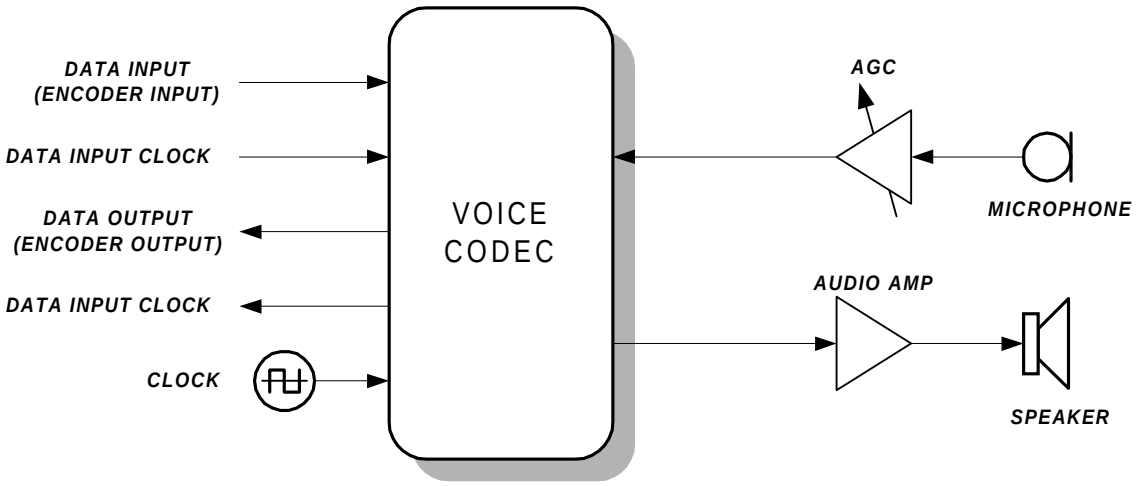

FIGURE 10.5: Block diagram of the audio front-end.

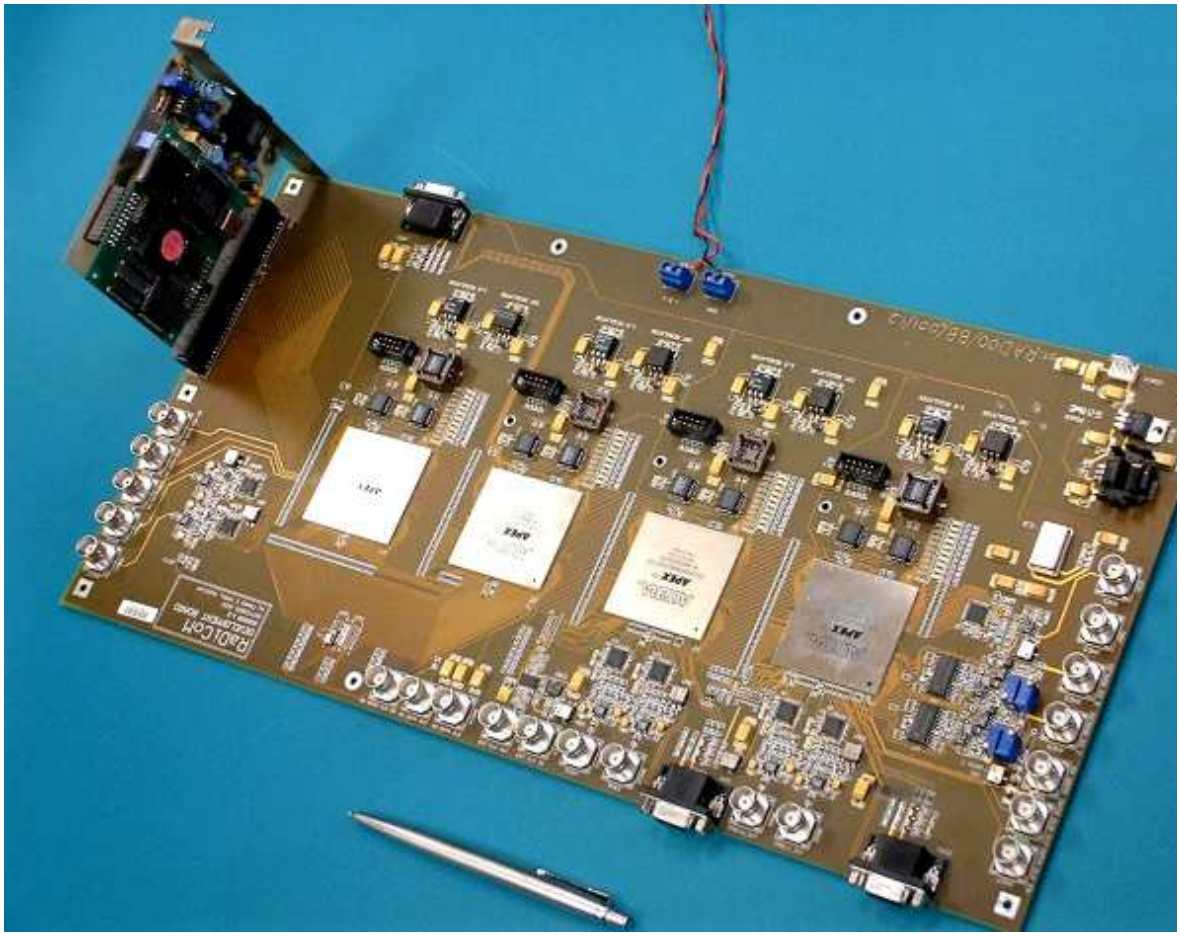

FIGURE 10.6: FPGA development board used as development platform for the DSSS modem employing complex spreading sequences.

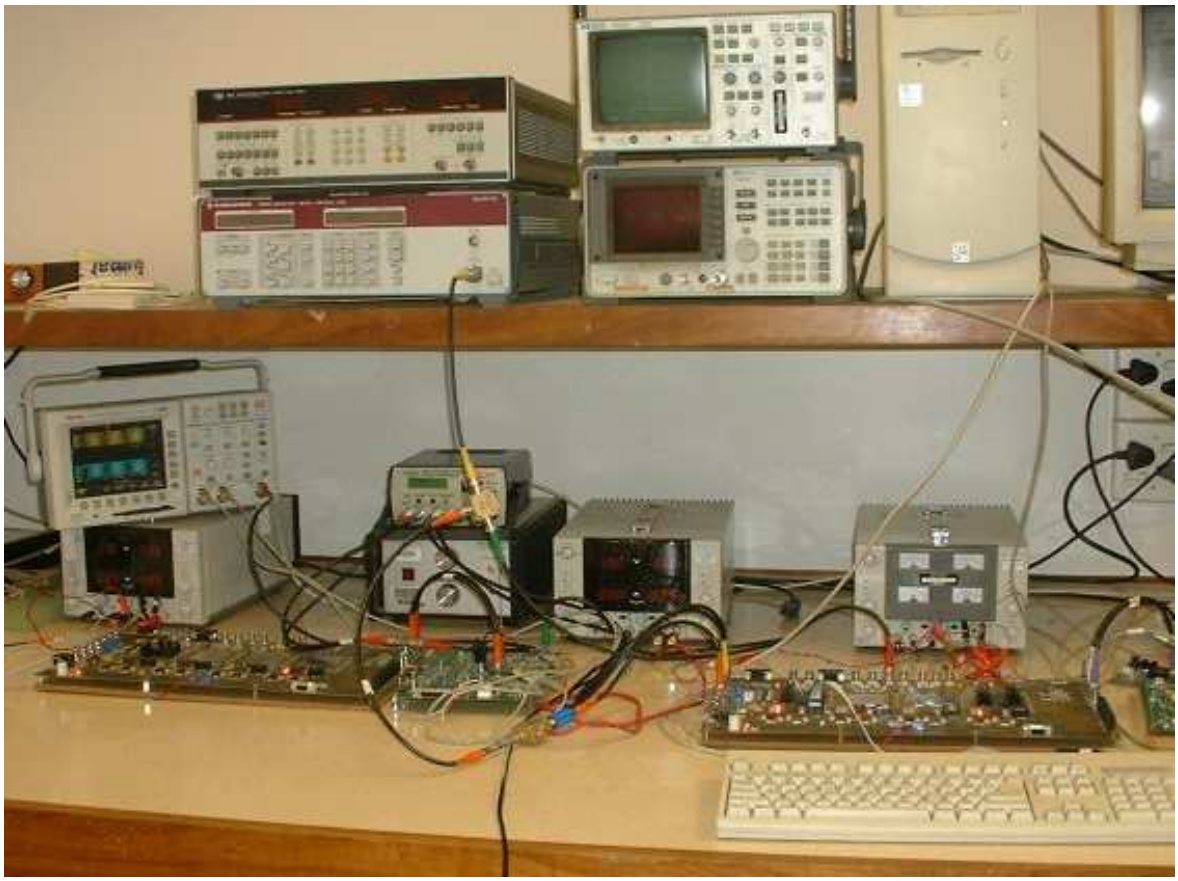

FIGURE 10.7: The hardware setup of the final DSSS modem employing CSS.

10.3 SYSTEM SPECIFICATIONS

The system specifications for the DSSS modem are given in Table 10.1. This table includes both the first design version specifications and the final design system specifications for the DSSS modem employing CSS. The system can easily be software configured to establish a system with different spreading sequence length, processing gain (PG) , data rate, transmission bandwidth, balanced or dual mode DSSS QPSK modulation, system sample frequency, etc. Some of these options are summarized in Tables 10.2, 10.3 and 10.4.

PARAMETER	**SPECIFICATION**
BASEBAND PROCESSOR	
Modulation technique	Balanced/dual channel QPSK DSSS
Spreading sequence	Families of complex spreading sequences
Sequence length	L (selectable - see Tables 10.2, 10.3 and 10.4)
Data rate	f_b (selectable - see Tables 10.2, 10.3 and 10.4)
Processing gain	$PG = 10logL$ (see Tables 10.2, 10.3 and 10.4)
Chip rate	$f_{chip} = 5/10/20Mchips/s$
Samples per chip	$spc = 4/8$
Sampling frequency	$f_{sample} = 20/80MHz$
Baseband bandwidth	$B_B = 2.5/5/10MHz$
RF TRANSMIT MODULE	
TX intermediate frequency	$f_{IF_{TX}} = 70/280/374MHz$
TX RF carrier frequency	$f_{RF_{TX}} = 2442/850MHz$
Transmission bandwidth	$B_T = 5/10/20MHz$
RF RECEIVE MODULE	
RX intermediate frequency	$f_{IF_{RX}} = 70/16/8MHz$
RX RF carrier frequency	$f_{RF_{RX}} = 2442/850MHz$
AGC dynamic range	$30dB$
LNA noise figure	$2\ dB$

TABLE 10.1: Complex DSSS modem specifications

	BALANCED QPSK	DUAL CHAN QPSK		
	DATA RATE (kbps)	DATA RATE (kbps)	L	PG (dB)
1	454.55	909.09	11	10.41
2	384.62	769.23	13	11.14
3	333.33	666.67	15	11.76
4	294.12	588.24	17	12.30
5	217.39	434.78	23	13.62
6	172.41	344.83	29	14.62
7	161.29	322.58	31	14.91
8	138.89	277.78	36	15.56
9	102.04	204.08	49	16.90
10	81.97	163.93	61	17.85
11	79.37	158.73	63	17.99
12	41.32	82.64	121	20.83
13	39.37	78.74	127	21.04

Table 10.2: Gross data rates for the DSSS modem with various spreading sequence lengths (L) and processing gains (PG) (Transmission bandwidth of $5MHz$; Chip rate of $f_{chip} = 5Mcps$).

	BALANCED QPSK	DUAL CHAN QPSK		
	DATA RATE (kbps)	DATA RATE (kbps)	L	PG (dB)
1	909.09	1818.18	11	10.41
2	769.23	1538.46	13	11.14
3	666.67	1333.33	15	11.76
4	588.24	1176.47	17	12.30
5	434.78	869.57	23	13.62
6	344.83	689.66	29	14.62
7	322.58	645.16	31	14.91
8	277.78	555.56	36	15.56
9	204.08	408.16	49	16.90
10	163.93	327.87	61	17.85
11	158.73	317.46	63	17.99
12	82.64	165.29	121	20.83
13	78.74	157.48	127	21.04

Table 10.3: Gross data rates for the DSSS modem with various spreading sequence lengths (L) and processing gains (PG). (Transmission bandwidth of $10MHz$; Chip rate of $f_{chip} = 10Mcps$).

	BALANCED QPSK	DUAL CHAN QPSK		
	DATA RATE (kbps)	DATA RATE (kbps)	L	PG (dB)
1	1818.18	3636.36	11	10.41
2	1538.46	3076.92	13	11.14
3	1333.33	2666.67	15	11.76
4	1176.47	2352.94	17	12.30
5	869.57	1739.13	23	13.62
6	689.66	1379.31	29	14.62
7	645.16	1290.32	31	14.91
8	555.56	1111.11	36	15.56
9	408.16	816.33	49	16.90
10	327.87	655.74	61	17.85
11	317.46	634.92	63	17.99
12	165.29	330.58	121	20.83
13	157.48	314.96	127	21.04

Table 10.4: Gross data rates for the DSSS modem with various spreading sequence lengths (L) and processing gains (PG) (Transmission bandwidth of $20MHz$; Chip rate of $f_{chip} = 20Mcps$).

10.4 HARDWARE MEASUREMENT RESULTS

Several measurement results were obtained from the hardware prototype DSSS modem (transmitter and receiver), employing CSS. These measurement results are presented and discussed in this section. The DSSS modem was configured with a CSS of length, $L = 121$, number of samples-per-chip, $spc = 8$, chip rate, $f_{chip} = 10Mcps$, a corresponding data rate of $f_{data} = 82.645kbps$ and processing gain of $PG = 20.8dB$. The measured results are presented in the following sections.

10.4.1 Complex DSSS Transmitter (Modulator)

Figure 10.8 shows the spectrum of the non-return-to-zero (NRZ) serial input data before spreading with a frequency span of $280\ kHz$. The first null of the spectrum corresponds with the data symbol rate of $82.645\ kbps$. The measured spectrum of the in-phase and quadrature spread branches are shown in Figures 10.9 and 10.10, respectively, with a frequency span of $20\ MHz$. The in-phase and quadrature spread branch signals are depicted in Figure 10.11, with a zoomed-in version in Figure 10.12, showing the polarity changes in the periodic sequences due to the data information.

The effect of data spreading is illustrated in Figures 10.13 and 10.14. In Figure 10.13 the spectrum of the unspread data is shown, while the spectrum of the spread data ($L = 121$) is depicted in Figure 10.14, both with a frequency span of $20\ MHz$.

The in-phase branch versus the quadrature branch plot is depicted in Figure 10.15. This plot is an indication of the power envelope of the final output signal of the transmitter in a two dimensional communication system. For the case of the balanced and dual channel QPSK DSSS communication systems, employing CSS, the in-phase branch vs. quadrature branch forms a perfect circle, indicating that the power envelope of the signal to be transmitted, will be constant. The constant envelope feature of the DSSS QPSK system employing CSS yields multiple advantages. The most important advantage of the system is power efficiency, which is related to most of the other benefits. These benefits include a communication system with the ability to operate close to the power amplifier $1\ dB$ compression point, and, consequently, a communication system with higher output power for a given maximum available supply power, yielding an extended coverage area. The power efficiency advantages ultimately relates to longer battery life, which again facilitates cheaper cellular handsets.

The final output spectrum of the DSSS transmitter employing CSS is shown in Figure 10.16. The $-6\ dB$ double sided bandwidth of the output is $10MHz$, which is the same as

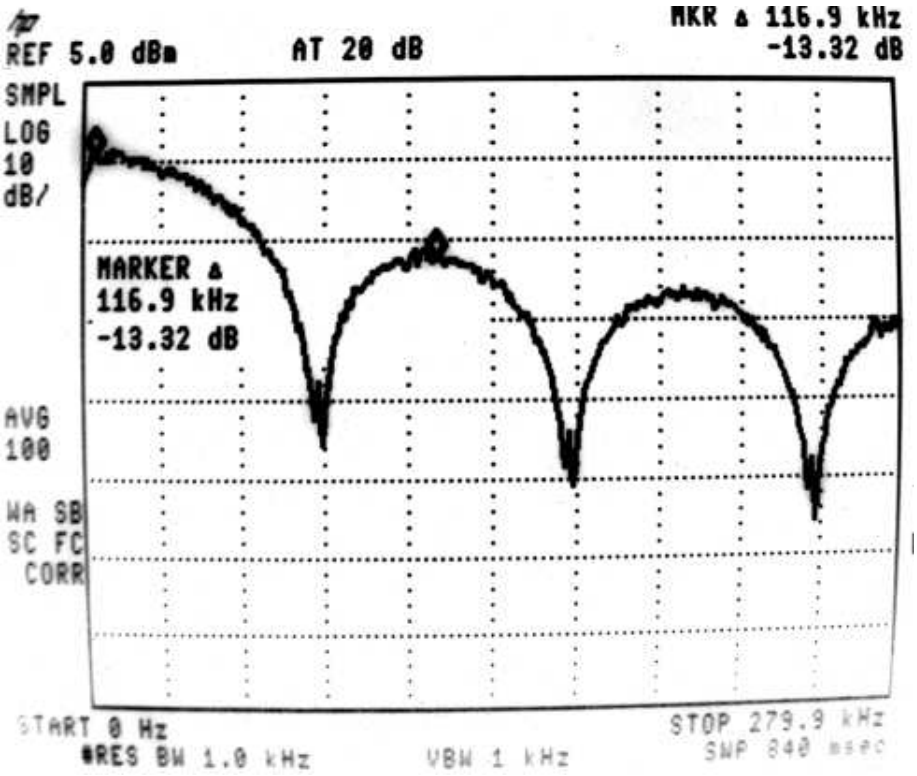

FIGURE 10.8: Spectrum of the NRZ serial input data before spreading.

the chip rate. This output spectrum is equivalent to that of a DSSS system employing binary spreading sequences filtered with a Nyquist filter with an effective roll-off factor of $\alpha = 0$ for sufficiently long spreading sequence lengths.

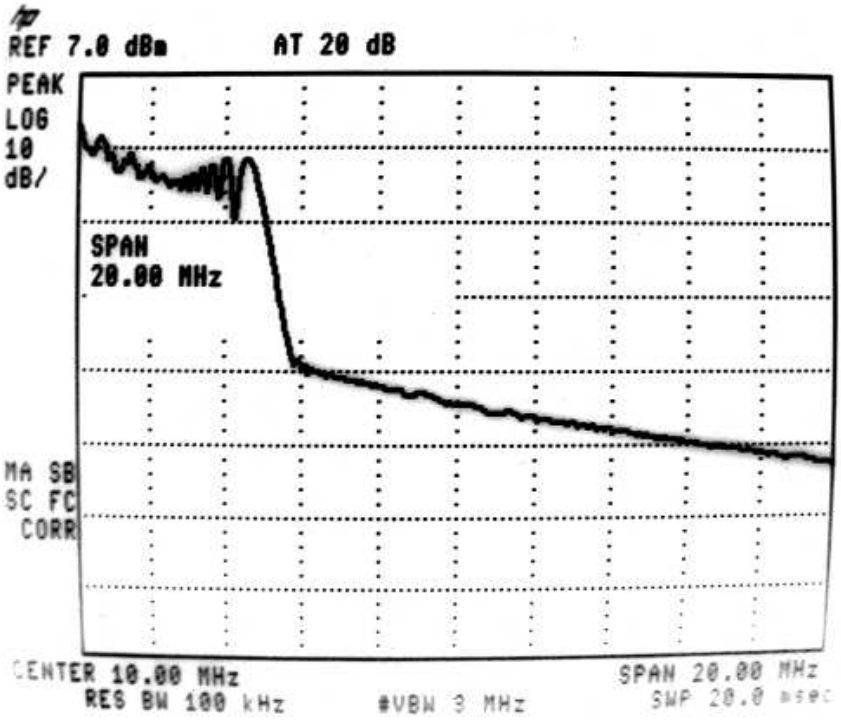

FIGURE 10.9: Measured spectrum of the in-phase branch composite complex spreading sequence in the DSSS transmitter.

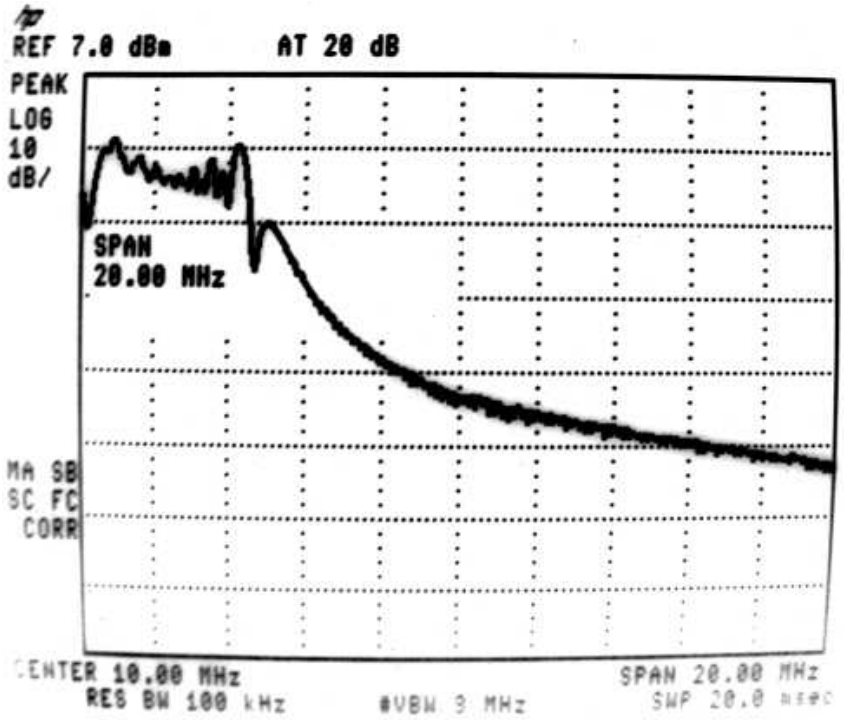

FIGURE 10.10: Measured spectrum of the quadrature branch composite complex spreading sequence in the DSSS transmitter.

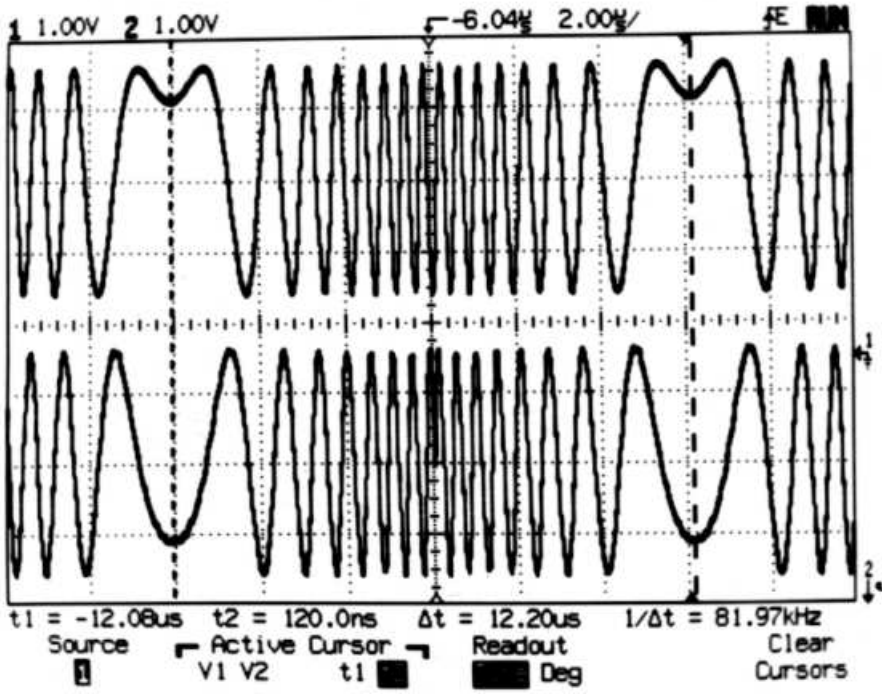

FIGURE 10.11: The two unique combinations of complex spreading sequences as implemented in the transmitter.

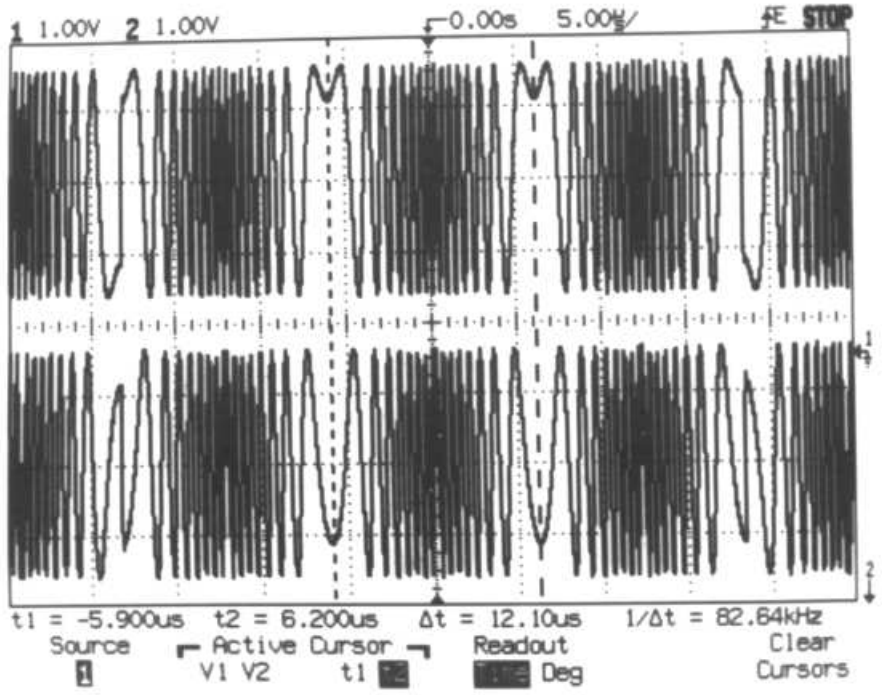

FIGURE 10.12: In-phase and quadrature phase branch signals, where the random data streams are spreaded with the unique combinations of complex spreading sequences, at the transmitter.

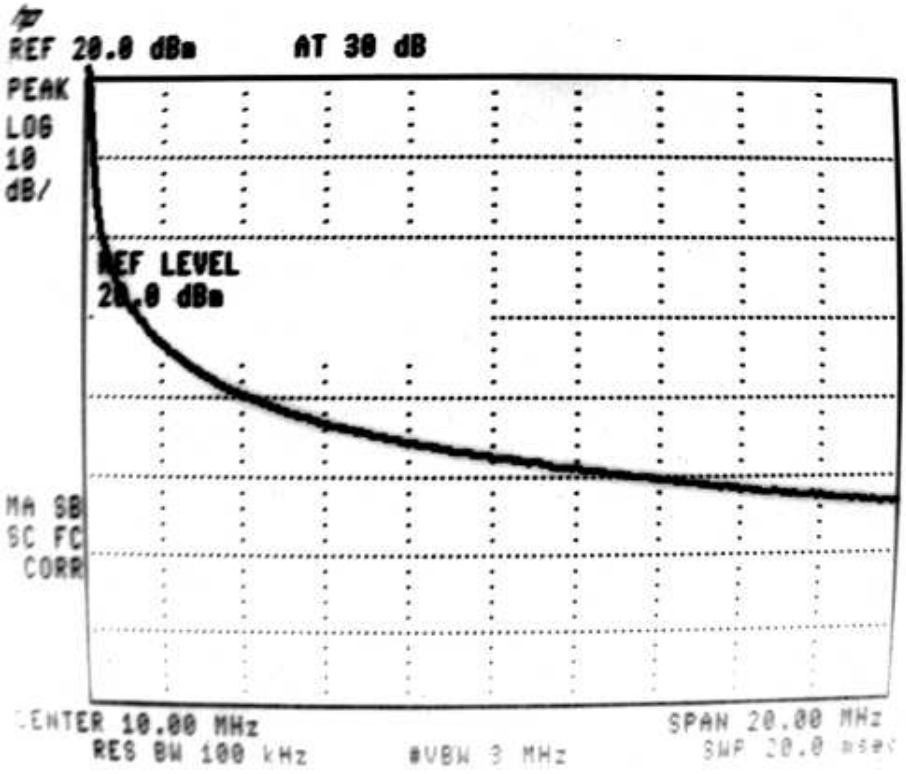

FIGURE 10.13: Spectrum of the NRZ serial input data before spreading.

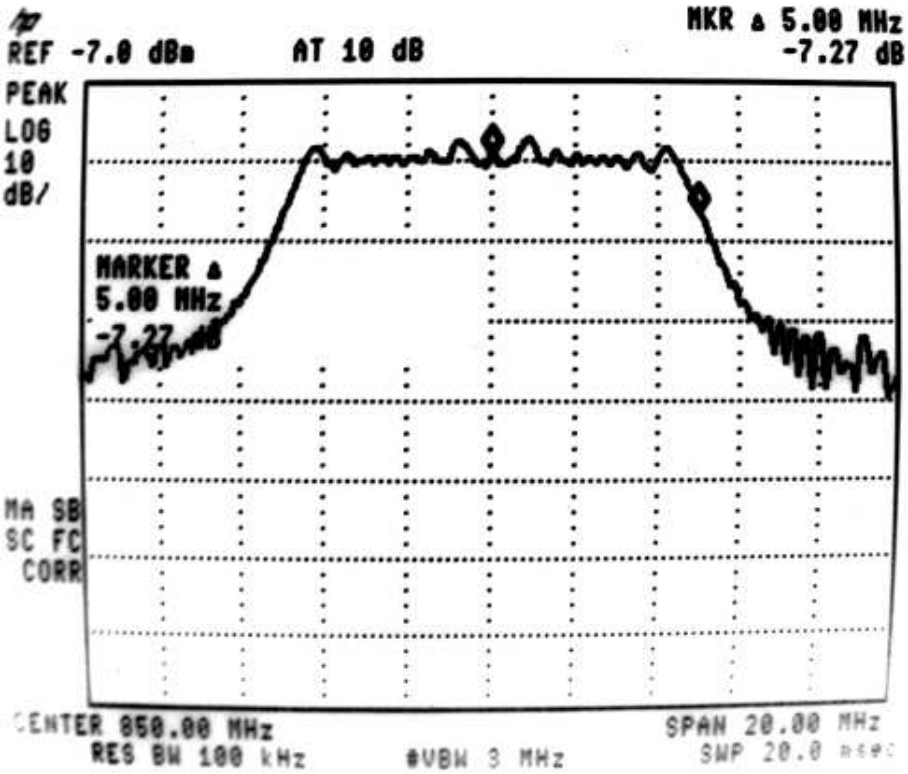

FIGURE 10.14: Measured spectrum of the quadrature branch composite complex spreading sequence in the DSSS transmitter.

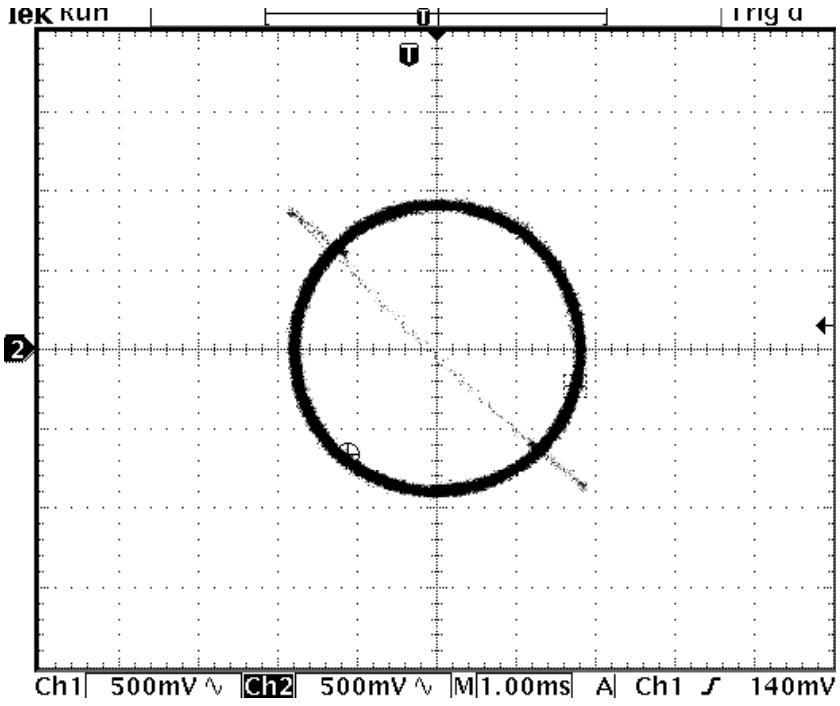

FIGURE 10.15: Measured in-phase versus quadrature branch plot at the output of the DSSS transmitter, employing CSS, to illustrate the constant envelope output.

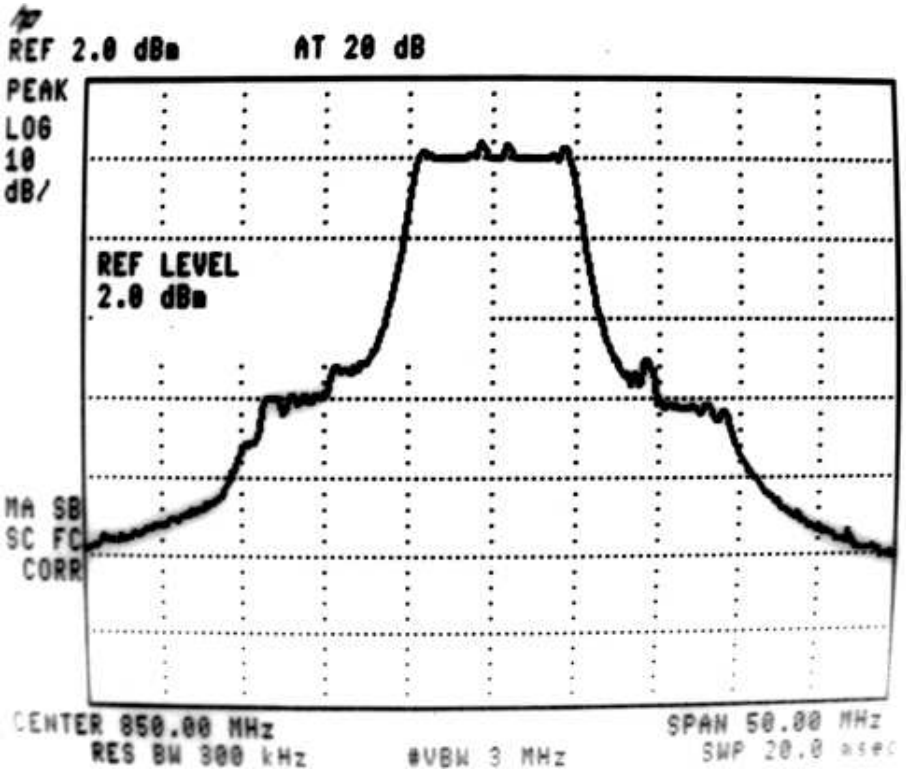

FIGURE 10.16: Final output spectrum of the DSSS transmitter employing CSS.

10.4.2 Complex DSSS Receiver (Demodulator)

The input to the receiver is down-converted to an IF of $16MHz$ before the sampling and analog-to-digital conversion process (ADC) is done. The spectrum of the signal on an IF of $16MHz$ is depicted in Figure 10.17. The composite in-phase and quadrature difference sequences used in the DD-CDLL, to determine the code error, are shown in Figure 10.18, top and bottom, respectively.

The Auto-Correlation peak, obtained from the sliding correlation process between the incoming spreading code and locally generated spreading code at the receiver, is depicted in Figure 10.19. This auto-correlation peak is produced from the sample-and-hold output after the integrate-and-dump operation in the sliding correlation despreading process. The integrate-and-dumped output is also shown in the bottom part of Figure 10.19. A zoomed-in version of this auto-correlation peak, as well as the integrate-and-dumped output, are illustrated in Figure 10.20

Another factor that influence the performance of the auto-correlation process, except for the time shift between the received and locally generated spreading sequence, is the phase error between the received and recovered carrier. The DD-CCRL is responsible for tracking the phase of the incoming carrier. Figure 10.21 shows the auto-correlation output (top) with the corresponding carrier phase error (DD-CCRL open-loop error) (bottom). A zoomed-in version of this hardware result is shown in Figure 10.22.

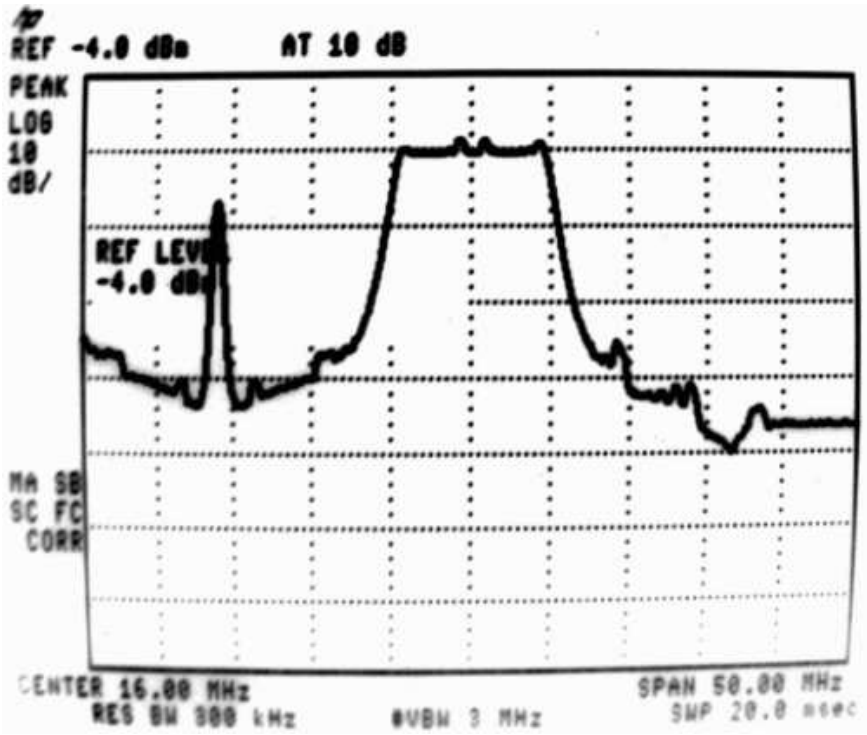

FIGURE 10.17: Spectrum of the incoming signal at the receiver on an IF of 16 MHz, as input to the ADC.

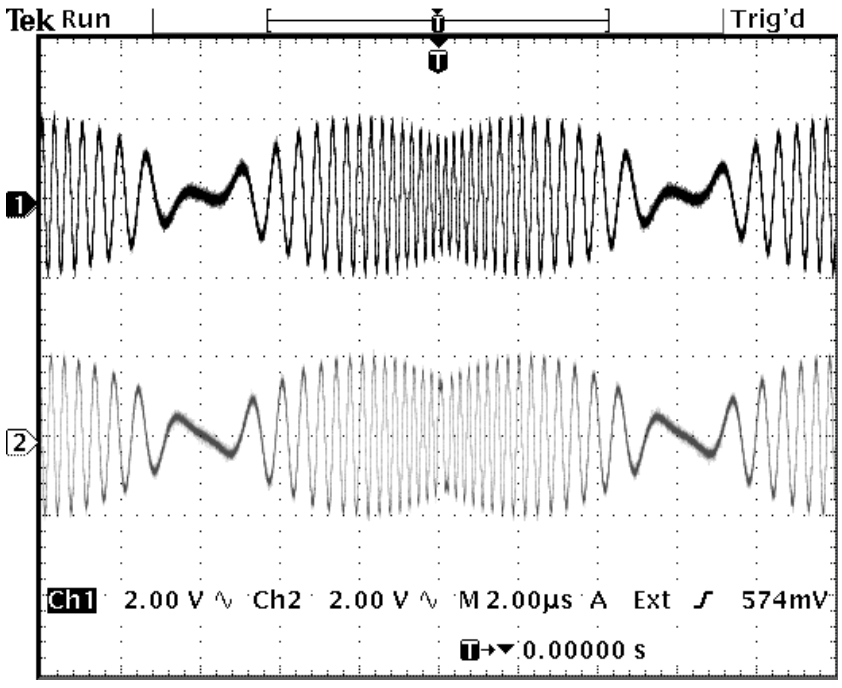

FIGURE 10.18: Composite in-phase (top) and quadrature (bottom) difference sequences used in the CDLL to determine the code error.

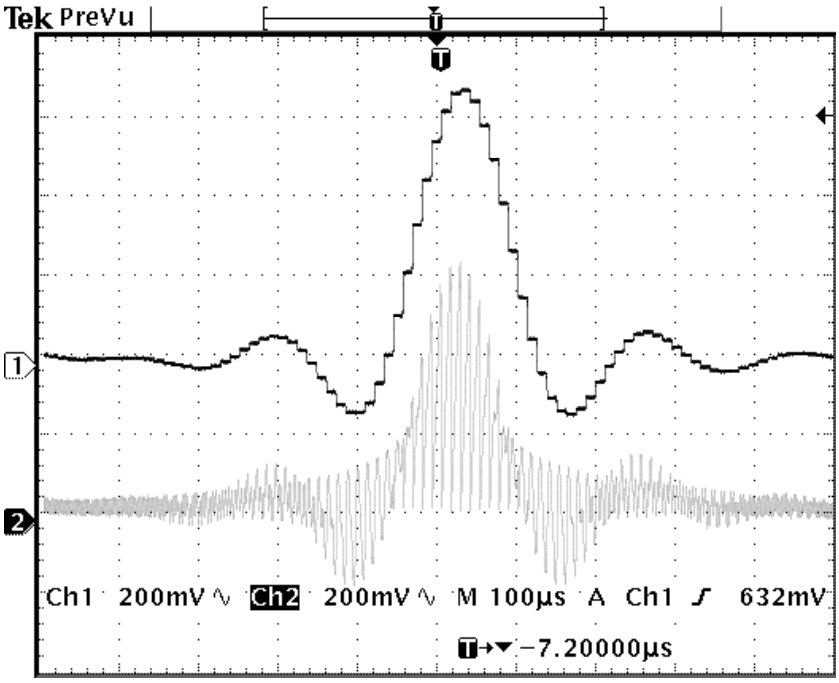

FIGURE 10.19: Auto-Correlation peak obtained (top graph) as output of sliding correlation performed between incoming spreading code and locally generated spreading code at the receiver. Integrate-and-dump output of the sliding correlation output before sample-and-hold (bottom).

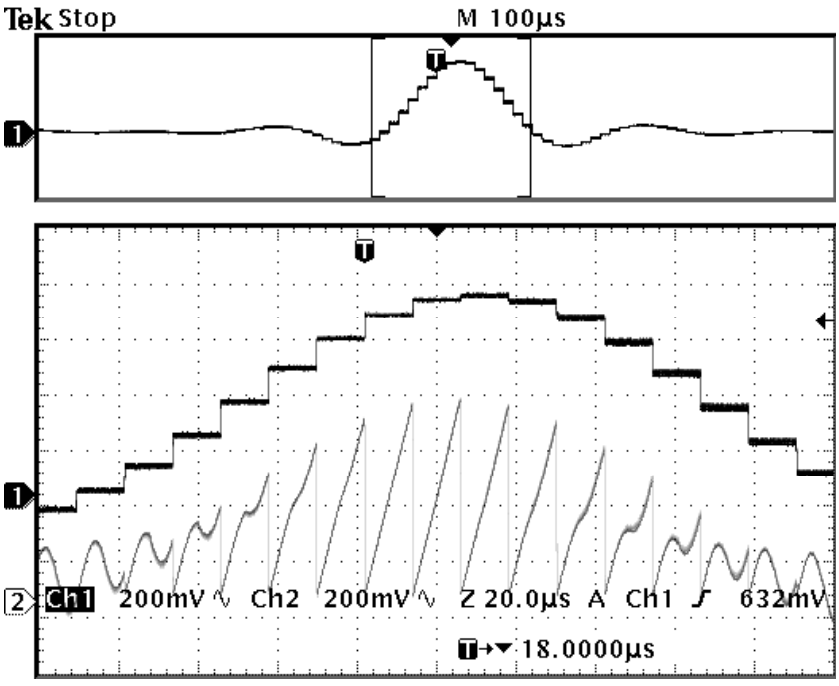

FIGURE 10.20: Auto-Correlation peak obtained (trace 1) as output of sliding correlation performed between incoming spreading code and locally generated spreading code at the receiver. Integrate-and-dump output of the sliding correlation output before sample-and-hold (trace 2).

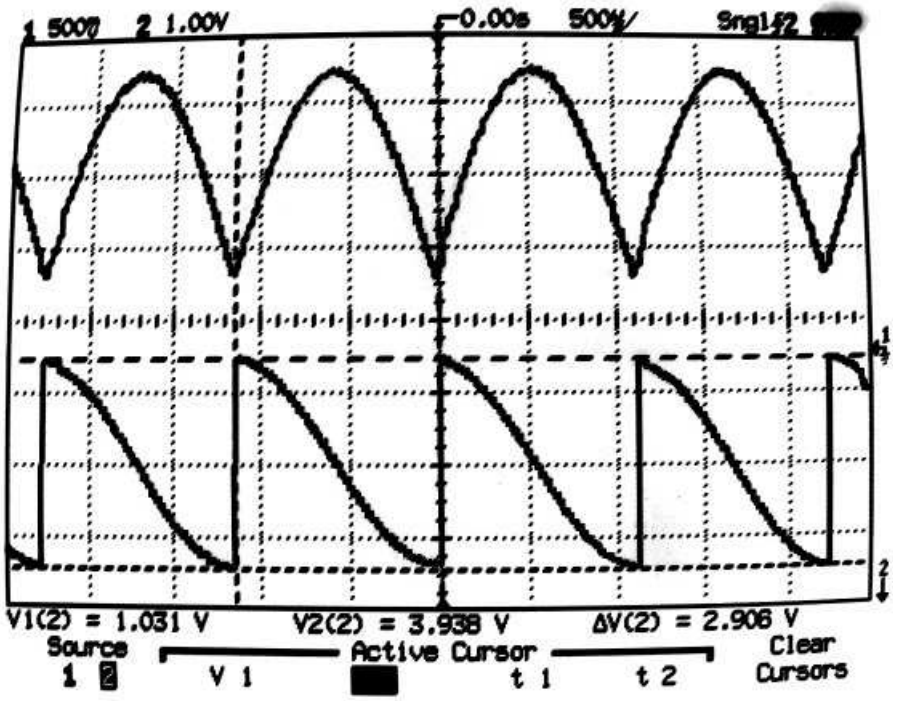

FIGURE 10.21: Auto-correlation output (top) after code acquisition has been acquired with the corresponding DD-Costas carrier recovery loop error (bottom) before carrier lock.

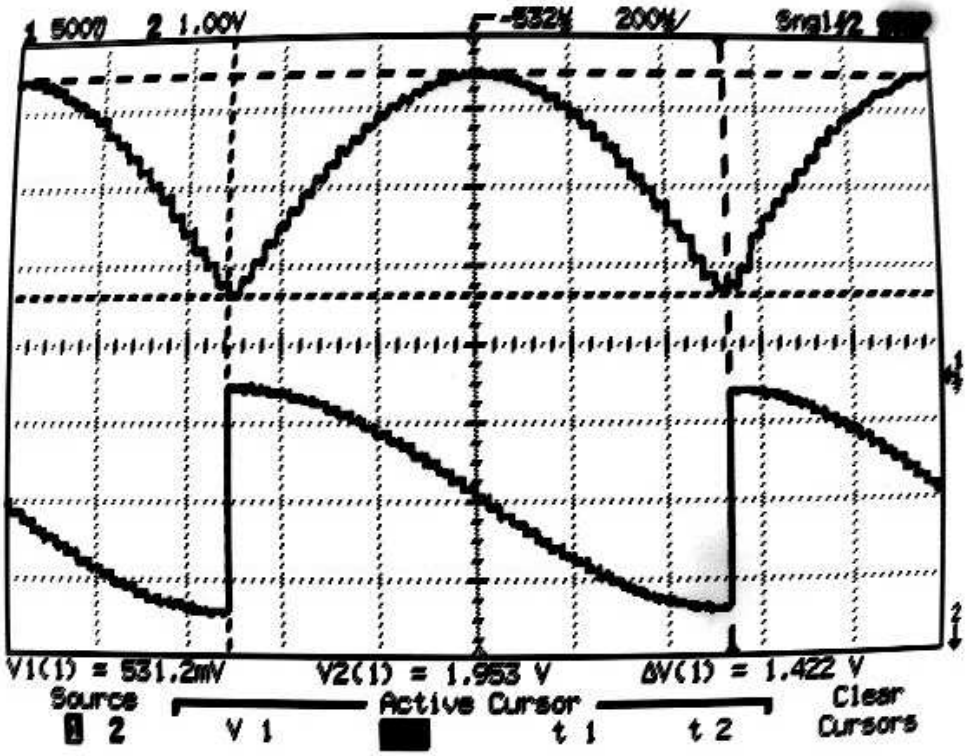

FIGURE 10.22: Zoomed in auto-correlation output (top) after code acquisition has been acquired with the corresponding DD-Costas carrier recovery loop error (bottom) before carrier lock.

PART V

SYSTEM PERFORMANCE EVALUATION AND CONCLUSIONS

CHAPTER ELEVEN

SYSTEM VERIFICATION AND PERFORMANCE EVALUATION

11.1 INTRODUCTION

This chapter compares the system performances of the balanced and dual channel DSSS QPSK modulation configurations, employing a class of constant-envelope root-of-unity (CE-RU) filtered complex spreading sequences, with conventional Nyquist filtered QPSK modulated CDMA systems employing binary spreading sequences. A verification and performance evaluation of the balanced and dual channel DSSS QPSK system employing CSS are presented in terms of bit error rate performance, spectral and power efficiency, transmitter output peak-to-average power ratio (PAPR), etc.

The comparison is also done in non-linear power amplification and is based on Complementary Cumulative Probability Density Function Peak-to-Average Power Ratio (CCDF-PAPR) measurements, as well as the amount of spectral regrowth experienced when the power amplifier is driven close to the so-called $1dB$ saturation point. Simulation as well as hardware results are presented to illustrate the superiority of the new complex-spreaded WCDMA modulation schemes over conventional methods in terms of spectral and power efficiency in the presence of non-linear power amplification.

The importance of nonlinear amplifier effects in communication systems design is supported by a number of research studies that have been conducted on this topic. Liang *et al* [47] investigates the tradeoffs between amplifiers and modulation waveforms in complex digital communication systems and introduces a figure-of-merit whereby a better understanding of the relations between amplifier efficiency, amplifier distortion, signal to in-band and adjacent channel interference, and power consumption may be obtained.

The effect of different input drive levels of the amplifier on the in-band distortion, as well as adjacent channel interference (ACI) due to spectral regrowth are quantified. In [48] analytical results are presented on spectral regrowth of modulation schemes, which are useful in finding optimal operating conditions of the power amplifier (PA) to achieve maximum efficiency without violating the out-of-band emission requirement.

11.2 BER PERFORMANCE MEASUREMENTS

11.2.1 Signal-to-Noise Ratio

As stated in [49], when there is only one transmitter in operation, the receiver performance can only be limited by noise. If it is assumed that the externally caused interference (ECI) is negligible, the total noise power P_N in the receiver bandwidth is

$$P_N = k \cdot T \cdot B_N \cdot NF \tag{11.1}$$

where

k = Boltzman's constant ($-228.6 dBW sec/^oK$ or 1.380 x $10^{-23} J/^oK$)

T = Absolute temperature in degrees Kelvin

B_N = Double-sideband noise bandwidth of the receiver

NF = Noise figure of the receiver

At a room temperature of 17^oC (290^oK), the parameter $kT = -174 dBm/Hz$.

The bit energy-to-noise density, E_b/N_o, ratio is an important parameter for the performance evaluation and comparisons between different systems. In practical systems it is more convenient to measure the average received signal-to-average noise power ratio, (P_S/P_N). The following relations for converting from E_b/N_o to P_S/P_N, as given in [49], are

$$E_b = P_S \cdot T_b = P_S \left(\frac{1}{f_b} \right) \tag{11.2}$$

$$N_o = \frac{P_N}{B_N} \tag{11.3}$$

$$\frac{E_b}{N_o} = \frac{P_S \cdot T_b}{P_N / B_N} = \frac{P_S / f_b}{P_N / B_N} = \frac{P_S \cdot B_N}{P_N \cdot f_b} \tag{11.4}$$

$$\frac{E_b}{N_o} = \frac{P_S}{P_N} \cdot \frac{B_N}{f_b} \tag{11.5}$$

Thus, the ratio E_b/N_o is the product of the P_S/P_N ratio and the receiver noise bandwidth-to-bit rate ratio (B_N/f_b).

In the case of a DSSS communication system the receiver noise bandwidth, B_N, can be expressed in terms of the chip rate, f_{chip}, as

$$B_N = x \cdot f_{chip} \tag{11.6}$$

where normally $x < 1$. Equation 11.5 can therefor be rewritten as

$$\frac{E_b}{N_o} = \frac{P_S}{P_N} \cdot x \cdot \frac{f_{chip}}{f_b} \tag{11.7}$$

Given that the processing gain (PG) of the DSSS system is defined by

$$PG = \frac{f_{chip}}{f_b} \tag{11.8}$$

Equation 11.7 becomes

$$\frac{E_b}{N_o} = \frac{P_S}{P_N} \cdot x \cdot PG \tag{11.9}$$

The E_b/N_o ratio in Equation 11.9 can be presented in terms of decibels (dB) as

$$\frac{E_b}{N_o}[dB] = \frac{P_S}{P_N}[dB] + 10\log x + 10\log PG \tag{11.10}$$

The first step in evaluating the DSSS communication system, employing CSS, was to perform bit error rate (BER) tests. The output of the DSSS transmitter, modulated onto an $850\ MHz$ IF frequency, is attenuated to the appropriate power levels for the tests by means of a variable attenuater. The attenuated output is then produced as input to an Hewlett Packard (HP) noise test set, which adds AWGN to the signal for a given $\frac{E_b}{N_o}$ value. The signal plus AWGN forms the input to the DSSS receiver, which demodulates, despreads and differential decode the signal to recover the original transmitted data. A BER analyser is used to perform the bit error probability test, comparing the transmitted data stream with the recovered data stream at the receiver.

Figure 11.1 depicts the BER of the hardware implemented differential encoded balanced/dual DSSS QPSK system employing CSS compared to the BER of theoretical QPSK and differential encoded QPSK. The hardware implementation loss of the DSSS system is in the order of $1.5\ dB$, compared to that of theoretical differential encoded QPSK.

The complete DSSS system was simulated and BER results were obtained. The simulated BER result, in the presence of AWGN, is shown in Figure 11.2.

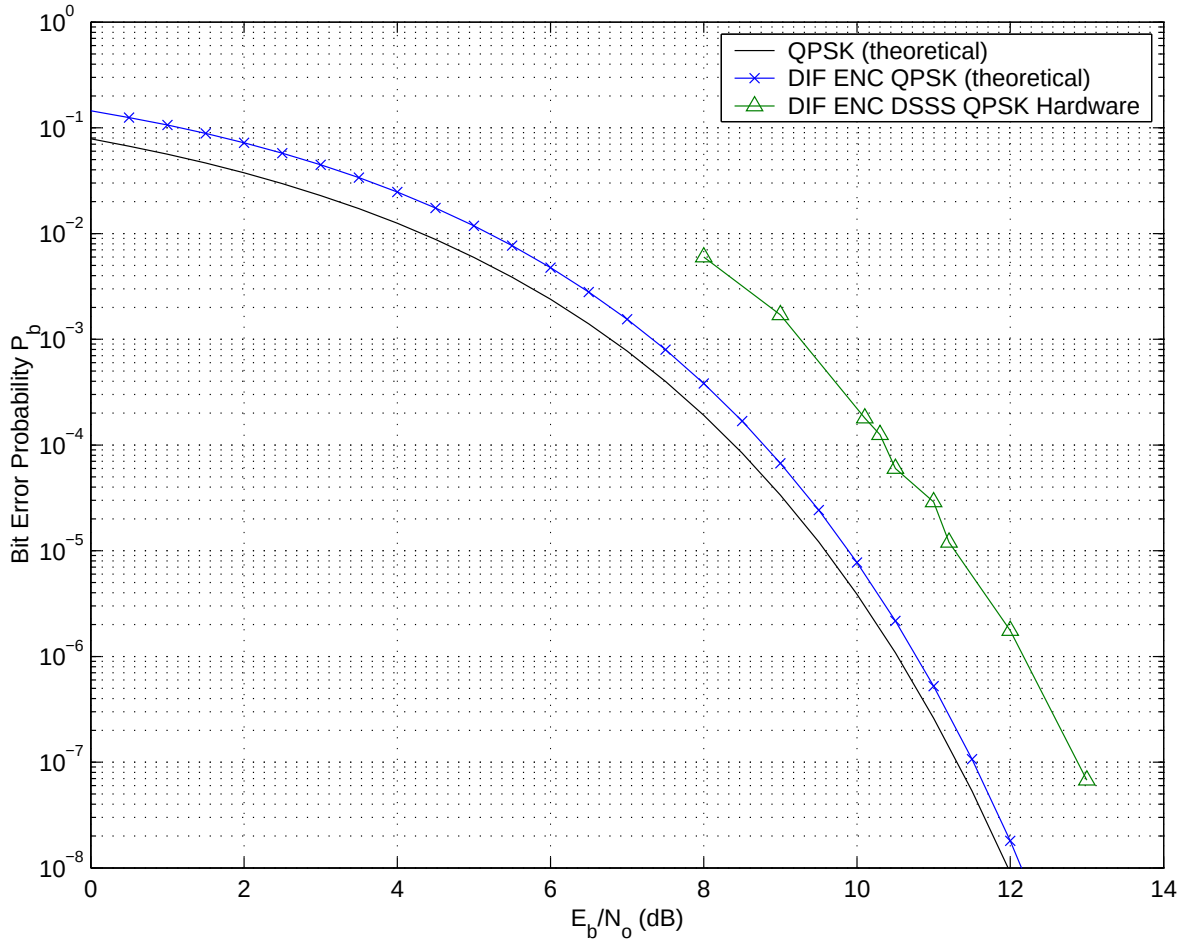

FIGURE 11.1: Bit error probability of the hardware implemented differential encoded balanced/dual DSSS QPSK system employing CSS compared to BER of theoretical QPSK and DE theoretical QPSK

The system was also simulated to investigate the effect of different phase errors on the BER performance of the DSSS system. Figure 11.4 shows the BER of the dual channel DSSS QPSK system with different phase errors between transmit and receive quadrature carriers. This result can be compared to the BER performance of a theoretical QPSK communication system also with different phase errors between transmit and receive carriers as shown in Figure 11.3. The simulated BER results corresponds with the theoretical BER results for specific phase errors.

A Motorola channel simulator, written in C++ language, was used to do system simulations in a Raleigh-faded and AWGN channel. The simulated BER result obtained is compared with the corresponding BER result of a theoretical QPSK system in an AWGN and Raleigh-faded channel, as depicted in Figure 11.5.

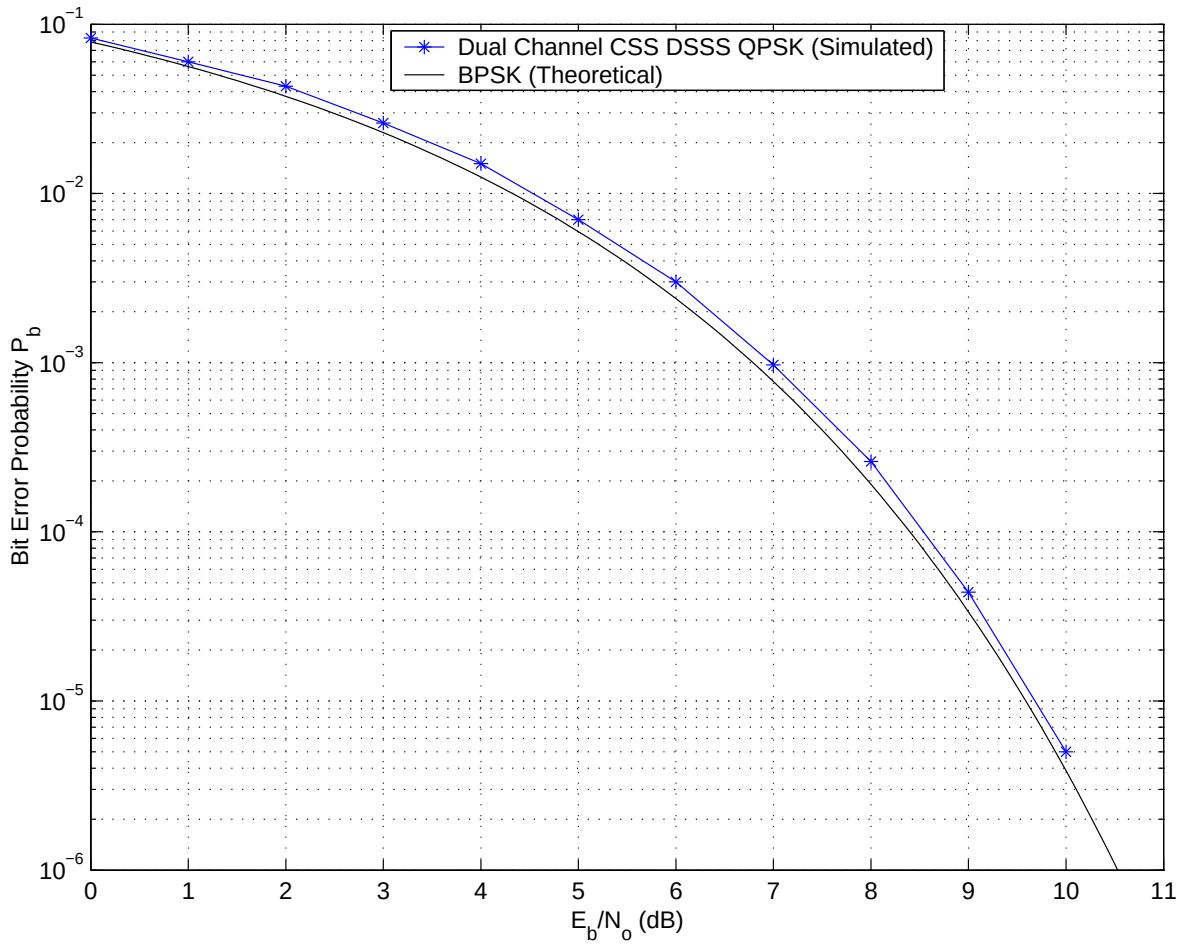

FIGURE 11.2: Bit error probability of the simulated balanced/dual DSSS QPSK system employing CSS compared to BER of theoretical QPSK

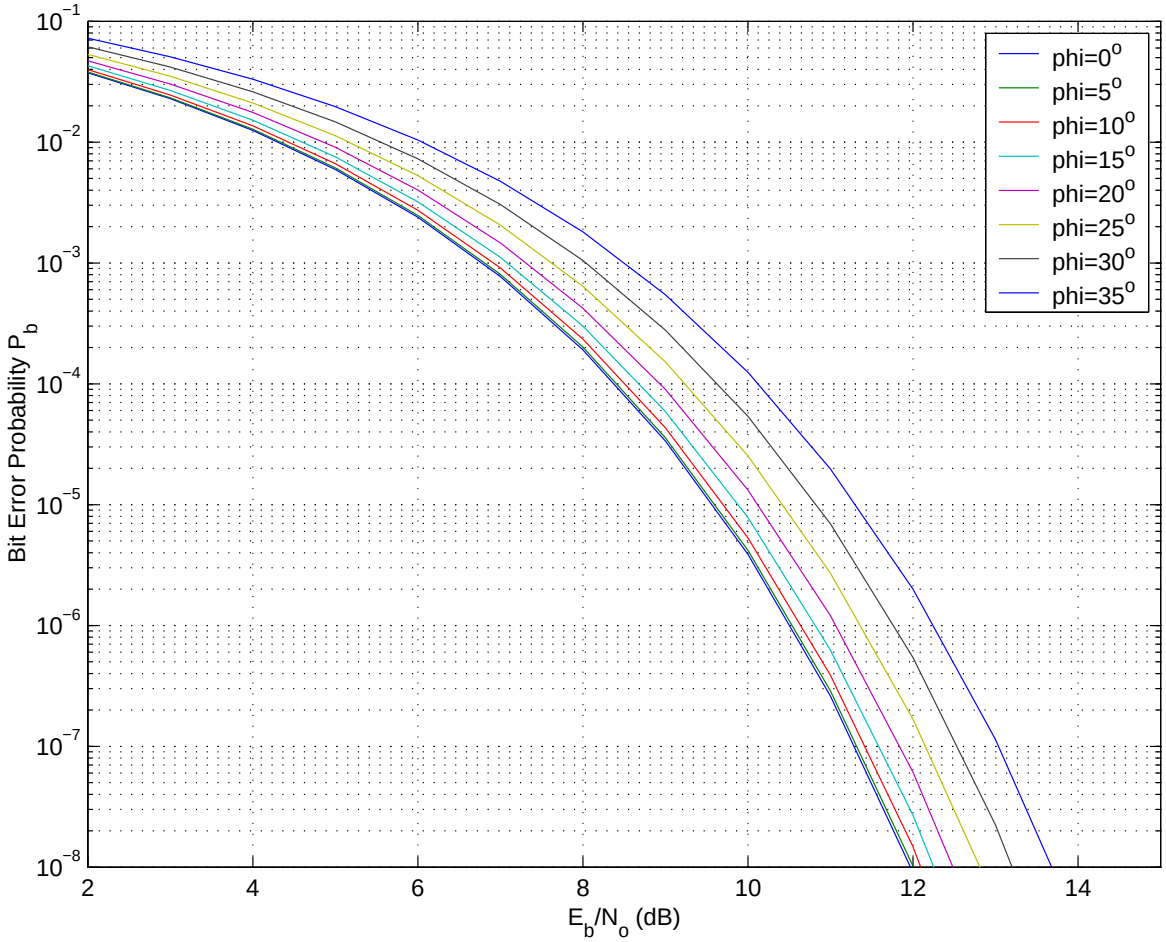

FIGURE 11.3: Bit error probability of a theoretical QPSK communication system with different phase errors between transmit and receive quadrature carriers

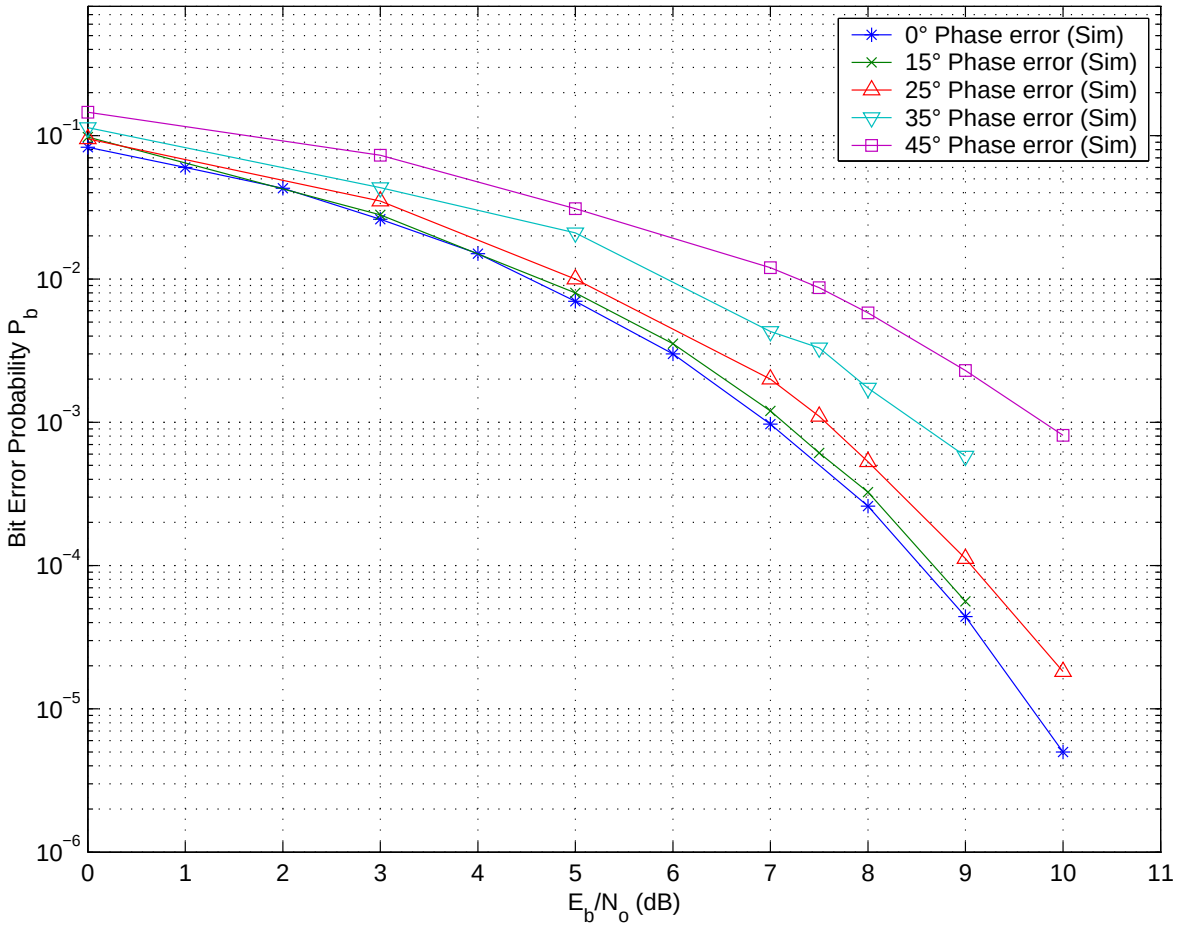

FIGURE 11.4: Bit error probability of the dual channel DSSS QPSK system employing CSS with different phase errors between transmit and receive quadrature carriers

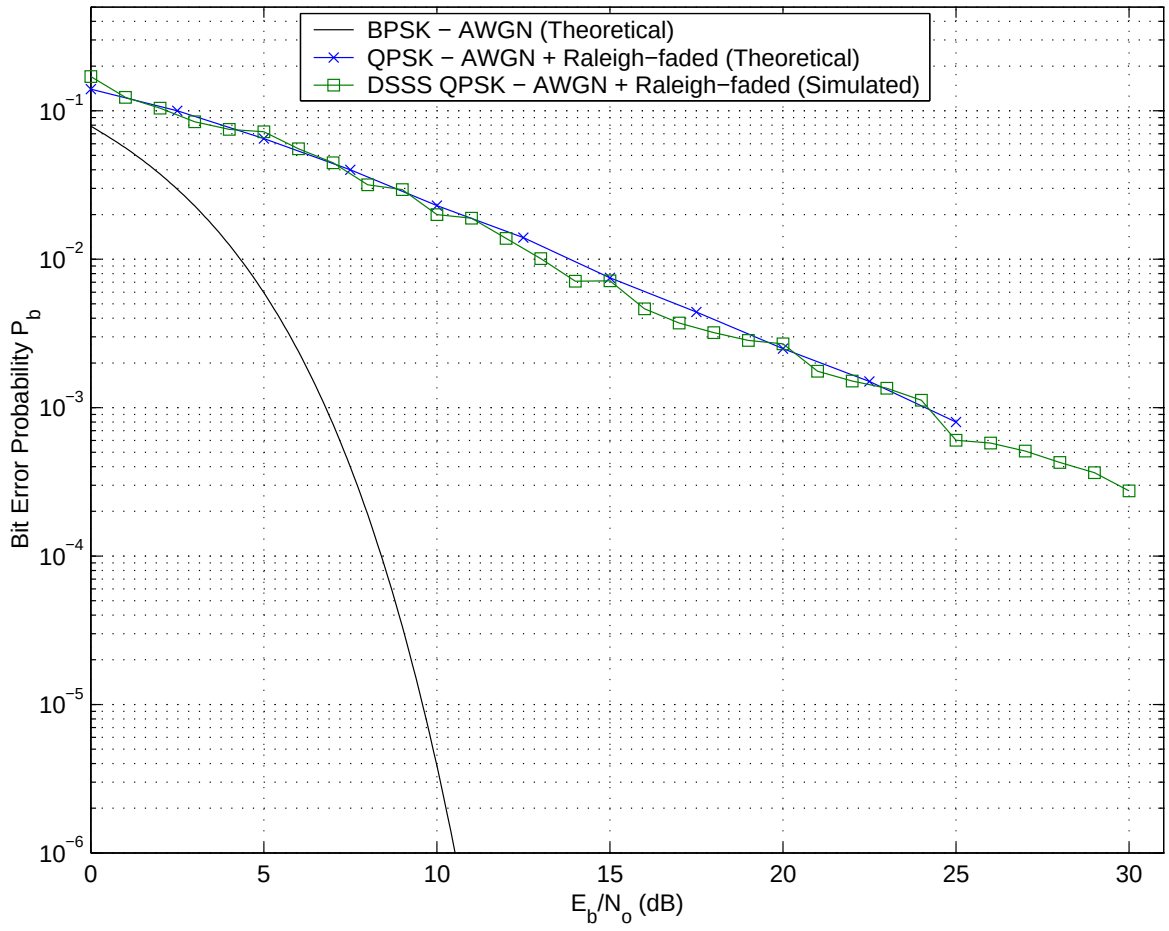

FIGURE 11.5: Bit error probability of the simulated balanced/dual DSSS QPSK system employing CSS in an AWGN and Raleigh-faded channel compared to BER of theoretical QPSK in an AWGN and Raleigh-faded channel.

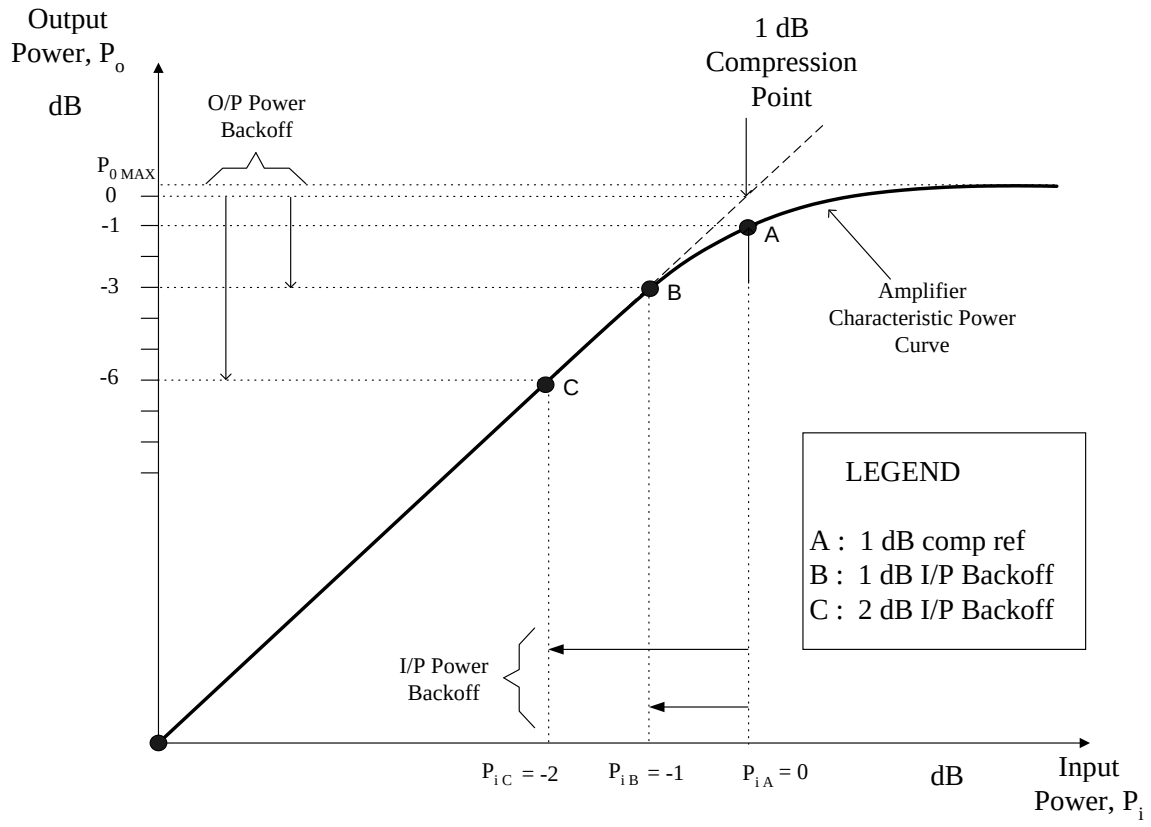

FIGURE 11.6: Typical theoretical High Power Amplifier (HPA) input/output power saturation characteristic curve

11.3 POWER SATURATION PERFORMANCE

Power amplification constitutes one of the most important processes in modern cellular communication systems. Since the power amplifier provides the transmit signal levels needed to overcome the path loss between the transmitter and receiver, and may consume a significant fraction of the power used by the system, it plays a crucial role in the definition of battery life in the design of mobile communication systems. Furthermore, apart from the power source (battery pack), it turns out to be the single most expensive component in portable telephone handsets. Since the power amplifier is an active device, it is subject to non-linear effects that can add noise and cause signal distortion. The amplifier efficiency increases with increasing input power, thus, a system-level tradeoff exists between power efficiency or battery life and the resulting distortion introduced when power amplifiers are driven close to their so-called *1dB saturation* or *1dB compression point* (see Figure 11.6).

To keep costs down without sacrificing system performance, power amplifiers have to be designed for optimum power amplification efficiency. Several system parameters dictate the choice of a specific amplifier configuration, which may be class A, A-B, B or C. Firstly, it is

well known that the power efficiency of class B amplifiers are in the order of 70%, whereas the power efficiency of class A amplifiers are considerably $(\pm 40\%)$ lower and in the order of 30%. Significant power savings are therefore incurred if linear amplifiers can be replaced by non-linear devices. Secondly, the degree of amplifier linearity required for a particular application is primarily dictated by the modulation scheme employed. Class A amplifiers are mostly chosen in cases where a high degree of linearity is required, whereas the operation of class B and C amplifiers are known to be non-linear. As a rule linear amplification methods are preferred when modulation schemes with large amplitude variations are employed, while non-linear amplification methods such as class B or C configurations may suffice in the case of so-called constant-envelope modulation schemes. An example of the latter is Minimum Shift Keying (MSK), which is the chosen modulation scheme in the Global System for Mobile (GSM) Communication cellular modulation standard.

The power efficiency of modulation schemes are usually measured in terms of the peak-to-average power ratio (PAPR) characteristics exhibited by the modulator output signal. This parameter defines the headroom required in linear amplifiers to prevent clipping or compression of the modulated carrier. When this quantity approaches one, the modulation method is relatively insensitive to power (envelope) saturation. This insensitivity is measured or sensed in terms of the degree of spectral regrowth experienced during saturation. It is well known that constant envelope modulation schemes exhibit very little, if any, spectral regrowth under non-linear amplification (saturation). Not only may non-linear amplifiers be employed in these cases, but even larger power efficiency may be achieved by allowing the power amplifier to operate closer to the amplifier 1dB saturation point, without causing excessive spectral regrowth. This chapter investigates the tradeoffs between modulation and power amplifier nonlinearity and efficiency, the goal being to minimize the energy required to communicate WCDMA-modulated digital information in an adverse mobile communication environment.

In the system evaluation in this chapter a statistical approach to power amplifier PAPR measurements is taken. In particular, Complementary Cumulative Distribution Function (CCDF) results are presented. The CCDF expresses the probability that the power is greater than a specified power value. The CCDF of two patented near Constant Envelope (CE) WCDMA modulation configurations employing complex spreading sequences, henceforth referred to as ”1/2C” and ”1C”, respectively, is presented [50] and [51]. The results are compared to a Nyquist filtered QPSK reference system, resembling the binary pilot channel specified in the WCDMA standards [52]. QPSK has been chosen as the reference

system, firstly to facilitate direct comparison with a diverse variety of theoretical and practical modulation schemes, and secondly by virtue of its universal application in a host of applications, including the UMTS [53] and 3GPP WCDMA standards.

11.3.1 Peak-to-Average Power Ratio (PAPR) Complementary Cumulative Distribution Function

In a non-statistical peak power measurement the peak-to-average power ratio (PAPR) is easy to visualise in the case of simple modulation schemes in which there are close correspondence between the modulating waveform and the carrier envelope. In the absence of this correspondence, the PAPR alone does not provide adequate information. This is particularly true with digital modulation methods in which amplitude and phase modulation are combined in a multi-level arrangement, resulting in signal envelopes which are a complex function of the data stream content, rather than the amplitude of the modulating signal. In these cases the resulting signal envelope cannot be directly related to modulation parameters such as modulation depth and modulation index.

The resulting noise-like character of these signals suggests a statistical approach to peak and average power analysis.

Let Y be a discrete random variable (rv) with a range equal to all possible sampled values of peak-to-average carrier power. Then y denotes a specific power value contained in Y. Let PDF denote the probability distribution function of Y. Then PDF is the percentage of time that the PAPR is equal to or smaller than a specific value, y. PDF expressed as a percentage is

$$\text{PDF} = P(y) = 100 \times P(Y = y) \tag{11.11}$$

where y ranges over all values in Y, $0 \leq P(y) \leq 100\%$. The PDF, and specifically the envelope PDF, is useful for analysing the nature of modulating signals. Sustained power levels such as the flat tops of pulses or steps will show up as spectral peaks or lines. Random noise will produce a smooth Gaussian shaped curve.

Let CDF denote the cumulative distribution function of Y. The CDF is the probability that the PAPR is less than or equal to a specific value, y. The CDF is non-decreasing in y, that is, the graph of CDF versus y cannot have negative slope. The maximum PAPR sample taken will lie at 100%. CDF expressed as a percentage is

$$\text{CDF} = Q(y) = 100 \times P[Y \leq y] \tag{11.12}$$

where y ranges over all values in Y, $0 \leq Q(y) \leq 100\%$ $Q(y_{max}) = 100\%$ and $\sum Q(y) = 100\%$

It is convenient to use the complementary CDF, or CCDF, i.e., $1 - CDF$ (sometimes called the "upper tail area") in the analysis of the envelopes of digital modulation schemes. CCDF expressed as a percentage is:

$$\text{CCDF} = 1 - Q(y) = 100 \times P[Y > y] \tag{11.13}$$

where y ranges over all values in Y. The CCDF has the following properties:

$$0 \leq 1 - Q(y) \leq 100\%;\ 1 - Q(y_{\max}) = 0\% \tag{11.14}$$

In a non-statistical peak power measurement the PAPR is the parameter which describes the headroom required in linear amplifiers to prevent clipping or compressing the modulated carrier. The meaning of this ratio is easy to visualize in the case of simple modulation in which there is close correspondence between the modulating waveform and the carrier envelope. When this correspondence is not present, the PAPR alone does not provide adequate information. It is necessary to know what fraction of time the power is above (or below) particular levels. For example, some digital modulation schemes produce narrow and relatively infrequent power peaks which can be compressed with minimal effect. The peak-to-average ratio alone would not reveal anything about the fractional time occurrence of the peaks, but the CDF or CCDF clearly show this information. The CCDF can be used to determine optimum transmitter power output and is also used to evaluate the various modulation schemes considered, to determine the demands that will be made on linear amplifiers and transmitters and the sensitivity to non-linear behaviour.

11.4 CCDF RESULTS FOR DIFFERENT WCDMA MODULATION CONFIGURATIONS

The PAPR CCDF of three WCDMA modulation techniques are presented in this section, namely the CCDF of conventional QPSK-modulated CDMA, as well as two versions of a patented WCDMA modulation technique employing constant-envelope root-of-unity filtered complex spreading sequences (CE-RU-CSS), denoted by 1/2C and 1C, respectively. The 1/2C WCDMA scheme, which features a perfectly constant signal envelope after modulation, produces a data throughput rate equal to that of conventional QPSK-modulated WCDMA. 1C denotes a more spectrally efficient four-dimensional extension of 1/2C, employing only one CSS for every four dimensions.

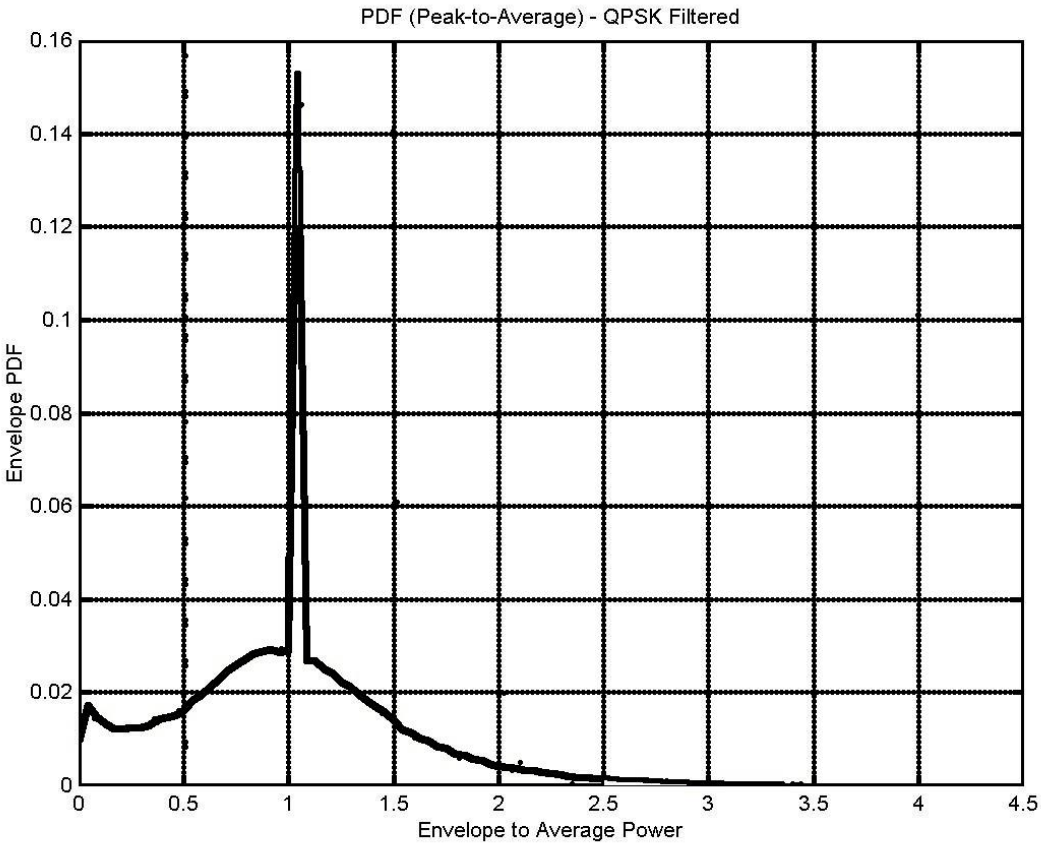

FIGURE 11.7: PDF of peak to average power ratio (PAPR) for QPSK

11.4.1 PAPR-CCDF of Conventional Nyquist-filtered Non Constant Envelope QPSK

The PAPR PDF of conventional Nyquist-filtered QPSK is shown in Figure 11.7, and the corresponding CCDF in Figure 11.8.

On the abscissa of Figure 11.7, 1 dB represents the average of the peak-to-average power. This reference value is normalized to 0 dB in Figure 11.8. The PAPR is plotted in terms of decibels and only for values equal to or exceeding 0dB, since this is the range of power ratios that directly determines the required transmitter power amplifier power back-off. According to the graph peak-to-average power values of greater or equal to 4.1 dB occur less than 1% of the time.

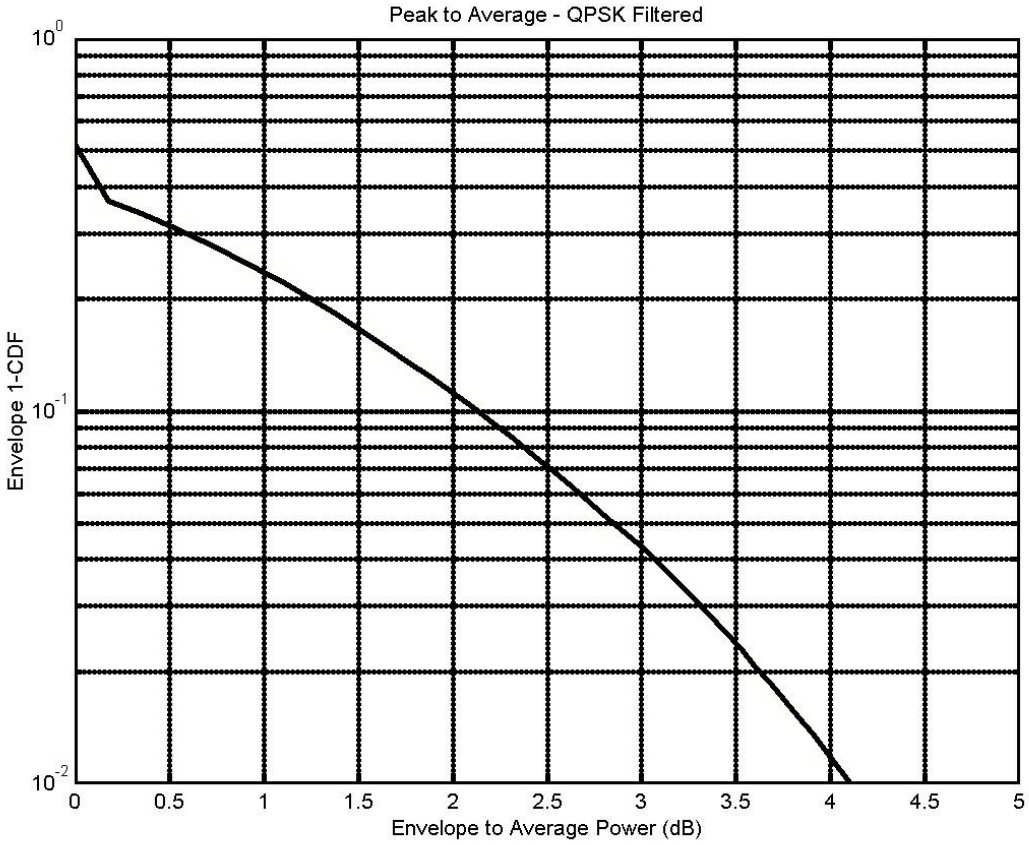

FIGURE 11.8: CCDF of peak to average power ratio (PAPR) for QPSK

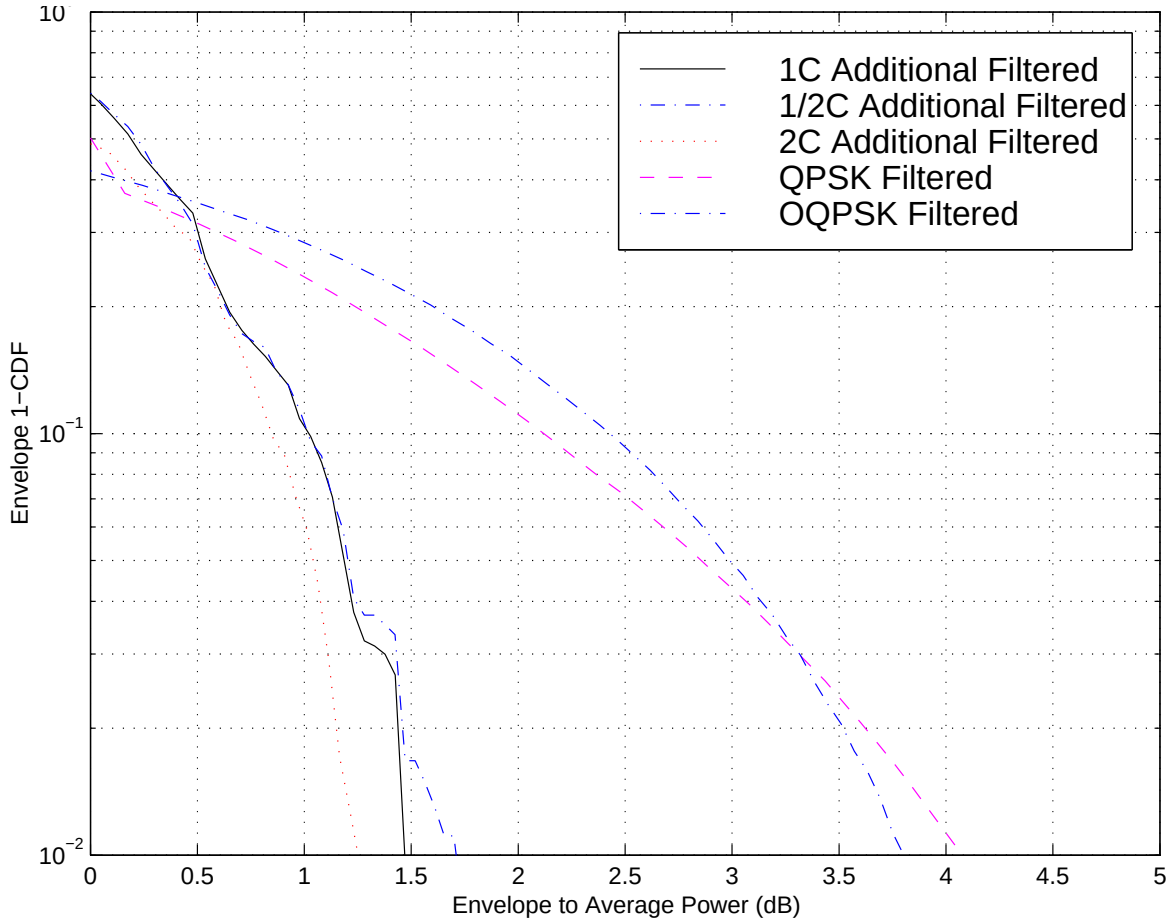

FIGURE 11.9: Peak-to-Average Power Ratio Complementary Cumulative Probability Distribution Function (PAPR-CCDF) measurements for CE-RU-filtered 1/2C and 1C modulated WCDMA, compared to conventional Nyquist-filtered QPSK-modulated WCDMA

11.4.2 PAPR-CCDF of Constant-Envelope 1/2C and 1C WCDMA modulation schemes

Figure 11.9 compares the PAPR-CCDF measurements of CE-RU-filtered 1/2C and 1C WCDMA modulation configurations, with a Nyquist filtered QPSK reference system.

In the case of the 1/2C modulation scheme it is clear that most of the power is contained in the peak-to-average power range of 1 to 1.2 dB. Before any additional filtering is applied, the instantaneous power envelope is totally constant and the PDF is only a single value at a peak-to-average power of 1 dB. Additional filtering is necessary to band limit the output signal to fit a specified RF spectral mask. It is the additional filtering that causes the peak-to average power variation seen in Figure 11.9. PAPR values of greater or equal to 1.7 dB nevertheless occur less than 1% of the time. It is also observed from the figure that the 1C

WCDMA modulation scheme exhibits PAPR values of greater or equal to 1.47 dB less than 1% of the time, which is only slightly worse than for 1/2C, but at twice the data throughput rate of conventional QPSK and 1/2C.

A direct comparison between the PAPR-CCDF measurements of the said modulation schemes reveals a 90-percentile peak-to-average power ratio advantage of approximately 2.15 and 2.2 dB for 1/2C and 1C, respectively, relative to QPSK under identical operating (filtering) conditions. Note the small but remarkable statistical PAPR power advantages gained by the 1C multi-dimensional CE-RU-filtered WCDMA modulation scheme relative to the perfectly constant envelope 1/2C configuration (approximately 0.25 dB), as well as the large improvement (approximately 2.5 dB) on the Nyquist filtered QPSK reference system.

11.5 POWER SATURATION PERFORMANCE OF MODULATION STANDARDS: EXPERIMENTAL TEST SETUP

Figure 11.10 gave a schematic representation of the 1 dB compression point of a power amplifier. The 1 dB Power Amplifier (PA) saturation point is defined as the point **A** where the low noise amplifier characteristic (solid graph) deviates 1 dB from the ideal linear amplifier power saturation curve (dashed graph). It serves as a reference point for both the PAPR-CCDF tests performed on the output signal of GSM and WCDMA modulation systems, as well as to different modulation schemes when subjected to non-linear power amplification and saturation.

The experimental test setup for non-linear power amplification (hard limiting) and power amplifier saturation measurements is shown in Figure 11.10. A Mini-Circuits ZFL-1000LN low noise amplifier (LNA) was used to perform the amplifier saturation tests presented.

The cdma2000 modulation schemes investigated in this report were all implemented on a generic FPGA development platform containing four Altera 600k FPGA devices. These configurations comprise a conventional Nyquist filtered QPSK CDMA reference transmitter, as well as three multi-dimensional WCDMA modem transmitter configurations (referred to as 1/2C and 1C) employing constant envelope root-of-unity filtered complex spreading sequences (CE-RU-CSS). A variable rate pseudo-noise (PN) generator, with length $N = 2^{48} - 1$, provides a serial random data input stream to each modem. The FPGA development platform produces the in-phase (I) and quadrature (Q) baseband signals of individual transmitter configurations. These digital I and Q channel outputs are then digital-to-analog converted, low-pass filtered and amplified, prior to modulation onto 250

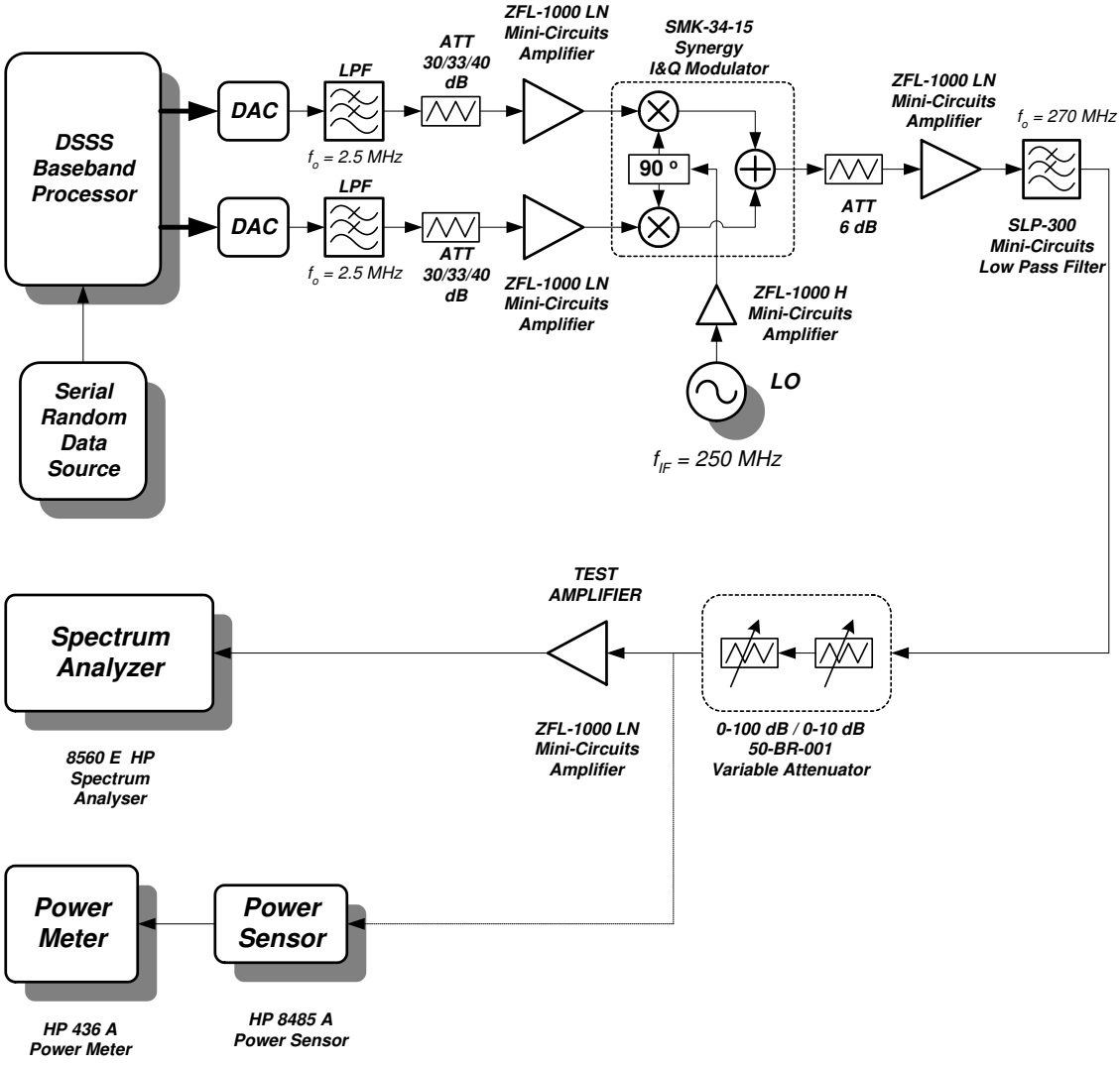

FIGURE 11.10: Block diagram of the power amplifier saturation test setup

MHz intermediate quadrature carrier frequencies.

The resultant modulated signal is then amplified and low-pass filtered to eliminate any unwanted, out-of-band harmonic components that may have been produced by the I&Q modulator. A variable attenuator is used to adjust the power level to the input of the *TEST AMPLIFIER* in 1 dB increments. Quadrature modulation and summation is done by means of an I&Q modulator and summer (Synergy, SMK-34-15). A properly calibrated HP 8485A power sensor and HP 436A power meter combination were used to perform all power measurements. Spectral measurements were done with a HP 8560E spectrum analyzer.

11.6 POWER SATURATION TEST RESULTS

The results presented below present spectral measurements under varying power saturation conditions performed on the proprietary 1/2C and 1C WCDMA modulation schemes and a standard QPSK-modulated WCDMA modulation scheme resembling the 3GPP WCDMA standard pilot channel. Both modulators comprise identical spreading (chip) rates and Nyquist baseband filtering to achieve the desired 3GPP 5 MHz RF spectral mask.

11.6.1 PSD Benchmarks

Figure 11.11 depicts the Power Spectral Density (PSD) of the Nyquist filtered QPSK modulated WCDMA reference system at a power amplifier input level of 20 dB below the 1 dB saturation point.

In contrast, Figure 11.12 depicts the PSD of the unsaturated CE-RU-filtered 1/2C WCDMA system at identical data and spreading rates, with additional filtering added to meet the specified RF spectral mask. Note that the attenuation at the ± 3 MHz (relative to the carrier) passband edges is 40.99 dB down relative to the signal level at the passband center, which is more than 10 dB better than the QPSK reference system in Figure 11.11.

Figure 11.13 shows the PSD of the Nyquist filtered QPSK modulated WCDMA reference system with the power amplifier input level at 2 dB below the 1 dB PA compression point. This result can be compared to the PSD of CE-RU-filtered 1/2C-modulated WCDMA with the power amplifier input level also set at 2 dB below the 1 dB compression point as illustrated in Figure 11.14.

The PSD of the Nyquist filtered QPSK modulated WCDMA reference system with the power amplifier input level at the 1 dB compression point and the PSD of CE-RU-filtered

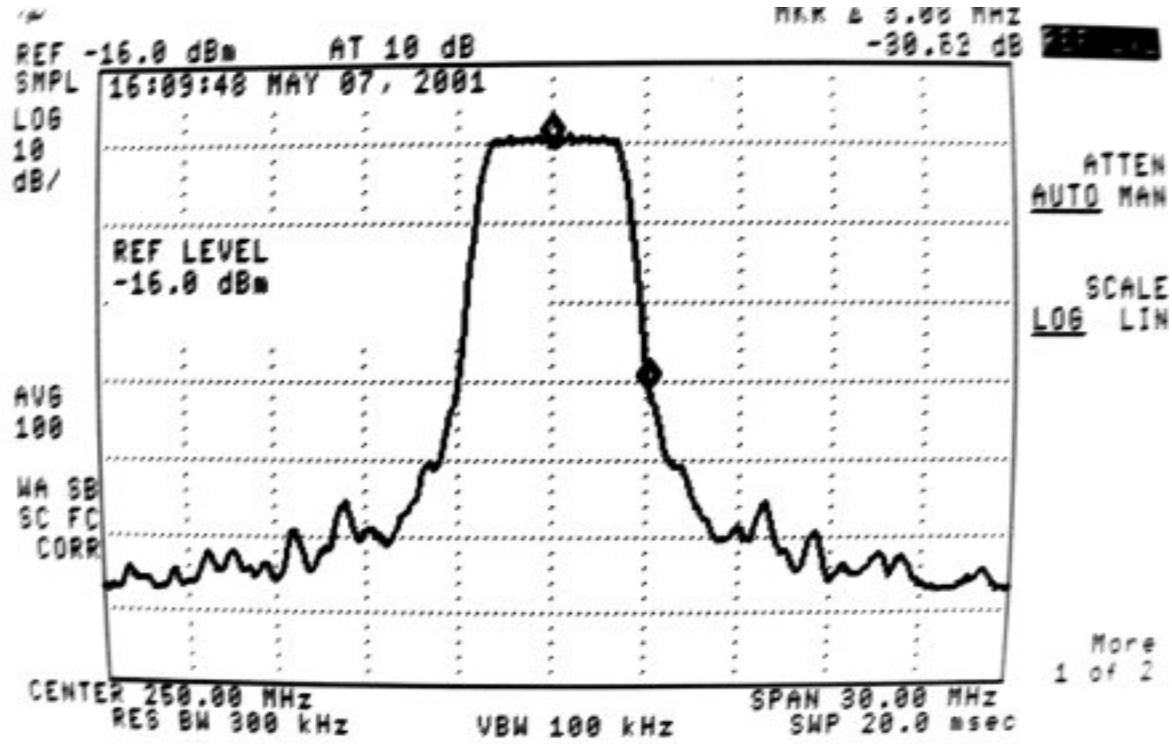

FIGURE 11.11: PSD of unsaturated Nyquist filtered QPSK modulated WCDMA reference system (power amplifier input level at 20 dB below the 1 dB PA compression point)

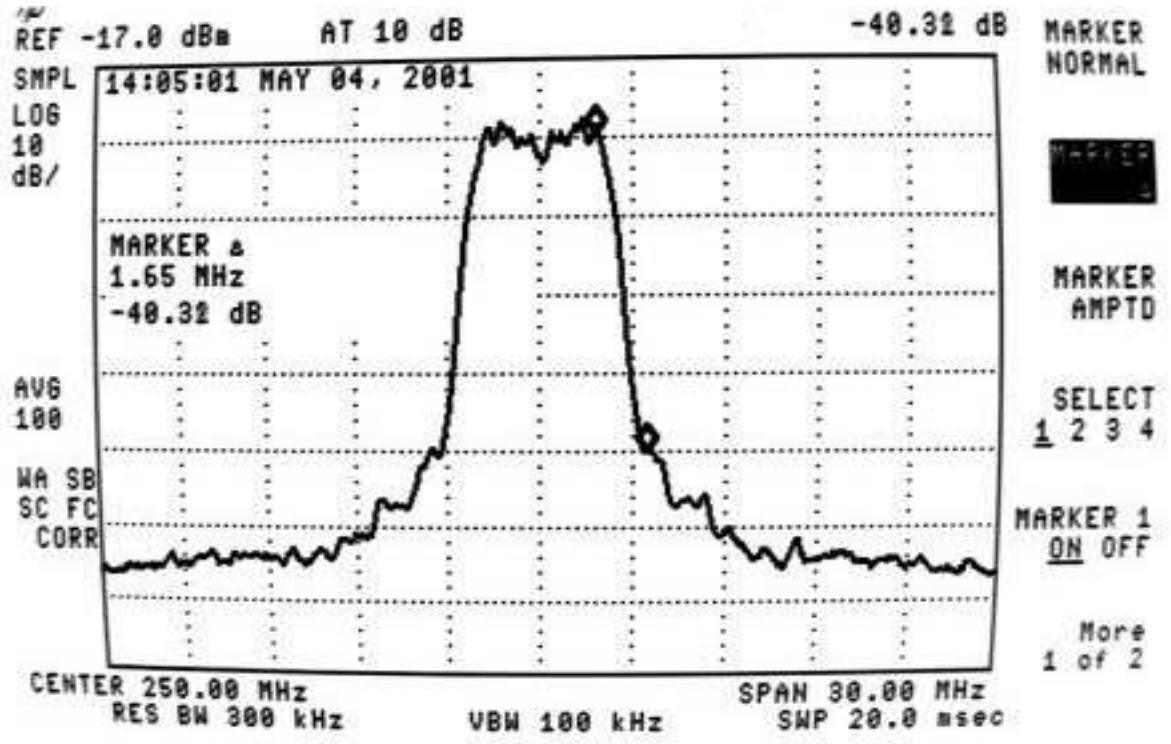

FIGURE 11.12: PSD of unsaturated CE-RU-filtered 1/2C-modulated WCDMA (power amplifier input level set at 20 dB below the 1 dB compression point).

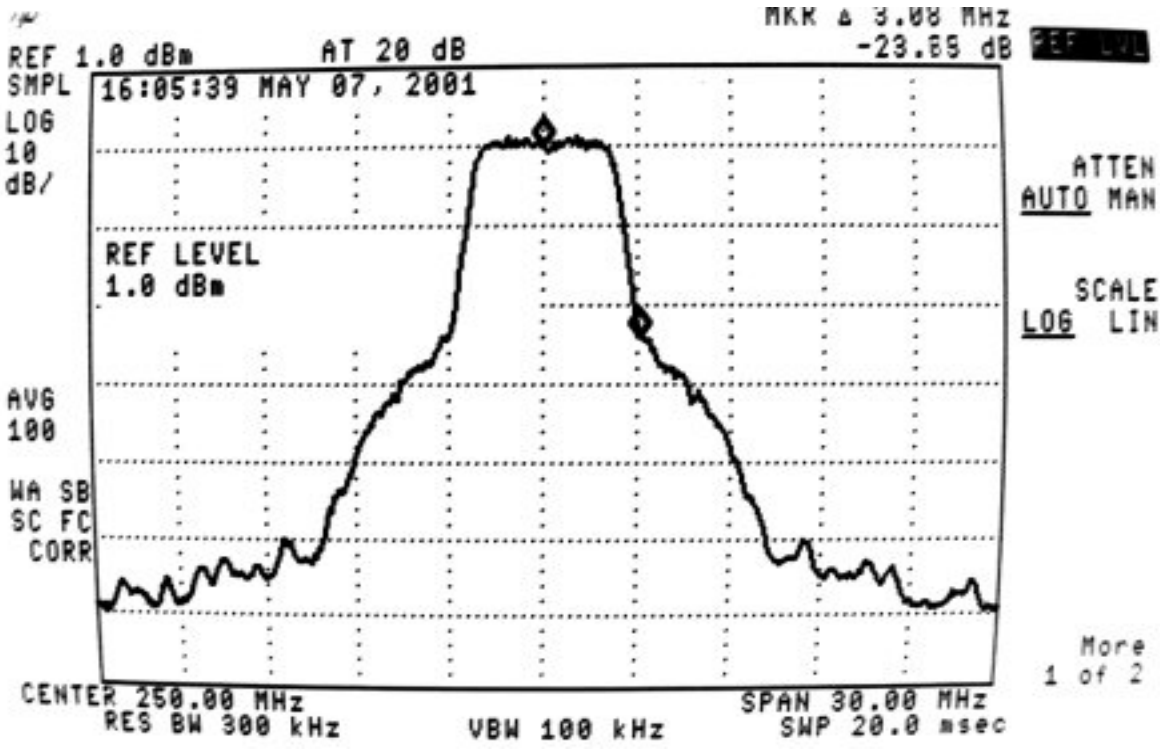

FIGURE 11.13: PSD of the Nyquist filtered QPSK modulated WCDMA reference system with the power amplifier input level at 2 dB below the 1 dB PA compression point

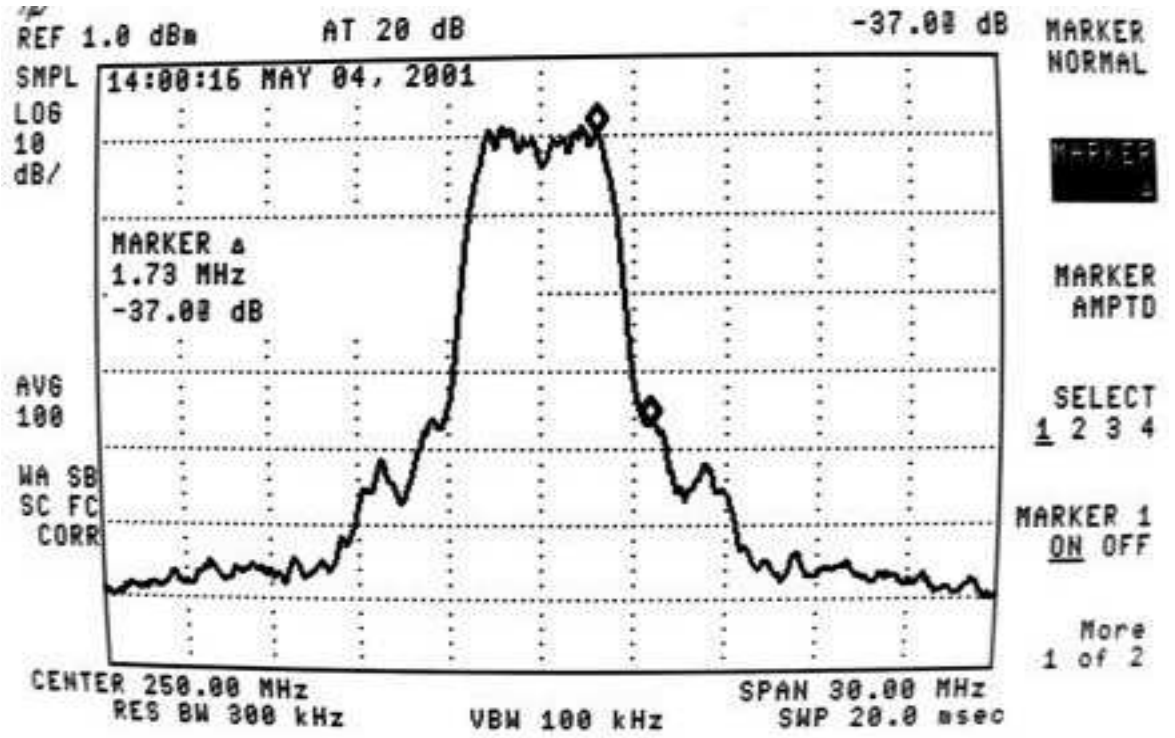

FIGURE 11.14: PSD of CE-RU-filtered 1/2C-modulated WCDMA with the power amplifier input level set at 2 dB below the 1 dB compression point

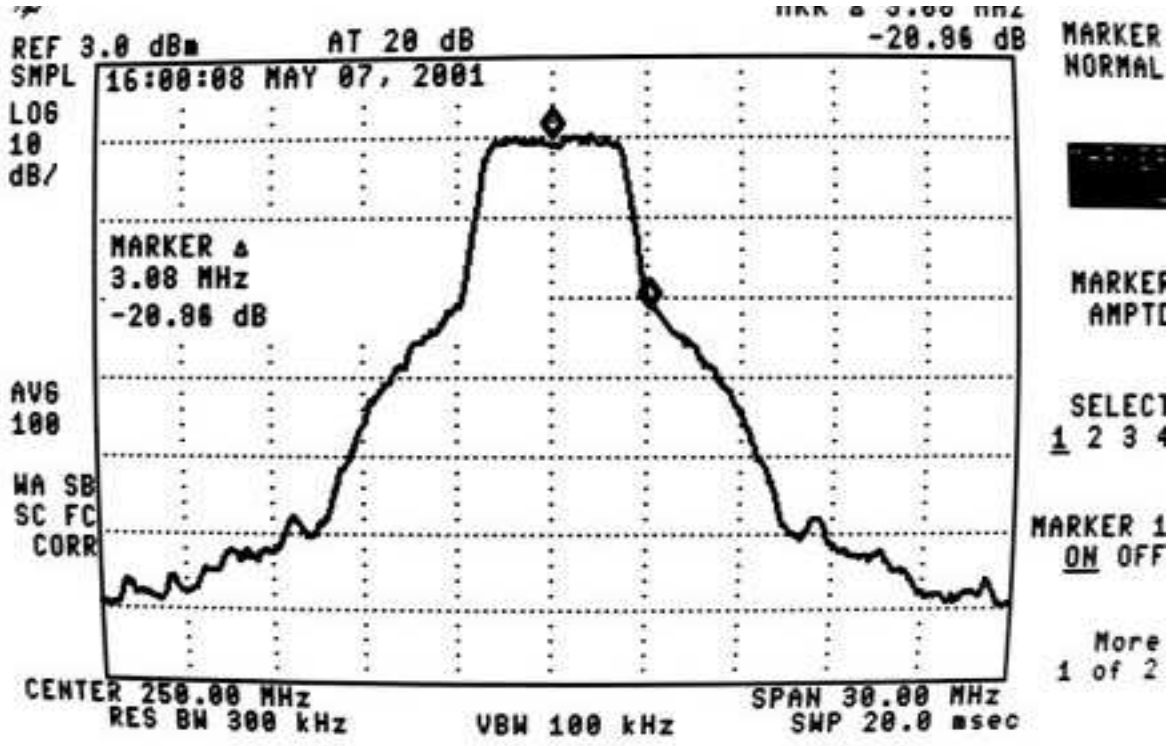

FIGURE 11.15: PSD of the Nyquist filtered QPSK modulated WCDMA reference system with the power amplifier input level at the 1 dB PA compression point

1/2C-modulated WCDMA with the power amplifier input level set at the 1 dB compression point are depicted in Figure 11.15 and Figure 11.16, respectively.

11.6.2 PSD of Modulation Schemes under Power Saturation Conditions

Spectral regrowth was investigated by comparing the power spectral densities of the various modulation schemes with a typical cdma2000 RF mask, as a function of the degree of amplifier saturation. The RF mask served as a benchmark to establish whether the spectral regrowth was within the excepted limits set by the mask. An attenuation of 30 dB relative to the nominal passband power level had to be achieved within a frequency span of 1.2 times the one-sided -3 dB transmission bandwidth $B/2$ centered on the IF carrier, where the cdma2000 bandwidth B is specified as 5 MHz for this application.

The spectral characteristics of each modulation scheme were monitored when the power amplifier was successively driven with input power levels of $-20, -10, -5, -3, -2, -1, 0, +1$ and $+5$ dB relative to the amplifier 1 dB compression point of -17 dBm. Only the -20 and -2 dB measurements are presented here.

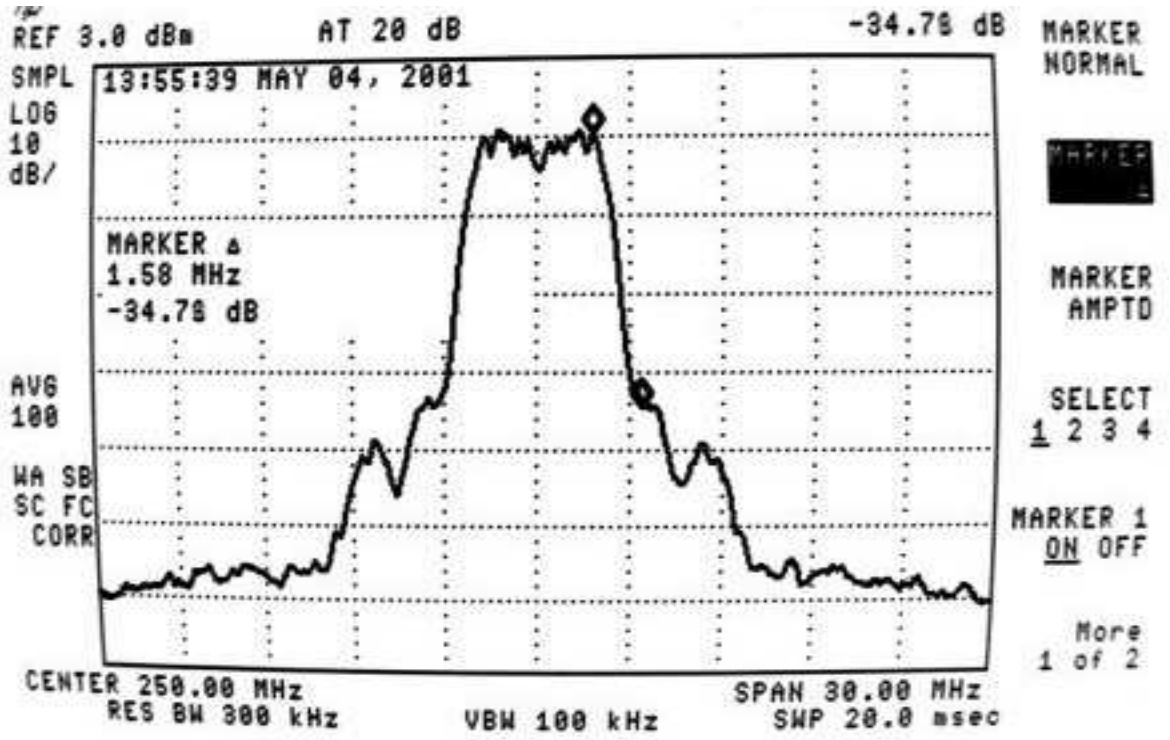

FIGURE 11.16: PSD of CE-RU-filtered 1/2C-modulated WCDMA with the power amplifier input level set at the 1 dB compression point

When the power amplifier is driven at a level of 2 dB below the 1 dB PA saturation point, the PSD of the Nyquist filtered QPSK reference system is attenuated by 23.85 dB at the ± 3 MHz passband reference frequencies, falling short of the specified required band edge attenuation of 30 dB by nearly 6 dBs. Significant spectral regrowth is thus evident in this particular case.

In the case of the constant-envelope root-of-unity (CE-RU) filtered 1/2C WCDMA modulation configuration the PSD attenuation at the 3 MHz band edges is only 38 dB when the power amplifier is driven at a level of 2 dB below the 1 dB PA saturation point. This represents an approximate 3 dB deterioration compared to the previous benchmark measurement depicted in Figure 11.12, but is more than 14 dB better than the QPSK reference system for the same PA input level. The corresponding attenuation for the 1C configuration is 32.09 dB relative to the nominal pass band power level, which easily meets the RF spectral mask requirement of 30 dB. Although this is nearly 6 dBs worse than 1/2C, it is still more than 8 dBs better than WCDMA spreaded Nyquist filtered QPSK. Note that this spectral confinement is achieved at *twice* the data throughput rate offered by both QPSK and the 1/2C WCDMA CE-RU filtered complex spreaded modulation schemes in a given spreading bandwidth.

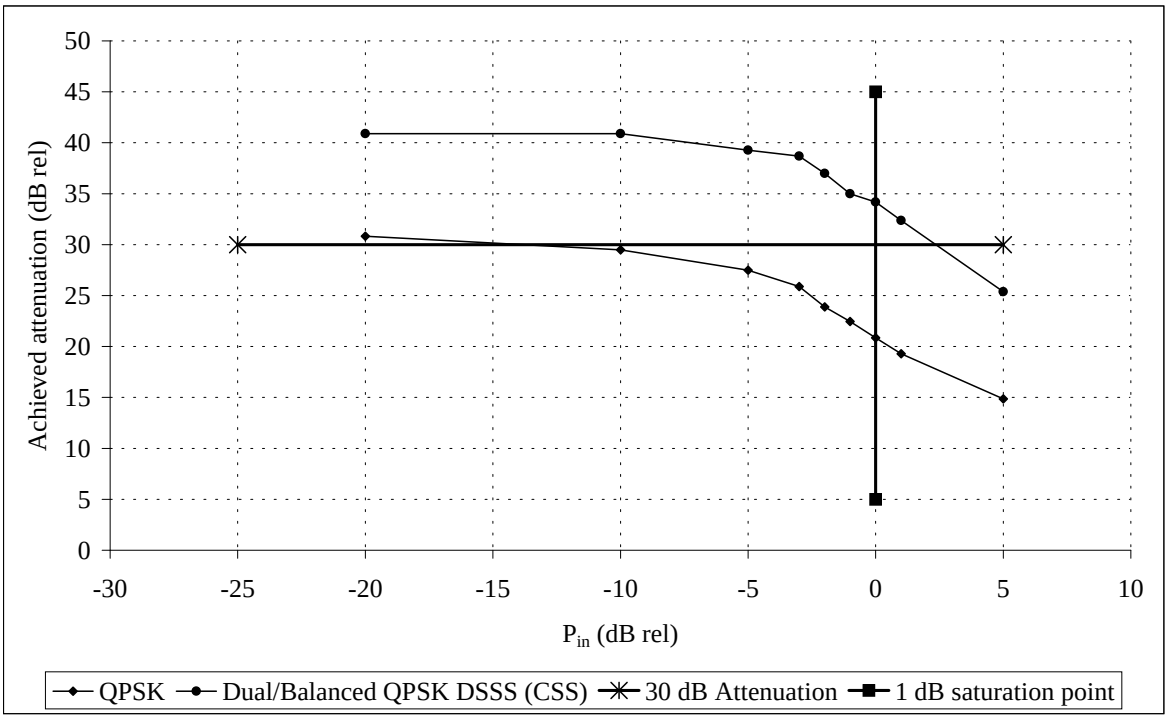

FIGURE 11.17: Graphical display of the spectral regrowth of the $\frac{1}{2}$C configuration CDMA system employing complex spreading sequences relative to a standard QPSK reference system as a function of power amplifier (PA) input level relative to the 1dB PA compression point.

The power saturation measurement results are summarized in Figure 11.17.

Table 11.1 compares the spectral regrowth results of the modulation schemes considered. The results indicate a relative advantage of several dBs for the 1/2C and 1C modulation schemes relative to QPSK in terms of the amount of power back-off required to operate within a specified RF mask and corresponding spectral regrowth limits.

Table 11.1: Summary of spectral regrowth of three modulation schemes based on P_{in} (dB) (Power amplifier input power level relative to the 1 dB PA compression point)

P_{in} (dB rel) Mod. Scheme	-20	-10	-5	-3	-2	-1	0	1	5
QPSK	30.82	29.49	27.48	25.89	23.88	22.46	20.86	19.28	14.86
Dual/Balanced DSSS QPSK (CSS)	40.89	40.98	39.28	38.68	37.00	35.00	34.18	32.38	25.38

11.7 CONCLUSIONS

With reference to Figure 11.9, a direct comparison between the PAPR-CCDF measurements of the said modulation schemes reveals 90-percentile peak-to-average power ratio advantages of approximately 2.15 and 2.2 dB for 1/2C and 1C, respectively, relative to QPSK under identical operating (filtering) conditions, but with data throughput rates in the ratio 1:2 compared to the QPSK reference system. A small but remarkable statistical PAPR advantage is noted for the multi-dimensional 1C WCDMA modulation scheme relative to the perfectly constant envelope 1/2C configuration (approximately 0.25 dB), as well as a large improvement (approximately 2.5 dB) on the Nyquist filtered QPSK reference system.

The relative PAPR CCDF measurement differences amongst the patented 1/2C and 1C WCDMA modulation schemes and the reference QPSK system depicted in Figure 11.9 exhibit remarkable correspondence with the relative power saturation and back-off hardware measurements which have been presented in Section 11.6. The results indicate that the QPSK modulation format must operate at a back-off of more than 10 dB (typically 14 dB) relative to the 1 dB saturation point in order to conform to the cdma2000 spectral mask at the 3 MHz, -30 dB attenuation reference points. The corresponding required back-offs for the proprietary 1/2C and 1C modulation schemes are 0 dB and -2 dB relative to 1 dB saturation point, respectively. In fact, no backup is required for the 1/2C modulator, which can operate well within the limits defined by the RF spectral mask at input levels up to 2 dB above the power amplifier 1 dB saturation point.

From the results presented it may be concluded that both CE-RU-filtered modulation schemes considered in this chapter have PAPR-CCDF and spectral regrowth advantages (measured in terms of how successful the RF spectral mask is met at the 3 MHz, -30 dB attenuation reference points) in the order of 12 to 16 dB over the standard QPSK reference system for power amplifier input levels in the range of -15 to +3 dB relative to the amplifier 1 dB saturation point. It should be emphasised that all the benefits in terms of spectral and power efficiency offered by all three CE-RU WCDMA modulation schemes are obtained while achieving uncoded bit error rate (BER) performances approximately equal (to within 0.5 to 2 dB) of the theoretical QPSK BER performance AWGN, as well as in Rayleigh fading, with data throughput advantages 1 and 2 for 1/2C and 1C, respectively, compared to the conventionally filtered WCDMA QPSK-modulated reference system.

CHAPTER TWELVE

ASPECTS FOR FUTURE RESEARCH AND CONCLUSION

12.1 ASPECTS FOR FUTURE RESEARCH

A wireless DSSS communication link was developed during the research and development study, comprising the various subsystems and exploiting the advantages and applications outlined in this dissertation. A two-dimensional hardware prototype evolved, consisting of a DSSS transmitter and receiver, employing complex spreading sequences. Novel carrier synchronization techniques, using novel sum and difference sequence combinations, were designed and analysed in order to overcome the presence of unwanted interference terms, generated in the process of achieving carrier phase estimation in the presence of complex spreading. Dedicated code tracking loops have been proposed, designed and analyzed, capable of tracking the chip timing of the desired received DSSS signal's complex spreading code within fractions of one chip period. The proposed new generic DSSS system is furthermore sufficiently versatile to allow the use of either binary or complex spreading sequences. Families of Non-Linearly-Interpolated Root-of-Unity (NLI-RU) filtered complex spreading sequences have been utilised, capable of producing constant-envelope Double-Side-Band (DSB), as well as Single-Side-Band (SSB) DSSS outputs. The generic DSSS system is very flexible in terms of data rate, spreading sequence length and Processing Gain (PG). Not only can different multi-phase as well as multi-amplitude modulation techniques be very easily implemented, but the system may also be easily adapted to serve various applications.

By virtue of the numerous possibilities and applications outlined for the prototype DSSS technology developed, a multitude of possible future research opportunities can be identified.

Different modulation extensions can be evaluated on the same platform. The system can be further evaluated in terms of different channel effects, etc. Additional digital signal processing (DSP) building blocks may be added to improve system performance. Typical building blocks are multi-user interference cancellation (MUIC), RAKE combining, forward error correction (FEC) coding, power control and equalisation. Although this dissertation concentrated on the application of CSS in two-dimensional modulation structures, extension of the principles to more dimensions (¿2) leaves scope for significantly advanced systems with improved spectral efficiency. The upwards-extendibility of the complex modulation concepts developed in this dissertation is a topic for future research.

12.2 CONCLUSION

The ultimate goal of this research project was to design and develop a generic DSSS modem employing complex spreading sequences (CSS). This objective has been achieved with the establishment of a prototype WLL RF-link, providing the required vehicle and test bed to verify and illustrate all the principles and concepts formulated, e.g., the concept of linear root-of-unity filtering and its realisation in hardware. The list of objectives outlined in the introductory part of the dissertation will now be reviewed briefly to illustrate what has been achieved, and the verify if all goals have been met.

The first objective was the theoretical design and analysis of a DSSS communication system employing complex spreading sequences. The theoretical analysis and design are presented in PART II of the dissertation, consisting of Chapters $2, 3, 4, 5$ and 6.

The second objective comprised the simulation of a DSSS wireless communication link employing complex spreading sequences. A complete system simulation was performed and all the results are depicted and described in PART III, consisting of Chapter 7 and 8, for the DSSS transmitter and receiver, respectively.

The design of implementation structures for the transmitter and receiver of a DSSS communication system with complex spreading sequences, employing appropriate (FPGA) implementation technologies forms the third objective. Different implementation technologies have been investigated and used in the hardware implementation of the transmitter and receiver structures. The system evolved from fast discrete FCT logic to the final Altera FPGA-based development platform on which the complete prototype system was finalised. Details of the hardware design and development are presented in Chapter 9 and 10.

The fourth objective comprised the design and realisation of implementation technologies for the synchronization of timing (code, bit and frame synchronisation), carrier frequency and phase estimation of a DSSS communication system employing complex spreading sequences. All the synchronisation subsystems have been implemented in reprogrammable FPGA hardware, resulting in the generation of considerable intellectual property (IP) in the form of additional DSSS/CDMA VHDL functional core software. These subsystems were all integrated as part of the final wireless DSSS modem link on the FPGA-based development platform. Chapter 10 contains the description and results of the final hardware DSSS modem transmitter and receiver prototype, utilising complex spreading sequences.

The final objective comprised the simulation and prototype hardware performance evaluation of the DSSS system under typical AWGN and some fading mobile channel conditions, including power saturation effects. The verification and performance evaluation of the implemented DSSS communication RF-link are presented in Chapter 11. Firstly the bit error rate (BER) performance was investigated. The BER performance of the hardware implemented differential encoded coherent balanced/dual DSSS modem is presented in Figure 11.1, and compared with the theoretical BER of QPSK and differentially encoded coherent QPSK. The hardware implementation loss of the DSSS system has been found to be in the order of $1.5\ dB$. This hardware implementation loss includes the losses due to the surface acoustic wave (SAW) bandpass filters, the non-linear effects of mixers in the transmission path, the effect of drifting and phase noise in all the local oscillators (LOs), etc. Considering all the impairments that have been included, the observed hardware implementation loss is relatively small. The system was simulated to investigate the effect of different phase errors on the BER performance. This simulation results are depicted in Figure 11.4 and is compared to the theoretical BER results of a QPSK system with different phase errors between transmit and receive carriers, presented in Figure 11.3. The simulated BER results correspond with the theoretical BER results for specific phase errors. System simulations were performed in a Raleigh-faded and AWGN channel. The simulated BER results obtained have been compared with the corresponding BER result of a theoretical QPSK system in an AWGN and Raleigh-faded channel, as shown in Figure 11.5.

Two specifications have been identified to evaluate the power amplifier saturation performance of the DSSS system. The first specification verifies if the output spectrum meets a specific RF mask specified for the transmitter output power spectrum. The second

verification test establishes whether a certain required bit error rate performance is achieved under power saturation conditions. The power efficiency of modulation schemes are usually measured in terms of the peak-to-average power ratio (PAPR) characteristics exhibited by the modulator output signal. Constant envelope modulation schemes exhibit very little, if any, spectral regrowth under non-linear amplification (saturation). Thus, with a constant envelope modulation communication system, larger power efficiency may be achieved by allowing the power amplifier to operate closer to the amplifier 1dB saturation point, without causing excessive spectral regrowth. It was found that the proposed constant envelope (CE) DSSS communication system employing complex spreading sequences passed both power saturation tests and outperformed binary DSSS systems employing Nyquist filtering, yielding non-constant envelope outputs. The power saturation evaluation results are presented in Chapter 11, with associated summaries given in Table 11.1 and Figure 11.17, respectively.

As a final example, an appropriately adapted version of the wireless DSSS communication system proposed in this dissertation, employing complex spreading sequences, was in fact utilised for a specific commercial application. The particular application comprised a long distance ($>$ 200 km) ultra wide-band DSSS equivalent of the prototype DSSS system, capable of meeting all the stringent requirements specified for this project, including low probability of interception (LPI) operation and synchronisation in the presence of adverse (sub-zero dB SNR) conditions. This project provided the final verification of the integrity of the results presented in this dissertation, and also illustrated the versatility and applicability of the concepts proposed, developed and presented during this research programme.

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APPENDIX A
UNIQUE COMBINATION SEQUENCE RESULTS

Unique combinations of the real and imaginary parts of the complex spreading sequences are used as defined by

$$C_{r_1 comb} = C_{r_1} - C_{i_1} \tag{A.1}$$

$$C_{i_1 comb} = -C_{r_1} - C_{i_1} \tag{A.2}$$

and is shown in Figure A.1. The real and imaginary parts of the root-of-unity filtered complex spreading sequence 1 and 6 of length, $L = 121$, and samples per chip, $spc = 8$, are depicted in Figures A.1 and A.4, while the real vs. imaginary parts of sequence 1 and 6 are shown in Figures A.2 and A.5, respectively. The power spectral densities (PSD) for sequence 1 and sequence 6 are shown in Figures A.3 and A.6, respectively.

The same for complex spreading sequence 6

$$C_{r_6 comb} = C_{r_6} - C_{i_6} \tag{A.3}$$

$$C_{i_6 comb} = -C_{r_6} - C_{i_6} \tag{A.4}$$

and is depicted in Figure A.4.

A.1 AUTOCORRELATION FUNCTION

The sequence $\{s_k\}$ of length L has periodic AC function, $R_{ss}[l]$, given as:

$$R_{ss}[l] = \sum_{k=0}^{L-1} s[k] \cdot s^*[k+l]_{mod\, L} \tag{A.5}$$

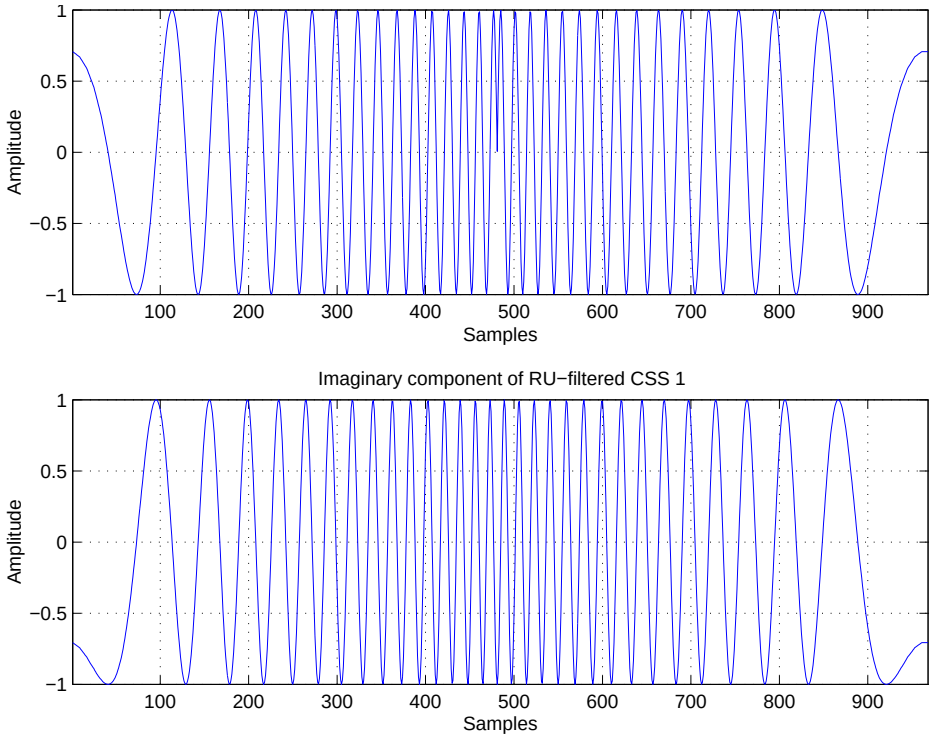


FIGURE A.1: The Real, (a), and Imaginary, (b), part of the unique combination of CSS 1. $(L = 121, RU filtered, spc = 8)$

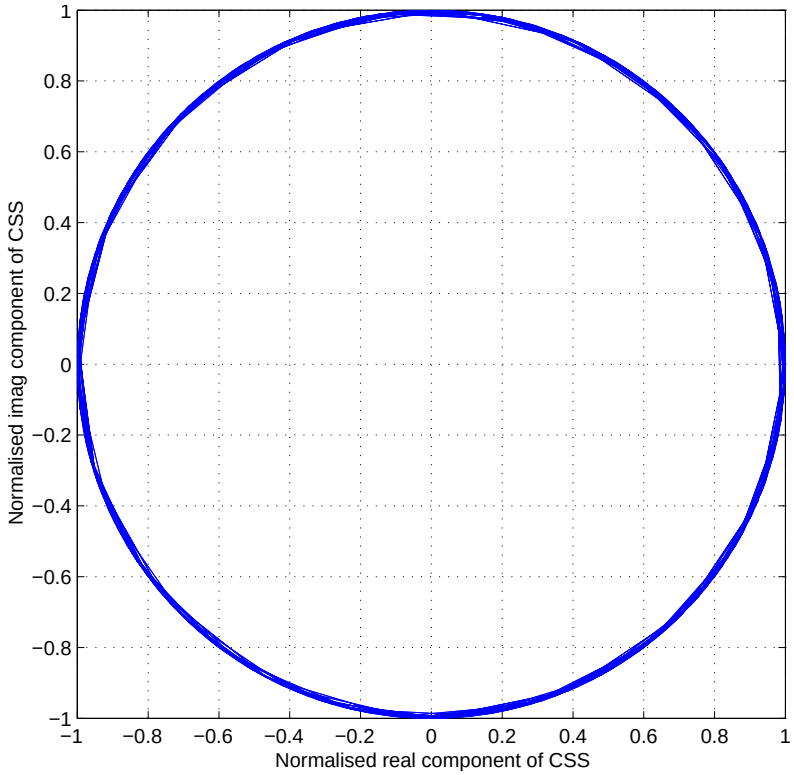


FIGURE A.2: Real vs. Imaginary part of unique combination of complex spreading sequence 6. $(L = 121, RU filtered, spc = 8)$

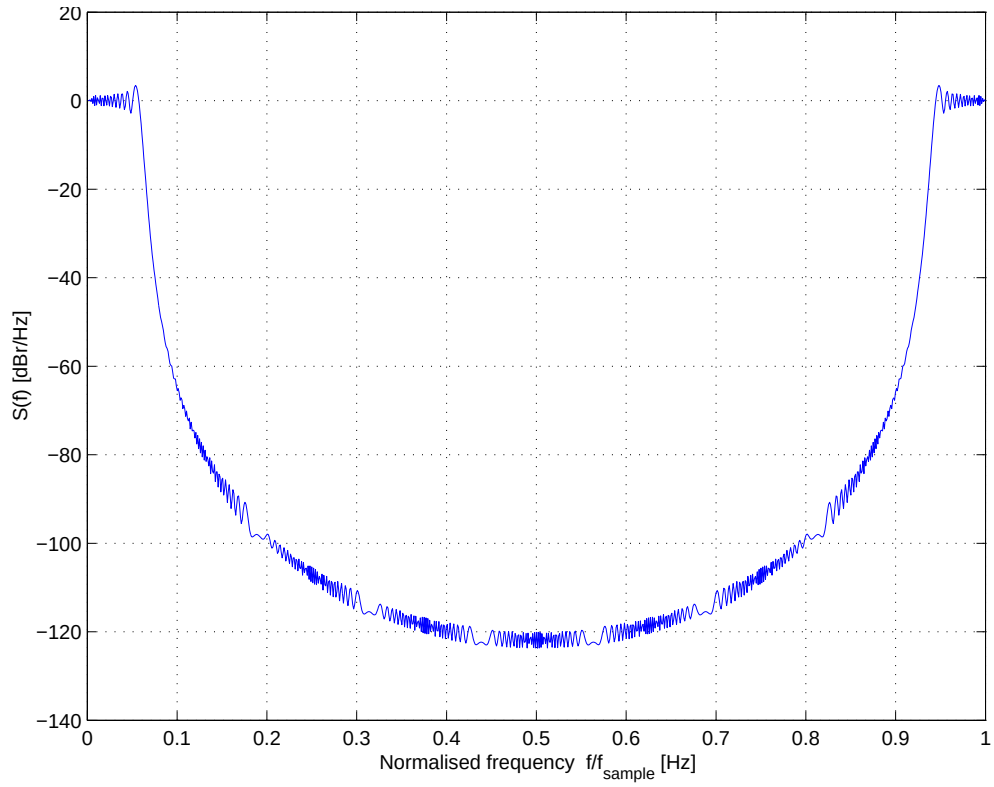


FIGURE A.3: Power spectral density (PSD) of unique combination of complex spreading sequence 1. $(L = 121, RU filtered, spc = 8)$

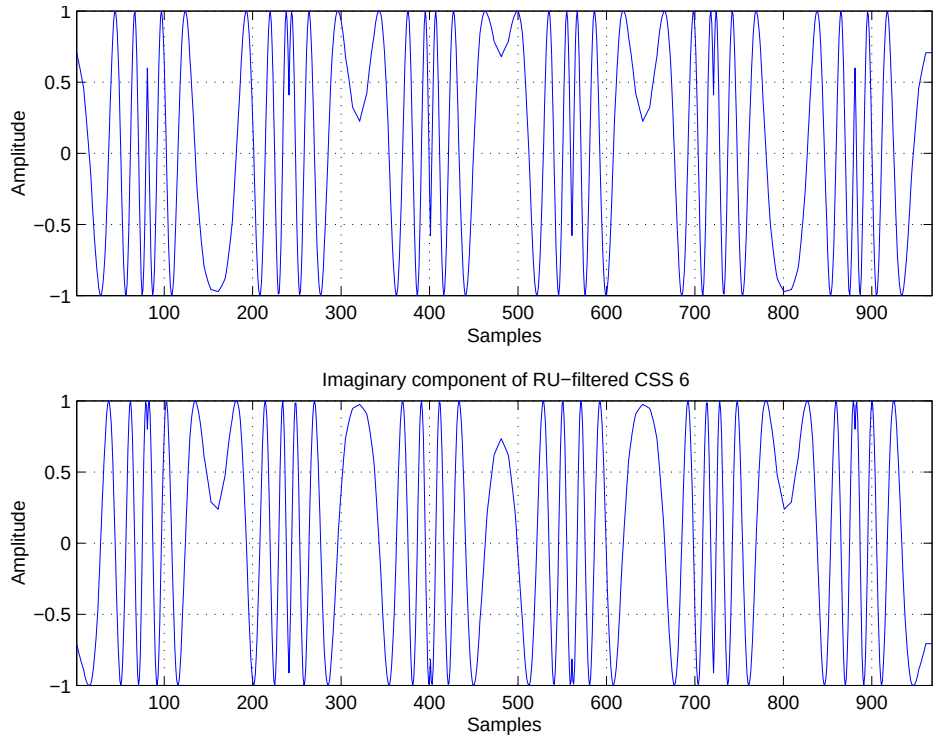


FIGURE A.4: The Real, (a), and Imaginary, (b), part of unique combination of CSS 6. $(L = 121, RU filtered, spc = 8)$

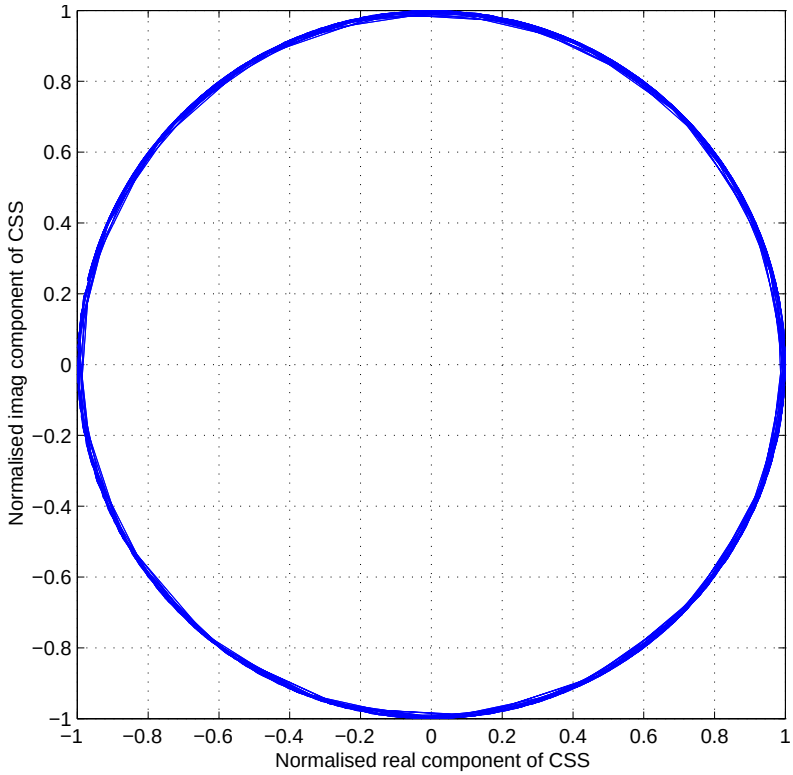


FIGURE A.5: Real vs. Imaginary part of unique combination of complex spreading sequence 6. $(L = 121, RU filtered, spc = 8)$

where * denotes the complex conjugate, the index $[k + l]$ is computed modulo L, and the time shift is l.

Thus for the ZC sequences, the periodic AC function is:

$$R_{ss}[l] = \sum_{k=0}^{L-1} W_L^{\frac{k(k+1)}{2}} \cdot W_L^{\frac{-(k+l)_{mod\,L}\,((k+l)_{mod\,L}+1)}{2}} \tag{A.6}$$

for $q = 0$ and L odd.

The periodic AC functions for the ZC sequences 1 and 6, for a length of 121, can be seen in Figures A.7, A.8 and Figures A.9, A.10, respectively.

For a sequence s_k of length L the aperiodic AC function is defined as:

$$R_{ss}[l] = \int_{-\infty}^{\infty} s[l] \cdot s^*[t + l]\, dl \tag{A.7}$$

where * denotes the complex conjugate and the time shift is l.

In discrete time notation the aperiodic AC function can be expressed as:

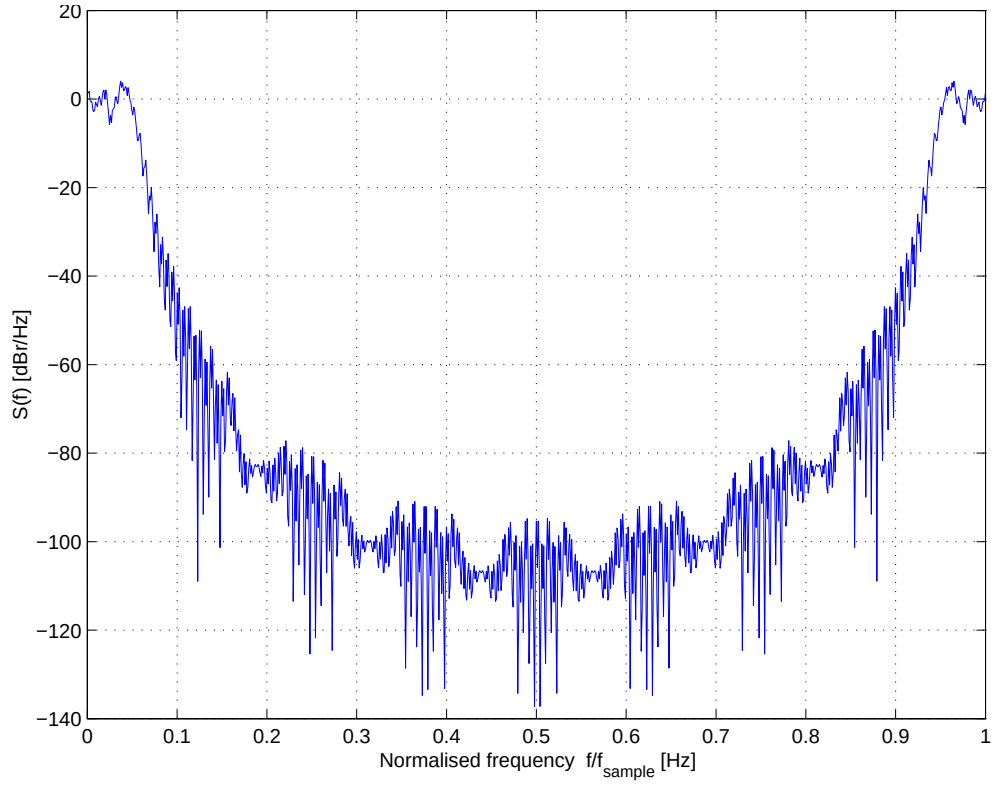


FIGURE A.6: Power spectral density (PSD) of unique combination of complex spreading sequence 6. $(L = 121, RU filtered, spc = 8)$

$$R_{ss}[l] = \begin{cases} \sum_{k=0}^{L-1-l} s[l] \cdot s^*[k+l] & ;0 \leq l \leq L-1 \\ \sum_{k=0}^{L-1+l} s[k-l] \cdot s^*[k] & ;1-L \leq l < 0 \\ 0 & ;\mid l \mid \geq L \end{cases} \tag{A.8}$$

For ZC sequences the aperiodic AC function is:

$$R_{aa}[l] = \begin{cases} \sum_{k=0}^{L-1-l} W_L^{\frac{k(k+1)}{2}} \cdot W_L^{\frac{-(k+1)(k+l+1)}{2}} & ;0 \leq l \leq L-1 \\ \sum_{k=0}^{L-1+l} W_L^{\frac{(k-l)(k-l+1)}{2}} \cdot W_L^{\frac{-k(k+l)}{2}} & ;1-L \leq l < 0 \\ 0 & ;\mid l \mid \geq L \end{cases} \tag{A.9}$$

for $q = 0$ and L odd.

The aperiodic AC functions for the ZC sequences 1 and 6, for a length of 121, can be seen in Figures A.11, A.12 and Figures A.13, A.14, respectively.

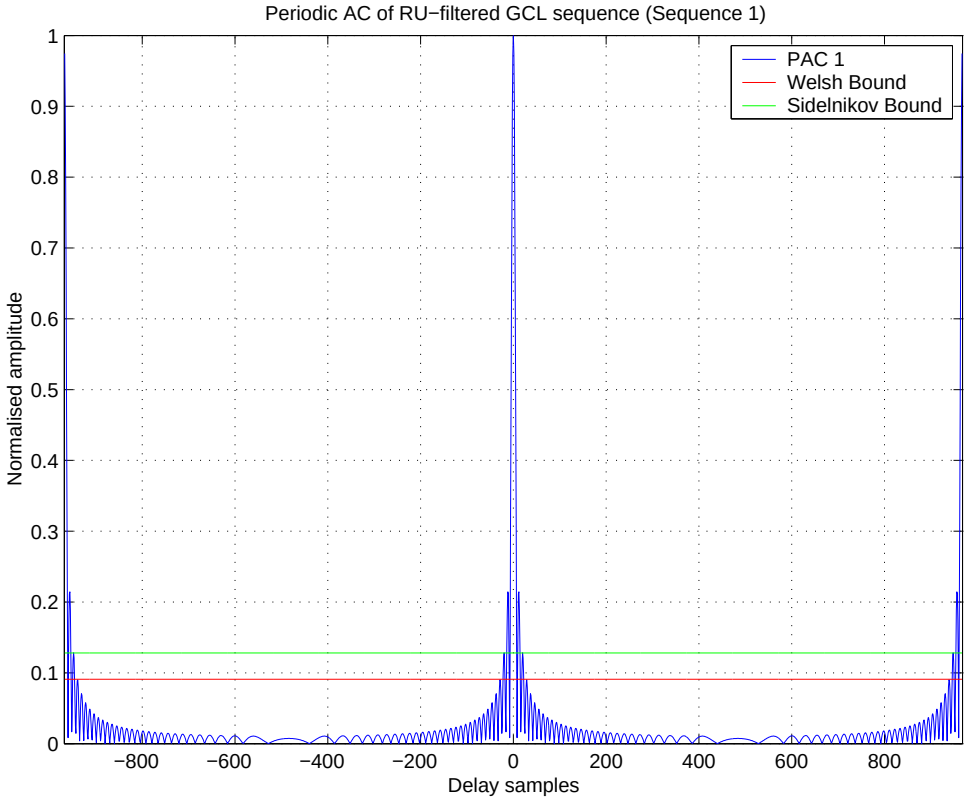


FIGURE A.7: Periodic Auto Correlation (PAC) function of unique combination of complex spreading sequence 1. $(L = 121, RU filtered, spc = 8)$

A.2 CROSSCORRELATION FUNCTION

The CC function shows the correspondence between two signals at different time shifts. The periodic CC function between any two sequences s_k and u_k, both of length L, is defined as:

$$R_{su}[l] = \sum_{k=0}^{L-1} s[k] \cdot u^*[(k+l)_{modL}] \tag{A.10}$$

where $*$ denotes the complex conjucate, the index $(k + l)$ is computed modulo L, and the time shift is l.

Thus for the ZC sequence the periodic CC function is:

$$R_{ab}[l] = \sum_{k=0}^{L-1} W_{L_a}^{\frac{k(k+1)}{2}} \cdot W_{L_a}^{\frac{-(k+l)_{modL}((k+l)_{modL}+1)}{2}} \tag{A.11}$$

for $q = 0$ and L odd.

The periodic cross correlation functions between spreading code number 1 and 6 are shown in Figures A.15 and A.16.

The aperiodic CC function between any two sequences s_k and u_k, both of length L, in discrete time notation is defined as:

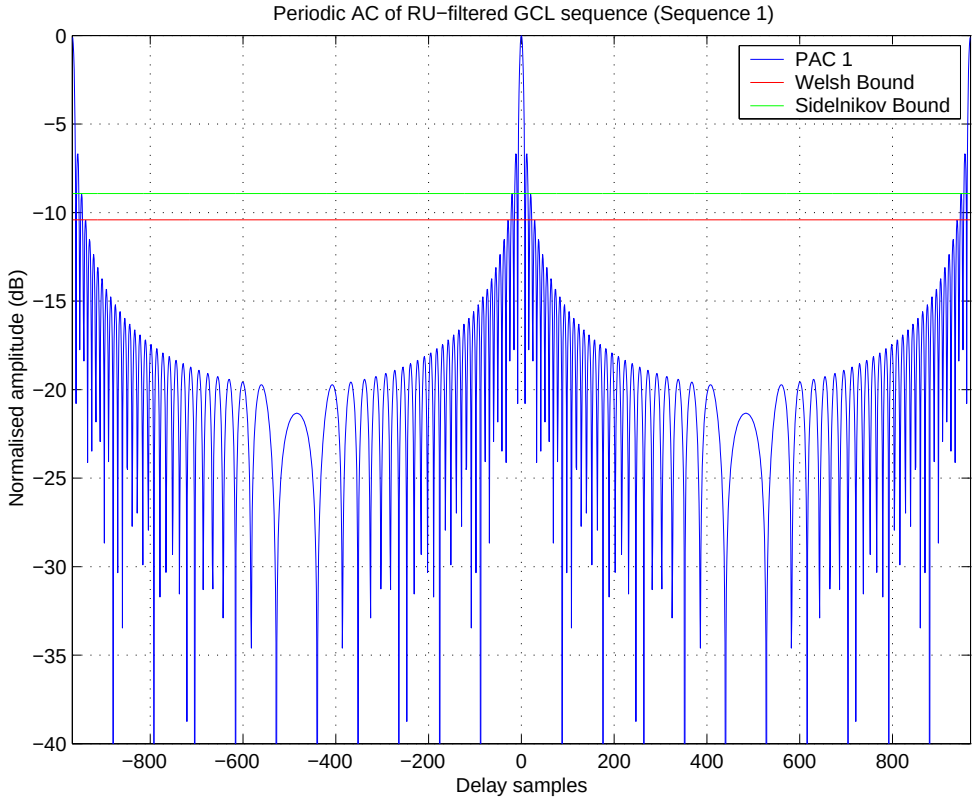


FIGURE A.8: Periodic Auto Correlation (PAC) function of unique combination of complex spreading sequence 1 in decibels. $(L = 121, RU filtered, spc = 8)$

$$R_{su}[l] = \begin{cases} \sum_{k=0}^{L-1-l} s[l] \cdot u^*[k+l] & ; 0 \leq l \leq L-1 \\ \sum_{k=0}^{L-1+l} s[k-l] \cdot u^*[k] & ; 1-L \leq l < 0 \\ 0 & ; \mid l \mid \geq L \end{cases} \tag{A.12}$$

where * denotes complex conjugate and the time shift is l.

For the ZC sequences the aperiodic CC function is

$$R_{ab}[l] = \begin{cases} \sum_{k=0}^{L-1-l} W_{L_a}^{\frac{k(k+1)}{2}} \cdot W_{L_b}^{\frac{-(k+1)(k+l+1)}{2}} & ; 0 \leq l \leq L-1 \\ \sum_{k=0}^{L-1+l} W_{L_a}^{\frac{(k-l)(k-l+1)}{2}} \cdot W_{L_b}^{\frac{-k(k+l)}{2}} & ; 1-L \leq l < 0 \\ 0 & ; \mid l \mid \geq L \end{cases} \tag{A.13}$$

The aperiodic cross correlation functions for the ZC sequences are depicted in Figures A.17 and A.18.

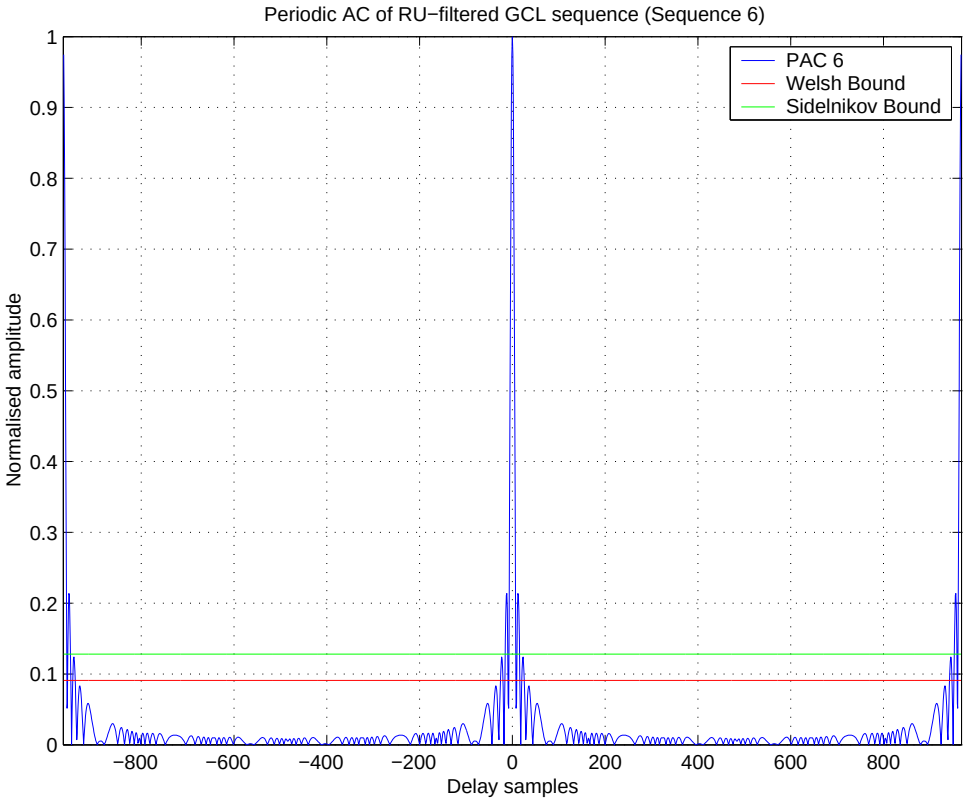


FIGURE A.9: Periodic Auto Correlation (PAC) function of unique combination of complex spreading sequence 6. $(L = 121, RUfiltered, spc = 8)$

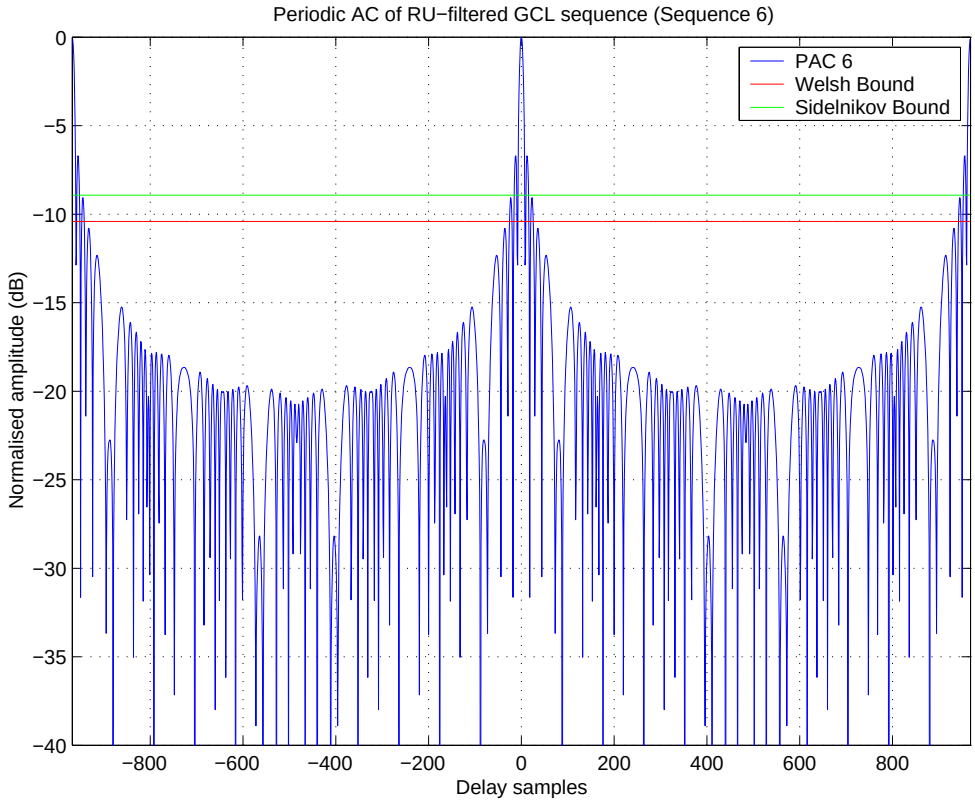


FIGURE A.10: Periodic Auto Correlation (PAC) function of unique combination of complex spreading sequence 6 in decibels. $(L = 121, RU filtered, spc = 8)$

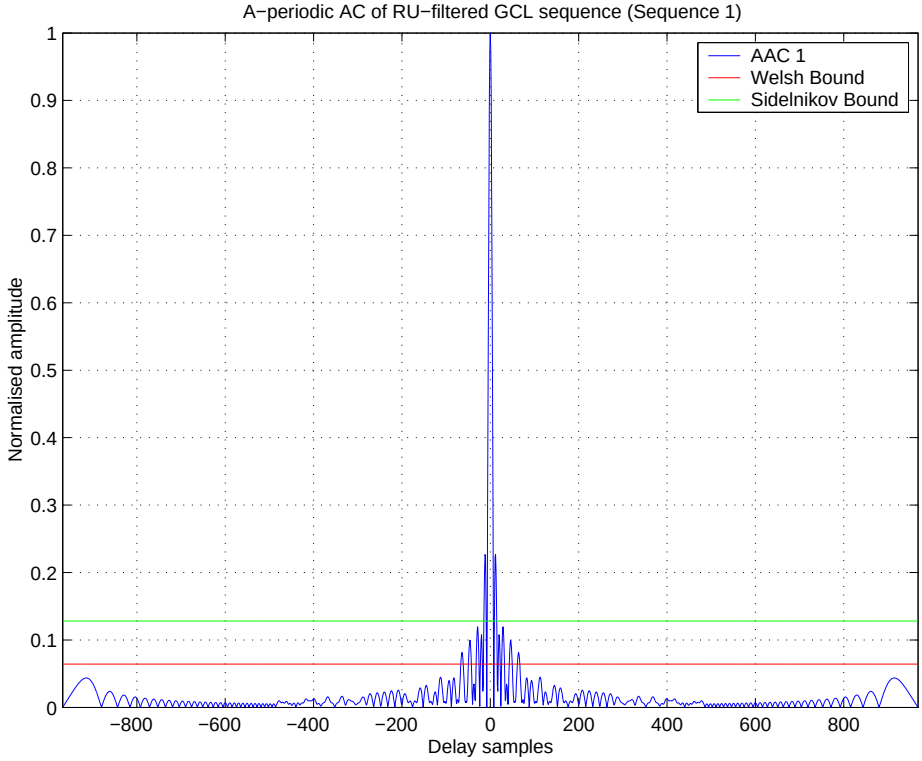


FIGURE A.11: Aperiodic Auto Correlation (AAC) function of unique combination of complex spreading sequence 1. $(L = 121, RU filtered, spc = 8)$

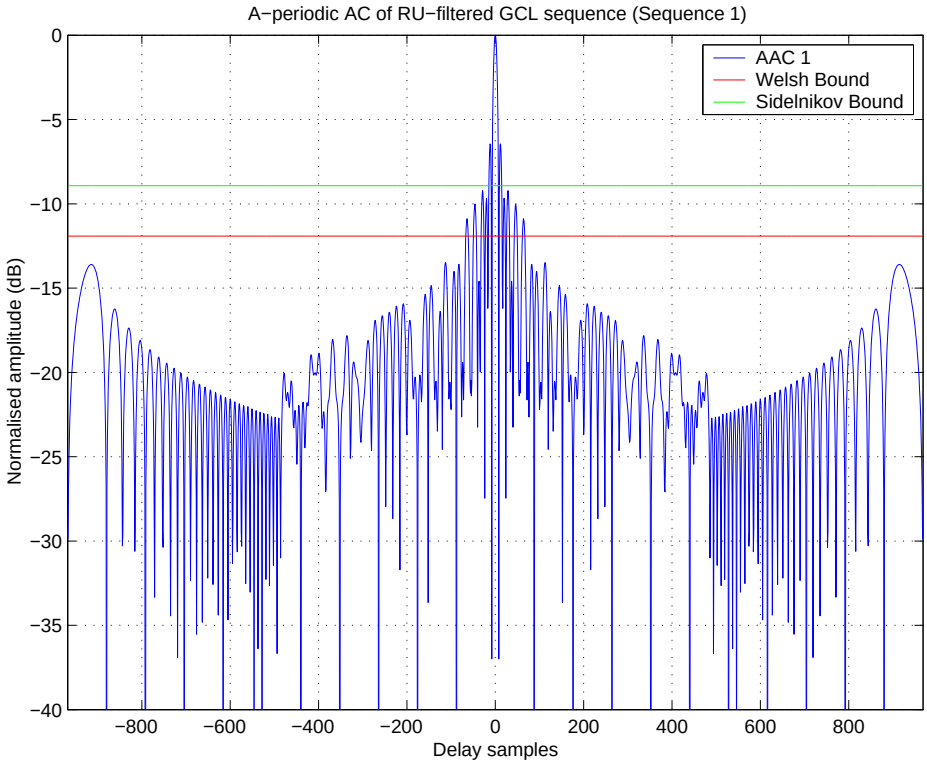


FIGURE A.12: Aperiodic Auto Correlation (AAC) function of unique combination of complex spreading sequence 1 in decibels. $(L = 121, RU filtered, spc = 8)$

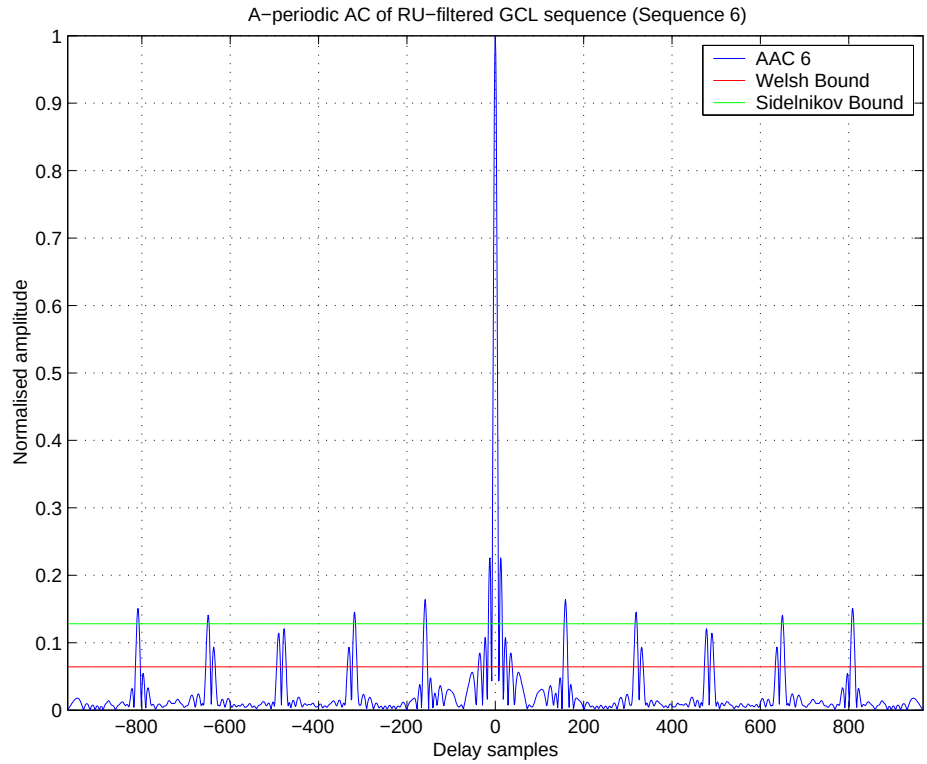


FIGURE A.13: Aperiodic Auto Correlation (AAC) function of unique combination of complex spreading sequence 6. $(L = 121, RU filtered, spc = 8)$

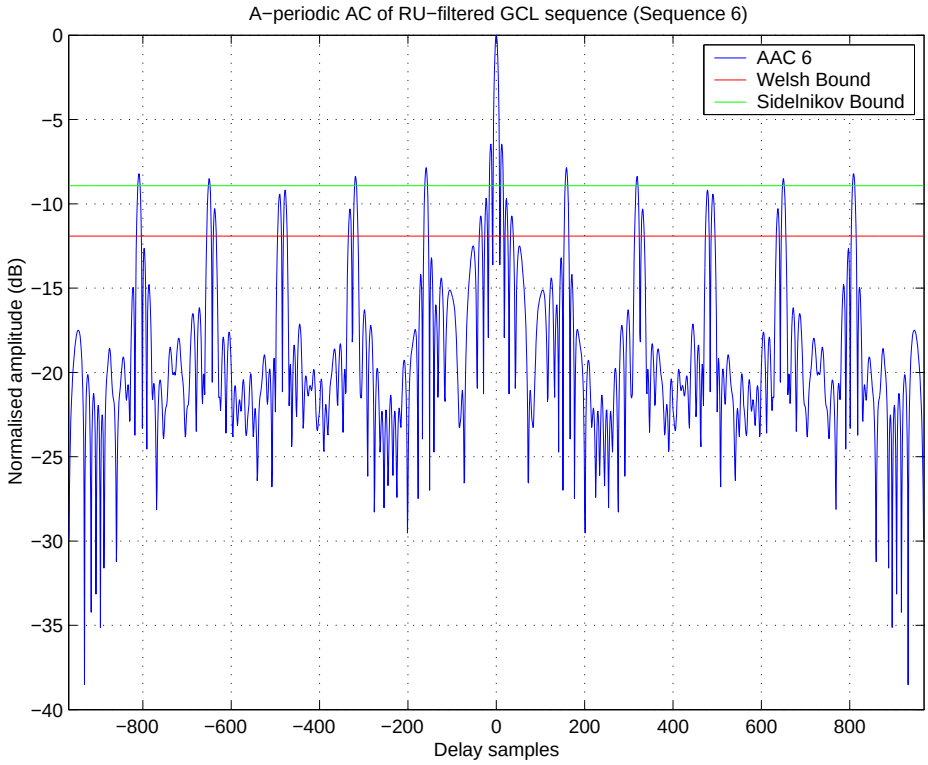


FIGURE A.14: Aperiodic Auto Correlation (AAC) function of unique combination of complex spreading sequence 6 in decibels. $(L = 121, RU filtered, spc = 8)$

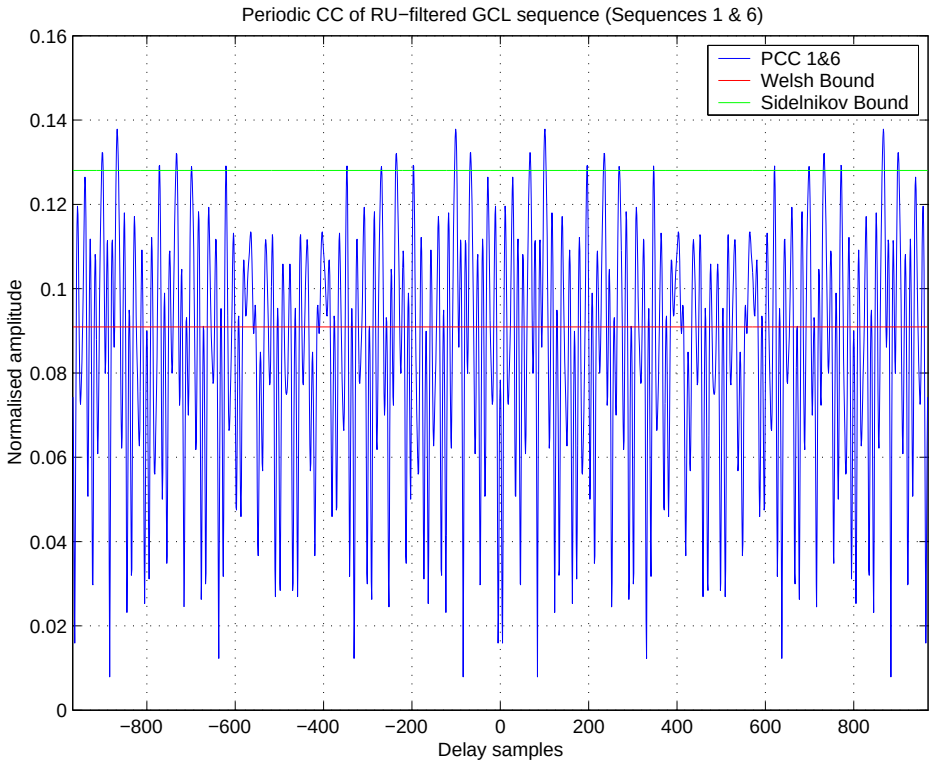


FIGURE A.15: Periodic Cross Correlation(PCC) function between unique combinations of complex spreading sequences 1 and 6. $(L = 121, RU filtered, spc = 8)$

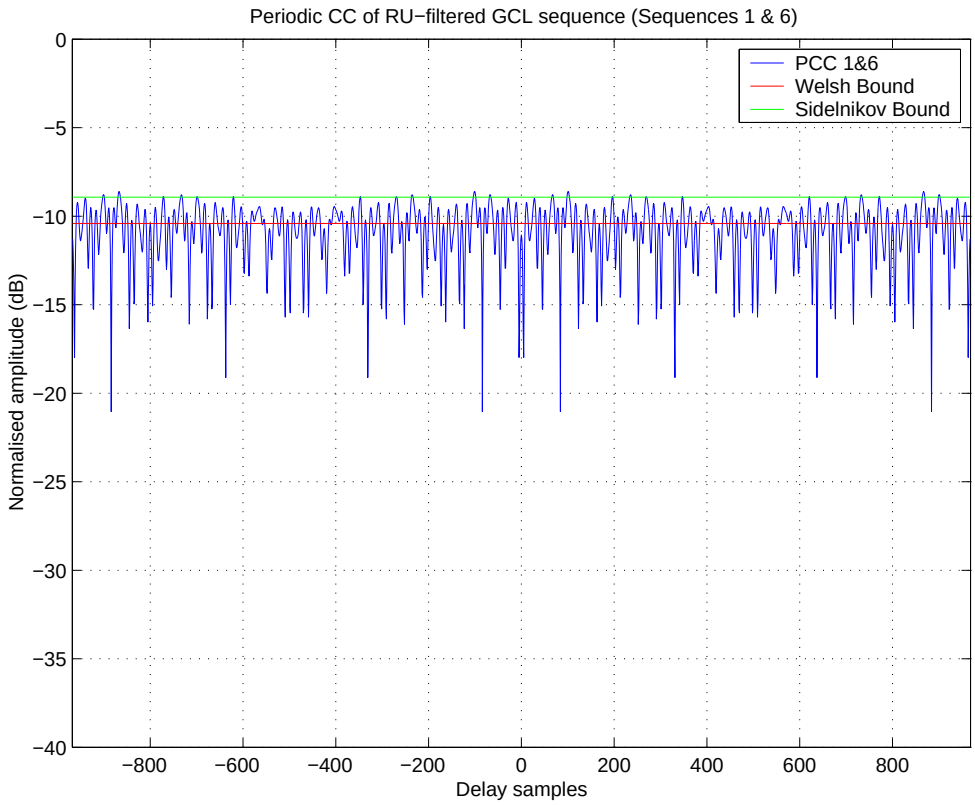


FIGURE A.16: Periodic Cross Correlation(PCC) function between unique combinations of complex spreading sequences 1 and 6 in decibels. $(L = 121, RU filtered, spc = 8)$

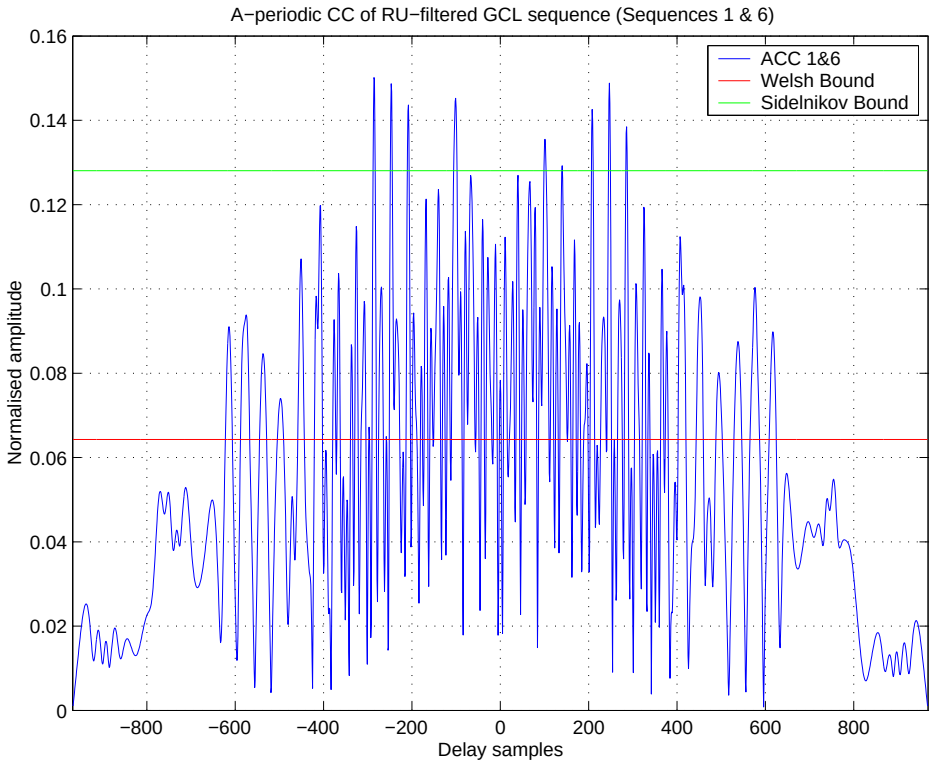


FIGURE A.17: Aperiodic Cross Correlation(PCC) function between unique combinations of complex spreading sequences 1 and 6. $(L = 121, RU filtered, spc = 8)$

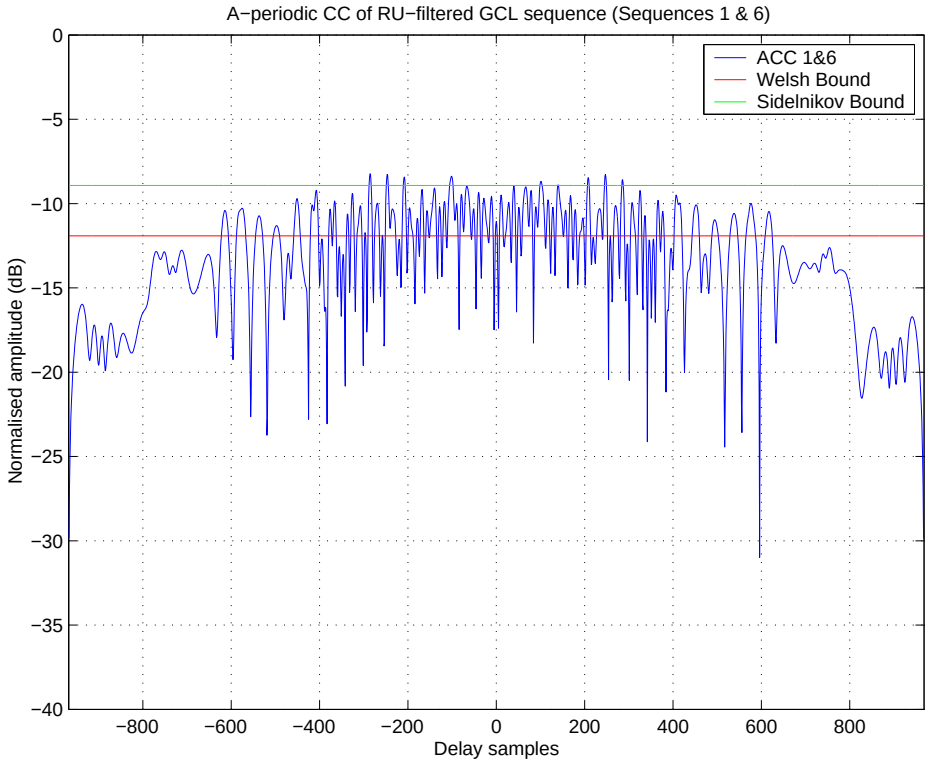
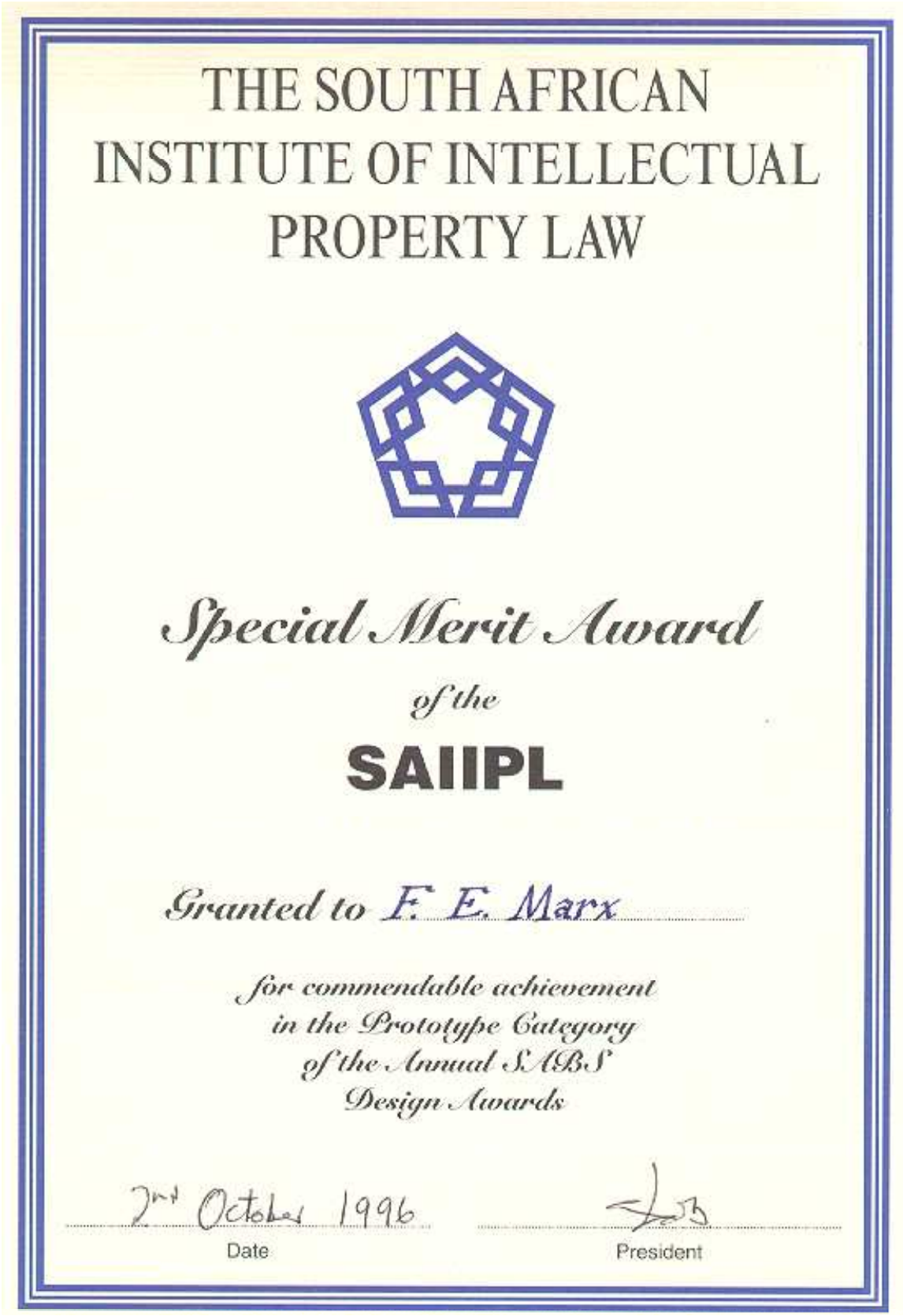


FIGURE A.18: Periodic Cross Correlation(PCC) function between unique combinations of complex spreading sequences 1 and 6 in decibels. $(L = 121, RU filtered, spc = 8)$

APPENDIX B

AWARDS RECEIVED DURING MASTERS DEGREE

- F.E. Marx and L.P. Linde, SABS design institute awards, 1996.
- F.E. Marx, Special Merit Award of the SAIIPL, 1996.
- L.P. Linde, D.J. van Wyk, B. Westra, F.E. Marx and W.H. Büttner, SABS design institute awards, 1997.



THE SOUTH AFRICAN
INSTITUTE OF INTELLECTUAL
PROPERTY LAW

Special Merit Award

of the

SAIIPL

Granted to F. E. Marx

for commendable achievement
in the Prototype Category
of the Annual SABS
Design Awards

2nd October 1996
Date

President

FIGURE B.1: Special Merit Award of the SAIIPL