APPENDIX A: DIGITAL DECODER – VHDL CODE AND CIRCUIT SCHEMATIC

The following shows the complete VHDL code that was used in order to design the digital decoder discussed in section 4.9. The circuit schematic of the digital decoder is also shown and its layout follows in Appendix B.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY phaseshift IS
PORT
(phaseSel: in std_logic_vector(3 downto 0);
IPhase: out std_logic_vector(7 downto 0);
Qphase: out std_logic_vector(7 downto 0));
END phaseshift;

ARCHITECTURE arch OF phaseshift IS
BEGIN
mapping: Process(phaseSel)
Begin
case phaseSel is
when "0000" =>
IPhase<= "11111111";
Qphase<= "00001111";
when "0001" =>
IPhase<= "01111111";
Qphase<= "00011111";
when "0010" =>
IPhase<= "00111111";
Qphase<= "00111111";
when "0011" =>
IPhase<= "00011111";
Qphase<= "01111111";
when "0100" =>
IPhase<= "00001111";
Qphase<= "11111111";
when "0101" =>
IPhase<= "00000111";
Qphase<= "01111111";
when "0110" =>
IPhase<= "00000011";
Qphase<= "00111111";
when "0111" =>
IPhase<= "00000001";
Qphase<= "00011111";
when "1000" =>
```

```
IPhase<= "00000000";
Qphase<= "00001111";
when "1001" =>
IPhase<= "00000001";
Qphase<= "00000111";
when "1010" =>
IPhase<= "00000011";
Qphase<= "00000011";
when "1011" =>
IPhase<= "00000111";
Qphase<= "00000001";
when "1100" =>
IPhase<= "00001111";
Qphase<= "00000000";
when "1101" =>
IPhase<= "00011111";
Qphase<= "00000001";
when "1110" =>
IPhase<= "00111111";
Qphase<= "00000011";
when "1111" =>
IPhase<= "01111111";
Qphase<= "00000111";
when others =>
IPhase<= "11111111";
Qphase<= "11111111";
end case;
end Process;
END arch;
```

Figure A.1. VHDL code used to design the digital decoder.

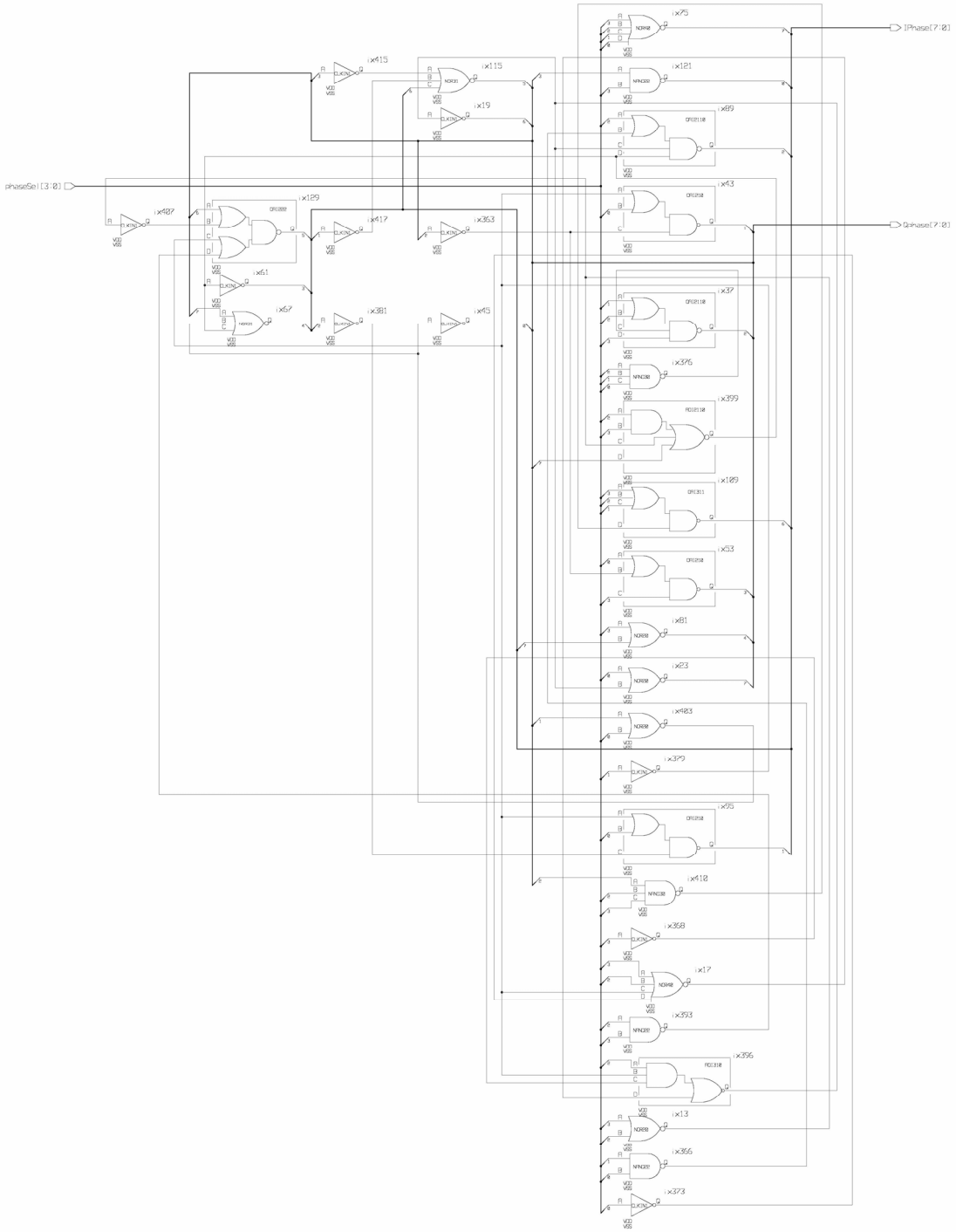

Figure A.2. Circuit schematic of the digital decoder that was generated using the VHDL code of Figure A.1.

APPENDIX B: DETAILED CIRCUIT LAYOUTS

The following shows more detailed figures of the main layouts as discussed in section 4.11. In particular, components labelled 1-6 in Figure 4.27 are shown in Figure B.2-Figure B.7 respectively with more detail. The legend of the layout is shown in Figure B.1 and the layout of the digital decoder is shown in Figure B.8. The bonding diagram of the QFN package is shown in Figure B.9. Chip photographs of components labelled 1,2,4 and 5 in Figure 4.27 are shown in Figure B.10-Figure B.13 respectively.

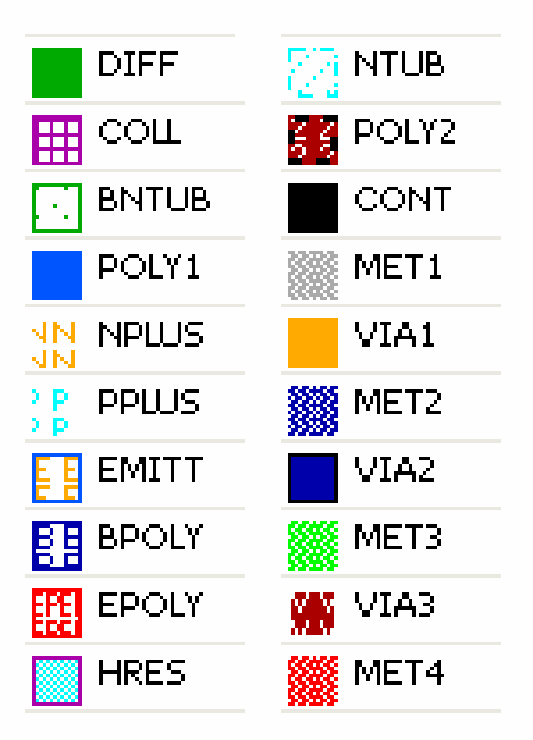

Figure B.1. Legend of the layouts that follow.

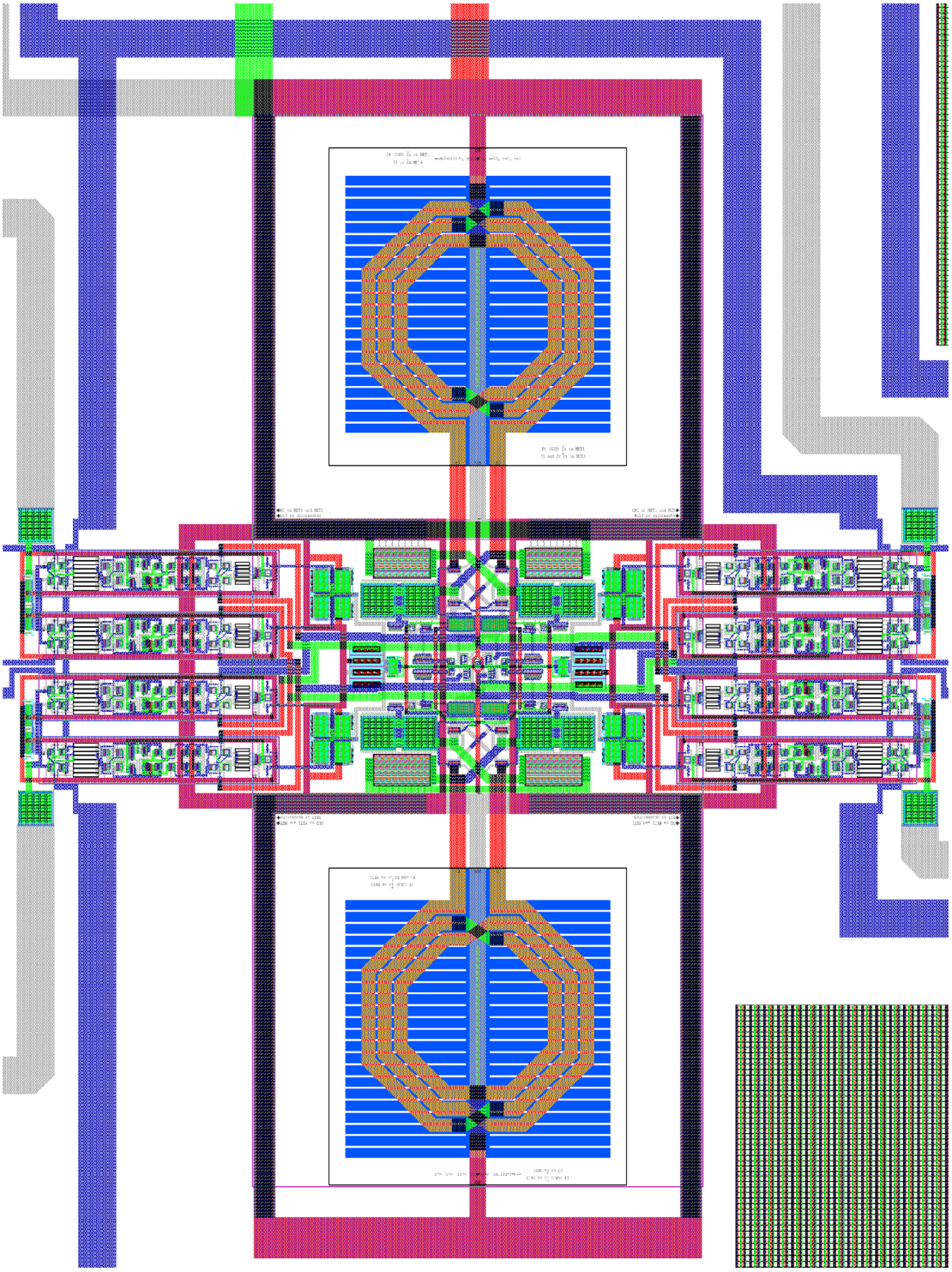

Figure B.2. Layout of the complete circuit, excluding the digital phase tuner.

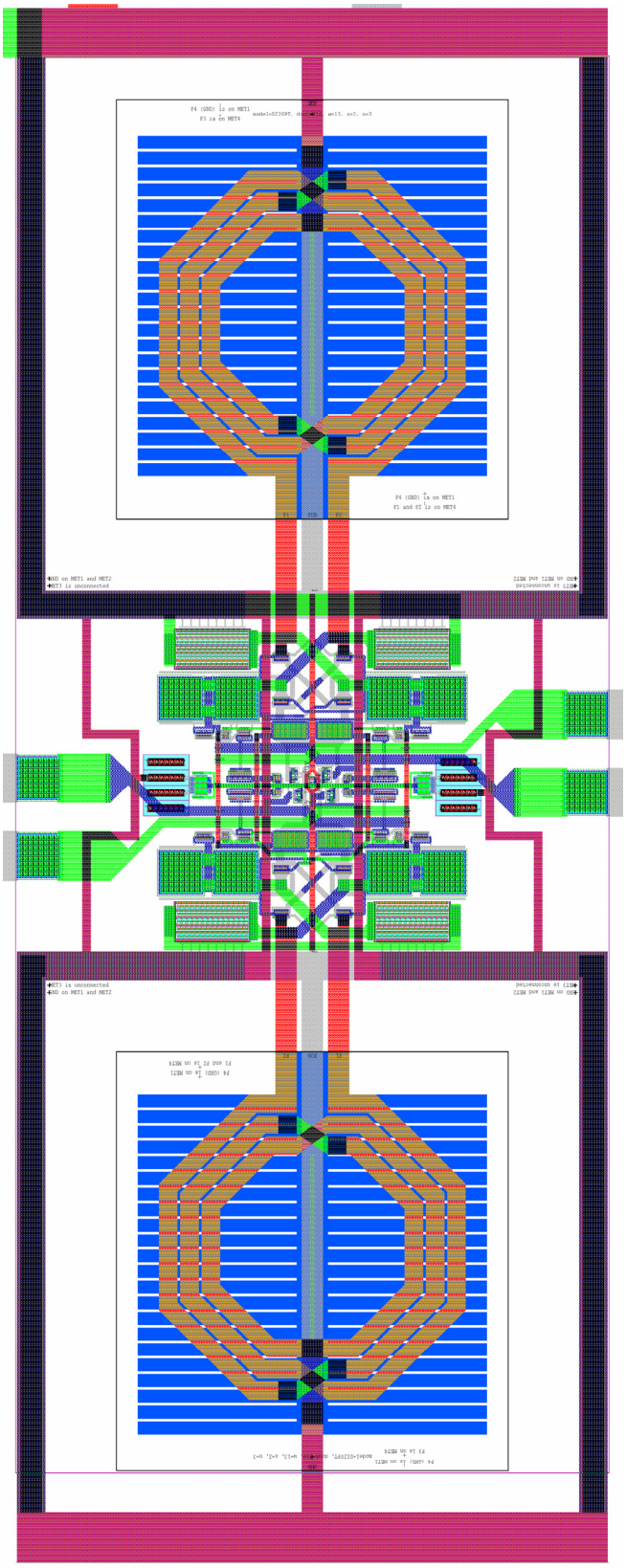

Figure B.3. Quadrature *LC*-VCO layout.

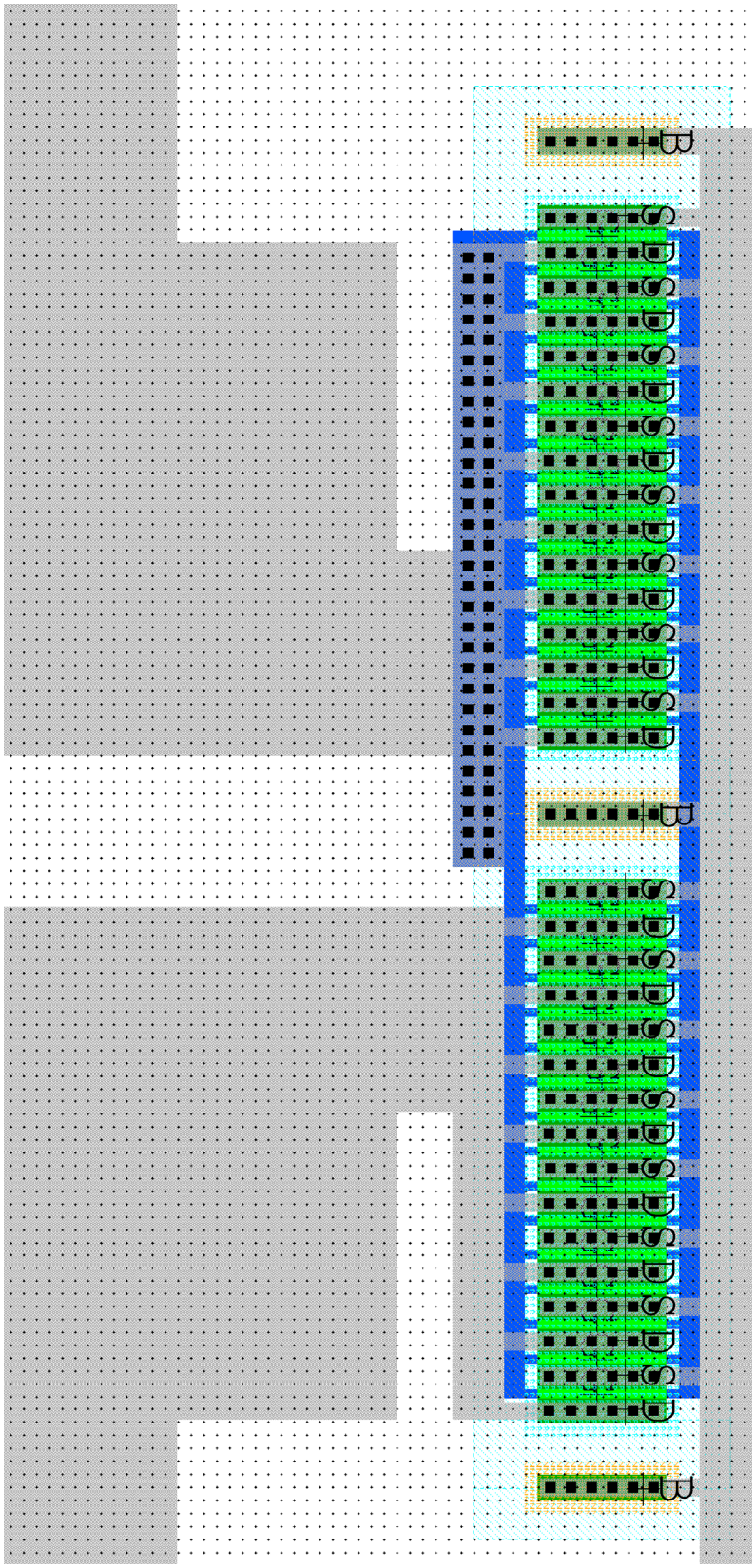

Figure B.4. Single current mirror layout.