DESIGN AND MANUFACTURE OF NANOMETRE-SCALE SOI LIGHT SOURCES

by

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SUMMARY

Keywords: Electron-beam lithography, Impurity redistribution, Nanometre-scale SOI, Quantum confinement, Silicon electroluminescence, Silicon infrared light emission, Silicon light source, SOI buried oxide light reflection, SOI light sources, SOI wafer manufacture.

To investigate quantum confinement effects on silicon (Si) light source electroluminescence (EL) properties like quantum efficiency, external power efficiency and spectral emission, thin Si finger junctions with nanometre-scale dimensions were designed and manufactured in a fully customized silicon-on-insulator (SOI) semiconductor production technology.

Since commonly available photolithography is unusable to consistently define and align nanometre-scale line-widths accurately and electron-beam lithography (EBL) by itself is too time-expensive to expose complete wafers, the wafer manufacturing process employed a selective combination of photolithography and EBL.

The SOI wafers were manufactured in the clean-rooms of both the Carl and Emily Fuchs Institute for Microelectronics (CEFIM) at the University of Pretoria (UP) and the Georgia Institute of Technology's Microelectronic Research Centre (MiRC), which made a JEOL JBX-9300FS electron-beam pattern generator (EPG) available. As far as is known this was the first project in South Africa (and possibly at the MiRC) that employed EBL to define functional nanometre-scale semiconductor devices.

Since no standard process recipe could be employed, the complete design and manufacturing process was based on self-obtained equipment characterization data and material properties.

The manufacturing process was unprecedented in both the CEFIM and MiRC clean-rooms. The manufacture of nanometre-scale Si finger junctions not only approached the manufacturing limits of the employed processing machinery, but also had to overcome undesirable physical effects that in larger-scale semiconductor manufacture usually are negligible. The device design, mask layout and manufacturing process therefore had to incorporate various material, equipment limitation and physical phenomena like impurity redistribution occurring during the physical manufacturing process.

Although the complicated manufacturing process allowed many unexpected problems to occur, it was expected that at least the simple junction breakdown devices be functional and capable of delivering data regarding quantum confinement effects.

Although due to design and processing oversights only 29 out of 505 measured SOI light sources were useful light emitters, the design and manufacture of the SOI light sources was successful in the sense that enough SOI light sources were available to conduct useful optical characterization measurements.

In spite of the fact that the functional light sources did not achieve the desired horizontal (width) confinement, measured optical spectra of certain devices indicate that vertical (thickness) confinement had been achieved.

All spectrometer-measured thickness-confined SOI light sources displayed a pronounced optical power for 600 nm < λ < 1 µm. The SOI light source with the highest optical power output emitted about 8 times more optical power around λ = 850 nm than a 0.35 µm bulk-CMOS avalanche light-source operating at the same current. Possible explanations for this effect are given.

It was shown that the buried oxide (BOX) layer in a SOI process could be used to reflect about 25 % of the light that would usually be lost to downward radiation back up, thereby increasing the external power efficiency of SOI light sources.

This document elaborates on the technical objectives, approach, chip and process design, physical wafer manufacture, production process control and measurement of the nanometre-scale SOI light sources.

Opsomming

Sleutelwoorde: Elektronstraal litografie, Kwantumbeperking, Nanometer-skaal SOI, Onsuiwerheid herdistribusie, Silikon elektroluminensie, Silikon infrarooi lig uitstraling, Silikon ligbron, SOI begraafde oksied lig refleksie, SOI lig bronne, SOI skyf vervaardiging.

Om kwantumbeperkingseffekte op silikon (Si) ligbron elektroluminensie (EL) eienskappe soos kwantum effektiwiteit, eksterne drywing effektiwiteit and spektrale emissie te ondersoek, is dun Si vinger koppelvlakke met nanometer-skaal dimensies ontwerp en vervaardig in ’n ten volle pasgemaakte silikon-op-isolator (SOI) halfgeleier vervaardigingstegnologie.

Omdat die huidig beskikbare fotolitografie onbruikbaar is om herhaaldelik nanometer-skaal lyn-wydtes akkuraat te definieer, en elektron-straal litografie (ESL) alleen te tydsaam is om hele skywe te belig, moes die vervaardigingsproses van ’n selektiewe kombinasie van fotolitografie en ESL gebruik maak.

Die SOI skywe is vervaardig in die skoonkamers van beide die Carl en Emily Fuchs Instituut vir Mikroëlektronika (CEFIM) by die Universiteit van Pretoria (UP) en die Georgia Instituut van Tegnologie se Microelectronic Research Centre (MiRC), wat ’n JEOL JBX-9300FS elektronstraal patroongenerator (EPG) beskikbaar gemaak het. Sovêr bekend, was hierdie die eerste projek in Suid Afrika (en moontlik by die MiRC) waar ESL gebruik was om werkende nanometer-skaal halfgeleier komponente te vervaardig.

Omdat geen standaardproses gebruik kon word nie, moes die ontwerp en vervaardigingsproses op empiriese toerustingkarakteriseringsdata en materiaaleienskappe gebaseer word.

Die ingewikkelde vervaardiging van die nanometerskaal Si koppelvlakke was ongeëwenaard in die CEFIM en MiRC skoonkamers en het nie net die vervaardigingslimiete van die gebruikte prosesapparat benader nie, maar moes ook ongewenste fisiese effekte wat in grootskaal-halfgeleier vervaardiging normaalweg ignoreer word, oorkom. Die komponentontwerp, maskeruitleg en vervaardigingsproses moes dus verskeie materiaal effekte, toerustingbeperkings en fisiese verskynsels soos onsuiwerheid herdistribusie wat gedurende die fisiese vervaardigingsproses gebeur in ag neem.

Alhoewel die komplekse vervaardigingsproses baie onverwagte probleme geopenbaar het, is verwag dat ten minste die eenvoudige koppelvlak avalanche komponente funksioneel sou wees en data oor kwantumbeperking sou oplewer.

Alhoewel weens ontwerp- en prosesseringsfoute net 29 van die 505 gemete SOI komponente bruikbare ligbronne was, was die ontwerp en vervaardiging van die SOI ligbronne steeds suksesvol in die sin dat genoeg SOI ligbronne beskikbaar was om bruikbare optiese karakteriserings te doen.

Ten spyte daarvan dat die funksionele ligbronne nie die gewenste horisontale beperking bereik het nie, het optiese metings van sekere komponente gewys dat die vertikale kwantumbeperking behaal is.

Al die SOI ligbronne het ’n sterk optiese drywing in die bereik 600 nm < λ < 1 µm gewys. Die SOI ligbron met die hoogste optiese drywing het ongeveer 8 keer meer optiese drywing uitgestraal by λ = 850 nm as ’n 0.35 µm CMOS ligbron by dieselfde stroom. Moontlike redes vir hierdie effek is gegee.

Daar is gewys dat die begraafde oksied (BOX) in ’n SOI proses gebruik kan word om ongeveer 25 % van die lig wat normaalweg deur afwaartse straling verloor word weer na bo te reflekteer en daardeur die eksterne drywingseffektiwiteit van SOI ligbronne te verbeter.

Omdat hierdie eerste iterasie kwantumbeperkte ligbronne belowende resultate gewys het, is ’n volgende ontwikkelingsfase beplan. Resultate van hierdie werk kan aangewend word om selfs dunner SOI ligbronne te vervaardig.

Hierdie dokument beskryf die tegniese doel, benadering, vlokkie- en prosesontwerp, fisiese skyf vervaardiging, produksie proseskontrole en meting van die nanometer-skaal SOI ligbronne.

Acknowledgment

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The experienced support of Mrs. P. Grovè, the clean-room technician at CEFIM, with all processing steps performed in the CEFIM clean-room is also highly appreciated.

LIST OF ABBREVIATIONS

BOE	Buffered Oxide Etch
BOX	Buried Oxide
CEFIM	Carl and Emily Fuchs Institute for Microelectronics
CCD	Charge-Coupled Device
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapour Deposition
DRC	Design Rule Check
EBL	Electron-Beam Lithography
EL	Electroluminescence
EPE	External Power Efficiency
FOX	Field Oxide
GT	Georgia Tech (Georgia Institute of Technology)
HF	Hydrofluoric (Acid)
IC	Integrated Circuit
ICP	Inductively-Coupled Plasma
IPA	Iso-Propanol Alcohol
IR	Infrared
MiRC	Microelectronic Research Centre (at the Georgia Institute of Technology)
NTED	Near-To-Eye Display
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PL	Photoluminescence
PR	Photolithographic Resist
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
SOI	Silicon on Insulator
UV	Ultraviolet

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1. INTRODUCTION

1.1. Problem Statement

Silicon (Si) is by far the most dominantly used semiconductor material with over 97 % utilization in integrated microelectronics [1].

The speed limitation of electrical interconnect is to a first order proportional to the product of conductor resistance and capacitance to ground ([2], pg. 5). The persistent miniaturization trend in modern microelectronic manufacturing processes has the effect of increasing both the resistance of the thinner conductors and the capacitance of the more closely spaced conductors. This has the detrimental effect of decreasing the maximum Si CMOS intra-chip data transmission speed to about 3.5 GHz. The situation is worse for inter-chip data communication where the resistance and capacitance of printed circuit board (PCB) tracks and integrated circuit (IC) package pins are even higher. These fundamental speed limitations are becoming so problematic that other data and clock distribution means are desperately sought.

The practically proven high speed, space saving, noise immune, low power consumption, high capacity and economical advantages of fibre-optic data communication seem to suggest that optical clock and data distribution could also be employed in short-distance inter- and intra-chip applications.

While on-chip Si optical transmission [3], detection and manipulation elements are already practically achievable ([4] and [5]), a suitably efficient on-chip Si light source is not yet available. Although light emission from Si was observed as early as 1955 [6] and its high-speed capability ([7] and [8]) and long-term reliability ([9] - [11]) are established, the major reason for silicon's inherently weak light emission is that it is an indirect band-gap material ([12] and section 2.1.4). While alternative light-sources have been proposed ([4] and [13] - [21]), most require special manufacturing steps that are not easily implemented in the currently prevailing CMOS manufacturing processing technology.

Power efficient silicon-based light sources are also desirable in near-to eye (NTE) displays ([22] and [23]) and in bio-medical lab-on-chip applications [24].

The provision of CMOS-compatible light sources necessitates better understanding of light emission in Si ([25] - [37]) and resultantly improving the power efficiency of Si light sources to practically usable levels with, if possible, no or a minimum of additional manufacturing steps.

The Carl and Emily Fuchs Institute for Microelectronics (CEFIM) at the University of Pretoria (UP) has been developing Si light sources since 1992 ([38] - [46]). Si electroluminescence (EL) improvement research within the INSiAVA project at CEFIM focussed on promising light source configurations that include *inter alia* avalanche, punch-through (see section 2.1.9) and carrier-injection ([38], [39] and subsection 2.2.1.4) Si light sources.

1.2. Quantum Confinement

Enhancement factors of up to 30 in EL due to quantum mechanical confinement in ultra-thin single crystal Si compared to bulk devices were reported in [47] - [50].

References [47] and [48] reported a strong efficiency improvement in forward-biased SOI light-emitting diodes (LEDs) on a buried oxide (BOX) when the thickness of the regions shown in Figure 1.1 was reduced.

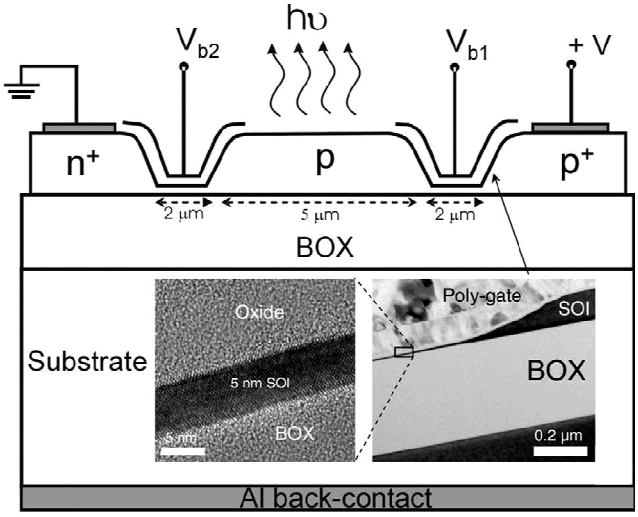


Figure 1.1 Cross-section of the SOI LED manufactured in [47] and [48].

The dramatic increase in integrated EL with reduced device layer thickness (Figure 1.2) is mostly attributed to the suppression of non-radiative recombination.

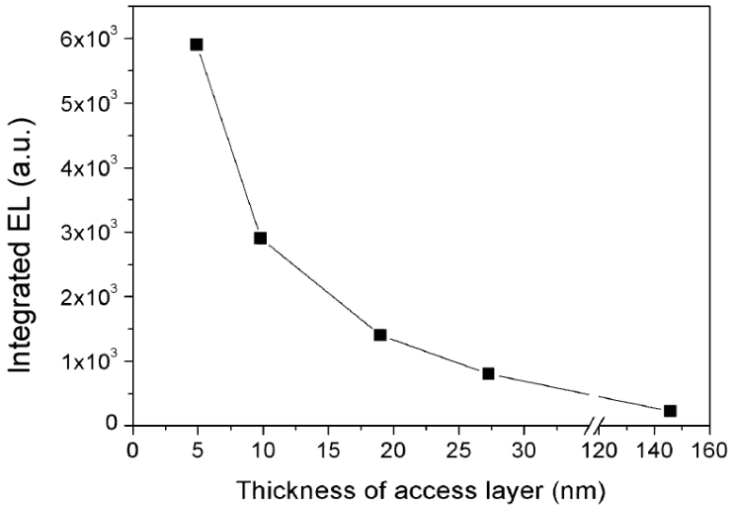


Figure 1.2 Integrated EL intensity against access layer thickness [48].

Abovementioned SOI light sources are only thin in one dimension (1D), their planar thickness, with device widths ranging between 20 and 60 µm. Their *pn*-junctions are also located outside the thinned area.

1.3. Objective

The main purpose of this work was to design and manufacture SOI light sources that would enable the investigation of quantum confinement effects in avalanche, punch-through and carrier-injection Si light sources on EL characteristics like external power efficiency and spectral emission.

Instead of just creating planar thin (1D quantum-confined) devices, the technical objective was to design and manufacture SOI light sources that are smaller in two dimensions, i.e. two-dimensional (2D) quantum-confined SOI light sources.

With reference to the definitions in Figure 1.3, the following finger junction dimensions were aimed at:

$$5\text{ nm} \leq t \leq 100\text{ nm}, \tag{1.1}$$

$$10\text{ nm} \leq w \leq 100\text{ nm and} \tag{1.2}$$

$$200\text{ nm} \leq l \leq 400\text{ nm}. \tag{1.3}$$

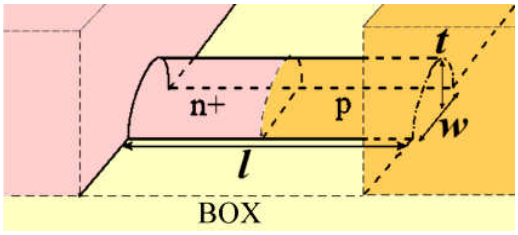


Figure 1.3 Generalized SOI finger junction dimension definitions.

Manufacturing larger rectangular Si structures and selectively oxidizing these created the desired thinner Si fingers.

Nanometre-scale Si wires had already been manufactured through oxidation ([51] - [52]), but *pn*-junctions had, to our knowledge, never been implemented inside such thin Si wires.

Without explaining their functional principles here, the three Si light source types that were selected for silicon-on-insulator (SOI) miniaturization in this research work are:

- Avalanche (n^+p or p^+n junctions),
- Punch-through (n^+pn^+ or p^+np^+ junctions) and
- Carrier-injection light sources.

1.4. Approach

Figure 1.4 displays the approach in terms of an activity flow diagram.

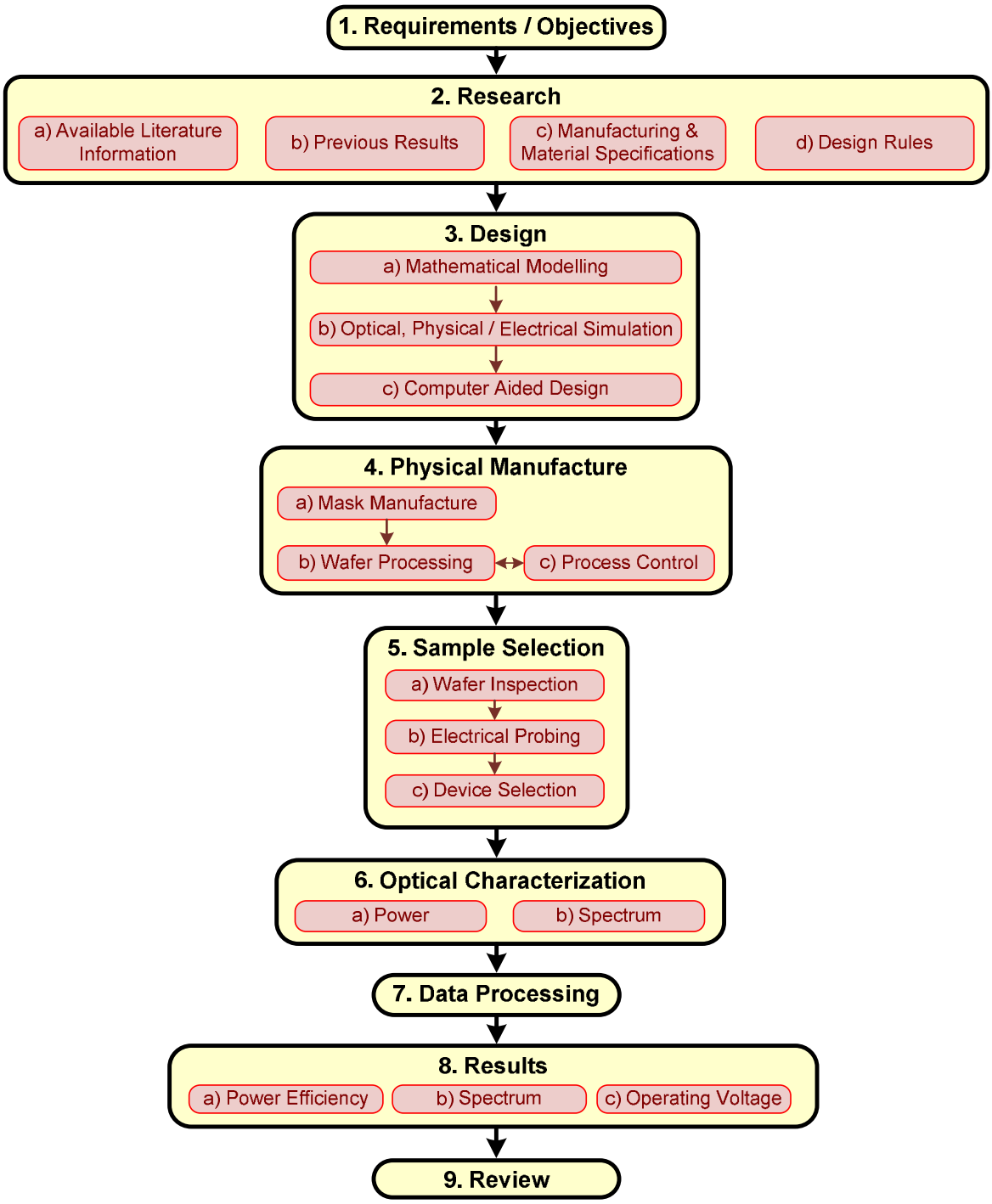


Figure 1.4. Activity flow diagram.

Although this work is mostly concerned with the design and manufacture of the nanometre-scale SOI light sources, some basic electrical and optical measurements were also conducted.

2. SILICON BACKGROUND

Before delving into the design and manufacture aspects of the nanometre-scale SOI light sources, some physical and optical properties of silicon that found application in this works are briefly highlighted in this chapter.

2.1. Semiconductor Properties

To estimate required physical parameters, like semiconductor acceptor and donor doping concentrations N_A and N_D, and resultant material and junction properties, like junction breakdown voltage V_{BD}, resistivity ρ ,sheet resistance R_S and depletion region width w_D, the relations in this section were used.

2.1.1. Resistivity

The relationship between a material's resistivity ρ, its sheet resistance R_S and thickness $\boldsymbol{t}$ can be stated as ([53], pg. 31)

$$\rho = R_S t. \tag{2.1}$$

Figure 2.1 illustrates the relationship between impurity doping concentration and resistivity of doped Si ([53], pg. 32).

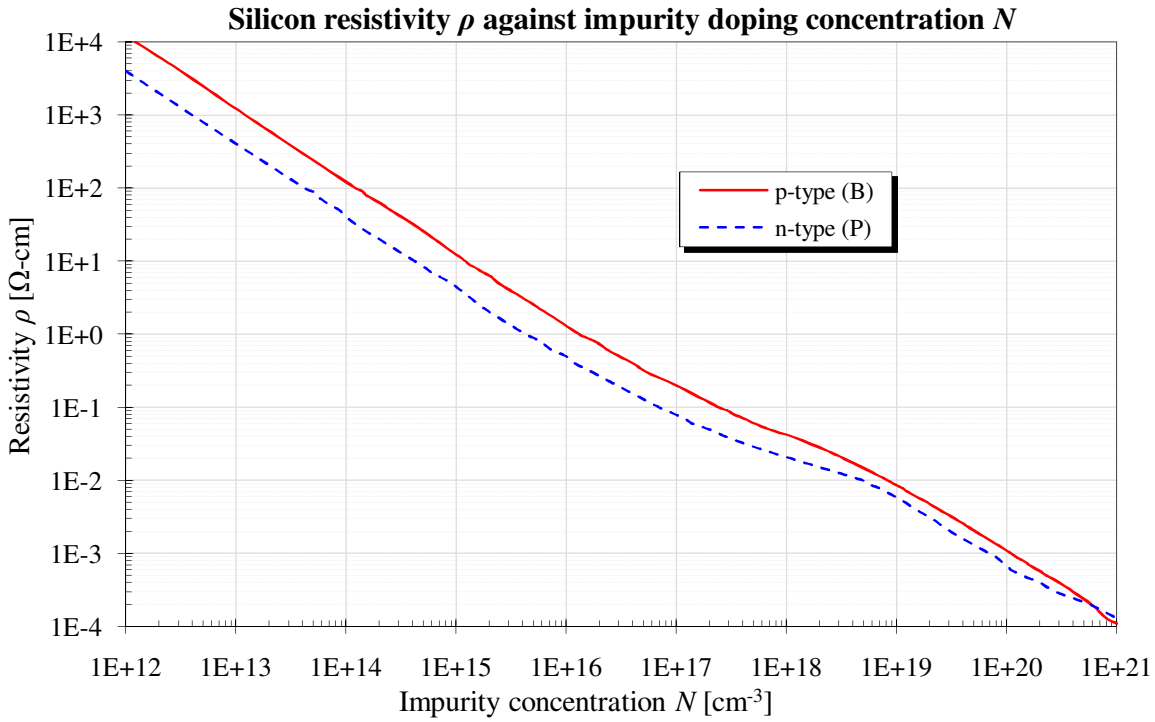


Figure 2.1. Silicon resistivity as a function of impurity doping concentration.

2.1.2. Intrinsic Carrier Concentration

Figure 2.2 shows how silicon's intrinsic carrier concentration n_i increases with impurity doping concentration above about 10^{16} cm^{-3} with respect to the weakly or undoped silicon intrinsic concentration $n_{i0} = 1.45 \cdot 10^{10}$ cm^{-3} at 300 K (physical constants listed in Addendum A).

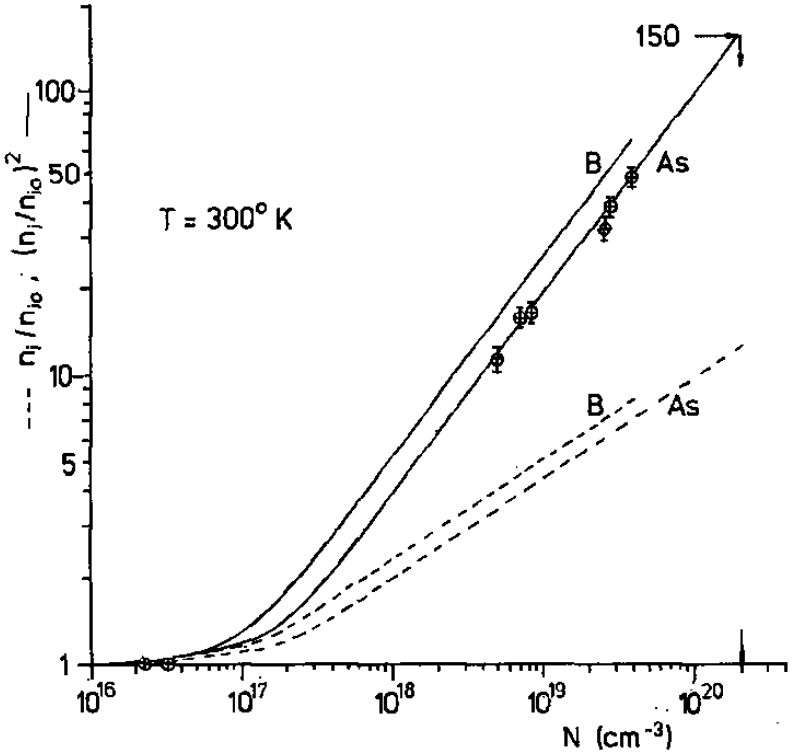


Figure 2.2. Silicon intrinsic concentration n_i variation with doping species and concentration [54].

An empirical expression modelling above band-gap narrowing in a simulation program is given in [55] pg. 347, but assuming that estimated ratios from above plot are sufficient shows that n_i in a n^+ material with Arsenic (As) concentration of 10^{19} cm^{-3} is about $4.1n_{i0} = 5.9 \cdot 10^{10}$ cm^{-3} and $2.3n_{i0} = 3.3 \cdot 10^{10}$ cm^{-3} for a Boron (B) concentration of 10^{18} cm^{-3}.

2.1.3. Junction Built-in Potential

The *pn*-junction built-in potential ψ_{BI} is defined as ([53], pg. 81)

$$\psi_{BI} \approx \frac{k_B T}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right), \tag{2.2}$$

where k_B is Boltzmann's constant, T is the absolute temperature, q is the electron charge, n_i is silicon's intrinsic carrier concentration, N_A and N_D are the acceptor and donor impurity doping concentrations in the p and n-type regions respectively.

For $N_A = 10^{19}$ cm^{-3} and $N_D = 10^{17}$ cm^{-3}, $\psi_{BI} = 875$ mV.

2.1.4. Energy Band Structure

Figure 2.3 displays the energy band structure of an infinitely large ultra-pure perfect Si crystal at 300 K against the three basic wave-vector directions (k = Λ, Γ and Σ) from the centre (Γ) of silicon's first Brillouin zone ([53], pg. 11 – 13).

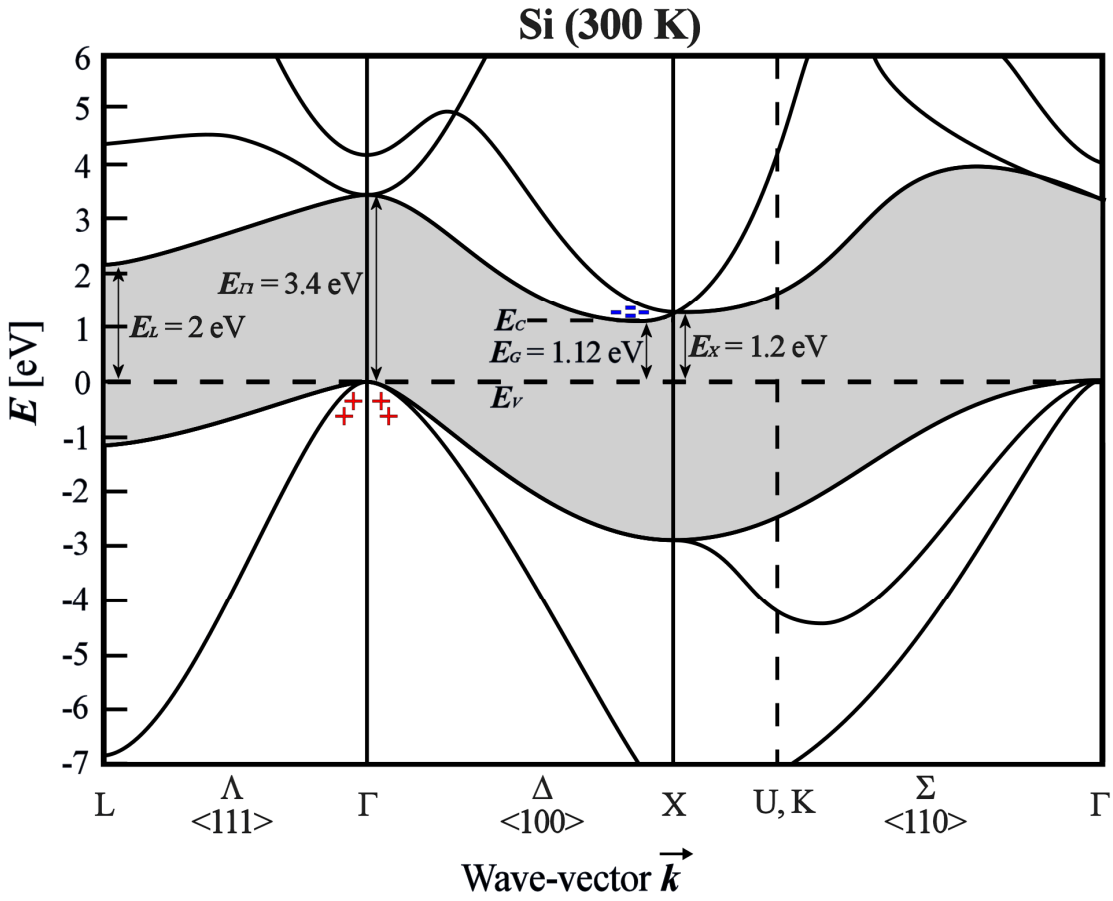


Figure 2.3. Energy band structure of Si at 300 K.

The bands below and above the gray "forbidden" zone are the valence and conduction bands respectively. Only the lowest-energy bands directly bordering on the band-gap are depicted. Although there are many more bands above and below the energy gap, these have almost no effect on the electronic properties of the material.

While electrons and holes can occupy any energy and position in the conduction and valence bands, they cannot remain in the gray "forbidden" zone for any appreciable time. The "-" and "+" symbols denote the locations of electrons and holes in the lowest-energy conduction and valence bands respectively.

The valence band is very similar for most crystalline materials and usually has a maximum at location $k = \Gamma$ (= 0), the centre of the Brillouin zone ([56], pg. 3). The maximum valence band energy is indicated with E_V (and is in this case set to E = 0 eV). The lowest conduction band energy occurs close to k = X and is identified by E_C.

The energy band-gap E_G is the energy difference between the valence and conduction bands. E_G = 1.12 eV for pure Si at 300 K. This is the minimum energy associated with an electron-hole generation or recombination across the forbidden energy gap. Since silicon's lowest conduction-band energy valley and the highest valence peak do not coincide at the same wave-vector position within the Si crystal, Si, in contrast to GaAs, is an indirect band-gap material.

The energy band diagram in Figure 2.3 is only valid for an infinitely large, pure and perfect Si crystal at 300 K. Reducing the dimensions of the crystal, varying the temperature and the presence of impurities and crystal defects will alter the position and shape of the energy bands. All of these factors can therefore change the energy band-gap. This work attempts to increase the light emission efficiency of a Si light emitter by reducing the device dimensions, which should increase the band-gap energy and the wave-vector difference associated with it ([15], pg. 6, [16], pg. 629, [20], pg. 32, [21], pg. 29, [27], pg. 1044, [48], pg. 85 and [57], pg. 2).

2.1.5. Impact Ionization

In a sufficiently high electric field, a carrier can gain energy higher than the band-gap and excite additional electron-hole pairs through impact ionization. This carrier multiplication process is characterized by the ionization rate α that is defined by the number of electron-hole pairs generated by a primary electron (hole) carrier with velocity v_n (v_p) per unit distance travelled ([53], pg. 37)

$$\alpha_n = \frac{1}{nv_n}\frac{\mathrm{d}n}{\mathrm{d}t} \text{ and} \tag{2.3}$$

$$\alpha_p = \frac{1}{nv_p}\frac{\mathrm{d}p}{\mathrm{d}t}, \tag{2.4}$$

which lets the carrier density or current variation with distance x be expressed as

$$\frac{\mathrm{d}J_n}{\mathrm{d}x} = -\frac{\mathrm{d}J_p}{\mathrm{d}x} = \alpha_n J_n + \alpha_p J_p, \tag{2.5}$$

where the total current $J = J_n + J_p$ is constant at any position x.

The electron and hole ionization rates are highly dependent on the electric field and can be expressed in the form [53]

$$\alpha(\mathscr{E}) = \frac{q\,\mathscr{E}}{E_I} e^{\frac{-\mathscr{E}_I}{\mathscr{E}\left(1+\frac{\mathscr{E}}{\mathscr{E}_P}\right)+\mathscr{E}_T}}, \tag{2.6}$$

where E_I is the high-field effective ionization threshold energy and is typically 3.6 eV for electrons and 5.0 eV for holes for Si. $\mathscr{E}_T$, $\mathscr{E}_P$ and $\mathscr{E}_I$ are thermal, phonon-optical and ionization threshold fields respectively.

Figure 2.4 shows that the ionization rate of electrons is always higher than that of holes.

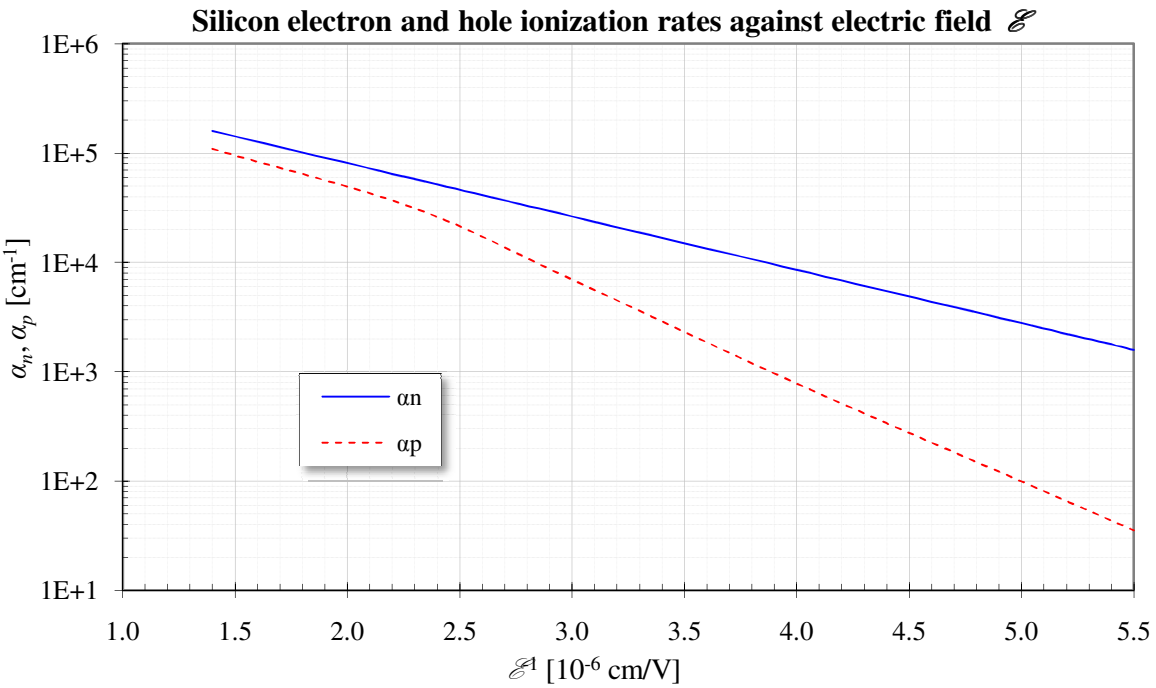


Figure 2.4. Silicon electron and hole ionization rates against electric field.

2.1.6. Critical Electric Field

As Figure 2.5 shows, the critical electric field $\mathscr{E}_C$ of an abrupt Si junction at breakdown can be expressed in terms of background doping concentration N [cm^{-3}] by ([53], pg. 107)

$$\mathscr{E}_C = \frac{4 \cdot 10^5 \text{ V/cm}}{1 - \frac{1}{3}\log_{10}\left(\frac{N}{10^{16} \text{ cm}^{-3}}\right)}. \tag{2.7}$$

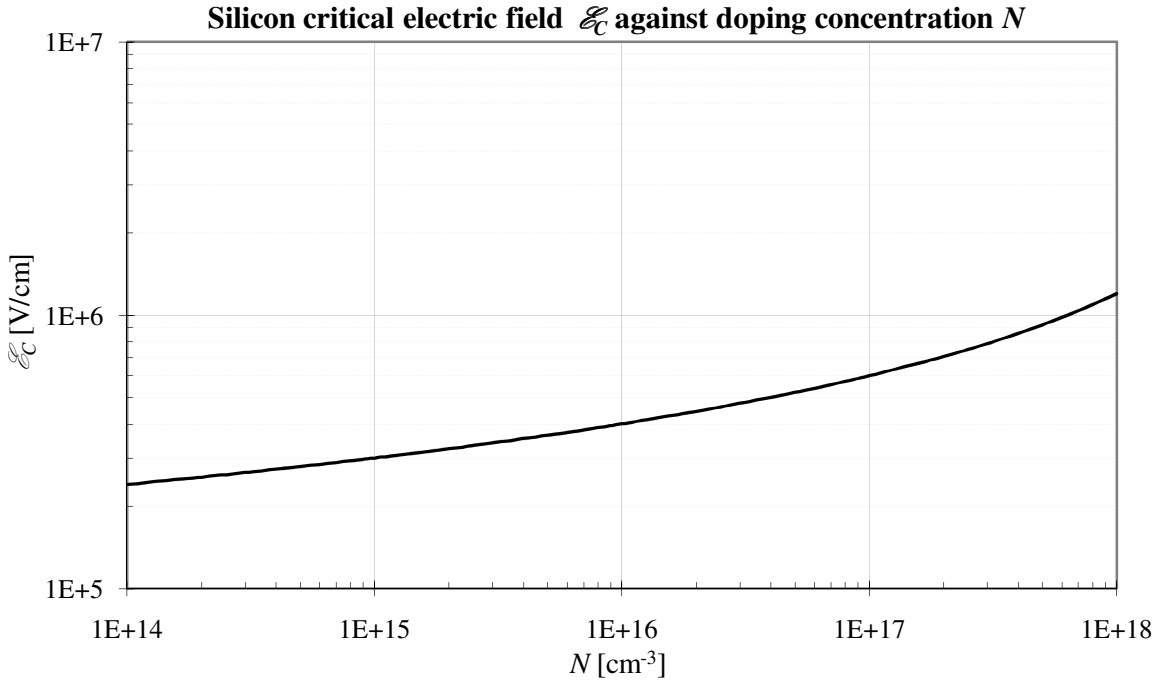


Figure 2.5. Si critical electric field $\mathscr{E}_C$ against background doping N.

For a background doping $N = 10^{17}$ cm^{-3} the critical electric field $\mathscr{E}_C \approx 6 \cdot 10^5$ V/cm.

2.1.7. Avalanche Breakdown

The planar avalanche breakdown voltage of an abrupt junction is expressible in terms of background doping concentration N and silicon's critical electric field $\mathscr{E}_C$ by

$$V_{BD} \cong \frac{\varepsilon_{Si}\mathscr{E}_C^{\,2}}{2qN} - \psi_{BI}, \tag{2.8}$$

where silicon's dielectric constant $\varepsilon_{Si} = \varepsilon_0\varepsilon_{rSi}$ (Addendum A).

Above equation is plotted in Figure 2.6, but also indicates that (2.8) is only valid for impurity concentrations to the left of the stippled line. For higher concentrations, quantum mechanical tunnelling (Zener breakdown) will contribute and later dominate the breakdown mechanism.

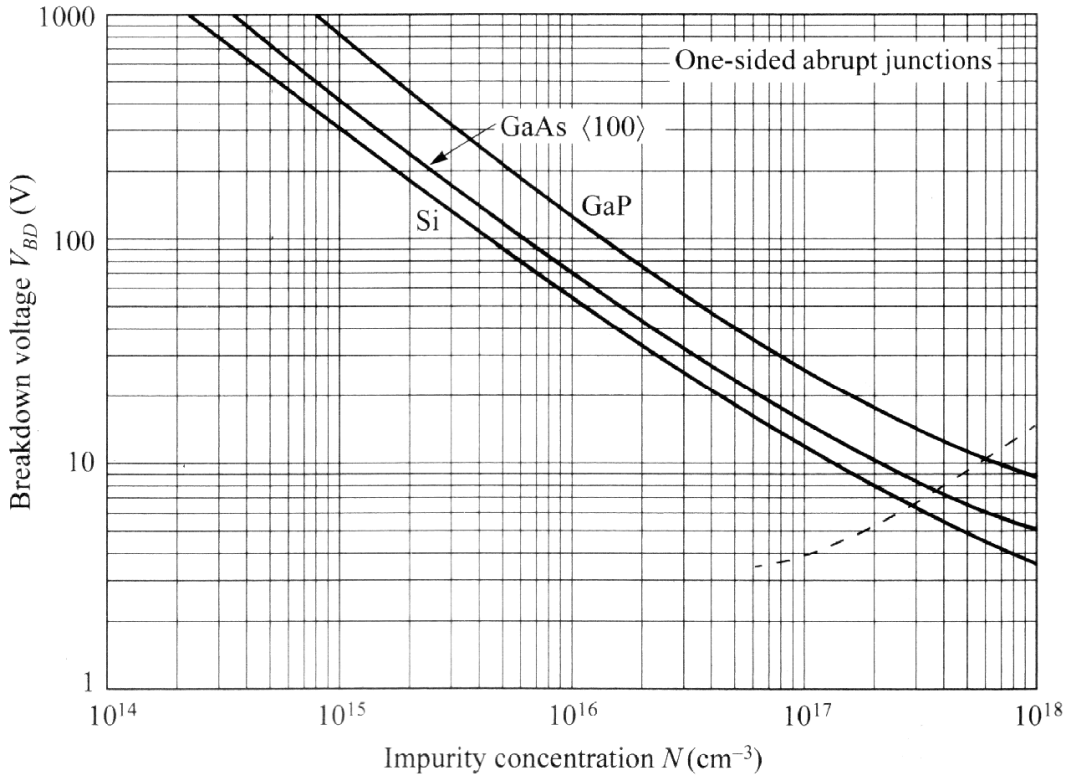


Figure 2.6. Planar breakdown voltage V_{BD} against impurity doping concentration N ([53], pg. 108).

Since tunnelling is not yet dominant at $N = 10^{17}$ cm^{-3}, the planar breakdown voltage of a *pn*-junction with $N_A = 10^{19}$ cm^{-3} and $N_D = 10^{17}$ cm^{-3} is approximately $V_{BD} \approx 11$ V.

2.1.8. Depletion Region Width

The depletion region width w_d of a *pn*-junction can be expressed as ([53], pg. 83)

$$w_d = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\left(\psi_{BI} - 2\frac{k_B T}{q} - V_D\right)}, \tag{2.9}$$

where V_D is the voltage applied across the junction and is positive for forward bias.

For a junction with N_A = 10^{19} cm^{-3} and N_D = 10^{17} cm^{-3} biased at V_D = 0 V the thermal equilibrium depletion region width w_D = 104 nm.

As Figure 2.7 confirms, the same junction at breakdown (V_D = -V_{BD} = -11 V) has a depletion region width w_D = 389 nm.

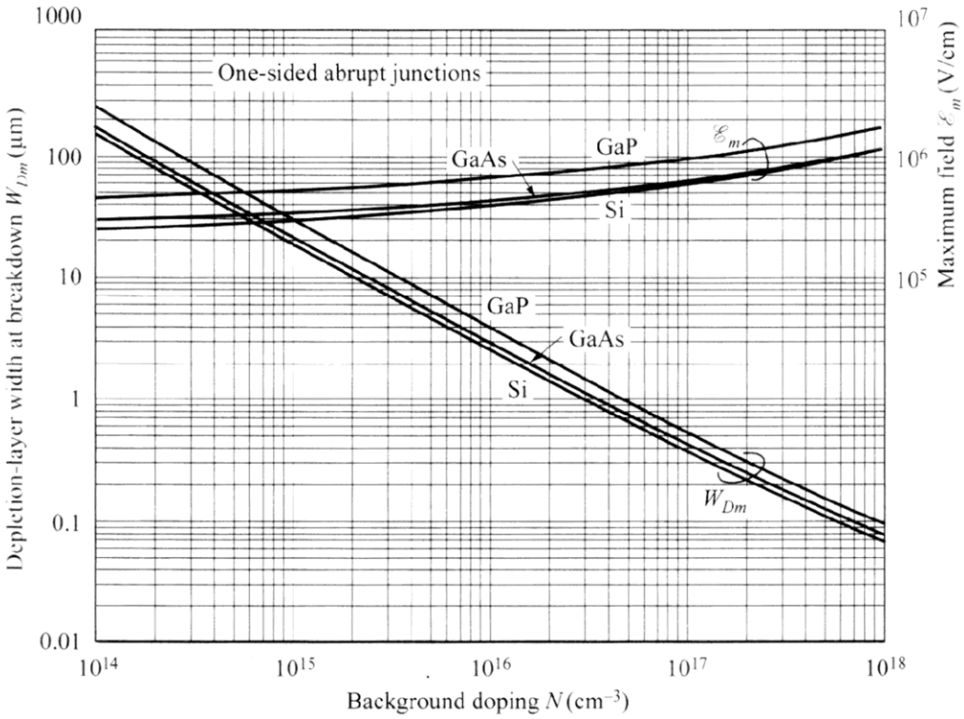


Figure 2.7. Breakdown depletion width and critical field against background doping [53].

The depletion region extensions x_n and x_p into the *n*- and *p*-doped sides of a junction respectively depend on the impurity doping concentrations on both sides as ([58], pg. 41)

$$x_n = w_d \frac{N_A}{N_A + N_D} \text{ and} \tag{2.10}$$

$$x_p = w_d \frac{N_D}{N_A + N_D}. \tag{2.11}$$

For $N_A = 10^{19}$ cm^{-3} and $N_D = 10^{17}$ cm^{-3} $x_n = 103$ nm and $x_p = 1.03$ nm at $V_D = 0$ V and $x_n = 385$ nm and $x_p = 3.85$ nm at breakdown ($V_D = -V_{BD}$). As expected from the fact that $N_A = 100N_D$, $x_n = 100x_p$.

2.1.9. Punch-through

Figure 2.8 shows two heavily doped p^+ end regions with equal acceptor concentration N_A spaced a distance W_P apart by a lower doped n-type drift region with donor concentration N_D.

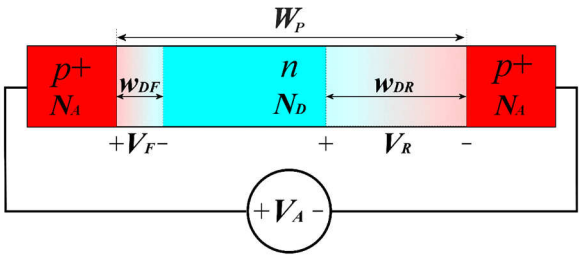


Figure 2.8. Punch-through voltage variable definitions.

Applying a voltage V_A across the two back-to-back diodes has the effect of forward biasing the left junction and reverse biasing the right junction. From equation (2.9) the depletion region widths of both junctions can be expressed as

$$w_{DF} = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\left(\psi_{BI} - 2\frac{k_B T}{q} - V_F\right)} \text{ and} \tag{2.12}$$

$$w_{DR} = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\left(\psi_{BI} - 2\frac{k_B T}{q} + V_R\right)}, \tag{2.13}$$

where the sum of the voltages across the forward and reverse biased junction, V_F and V_R respectively, equals the applied voltage V_A.

Under the condition that the reverse biased junction does not experience avalanche breakdown, the applied voltage V_A can be increased to the point where the expanding reverse biased depletion region reaches the forward biased depletion region. The applied voltage V_A at which $w_{DF} + w_{DR} = W_P$ is defined as the punch-through voltage

$$V_{PT} = \frac{qW_P^2}{2\varepsilon_{Si}}\left(\frac{N_A N_D}{N_A + N_D}\right) - W_P\sqrt{\frac{2q}{\varepsilon_{Si}}\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\psi_{BI} - 2\frac{k_B T}{q} - V_F\right)} \tag{2.14}$$

$$\approx \frac{qW_P^2}{2\varepsilon_{Si}}\left(\frac{N_A N_D}{N_A + N_D}\right) - W_P\sqrt{\frac{2q}{\varepsilon_{Si}}\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\psi_{BI} - 2\frac{k_B T}{q}\right)}. \tag{2.15}$$

Approximation (2.15) is not very accurate though as substitution for a n^+pn^+ punch-through structure with $N_A = 10^{19}$ cm^{-3}, $N_D = 10^{17}$ cm^{-3}, $W_P = 400$ nm and assumed $V_F = 0.7$ V shows: equation (2.15) renders a punch-through voltage $V_{PT} \approx 6$ V, which is almost half the punch-through voltage $V_{PT} \approx 10$ V predicted by equation (2.14).

Figure 2.9 shows the energy band diagrams of the p^+np^+ punch-through device for different biasing voltages: a) no applied bias ($V_A = 0$V), b) 0 V < V_A < V_{PT} and c) $V_A = V_{PT}$.

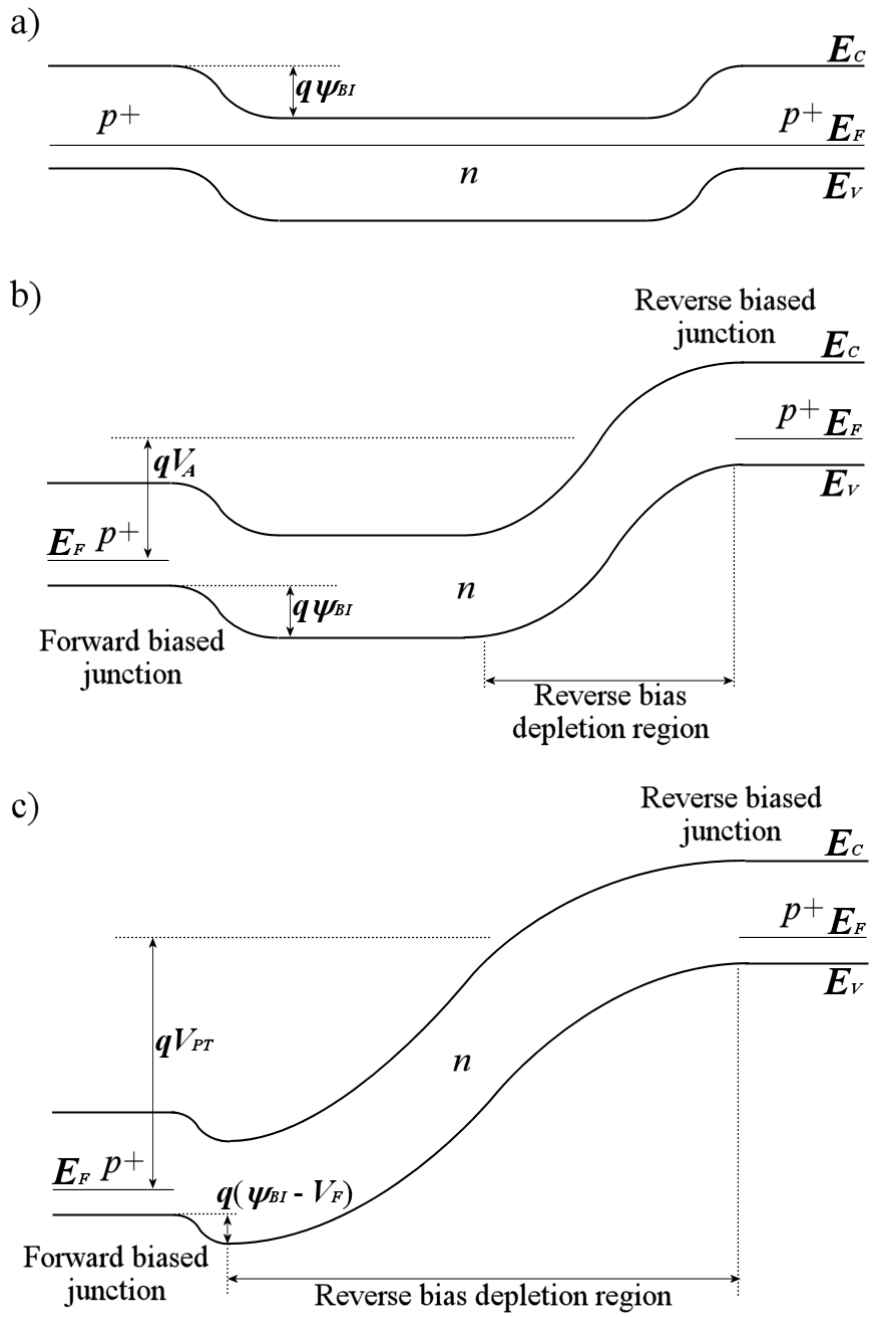


Figure 2.9. Energy-bands of the p^+np^+ junctions at a) $V_A = 0$ V, b) 0 V < V_A < V_{PT} and c) $V_A = V_{PT}$.

It is evident that when the reverse-bias depletion region reaches the forward-biased junction at $V_A = V_{PT}$, that it lowers the energy barrier at the forward-biased junction, which then injects a larger thermionic emission hole current.

Figure 2.10 shows the electron (n_{xy}) and hole (p_{xy}) carrier distributions in the p^+np^+ device for a) 0V < V_A < V_{PT} and b) $V_A = V_{PT}$.

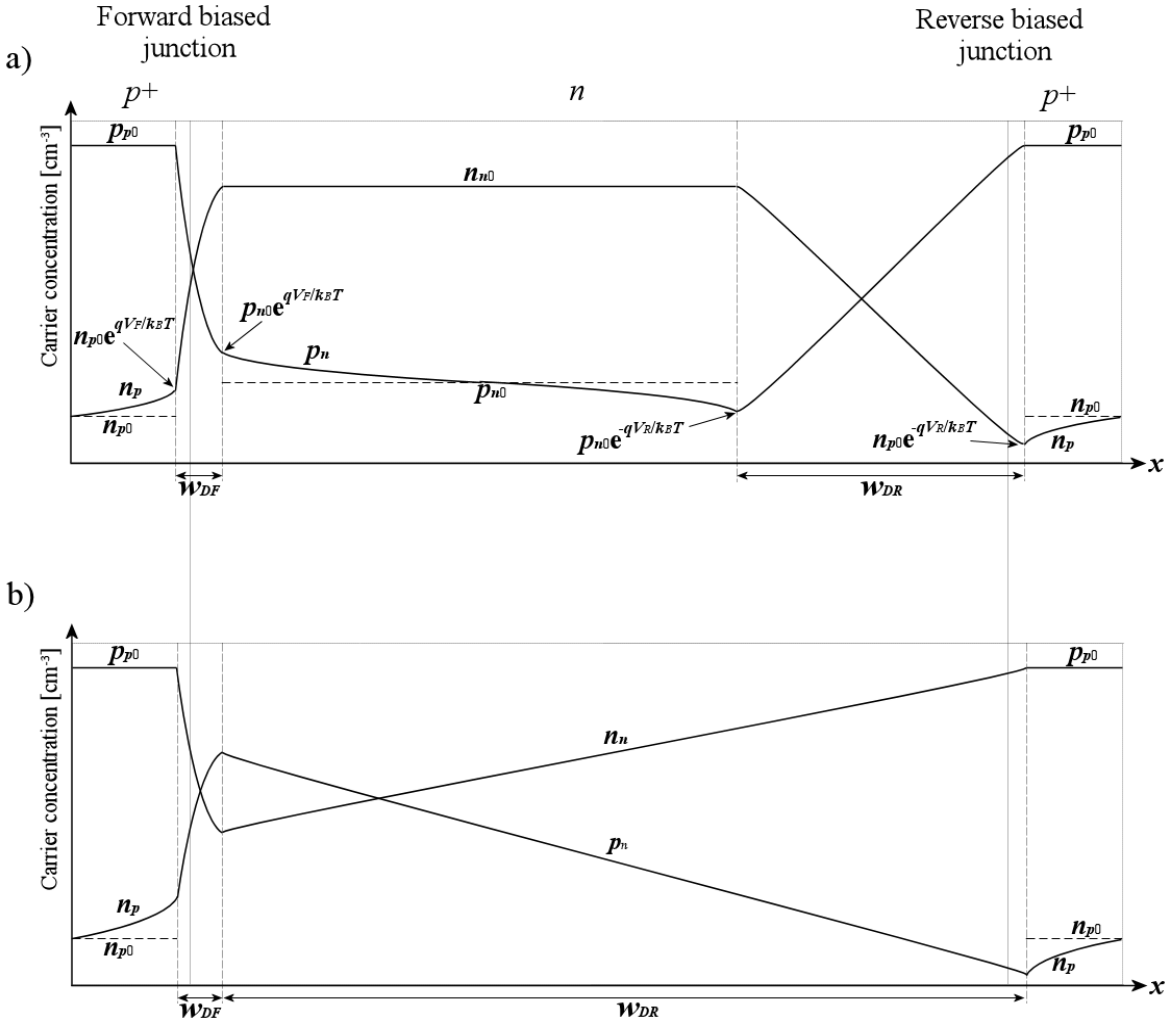


Figure 2.10. Back-to-back p^+np^+ junction carrier distribution for a) 0 V < V_A < V_{PT} and b) $V_A = V_{PT}$.

The barrier-lowering effect of the reverse-bias depletion region punching-through to the forward-biased junction has the effect of increasing the hole injection (p_n) into the intermediate *n*-type drift region. This makes more minority carriers in the reverse-bias depletion region available for avalanche multiplication and radiative recombination.

Since the radiative recombination rate is proportional to the *pn*-product {see equation (2.20)} a higher minority carrier concentration in the drift region will increase the probability of radiative recombination. The wider spread of high carrier concentrations in the intermediate *n*-region in Figure 2.10 b) also means the *pn*-product is larger for a wider region within the reverse biased depletion region, which also increases the probability of radiative recombination.

The fact that higher avalanche currents are achievable at lower terminal voltages also implies that the power efficiency of a punch-through light source is higher than the power efficiency of a single avalanching *pn*-junction.

Figure 2.11 shows the electric field distribution of the back-to-back diodes of Figure 2.8 at punch-through.

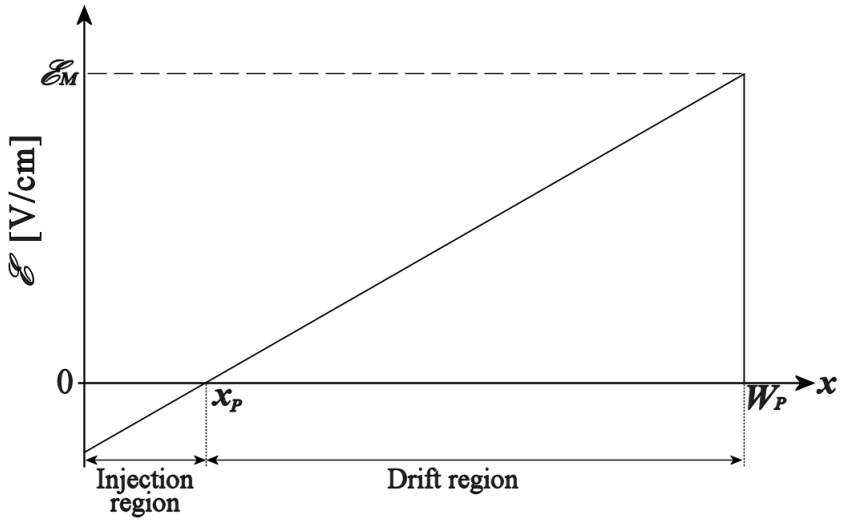


Figure 2.11. Electric field distribution in the punch-through device.

The linear electric field $\mathscr{E}$ is zero at $x = x_P$ (the point where the reverse-biased depletion region touches the forward-bias depletion region) and achieves its maximum field strength $\mathscr{E}_M$ at $x = W_P$ at the reverse biased junction. Since Figure 2.4 showed that the carrier ionization rates increase with electric field strength, it is expected that radiative recombination will predominantly occur in the depletion region close to the reverse biased junction at W_P.

This section illustrated the punch-through effect with a p^+np^+ device, but the higher impact ionization constant of electrons compared to holes (section 2.1.5) suggests that an n^+pn^+ punch-through light source would have a higher optical power efficiency than an equivalent p^+np^+ device.

2.1.10. Reach-through

While the punch-through device can increase radiative recombination by injecting additional minority carriers into the reverse-bias depletion region, its electric field decreases linearly from its maximum $\mathscr{E} = \mathscr{E}_M$ at $x = W_P$ to zero at x_P (Figure 2.11). Replacing the left p^+ diffusion of the forward-biased punch-through device junction in Figure 2.8 with an n^+ creates a reach-through device that does not feature carrier injection, but its electric field strength changes more gradually in the lower-doped drift region.

Figure 2.12 depicts that the trapezoidal electric field in the W_R–wide n^- drift region between the n^+ and p^+ end regions in a reach-through device is close to the maximum electric field $\mathscr{E}_M$ existing at the reverse biased junction and drops off sharply in the heavily doped n^+ end region([59], pg. 101).

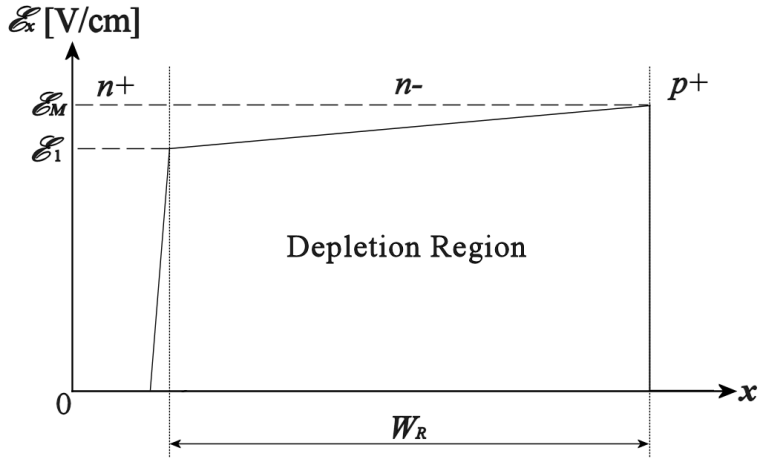


Figure 2.12. Electric field distribution in a reach-through device.

The high electric field throughout the entire drift region causes a larger number of high-energy ("hot") carriers, a higher carrier ionization rates, more carrier multiplication, higher probability of radiative recombination and resultantly a higher Si light source efficiency. The high electric field throughout the depletion region also causes the carriers to travel at their saturated velocity, which gives the device a fast switching speed compared to conventional *pn*-junctions in avalanche.

The electric field E_1 at the interface between the n^- drift and n^+ end region depends on the maximum electric field $\mathscr{E}_M$ and n^- drift region doping concentration N_{DR} through

$$\mathscr{E}_1 = \mathscr{E}_M - \frac{qN_{DR}}{\varepsilon_{Si}} W_R . \tag{2.16}$$

Neglecting the small voltage drop in the n^+ end region allows stating the voltage across the reach-through device as

$$V_{RT} \cong \left(\frac{\mathscr{E}_M + \mathscr{E}_1}{2} \right) W_R . \tag{2.17}$$

Avalanche breakdown will occur when the maximum electric field $\mathscr{E}_M$ is equal to the critical electric field $\mathscr{E}_C$.

Combining (2.16) and (2.17) and substituting $\mathscr{E}_M = \mathscr{E}_C$ renders the reach-through breakdown voltage as

$$V_{BD\_RT} \cong \mathscr{E}_C W_R - \frac{qN_{DR}W_P^{\,2}}{2\varepsilon_{Si}} . \tag{2.18}$$

With $N_{DR} = 10^{17}$ cm^{-3} and $W_R = 400$ nm $V_{BD\_RT} \approx 12$ V.

2.2. Optical Properties

This section briefly explores some important optical properties of Si and its associated processing materials and steps that were used in this work. This includes defining integrated light source efficiency (subsection 2.2.1.2), presenting the average power spectrum of typical CMOS light sources (subsection 2.2.1.3), quantifying refractive indices and extinction coefficients of Si, silicon dioxide (SiO_2) and silicon nitride (Si_xN_y or Si_3N_4) in subsection 2.2.2, photon absorption within Si (subsection 2.2.3.1) and optical transmission through the SiO_2 and Si_xN_y layers covering ICs (subsection 2.2.3.2),.

2.2.1. Electroluminescence

2.2.1.1. Radiative Recombination

Avalanche electroluminescence in semiconductors is mostly caused by radiative recombination of mobile electrons and holes. Two types of radiative recombination can occur: direct (band-to-band) radiative recombination and radiative band-to-impurity recombination ([60], pg. 161).

Figure 2.3 on pg. 8 showed that silicon, in contrast to GaAs, has its minimum conduction band energy not at the same waver vector as its maximum valence energy at Γ, which makes it an indirect band-gap semiconductor. Since electron-hole radiative recombination requires that momentum be conserved, this means that a phonon with equal but opposite momentum to the electron's initial state in the conduction. Such a two-step process has a lower occurrence probability compared to direct recombination, which makes Si an inefficient light emitter ([56], pg. 3).

Since the photon energy $\hbar\omega$ emitted during radiative recombination is equal or slightly larger than the recombination energy gap E_G, the recombination path(s) can be estimated from the wavelength (spectrum) of the generated light through

$$E_G \cong \hbar\omega. \tag{2.19}$$

Since both electrons and holes are necessary for band-to-band recombination, the radiative recombination rate R_{BTB} is proportional to the *np*-product

$$R_{BTB} \propto np - n_i^2. \tag{2.20}$$

Similarly, the band-to-impurity radiative recombination rate R_{BTI} is proportional to the product of the electron-hole pair concentration N_P and the concentration of impurities N_I involved in the radiative recombination process through

$$R_{BTI} \propto N_P N_I. \tag{2.21}$$

2.2.1.2. Integrated Light Source Efficiency

Two types of integrated light source efficiencies can be considered: the quantum conversion efficiency and the external power efficiency.

2.2.1.2.1 Quantum Conversion Efficiency

The quantum-conversion efficiency η of a light source is defined by the ratio

$$\eta = \frac{\text{average number of photons emitted per unit time}}{\text{average number of electrons passing through source per unit time}}. \tag{2.22}$$

Generally, two types of quantum efficiency definitions are used. While the internal quantum-conversion efficiency η_i relates the emitted photons to electrons right at the light generation site, the external quantum efficiency η_e uses the externally available photon count that incorporates optical losses (for example surface reflection and media absorption) associated with the environment between source and region where the light is used.

Although the quantum efficiency of a source is a valid performance criterion parameter, it is not very practical in physical implementations.

2.2.1.2.2 External Power Efficiency

The external power efficiency *EPE* of an integrated light source is defined as the ratio of the externally available optical power $P_{Optical\_Out}$ to the electric power $P_{Electrical\_In}$ invested to generate the light

$$EPE = \frac{P_{Optical\_Out}}{P_{Electrical\_In}}. \tag{2.23}$$

Since the external power efficiency relates how many Watt of electrical power are necessary to generate a specific Wattage of optical power it is much more useful comparison figure in practical applications, where a certain optical power is desired for a minimum of electrical power needed to generate the light.

2.2.1.3. CMOS Light Source

Figure 2.13 illustrates that the shallow n^+ in p-well and p^+ in n-well junctions in the standard CMOS process mainly constitute horizontal diodes; i.e. most of the pn-interface is oriented in the horizontal plane, with most of the depletion region (indicated by dotted lines) extending into the underlying lighter doped material under applied reverse bias.

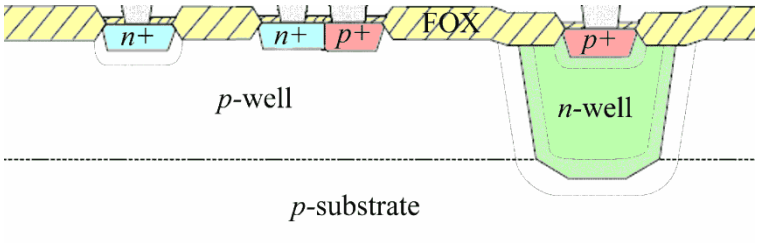


Figure 2.13. Cross-sectional view of the three typical CMOS pn-junction diode types.

The typical CMOS light source employs either the n^+ in p-well or p^+ in n-well junctions in avalanche. Depending on the electric field distribution, the light generation site is usually located along one sidewall of either junction.

Figure 2.14 depicts average measured optical power spectra of 0.35 µm CMOS light sources operating at a current of 650 µA when the light source is placed directly in front of a spectrometer's fibre-optical receptor and the spectrometer's response (see Addendum B) is taken into account.

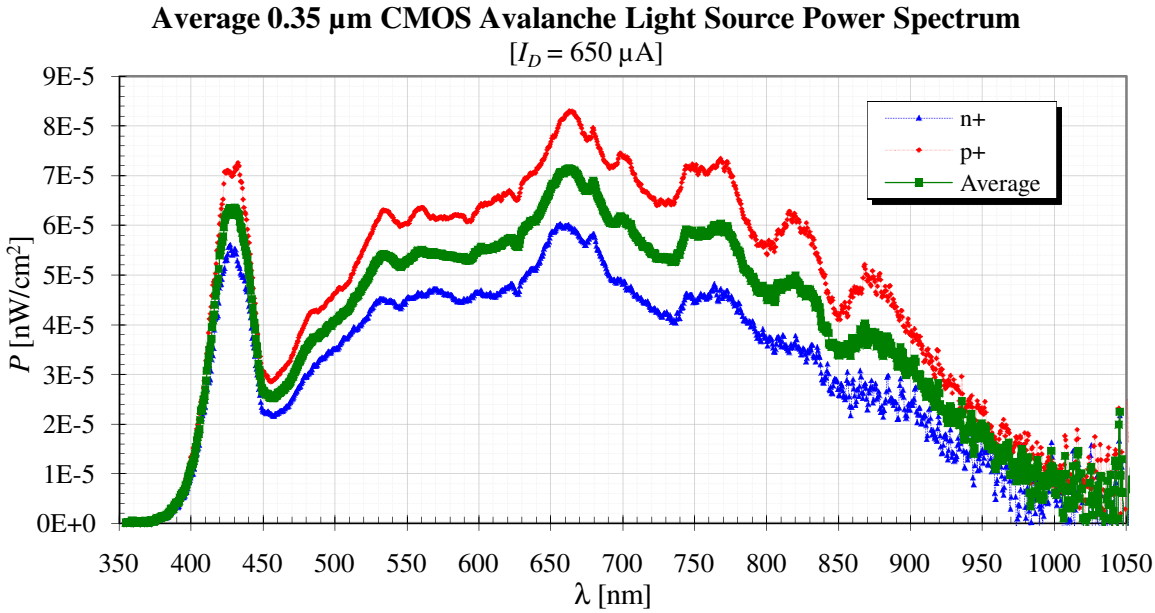


Figure 2.14. Average 0.35 µm CMOS avalanche light source power spectrum (I_D = 650 µA).

The silicon light source spectrum in above figure indicates that the silicon light source has its maximum optical power emission around 660 nm, which is in the visible region.

It should be kept in mind that above power spectral density plot still incorporates absorption from the bulk silicon depth from which the light originates and transmission losses from the silicon dioxide and nitride layers covering the chip, both of which introduce attenuation of the shorter wavelengths. Furthermore, the optical acceptance angle of the spectrometer only captures a small solid angle of the complete optical radiation pattern.

The light emission power spectrum of a thin Si wire junction is expected to not only be much stronger, but should also be much more pronounced for shorter wavelengths.

2.2.1.4. Carrier Injection

du Plessis *et al* ([38] and [39]) found that the quantum conversion efficiency of Si electroluminescence can be improved by injecting "cool" (low energy) carriers from a forward-biased junction into the high electric field existing in the depletion region of a reverse-biased junction so that they can recombine with "hot" (high energy) carriers. In contrast to a simple *pn*-junction in which the avalanche-multiplied minority carriers are due to the leakage current thermally generated in the drift region, the carrier injection technique improves the optical power efficiency of an integrated light source by making more carriers available to avalanche multiplication at the same reverse bias.

Such a Si light source is achievable by placing a forward-biased injecting junction in close proximity of an avalanching reverse-biased junction. The resultant Si light source can have two or three terminals. In the three-terminal configuration, the third connection to the lower-doped drift region that contains the reverse-bias depletion region allows separate manipulation of the forward- and reverse-biased junction currents. In the two-terminal configuration, the intermediate drift region remains floating and the forward and reverse biased junctions are forced to have the same current. Bulk CMOS injection light sources have the disadvantage that it is quite difficult to direct all of the injected carriers into the avalanching depletion region. The forward-biased junction injection can be illustrated with an analogy to an overflowing dam with equal dam wall height all around it: the water would spill equally in all directions. This unidirectional carrier injection into the bulk of the forward-biased junction has the effect that only a relatively small fraction of the "cool" carriers reaches the depletion region – the rest is lost in the bulk, but because it still contributes to the forward current, it decreases the power efficiency of the light source.

One way of increasing the electroluminescent efficiency is to ensure that all injected carriers enter the depletion region by implementing the two junctions next to each other in a Si wire surrounded by an insulator. The SOI manufacturing technology is a perfect candidate for realizing such devices as it provides a thin Si layer on top of a thick SiO_2 layer. Etching the superfluous Si away on adjacent sides of the junctions would leave a Si channel that constricts the carrier movement in it. The overflowing water analogy would entail having the dam surrounded by mountains except for one spill-way channel that the water is forced to flow through.

Another way of ensuring that most of the injected carriers reach the depletion region is to employ the punch-through effect introduced in section 2.1.9 (pg. 14). As the reverse-bias depletion region reaches the forward biased junction, it only decreases the barrier energy at that location so that most of the cool carriers enter directly into the encroaching depletion region. Depending on the degree of barrier lowering, some carriers can still be thermally injected over the higher barrier at other locations. The water analogy would employ a dam with a depression in its otherwise equal-height dam wall surrounding it. Most of the water would flow out at this lower barrier, although, depending on the depth of the localized dam wall depression, the wind could still spill some water over the higher dam wall at other places. By reverse biasing the injector-junction slightly with respect to the bulk, the thermally excited component can be suppressed so that only the localized punch-through region is forward biased and injecting cool carriers into the touching reverse-bias depletion region.

An example of an injection-enhanced Si light source would be the punch-through device. Manufacturing this device in an SOI technology with a drift region doping level selected in such a way that the reverse-biased depletion region touches the forward biased junction (enabling carrier injection) while at the same time exhibiting avalanche breakdown should render a Si light source with improved quantum conversion efficiency.

2.2.2. Refractive Indices and Extinction Coefficients

2.2.2.1. Silicon

Figure 2.15 plots silicon's refractive index and extinction coefficient against wavelength.

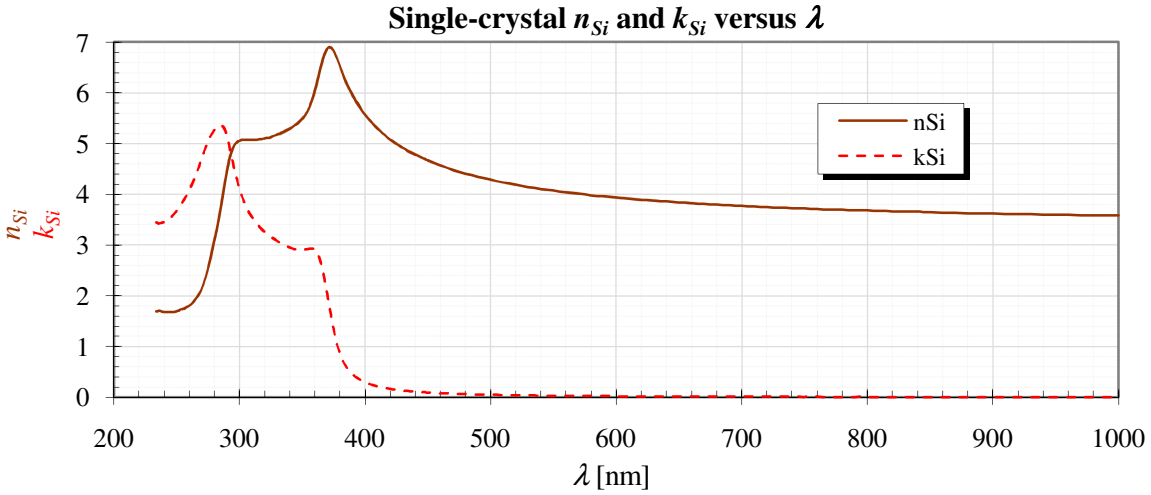


Figure 2.15. Single-crystal silicon refractive index n_{Si} and extinction coefficient k_{Si} ([61] - [63]).

A material's extinction coefficient k is relatable to the material's optical absorption coefficient α (see subsection 2.2.3.1) through

$$k = \frac{\alpha\lambda}{4\pi}. \tag{2.24}$$

Due to the strong gradient variation of silicon's refractive index and extinction coefficient between 286 nm and 372 nm, curve-fitting is easier when both are plotted against the photon energy E_{Ph} ($\approx$ 1.24 [eV/nm]/λ) as shown in Figure 2.16.

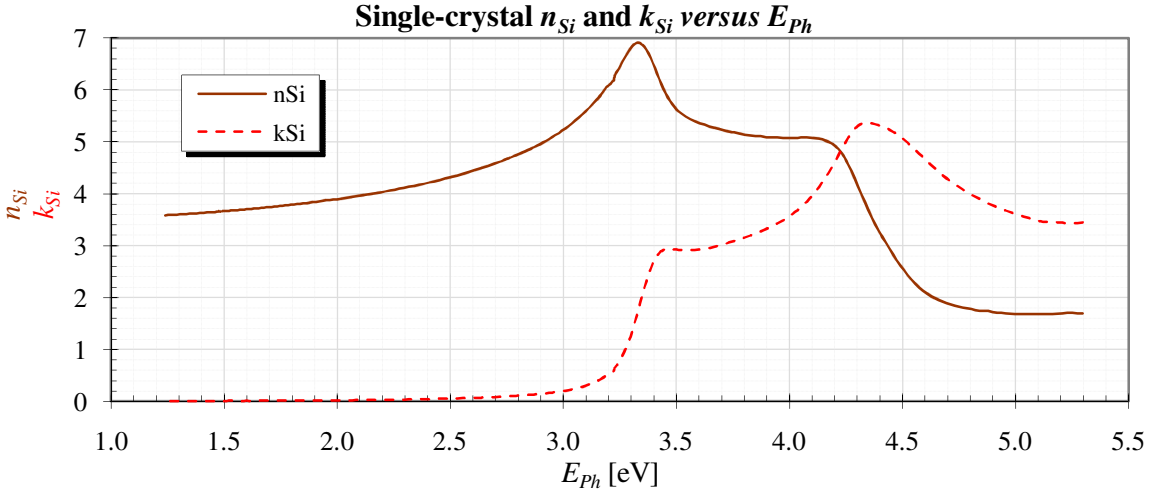


Figure 2.16. Silicon refractive index n_{Si} and extinction coefficient k_{Si} against photon energy E_{Ph}.

Jellison *et al* [62] propose that the silicon index of refraction n_{Si} below the direct band edge, $E_{Ph} < 3.33$ eV (372 nm < λ), can be represented by

$$n_{Si}(E_{Ph},T) = \sqrt{4.386 - 0.00343T + \frac{99.14 + 0.062T}{E_G{}^2 - E_{Ph}{}^2}}, \tag{2.25}$$

where T is the temperature in ºC and the fitted energy gap $E_G = 3.652$ eV.

For the region above the direct band edge, 3.33 eV < E_{Ph} < 4.33 eV (286 nm ≤ λ < 372 nm), Figure 2.17 shows a polynomial fit for n_{Si}.

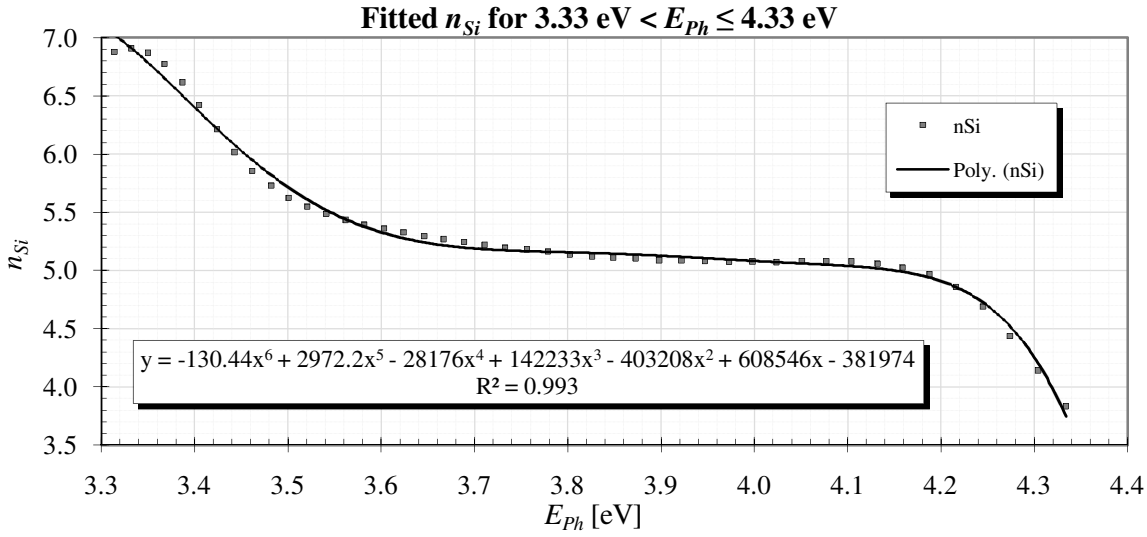


Figure 2.17. Fitted silicon refractive index for 286 nm ≤ λ ≤ 372 nm.

Due to large gradient variations, the best silicon extinction coefficient curve-fit is achieved in three overlapping parts over the range 1.24 eV ≤ E_{Ph} < 4.33 eV (286 nm ≤ λ ≤ 1 µm)

Figure 2.18 shows a k_{Si} polynomial fit for 1.24 eV ≤ E_{Ph} < 3.11 eV (398 nm ≤ λ ≤ 1 µm).

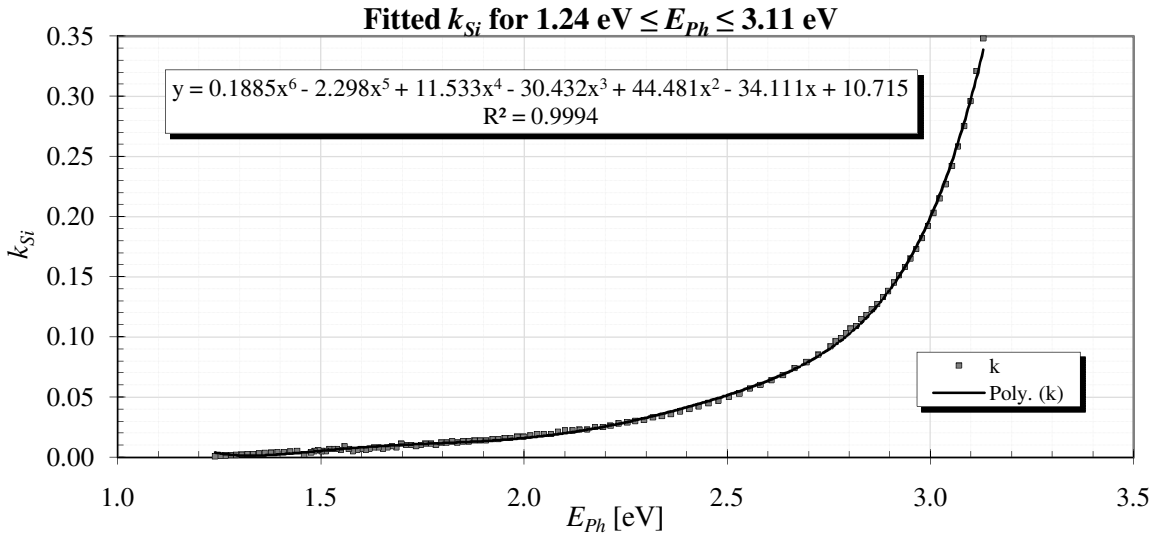


Figure 2.18. Silicon extinction coefficient k_{Si} polynomial fit for 1.24 eV ≤ E_{Ph} < 3.11 eV.

Figure 2.19 shows a k_{Si} polynomial curve fitting for 3.1 eV ≤ E_{Ph} < 3.42 eV (362 nm ≤ λ ≤ 400 nm)

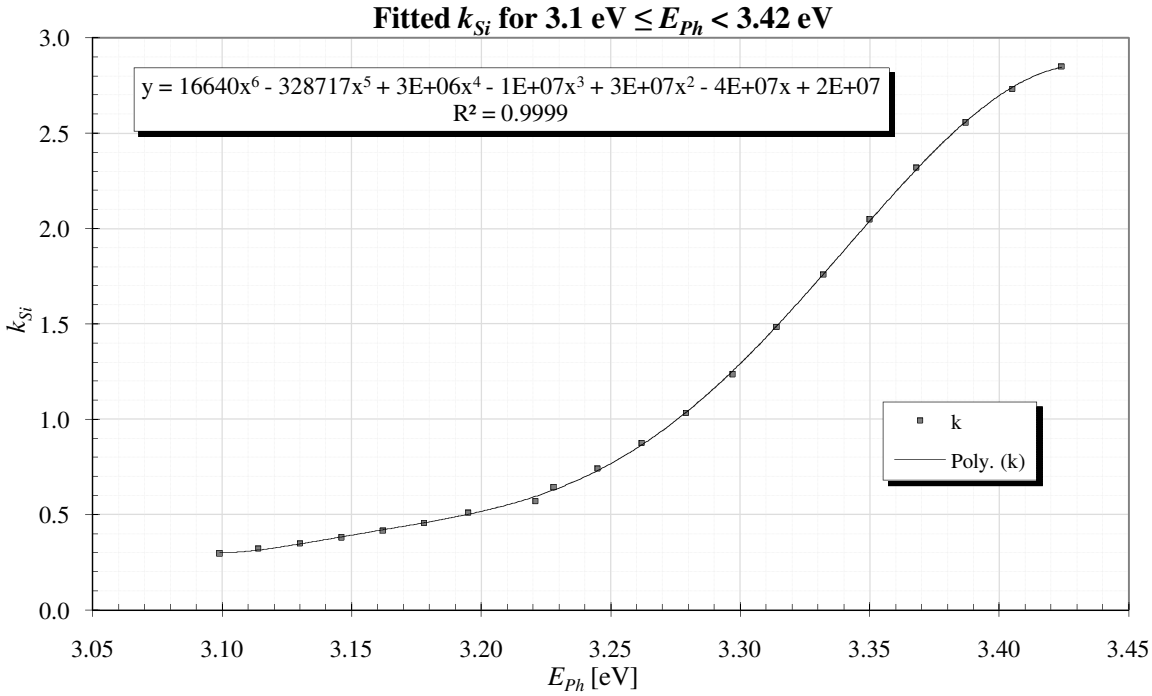


Figure 2.19. Silicon extinction coefficient k_{Si} polynomial fit for 3.1 eV ≤ E_{Ph} < 3.42 eV.

Figure 2.20 shows a k_{Si} polynomial curve fit for 3.39 eV ≤ E_{Ph} ≤ 4.33 eV (286 nm ≤ λ ≤ 366 nm).

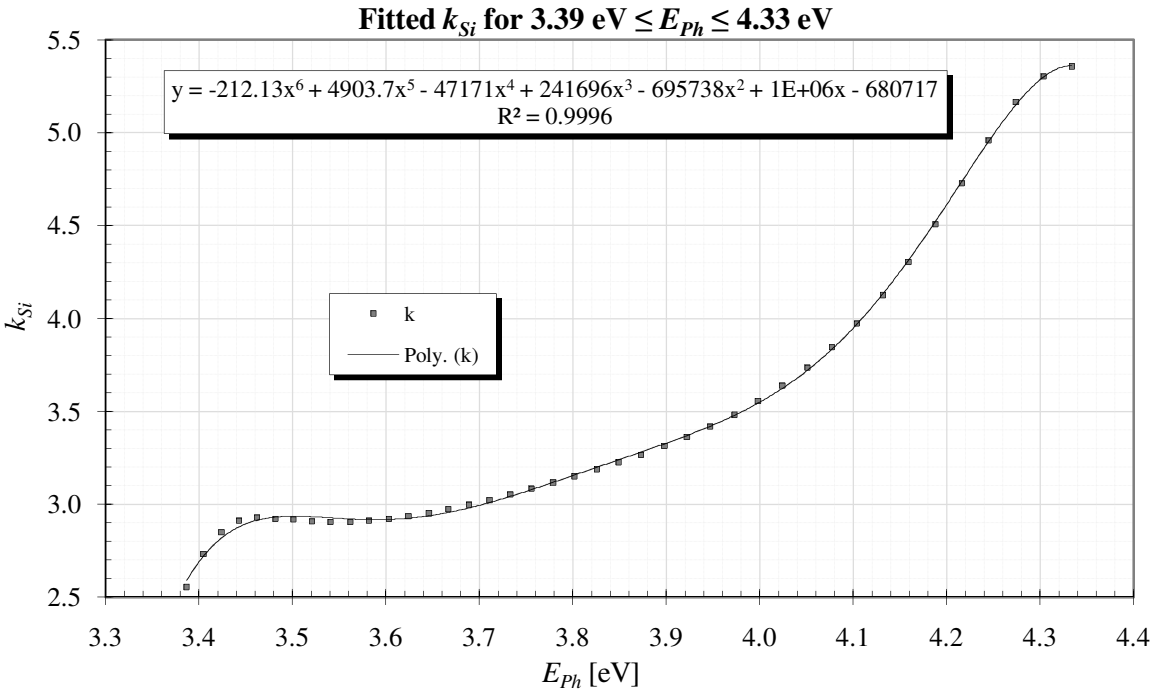


Figure 2.20. Silicon extinction coefficient k_{Si} polynomial fit for 3.39 eV ≤ E_{Ph} ≤ 4.33 eV.

2.2.2.2. Silicon Dioxide and Silicon Nitride

The refractive indices of chemical vapour deposited (CVD) SiO_2 and Si_xN_y are usually assumed fixed as $n_{SiO2} \approx 1.46$ and $n_{SixNy} \approx 1.99$ respectively although material properties like the polarizability of impurity ions [64] and the manufacturing process can, for example, vary n_{SiO2} between 1.43 and 1.51 and n_{SixNy} between 1.98 and 2.

The absorption coefficients of SiO_2 and Si_xN_y are very close to zero and usually only become significant in the deep-UV spectrum.

2.2.3. Optical Loss Mechanisms

2.2.3.1. Silicon Photon Absorption

Light travelling in silicon is absorbed as photons annihilate themselves by generating hole-electron pairs that diffuse from their generation site.

The wavelength-dependant average photon travelling distance $x_{Absotption}$ in which a material absorbs 63 % of the light is related to the material's absorption coefficient α through

$$\overline{x_{Absorption}} = \frac{1}{\alpha}. \tag{2.26}$$

Figure 2.21 illustrates the wavelength dependence of the optical absorption coefficient α and the average photon travelling distance $x_{Absorption}$ in silicon ([53], pg. 53, [65] and [66]).

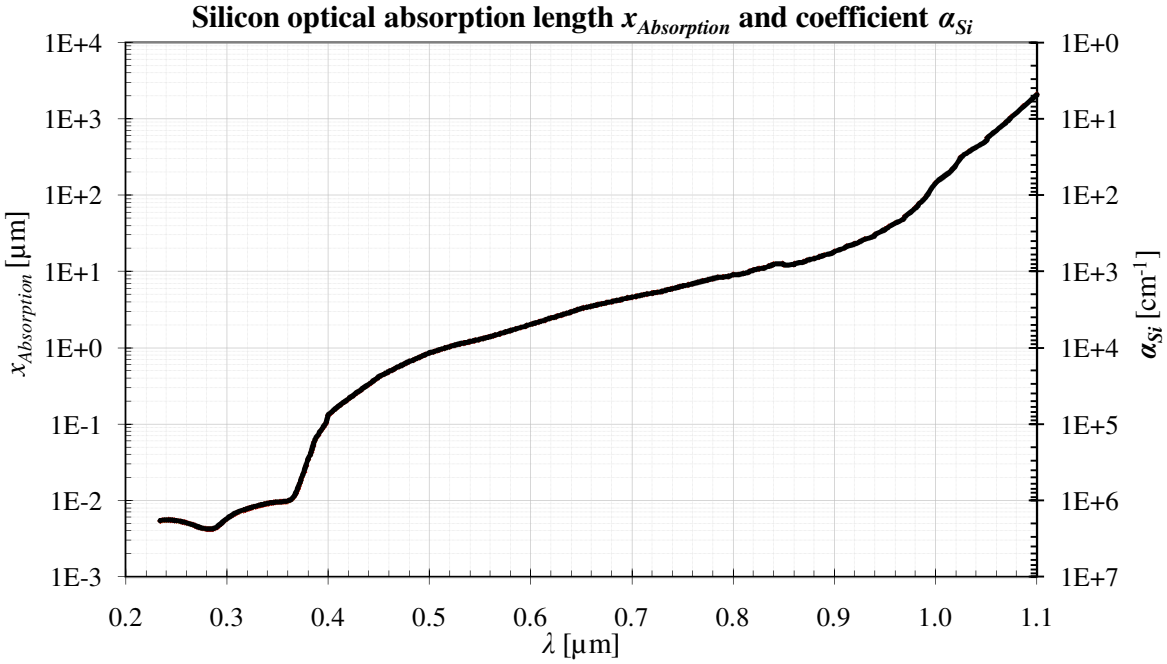


Figure 2.21. Silicon optical absorption distance $x_{Absorption}$ and coefficient α_{Si} against wavelength λ.

Figure 2.21 illustrates how 63 % of light with λ = 350 µm is absorbed within 10 nm of silicon, but light with λ = 1 µm can travel more than 100 µm through silicon.

According to [65] for 400 nm $\leq \lambda \leq$ 850 nm silicon's optical absorption coefficient α_{Si} can be numerically approximated in terms of wavelength λ (in µm) by

$$\alpha_{Si} \cong 10^{13.2131-36.7985\lambda+48.1893\lambda^2-22.5562\lambda^3} \text{ cm}^{-1}. \tag{2.27}$$

From (2.26) the photon flux at a distance x from a light source in a material is expressible as ([65], pg. 22)

$$\Phi_x = \Phi_0 \alpha \mathrm{e}^{\alpha x}, \tag{2.28}$$

where Φ_0 is the photon flux at the source ($x = 0$).

The optical power P_{Out} leaving the material's surface with total surface reflection coefficient R can be related the surface photon-flux Φ_S by

$$P_{Out} = \frac{\Phi_S E_{ph}}{(1-R)}, \tag{2.29}$$

where the photon energy E_{ph} depends on Planck's constant h, speed of light c (Addendum A) and wavelength λ by

$$\begin{aligned} E_{ph} &= h\frac{c}{\lambda} \\ &\approx \frac{1.24\,[\mathrm{eV}\cdot\mu\mathrm{m}]}{\lambda}. \end{aligned} \tag{2.30}$$

Since the absorption coefficient α, photon-flux Φ_0 and reflection coefficient R in equations (2.28) and (2.29) usually vary with wavelength, different light wavelengths will have different absorption lengths within a material.

The discussion in this subsection makes it evident that one way of increasing the externally available optical power from a silicon light source is to minimize the distance that the light has to travel through silicon. The possibility of decreasing the photon absorption within the silicon material between light generation site and surface is another incentive to manufacture nanometre-scale silicon light sources.

2.2.3.2. Optical Transmission through Si, SiO_2 and Si_xN_y Stacks

In addition to the light absorbed in the silicon around the light generation site, the different refractive indices of the different materials in the optical path will cause reflections and refractions that introduce a wavelength-dependant light attenuation.

Figure 2.22 illustrates how incident light *I* generated in the Si is reflected and transmitted by the SiO_2 and Si_xN_y layers covering the silicon surface [67].

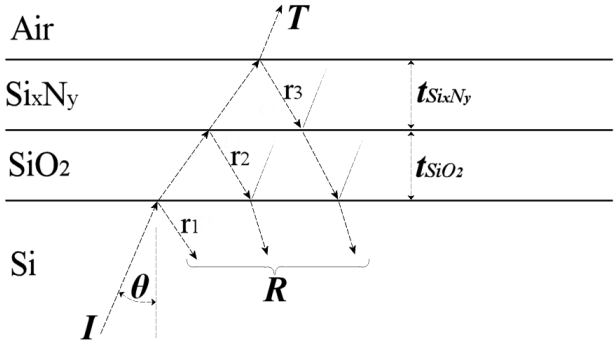


Figure 2.22. Light transmission through the Si, SiO_2, Si_xN_y and air layer stack.

In above figure the incident light (*I*) enters with angle θ to the normal of the Si-SiO_2 surface, *T* is the total light transmitted through to the air above the chip and *R* is the total reflection consisting of the reflection components r_1, r_2 and r_3 at the Si-SiO_2, SiO_2-Si_xN_y and Si_xN_y-air interfaces with thicknesses t_{SiO2} and t_{SixNy} respectively. As indicated, the light experiences multiple forward and backward reflections between the layer interfaces, which cause constructive and destructive interference and standing waves in a layer when the wavelength of the light is a multiple of the layer thickness.

Considering only perpendicular incidence (θ = 0) of light polarized in the plane of the Si surface, simplifies the electromagnetic wave analysis to the bidirectional field components illustrated in Figure 2.23.

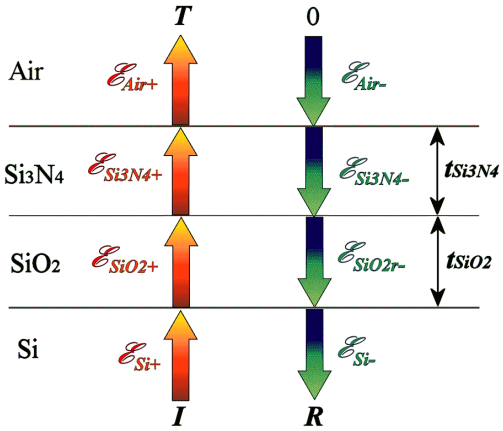


Figure 2.23. Electromagnetic fields in the Si-SiO_2-Si_xN_y-air interfaces.

In previous figure $\mathscr{E}_{x+}$ and $\mathscr{E}_{x-}$ denote the forward and reverse electromagnetic field components in material *x* respectively. The usage of these two distinct wave direction components is only to ease the analysis of a single complex electromagnetic field that is actually present.

Since the tangential electromagnetic field components at each dielectric interface must be continuous [68], the field strengths either side of an interface between materials x and y must be interrelated by

$$\mathscr{E}_{x+} - \mathscr{E}_{x-} = \mathscr{E}_{y+} - \mathscr{E}_{y-}. \tag{2.31}$$

Furthermore the refractive indices n_x and n_y of the materials either side of the interface interrelate the forward transmission and reverse reflection components by [69]

$$\begin{bmatrix} 1 & 1 \\ n_x & -n_x \end{bmatrix}\begin{bmatrix} \mathscr{E}_{x+} \\ \mathscr{E}_{x-} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ n_y & -n_y \end{bmatrix}\begin{bmatrix} \mathscr{E}_{y+} \\ \mathscr{E}_{y-} \end{bmatrix}. \tag{2.32}$$

Rewriting previous relation to express the field components in material x in terms of the field components existing in material y renders

$$\begin{aligned} \begin{bmatrix} \mathscr{E}_{x+} \\ \mathscr{E}_{x-} \end{bmatrix} &= \begin{bmatrix} 1 & 1 \\ n_x & -n_x \end{bmatrix}^{-1}\begin{bmatrix} 1 & 1 \\ n_y & -n_y \end{bmatrix}\begin{bmatrix} \mathscr{E}_{y+} \\ \mathscr{E}_{y-} \end{bmatrix} \\ &= \frac{1}{2}\begin{bmatrix} 1+\frac{n_y}{n_x} & 1-\frac{n_y}{n_x} \\ 1-\frac{n_y}{n_x} & 1+\frac{n_y}{n_x} \end{bmatrix}\begin{bmatrix} \mathscr{E}_{y+} \\ \mathscr{E}_{y-} \end{bmatrix}, \end{aligned} \tag{2.33}$$

which shows that $\mathscr{E}_{x+} = \mathscr{E}_{y+}$ is completely independent of $\mathscr{E}_{x-} = \mathscr{E}_{y-}$ when $n_y/n_x = 1$ and that the forward and reverse components "feed" into each other for $n_x \neq n_y$.

The relationship between the electromagnetic field strengths at opposite ends of material x depends on the layer's thickness t_x, the material's refractive index n_x and wavelength λ in the diagonal phase matrix

$$\Phi_x = \begin{bmatrix} \cos\phi_x + i\sin\phi_x & 0 \\ 0 & \cos\phi_x - i\sin\phi_x \end{bmatrix}, \tag{2.34}$$

where $\phi_x = 2\pi n_x t_x/\lambda$ and $i = \sqrt{-1}$. Above matrix models the constructive and destructive interference when the light's wavelength λ is a multiple of the layer thickness t_x.

Using the matrices in (2.32) and (2.34) the electromagnetic fields $\mathscr{E}_{Air}$ and $\mathscr{E}_{Si}$ of Figure 2.23 are relatable by

$$\begin{bmatrix} \mathscr{E}_{Air+} \\ \mathscr{E}_{Air-} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ n_{Air} & -n_{Air} \end{bmatrix}^{-1}\begin{bmatrix} \cos\phi_{Si_xN_y} & i\frac{\sin\phi_{Si_xN_y}}{n_{Si_xN_y}} \\ n_{Si_xN_y} i\sin\phi_{Si_xN_y} & \cos\phi_{Si_xN_y} \end{bmatrix}\begin{bmatrix} \cos\phi_{SiO_2} & i\frac{\sin\phi_{SiO_2}}{n_{SiO_2}} \\ n_{SiO_2} i\sin\phi_{SiO_2} & \cos\phi_{SiO_2} \end{bmatrix}\begin{bmatrix} 1 & 1 \\ n_{Si} & -n_{Si} \end{bmatrix}\begin{bmatrix} \mathscr{E}_{Si+} \\ \mathscr{E}_{Si-} \end{bmatrix}. \tag{2.35}$$

The total power reflection R_P and transmission T_P of the stacked layers are calculated by

$$R_P = \left|\frac{\mathscr{E}_{Si-}}{\mathscr{E}_{Si+}}\right|^2 \text{ and} \tag{2.36}$$

$$T_P = \left|\frac{\mathscr{E}_{Air+}}{\mathscr{E}_{Si+}}\right|^2. \tag{2.37}$$

Rewriting equation (2.35) in a simpler form as

$$\begin{bmatrix}\mathscr{E}_{Air+}\\ \mathscr{E}_{Air-}\end{bmatrix} = \begin{bmatrix}U & V\\ W & X\end{bmatrix}\begin{bmatrix}\mathscr{E}_{Si+}\\ \mathscr{E}_{Si-}\end{bmatrix}$$
$$\begin{bmatrix}T\\ 0\end{bmatrix} = \begin{bmatrix}U & V\\ W & X\end{bmatrix}\begin{bmatrix}I\\ R\end{bmatrix}, \tag{2.38}$$

where the fact that no light is incident from the air ($E_{Air-} = 0$) can be used to express the total reflected power as

$$R_P = \left|\frac{-W}{X}\right|^2. \tag{2.39}$$

Using (2.35) to obtain W and X, the power transmission T_P through all layers becomes

$$\begin{aligned} T_P &= 1 - R_P \\ &= 1 - \left|\frac{W}{X}\right|^2 \\ &= 1 - \frac{(n_{Si}a - n_{Air}d)^2 + (n_{Air}n_{Si}b - n_{Air}c)^2}{(n_{Si}a + n_{Air}d)^2 + (n_{Air}n_{Si}b + n_{Air}c)^2}, \end{aligned} \tag{2.40}$$

where

$$a = \cos\phi_{SiO_2}\cos\phi_{Si_xN_y} - \frac{n_{SiO_2}}{n_{Si_xN_y}}\sin\phi_{SiO_2}\sin\phi_{Si_xN_y}, \tag{2.41}$$

$$b = \frac{\sin\phi_{SiO_2}\cos\phi_{Si_xN_y}}{n_{SiO_2}} + \frac{\cos\phi_{SiO_2}\sin\phi_{Si_xN_y}}{n_{Si_xN_y}}, \tag{2.42}$$

$$c = n_{Si_xN_y}\cos\phi_{SiO_2}\sin\phi_{Si_xN_y} + n_{SiO_2}\sin\phi_{SiO_2}\cos\phi_{Si_xN_y} \text{ and} \tag{2.43}$$

$$d = \cos\phi_{SiO_2}\cos\phi_{Si_xN_y} - \frac{n_{Si_xN_y}}{n_{SiO_2}}\sin\phi_{SiO_2}\sin\phi_{Si_xN_y}. \tag{2.44}$$

As before, $\phi_x = 2\pi n_x t_x/\lambda$ (where "x" is a placeholder for either Si_xN_y or SiO_2).

With the availability of the thin-film interference expression in (2.40), knowledge of the SiO_2 and Si_xN_y layer thicknesses t_{SiO2} and t_{SixNy} will allow the estimation of the optical power passing through the SiO_2 and Si_xN_y layers covering the wafer.

To briefly investigate the optical transmission effects of SiO_2 and Si_xN_y layers covering an IC the typical CMOS layer thicknesses in Table 2.1 are used in an example.

Table 2.1. Typical AMS 0.35 µm SiO_2 and Si_xN_y layer thicknesses.

Layer	**Thickness** [nm]
t_{FOx}	55.2
t_{GOx}	7.6
t_{P1}	282
t_{P1M1Ox}	918
t_{M1}	665
t_{IMOX12}	1000
t_{M2}	640
t_{IMOX23}	1000
t_{M3}	640
t_{IMOX34}	1000
$\boldsymbol{t_{SiO2}}$	**6208**
t_{Prot1}	1030
t_{Prot2}	1000
$\boldsymbol{t_{Si3N4}}$	**2030**

Figure 2.24 compares the nominal Si-air, Si-SiO_2-air and Si-SiO_2-Si_xN_y-air interface transmissions of above typical CMOS layer thicknesses.

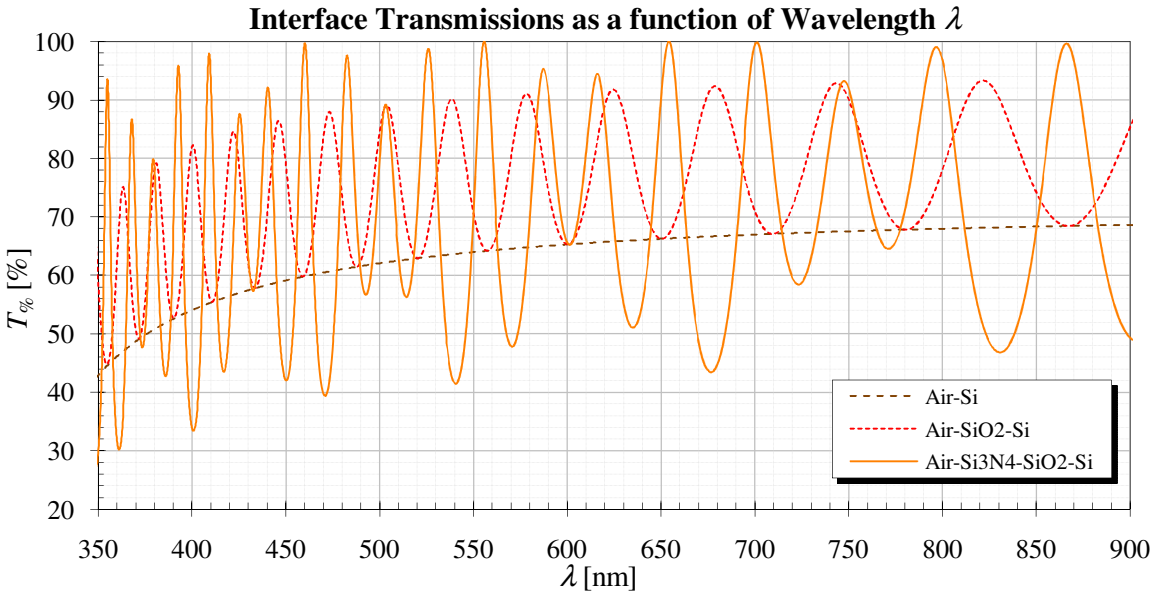


Figure 2.24. Comparison of Air-Si_xN_y-SiO_2-Si, Air-SiO_2-Si and Air-Si transmissions.

For all light transmission profiles above it is evident that the average transmission initially decreases slowly with decreasing wavelength, but then drops off significantly for $\lambda < 400$ nm. This characteristic attenuation of shorter wavelengths is due to the wavelength-dependant refractive index of the bulk Si (section 2.2.2.1) and independent of the SiO_2 and Si_xN_y layer properties.

Since it might be expected that removing the SiO_2 and/or Si_xN_y layer(s) could remove the wavelength-dependant transmission and lead to a higher optical coupling into the air, these scenarios are discussed next.

It is evident in Figure 2.24 that the addition of the SiO_2 layer on top of the silicon "builds on" the Si-air transmission by periodically improving the transmission at certain wavelengths, but never reducing the transmission below the Si-air transmission. This is due to constructive interference of standing waves in the SiO_2 layer.

Adding the Si_xN_y layer on top of the SiO_2 also improves the transmission at certain wavelengths, but reduces the transmission for other wavelengths.

Figure 2.25 compares the average light transmissions through the Si-air, Si-SiO_2-air and Si-SiO_2-Si_xN_y-air interface systems.

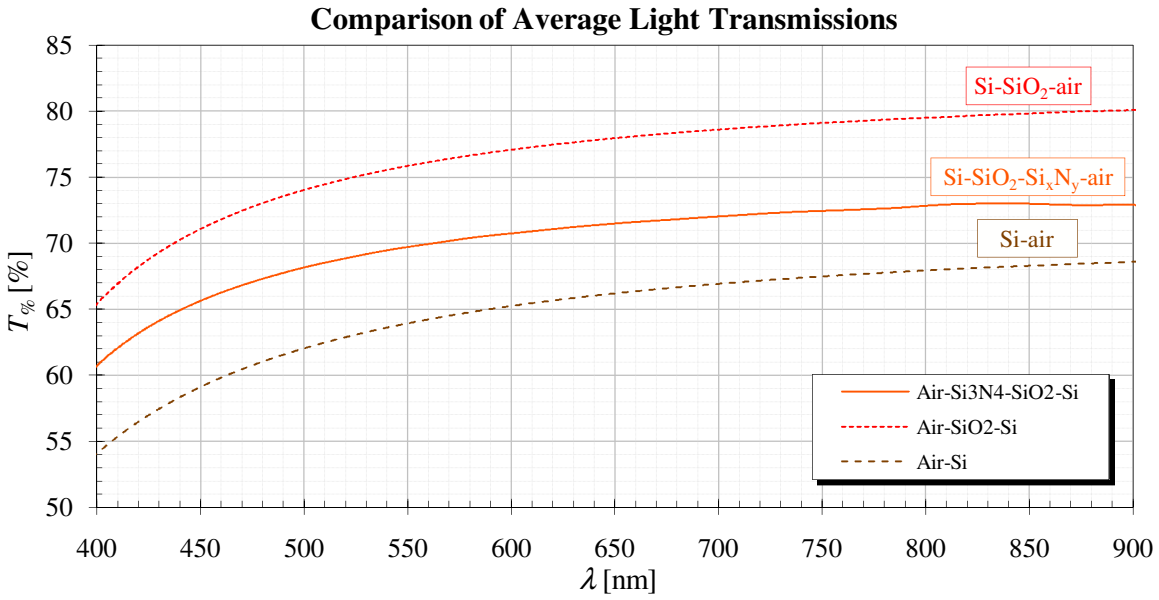


Figure 2.25. Average light transmissions through Si-air, Si-SiO_2-air and Si-SiO_2-Si_xN_y-air stacks.

As shown in above plot, the simple Si-air interface (without SiO_2 and Si_xN_y layers), while eliminating the interference patterns in Figure 2.24, also results in the lowest average light power exiting into the air above the chip.

Figure 2.25 shows that the highest average light transmission occurs for the Si-SiO_2-air interface system that transmits on average about 6 % more than the Si-SiO_2-Si_xN_y-air interfaces and about 12 % more than the Si-air system. The cause of this phenomenon is that while constructive and destructive light interference causes the wavelength-dependant transmission variations (when the light wavelength is a multiple of a layer thickness), the relation between the refractive indices of the materials determines the average light transmission and reflection through them. While the SiO_2 refractive index of about 1.46 is between the refractive indices of air (n_{Air} = 1) and silicon ($3.5 \leq n_{Si} \leq 5$ for 0.4 µm $\leq \lambda \leq$ 0.9 µm), the refractive index of Si_xN_y (≈ 2) is not between the refractive indices of air and SiO_2. The criteria for increasing the average transmission therefore requires that the refractive indices of intermediate layers satisfy the relationship $n_{Si} \geq n_1 \geq \ldots \geq n_x \geq n_{Air}$, where materials 1 to x are arbitrary transparent layers covering the chip. For this reason, the SiO_2 layer acts as antireflection coating that reduces the total light reflection by introducing an intermediate refractive index value between the refractive indices of Si and air.

The previous transmission calculations ignore the optical absorption within the SiO_2 and Si_3N_4 layers as their extinction coefficients are usually considered negligibly small in the wavelength range of interest (350 to 950 nm), but their processing-dependant absorption coefficients could become influential when sufficient impurities are present within them.

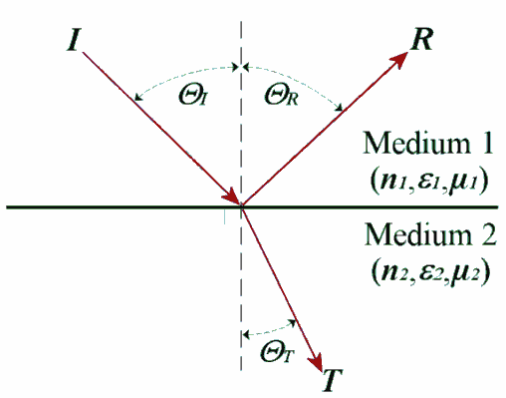
2.2.3.3. Oblique Light Incidence

The thin-film interference analysis in the previous section assumed orthogonal light incidence. Since light from the source will not always pass all interfaces in the optical path perpendicularly, it is worthwhile to calculate the effect of varying incidence angle on material interface transmission and reflection.

With reference to Figure 2.26, Snell's laws of reflection and refraction state that the incidence, transmission and reflection angles of an electromagnetic wave impinging on an interface between two materials with refractive indices n_1 and n_2 and equal permeability ($\mu_1 = \mu_2$) are related by [68]

$$\Theta_R = \Theta_I \text{ and} \tag{2.45}$$

$$\frac{\sin\Theta_T}{\sin\Theta_I} = \frac{n_1}{n_2} = \sqrt{\frac{\varepsilon_1}{\varepsilon_2}} = \sqrt{\frac{\varepsilon_{r1}}{\varepsilon_{r2}}}, \tag{2.46}$$



where equation **Error! Reference source not found.** has been used to relate material refractive index to permeability.

Figure 2.26. Medium and angle definitions for Snell's laws of reflection and refraction.

Figure 2.27 plots the transmission refraction angle Θ_T against incident angle Θ_I when each medium interface is considered separately.

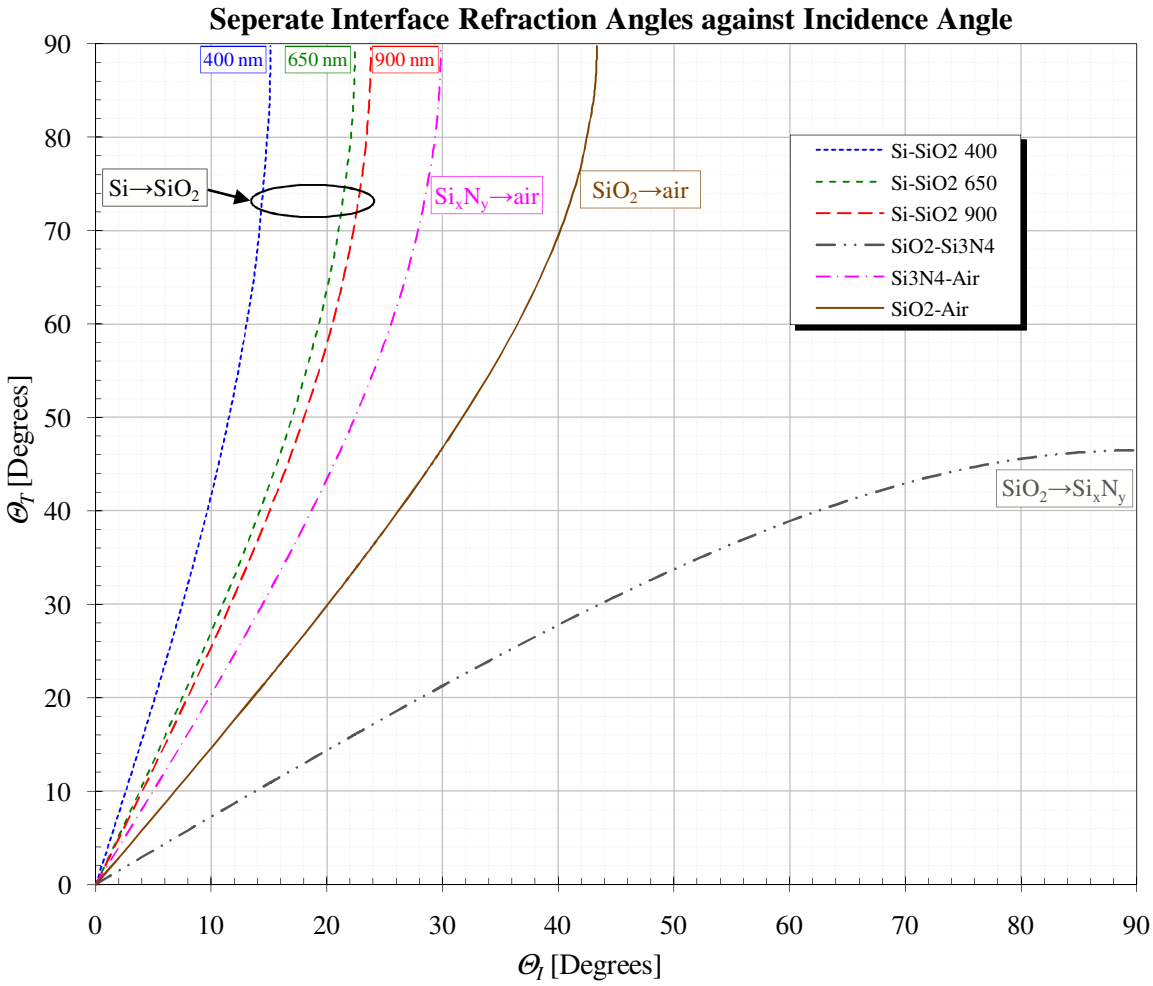


Figure 2.27. Single interface transmission angles against incidence angle.

Except for the $SiO_2 \rightarrow Si_xN_y$ interface, all other interfaces have $\Theta_T > \Theta_I$, i.e. they bend the refracted light away from the normal to the interface.

The maximum exit angle of about 46 ° for the $SiO_2 \rightarrow Si_xN_y$ interface is due the interface's critical angle Θ_C, which is equal to

$$\Theta_C = \sin^{-1} \frac{n_{SiO_2}}{n_{Si_xN_y}} \tag{2.47}$$

and only occurs when light passes from a less dense into a denser medium.

To establish which acceptance angles on the Si side of the Si-SiO_2 boundary will still allow light to exit the top-most SiO_2 or Si_xN_y surface into the air, the refracted angle from one interface can be used as incidence angle for the next interface above it.

This is done in Figure 2.28, which shows the final SiO_2-air exit angle Θ_{Air} against the Si-SiO_2 entry angel Θ_{Si}.

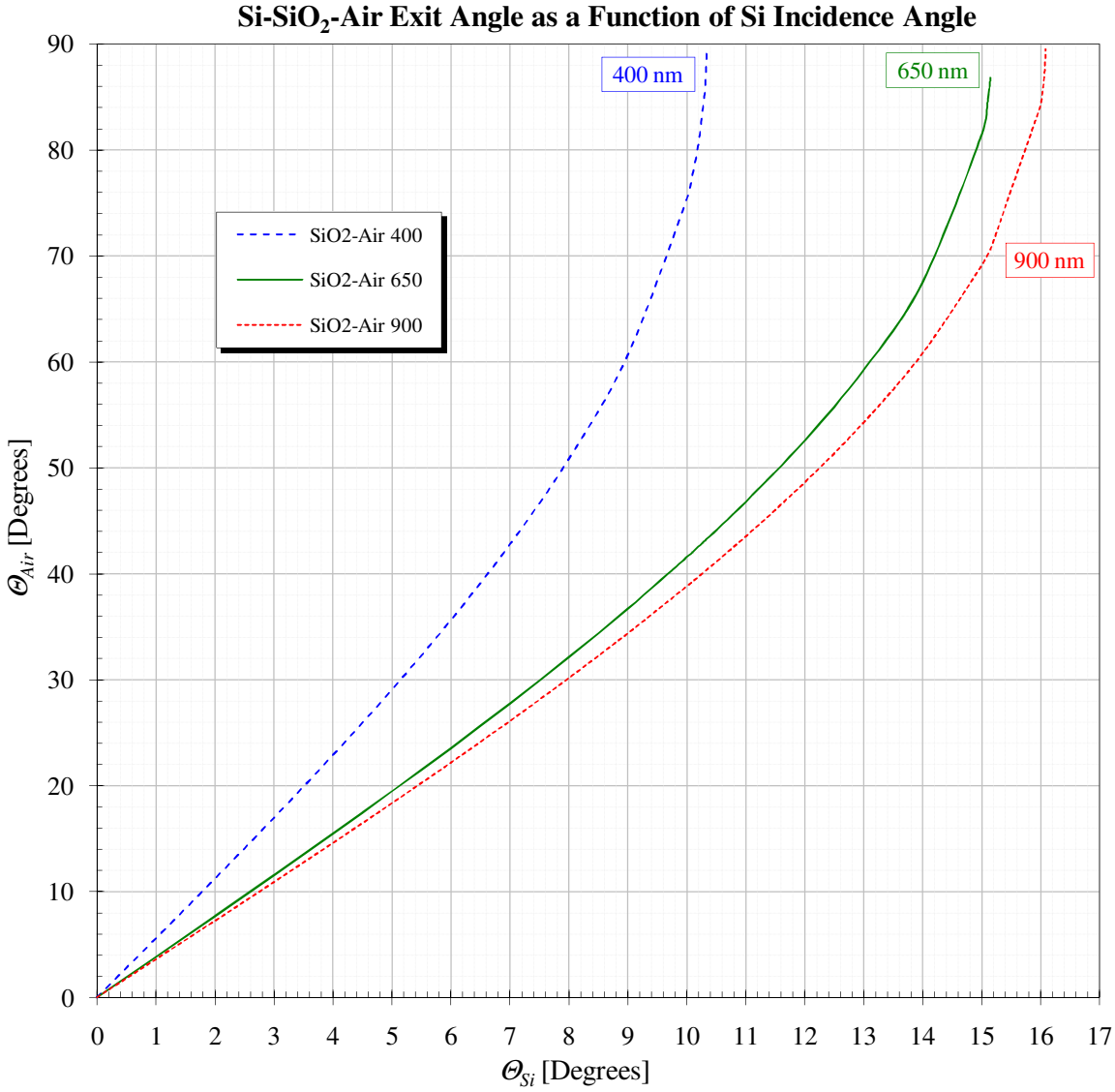


Figure 2.28. Single interface transmission angles against incidence angle.

Figure 2.28 shows that for an air exit-angle $\Theta_{Air} = 90°$ the acceptance angle on the silicon side of the Si-SiO_2–air boundary Θ_{Si} varies with wavelength between 10.4° and 16.1° for 400 nm $\leq \lambda \leq$ 900 nm. Exactly the same bulk Si acceptance angle limit is present whether a Si_xN_y layer is introduced between the SiO_2 and air or even when the SiO_2 is removed from the chip's surface.

Symbolic substitutions into equation (2.46) confirm that the exit angle from a stack of transparent media depends only on the refractive indices of the initial and final media if the refraction angles do not exceed the critical angles of intermediate interfaces.

$$\begin{aligned}\Theta_{Si} &= \sin^{-1}\left(\frac{n_{SiO2}}{n_{Si}}\sin\Theta_{SiO2}\right)\\ &= \sin^{-1}\left[\frac{n_{SiO2}}{n_{Si}}\sin\left\{\sin^{-1}\left(\frac{n_{Si3N4}}{n_{SiO2}}\sin\Theta_{Si3N4}\right)\right\}\right]\\ &= \sin^{-1}\left(\frac{n_{Si3N4}}{n_{Si}}\sin\Theta_{Si3N4}\right)\\ &= \sin^{-1}\left[\frac{n_{Si3N4}}{n_{Si}}\sin\left\{\sin^{-1}\left(\frac{n_{Air}}{n_{Si3N4}}\sin\Theta_{Air}\right)\right\}\right]\\ &= \sin^{-1}\left(\frac{n_{Air}}{n_{Si}}\sin\Theta_{Air}\right).\end{aligned} \tag{2.48}$$

Above finding makes it clear that, depending on distance from the Si-SiO_2 interface, a large percentage of the light generated at the isotropic Si light source generation site is lost and does not exit into the air above the IC.

One way of making more light externally available would therefore be to manufacture circular or hemispherical light sources in which light reaching the Si surface will impinge with an angle smaller than about 10 ° (for λ = 400 nm).

2.3. Processing Properties

2.3.1. Self-limiting Thermal Oxidation

Some metals (Fe, Al, Si, …) react with oxygen very easily. Over time, oxygen chemically combines with the atoms on the materials surface to form an oxide layer. Two requirements are necessary for this oxidation: oxygen in the environment (O_2 or H_2O) and thermal energy (i.e. heat). Since both of these are readily available in most uncontrolled environments, Si is usually covered with a native oxide layer a few nanometres thick.

Figure 2.29 shows how thermal oxidation reduces the thickness of Si by an amount ΔSi by growing a SiO_2 layer with thickness t_{SiO2} on the Si.

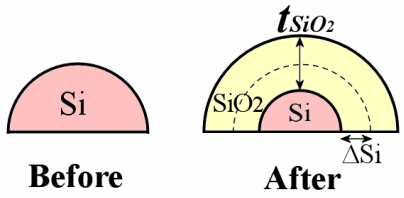


Figure 2.29. Si finger thinning oxidation dimensions.

The ratio of ΔSi removed to SiO_2 thickness t_{SiO2} grown during oxidation≈ 0.44 so that for every micron of SiO_2 grown about 440 nm of Si are consumed.

The thermal oxidation of Si in an oxygen ambient involves two kinetic processes: the diffusion of O_2 through the SiO_2 and the chemical reaction [70]

$$\mathrm{Si} + \mathrm{O}_2 \Leftrightarrow \mathrm{SiO}_2. \tag{2.49}$$

As oxidation progresses in time, the thicker growing SiO_2 layer covering the Si makes it more and more difficult for oxygen to diffuse through it to chemically react with the Si underneath and form SiO_2. This means that the oxidation rate slows down more and more with time until it seems to have stopped. This effect depends on the diffusivity of oxygen in SiO_2, which depends on the oxidation temperature T_{Ox}. At room temperature T_{Ox} is rather low (≈ 300 K), which explains why the native Si oxide thickness is only a few nanometres thick. The self-limiting oxidation effect described by the Deal-Grove model [71] can be clearly seen in the measured thermal oxidation data plotted in Figure D.3.

The SiO_2 thickness t_{SiO2} depends on oxidation temperature and oxidation time t_{Ox} through

$$t_{SiO_2}{}^2 + A t_{SiO_2} = B\left(t_{Ox} + \tau\right), \tag{2.50}$$

where A [µm] is the linear growth factor, B [µm^2/h] is the parabolic growth factor and τ [h] is the oxidation time offset that compensates for an initial oxide thickness at $t_{Ox} = 0$.

A and B depend on oxidation temperature and whether the oxidation is wet or dry. Since the initial (native) oxide thickness for wet oxidations is very small, $\tau \approx 0$ for wet oxidation.

For short oxidation times the oxidation is reaction rate limited and the oxide growth in this "linear regime" is calculated as

$$t_{SiO2} = \frac{B}{A}(t_{Ox} + \tau). \tag{2.51}$$

Longer oxidation times are diffusion limited where the oxide growth in the "parabolic regime" can be expressed as

$$t_{SiO2}{}^2 = B(t_{Ox} + \tau). \tag{2.52}$$

For dry oxidation the parabolic SiO_2 growth rate constant B at an oxidation temperature T_{Ox} can be expressed as

$$B = 772\,\mathrm{e}^{\frac{-1.23\,\mathrm{eV}}{k_B T_{Ox}}}\ [\mu\mathrm{m}^2/\mathrm{h}], \tag{2.53}$$

and for wet oxidation with water temperature T_{H2O} as

$$B = \left(0.217\,\mathrm{e}^{\frac{T_{H_2O}}{62.1^{\circ}C}}\right)^2 386\,\mathrm{e}^{\frac{-0.78\,\mathrm{eV}}{k_B T_{Ox}}}\ [\mu\mathrm{m}^2/\mathrm{h}]. \tag{2.54}$$

The parabolic SiO_2 growth rate constant B is about 25 times higher at T_{Ox} = 1050 ºC in a wet ambient compared to dry oxidation. This is primarily due to the much higher solid solubility of H_2O in SiO_2 than of O_2 in SiO_2, thus providing a much higher supply of oxidizing O_2 to the underlying Si for oxidation.

Etching the SiO_2 away and subjecting the Si again to an thermal oxidizing environment starts the oxidation sequence again in the linear region.

Oxidation of Si with a non-planar surface (i.e. wires, dots or other structures with curved surfaces) introduces another limiting factor into the oxidation process. As SiO_2 grows on the curved Si surface, the accumulating mechanical stress in the oxide slows down the chemical oxidation reaction rate and the diffusion of O_2 through the stressed SiO_2 ([72] and [73]). Similar stresses in grown SiO_2 are also responsible for the well-known "birds beak" shape of the LOCOS oxide [74].

This effect is especially pronounced in Si nano-structures since with decreasing structure dimensions and consequently decreasing surface curvature radius the oxidation rate decreases much more dramatically compared to planar bulk Si [75]. These self-limiting oxidation effects can therefore be used to create nanometre-scale Si structures like wires and nano-dots with predictable final dimensions that can be estimated from the initial Si dimensions, crystal orientation and the oxidation parameters (oxidation time and temperature) [76].

According to Kedzierski *et al* [77] the oxidation progress of SOI Si nano-wires can be expected to progress as shown in Figure 2.30.

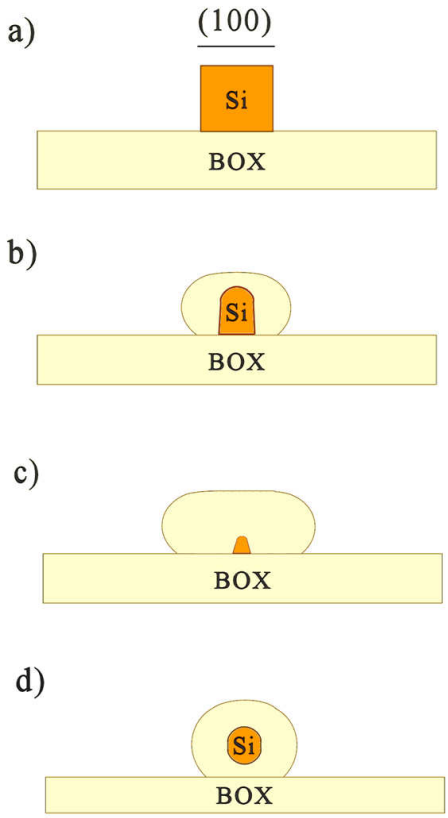


Figure 2.30. Si shape a) before oxidation, during b), c) continuous and d) undercutting oxidation.

Figure 2.30 a) shows the cross-sectional view of the initial Si bar. Figure 2.30 b) then shows that the Si wire will first be predominantly oxidized from the sides parallel to the (100) plane and from the top. Since less O_2 diffuses to the bottom of the structure, it will oxidize slower than the top. Figure 2.30 c) shows that if oxidation is continued, the wire will first get thinner from the sides until the top side of the Si is consumed and a smaller triangular shape remains close to the BOX. Figure 2.30 d) shows one way of achieving round Si finger wires. By etching the grown SiO_2 and the BOX, the Si finger is also oxidized from the bottom, which gives it a rounder shape.

2.3.2. Dopant-dependant Oxidation

The oxidation of extrinsic silicon can be modelled by modifying the Deal-Grove linear-parabolic growth law in (2.51) in subsection 2.3.1. The dependence of silicon oxidation kinetics on doping concentration manifests as part of the linear rate constant, where the physical effects of higher doping levels has been explained primarily as an electrical effect. The modified linear rate constant that includes the doping dependence becomes [78]

$$\frac{B}{A} = \left(\frac{B}{A}\right)_i \left(\frac{B}{A}\right)_{Doping} \tag{2.55}$$

where $(B/A)_i$ is the linear rate constant on intrinsic Si and [79]

$$\left(\frac{B}{A}\right)_{Doping} = \left\{1 + B_{K0} e^{-\frac{B_{FE}}{k_B T}\left(\frac{V^*}{V_i^*} - 1\right)}\right\} \tag{2.56}$$

where V^* is the equilibrium vacancy concentration in the doped Si at the Si/SiO_2 interface, V_i^* is the equilibrium vacancy concentration in intrinsic Si, B_{K0} and B_{FE} are experimentally-determined Arrhenius coefficients relating to the doping dependence of the oxidation rate.

In general, the doping type and concentration in the Si cause a Fermi level shift that alters the Si equilibrium vacancy concentration, composed of vacancy defects in different charged states [80]. Figure 2.31 shows the functional dependence of the equilibrium vacancy concentration at 950 ºC versus doping concentration for commonly used Si dopants.

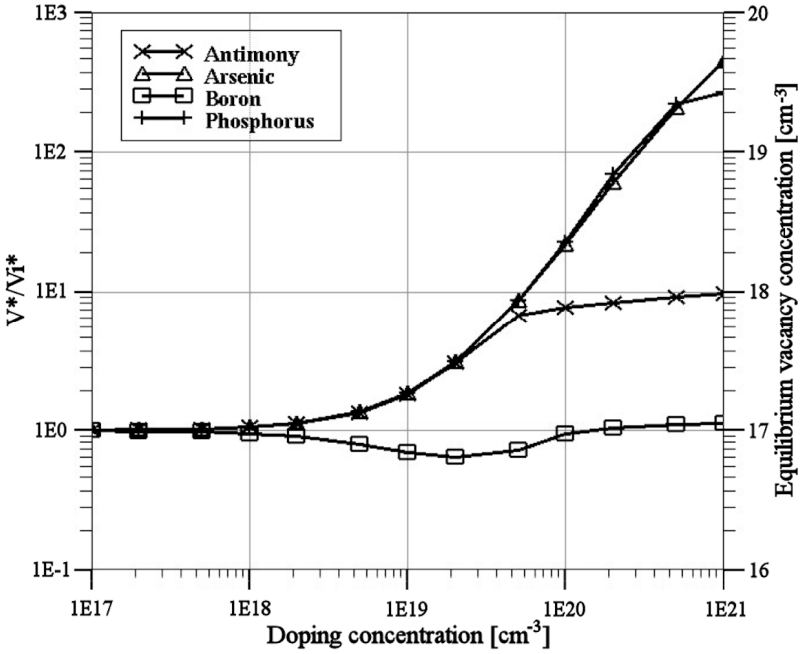


Figure 2.31. Si equilibrium vacancy concentration versus doping density and species at 950 ºC.

The physical significance of an increase in the vacancy concentration is a higher availability of unoccupied Si lattice reaction sites for the incoming oxidant molecules, which in turn enhances the oxidation rate.

An increased equilibrium vacancy concentration and consequently larger Si oxidation (with respect to the lower doping concentrations) is observed with increasing *n*-type doping, but remains essentially constant for the *p*-type dopant.

2.4. Summary

Section 2.1 revised important semiconductor properties of Si. Aspects like resistivity, intrinsic carrier concentration, built-in potential and depletion region width were used to design the layout dimensions of the SOI light sources while the influence of silicon's energy band diagram, impact ionization, avalanche breakdown, punch-through and reach-through properties on electroluminescence were introduced.

Subsection 2.2.1.2 investigated the radiative recombination mechanism in Si.

Subsection 2.2.1 determined that the optical power spectrum expected from a Si nanometre-scale finger junction would be similar to the typical CMOS light source power spectrum in Figure 2.14, but that it would have a higher amplitude with higher intensities for shorter wavelengths.

Subsection 2.2.1.4 discussed how carrier injection can be used to increase the quantum efficiency and resultant power efficiency of integrated Si light sources.

Comparing the average light transmissions through the Si-air, Si-SiO_2-air and Si-SiO_2-Si_xN_y-air interface systems in Figure 2.25 (subsection 2.2.3.2) revealed that the Si-SiO_2-air system transmits the most optical power from the Si light source into the air above.

Section 2.3 showed that geometrical factors, doping species and concentration affect the oxidation rate of Si.

3. PHYSICAL AND OPTICAL SIMULATION

Simulations were useful during the design stage to predict physical and optical properties achievable at the end of the manufacturing process.

3.1. Impurity Redistribution during Oxidation

The low diffusivity and solubility of arsenic (As) in SiO_2 results in the "snow-shovel" effect that causes As to pile up against the moving SiO_2 boundary during thermal oxidation, ([81] - [83]).

Boron (B) with its higher diffusivity and solubility in SiO_2 is absorbed into the SiO_2 during thermal oxidation, therefore decreasing its concentration in the Si, ([84] - [89]). Since the lower B background doping concentration of n^+p junctions plays a larger role in determining junction characteristics like depletion region width w_d than the higher As concentration, only the spatial B concentration variation with thermal oxidation was further considered.

The SOI B concentration $C(y,t)$ as a function of distance y from the BOX-Si interface and oxidation time t during thermal oxidation can be expressed as [84]

$$\frac{C(y,t)}{N_B} = 1 - \frac{\frac{k-m}{2}\sqrt{\frac{B\pi}{D_B}}\left\{\operatorname{erfc}\left(\frac{l-m\sqrt{Bt}-y}{2\sqrt{D_B t}}\right)+\operatorname{erfc}\left(\frac{l-m\sqrt{Bt}+y}{2\sqrt{D_B t}}\right)\right\}}{1-e^{-\left(\frac{l-m\sqrt{Bt}}{\sqrt{D_B t}}\right)^2}+\frac{k-m}{2}\sqrt{\frac{B\pi}{D_B}}\left\{1+\operatorname{erfc}\left(\frac{l-m\sqrt{Bt}}{2\sqrt{D_B t}}\right)\right\}}, \tag{3.1}$$

where $m \approx 0.44$ is the ratio of ΔSi removed to SiO_2 thickness t_{SiO2} grown during oxidation (section 2.3.1), B is the parabolic SiO_2 growth-rate constant, D_B the B diffusion constant and l is the initial SOI active layer thickness. $k = C_{SiO2}/C_{Si}$ is the segregation coefficient defined by C_{SiO2}, the B concentration on the SiO_2 side of the Si/SiO_2 boundary and C_{Si} the B concentration on the Si side of the same interface.

The B diffusion constant D_B can be expressed as

$$D_B = D_{B\infty}\, e^{\frac{-E_{As}}{k_B T_{Ox}}}\ [\mathrm{cm}^2/\mathrm{s}], \tag{3.2}$$

where $D_{B\infty}$ is a B diffusion constant and E_{As} is the activation energy for B diffusing through Si.

Figure 3.1 shows the simulated B concentration decrease from the initial implanted concentration during successive oxidations.

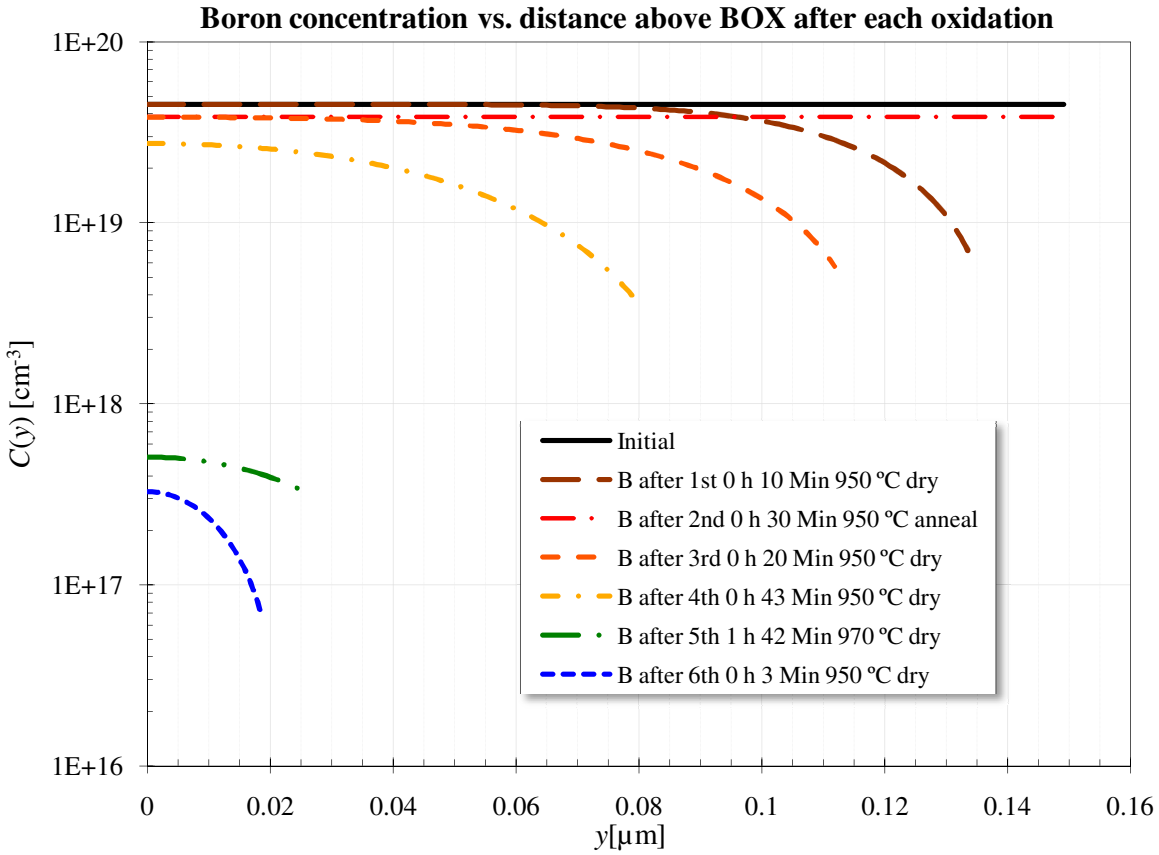


Figure 3.1. Boron redistribution during thermal oxidation and anneal processing steps.

Prior knowledge of oxidation steps therefore allowed specifying the initial B implantation dose so that the desired final average finger background B concentration of $\approx 10^{17}$ cm^{-3} would be achievable.

In reality, some B segregation and re-diffusion into the Si also occurs at the BOX interface [90], but was ignored in the simulation shown in above Figure.

3.2. Optical Radiation Simulation

Employing the geometrical optics RAYTRACE[1] software enabled the simulation of spatial light radiation characteristics of the Si fingers with varying finger geometries and light source locations.

Figure 3.2 for example shows how light generated at the centre of a finger with rounded corners focuses into four lobes (recognizable by higher ray density) emanating from the rounded top surface of the Si finger.

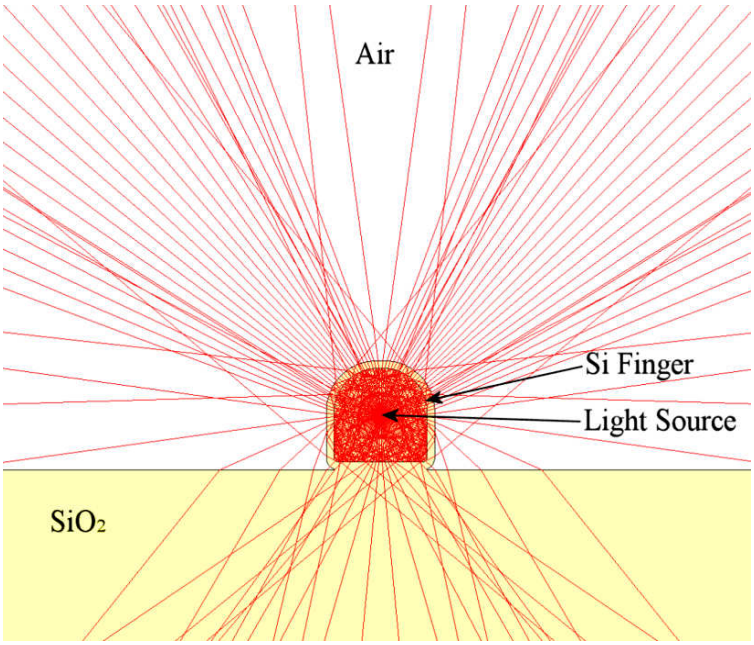


Figure 3.2. SOI finger spatial light radiation pattern simulation.

It was *inter alia* determined that the maximum useful light emission directed away from the chip surface is achieved with a hemispherical round top finger surface to minimize internal reflection beyond the critical interface incidence angle and a flat bottom surface to maximize reflection back to the top surface. Shaping the Si fingers in this way can increase the usefully radiated light by up to a factor five.

[1]Version 2.22, IME software, Ian Moore 1994 – 2006, http://www.ozemail.co.au/~imesoft.

4. DESIGN

To achieve the previously stated objective of creating Si wire junctions with diameters less than 50 nm, the SOI test-devices could not be manufactured in a standard process with supplied design rules. Instead, the layout and process design had to consider various equipment limitations and characteristics as well as physical effects occurring during the self-processing.

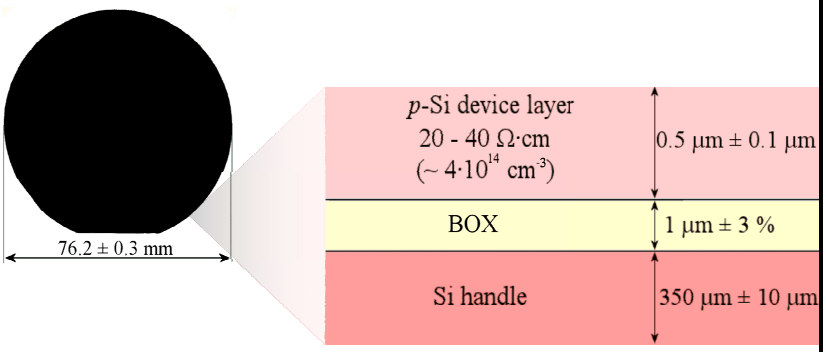
4.1. Starting Material

Before any design can commence the properties of the starting material need to be taken into consideration.

Table 4.1 shows the specifications of the SOI starting material wafers as supplied by Siegert Consulting e.K.[2].

Table 4.1. Siegert SOI Starting Material Specifications.

Parameter	Value	Graphical Representation
Type	Epitaxial Transfer SOI	
D_{Wafer}	76.2 ± 0.3 mm	
Doping	*p* (B)	
$t_{Device\ Layer}$	0.5 ± 0.1 µm	
$\rho_{Device\ Layer}$	20 - 40 Ω·cm ($\sim 4 \cdot 10^{14}$ cm^{-2})	
t_{Box}	1 µm ± 3 %	
ρ_{Handle}	0.01 – 0.02 Ω·cm	
t_{Handle}	350 µm ± 10 µm	
Edge exclusion	< 3 mm	



The 500 nm thick SOI active device layer above the BOX is the region where the light sources were implemented after its thickness was reduced to about 150 nm through thermal oxidation.

The 100 nm tolerance in SOI active device layer thickness might seem excessive, but is useful since a large variation in SOI light source thicknesses can be achieved with relative ease.

[2] Siegert Consulting e.K., TZA-Technologiezentrum Aachen, Dennewartstr. 25-27, Raum A 1.14, D-52068 Aachen, Germany.

4.2. Lithographic Patterning

As indicated in Table 4.2, the small geometries and precise pattern alignment of the current work required electron-beam lithography (EBL), but the single beam exposure scan of EBL is too slow to write all features across complete wafers.

Table 4.2. Photolithography and EBL Comparison.

Aspect	**Photolithography**	**EBL**
Wavelength/spot-size	≈ 300 nm	≈ 2 nm
Minimum feature size	≈ 0.5 µm	≈ 6 nm
Alignment accuracy	> 1 µm	> 6 nm
Exposure speed per wafer	Whole wafer at once Fast: Minutes	Serial scanning beam Very slow: hours

While photolithographic patterning is possible at the CEFIM, the Microelectronic Research Centre (MiRC) of the Georgia Institute of Technology was visited to make use of their JEOL JBX-9300FS EPG.

4.3. Mask Definitions

For the reasons in previous subsection, as Table 4.3 shows, different processing steps and geometry areas of the wafer selectively employed photolithography or EBL.

Table 4.3 Photolithographic and EBL Mask Detail.

Processing	**Document**	**GDS**	**Layout**	**Mask**			**Alignment**	
Step	**Section**	**No.**	**Rendering**	Name	Type	Polarity	Marker	Align to
3d	5.3	1		Si Island	Photo	Positive	-	-
4d	5.4	2		Arsenic (EBL)	EBL	Positive Tone	*AlignmentMarkerEBL*	Si Island
4j	5.4	3		Arsenic (Photo)	Photo	Negative	*AlignmentMarkerPhotoNoOx*	Si Island
5b	5.5	4		Finger Spacing	EBL	Positive Tone	*AlignmentMarkerEBL*	Si Island
6b	5.6	5		Oxidation (EBL)	EBL	Positive Tone	*AlignmentMarkerEBL*	Si Island
6c	5.6	6		Oxidation (Photo)	Photo	Negative	*AlignmentMarkerOx*	Si Island
7a	5.7	7		Contact	Photo	Negative	*AlignmentMarkerPhotoNoOx*	Si Island
7e	5.7	8		Metal	Photo	Positive	*AlignmentMarkerPhotoNoOx*	Contact
8	-	9		Si Isolation Spacing	Photo	Negative	*AlignmentMarkerPhotoNoOx*	Si Island

Six photolithographic plates and three EBL file masks were required. The photolithographic *Si Island* mask defines where Si islands remain on the BOX after reactive ion etching (RIE) removes the superfluous Si. The thin Si fingers are created by using the fine *Finger Spacing* EBL mask to RIE slits into the Si islands. The *Oxidation* mask was then used to selectively oxidize the Si between the slits into thin SOI fingers.

4.4. Design Rules

To facilitate the successful manufacture of the SOI light sources, self-made design rules had to be set-up. These design rules had considered possible mask alignment errors, limitations of the processing equipment and physical phenomena occurring during the wafer manufacturing process. These self-setup design rules are listed in Addendum C.

4.5. SOI Light Sources

Two types of SOI light sources were designed and manufactured:
2D-confined light sources are thin in two dimensions, thickness and width.
1D-confined light sources are only thin in one dimension, the thickness.

Both light source types were implemented for comparative purposes to investigate the possible increase in Si electroluminescence power efficiency improvement of 2D-confined device over 1D-confined Si light sources.

4.5.1. 2D-confined SOI Light Sources

Three types of 2D-confined SOI light sources were implemented:

1) n^+p finger junction avalanche light sources,
2) n^+pn^+ punch-through light sources and
3) Injection-enhanced light sources.

The design of these three types of 2D-confined Si light sources is described in the remainder of this sub-section.

4.5.1.1. n^+p Finger Junction Avalanche Light Sources

Figure 4.1 shows the pre-oxidized avalanche SOI finger light source layout.

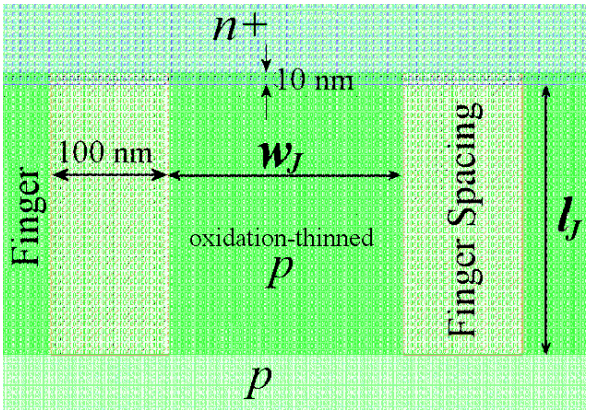


Figure 4.1. Avalanche finger layout dimensions.

The Si island regions above and below the fingers remained thick while an EBL-written oxidation mask opening across the fingers allowed the selective thinning through oxidation of the SOI finger junctions.

The dimensioning of the devices shown in Figure 4.1 had to comply with the following specifications to ensure proper functionality of the devices:

$$l_J \geq w_d + d_{Ox} + 3\Delta R_{\perp As} \approx 226 \text{ nm and} \quad (4.1)$$

$$w_J \approx 2t_{Si}, \quad (4.2)$$

where w_d is the reverse bias depletion region width at breakdown (see section 2.1.8), d_{Ox} is the worst-case As diffusion distance during all thermal oxidation steps after As implantation, $\Delta R_{\perp As}$ is the transverse As implantation straggle (Figure 5.4) and the initial Si thickness before oxidation was assumed to be 100 nm $\leq t_{Si} \leq$ 150 nm.

Relation (4.1) ensured that the fingers were long enough to accommodate the complete depletion region width after the implanted As (with its horizontal implant straggle) has diffused into the fingers after oxidation.

Equation (4.2) aimed to create semi-circular round fingers by assuming isotropic finger shaping oxidation that would thin the Si fingers equally from all sides.

Figure 4.2 depicts a 30 µm x 34 µm n^+p junction device with 100 parallel finger junctions.

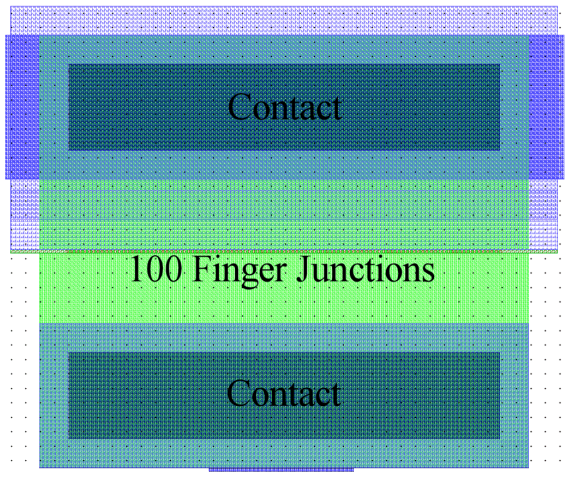


Figure 4.2. Finger junction device layout on a 1-µm grid.

Table 4.4 shows the dimensions of implemented n^+p avalanche SOI light sources.

Table 4.4. Implemented n^+p avalanche finger junctions.

Chip	**Group**	**Device**	**Pin**	**Type**	**Oxidized?**	w_J	l_J
#	*Name*		#			[nm]	
1	*FingerJunctions_Ox*	*100FingerJunctions200nm*	18	n^+p *Avalanche*	Oxidized	200	230
		100FingerJunctions220nm	17			220	
		100FingerJunctions240nm	16			240	
		100FingerJunctions260nm	15			260	
		100FingerJunctions280nm	14			280	
		100FingerJunctions300nm	13			300	
	FingerJunctions_NoOx	*100FingerJunctions200nm_NoOx*	24		Not oxidized	200	
		100FingerJunctions220nm_NoOx	23			220	
		100FingerJunctions240nm_NoOx	22			240	
		100FingerJunctions260nm_NoOx	21			260	
		100FingerJunctions280nm_NoOx	20			280	
		100FingerJunctions300nm_NoOx	19			300	

The common n^+ terminal to all above devices is connected to pad 5.

Figure 4.3 shows the 2D-confined finger junction avalanche SOI device layouts in *Chip1* (Figure 4.24) and the location of light source S with the narrowest pre-oxidized finger width (w_J = 200 nm).

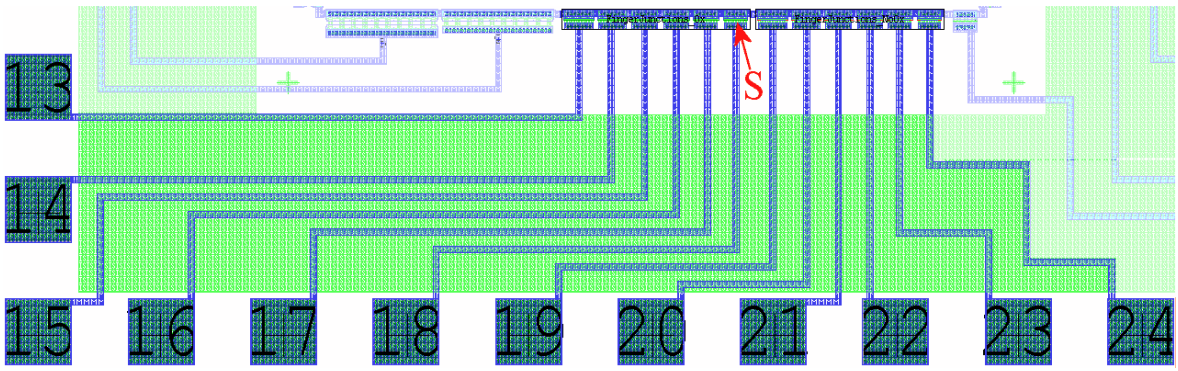


Figure 4.3. Finger junction devices layout.

4.5.1.2. n^+pn^+ Punch-through Light Sources

Figure 4.4 shows the designed layout dimension definitions of the punch-through SOI light source fingers.

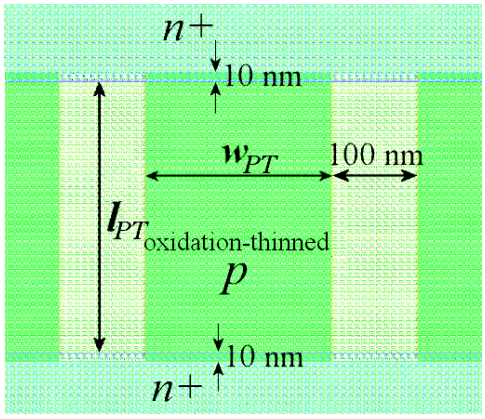


Figure 4.4. n^+pn^+ punch-through finger layout dimension definitions.

Similar to the avalanche breakdown devices the dimensioning of the devices shown in Figure 4.4 had to comply with the following specifications to ensure proper functionality of the devices:

$$l_{PT} \approx w_d + 2\left(d_{Ox} + 3\Delta R_{\perp As}\right) \approx 352 \text{ nm and} \tag{4.3}$$

$$w_{PT} \approx 2t_{Si}. \tag{4.4}$$

Figure 4.5 shows how 100 punch-through fingers shown in Figure 4.4 are placed in parallel between thicker and larger Si islands that allow electrical biasing through the interconnect metallization.

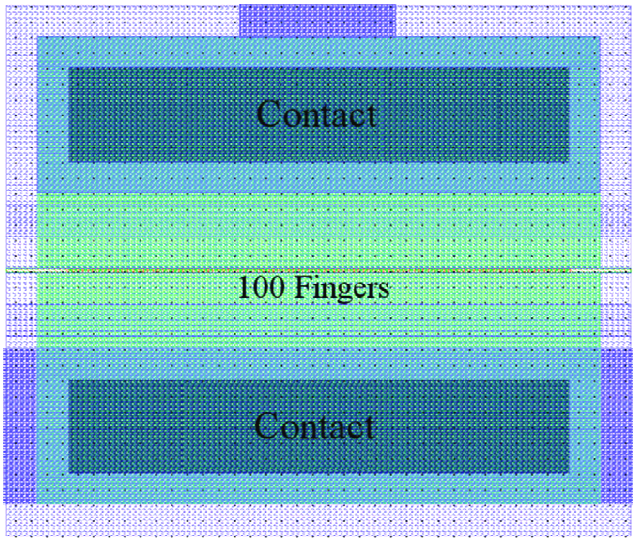


Figure 4.5. Device layout incorporating 100 parallel n^+pn punch-through fingers of Figure 4.4.

Table 4.5 and Table 4.6 show the implemented n^+pn^+ punch-through device dimensions.

Table 4.5. Oxidation-thinned punch-through device pin-out.

Oxidized		l_{PT} [nm]								
		320	330	340	350	360	370	380	390	400
w_{PT} [nm]	220	*34*	*25*	*29*	*35*	*26*	*30*	**38**	*27*	**33**
	260	*36*	**39**	*31*	**34**	*28*	*37*	**40**	*32*	**35**
	300	*38*	**3**	*33*	**1**	**4**	**36**	**2**	-	**37**

Legend: *pin on Chip1* **pin on Chip2**

Table 4.6. Non-thinned punch-through device pin-out.

Not oxidized		l_{PT} [nm]								
		320	330	340	350	360	370	380	390	400
w_{PT} [nm]	220	22	16	28	23	17	29	11	18	6
	260	24	12	30	7	19	26	13	31	8
	300	27	20	32	14	21	9	15	-	10

All pins on *Chip2*

The node common to all above devices is connected to pad 5.

Figure 4.24 shows *Chip2*, which is populated with the 2D-confined n^+pn^+ punch-through SOI light sources.

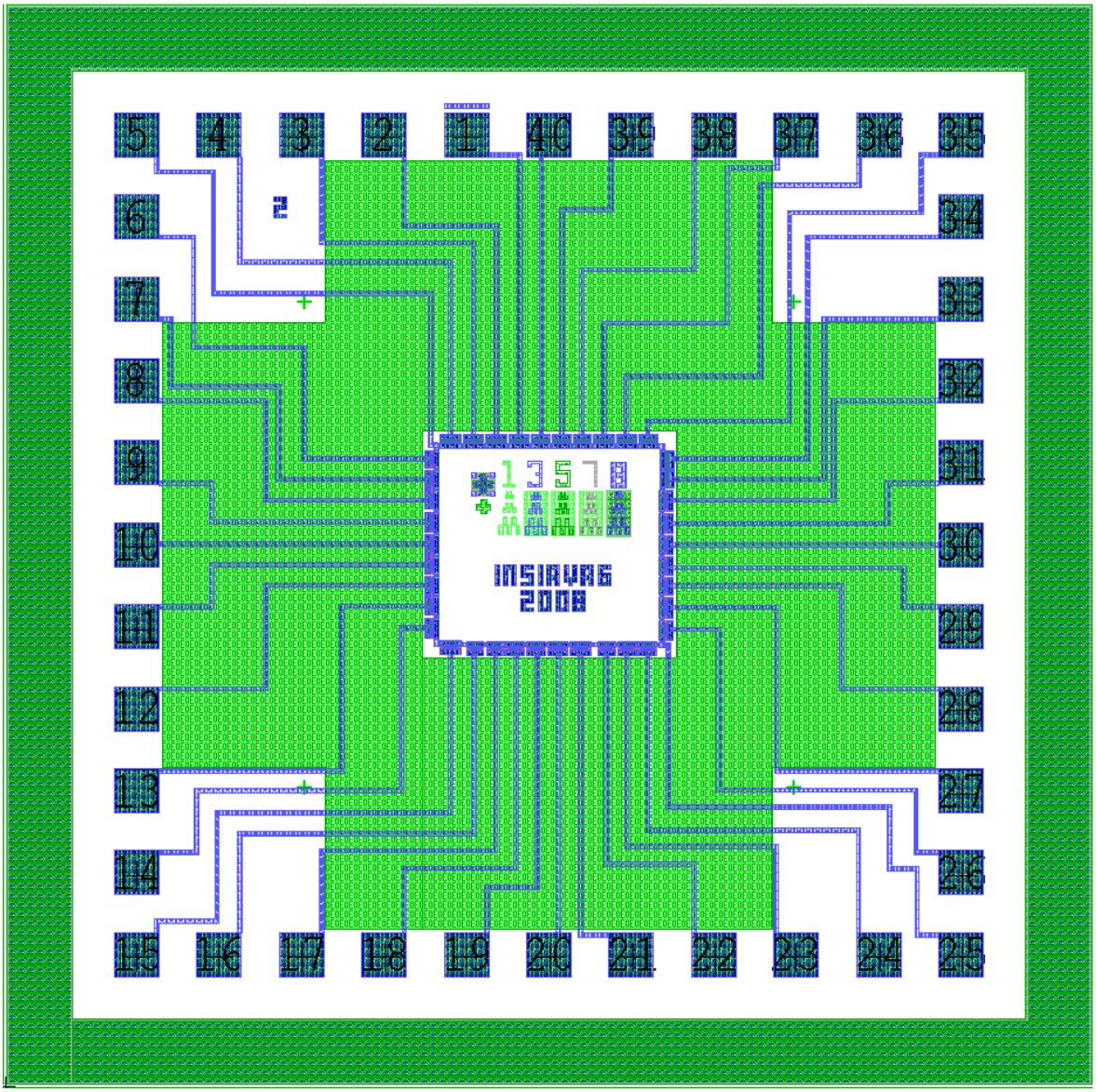


Figure 4.6. *Chip2* layout.

Chip1 and *Chip2* contain 2D-confined n^+pn^+ punch-through SOI light sources, but most are located on *Chip2*.

4.5.1.3. Carrier-injection Light Sources

Two different carrier-injection SOI light sources were designed and implemented: The *Opposite* injector configuration has a forward-biased injector and reversed-biased acceptor junctions opposite to each other and the *Side* configuration where two injection junctions are adjacent to the acceptor junction.

4.5.1.3.1 Opposite-injectors

Figure 4.7 shows that the opposite-injection SOI light source element has the forward-biased n^+p injector junction (interface between F and I regions) opposite to the reverse-biased n^+p acceptor junction (between R and I regions).

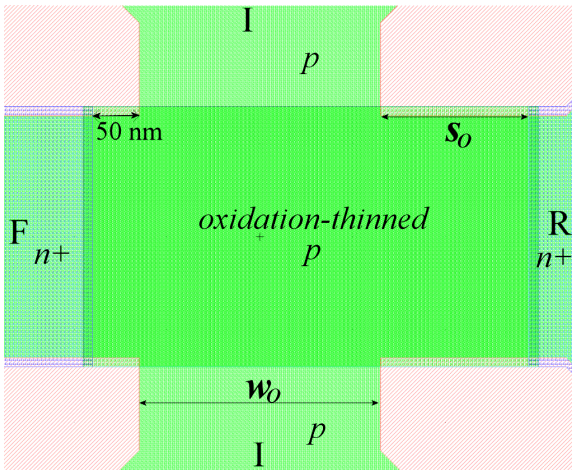


Figure 4.7. Opposite-injection SOI element layout dimension definitions.

It is expected that the reverse-bias depletion region extending from the R-I interface will stretch towards the forward-biased injector junction (F-I interface) from where it will receive cool electrons for radiative recombination with hot holes in its high electric field.

The dimensioning of the devices shown in Figure 4.7 had to comply with the following specifications to ensure proper functionality of the devices:

$$s_O \approx d_{Ox} + 3\Delta R_{\perp As} \approx 126\,\text{nm}, \tag{4.5}$$

$$w_O > w_d + \Delta Si, \tag{4.6}$$

where ΔSi is the Si thickness removed during the thinning oxidations. Equation (4.5) intends to advance the final (after all thermal processing) reverse-bias n^+ interface a distance s_O to the left, i.e. on the right side of the drawn intermediate (I) nodes. Relation (4.6) ensures that the final intermediate node widths are not completely covered by the reverse-bias depletion region so that the injector can still be forward-biased.

Single opposite-side injection elements are implemented in cells as shown in Figure 4.12, which allowed laying them out in interconnected arrays of 19 devices in parallel.

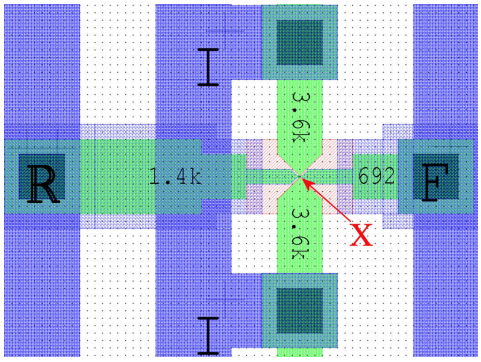


Figure 4.8. Single opposite-injector element layout on a 1-µm grid.

"X" demarcates the location of an injector type shown in Figure 4.7. R, F and I denote the reverse-biased acceptor, forward-biased injector and intermediate nodes respectively.

Table 4.7 lists the dimensions of the implemented opposite-side SOI injector light sources.

Table 4.7. Opposite-side injection devices pin-out.

Opposite-injectors				
Oxidized				
Dimension		s_O [nm]		
	Pin #	120	160	200
w_O [nm]	200	F: 11 I: 12	F: 14 I: 13	F: 15 I: 16
	260	F: 18 I: 17	F: 19 I: 20	F: 22 I: 21
	300	F: 23 I: 24	F: 26 I: 25	F: 27 I: 28
Non-oxidized				
Dimension		s_O [nm]		
	Pin #	120	160	200
w_O [nm]	200	F: 31 I: 32	F: 34 I: 33	F: 35 I: 36
	260	F: 38 I: 37	F: 39 I: 40	F: 2 I: 1
	300	F: 3 I: 4	F: 6 I: 5	F: 7 I: 8

The common reverse-biased node R of all devices is connected to pads 9 and 29.

Figure 4.9 shows how the nine differently dimensioned opposite-side injection light source arrays are arranged in a matrix.

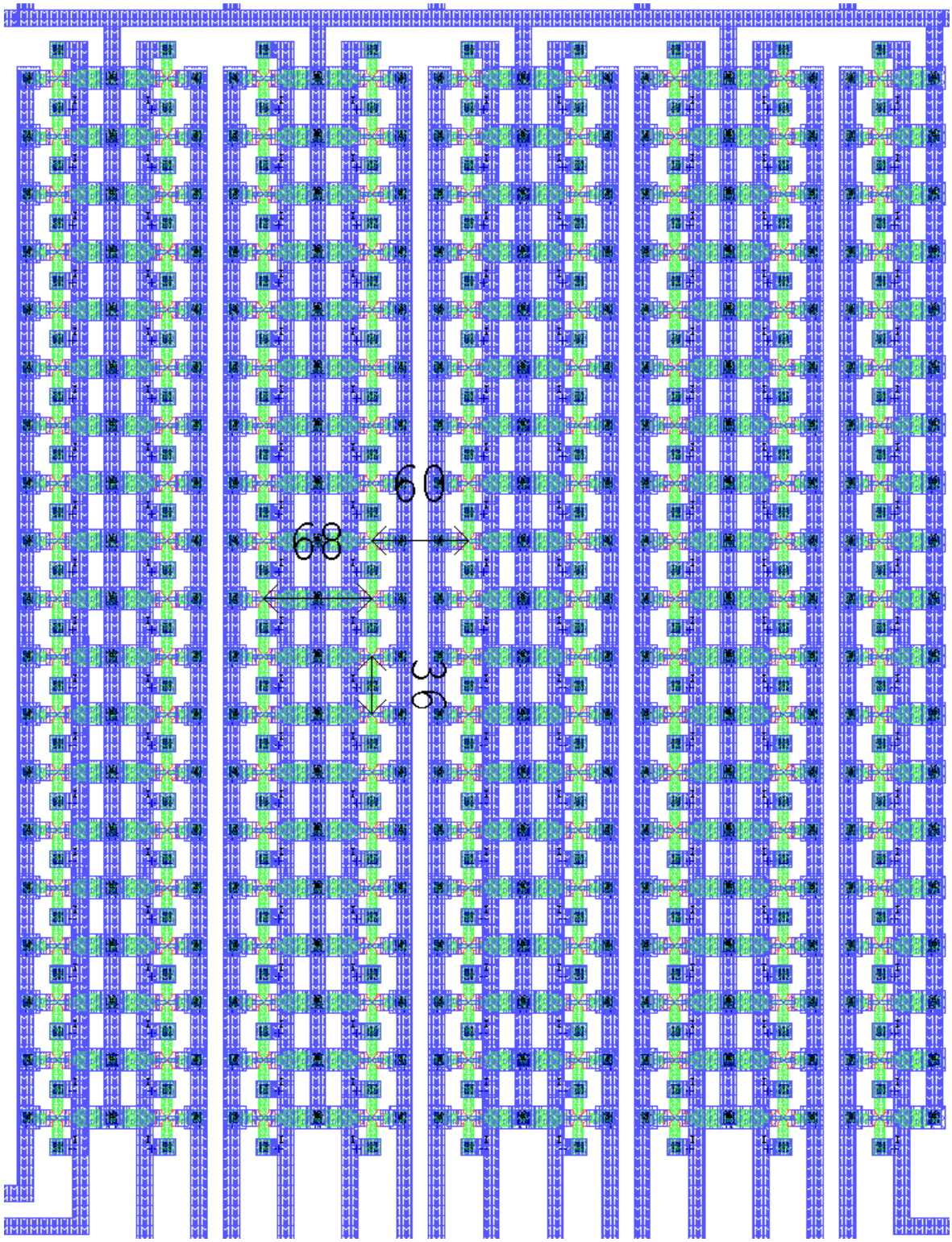


Figure 4.9. Nine columns of 19-element opposite-side injection device line-arrays.

Figure 4.10 shows *Chip3*, which contains the oxidized and non-oxidized opposite-side injection devices.

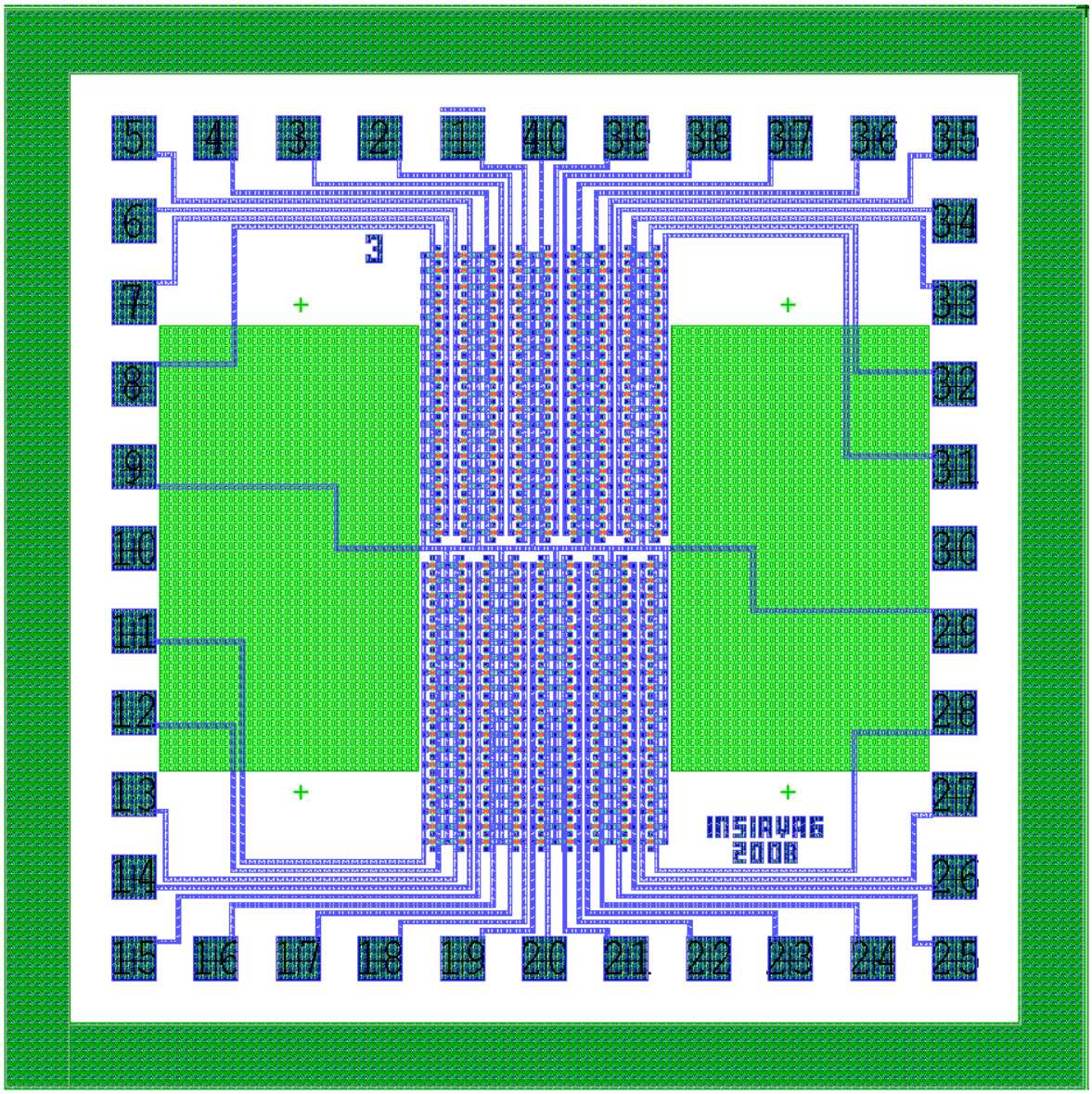


Figure 4.10. *Chip3* layout containing the *Opposite* injector light sources..

4.5.1.3.2 Side-injectors

As shown in Figure 4.11 the side-injection device has two injecting forward-biased junctions (F-I interface) adjacent to the reverse-biased acceptor junction (R-I interface).

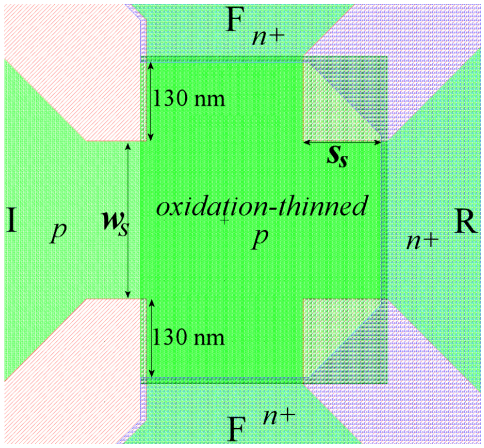


Figure 4.11. Side-injection SOI device layout dimension definitions.

The dimensioning of the devices shown in Figure 4.11 had to comply with the following specifications to ensure proper functionality of the devices:

$$s_S \approx d_{Ox} + 3\Delta R_{\perp As} \approx 86 \text{ nm and} \tag{4.7}$$

$$w_S = w + 2\Delta Si. \tag{4.8}$$

While relation (4.7) attempts to place the final reverse-biased R-I pn^+ acceptor interface a distance s_S to the left so that it borders in line with the right edge of the drawn forward-biased F-I injector interface, equation (4.8) intends to round the final Si strips.

The injection devices in Figure 4.11 are implemented in elemental cells as shown in Figure 4.12, which allowed laying them out in interconnected arrays of 19 devices in parallel.

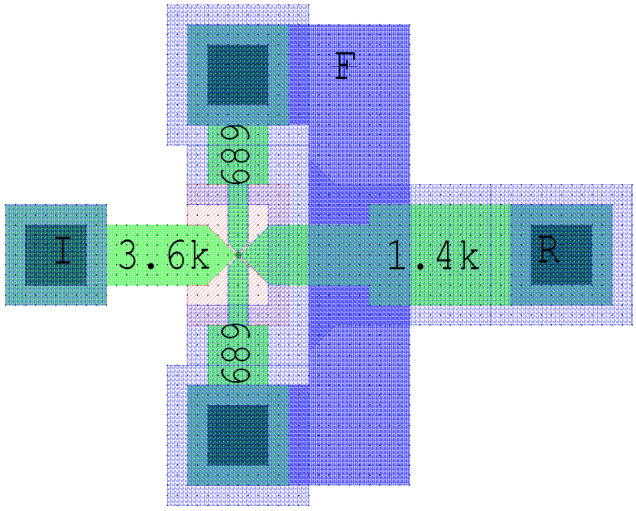


Figure 4.12. Single side-injection SOI injector element layout on a 1-µm grid.

Table 4.8 lists the dimensions of the implemented side-injection SOI light sources.

Table 4.8. Side-injection devices pin-out.

Side-injectors				
Oxidized				
Dimension		x_S [nm]		
	Pin #	50	90	130
w_S [nm]	200	F: 12 I: 11	F: 13 I: 14	F: 16 I: 15
	260	F: 17 I: 18	F: 20 I: 19	F: 21 I: 22
	300	F: 24 I: 23	F: 25 I: 26	F: 28 I: 27
Non-oxidized				
Dimension		x_S [nm]		
	Pin #	50	90	130
w_S [nm]	200	F: 32 I: 31	F: 33 I: 34	F: 36 I: 35
	260	F: 37 I: 38	F: 40 I: 39	F: 1 I: 2
	300	F: 4 I: 3	F: 5 I: 6	F: 8 I: 7

The common reverse-biased node R of all devices connects to pads 9 and 29 (Figure 4.13).

Figure 4.13 shows the layout of *Chip4*, which contains the oxidized and non-oxidized side-injection SOI light sources.

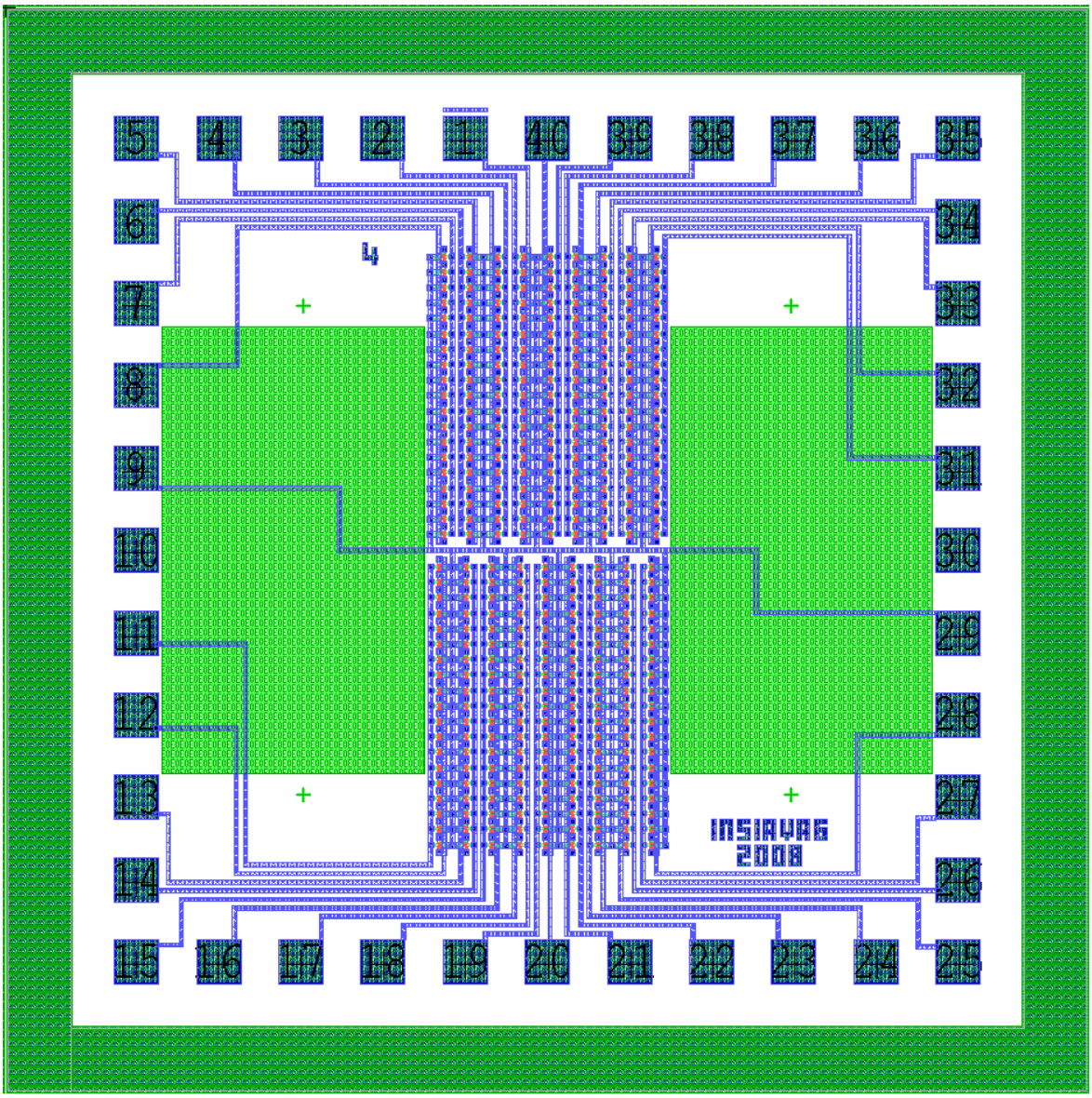


Figure 4.13. *Chip4* layout.

4.5.2. 1D-confined Comparison Light Sources

In parallel to the manufacture of the nanometre-scale SOI light sources, another SOI design (*INSiAVA1*) was manufactured entirely at the CEFIM. This test-chip did not make use of EBL or RIE processing steps and could only produce horizontally large (planar), but vertically thin SOI light sources.

For comparative purposes, some *INSiAVA1* avalanche and punch-through devices were implemented in this work. The implemented *INSiAVA1* devices are geometrically identical to *INSiAVA1* devices manufactured in the CEFIM clean-room, but exist in two variants: One version of *INSiAVA1* devices are oxidation-thinned to about 20 nm while the other set incorporates devices that remain at the initial silicon island thickness of about 150 nm.

4.5.2.1. n^+p Avalanche Light Sources

Figure 4.14 and Figure 4.15 show the dimensions of two *INSiAVA1* avalanche breakdown devices.

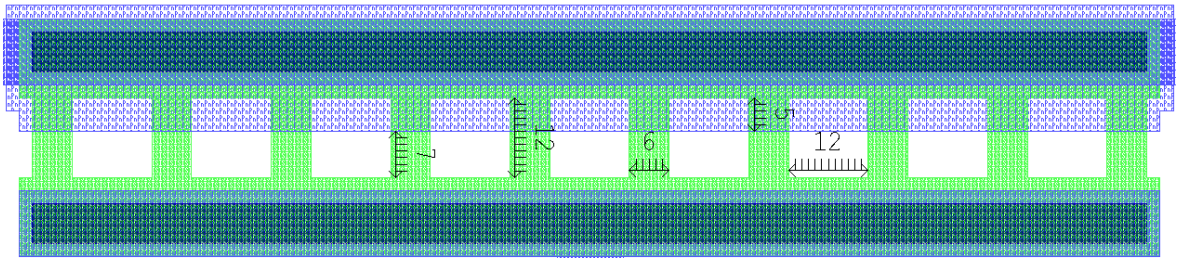


Figure 4.14. *INSiAVA1* n^+p avalanche breakdown device layout.

To possibly increase the light intensity with a higher electric field in a confined light generation area, the device in Figure 4.15 implemented triangular n^+ regions.

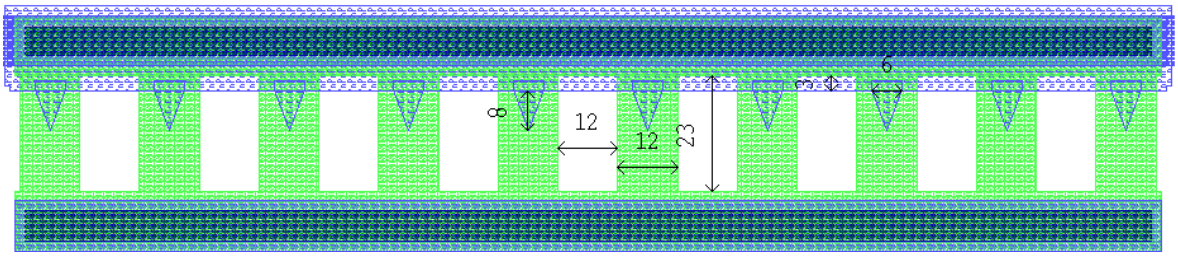


Figure 4.15. Triangular *INSiAVA1* n^+p avalanche breakdown device layout.

4.5.2.2. n^+pn^+ Punch-through Light Sources

Figure 4.16 and Figure 4.17 display the two types of *INSiAVA1* punch-through devices implemented.

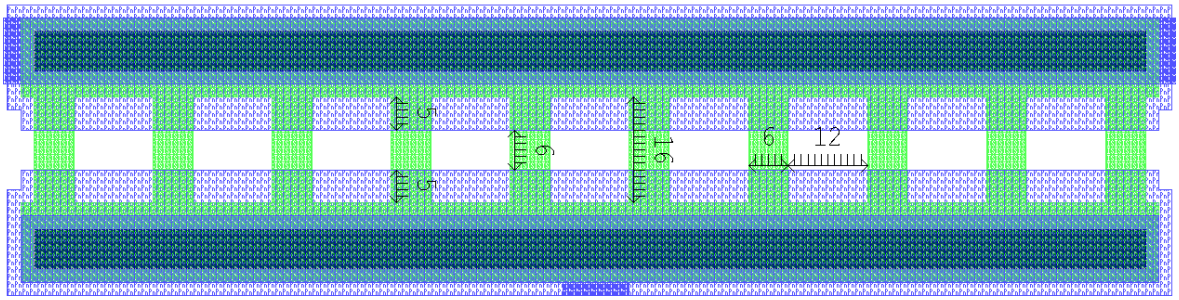


Figure 4.16. *INSiAVA1* n^+pn^+ punch-through device layout.

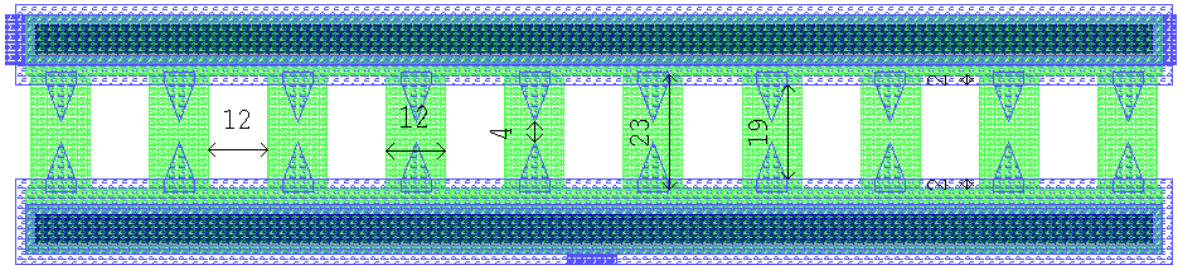


Figure 4.17. *INSiAVA1* triangular n^+pn^+ punch-through device layout.

4.6. Process Monitor Resistors

To measure process and material properties like finger thicknesses and doping concentrations, a matrix of n^+ and p resistor finger devices were included in the design. These resistors had similar dimensions to the avalanche-breakdown junction devices, but were either doped completely n^+ or p.

Figure 4.18 illustrates the process monitor resistor finger width w and length l definitions.

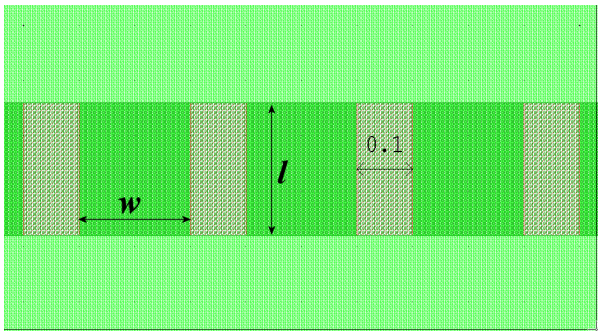


Figure 4.18. Process monitor resistor finger dimension definition.

Figure 4.19 shows a 100-finger process monitoring resistor device layout.

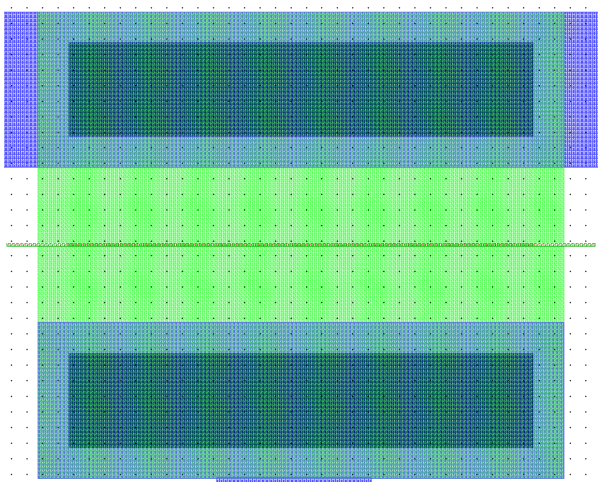


Figure 4.19. 100-finger process monitor resistor layout.

To enable the determination of doping concentration and thickness through resistive measurements, the n^+ and p resistors were each designed in two variants: While the one version had the fingers as shown above, the second version omitted the finger definition mask from the layout. In this way the resistance of various finger widths, as well as very wide, but thin silicon structures could be measured.

Figure 4.20 shows the configuration of the four different process-monitor resistor types.

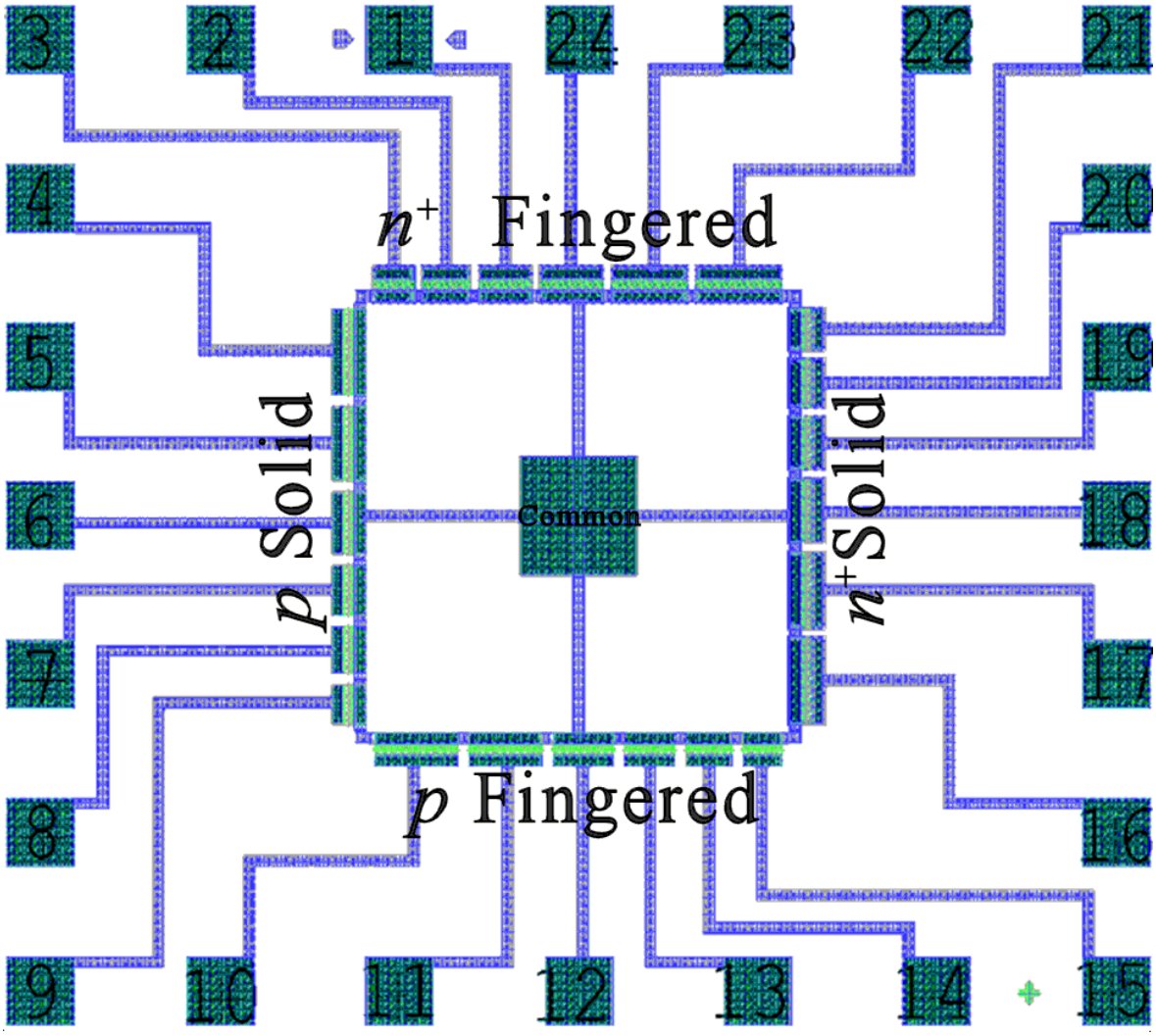


Figure 4.20. Process monitoring resistors.

Table 4.9 lists the dimensions and pin-out of all implemented resistor types.

Table 4.9. Implemented process-monitor resistors.

Chip No.	**Group**	**Device**	**Pin No.**	**Type**	**Oxidized?**	***w***	***l***
	Name					[nm]	
1 (*RsFramed*)	*RnOx*	*Rn200nmOx*	3	n^+	Oxidized	200	240
		Rn260nmOx	2			260	
		Rn300nmOx	1			300	
		Rn400nmOx	24			400	
		Rn500nmOx	23			500	
		Rn600nmOx	22			600	
	RnNoOx	*Rn200nmNoOx*	21		Not oxidized	200	
		Rn260nmNoOx	20			260	
		Rn300nmNoOx	19			300	
		Rn400nmNoOx	18			400	
		Rn500nmNoOx	17			500	
		Rn600nmNoOx	16			600	
	RpOx	*Rp200nmOx*	15	*p*	Oxidized	200	
		Rp260nmOx	14			260	
		Rp300nmOx	13			300	
		Rp400nmOx	12			400	
		Rp500nmOx	11			500	
		Rp600nmOx	10			600	
	RpNoOx	*Rp200nmNoOx*	9		Not oxidized	200	
		Rp260nmNoOx	8			260	
		Rp300nmNoOx	7			300	
		Rp400nmNoOx	6			400	
		Rp500nmNoOx	5			500	
		Rp600nmNoOx	4			600	

The common terminal to all above resistors is connected to a pad at the centre of the resistor cluster in Figure 4.20.

4.7. Alignment Markers

To achieve the required alignment accuracy when positioning the *Arsenic*, *Finger Spacing* and *Oxidation* masks relative to each other, EBL alignment marker crosses were initially etched into the SOI active layer and refined with the first EBL and etch step.

The marker in Figure 4.21 aligned *Finger Spacing* to *Si Island* and then the following EBL features to *Finger Spacing*.

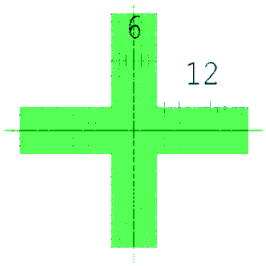


Figure 4.21. *AlignmentMarkerEBL* layout.

The marker in Figure 4.22 aligned *Oxidation (Photo)* to *Si Island*.

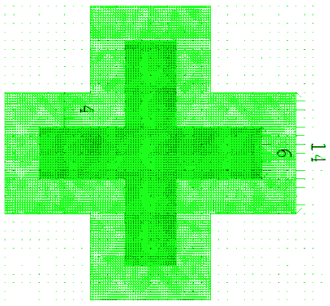


Figure 4.22. *AlignmentMarkerOx* layout.

The marker in Figure 4.23 aligned all photo masks, except *Oxidation (Photo)*, to *Si Island*.

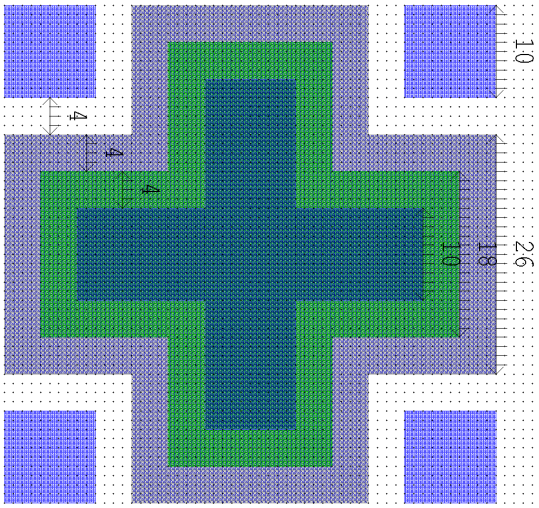


Figure 4.23. *AlignmentMarkerPhotoNoOx* layout.

4.8. Overall Layout

4.8.1. Chip1

Figure 4.24 shows the complete *Chip1* layout that contains the 1D-confined test-devices, the 2D-confined n^+p avalanche breakdown finger-junction light sources, some 2D-confined n^+pn^+ punch-through devices and all process-monitoring resistors

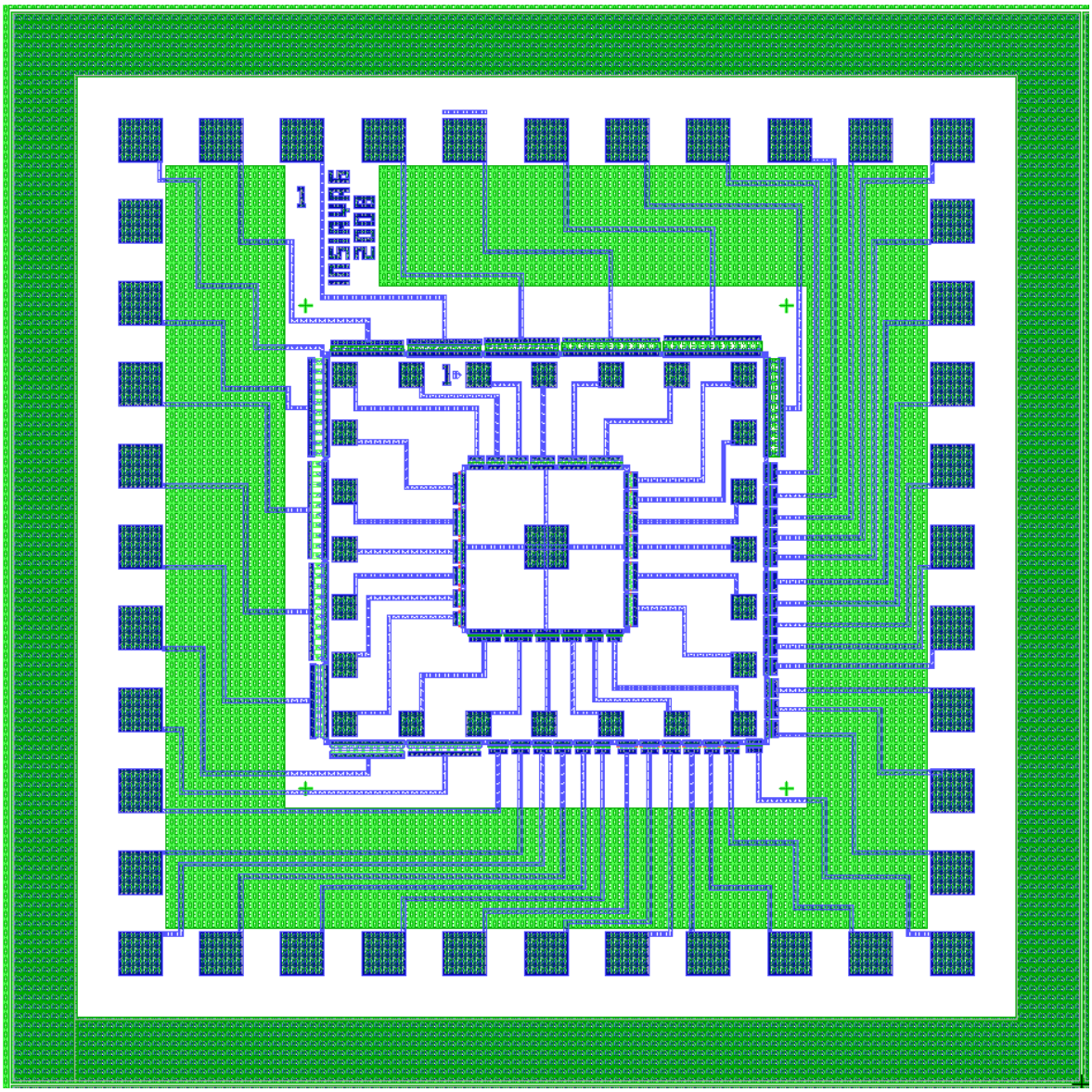


Figure 4.24. *Chip1* layout.

The other three chip layouts were already presented in the sections that described their constituent test devices.

Figure 4.24 depicts the complete four-chip test-cluster CAD layout that was used to manufacture the photolithographic masks and generate the EBL data files required by the JEOL JBX-9300FS electron-beam pattern generator EPG.

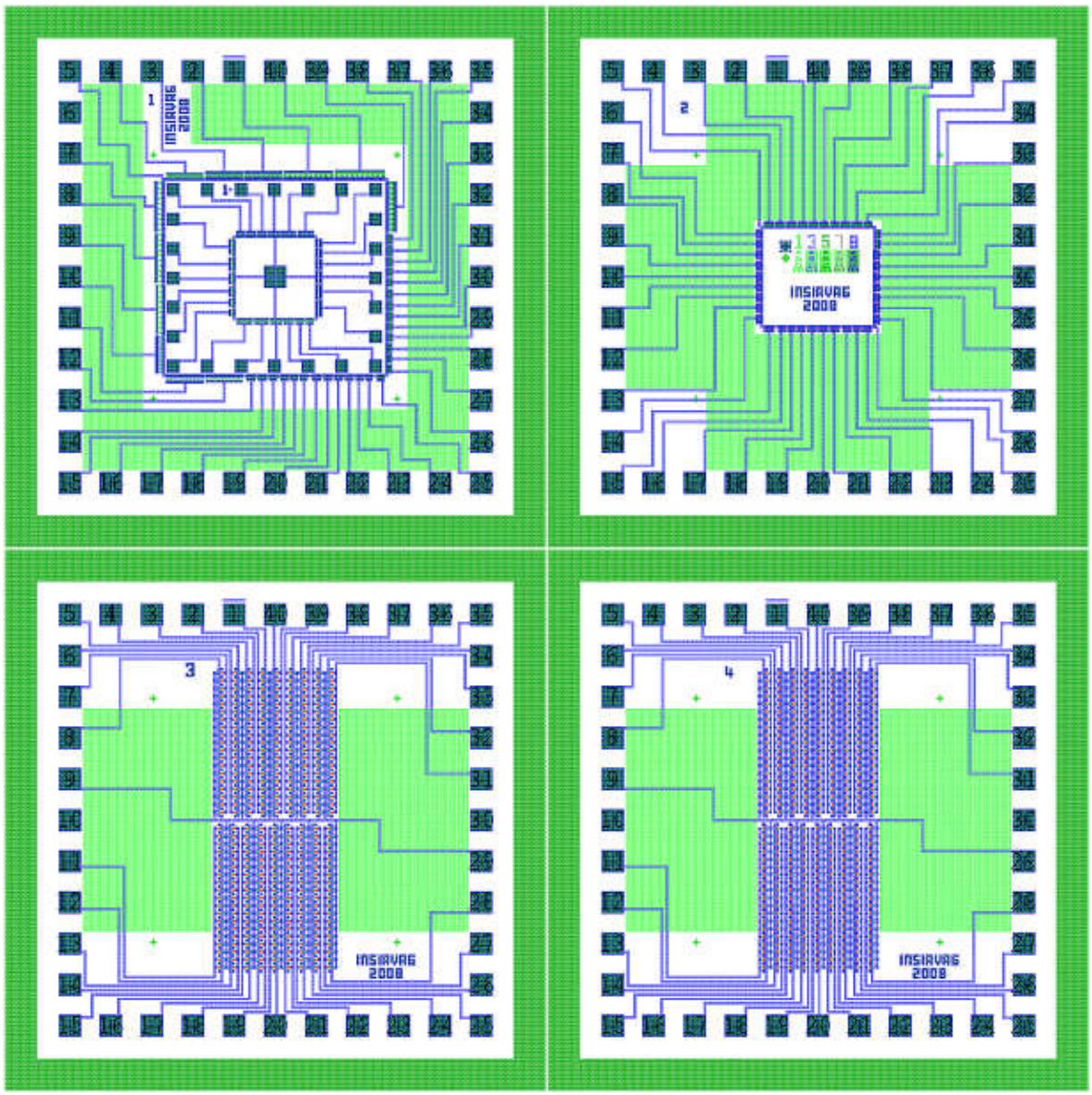


Figure 4.25 CAD layout showing the four chips in a 5.1 mm x 5.1 mm cluster.

Chip 1 in the top-left quadrant of the cluster contains 18 avalanche and 19 punch-through 100-finger SOI light source arrays, *Chip 2* (top right) contains 39 100-finger punch-through device arrays while *Chip 3* and *Chip 4* contain 36 19-element arrays of the two different injection light source types.

4.9. Photo-mask Layout

Figure 4.26 shows that 73 test-chip clusters fit on a 3-inch SOI wafer if 1.5 mm wide Si oxidation-monitoring areas are maintained between clusters.

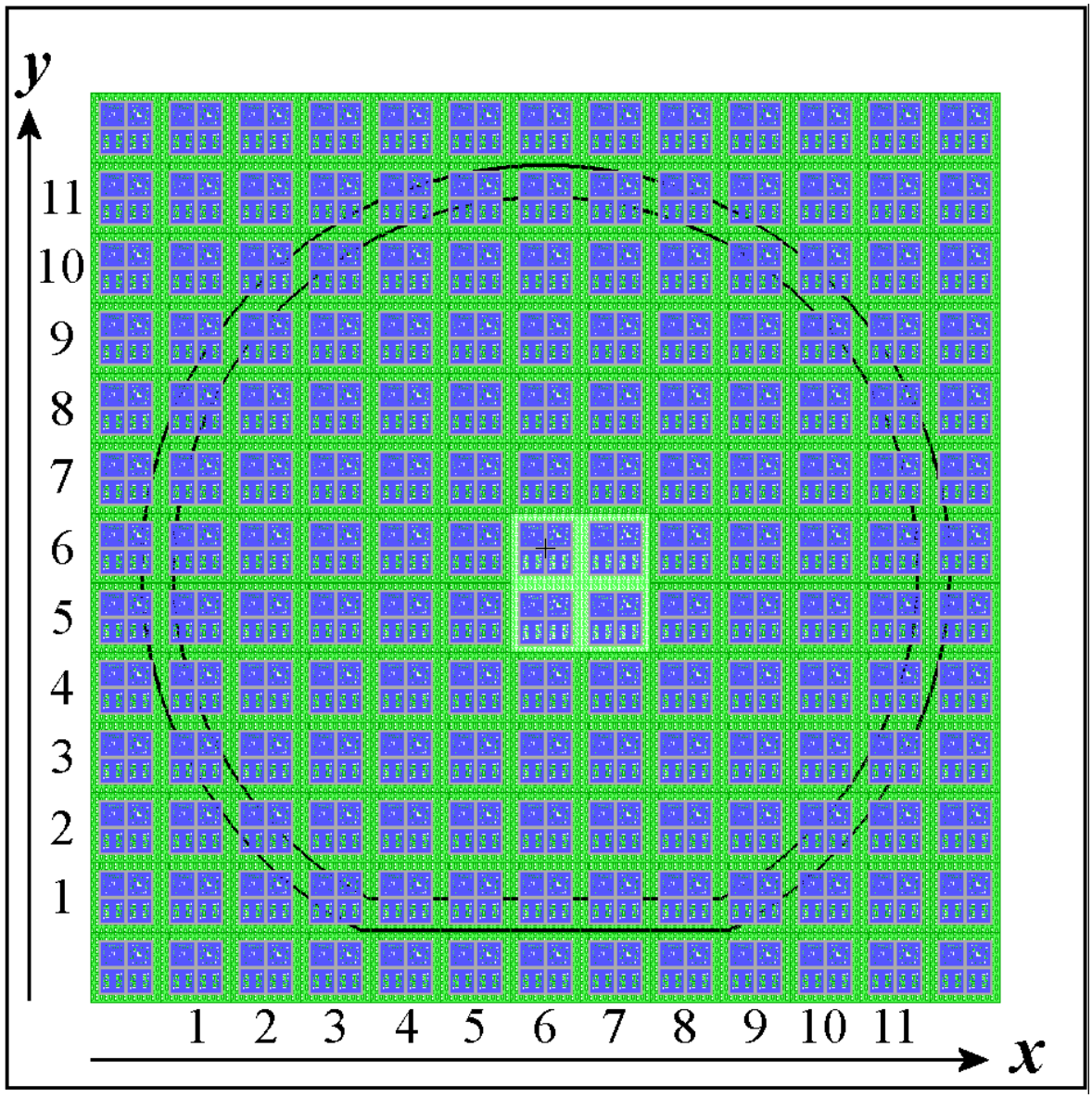


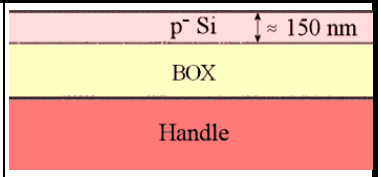
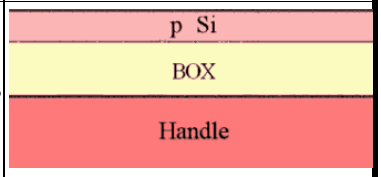
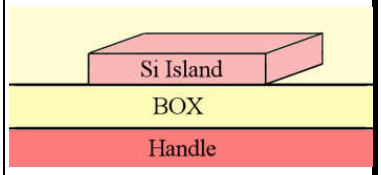
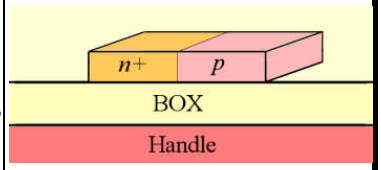
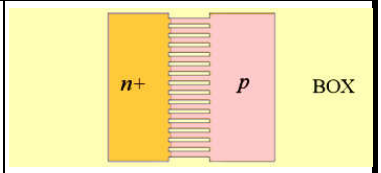
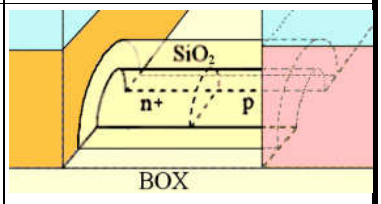
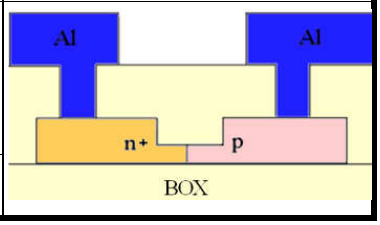
Figure 4.26. Layout and position denotation of the 73 test-chip clusters on a 3-inch wafer.

The four clusters in the approximate middle of the wafer (x = 6, 7; y = 5, 6) are the "*EBL clusters*" and are different from the surrounding "*Photo clusters*". While the *As* and *Oxidation* masks are duplicated on the photo and EBL masks (except for the omission of large oxidation control areas in the EBL files), the *photo-clusters* do not contain the 100 nm wide finger-spacing slits that could only be patterned through EBL.

5. MANUFACTURE

Table 5.1 gives a brief summary of the processing steps, equipment and facilities involved in the manufacture of the SOI light sources.

Table 5.1. Process flow overview.

Step	Section	Action	Equipment	Facilities	Graphical representation
1	5.1	Si thinning	Furnace, Reflective spectrometer	CEFIM, MiRC	
2	5.2	Blanket B implant	Ion implanter	Core Systems	
3	5.3	Si island definition	PECVD, Mask aligner, RIE	MiRC	
4	5.4	As implant	PECVD, EPG, Mask aligner, RIE, Ion implanter	MiRC, Core Systems	
5	5.5	Finger definition	EPG, RIE	MiRC	
6	5.6	Finger thinning oxidation	PECVD, EPG, Furnace	MiRC, CEFIM	
7	5.7	Metallization	PECVD, Mask aligner, Sputterer	CEFIM, Elume	
8	-	Si isolation spacing	Mask aligner	CEFIM	

Each of the manufacturing steps in Table 5.1 is discussed in more detail in the following subsections in the remainder of this chapter.

Since no standard process recipe was employable, the complete manufacturing process had to be designed on self-obtained equipment characterization data, material and chemical properties.

To ensure consistent results and confirm acceptable manufacturing performance, process control and monitoring was employed. This involved the simultaneous processing of monitor wafer pieces and the measurement of on-chip test-structures that could be analyzed with a SEM, a reflective spectrometer (to measure thin film thicknesses) and a profilometer.

The processing equipment was controlled by adapting machine-specific “recipe” variables like processing time, pressure, DC & AC (plasma) power, gas flows, etc.

5.1. Si Thinning

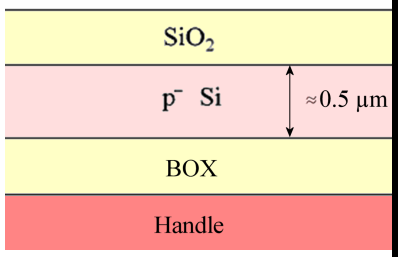
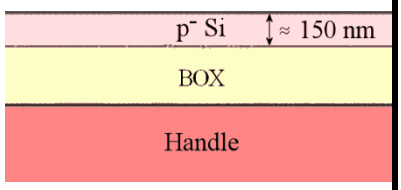
Since as shown in Table 4.1, the initial SOI wafer handle was too thick (0.5 µm ± 0.1 µm), the very first processing requirement was to thin down the SOI device layer. The requirements of the Si island thickness were:

1) The alignment marker thickness should be automatically recognizable by the EPG.
2) The step height from the BOX surface to the Si pad and contact area islands should not cause metal step coverage problems.
3) The difference between initial and final finger thickness (≈ 30 nm) should be easily be reduced through dry oxidation.
4) The Si island thickness should consider the possible handle thickness variation of about 100 nm so that that Si islands should remain after the thinning oxidation.

As a compromise to above requirements, it was decided to aim for an average Si island thickness of about 150 nm.

Table 5.2 lists the processing steps associated with thinning down the SOI wafer handle thicknesses down to about 150 nm.

Table 5.2. Si thinning processing steps.

Step	Action	Equipment	Material	Facilities	Graphical representation
1a	Si wet oxidation 1 h 48 Min @ 1050 ºC (oxidizes ~ 322 nm)	Furnace	H_2O	CEFIM / MiRC	
1b	SiO_2 etch	Fume hood	BOE		
1c	Measure t_{Si}	Reflective spectrometer Chemical scale	-		
Repeat steps 1a to 1c until t_{Si} of each wafer ≈ 150 nm					

The initial thinning oxidations were done in the CEFIM clean-room at UP. Since no reflective spectrometer was available and four-point probe measurements delivered vague Si thickness variation monitoring results during the oxidations, it was decided to use a highly sensitive chemical scale in the CEFIM clean-room to measure the change in wafer weight Δw_{Wafer} and use the wafer diameter D_{Wafer} (Table 4.1) and density of Si d_{Si} (Addendum A) in the relation

$$\Delta t_{Si} = \frac{\Delta w_{Wafer}}{\pi\left(\frac{D_{Wafer}}{2}\right)^2 d_{Si}}, \tag{5.1}$$

to determine the Si thickness Δt_{Si} removed during oxidation. Since Si was removed on both sides of the wafer, the Si device layer thickness reduction $\Delta t_{Device} = \frac{1}{2}\Delta t_{Si}$. Table 5.3 shows the estimated wafer thicknesses after wet oxidation in the CEFIM clean-room and which wafers were selected for further processing at the MiRC.

Table 5.3. Siegert SOI wafer thinning at CEFIM.

Wafer No.	**Start**	**After 1st oxidation** (60 Min wet)			**After 2nd Oxidation** (48 Min wet)				**Processed further at**
	w_{Wafer}		Δw_{Wafer}	Δt_{Device}	w_{Wafer}	Δw_{Wafer}	Δt_{Device}	$\Sigma\Delta t_{Device}$	
	[mg]			[nm]	[mg]		[nm]		
S1	**3616.24**	**3612.81**	**3.43**	**161**	**3609.66**	**3.15**	**148**	**310**	**MiRC**
S2	3632.64	3629.11	3.53	166	3625.95	3.16	149	315	CEFIM
S3	**3593.39**	**3589.85**	**3.54**	**167**	**3586.61**	**3.24**	**152**	**319**	**MiRC**
S4	3563.90	3560.36	3.54	167	3556.82	3.54	167	333	CEFIM
S5	**3605.66**	**3602.13**	**3.53**	**166**	**3598.82**	**3.31**	**156**	**322**	**MiRC**
S6	**3592.44**	**3588.92**	**3.52**	**166**	**3585.53**	**3.39**	**160**	**325**	**MiRC**
S7	3564.79	3561.26	3.53	166	3557.83	3.43	161	328	CEFIM
S8	**3609.29**	**3605.76**	**3.53**	**166**	**3602.46**	**3.30**	**155**	**321**	**MiRC**
S9	3630.30	3626.72	3.58	168	3623.40	3.32	156	325	CEFIM
S10	3647.60	3644.05	3.55	167	3640.69	3.36	158	325	CEFIM
MiRC Wafers **Max**	3616.24	3612.81	3.54	167	3609.66	3.39	160	325	=> $t_{Final} \geq$ 75 nm
Avg	3603.40	3599.89	3.51	165	3596.62	3.28	154	319	=> $t_{Final} \approx$ 181 nm
Min	3592.44	3588.92	3.43	161	3585.53	3.15	148	310	=> $t_{Final} \leq$ 290 nm
Δ [%]	0.66	0.66	3.13	3	0.67	7.32	7	5	

The five wafers to be processed further at the GT MiRC were optically selected to have the least thickness variation. This could be judged by counting the interference rings visible on the surface of the wafer.

Reflective spectrometer measurements at the MiRC showed that the SOI device layer thicknesses were in fact quite a bit thicker than estimated from wafer weights at the CEFIM. Table 5.4 shows the MiRC-measured SOI device layer thicknesses and the required oxidation times for each wafer to obtain the desired 150 nm layer thickness.

Table 5.4. Siegert SOI wafer thicknesses measured at the MiRC after oxidation at CEFIM.

		Measured									To be removed	After Removal		Desired t_{SiO2}	$T_{Oxidation}$ @ 1100 ºC
Wafer No.	**Measurement Set**	**BOX**	**Mid**	**N**	**E**	**S**	**W**	**Avg**	**Min**	**Max**		**Min**	**Max**		
		[nm]													
S1	1st	9795	312	460	392	259	260	338	258	461	**188**	70	273	426	49 Min
	2nd		308	459	387	258	279								
S3	1st	9829	280	211	291	340	167	261	167	340	**111**	56	230	251	21 Min
	2nd		260	229	331	317	180								
S5	1st	9811	444	408	401	467	417	432	393	468	**282**	111	186	640	1 h 37 Min
	2nd		463	409	393	468	448								
S6	1st	9826	525	560	436	423	513	497	423	599	**347**	76	252	789	2 h 19 Min
	2nd		536	599	439	430	512								
S8	1st	9763	299	348	258	295	392	316	258	392	**166**	93	227	376	40 Min
	2nd		297	349	282	293	343								
	Average	9805	372	403	361	355	351	369	167	599	219				

Above table also shows that the original device layer thicknesses averaged about 369 nm + 319 nm = 688 nm, which is above the maximum Siegert wafer thickness specification of 500 nm + 100 nm = 600 nm.

Table 5.5 shows the final measured silicon device-layer thicknesses after thermal oxidation in the Lindburg furnace.

Table 5.5. Wafer thicknesses after thinning oxidation (with aimed 150 nm average).

Wafer No.	**Thickness** [nm]								
	Centre	**North**	**East**	**South**	**West**	**Random**	**Min**	**Average** (Average – 150 nm)	**Max**
S1	124.8 129.9	255.8 273.9	174.2 188.2	44.8 50.2	63.6 77.3	106.6 143.6 112.5 133.5 107.6	44.8	**132.4** (-17.6)	273.9
S3	178.3 193.1	112.7 111.4	187.6 214.0	226.0 208.0	75.6 65.5	145.6 144.6 148.1 150.0	65.5	**154.3** (+4.3)	226.0
S5	152.1 154.4	139.9 133.5	119.5 162.0	173.3 197.7	171.6 167.8		119.5	**157.2** (+7.2)	197.7
S6	209.0 183.6	282.7 286.5	105.1 121.8	128.0 120.5	148.8 146.9		105.1	**173.3** (+23.3)	286.5
S8	138.2 118.0 131.6	186.3 216.3	102.6 98.7	105.3 120.5	148.7 157.7	123.3 132.1 104.0 132.8 100.1 148.3 144.3	98.7	**132.3** (-17.7)	216.3
Average	155.7	199.9	147.4	137.4	122.4	129.3	44.8	**149.9**	286.5

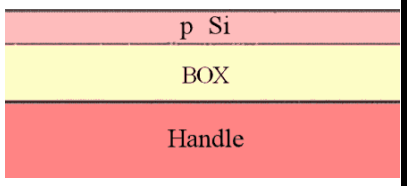
The average device-layer thicknesses are very close to the desired 150 nm, but *S1* and *S8* were about 18 nm thinner and *S6* was about 23 nm thicker than the desired 150 nm device layer thickness.

5.2. Blanket B Implant

Since the initial device-layer *p*-doping of $4 \cdot 10^{14}$ cm^{-3} of the supplied wafers (Table 4.1) was too low, a blanket B implant was necessary to achieve the desired impurity concentration of about 10^{18} cm^{-3}.

As shown in Table 5.6, the wafers had to be annealed after the B implantation at Core Systems[3] in California.

Table 5.6. Blanket B implant processing steps.

Step	Action	Equipment	Material	Facility	Graphical representation
2a	Blanket B implant $7 \cdot 10^{14}$ cm^{-2} @ 10 keV	Ion implanter	-	Core Systems	
2b	Annealing 30 Min @ 950 ºC	Tystar Furnace	N_2	MiRC	

The B implant was actually performed twice. The first implant ($7.24 \cdot 10^{14}$ cm^{-2} at 24 keV) occurred after the first oxidation thinning oxidation at CEFIM, but after receiving the wafers at the MiRC it was noticed that the first B implant was based on the erroneously derived Si thickness of about 181 nm. The resultant impurity concentration after Si thinning oxidation from about 369 nm to 150 nm was too low (see Table 5.7) and required another “top-up” B implant.

[3] Core Systems, A Subsidiary of Implant Sciences Corporation, 1050 Kiefer Road, Sunnyvale, CA

Table 5.7. 4-point probe measured SOI wafer resistivity and derived B doping.

Wafer No.	Resistivity										Doping N_A
	Centre	*North*	*East*	*South*	*West*	**Min**	**Avg**	**Max**	**Δ**		
	[Ω-cm]									[%]	[cm^{-3}]
S1	3.93E-1	3.74E-2	4.22E-2	2.34E-1	3.98E-1	3.74E-2	2.21E-1	3.98E-1	3.61E-1	163	8.27E+16
S3	1.79E-2	3.90E-2	2.06E-2	1.87E-2	1.97E-1	1.79E-2	5.86E-2	1.97E-1	1.79E-1	306	5.22E+17
S5	9.49E-2	1.98E-1	1.06E-1	7.91E-2	7.94E-2	7.91E-2	1.11E-1	1.98E-1	1.19E-1	107	2.14E+17
S6	9.11E-2	7.18E-2	2.12E-1	3.77E-1	1.16E-2	1.16E-2	1.53E-1	3.77E-1	3.65E-1	240	1.38E+17
S8	8.00E-2	6.28E-2	2.34E-1	1.45E-1	2.98E-2	2.98E-2	1.10E-1	2.34E-1	2.04E-1	185	2.17E+17
					Overall	1.16E-2	9.35E-2	3.98E-1	3.86E-1	413	2.73E+17

Wafers *S1*, *S3*, *S6* and *S8* (with average thickness of 144 nm) were sent to Core Systems for the top-up B implant. Wafer *S5* was arbitrarily chosen as a test-wafer with which to continue processing experiments.

Figure 3.1 shows that the average B concentration in the silicon is approximately reduced by a factor 45 during all oxidations (reducing the finger thickness from 150 nm to about 30 nm). This means that a final average B concentration of 10^{18} cm^{-3} (when the fingers are oxidized down to about 30 nm) requires an initial doping concentration of about $4.5 \cdot 10^{19}$ cm^{-3} when the fingers are still 150 nm thick. From Table 5.7 the geometrical mean B doping concentration of *S1*, *S3*, *S6* and *S8* was about $1.9 \cdot 10^{17}$ cm^{-3}. This means that the required implant dose $D = (4.5 \cdot 10^{19}\ cm^{-3} - 1.9 \cdot 10^{17}\ cm^{-3})(144\ nm) \approx 6.5 \cdot 10^{14}\ cm^{-2}$.

From Table 5.5 the implant energy is calculated for a range R_P equal to half the minimum Si thickness t_{Min}: $R_P = t_{Min}/2 = 44.8\ nm/2 = 224$ Å.

Data provided by Core Systems in Figure 5.1 shows that B ions implanted at their lowest acceleration energy of 10 keV penetrate to a range of about 400 Å, which was sufficient.

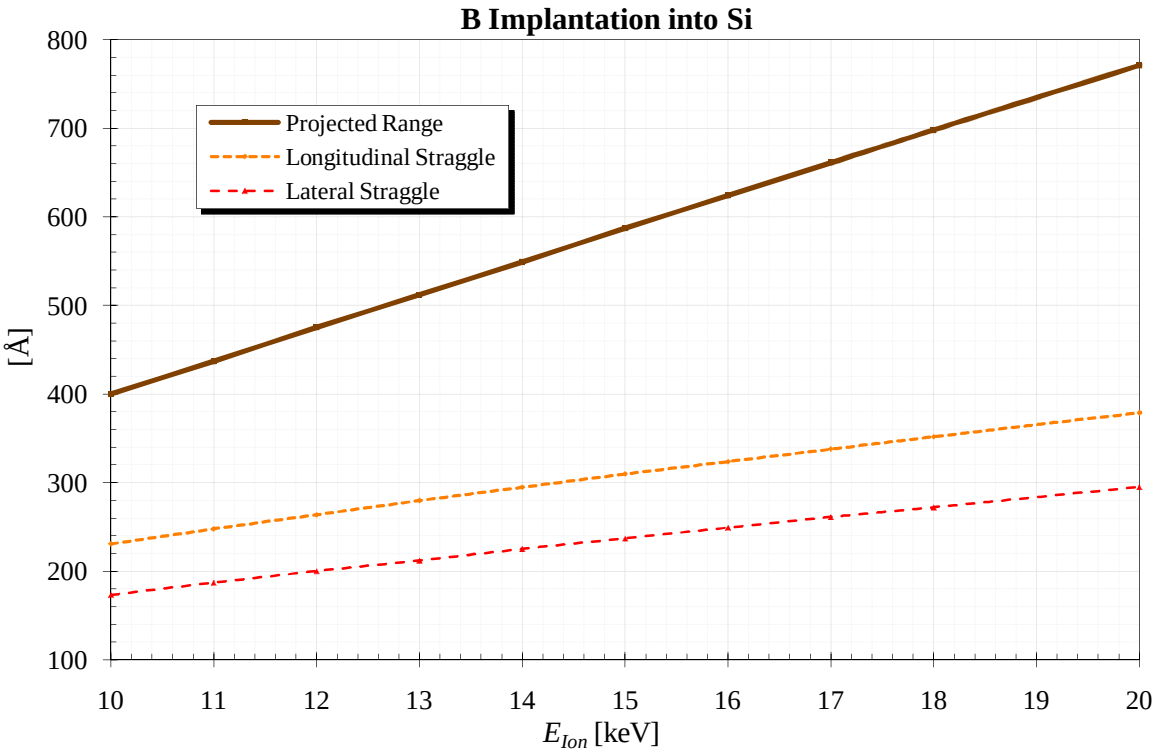


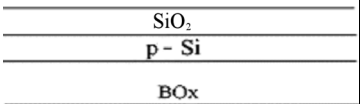
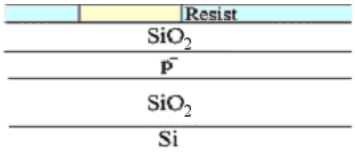
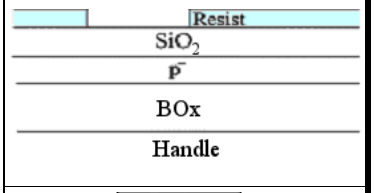
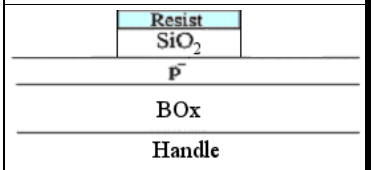
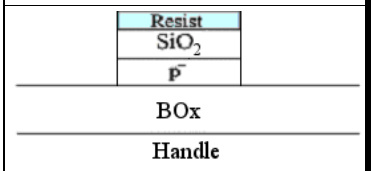
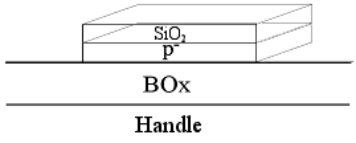
Figure 5.1. B implantation into Si range and straggle.

During wafer shipment to Core Implantation Systems in California for B implantation, wafer *S6* unfortunately broke and had to be excluded from subsequent processing.

5.3. Si Island Definition

Table 5.8 below shows the processing steps taken to create the Si islands on the BOX.

Table 5.8. Si island definition processing steps.

Step	Action	Equipment	Material	Facility	Graphical representation
3a	SiO_2 deposition 1 Min 20 s: 71 nm (Addendum D.3)	Unaxis PECVD	-	MiRC	
3b	Surface Dehydration (10 Min @ 120 ºC)	Oven	-		
3c	PR application (4 000 RPM: 1.2 µm)	Spin-coater	SC1813		
3d	Soft-bake PR (1 Min @ 115 ºC)	Hot-plate	-		
3e	Pattern transfer/ exposure ($t_{Exposure}$ = 3.6 s)	Karl Süss MA6 mask aligner	Si Island Photo-mask		
3f	Develop PR (1 Min)	Fume hood	FM319		
3g	Hard-bake PR (110 ºC, 30 Min)	Hot-plate	-		
3h	SiO_2 etch 5 Min: 71 nm (Appendix D.4.3.2)	Vision RIE	-		
3i	Si etch 2 Min: 286 nm (Addendum D.4.2.1)		-		
3j	PR strip	Fume-hood	10 Min Piranha 4:1 98 % H_2SO_4 : 30 % H_2O_2 560 ml + 140 ml = 700 ml		
3k	Wash wafers				

The first photolithographic Si island definition consumed three days due to problems with the Karl Süss MA6 TSA mask aligner. The initial photolithographic exposures were out of focus as shown in Figure 5.2.

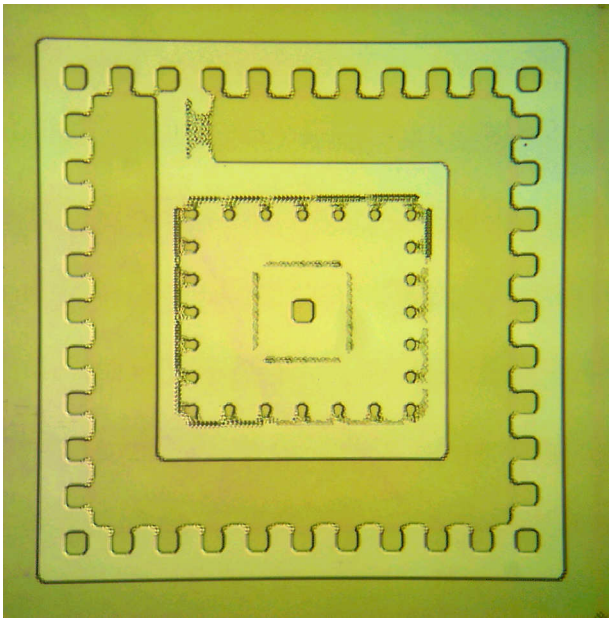


Figure 5.2. Bad *Chip1* Si Island exposure (step 3f).

After investigating many possible causes (including wafer warp and PR adhesion), it was found that the mask aligner had a cut in its wafer holder vacuum seal and that its wafer-holding screws were too far turned out for the thinner than usual Siegert SOI wafers. After faultfinding and fixing the mask aligner, decent photolithographic exposures, as shown in Figure 5.3, were achieved and subsequent photolithography was successful.

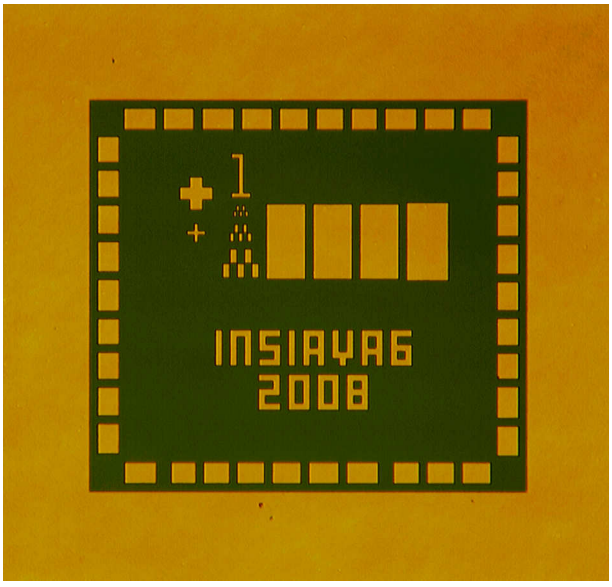
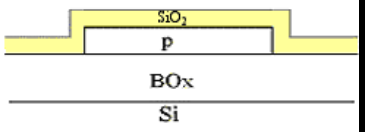
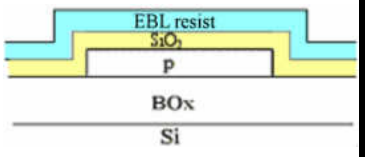
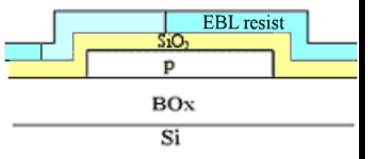
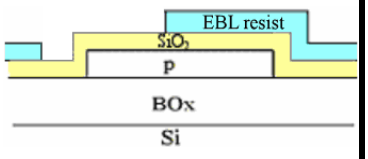
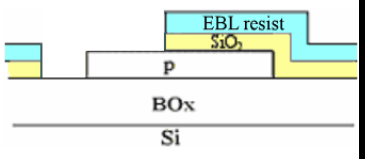
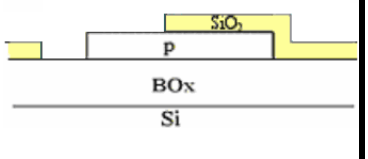


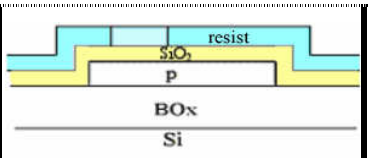
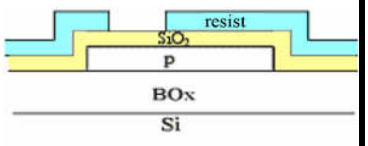
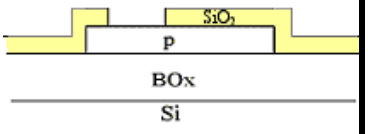
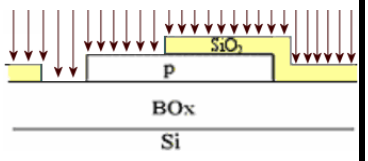
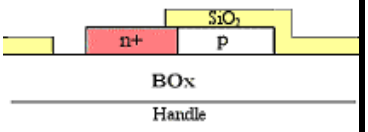
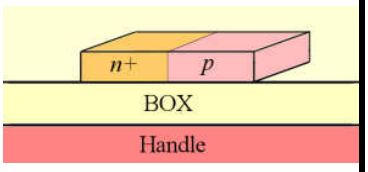
Figure 5.3. Proper *Chip2* Si Island exposure (step 3f).

5.4. As Implant

Table 5.9 lists the steps involved in implanting the As where n^+ diffusions are intended.

Table 5.9. Arsenic implantation processing steps.

Step	Action	Equipment	Material	Facility	Graphical representation
4a	SiO_2 deposition 3 Min 32 s: ≈ 200 nm (Addendum D.3)	Unaxis PECVD	Control wafer pieces	MiRC	
4b	Apply positive EBL resist (1 Min 2000 RPM: 500 nm)	Spin-coater	ZEP520A EBL resist		
4c	Soft-bake EBL resist (180 ºC for 2 Min)	Hot-plate	-		
4d	EBL exposure (200 µC/cm^2)	JEOL EPG	*As (EBL)* file		
4e	Develop EBL resist (2 Min)	Fume hood	Amyl Acetate		
4f	Wafer rinse (30 sec IPA immersion)		IPA		
4g	SiO_2 etch 13 Min: 210 nm (Addendum D.4.3.2)	Vision RIE	Control wafer pieces		
4h	ZEP de-scumming		O_2		
4i	Dehydration bake (10 Min @ 120 ºC)	Oven	-		
4j	PR application (4500 RPM: 1.1 um)	Spin-coater	SC1813		

4k	Pattern transfer exposure Mask EBL clusters with tape 4s	Mask aligner	As (Photo) mask	MiRC	
4l	Develop & hard-bake PR	Fume hood & oven	MF319 developer		
4m	SiO_2 etch (Si also etched!) 13 Min: 210 nm	Vision RIE	Control wafer pieces		
4n	PR removal & wafer clean	Fume-hood	Piranha H_2SO_4 & H_2O_2		
4o	As implant ($1.5 \cdot 10^{14}$ cm^{-2} @ 118 keV)	Ion implanter	As	Core Systems	
4p	Anneal 30 Min @ 950 ºC	AET RTP	N_2	MiRC	
4q	SiO_2 etch (Addendum D.2)	Fume hood	BOE		

Before the wafers could be sent to Core Systems for As implantation, holes had to patterned and etched into a SiO_2 masking layer that should be thick enough to prevent As from penetrating through it and reach the Si underneath it. Since it was determined that on some wafers an average of about 18 nm of the SiO_2 mask was not completely etched away in the n^+ implantation holes, it was decided to increase the As implantation acceleration energy to penetrate these thin SiO_2 layers.

Data supplied by Core Systems in Figure 5.4 shows that As implanted at E_{Ion} = 118 keV penetrates to a range Rp_{As_Si} of about 80 nm with lateral straggle $\Delta R\perp_{As\_Si}$ of about 18 nm.

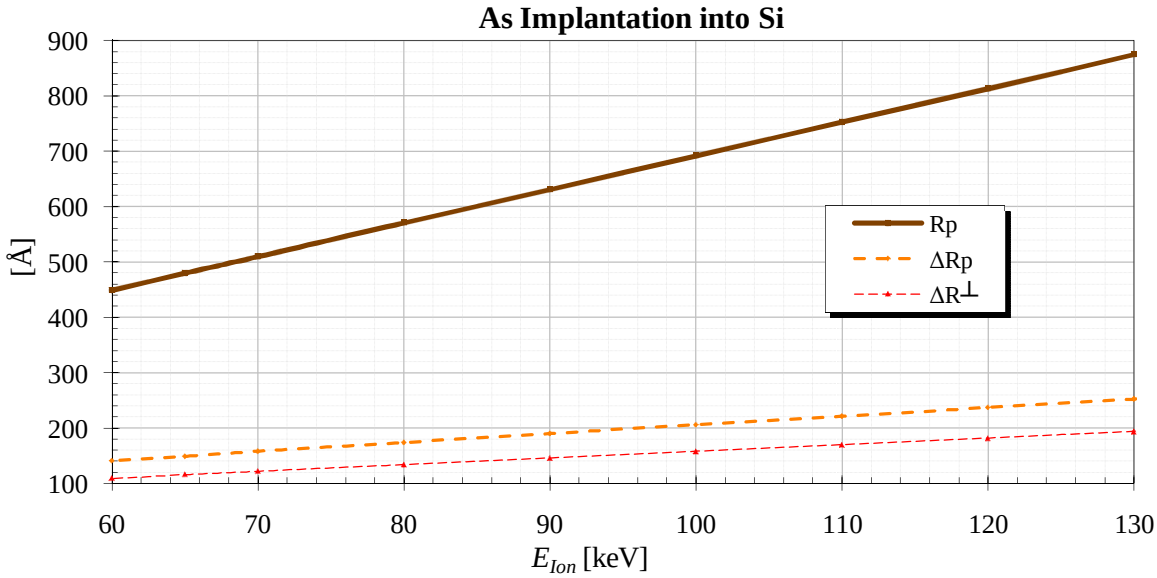


Figure 5.4. As implant range Rp_{As_Si}, longitudinal ΔRp_{As_Si} and transverse straggle $\Delta R\perp_{As\_Si}$ in Si.

Figure 5.5 shows that As implanted into SiO_2 at 118 keV will have a range of about 58 nm.

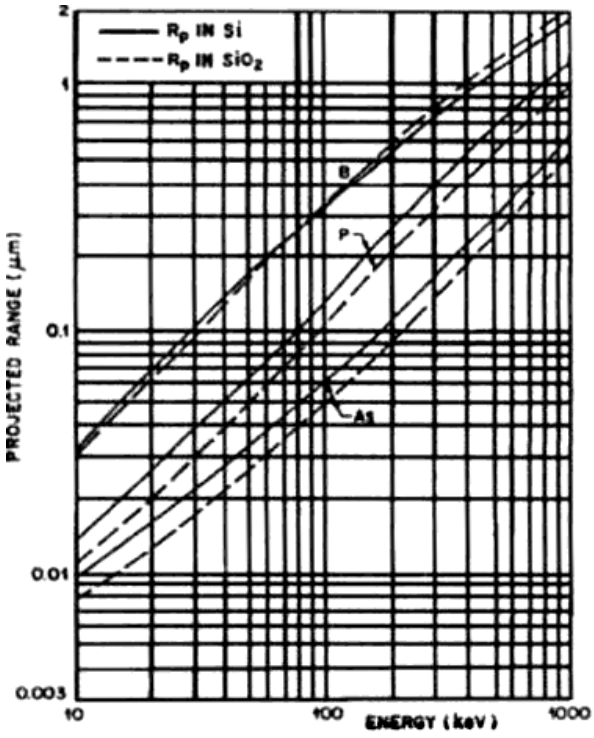


Figure 5.5. Projected ion implantation range Rp_{As_SiO2} in SiO_2 [91].

Since no straggle data was found for As implantation into SiO_2, it is assumed that a SiO_2 mask thickness of twice the projected range Rp_{As_SiO2} should be sufficient to block the As implant from reaching the underlying Si. Therefore $t_{SiO2} > 2Rp_{As\_SiO2}$ = 116 nm.

Figure 5.6 shows an *Opposite-injector* As mask pattern generated in the EBL resist during step 4f.

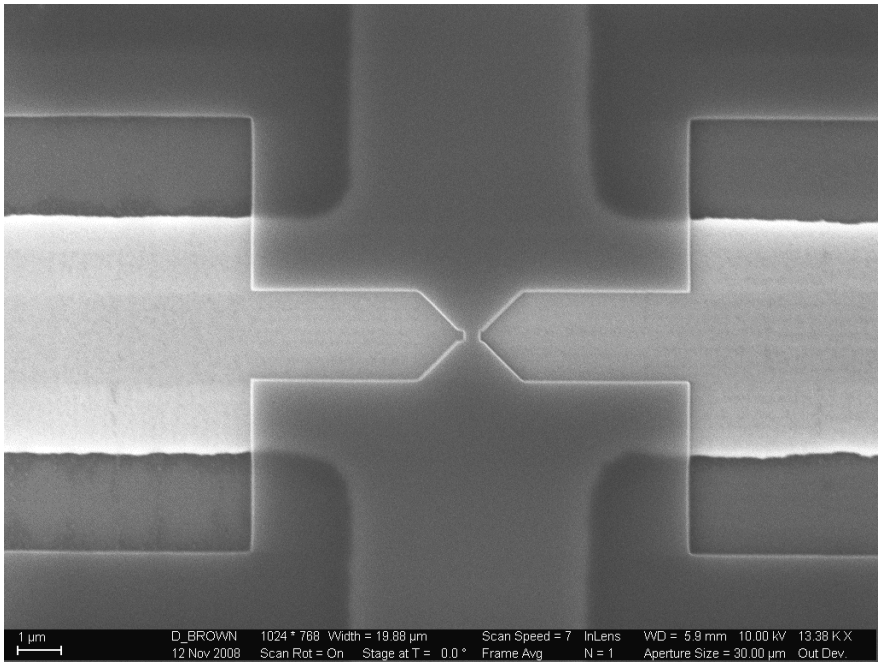


Figure 5.6. Arsenic EBL pattern in ZEP on oxide mask (step 4f).

Figure 5.7 shows the Arsenic mask spacing for the n^+pn^+ punch-through finger junctions after SiO_2 removal in the Vision RIE in step 4g.

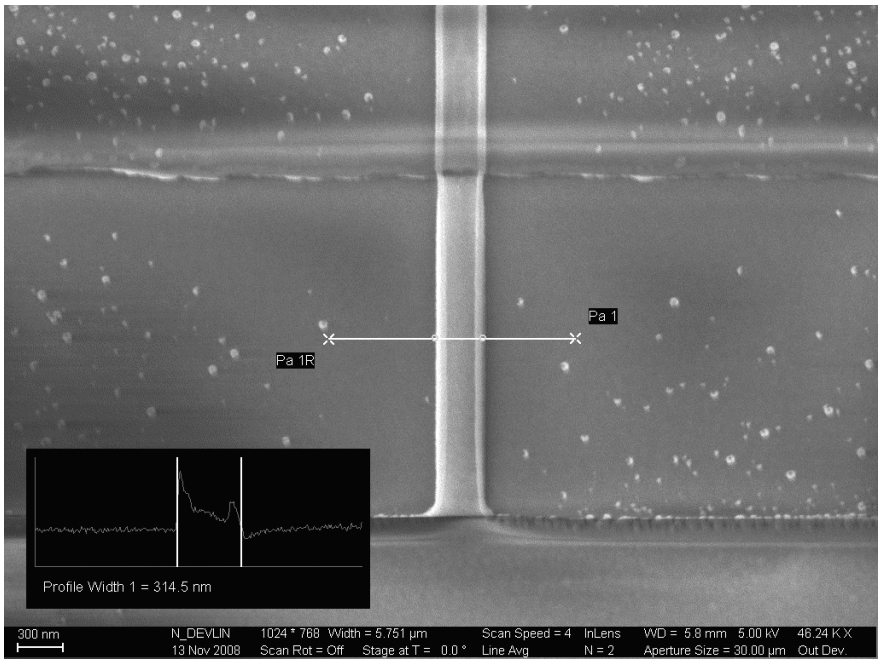


Figure 5.7. Arsenic EBL pattern after RIE (step 4g).

The 315 nm wide vertical stripe is the remaining SiO_2 that masks the intermediate region of the punch-through devices from the As implant.

Figure 5.8 shows an optical microscope image of patterned holes in the SiO_2 Arsenic masking layer at step 4h before Arsenic implant.

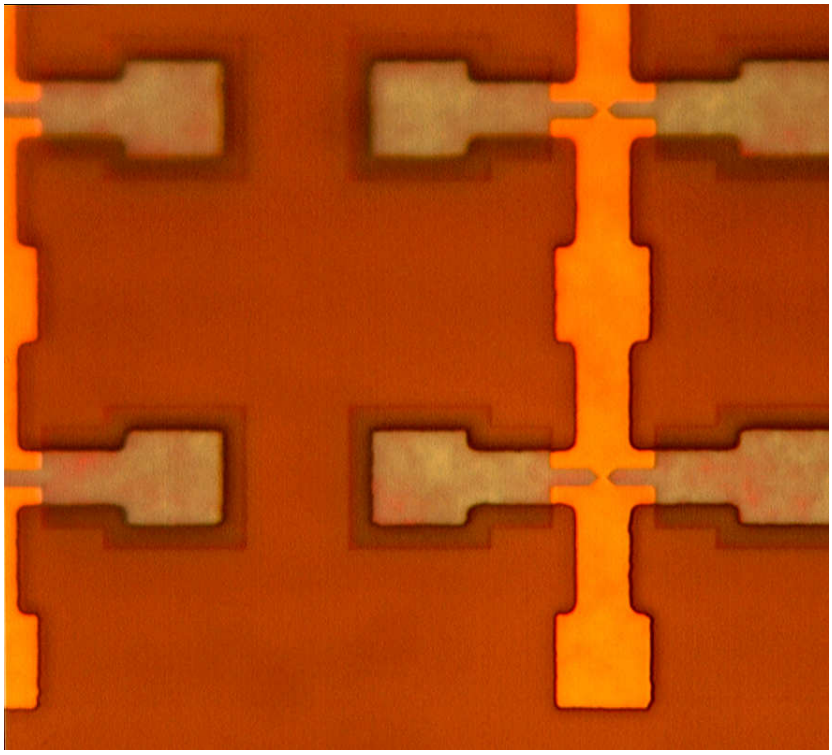


Figure 5.8. Arsenic EBL pattern before implant (step 4h).

Figure 5.9 shows the Arsenic implant holes etched into the SiO_2 mask generated by the photolithographic process at step 4m.

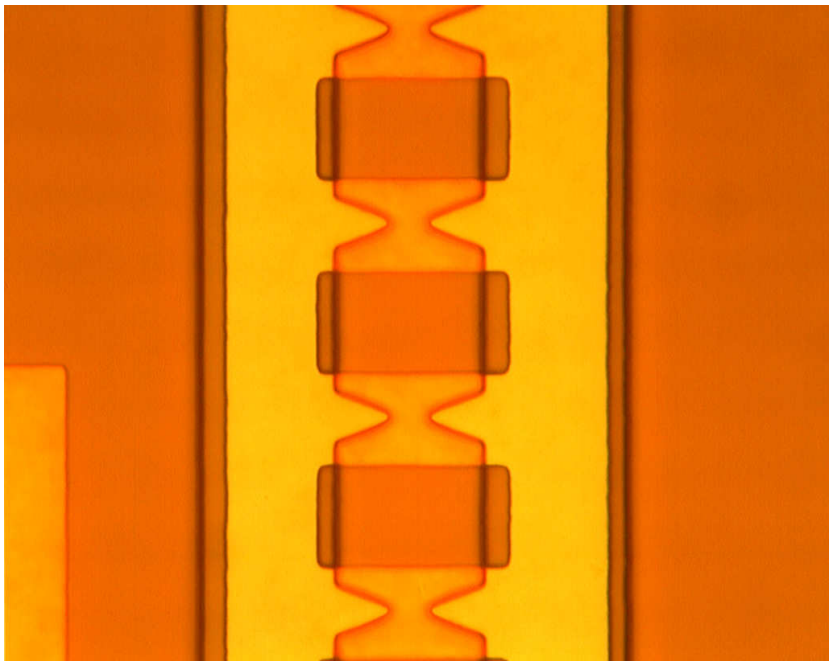
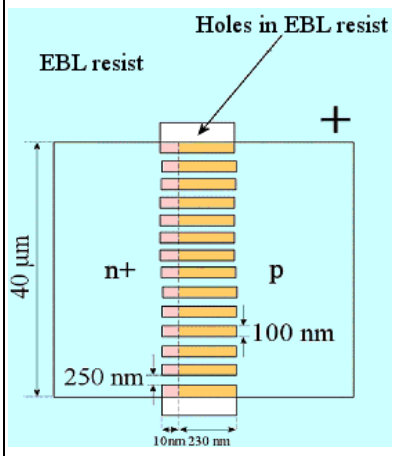
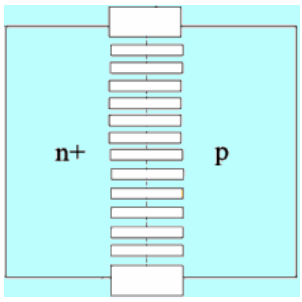
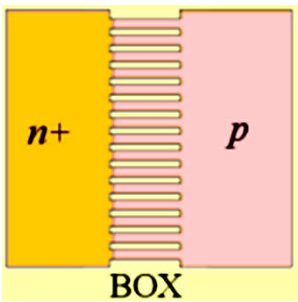


Figure 5.9. After Arsenic Photo RIE (step 4m).

5.5. Finger Definition

Table 5.10 shows the physical manufacturing steps involved in defining and etching the finger spacing strips into the Si.

Table 5.10. Finger definition process flow.

Step	Action	Equipment	Material	Facility	Graphical representation
5a	EBL: EBL steps 4b to 4h 600 nm ZEP Align to *Si Island* EBL marker (w_{Finger} = 2h_{Finger}, n_{Finger} = 100)	JEOL EPG	*Finger Spacing* EBL file	MiRC	
5b	Si etch	ICP	-		
5c	EBL resist removal	Vision RIE	O_2		
5d	Si finger width measurement	SEM	-		
5e	Wafer clean	Wet-bench	Piranha		

The SEM image in Figure 5.10 shows the finger spacing pattern in the ZEP EBL resist.

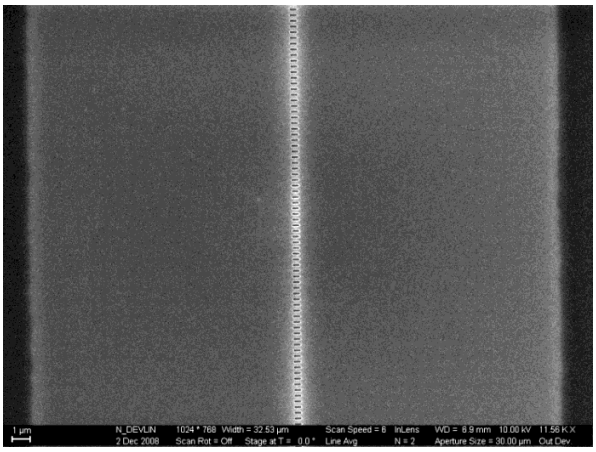


Figure 5.10. EBL finger spacing pattern (step 5a).

Figure 5.11 depicts a closer view of the EPG-written finger spacing pattern in the ZEP.

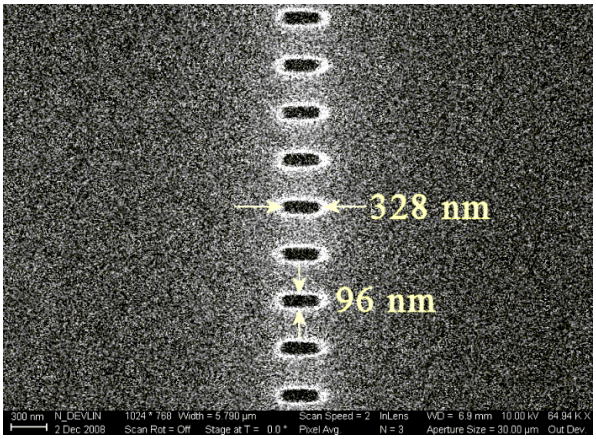


Figure 5.11. EBL finger spacing detail (step 5a).

Figure 5.12 shows the EBL-written ZEP holes that allow etching the superfluous Si away around the injector fingers.

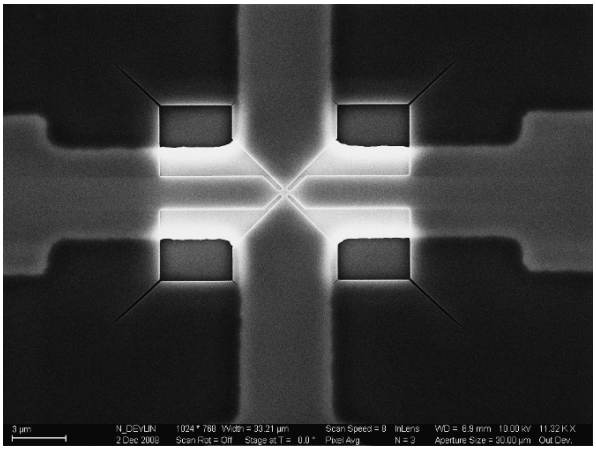


Figure 5.12. EBL injector spacing definition (step 5a).

The importance of characterizing the processing equipment to determine limitations and adapt the process accordingly can be illustrated by comparing the etch profiles of two different RIE systems.

While most oxidation and deposition steps delivered expected results, reactive ion-beam etching (RIE) on the recommended Vision Oxide RIE machine caused some uniformity and small-feature geometry etching variation problems. It was found that RIE etch rates were dramatically influenced by narrow masks and that dedicated etch and SEM cross-sectioning trial runs were necessary. Since the test designs, material and scanning electron microscope (SEM) availability were highly limited, this work had to rely on etch tests performed on a test wafer piece previously EBL-written by Devin Brown, the EBL specialist at the MiRC. Figure 5.13 shows that while the Vision Oxide RIE has an excellent etch selectivity towards Si when the ZEP EBL resist was used as a mask, its excessive horizontal etch-spread made it unsuitable for etching the 100 nm wide finger spacing slits.

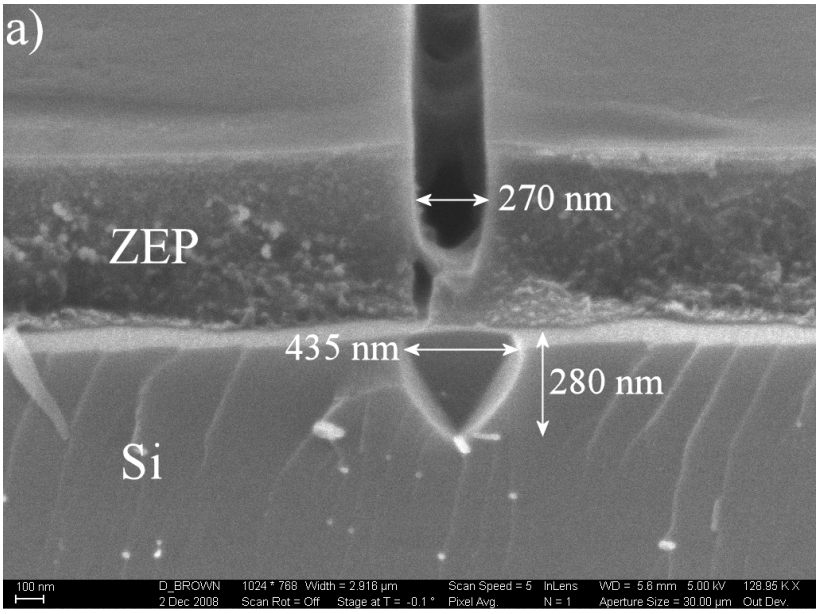


Figure 5.13. 100 nm Vision Oxide RIE Si groove etch test.

The Vision Oxide RIE is therefore not suitable for etching the 100 nm finger spacing slits into the Si since the resultant isotropic chemical etch width of up to 458 nm would completely remove the Si fingers. For this reason, the Plasmatherm ICP RIE, which was not included in the equipment training-program and was consequently not characterized extensively, had to be used.

Figure 5.14 shows that the PlasmaTherm ICP, which was eventually used for the finger spacing etching, exhibited a very narrow etch profile, but suffered from a relatively poor etch selectivity of only about 0.3.

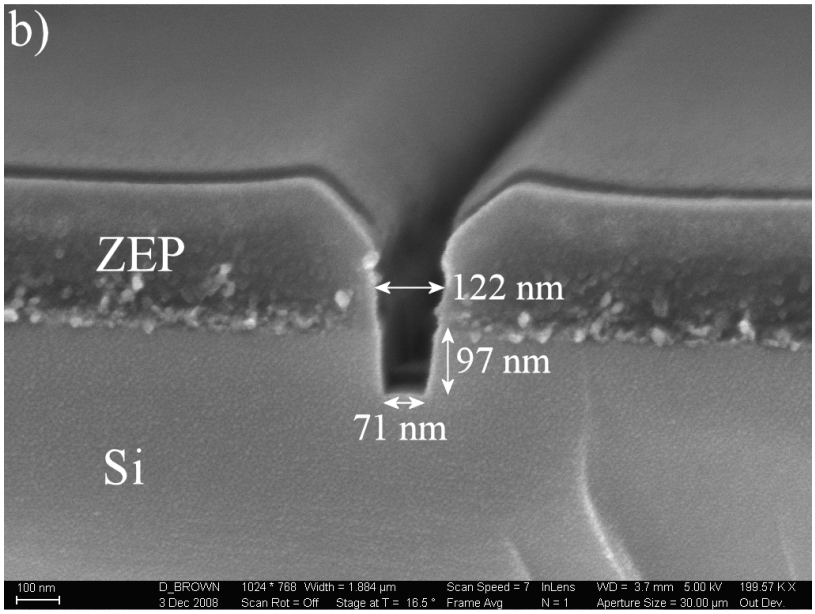


Figure 5.14. 100 nm ICP groove etch test.

The ICP could etch the 100 nm wide lines in the ZEP into about 71 nm wide and 97 nm deep grooves into the Si in 80 sec.

Figure 5.14 also shows the bad ICP etch selectivity of about 0.3. The etch selectivity is calculated as the etch rate ratio of desired material (in this case Si) to mask (in this case ZEP). The Plasmatherm ICP etched Si at an average rate of R_{Si} = 97 nm/80 sec = 73 nm/Min while removing the ZEP at the surface and sidewalls with an average rate of R_{ZEP} = (600 nm – 322 nm)/80 sec = 209 nm/Min. The ICP etch selectivity therefore is $R_{Si}/R_{ZEP} \approx 0.3$. Since the test-material used in above experiments had slightly different characteristics compared to the used wafers and the Plasmatherm ICP had a very low etch selectivity a best estimate etch time had to be compromised upon to etch sufficient silicon without completely removing the ZEP mask. It was decided that 2 Min 46 sec would only remove 582 nm of the 600 nm thick ZEP while still etching the thickest Si island thickness of 280 nm.

Due to Si island thickness variations, the finger definition ICP etch sufficiently formed all fingers but unfortunately the material around the injection devices was not completely removed before the ZEP EBL resist was also completely removed (see Figure 5.22).

The SEM image in Figure 5.15 shows the finger spacing holes ICP-etched into the Si that remained once the ZEP EBL resist was de-scummed after the finger definition RIE (before thinning oxidation).

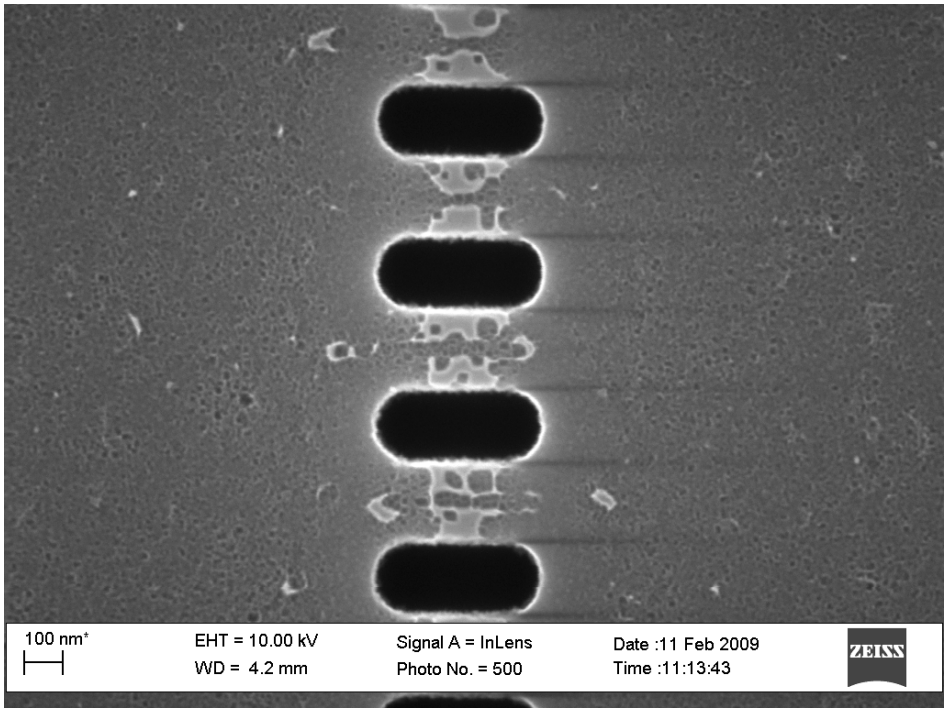


Figure 5.15. Finger spacing holes in the about 117 nm thick Si after RIE.

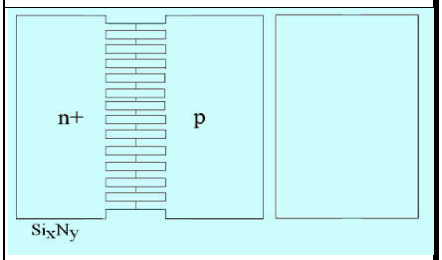
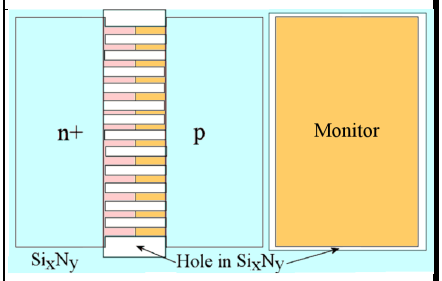
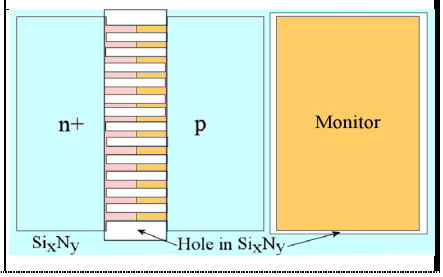
The device imaged above becomes a punch-through light source on wafer *S3*, cluster 1, *Chip 2*.

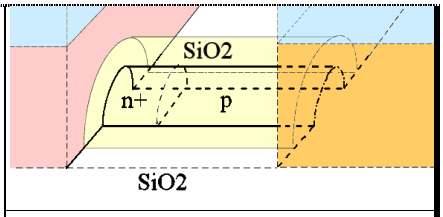
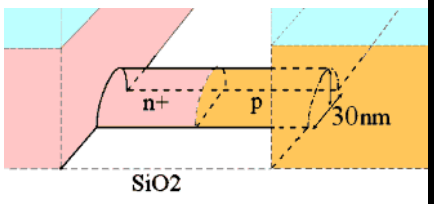
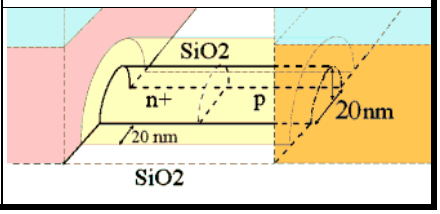
Although the EBL exposure and PlasmaTherm ICP etch resulted in rounded corners of the holes this is not critical to the junctions in the fingers.

5.6. Finger Thinning Oxidation

In the finger thinning oxidation processing steps in Table 5.11, the wafer was covered with a Si_xN_y masking layer. Oxidation windows were then etched into the Si_xN_y through which the Si fingers could be selectively oxidized thinner.

Table 5.11. Finger thinning oxidation process flow.

Step	Action	Equipment	Material	Facility	Graphical representation
6a	EBL data preparation	UNIX workstation	GDS data file	MiRC	
6b	Si_xN_y deposition Prior SiO_2 for adhesion 81 nm: 9 Min 52 s (Addendum D.3)	Unaxis PECVD	Chlorinated silane NH_3 Control pieces		
6c	PR application t_{SC1813} > 54 nm	Spinner	SC1813		
6d	Photolithography (see steps 3c to 3g)	Mask aligner	*Oxidation* photo-mask		
6e	Nitride etch 1 Min 6 s	Vision RIE	-		
6f	PR removal & wafer clean	Wet-bench	Piranha		
6g	Measure Si finger Width & height	Profilometer	-		
6h	Measure $w_{SiFinger}$	SEM	-		
6i	EBL (see steps 4b to 4h)	JEOL EPG	*Oxidation* EBL- file		
6j	Nitride etch 1 Min 20 s	Vision RIE	-		
6k	ZEP descum				

6l	Dry Si oxidation 27 Min @ 970 ºC $t_{SiO2} \approx 63$ nm; $\Delta t_{Si} \approx 28$ nm	Furnace	H_2O	CEFIM	
6m	Remove SiO_2 100 nm/Min (Addendum D.2)	Fume hood	BOE		
6n	Measure $w_{SiFinger}$ deduce $h_{SiFinger}$	SEM	-		
Repeat steps 6l to 6n until $h_{SiFinger} = w_{SiFinger} \sim 30$ nm					
6o	Dry Si oxidation 1 h 2 Min @ 970 ºC $h_{SiFinger} = 20$ nm $t_{SiO2} \approx 95$ nm	Furnace	O_2		

The thinning oxidation process parameters were determined with the help of the theory described in section 2.3.1 and the collected oxidation characterization data in Figure D.3.

Since the Si_xN_y mask deposited in step 6b will be the final passivation layer on light sources that are not oxidation-thinned, the thickness of the Si_xN_y layer can be set for maximum light transmission from the Si light source through the Si_xN_y into the air above. Employing the light transmission model derived in section 2.2.3.2, Figure 5.16 shows that maximum silicon-Si_xN_y-air light transmission for λ = 650 nm is achieved with a Si_xN_y thickness of 81 nm.

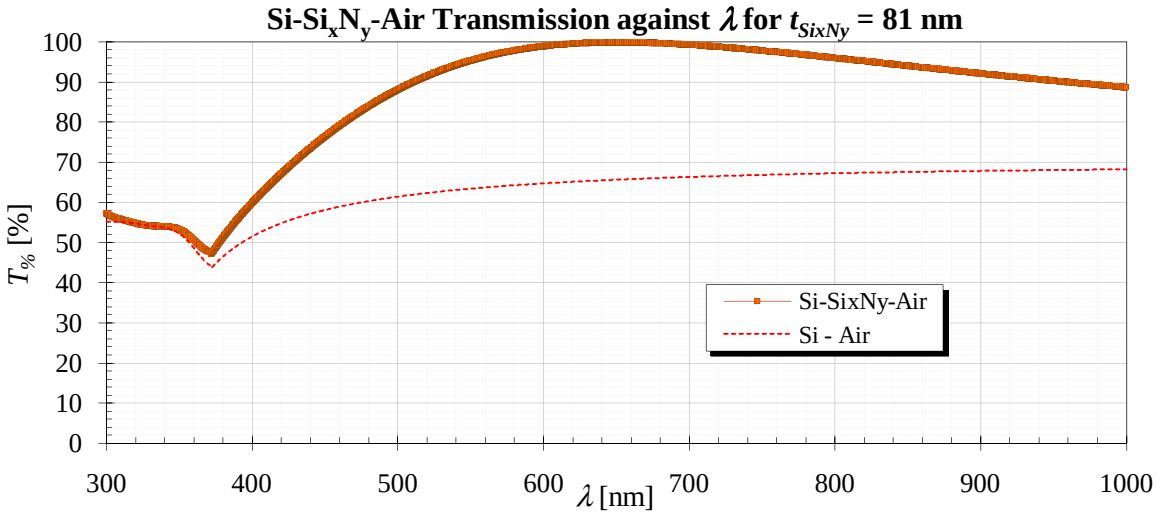


Figure 5.16. Si-Si_xN_y-air transmission at t_{SixNy} = 81 nm.

Figure 5.17 shows that the maximum overall silicon-Si_xN_y-air light transmission for 300 nm $\leq \lambda \leq$ 1 µm is realized with a Si_xN_y thickness of about 65 nm.

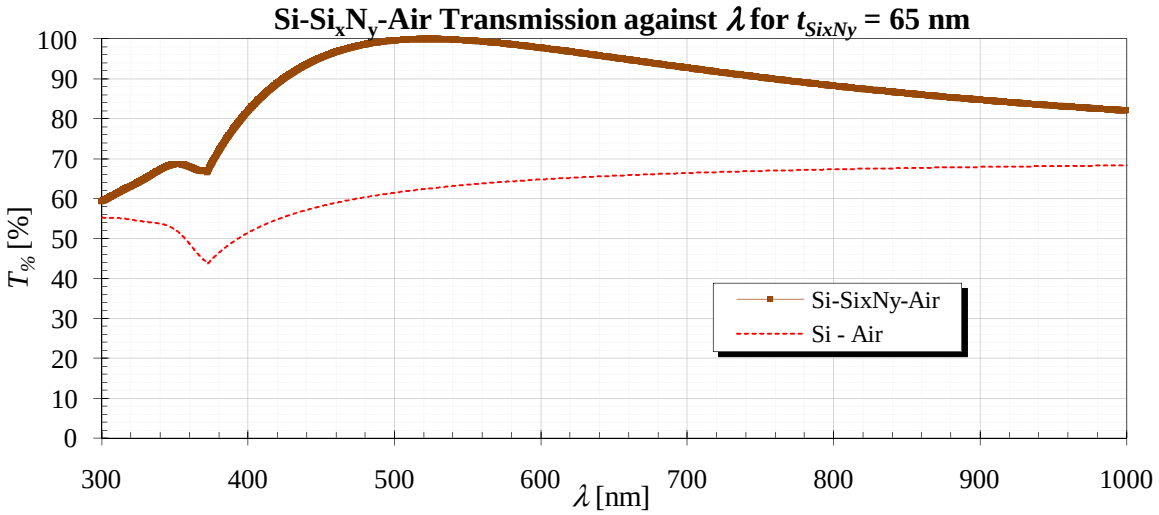


Figure 5.17. Si-Si_xN_y-air transmission at t_{SixNy} = 65 nm.

For maximum external light emission efficiency, the PECVD-deposited Si_xN_y thickness should therefore be between 65 and 81 nm. As described in section 2.2.3.2 adding a SiO_2 or Si_xN_y layer with refractive index between Si and air improves the light transmission over the Si-air interface transmission shown as a dotted line in Figure 5.16 and Figure 5.17.

Figure 5.18 shows the oxidation windows in the nitride over the wide 1D-confined Si fingers created through photolithography after step 6e.

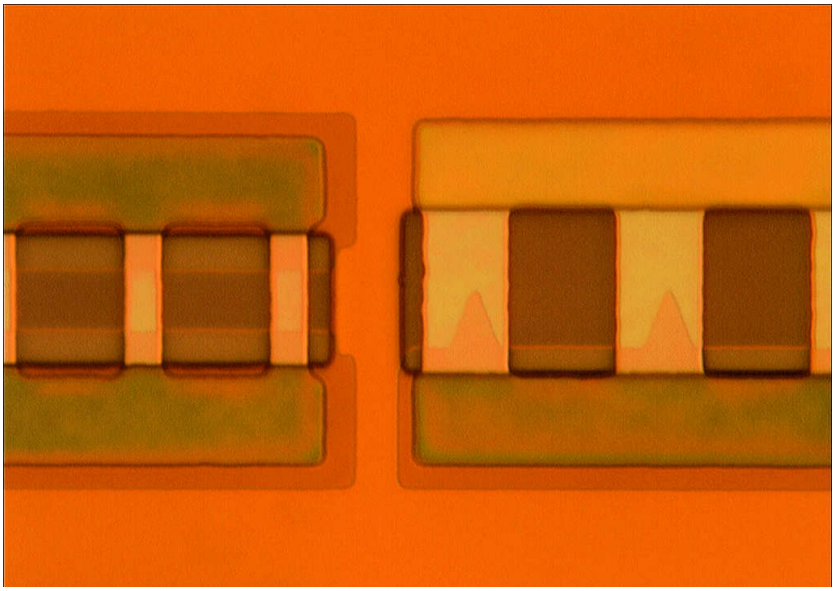


Figure 5.18. 1D-confined devices after finger oxidation (photo) RIE (step 6e).

The Si_xN_y oxidation window is visible as a darker box spreading across the fingers.

The SEM photo in Figure 5.19 shows the EBL-written oxidation windows in the Si_xN_y covering the Si finger devices as white lines in the top row and two top-most devices in the right row.

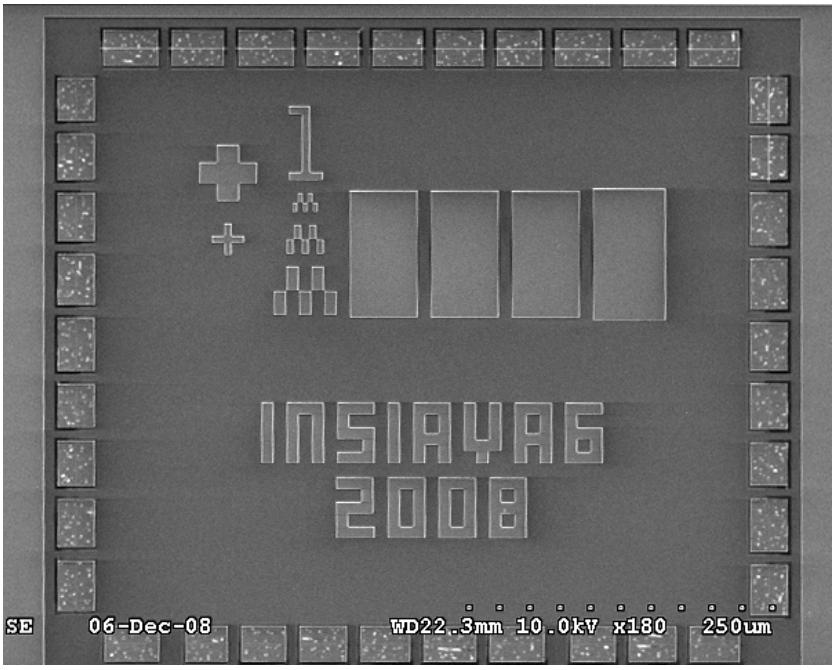


Figure 5.19. *Chip2* after oxidation EBL de-scum (step 6k).

The SEM image in Figure 5.20 shows the finger oxidation window overlaying the Si fingers (before thinning oxidation) as a bright horizontal band.

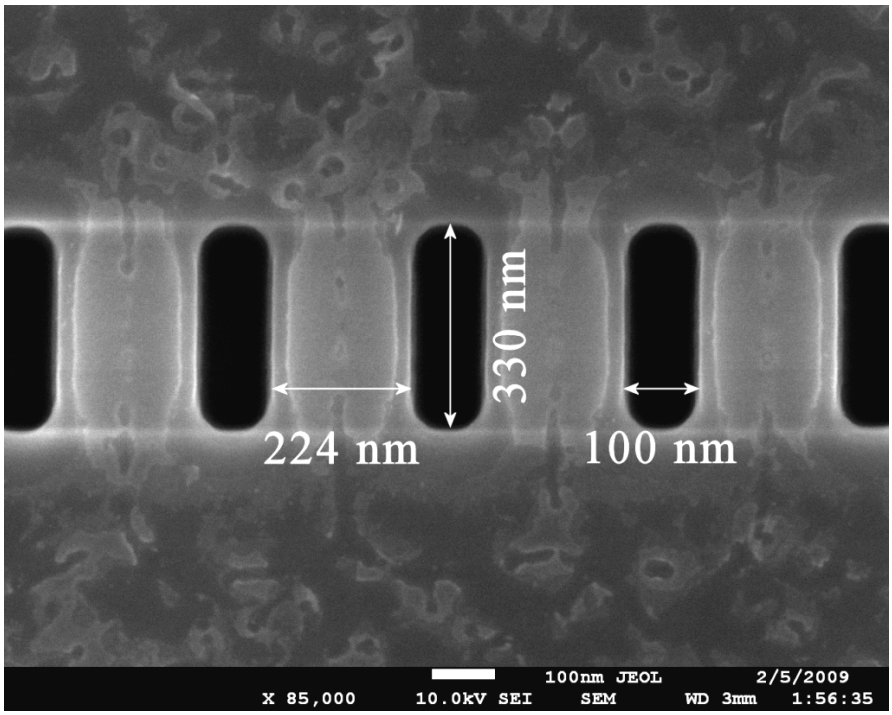


Figure 5.20. Oxidation window opening over the approximately 117 nm thick Si fingers.

The device imaged above is a punch-through light source on wafer *S8*, cluster 1, *Chip 2*, and was designed to have Si finger spacing slits 340 nm long, 100 nm wide and 260 nm apart. Although the EBL exposure and PlasmaTherm ICP etch resulted in rounded corners of the Si finger spacing holes, the dimensions of the holes are acceptably close to the layout dimensions.

Although all EBL exposures were completed, it was found that the last EBL exposure introduced a 50-µm alignment and exposure shift that resulted in the injection devices not obtaining oxidation-thinning windows at the correct locations (Figure 5.21 and Figure 5.22). The avalanche and punch-through finger junction SOI light sources obtained the correct oxidation-thinning window EBL exposure.

Figure 5.21 shows where the JEOL EPG scanned a transition to a Si monitor island instead of the alignment marker cross.

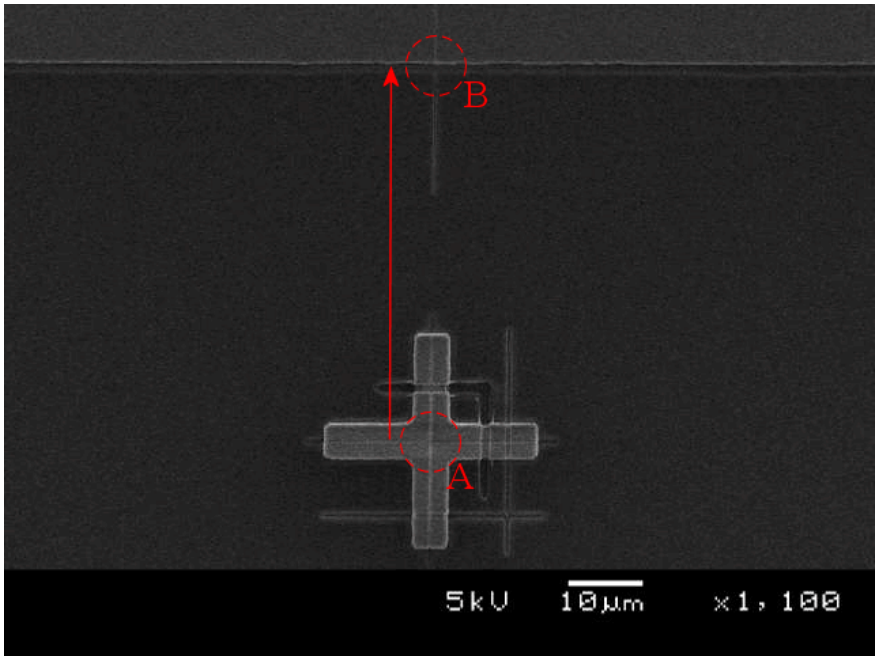


Figure 5.21. EPG scanning the wrong vertical edge causing misalignment.

This resulted in a 50 µm vertical offset of all oxidation windows over the injection-enhanced SOI light sources in *Chip3* and *Chip4* as shown in Figure 5.22

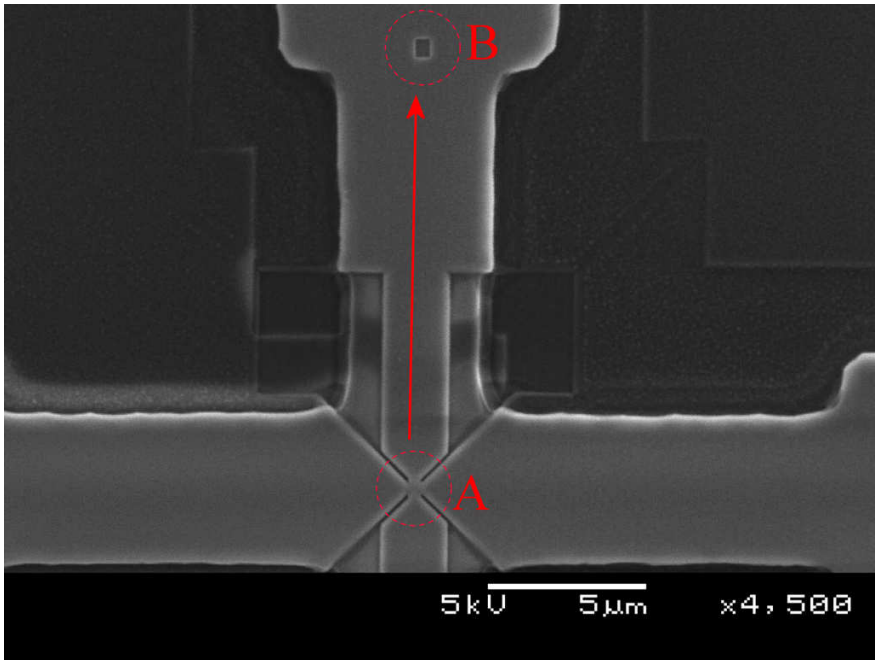


Figure 5.22. EBL oxidation window 50 µm vertical shift.

This meant that although the injection devices should still be functional, the effect of confining the dimensions of the injection region through oxidation could not be investigated anymore.

Since the SiO_2 grown on the fingers during the last thinning oxidation is usable as an anti-reflection layer between the Si finger and the air around it, the last SiO_2 layer thickness can be chosen to maximize the light transmission from the light source into the air above it. Figure 5.23 shows that maximum silicon-SiO_2-air light transmission for λ = 650 nm is achieved with a SiO_2 thickness of 112 nm.

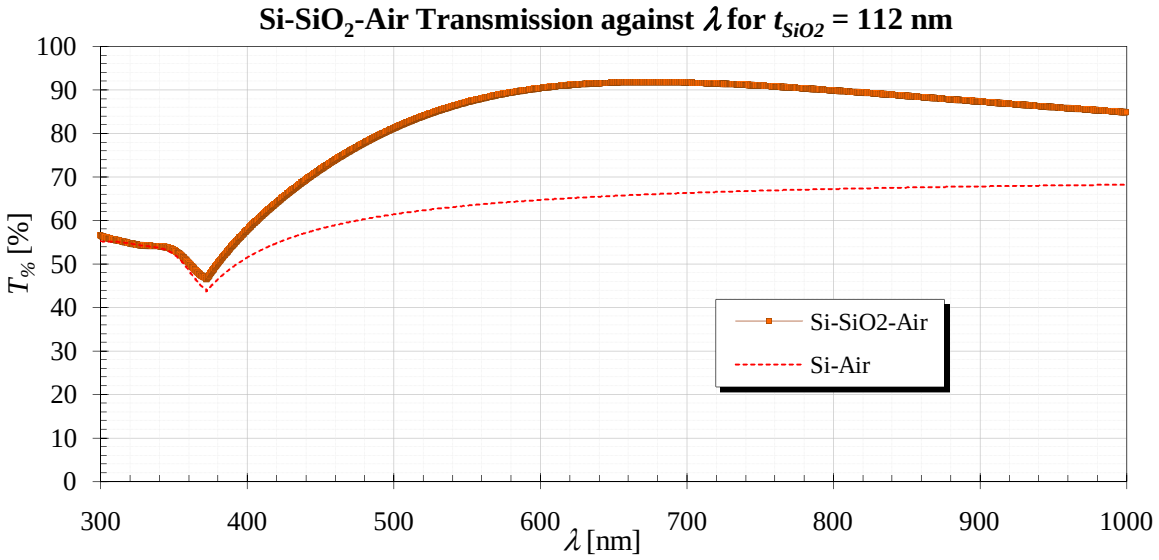


Figure 5.23. Si-SiO_2-Air transmission at t_{SiO2} = 112 nm.

Figure 5.24 shows that the maximum silicon-SiO_2-air light transmission for 300 nm $\leq \lambda \leq$ 1 µm is achieved with a SiO_2 thickness of about 65 nm.

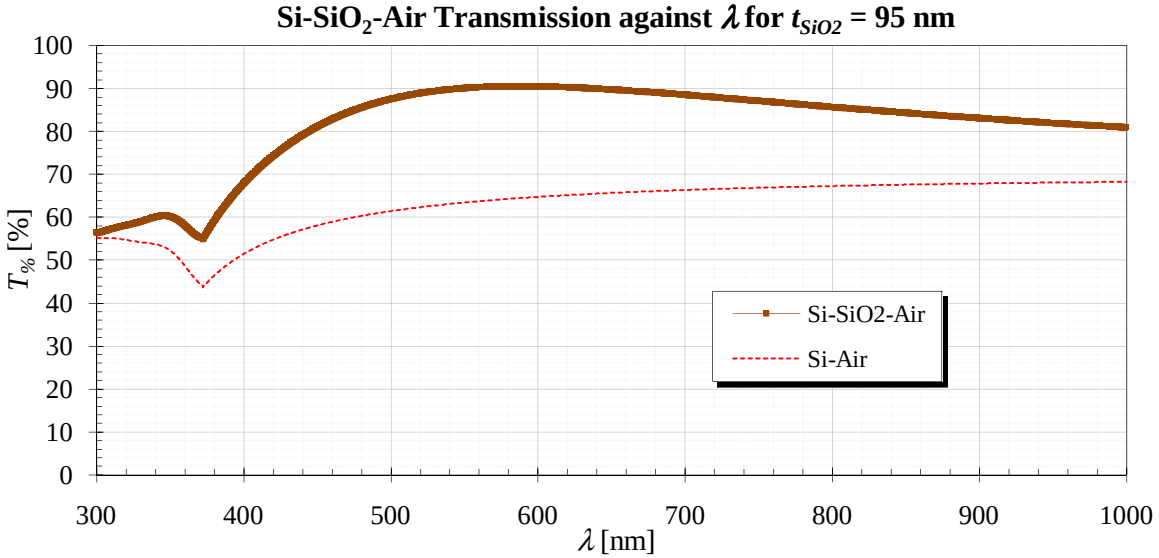


Figure 5.24. Si-SiO_2-Air transmission at t_{SiO2} = 95 nm.

For maximum external light emission efficiency, the PECVD-deposited SiO_2 thickness should therefore be between 95 and 112 nm.

The finger oxidation steps 6l and 6o were done in one of the oxidation furnaces in the clean-room of the CEFIM while the Zeiss Ultra SEM in the Centre for Microanalysis and Microscopy at UP was used to monitor the Si finger width reduction and deduce finger thickness.

Since the thinning oxidation and resultant Si finger dimensions were quite critical care was taken to slowly approach the desired finger thickness and width of around 20 nm without causing too much impurity redistribution, but still obtaining desired optical properties.

In spite of careful oxidation, it was found that many fingers were destroyed by mechanical stress that pulled the thin Si fingers apart. This is thought to have been caused by slightly differing expansion coefficients of the SiO_2 BOX and the Si on top of the BOX.

Figure 5.25 depicts three examples of final SOI finger junction dimensions achieved after the finger thinning oxidation.

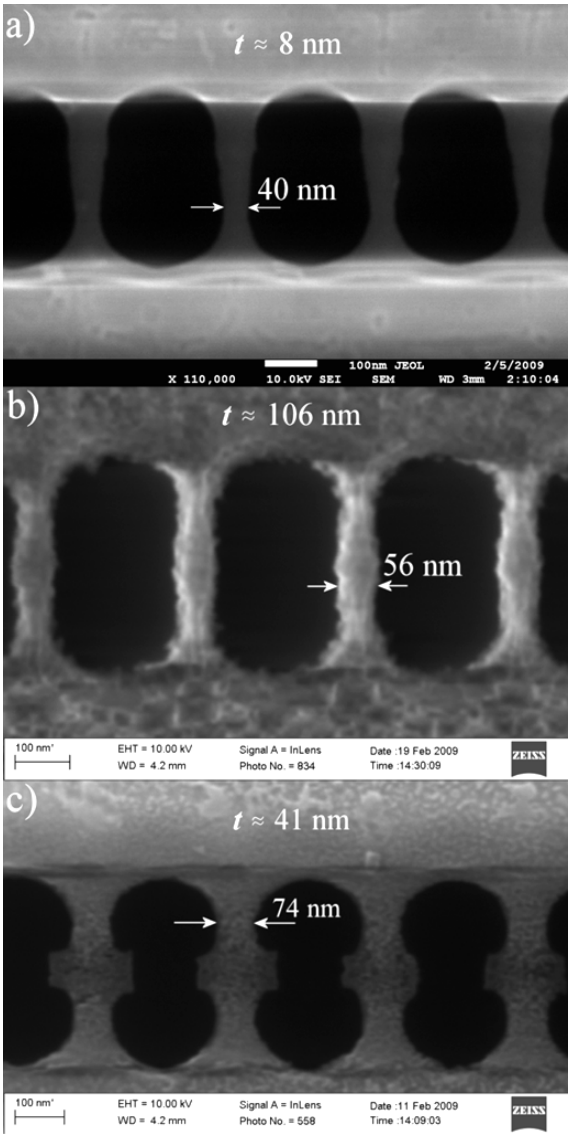


Figure 5.25. a), b) avalanche and c) punch-through SOI finger dimensions after thinning oxidation.

The Si finger thicknesses indicated in above images are estimates interpolated from reflective spectrometer measurements of the oxidation monitor islands. In contrast to the broad, but thin fingers in Figure 5.25 a), the fingers in Figure 5.25 b) are more thick than narrow.

The punch-through SOI light source in Figure 5.25 c) clearly shows how the heavily As doped Si oxidized faster than the lightly B-doped background (see subsection 2.3.2). This oxidation effect created a drift and recombination region that is slightly larger than the heavily doped contact region, which should result in higher useful light emission from the light sources since less light is lost due to internal reflection along the finger axis.

Table 5.12 shows the laid-out and final measured SOI finger dimensions.

Table 5.12. Achieved final SOI finger dimensions

Dimension	**Layout** [nm]	**Measured** [nm]
l_J	230	296 – 359
w_J	200, 220, 240, 260, 280, 300	38 – 101
l_{PT}	320, 330, 340, 350, 360, 370, 380, 390, 400	348 – 502
w_{PT}	220, 260, 300	30 – 210
s_S	50, 90, 130	Not measured
w_S	200, 260, 300	Not measured
s_O	120, 160, 200	Not measured
w_O	200, 260, 300	Not measured

5.7. Metallization

The successfulness of the wafer manufacture process could only be tested once the metallization allows electrical contact to the implemented devices.

It was initially planned to perform the metallization also at the MiRC, but since it was possible to sputter-deposit the Aluminium conductor onto the wafers by sending the wafers to Elume Inc[4]. in California, the micrometre-scale metal was chemically etched in the clean-room of the CEFIM at UP.

[4] ELume, Inc., Microchip Foundry, 587 N. Ventu Park Rd., Newbury Park, California 91320

Table 5.13. Metallization process flow.

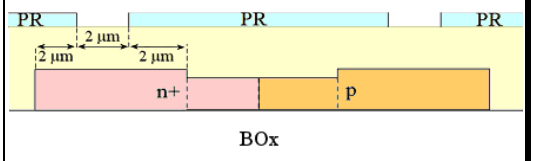
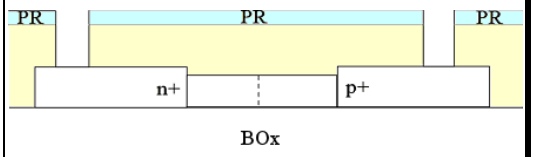
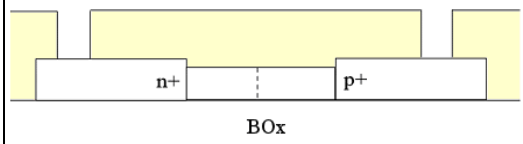
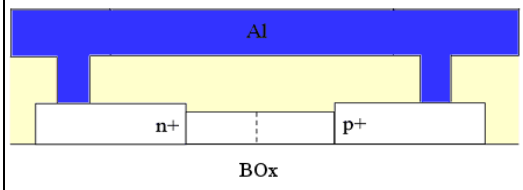
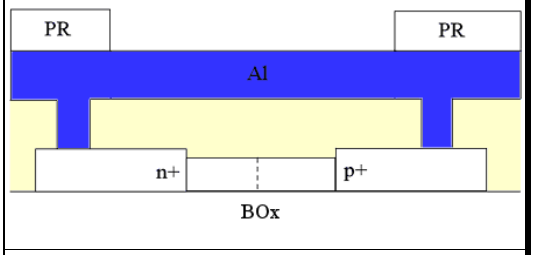
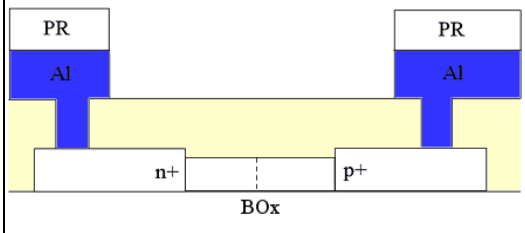
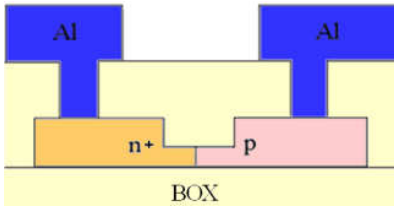
Step	Action	Equipment	Material	Facility	Graphical representation
7b	Photolithography (see steps 3c to 3g)	Karl Süss mask aligner	*Co* photo-mask SC1813	CEFIM	
7c	SiO_2 etch (Addendum D.2)	Wet-bench	BOE		
7d	Remove PR		Fuming Nitric Acid		
7e	Wafer clean	Spin-dryer	H_2O		
7f	Metallization 1 µm Al	Sputterer	Al	Elume	
7g	Pattern PR (see steps 3c to 3g)	Karl Süss mask aligner	*Metal* photo-mask SC1813	CEFIM	
7h	Al etch	Wet-bench	Al etch, BOE		
7i	Remove PR		Acetone,		
7j	Wafer clean No Acid (Metal)	Spin-dryer	H_2O		
7k	Al anneal 500 C 30 Min	Furnace	H_2N_2 forming gas		

Figure 5.26 to Figure 5.29 depict microphotographs of the final chips *Chip1* to *Chip4*.

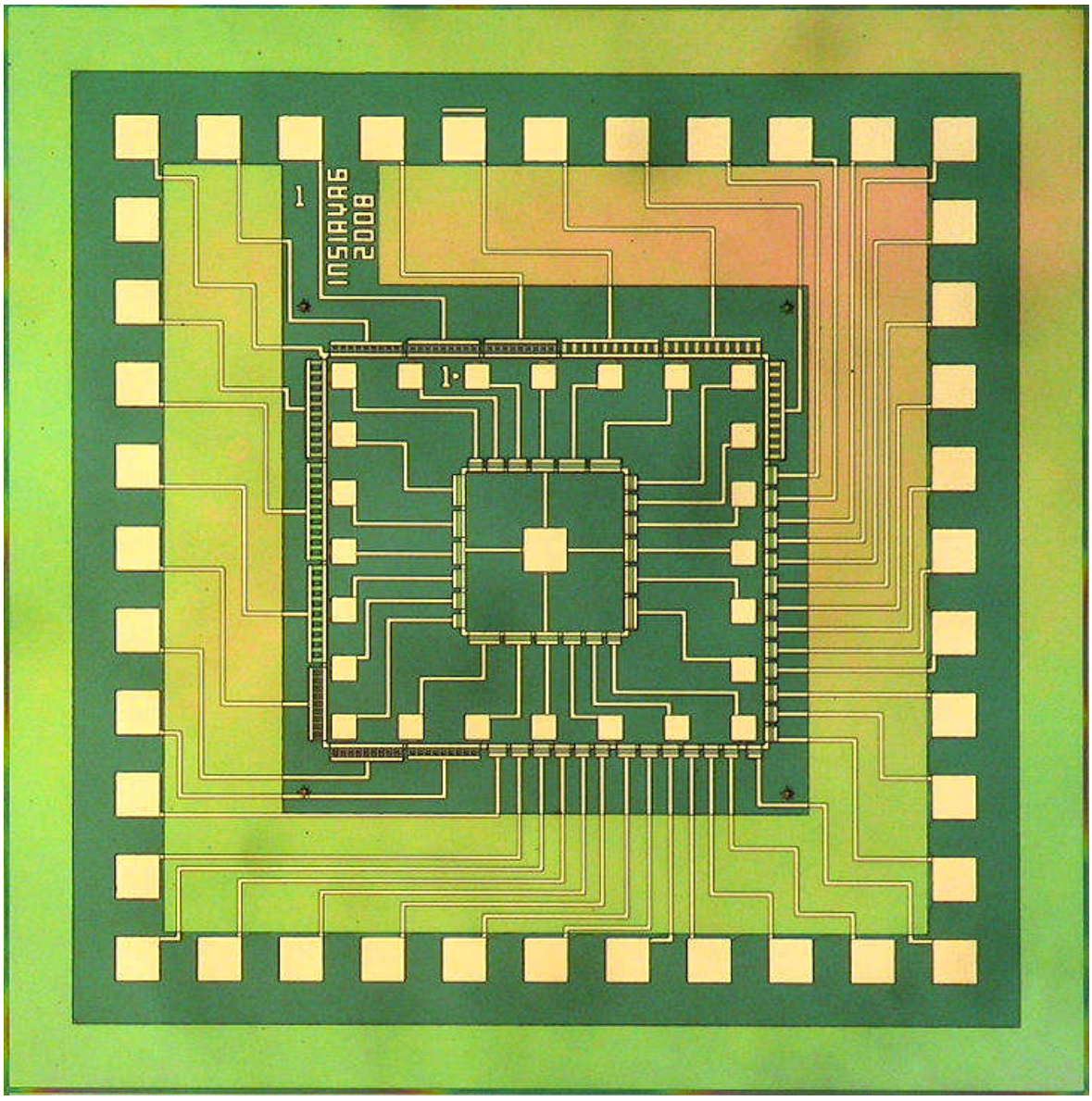


Figure 5.26. Micro-photograph of final *Chip1*.

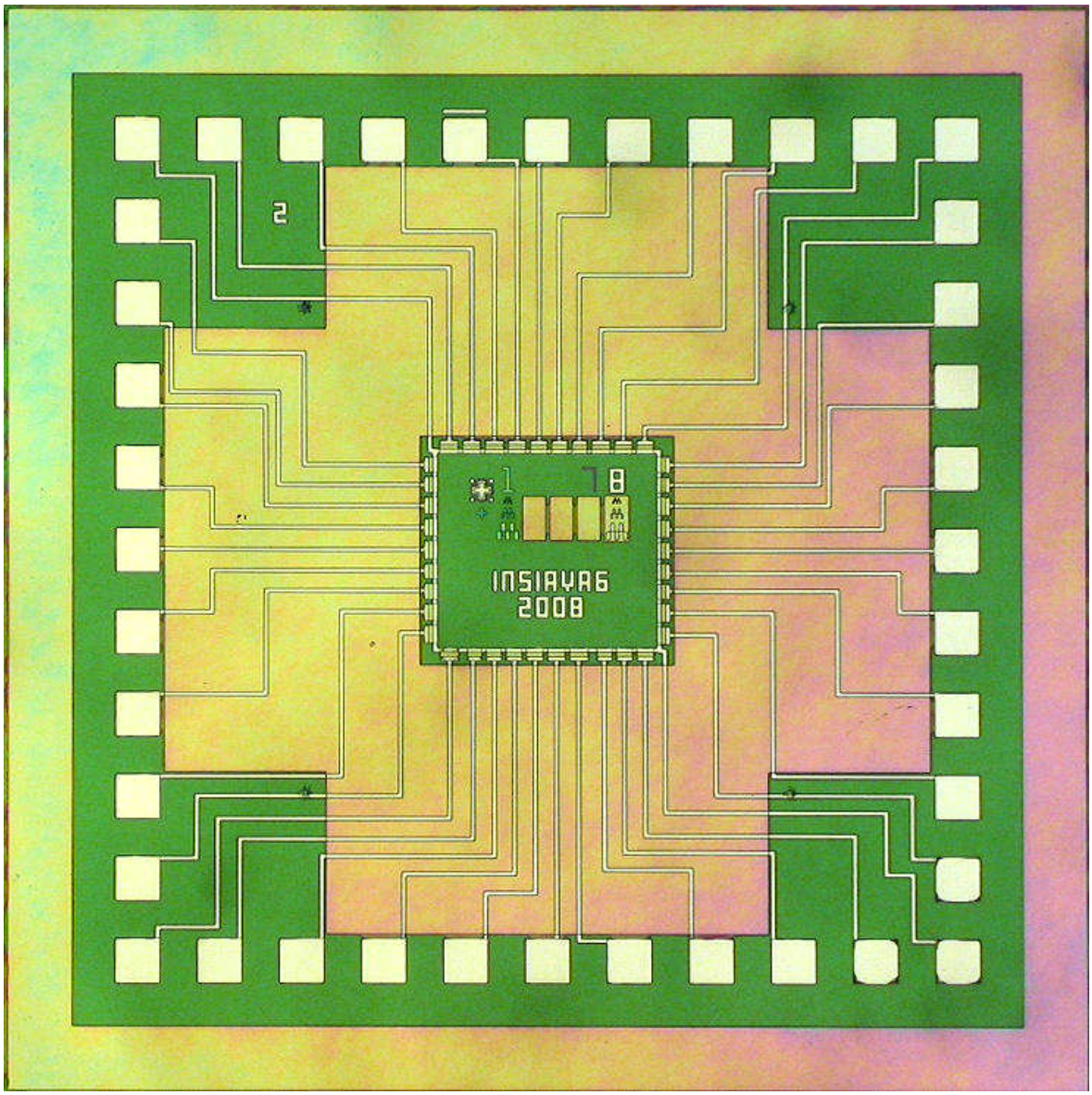


Figure 5.27. Micro-photograph of finalized *Chip2*.

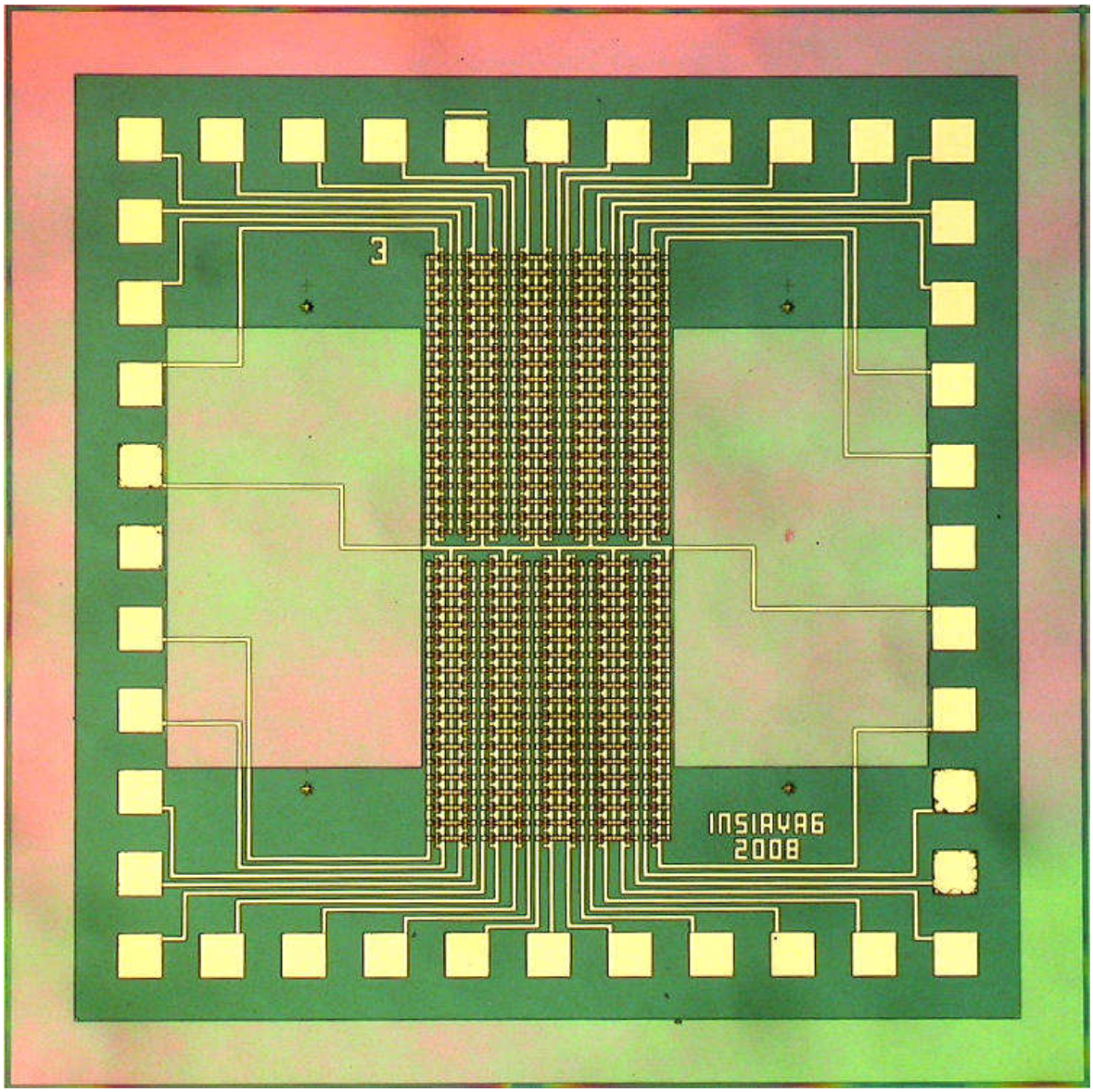


Figure 5.28. Micro-photograph of finalized *Chip3*.

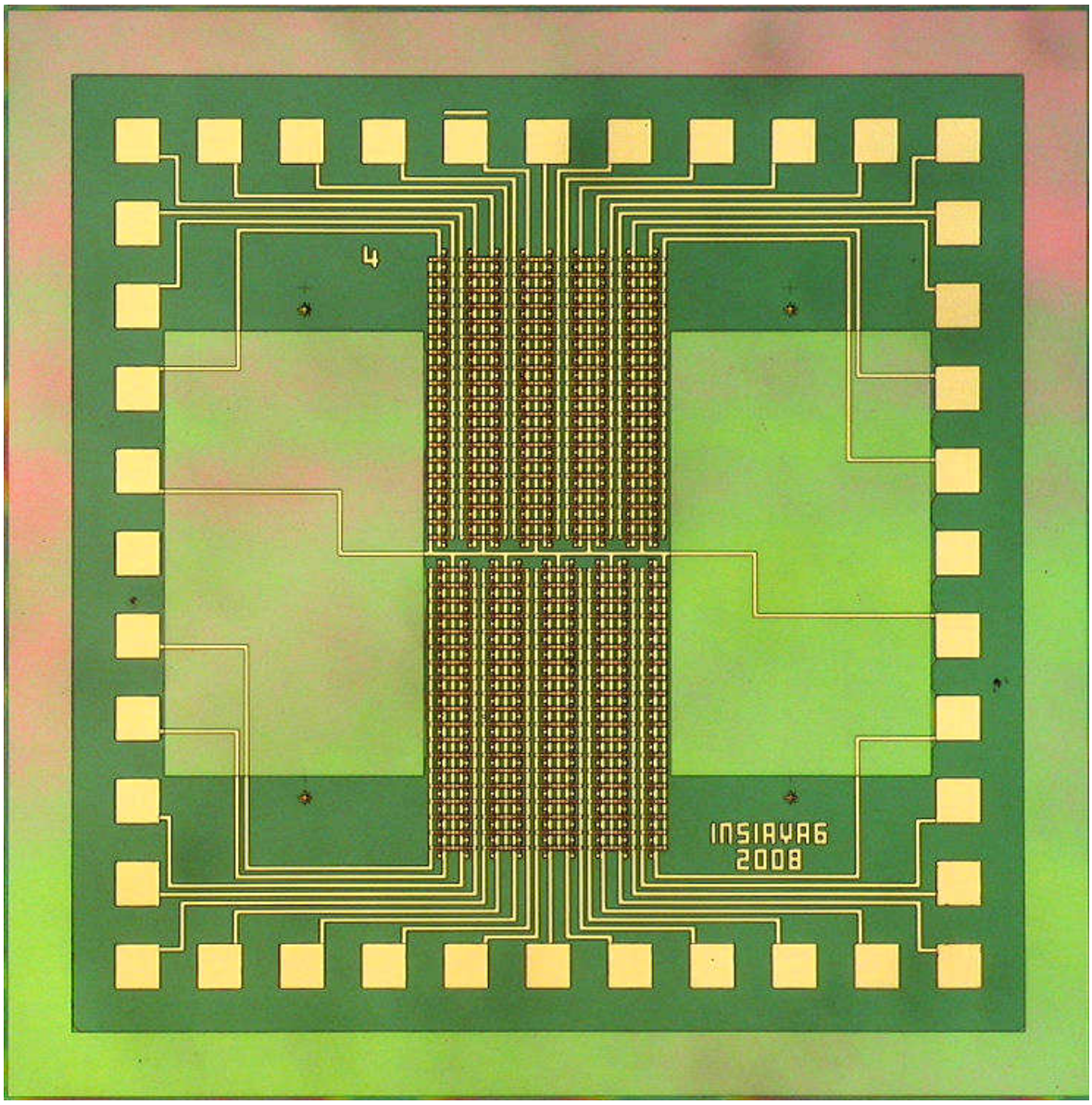


Figure 5.29. Micro-photograph of finalized *Chip4*.

6. MEASUREMENTS

After completing the metallization, wafer inspection and electrical probing selected devices for optical characterization with a calibrated spectrometer (see Addendum B), which allowed comparing the optical power spectrum to regular *pn*-junction avalanche light sources manufactured in the AMS 0.35 µm CMOS process.

6.1. Electrical Probing and Device Selection

505 devices across 34 clusters on all four wafers were manually probed. It was found that only two wafers contained light-emitting devices: *S3* and *S5*. About half of all devices lost their fingers due to either over-oxidation or mechanical stress that seems to have pulled the fingers apart.

Furthermore, it was found that an oversight during the design phase caused the un-thinned devices to become resistors. Since the Si_xN_y masking layer protected these devices from oxidation, the anticipated B extraction and redistribution could not occur. The B therefore overshadowed the weaker As implant. An unexpected advantage of this oversight was that many oxidation-thinned process-monitoring resistors became p^+np^+ punch-through light sources.

It was also determined that the one micron thick Al experienced step coverage problems. This was caused by the fact that the BOX was etched deeper into than expected. In many places the BOX etch undercut the Si islands, which caused discontinuities in the Al metallization. This discontinuity was especially pronounced on the sides of the bonding pads, which meant that most pads could not be used for electrical connection. A simple remedy would have been to underlay all Al metallization with Si island tracks during the design phase, but this was not considered at that stage (but will be remembered for future designs). Although most functional devices could still be measured by positioning the probing needles on the Al tracks leading to the devices, this had the disadvantage that none of the chips could be packaged. This meant that the optical characterization also had to be done on wafer level.

After wafer inspection, electrical measurements and subjective evaluation by eye was used to select seven light-emitting devices located on cluster *EBL2* on wafer *S3* for optical characterization. The layout and estimated dimensions of these seven devices are indicated in Figure 6.1 and Table 6.1 respectively.

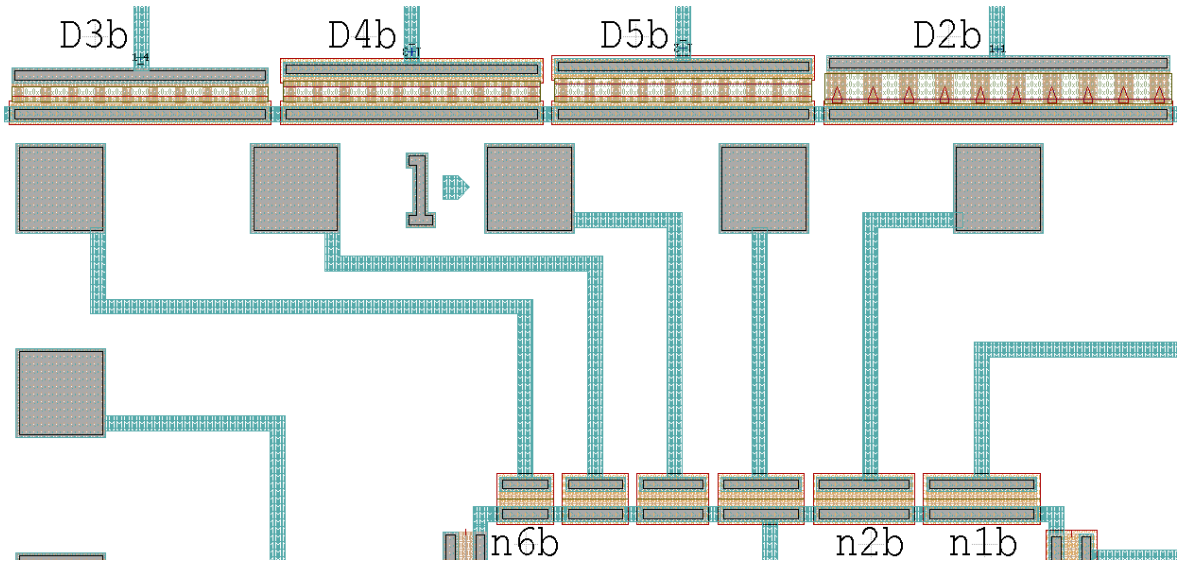


Figure 6.1. Devices in *Chip1* selected by electrical probing for comparative optical measurements.

Table 6.1. Estimated device and finger widths.

Dimension	w_{Device}	w_{Finger_Design}	Δ_{Finger}	w_{Finger_Final}
Device	[µm]			
D2b	228	12	0.1	11.9
D3b	168	6		5.9
D4b				
D5b				
	[µm]	[nm]		
n1b	74	600	115	485
n2b	64	500		385
n6b	34	200		85

Although none of these devices have nanometre-scale finger widths, their average finger thickness is estimated to be around 17 nm. Since the devices between *n6b* and *n2b* were open circuit and, as shown later, *D4b* and *D5b* are thinner than *D3b* and *D2b*, it seems that the Si device layer thickness had a minimum around the horizontal centre of Figure 6.1. Since the exact thicknesses of selected devices can only be measured by cross-section and further testing of the devices is still planned, such destructive thickness measurements have not yet been performed.

Figure 6.2 depicts the electrical characteristic curves of the selected test light sources.

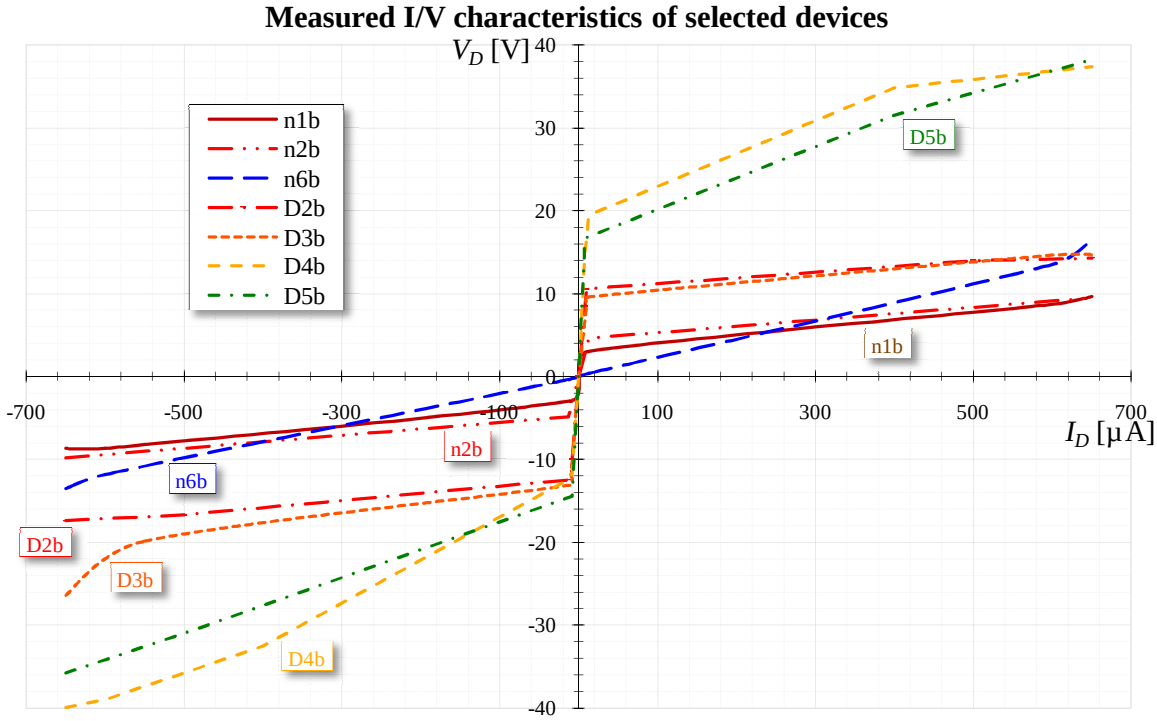


Figure 6.2. Measured current-voltage characteristic of selected punch-through SOI light source.

Although *n6b* emits light, its I-V curve shows that it has a resistance of about 20 kΩ in parallel. Since this resistance bypasses current through the device without contributing to the light generation, it is expected that *n6b* will have a low light emission efficiency. The voltage and resistance summary in Table 6.2 shows a higher breakdown voltage and higher series resistance for devices *D2b* to *D5b*.

Table 6.2. Voltages and resistance of selected devices at I_D = ±650 µA and ±11 µA.

Wafer	Location	Device	Reverse			Forward		
			$V_{D\text{-}11\mu A}$	$V_{D\text{-}650\mu A}$	$R_{\text{-}650\mu A}$	$V_{D11\mu A}$	$V_{D650\mu A}$	$R_{650\mu A}$
			[V]		[kΩ]	[V]		[kΩ]
S3	*EBL2*	*n1b*	-3.0	-8.7	3	3.0	9.7	3
		n2b	-4.9	-9.8	15	4.6	9.5	13
		n6b	-0.4	-11.8	19	0.4	16.5	39
		D2b	-12.5	-17.4	33	10.6	14.0	29
		D3b	-13.1	-26.4	54	9.6	14.7	39
		D4b	-12.1	-38.9	57	17.2	37.4	40
		D5b	-14.5	-35.7	74	16.7	38.3	77

Since a higher series resistance corresponds to a thinner Si device layer thickness and an increased breakdown voltage is characteristic of quantum-confinement, it is expected that especially *D4b* and *D5b* should have high light generation efficiencies.

Figure 6.3 shows a microphotograph of *D3b* emitting light at a bias of 650 µA.

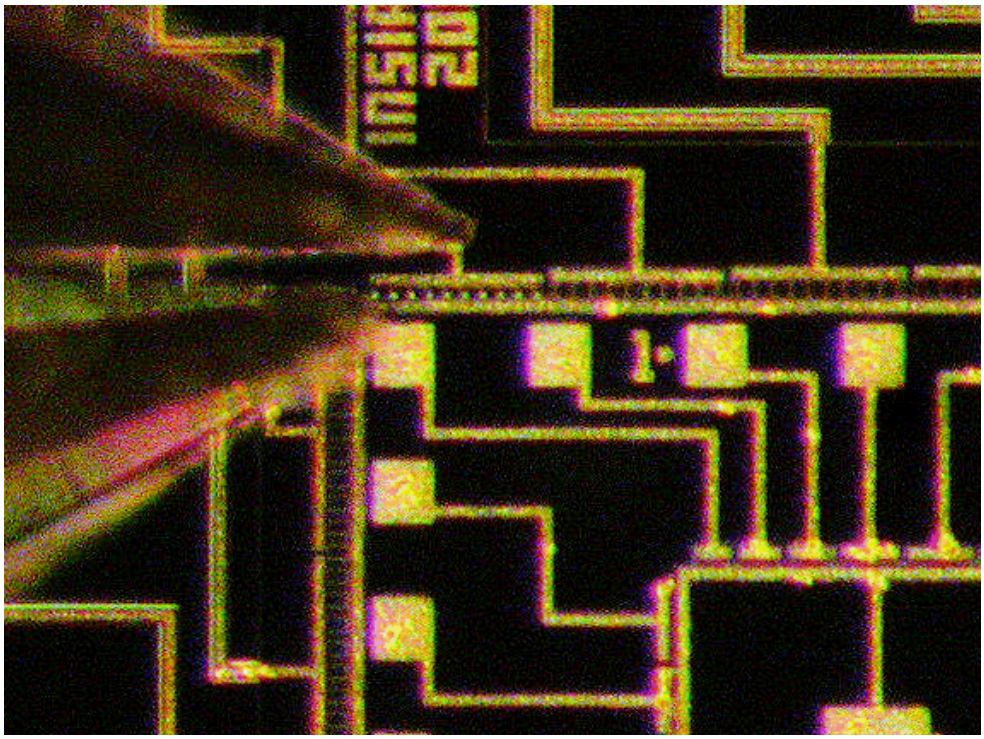


Figure 6.3. Electrical probing of test-device *D3b*.

Figure 6.4 shows the same view with the microscope light switched off.

Figure 6.4. Light generation of the same *D3b* test-device.

The emitted light is homogenously spread across all punch-through fingers.

Figure 6.5 shows the light-emitting punch-through device *n2b* at I_D = 650 µA.

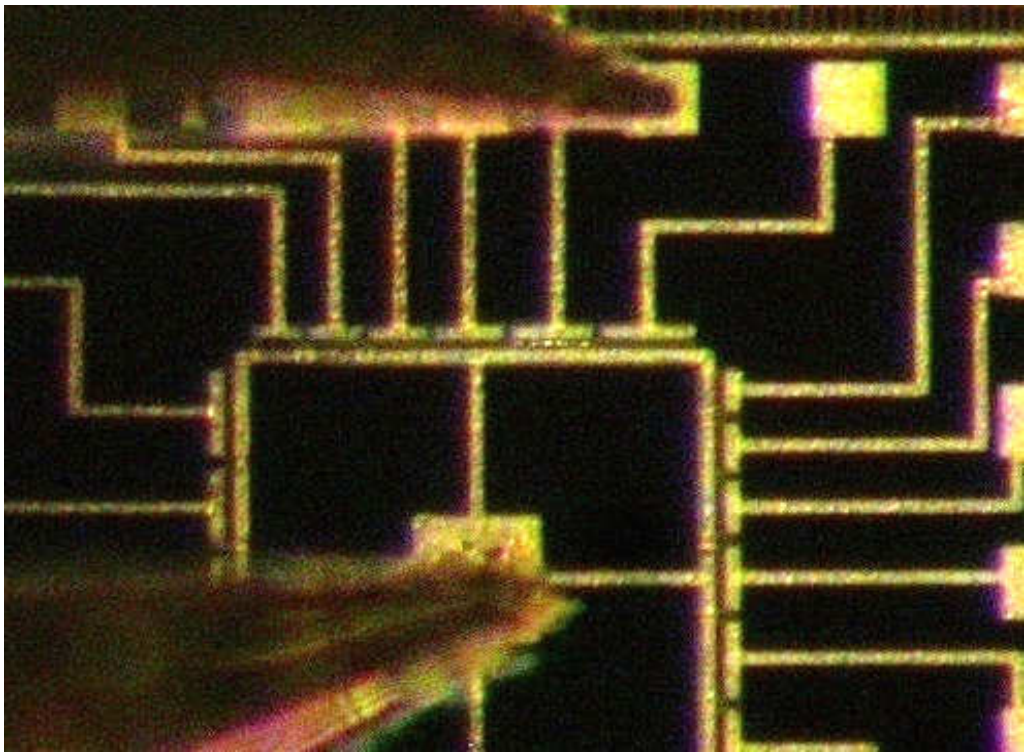


Figure 6.5. Probing of fingered punch-through device *n2b*.

Figure 6.6 shows the same view of *n2b*, but with the microscope light switched off.

Figure 6.6. Light generated by the fingered punch-through device *n2b*.

Above light emission is not homogenous and some fingers light up brighter than others do.

6.2. Optical Characterization

Since the mentioned Al metal step-coverage problem prohibits bonding and packaging of the manufactured SOI chips, the test light sources had to evaluated optically on the wafers. This was achieved by attaching a fibre-optic cable to one of the probing station manipulators. After successively stripping the fibre-optic cable of its shielding and protective sleeves, the 60-µm core of the cable was then aligned to point perpendicularly down on the wafer. As shown in Figure 6.7, this method allowed positioning the stripped core onto a specific SOI light source.

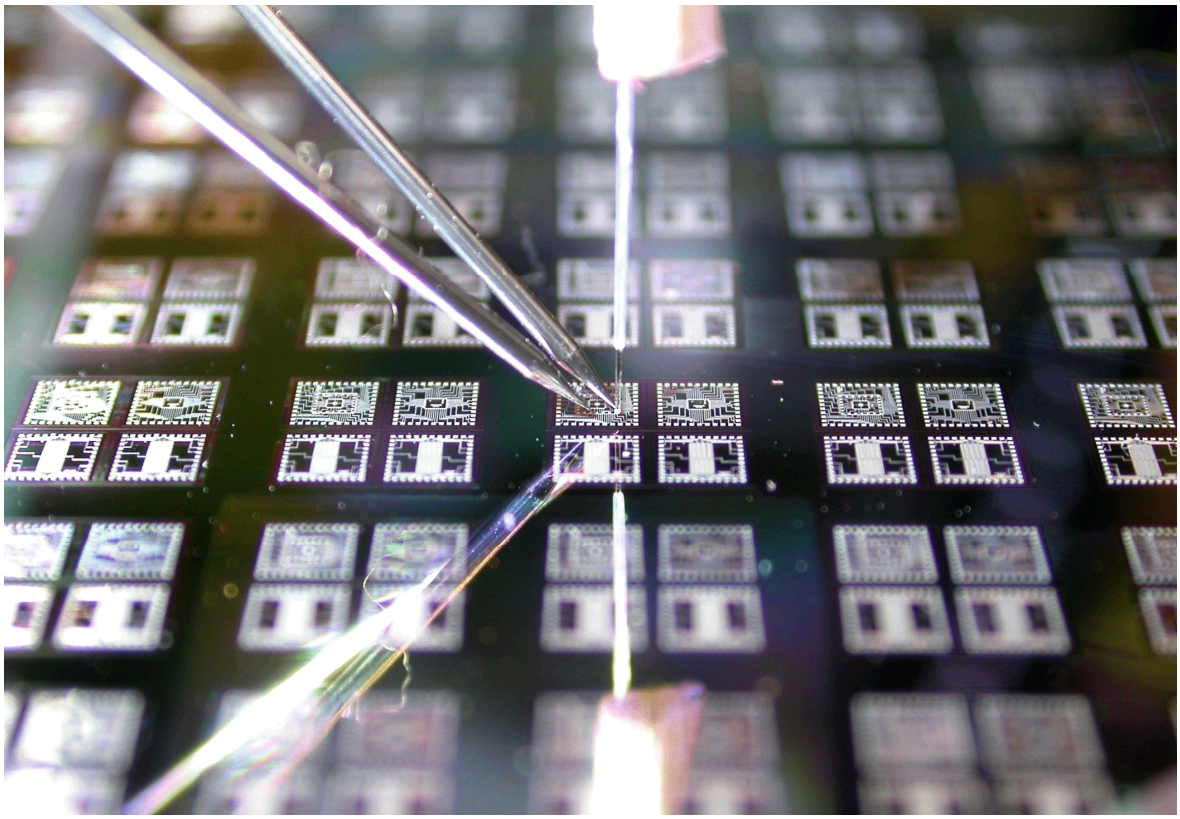


Figure 6.7. Spectroscopic probing of the SOI light-sources.

Since the emitted optical power was too low for a radiometer and photo-multiplier tube measurements only render a photon count without any spectral information, it was decided to connect the other end of the fibre-optic cable to a calibrated spectrometer (see Addendum B). Although the spectrometer could not measure accurate absolute optical power levels, the measured power spectra was used to compare the power spectra of the selected SOI test-devices to *pn*-junction avalanche light sources manufactured in the AMS 0.35 µm CMOS process.

Figure 6.8 compares the measured power spectra of test SOI light sources *D2b* to *D5b*. operating at I_D = 650 µA.

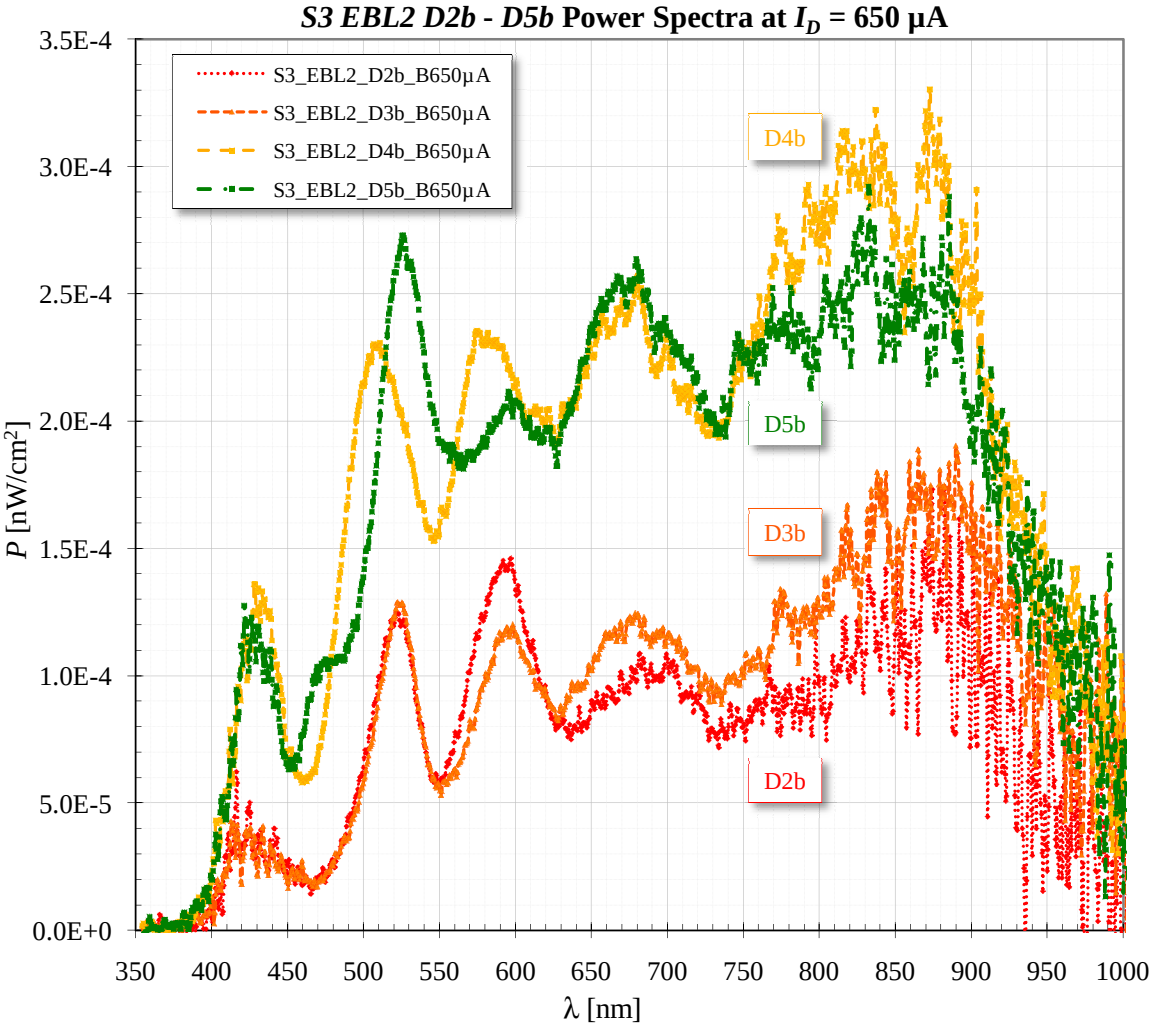


Figure 6.8. Measured power spectra of the *D2b – D5b* SOI light-sources.

In correlation to the observations made with respect to their current-voltage characteristics, *D4b* and *D5b* exhibit optical power outputs that are approximate 2.5 times higher than those measured on devices *D2b* and *D3b*. Their higher irradiance seems to confirm that *D4b* and *D5b* are already thin enough to experience quantum confinement effects that increase their optical power emission. The shifted peak of *D4b* in the UV spectrum (400 nm < λ < 600 nm) also seem to suggest that quantum confinement has shifted the band-gap structure of this device.

The large optical radiation power in the infrared (IR) spectrum range (750 nm < λ < 950 nm) though is unexpected.

Employing the same scaling as Figure 6.8, Figure 6.9 plots the measured optical power spectra of devices *n1b*, *n2b* and *n6b*.

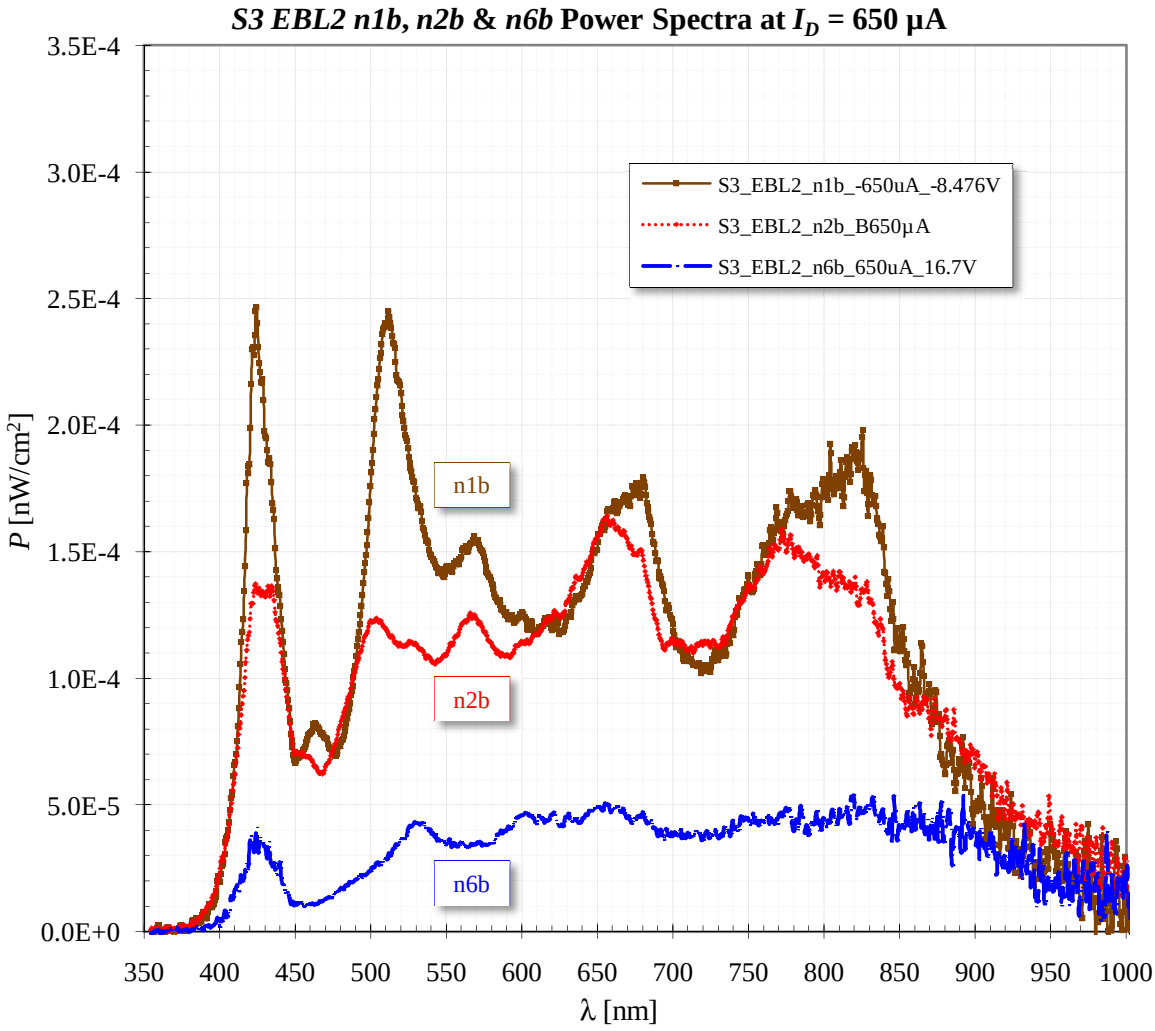


Figure 6.9. Measured power spectra of the *n1b*, *n2b* and *n6b* SOI light-sources.

The lower optical efficiency of *n6b* was already predicted from its current-voltage characteristic in Figure 6.2 that exhibited a parallel leakage resistance.

Since the optical power amplitudes of *n1b* and *n2b* are similar to those of *D2b* and *D3b* suggests that all these devices have about the same Si layer thickness, but in contrast to *D2b* and *D3b*, *n1b* and *n2b* exhibit less optical power in the infrared region.

The lack of UV peak shifting in above figure reinforces the suspicion that these devices are not yet thin enough to experience significant quantum confinement effects.

Figure 6.10 compares the "best" device from Figure 6.8 (*D4b*) to the "best" device from Figure 6.9 (*n1b*).

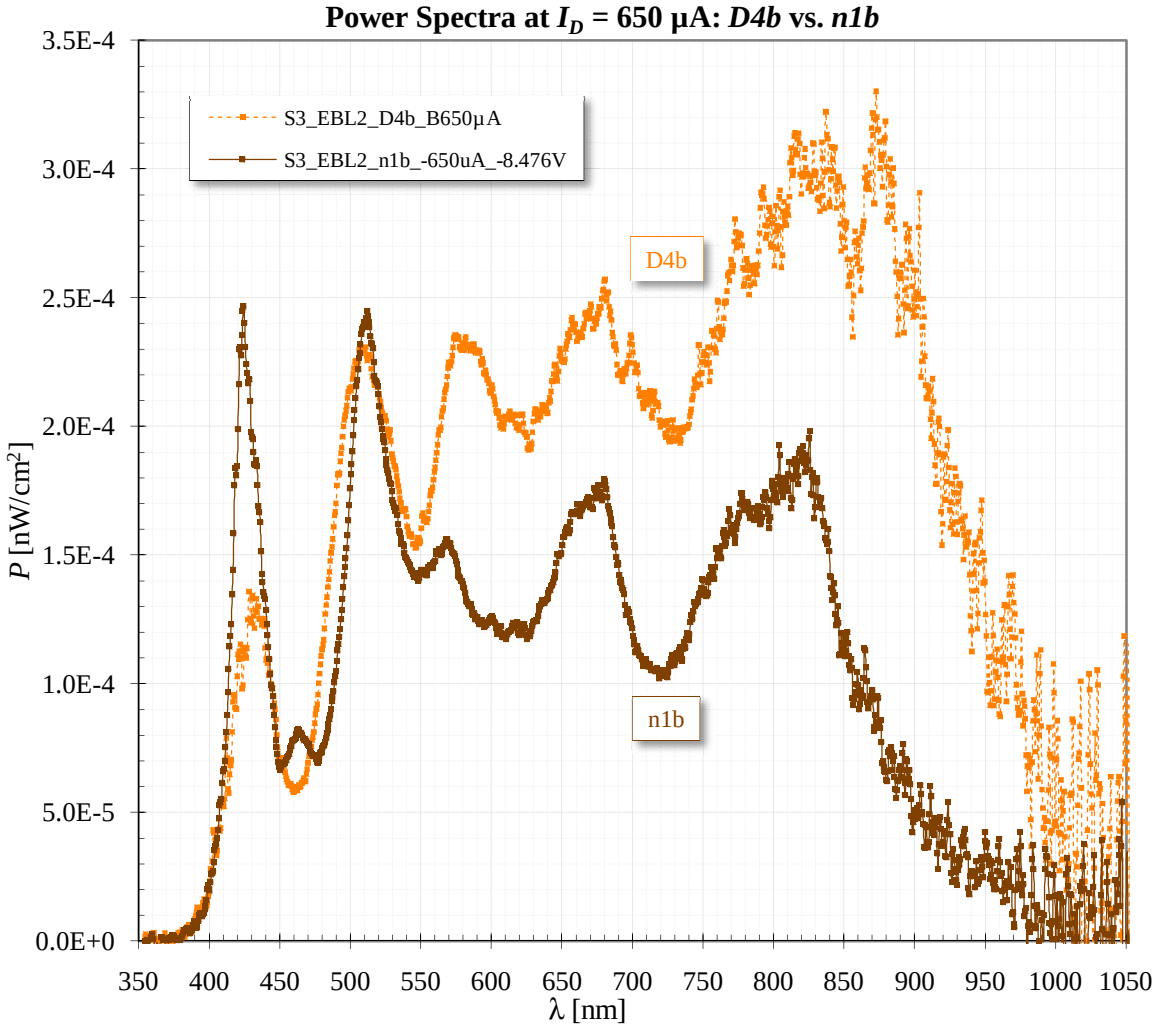


Figure 6.10. Measured power spectra comparison of the *n1b* and *D4b* SOI light-sources.

Both devices exhibit similar spectral peaks and have similar optical power in the UV side (λ < 550 nm) of the spectrum.

D4b displays an optical power that increases with wavelength up to twice the optical radiation of *n1b* in the infrared.

Figure 6.11 compares the spectrum of the SOI punch-through light source with the highest optical power (*D4b*) to the average optical power of 25 avalanche CMOS *pn*-junction light sources also biased at I_D = 650 µA and measured with exactly the same characterization setup.

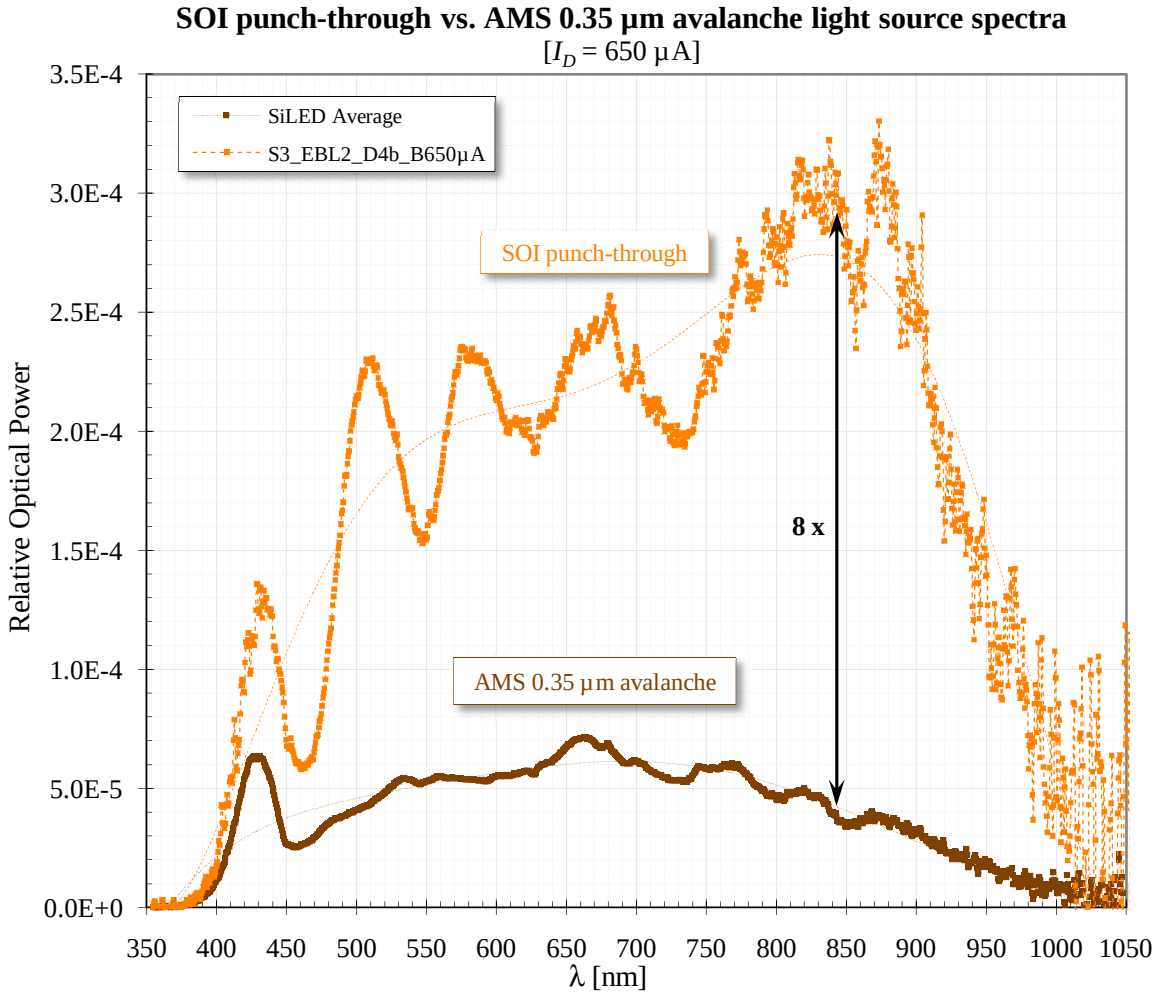


Figure 6.11. Spectra comparison of SOI punch-through and AMS 0.35 µm CMOS light-sources.

While the AMS 0.35 µm avalanche light source spectrum peaks around $\lambda \approx 660$ nm ($E_{Ph} \approx 1.88$ eV) the SOI punch-through light source peaks around $\lambda \approx 850$ nm ($E_{Ph} \approx 1.46$ eV).

It is evident that the SOI punch-through device radiates up to 8 times more optical power around 850 nm. Since significant IR radiation peaks have also been observed in Si nano-crystal EL and photoluminescence (PL) experiments ([92] and [57]), this could be indicative of quantum confinement.

Considering that photons at longer wavelengths have lower energies implies that more photons are required at longer wavelengths to achieve the same optical power as photons at lower wavelengths. It therefore seems that thickness-confined SOI light sources have significantly higher quantum conversion efficiencies than bulk-CMOS avalanche light sources.

IR spectral components were previously reported for forward-biased and avalanching junctions ([20], [27], [29], [56], [93] and [94]). The multi-mechanism Si avalanche photon-generation model [95] postulates that the optical radiation spectrum of an avalanching junction consists of three recombination paths: intra-band transitions (Bremsstrahlung), direct and indirect inter-band recombination. The relative strengths of these spectral contributions depend on electric field strength and ionization length of electrons and holes. While intermediate photon energies (2 eV < E_{Ph} < 2.3 eV) are attributed to indirect intra-band transitions, the low-energy photon emission (E_{Ph} < 1.8 eV) is thought to originate from indirect inter-band (phonon-assisted) recombination of electrons and holes in high-field populations.

It therefore seems that the spectra of the AMS 0.35 µm avalanche light sources with their peak around 1.88 eV are caused by a combination of indirect intra- and inter-band recombination. The observed spectra of the SOI light sources peak at around 1.46 eV and are predominantly generated by indirect inter-band recombination of hot carriers.

Other possible reasons for the increased IR optical radiation could include the closer shifting of carrier distributions in the energy bands, the valance and conduction bands shifting closer to each other or the presence of defect- or impurity-assisted radiative recombination [96].

The periodic optical power variation of all measured SOI light sources is due to light reflection off the SiO_2 BOX covering the Si handle layer of the SOI wafer. Employing the mathematical stack transmission model of subsection 2.2.3.2, the reflection R (= 1 – T) of a Si-SiO_2-air stack can be simulated for varying SiO_2 thicknesses. Starting with the average measured BOX thickness t_{BOX} = 980 nm (Table 5.4) and decreasing t_{BOX} until the reflection peaks agree with the spectral peaks of the measured SOI light source power spectra revealed that the best fit was achieved for $t_{BOX} \approx$ 860 nm (see Figure 6.12).

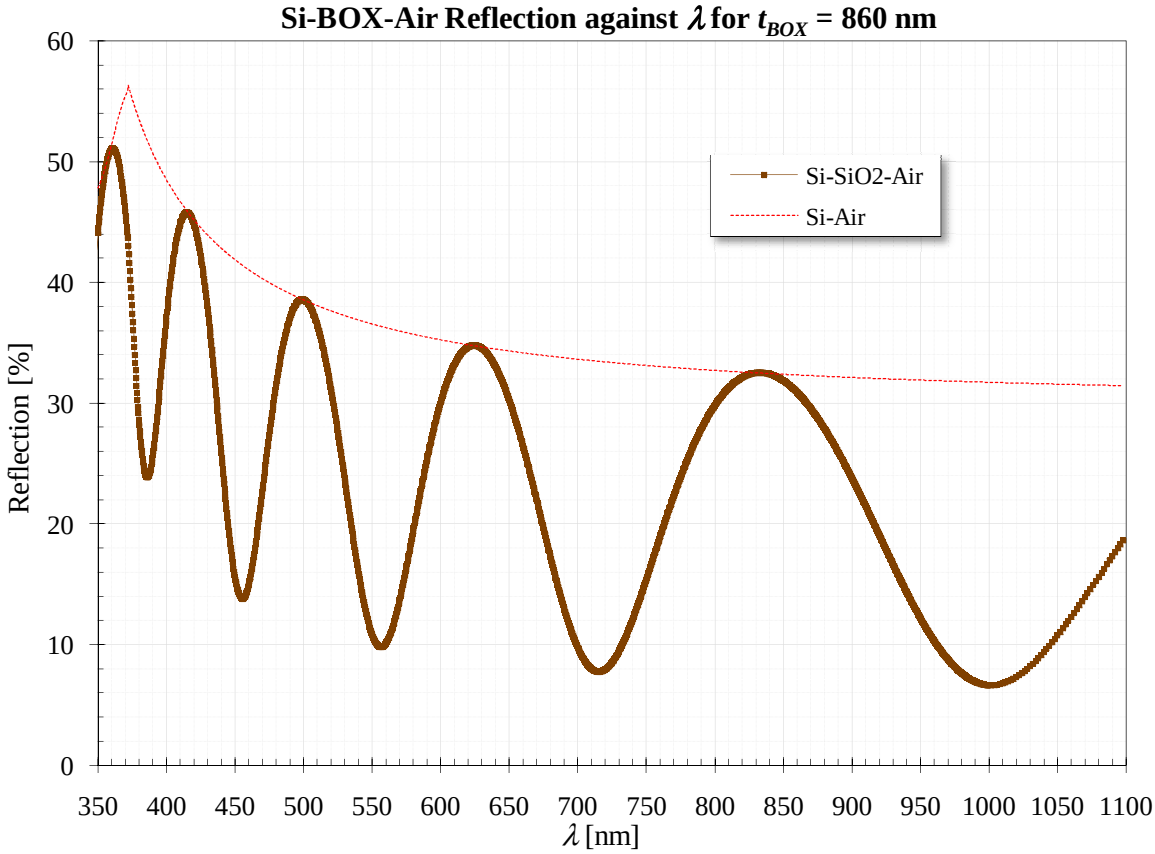


Figure 6.12. Simulated perpendicular BOX reflection for BOX thickness t_{BOX} = 860 nm.

Above plot shows that an average of 25 % of the light that would have been lost through downward radiation is reflected back up as useful light. Although this reflection and the efficiency improvement due to the finger shaping (see section 3.2) explain an increase in luminescence of the SOI light sources, they do not explain the increased infrared radiation measured as the average BOX reflection decreases with increasing wavelength.

Above also implies that about 120 nm of the BOX were etched away during processing. This was not considered during the design and explains the metal step coverage problem experienced.

7. CONCLUSION

This project was a first-iteration attempt at investigating quantum confinement in nanometre-scale SOI light sources as a method of increasing the quantum conversion and external power efficiency of Si light sources. For the author this was also the first exposure to clean-room self-processing and as far is known this was the first project in South Africa (and possibly at the MiRC) that employed EBL to define functional nanometre-scale semiconductor devices.

Although due to design and processing oversights only 29 out of 505 measured SOI light sources were useful light emitters, the design and manufacture of the SOI light sources was successful in the sense that enough SOI light sources were available to conduct useful optical characterization measurements. In spite of the fact that the functional light sources did not achieve the desired horizontal (width) confinement, measured optical spectra of certain devices indicate that vertical (thickness) confinement had been achieved.

All spectrometer-measured thickness-confined SOI light sources displayed a pronounced optical power for 600 nm < λ < 1 µm. The SOI light source with the highest optical power output emitted about 8 times more optical power around λ = 850 nm than a 0.35 µm bulk-CMOS avalanche light-source operating at the same current. Possible explanations for this effect were given. The expected dramatic increase in optical power in the UV spectrum region (λ < 600 nm) was not realized.

It was shown that the BOX layer in a SOI process could be used to reflect about 25 % of the light that would usually be lost to downward radiation back up, thereby increasing the external power efficiency of SOI light sources. Since it is estimated that the external power efficiency improvement factor due to the finger shaping and SOI box-handle interface reflection is about two, this leaves an improvement factor due to 17 nm thickness-confinement of about four, which agrees with results in Figure 1.2 previously reported at the University of Twente.

Since this first iteration attempt at quantum-confined light sources showed promising results, a following development phase is planned in which experience gained from this work is incorporated in creating even thinner 2D-confined SOI light sources.

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[95] N Akil, SE Kerns, DV Kerns, Jr., A Hoffmann and J-P Charles, "A multimechanism model for photon generation by silicon junctions in avalanche breakdown", IEEE Transactions on Electron Devices, Vol. 46, No. 5, May 1999, pp. 1022-1028.

[96] D Bisero, F Corni, G Ottaviani, R Tonini and L Pavesi, "Infrared Light Emission Due To Radiation Damage in Crystalline Silicon", Solid State Commun., Vol. 101, No. 12, 1997, pp. 889–891.

ADDENDUM A: PHYSICAL CONSTANTS

Table A.1 below lists the numeric values of all physical constants used in this work ([53], pg. 788 - 790).

Table A.1. Physical constants used in this document.

Constant	Description	Value	Unit
c	Speed of light in vacuum	$2.9979245805 \cdot 10^{8}$	m/s
d_{Si}	Si density	2.329	g/cm^3
ε_0	Free space permittivity	$8.85418781762 \cdot 10^{-14}$	F/cm
ε_{rSi}	Si relative permittivity	11.6 - 11.8	-
ε_{SiO2}	SiO_2 relative permittivity	3.8 - 3.9	-
Eg_{Si}	Si energy band-gap	1.12	eV
$\hbar$	Planck's constant	$6.6260994816 \cdot 10^{-34}$ $4.1356673310 \cdot 10^{-15}$	J·s eV·s
k_B	Boltzmann's constant	$1.380658 \cdot 10^{-23}$	J/K
k_{Air}	Air extinction coefficient	0	-
k_{SiO2}	SiO_2 extinction coefficient	0	-
m_e	Electron mass	$9.10939 \cdot 10^{-31}$	kg
n_{i0}	Si intrinsic concentration	$1.45 \cdot 10^{10}$	cm^{-3}
n_{Air}	Air refractive index	1.00029	-
n_{SiO2}	SiO_2 refractive index	1.43 - 1.47	-
n_{SixNy}	Si_xN_y refractive index	2.0	-
q	Electron charge	$1.60218 \cdot 10^{-19}$	C
T	Absolute temperature	300	K

ADDENDUM B: SPECTROMETER

B.1. Spectrometer Details

Manufacturer:	Avantes, Netherlands
Model:	AvaSpec-2048TEC
Type:	Thermo-electrically cooled fibre-optic spectrometer
Specifications:	
Range:	200 – 1100 nm
Peltier cooling:	-25 - -30 ºC below room temperature
Stray light:	< 0.1 %
Optical resolution:	< 8 nm
AD resolution:	16 bit
Maximum integration time:	10 Min
Sensitivity:	40 ph/count
	$2 \cdot 10^4$ counts/µW/ms
SNR:	200:1
Noise:	560 ph_{rms}
Hardware configuration:	
Detector:	2048 pixel Sony ILX554B
Detector coating:	>150 nm deep UV
Slit width:	200 µm
Grating:	UA
Grating lines:	300 grooves/mm
Blaze wavelength:	500 nm
Grating coating:	Order sorting OSC-UA 350 and 590 nm long-pass filter
Lens:	Quartz DCL-UV/VIS 200 – 1100 nm
Manufactured:	August 2007
Location:	Optical Laboratory, CEFIM, University of Pretoria
Software:	AvaSoft Full version 7.1 USB1

B.2. Spectrometer Calibration

The spectrometer was calibrated by first measuring the spectral irradiance of the Betham IL1 and M300 monochromator as shown Figure B.1.

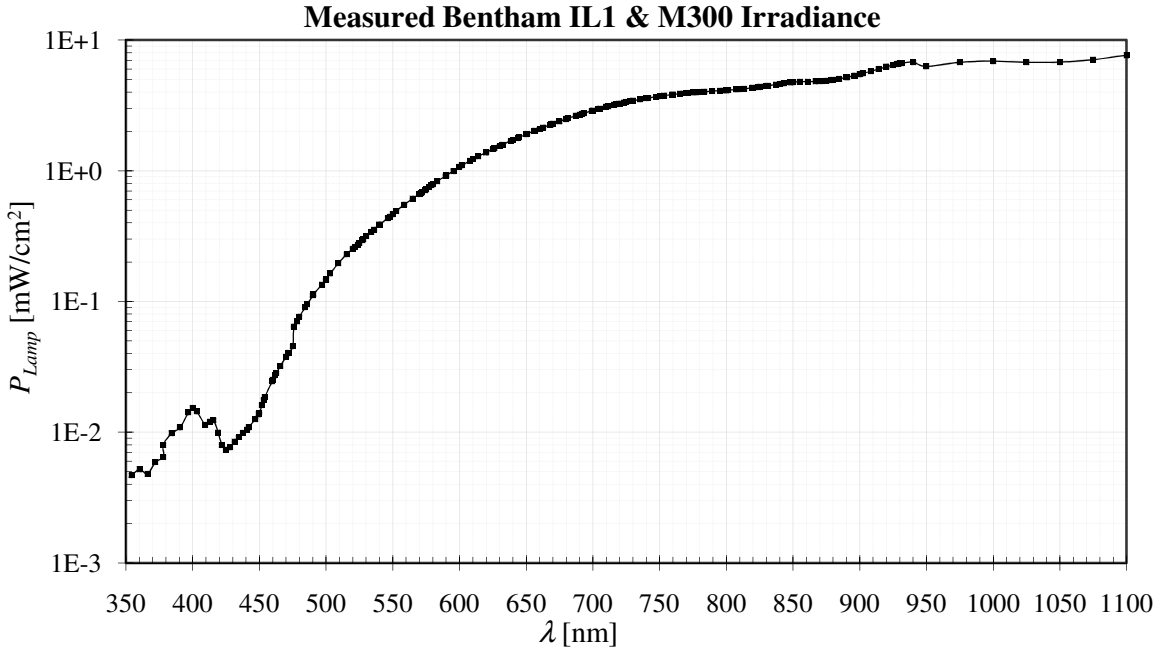

Figure B.1. Measured Bentham IL1 lamp and M300 monochromator output spectral irradiance.

The above optical source was then also measured with the spectrometer and the count per irradiance sensitivity calculated as shown Figure B.2.

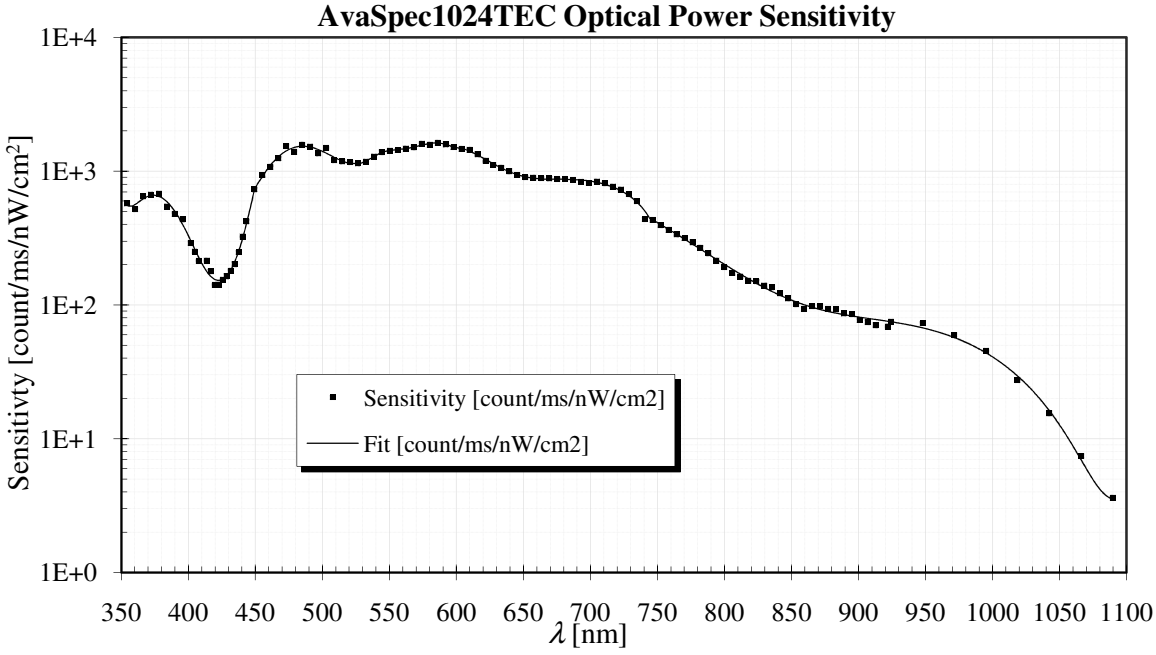

Figure B.2. Measured AvaSpec1024TEC spectral power sensitivity.

ADDENDUM C: DESIGN RULES

This addendum lists the self-determined design rules that were adhered to.

C.1. Si Island

Si islands remaining on BOx after etching.

1.1. Width	≥ 6 µm
1.2. Spacing	≥ 10 µm

C.2. Finger Spacing (EBL)

Island area between fingers etched away by RIE so that fingers remain.

2.1. Width (Finger spacing)	≥ 100 nm
2.2. Spacing (Finger width)	≥ 100 nm
2.3. Extension out of Si Island	≥ 2 µm
2.4. Extension out of As ≥ worst case(Rp_{As} + 3straggle$_{lateral}$ + w_d)	≥ 0.2 µm
2.5. Overlap into Si Island	≥ 2 µm

C.3. Oxidation (Photo)

Window to oxidize wide fingers and monitor finger oxidation.

3.1. Width	≥ 6 µm
3.2. Spacing	≥ 4 µm
3.3. Extension out of Si Island	≥ 2 µm
3.4. Overlap into Si Island	≥ 2 µm

C.4. Oxidation (EBL)

Window over fine fingers to be thinned by oxidation.

4.1. Width	≥ 100 nm
4.2. Spacing	≥ 540 nm
4.3. Extension out of Si Island	≥ 2 µm
4.4. Overlap into Si Island	≥ 2 µm

C.5. As (Photo)

Large-area As implant.

5.1. Width	≥ 6 µm
5.2. Spacing	≥ 4 µm
5.3 Spacing to Island	≥ 2 µm
5.4 Spacing to Finger Spacing	≥ 2 µm
5.5 Spacing to Oxidation (EBL)	≥ 2 µm
5.6. Extension out of Si Island	≥ 2 µm
5.7. Overlap of Si Island	≥ 2 µm
5.8. Overlap of Oxidation	≥ 2 µm

C.6. As (EBL)

Small-area As implant.

6.1. Width		≥ 100 nm
6.2. Spacing	≥ worst case{2(range + 3straggle$_{lateral}$) + w_d}	≥ 330 nm
6.3. Overlap of Si Island		≥ 2 µm
6.4. Overlap of Finger Spacing		≥ 10 nm
6.5. Overlap of Oxidation (EBL)		≥ 10 nm
6.6. Overlap of As (Photo)		≥ 2 µm

C.7. Contact

Metal contact to Island.

7.1. Width	≥ 6 µm
7.2. Spacing	≥ 10 µm
7.3. Spacing to Finger Spacing	≥ 2 µm
7.4. Spacing to (any) Oxidation	≥ 2 µm
7.5. Surround by Si Island	≥ 2 µm

C.8. Metal

Metal interconnect.

8.1. Width	≥ 10 µm
8.2. Spacing	≥ 10 µm
8.3. Spacing to Finger Spacing	≥ 2 µm
8.4. Spacing to (any) Oxidation	≥ 2 µm
8.5. Surrounding Contact	≥ 2 µm

ADDENDUM D: PROCESS CHARACTERIZATION DATA

This addendum characterizes the used processing equipment by plotting and analyzing self-measured rate information.

D.1. Oxidation Rates

Figure D.3 plots the measured thermal oxidation rate observed for the Lindburg furnace at the GT MiRC.

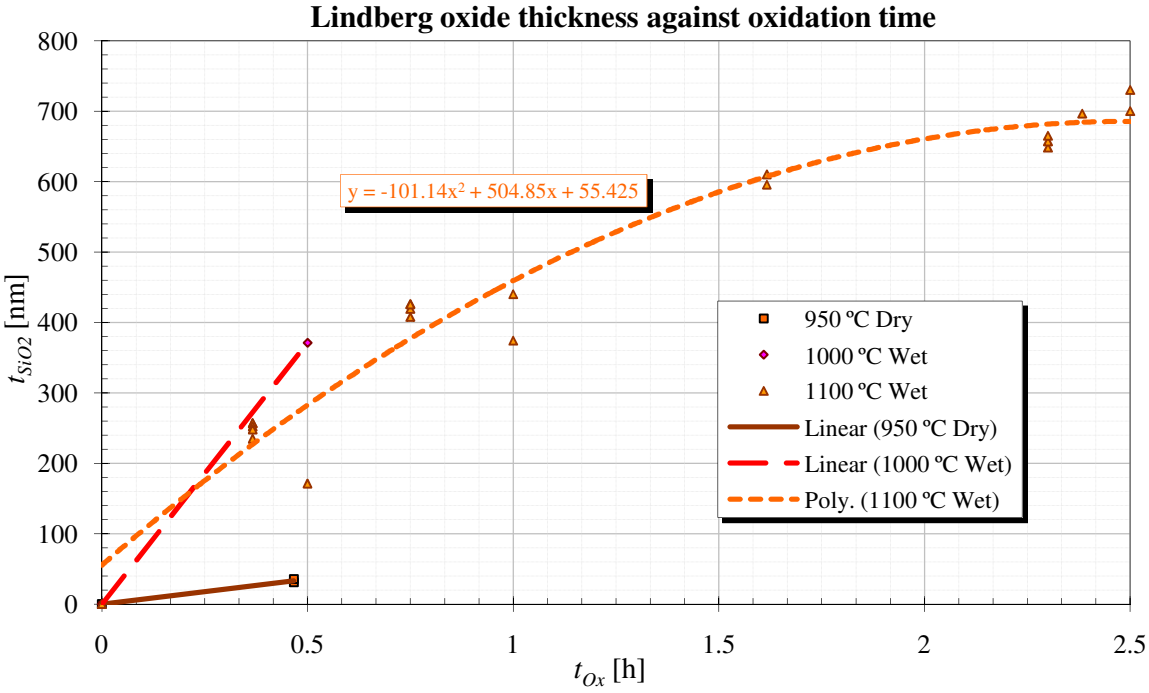

Figure D.3. Measured Lindburg furnace Si oxidation rates.

D.2. BOE Etch Rates

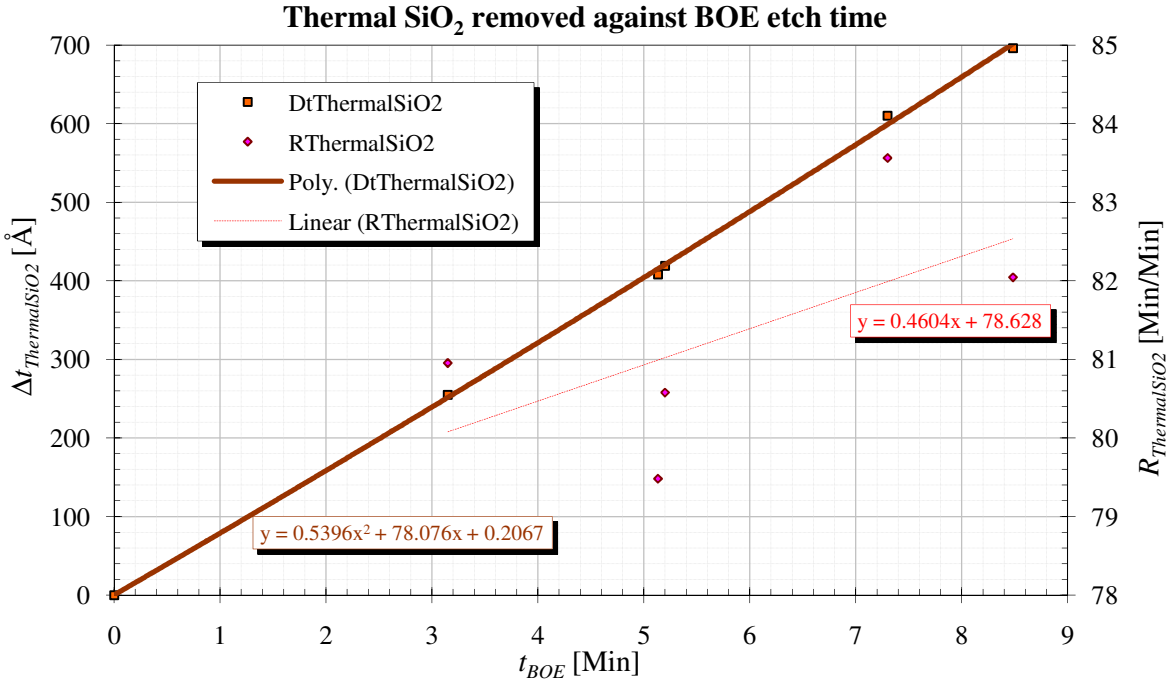

Figure D.4. Measured BOE etch rates of thermal SiO_2.

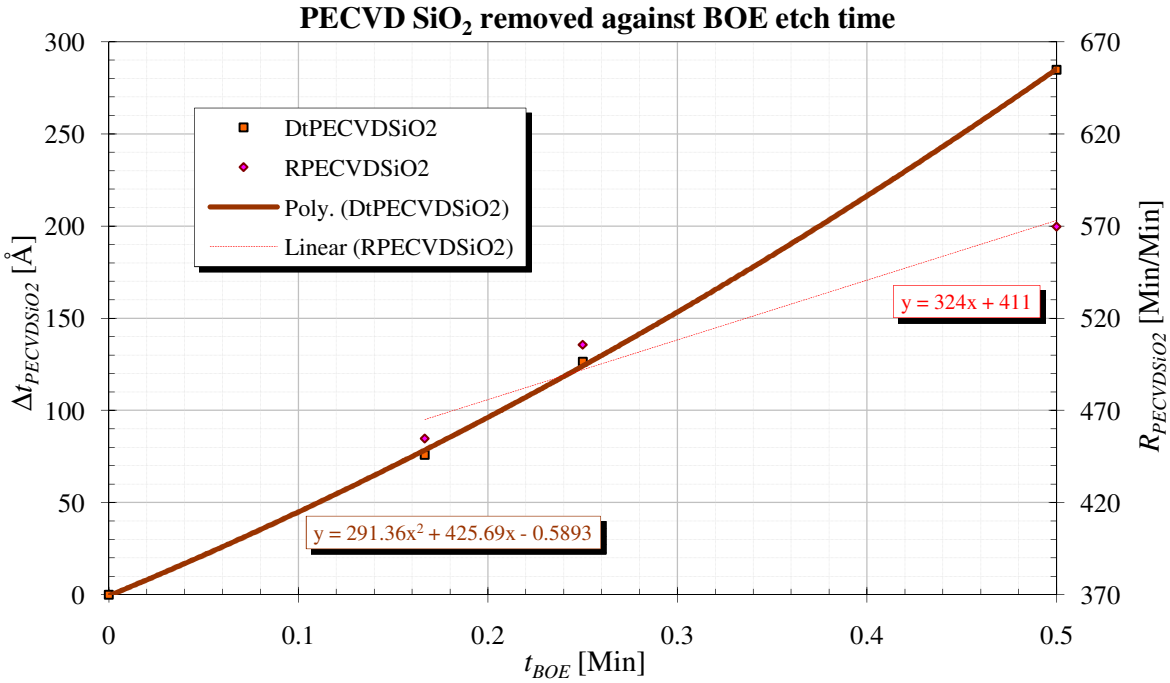

Figure D.5. Measured BOE etch rates of PECVD SiO_2.

D.3. Unaxis PECVD Deposition Rates

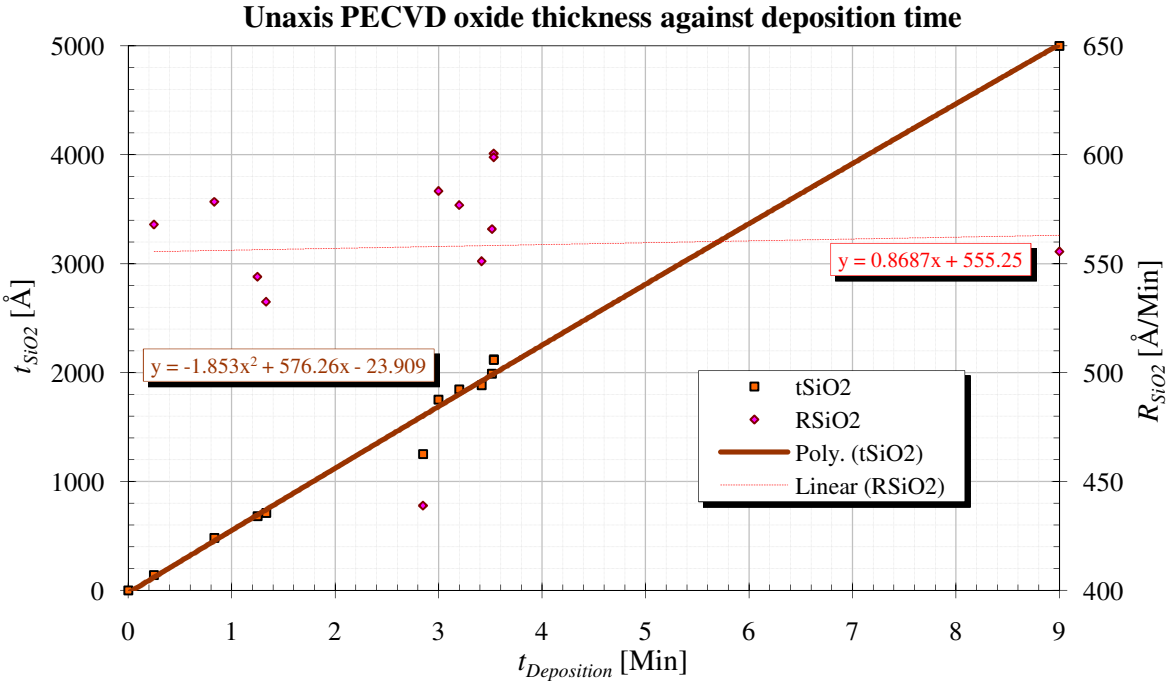

Figure D.6. Measured Unaxis PECVD SiO_2 deposition rates.

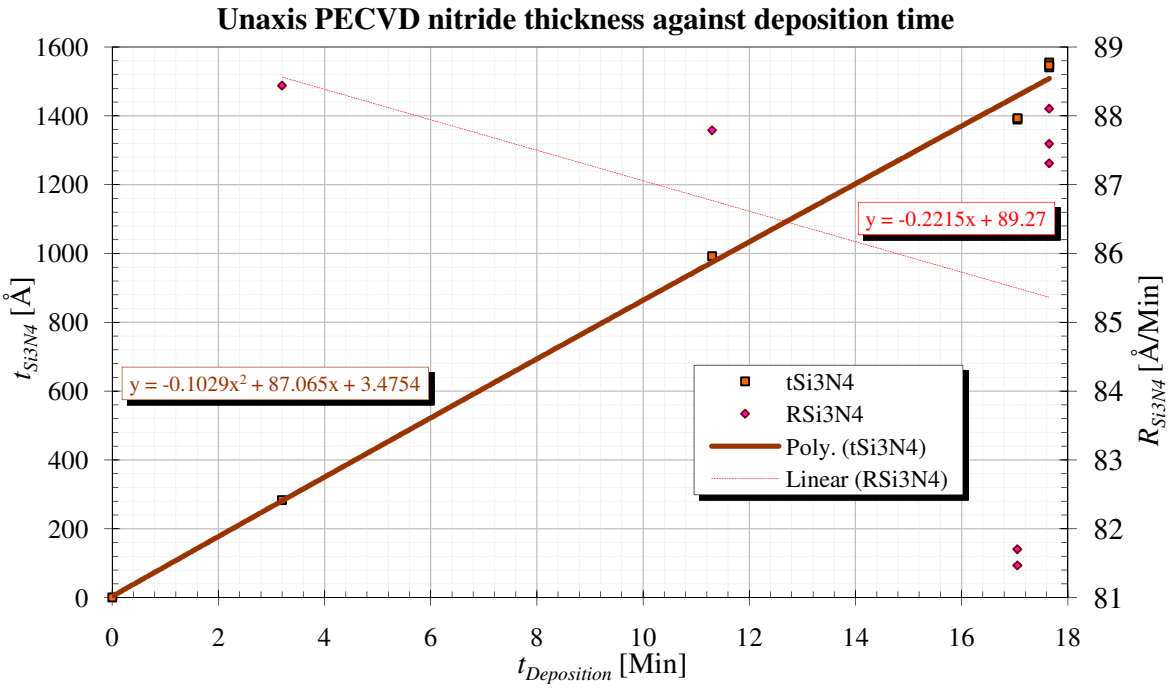

Figure D.7. Measured Unaxis PECVD Si_xN_y deposition rates.

D.4. Vision RIE Etch Rates

D.4.1. Summary

Table 8.2. Average Vision RIE etch rate summary.

Average Etch Rate [Å/Min]			Recipe		
			Si	Oxide	Nitride
Material	Si		2 297	127	
	SiO_2	PECVD	25	186	
		Thermal		129	80
	Si_xN_y		80	782	341
	SC1813		85	495	
	ZEP520A		114	252	

D.4.2. Silicon Recipe

D.4.2.1. Silicon

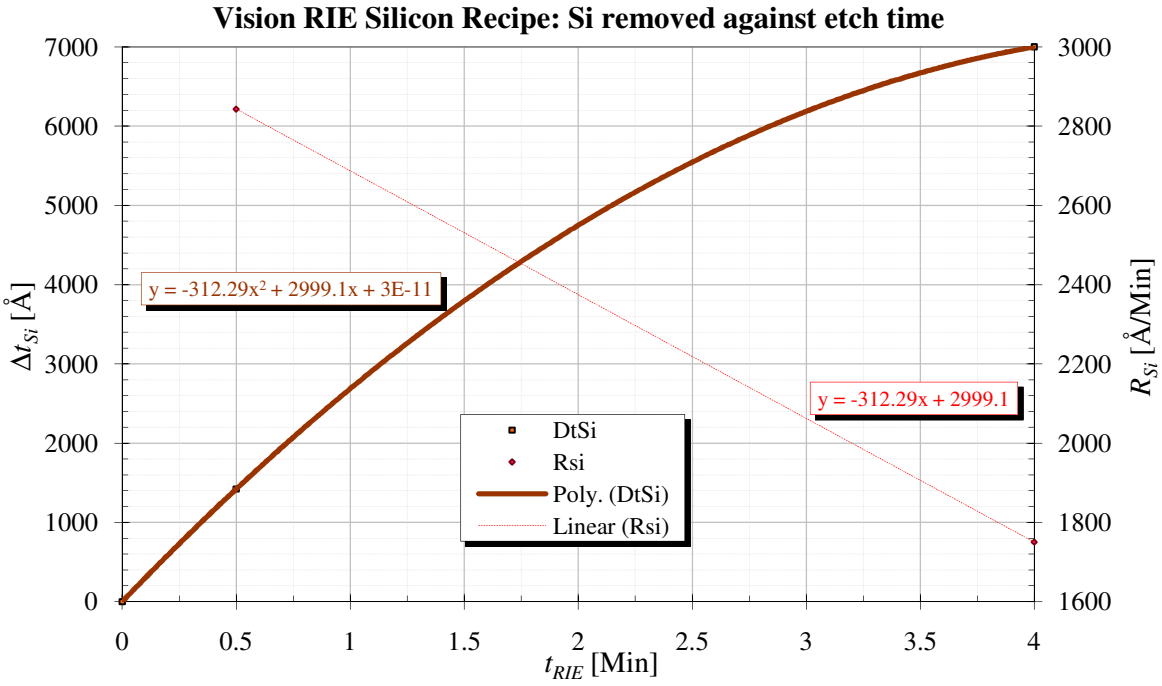

Figure D.8. Measured Si etch rate in Vision Oxide RIE Si recipe.

D.4.2.2. PECVD-SiO$_2$

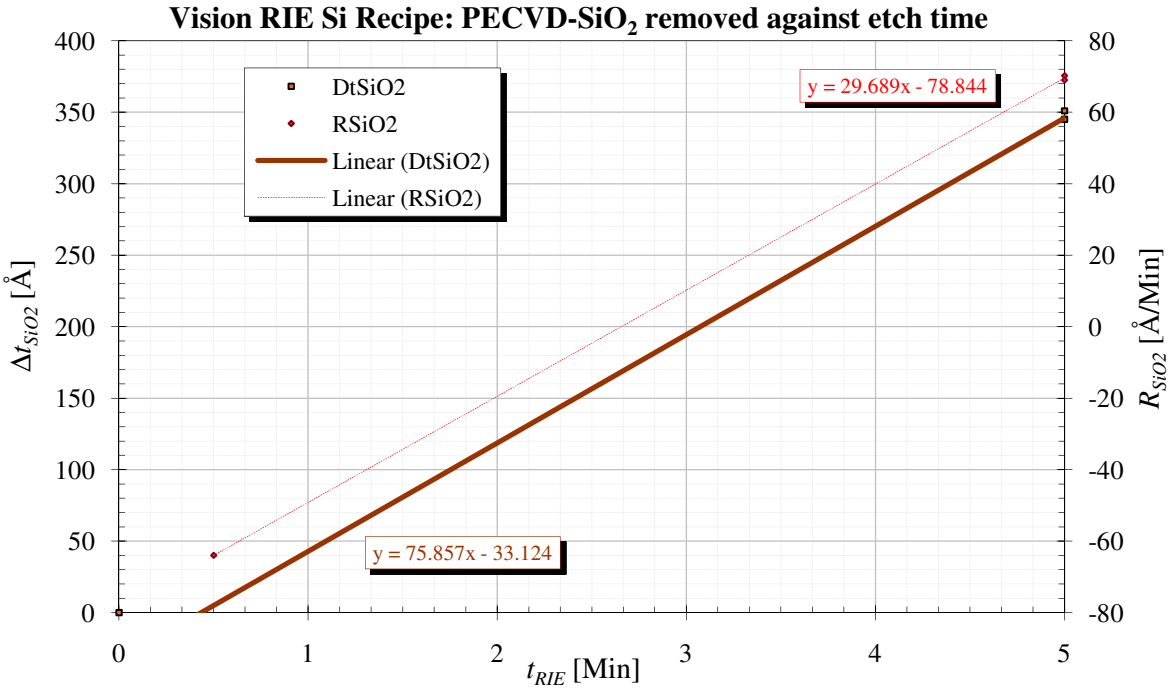

Figure D.9. Measured PECVD-SiO$_2$ etch rate in Vision Oxide RIE Si recipe.

D.4.2.3. Nitride

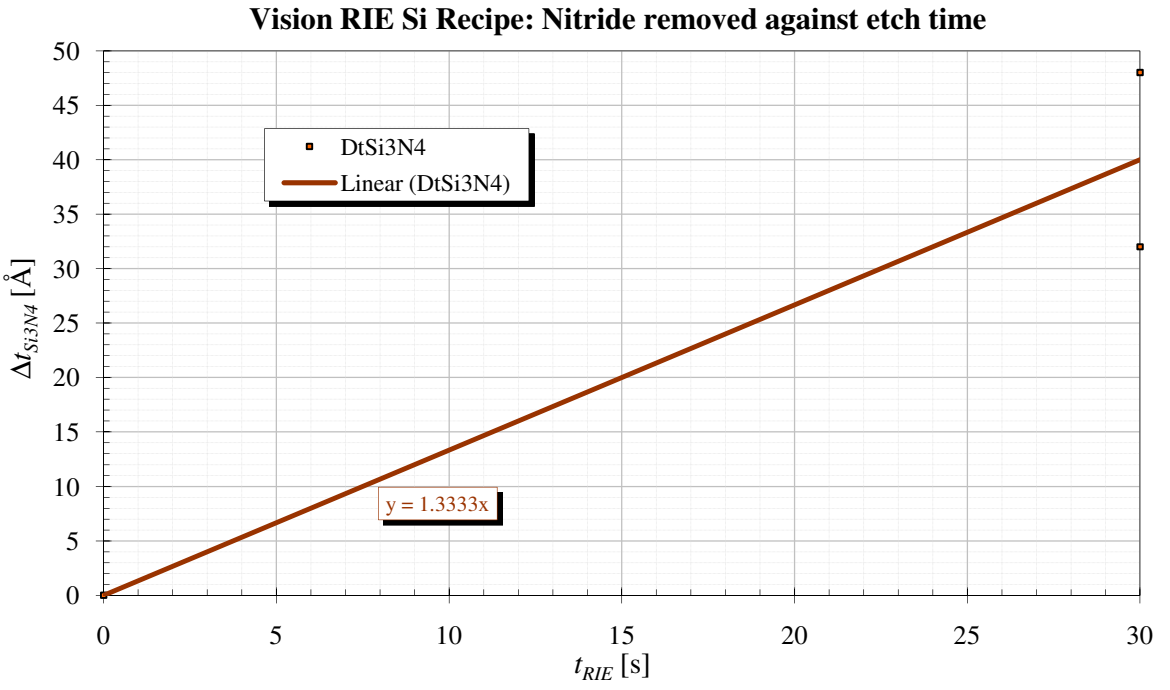

Figure D.10. Measured Si$_x$N$_y$ etch rate in Vision Oxide RIE Si recipe.

D.4.2.4. SC1813

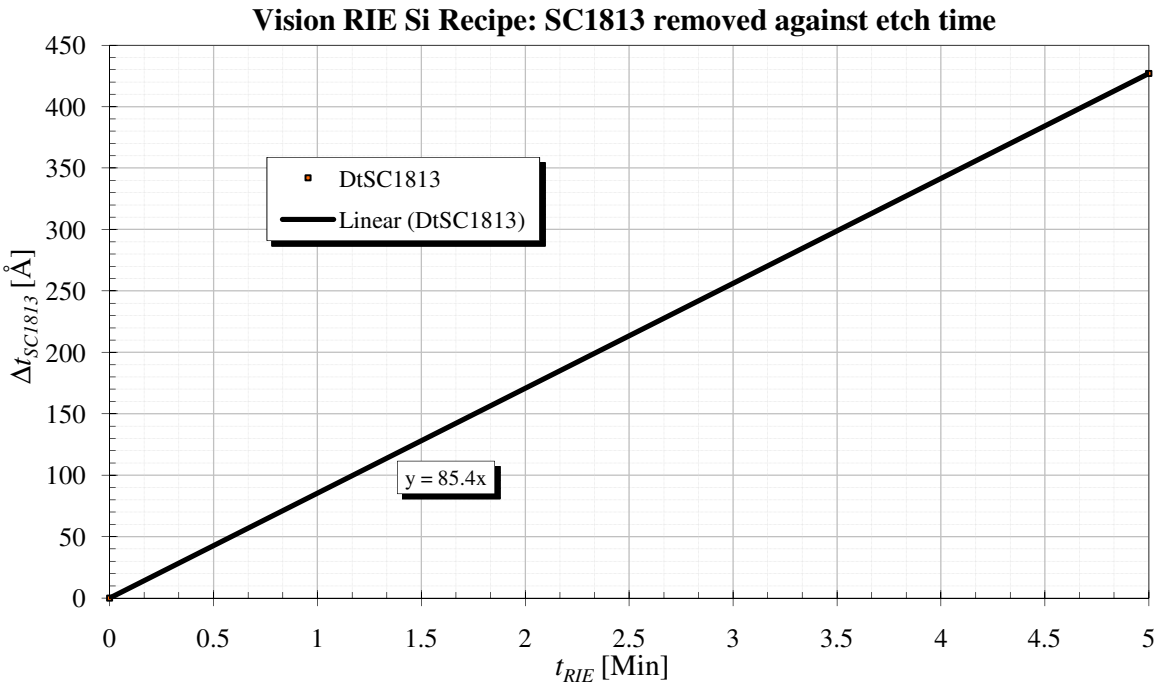

Figure D.11. Measured SC1813 etch rate in Vision Oxide RIE Si recipe.

D.4.2.5. ZEP520A

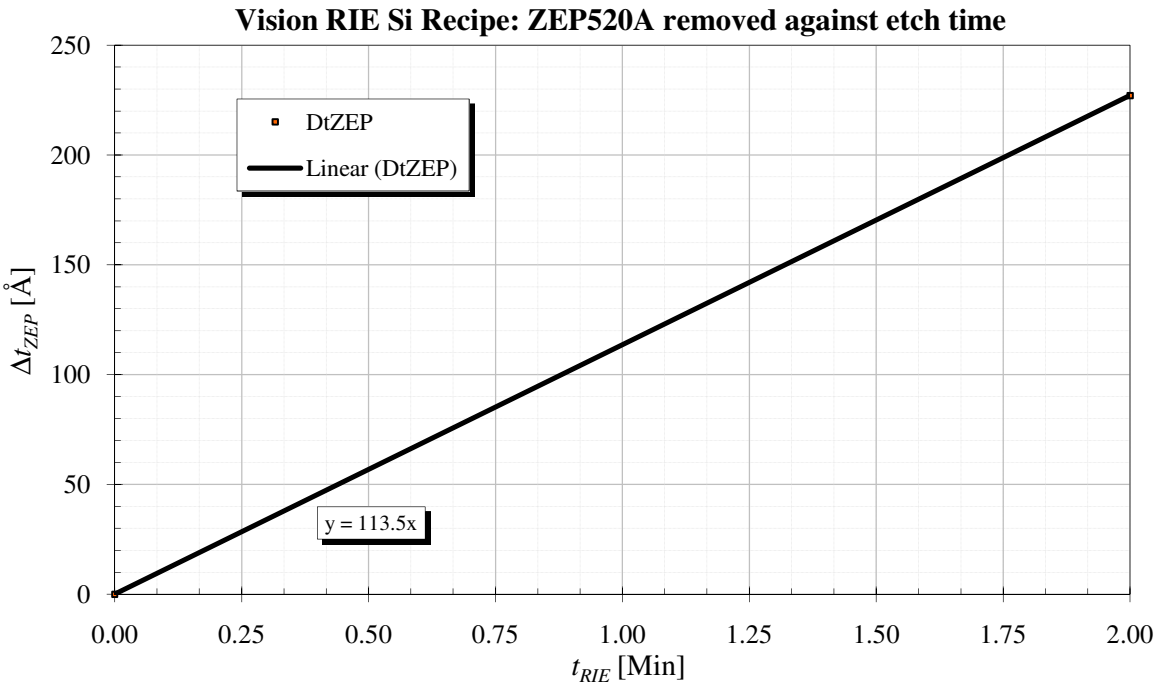

Figure D.12. Measured ZEP520A etch rate in Vision Oxide RIE Si recipe.

D.4.3. Standard Oxide Recipe

D.4.3.1. Silicon

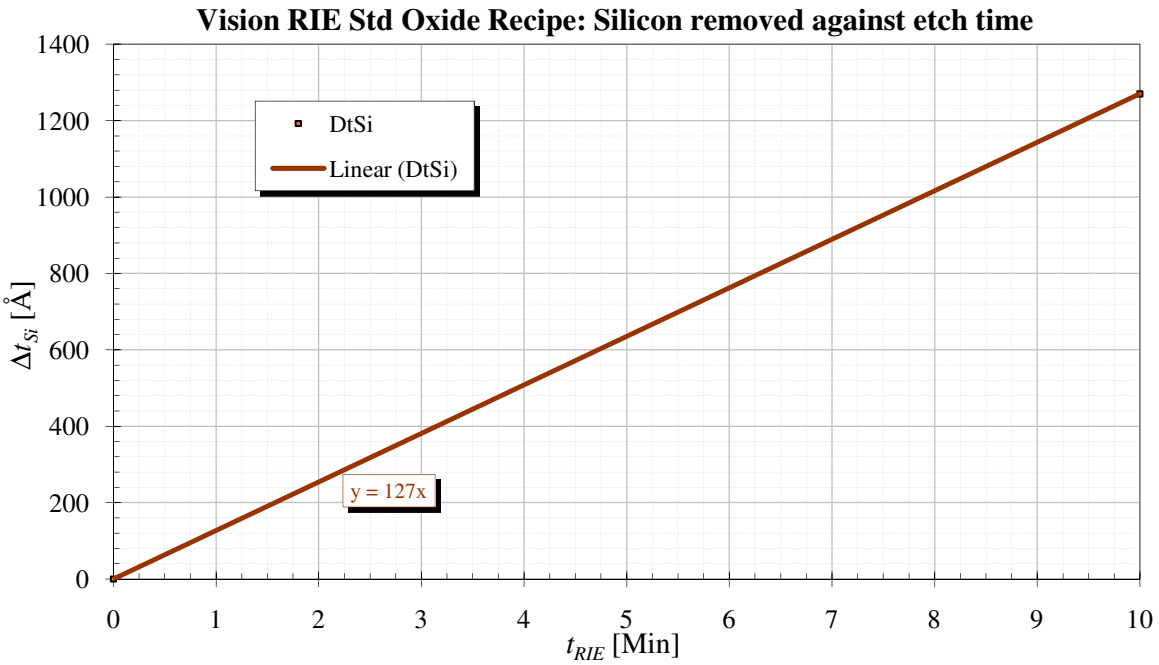

Figure D.13. Measured Si etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.2. PECVD-SiO_2

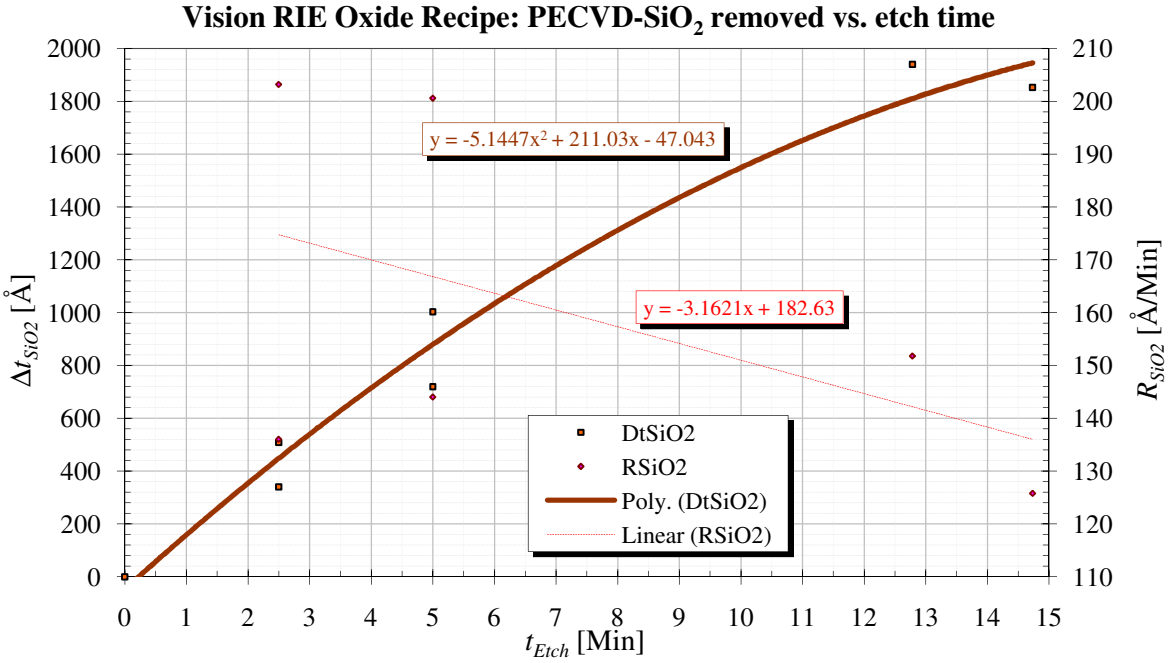

Figure D.14. Measured PECVD-SiO_2 etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.3. Thermal SiO_2

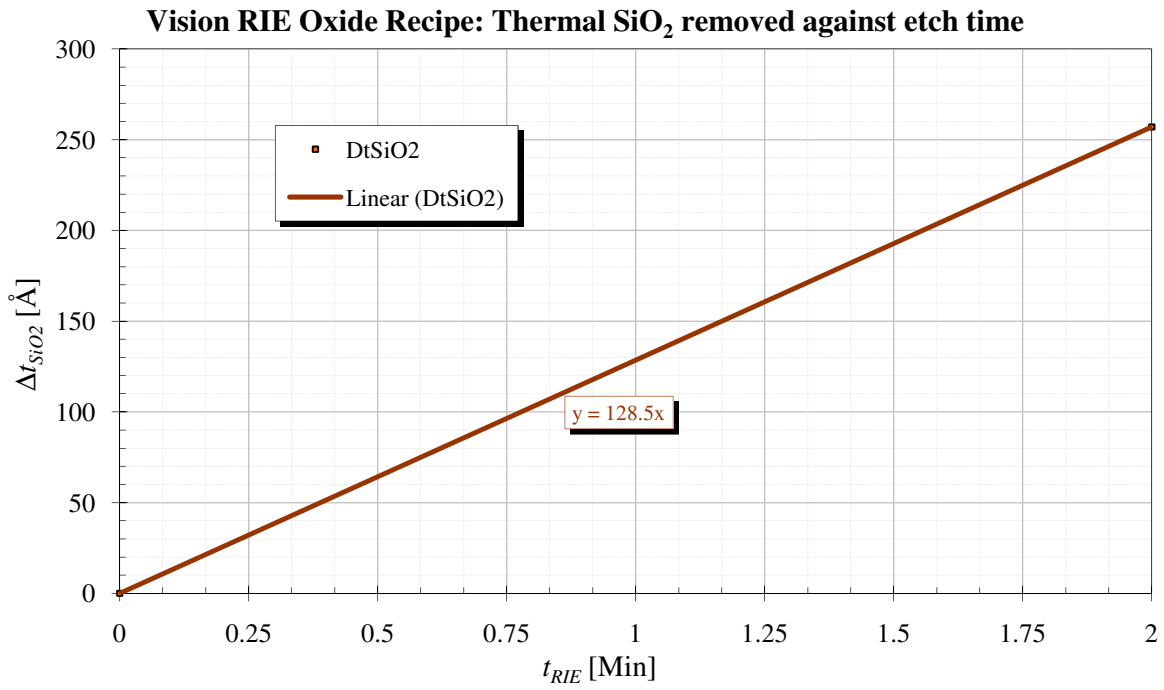

Figure D.15. Measured Thermal SiO_2 etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.4. Nitride

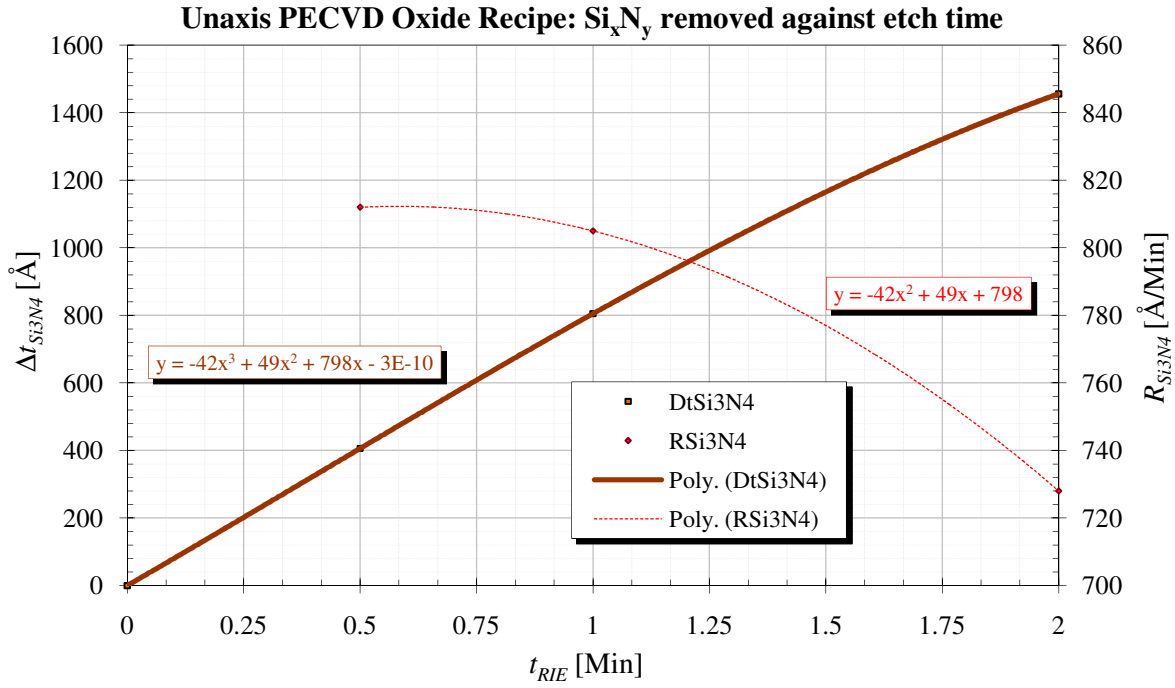

Figure D.16. Measured Si_xN_y etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.5. SC1813

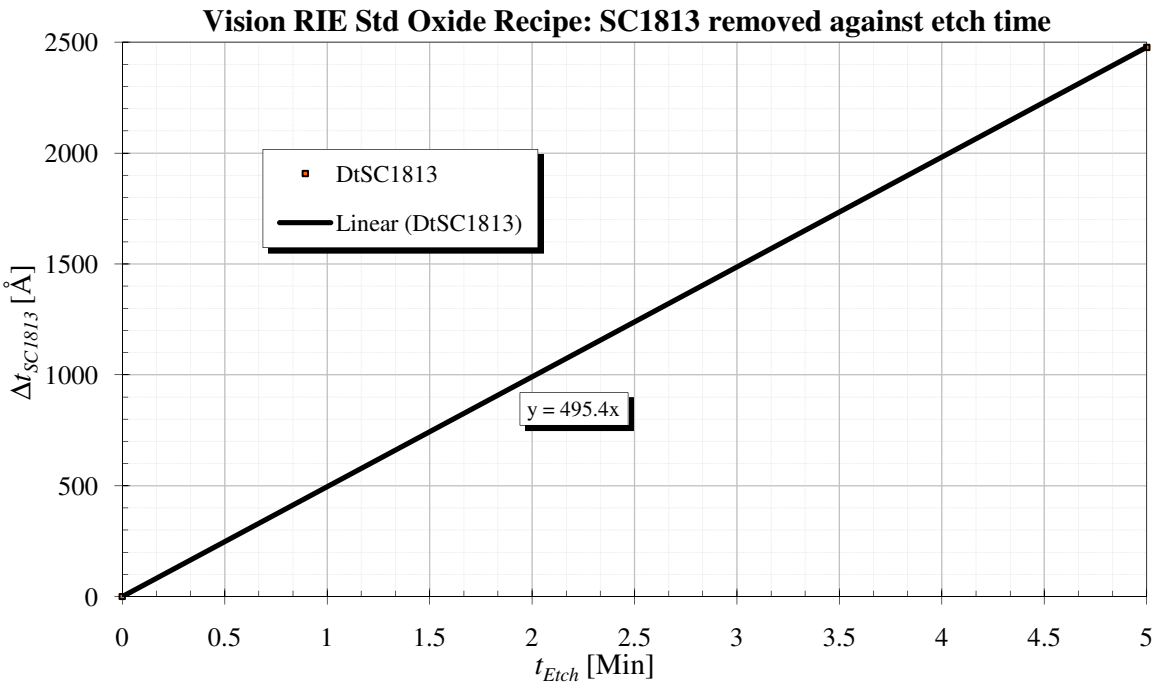

Figure D.17. Measured SC1813 etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.6. ZEP520A

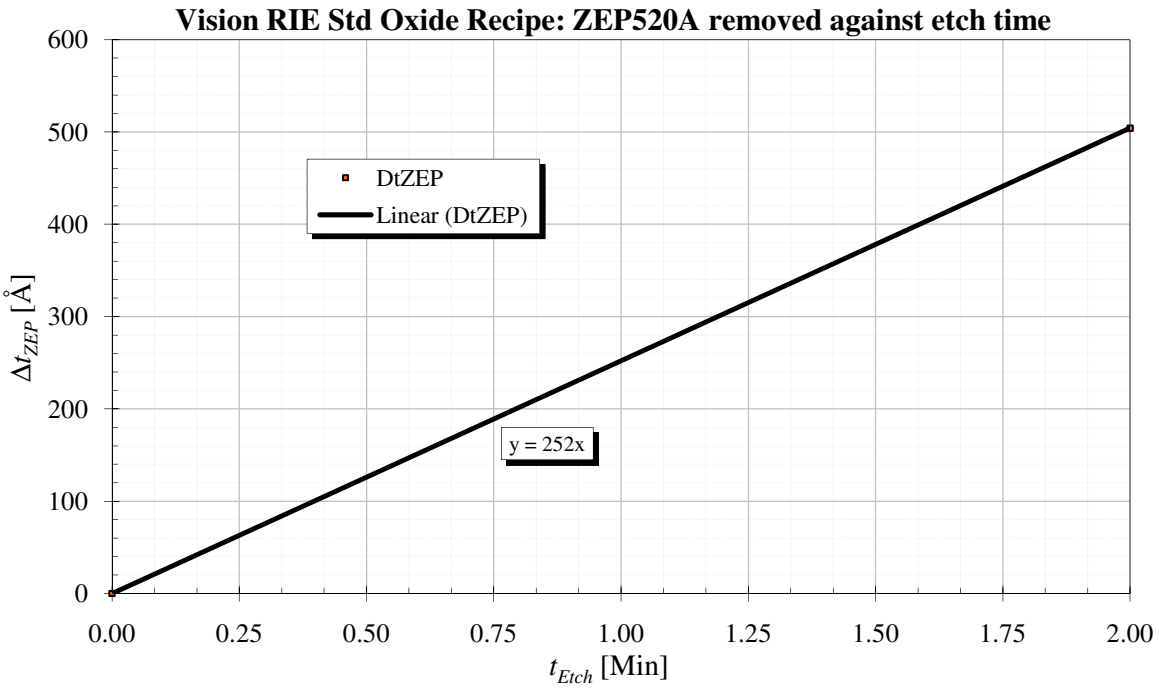

Figure D.18. Measured ZEP520A etch rate in Vision Oxide RIE standard oxide recipe.

D.4.4. Nitride Recipe

D.4.4.1. Thermal SiO_2

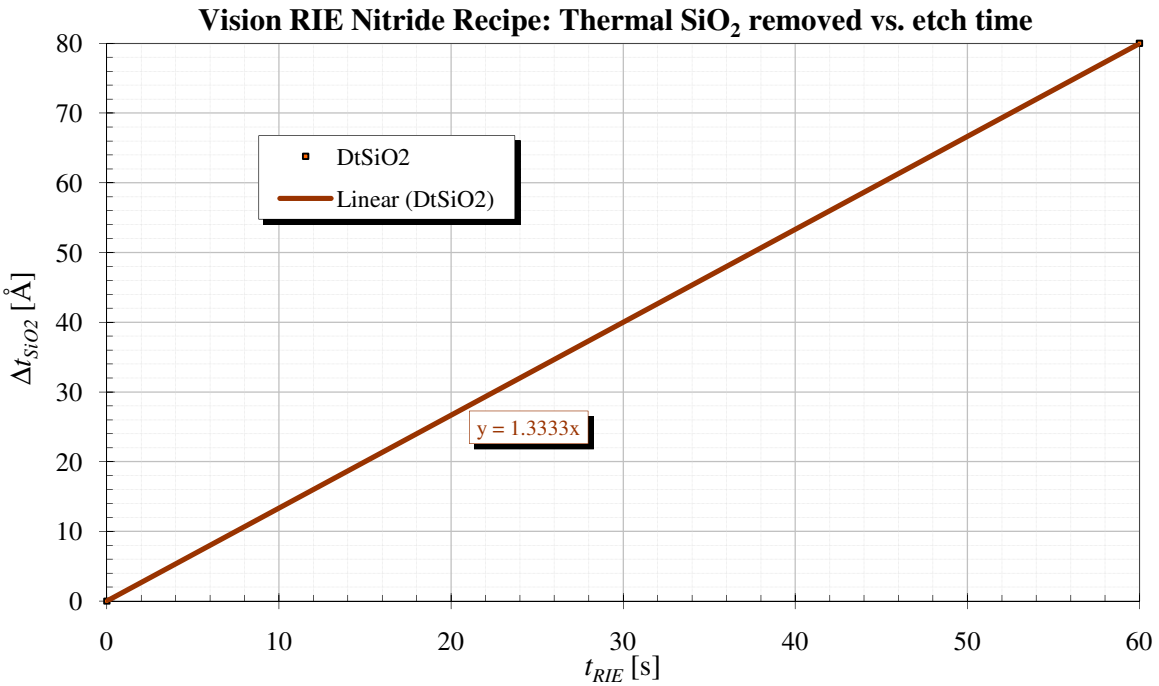

Figure D.19. Measured thermal SiO_2 etch rate in Vision Oxide RIE nitride recipe.

D.4.4.2. Si_xN_y

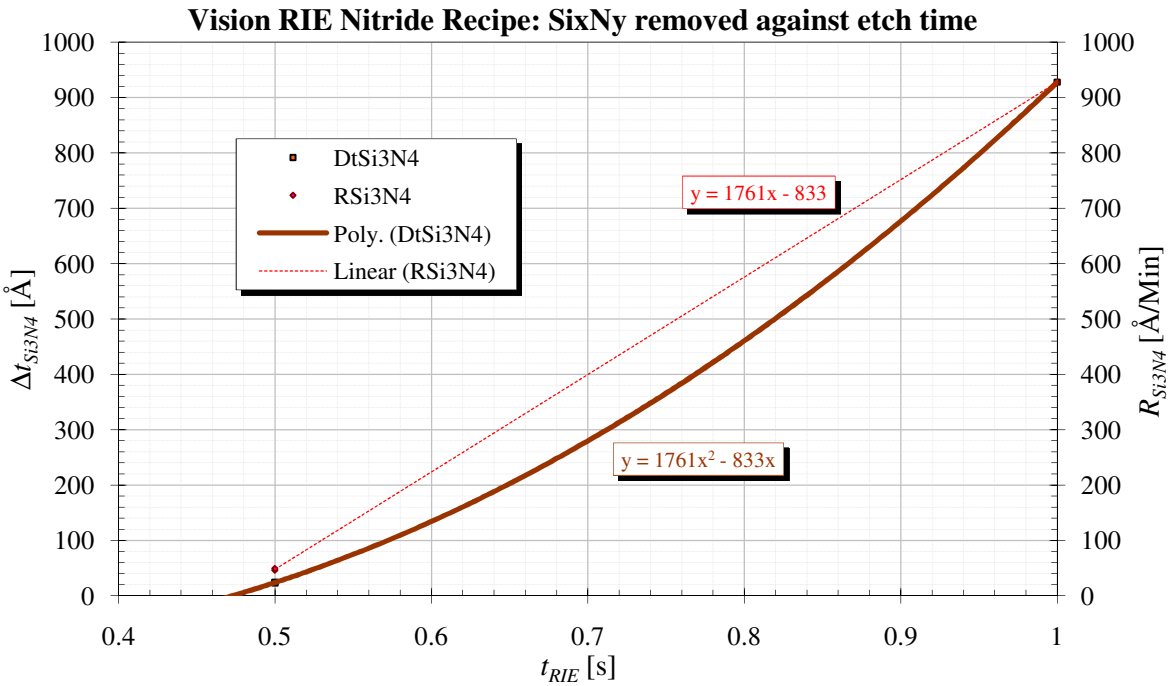

Figure D.20. Measured thermal Si_xN_y etch rate in Vision Oxide RIE nitride recipe.

ADDENDUM E: EBL WRITE TIMES

Table 8.3. EBL write time contributions per wafer.

Chip	Pattern					
	As	***Finger Spacing***	***Oxidation***	***As***	***Finger Spacing***	***Oxidation***
#	[µm^2]			[%] of Total		
1	118 437	279	22 665	13	0	2
2	60 772	284	3 484	7	0	0
3	227 898	25 285	50	25	3	0
4	429 400	25 274	61	47	3	0

	$A_{Cluster}$	836 507	51 122	26 260	[µm^2]
$n_{Clusters}$/wafer	4	3 346 029	204 489	105 038	
	A_{Wafer}	$3.3 \cdot 10^{-2}$	$2.0 \cdot 10^{-3}$	$1.1 \cdot 10^{-4}$	[cm^2]
	Dose	200			[µC/cm^2]
	I_{Beam}	2			[nA]
	t_{Write}	3 346	204	105	[s/wafer]
		56	3	2	[Min/wafer]
	t_{Align}	45			
	t_{Wafer}	101	48	47	
		1.7	0.8	0.8	[h/wafer]
n_{Wafer}	4	**7**	**3**	**3**	[h]
	t_{Total}	**13**			

Writing four wafers was estimated to take approximately 13 hours, but the final times were significantly longer since wafer and beam alignment and general set-up was found to be more time consuming than expected.