8. REFERENCES

[1] EA Steinman, VV Kveder, VI Vdovin and HG Grimmeiss, "The Origin and Efficiency of Dislocation Luminescence in Si and its Possible Applications in Optoelectronics", Solid State Phenomena 69-70, 1999, pg. 23 – 32.

[2] Plummer, Deal & Griffin, *Silicon VLSI Technology Fundamentals, Practice and Modeling*, Prentice Hall, Upper Saddle River, NJ, 2000.

[3] V Stenger, "Vertical multimode interference optical waveguide taps for silicon CMOS circuits", Ph.D. dissertation, Division of Research and Advanced Studies, Department of Electrical and Computer Engineering and Computer Science, College of Engineering, University of Cincinnati, 2003.

[4] L Chao, "Intel Technology Journal", Vol. 8, Issue 2, 10 May 2004, ISSN 1535-864X.

[5] RA Soref, "Silicon-Based Optoelectronics", Proceedings of the IEEE, Vol. 81, No. 12, December 1993, pg. 1687.

[6] R Newman, WC Dash, RN Hall and WE Burch, "Visible light from a Si p-n junction", Phys. Rev. Vol. 98 A, 1955, pg. 1536.

[7] A Chatterjee, B Bhuva and R Schrimpf, "High-Speed Light Modulation in Avalanche Breakdown Mode for Si Diodes", IEEE Electron Device Letters, Vol. 25, No. 9, September 2004, pg. 628.

[8] JC Tsang and JA Kash, "Picosecond hot electron light emission from submicron complementary metal–oxide–semiconductor circuits", Appl. Phys. Lett., Vol. 70, No. 7, 17 February 1997, pg. 889.

[9] A Chatterjee and B Bhuva, "High Speed CMOS - Si Light Emitters for On-Chip Optical Interconnect", Light-Emitting Diodes: Research, Manufacturing, and Applications VI, Proceedings of SPIE Vol. 4641, 2002, pg. 111.

[10] A Chatterjee and B Bhuva, "Accelerated Stressing and Degradation Mechanisms for Si-Based Photoemitters", IEEE Transactions on Device and Materials Reliability, Vol. 2, No. 3, September 2002, pg. 60.

[11] M de la Bardonnie, D Jiang, SE Kerns, DV Kerns Jr., P Mialhe, J-P Charles and A Hoffman, "On the Aging of Avalanche Light Emission from Silicon Junctions", IEEE Transactions On Electron Devices, Vol. 46, No. 6, June 1999, pg. 1234.

[12] SK Tewksbury, *Semiconductor Materials*, Microelectronic Systems Research Center, Dept. of Electrical and Computer Engineering, West Virginia University, Morgantown, WV 26506, 21 Sept. 1995, pg. 12.

[13] M Paniccia, V Krutul, R Jones, O Cohen, J Bowers, A Fang, H Park, "A Hybrid Silicon Laser: Silicon photonics technology for future tera-scale computing", White Paper, Research at Intel, September 2006.

[14] AW Fang, H Park, R Jones, O Cohen, MJ Paniccia, and JE Bowers, "A Continuous-Wave Hybrid AlGaInAs–Silicon Evanescent Laser", IEEE Photonics Technology Letters, Vol. 18, No. 10, 15 May 2006, pg. 1143.

[15] AR Wilkinson, "The Optical Properties of Silicon Nanocrystals and the Role of Hydrogen Passivation", Doctor of Philosophy Thesis, Australian National University, January 2006.

[16] R Stömmer, "Improvement of the direct optical transition probability in Si by wavefunction engineering", Appl. Phys. B, Vol. 82, 2006, pg. 627–631.

[17] V Kumar, *Nanosilicon*, Chapter 1 by N Daldosso and L Pavesi: "Low dimensional silicon as a photonic material", Elsevier, 2005.

[18] O Kwon, J Boeckl, ML Lee, AJ Pitera, EA Fitzgerald and SA Ringela, "Growth and properties of AlGaInP resonant cavity light emitting diodes on Ge/SiGe/Si substrates", Journal Of Applied Physics 97, Article 034504, 2005.

[19] Lorenzo Pavesi, "Routes toward silicon-based lasers", MaterialsToday, ISSN:1369 7021, Elsevier Ltd, January 2005, pg. 18.

[20] M E Castagna, S Coffa, A Muscara', A Costa, S Ravesi, S Lorenti, M Camalleri, "Si-based Resonant Cavity Light Emitting Devices", Light-Emitting Diodes: Research, Manufacturing, and Applications VIII, Proceedings of SPIE, Vol. 5366, SPIE, Bellingham, WA, 2004, pg. 26.

[21] H Röcken, "Optoelektronische Bauelemente durch fokussierende Ionenprojektion: Nanostrukturierte weiße Silizium-Leuchtdioden für Raumtemperaturbetrieb", Dissertation zur Erlangung des Grades eines Doktors der Naturwissenschaften in der Fakultät für Physik und Astronomie der Ruhr-Universität Bochum, Bochum 2002.

[22] P Jaguiro, P Katsuba, S Lazarouk and A Smirnov, "Porous Silicon Avalanche LEDs and their Applications in Optoelectronics and Information Displays", Proceedings of the International School and Conference on Optics and Optical Materials, ISCOM07, Belgrade, Serbia, Acta Physica Polonica A ,Vol. 112, No. 5, September 2007, pg. 1031.

[23] AR Chen, AI(T) Akinwande and H-S Lee, "CMOS-Based Microdisplay With Calibrated Backplane", IEEE Journal Of Solid-State Circuits, Vol. 40, No. 12, December 2005, pg. 2746.

[24] L Rebohle, T Gebel, RA Yankov, T Trautmann, W Skorupa, J Sun, G Gauglitz, R Frank, "Microarrays of silicon-based light emitters for novel biosensor and lab-on-a-chip applications", Optical Materials 27, Elsevier B.V., 2005, pp. 1055–1058.

[25] N Akil, VE Houtsma, P LeMinh, J Holleman, V Zieren, D de Mooij, PH Woerlee, A van den Berg and H Wallinga, "Modeling of light-emission spectra measured on silicon nanometer-scale diode antifuses", Journal of Applied Physics, Vol. 88, No. 4, 15 August 2008, pg. 1916.

[26] M Lahbabi, A Ahaitoufa, M Fliyou, E Abarkan, J-P Charles, A Bath, A Hoffmann, SE Kerns and DV Kerns Jr., "Analysis of electroluminescence spectra of silicon and gallium arsenide p–n junctions in avalanche breakdown", Journal of Applied Physics, Vol. 95, No. 4, 15 February 2004, pg. 1822.

[27] AT Fiory and NM Ravindra, "Light Emission from Silicon: Some Perspectives and Applications", Journal of Electronic Materials, Vol. 32, No. 10, 2003, pg. 1043.

[28] N Akil, SE Kerns, DV Kerns Jr., A Hoffmann and J-P Charles, "A Multimechanism Model for Photon Generation by Silicon Junctions in Avalanche Breakdown", IEEE Transactions on Electron Devices, Vol. 46, No. 5, May 1999, pg. 1022.

[29] T Puritis and J Kaupuzs, "Radiation Caused by Direct and Indirect Transitions in Silicon at Avalanche and Secondary Breakdown", Proc. 21st International Conference on Microelectronics (MIEL'97), Vol. 1, Nis, Yugoslavia, 14 - 17 September 1997, pg. 161.

[30] "IR -94 Annual Report", RDT&E Division, Naval Command, Control and Ocean Surveillance Centre, San Diego, CA 92152-5001, October 1994, pp. 57 - 80.

[31] JH Swoger and SJ Kovacic, "Enhanced luminescence due to impact ionization in photodiodes", J. Appl. Phys. 74 (4), 15 August 1993, pg. 2565.

[32] M Ruff, M. Fick, R Lindner, U Rössler and R Helbig, "The spectral distribution of the intrinsic radiative recombination in silicon", J. Appl. Phys., Vol. 74, No. 1, 1 July 1993, pg. 267.

[33] AL Lacaita, F Zappa, S Bigliardi and M Manfredi, "On the Bremsstrahlung Origin of Hot-Carrier-Induced Photons in Silicon Devices", IEEE Transactions on Electron Devices, Vol. 40, No. 3, March 1993, pg. 577.

[34] J Bude, N Sano and A Yoshii, "Hot-carrier luminescence in Si", Physical Review B, Vol. 45, No. 11, 15 March 1992, pg. 5848.

[35] S Tam, C Hu, "Hot-Electron-Induced Photon and Photocarrier Generation in Silicon MOSFET's", IEEE Transactions on Electron Devices, Vol. Ed. 31, No. 9, September 1984, pg. 1264.

[36] RP Gupta, WS Khokle, H Adachi and HL Hartnagel, "A new avalanche-plasma Si light emitter and its physical analysis", J. Phys. D: Appl. Phys., Vol. 14, 1981, pp. L31 – L34.

[37] DJ Rose, "Microplasmas in Silicon", Physical Review, Vol. 105, No. 2, 15 January 1957, pg. 413.

[38] M du Plessis, H Aharoni and LW Snyman, "Two- and multi-terminal CMOS/BiCMOS Si LEDs", Optical Materials, Vol. 27, 2005, pg. 1059 - 1063.

[39] LW Snyman, JM Matjila, H Aharoni and M du Plessis, "Increasing the efficiency of a three-terminal silicon CMOS LED through current density and carrier injection techniques", Proceedings of the 12th IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications, EDMO 2004, Kruger National Park, South Africa, pp. 71-82, 8-9 November 2004.

[40] H Aharoni and M du Plessis, "Low-operating-voltage integrated silicon light-emitting devices", IEEE Journal of Quantum Electronics, Vol. 40, No. 5, May 2004, pg. 557.

[41] LW Snyman, H Aharoni, M du Plessis, JFK Marais, D van Niekerk and A Biber, "Planar light-emitting electro-optical interfaces in standard silicon complementary metal oxide semiconductor integrated circuitry", Optical Engineering, Vol. 41, No. 12, pp. 3230-3240, December 2002.

[42] M du Plessis, H Aharoni and LW Snyman, "Silicon LEDs fabricated in standard VLSI technology as components for all silicon monolithic integrated optoelectronic systems", IEEE Journal of Selected Topics in Quantum Electronics, Vol. 8, Issue 6, November 2002, pp. 1412-1419.

[43] M du Plessis, H Aharoni, and LW Snyman, "Spatial and Intensity Modulation of Light Emission from a Silicon LED Matrix", IEEE Photonics Technology Letters, Vol. 14, No. 6, June 2002, pg. 768.

[44] M du Plessis, H Aharoni and LW Snyman, "A silicon transconductance light emitting device (TRANSLED)", Sensors and Actuators A, Vol. 80, 2000, pg. 242.

[45] LW Snyman, M du Plessis, E Seevinck and H Aharoni, "An efficient low voltage, high frequency silicon CMOS light emitting device and electro-optical interface", IEEE Electron Device Lett., Vol. 20, 1999, pp. 614 - 617.

[46] LW Snyman, H Aharoni, M du Plessis and RBJ. Gouws, "Increased efficiency of silicon light emitting diodes in a standard 1.2 micron complementary metal oxide semiconductor technology", Optical Engineering, Vol. 37, No. 7, pp. 2133-2141, July 1998.

[47] T Hoang, P LeMinh, J Holleman and J Schmitz, "Strong efficiency improvement of SOI-LEDs through carrier confinement", IEEE Electron Device Letters, Vol. 28, No. 5, May 2007, pg. 383.

[48] H Tu, "High efficient infrared light emission from silicon LEDs", Doctor degree dissertation at the University of Twente, ISBN 978-90-365-2557-2, Wöhrmann print service, Zutphen, The Netherlands, 2007, pg. 105.

[49] S Saito, D Hisamoto, H Shimizu, H Hamamura, R Tsuchiya, Y Matsui, T Mine, T Arai, N Sugii, K Torii, S Kimura and T Onai, "Electro-luminescence from Ultra-thin silicon", Japanese Journal of Applied Physics, Vol. 45, No. 27, 2006, pp. L679-L682.

[50] A Karsenty, A Sa'ar, N Ben-Yosef and J Shappir, "Enhanced electroluminescence in silicon-on-insulator metal-oxide-semiconductor transistor with thin silicon, Applied Physics Letters, Vol. 82, No. 26, June 2003, pg. 4830.

[51] D Shir, BZ Liu, AM Mohammad, KK Lew and SE Mohney, "Oxidation of silicon nanowires", J. Vac. Sci. Technol. B, Vol. 24, No. 3, May/Jun 2006, pg. 1333.

[52] X Tang, X Baie, JP Colinge, A Crahay, B Katschmarsyj, V Scheuren, D Spôte, N Reckinger, F van de Wiele and V Bayot, "Self-aligned silicon-on-insulator nano flas memory device", Solid-state Electronics 44, 2000, pp. 2259-2264.

[53] SM SZE and KK Ng, *Physics of Semiconductor Devices*, John Wiley & Sons, Hoboken, New Jersey, 2007.

[54] AW Wieder, "Emitter Effects in shallow bipolar devices: Measurements and consequences", *IEEE Journal of solid-state circuits*, Vol. SC-15, no. 4, pg. 4, August 1980.

[55] S Moinian, M Brooke and J Choma, "BITPAR: Processed-derived bipolar transistor Parameterization", *IEEE Journal of solid-state circuits*, Vol. SC-21, no. 2, pg. 344, April 1986.

[56] LM Phuong, "Silicon Light Emitting Devices for Integrated Application", Ph.D. thesis, Twente University Press, University of Twente, 2003.

[57] O Jambois, H Rinnert, X Devaux and M Vergnat, "Photoluminescence of size-controlled silicon nanocrystallites embedded in SiO_2 thin films", Journal of Applied Physics, Vol. 98, Article 046105, 2005.

[58] PE Allen and DR Holberg, *CMOS Analog Circuit Design*, Holt, Rinehart and Winston Inc., Orlando, Florida, 1987.

[59] BJ Baliga, *Fundamentals of Power Semiconductor Devices*, Springer Science and Business Media, 2008, pg. 102.

[60] W-K Chen, *The Electrical Engineering Handbook*, Elsevier Academic Press, 2005.

[61] GE Jellison Jr., "Optical functions of silicon determined by two-channel polarization modulation ellipsometry", Optical Materials 1, North Holland, Elsevier Science Publishers B.V., 1992, pg. 41 - 47.

[62] GE Jellison Jr. and FA Modine, "Optical functions of silicon at elevated temperatures", Journal of Applied Physics, Vol. 76, No. 6, pg. 3760, 1994.

[63] C Anagnostopoulos and G Sadasiv, "Transmittance of Air/SiO_2 /Polysilicon/SiO_2 /Si Structures", IEEE Journal of Solid-state Circuits, pg. 177, June 1975.

[64] LAA Warnes, *Electronic Materials*, MacMillan Education Ltd, London, pg. 215, 1990.

[65] S Radovanovic, AJ Annema and B Nauta, *High-speed photodiodes in standard CMOS technology*, Springer, Dordrecht, The Netherlands, pg. 20, 2006.

[66] DM Brown, M Ghezzo and M Garfinkel, "Transparent Metal Oxide Electrode CID Imager", IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 1, February 1976, pg. 128.

[67] C-H Lee, Y Chiu, H-PD Shieh, "High-extinction-ratio micro polarizing beam splitter for short wavelength optical storage applications", Optics Express, Vol. 13, No. 25, 12 December 2005, pg. 10296.

[68] DK Cheng, *Fundamental Engineering Electromagnetics*, Addison-Wesley Publishing Company, Reading, Massachusetts, USA, pg. 207,1993.

[69] VM Aroutiounian, KR Maroutyan and P Soukiassian, "Low reflectance of diamond-like carbon/porous silicon double layer antireflection coating for silicon solar cells", J. Phys. D: Applied Phys., Vol. 37, pp L26-L27, 2004.

[70] S Gorantla, S Muthuvenkatraman and R Venkat, "A Model for Thermal Growth of Ultrathin Silicon Dioxide in O_2 Ambient: A Rate Equation Approach", IEEE Transactions on Electron Devices, Vol. 45, No. 1, January 1998, pp. 336.

[71] BE Deal and AS Grove, “General relationship for the thermal oxidation of silicon”, J. Appl. Phys., Vol. 36, No. 12, pp. 3770, 1965.

[72] Y Chen, “Modeling of the Self-Limiting Oxidation for Nanofabrication of Si”, EECS Department, University of California, 2415 California Street, Berkeley, CA 94720, Tel. 510-642-9210, mailto:chenyj@eecs.berkeley.edu.

[73] HI Liu, DK Biegelsen, FA Ponce, NM Johnson and RFW Pease, “Self-limiting oxidation for fabricating sub-5 nm silicon nanowires”, Appl. Phys. Lett., Vol. 64, No. 11, 14 March 1994, pg. 1383.

[74] H Matsumoto and M Fukuma, “Numerical Modeling of Nonuniform Si Thermal Oxidation”, IEEE Transactions on Electron Devices, Vol. ED-32, NO. 2, February 1985, pp. 132.

[75] CC Büttner and M Zacharias, “Retarded oxidation of Si nanowires”, Applied Physics Letters, Vol. 89, 2006, Article 263106.

[76] Y Chen and Y Chen, “Modeling silicon dots fabrication using self-limiting oxidation”, Microelectronic Engineering 57–58, Elsevier Science B.V., 2001, pp. 897–901.

[77] J Kedzierski, J Bokor and C Kisielowski, “Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation”, J. Vac. Sci. Technol., Vol. B 15(6), Nov/Dec 1997, pp. 285.

[78] CP Ho and JD Plummer, "Si/SiO2 Interface Oxidation Kinetics: A Physical Model for the Influence of High Substrate Doping Levels, I. Theory", J. Electrochem. Soc., Vol. 126, No. 9, 1979, pp. 1516-1522.

[79] T Kersys, R Anilionis and D Eidukas, “Simulation of Doped Si Oxidation in Nano-dimension Scale”, T171 Microelectronics, Electronics and Electrical Engineering, Kaunas: Technologija, ISSN: 1392-1215, No. 4(84), 2008, pp. 43 - 44.

[80] JA van Vechten and CD Thurmond, "Entropy of Ionization and Temperature Variation of Ionization Levels of Defects in Semiconductors," Physical Review B, Vol. 14, No. 8, 1976, pp. 3539-3550.

[81] GA Tarnavskii, SI Shpak and MS Obrecht, “Features of segregation of doping impurities of V(a) subgroup elements on angular configurations of the silicon/silicon dioxide oxidation boundary”, Journal of Engineering Physics and Thermophysics, Vol. 75, No. 1, 2002, pp. 190.

[82] SS Choi, "Temperature-dependant redistribution of arsenic impurities at the Si/SiO2 interface", Journal of the Korean Physical Society, Vol. 28, No. 6, December 1995, pp. 763 – 767.

[83] SS Choi and MJ Park, "Redistribution of arsenic during thermal oxidation of arsenic ion-implanted silicon", Journal of the Korean Physical Society, Vol. 24, No. 6, December 1991, pp. 499 - 505.

[84] Z Đurić, MM Smiljanić, K Radulović and Z Lazić, "Boron redistribution during SOI wafer thermal oxidation", Proc. 25th International Conference on Microelectronics (MIEL 2006), Belgrade, Serbia and Montenegro, 14 – 17 May 2006.

[85] K Suzuki and T Miyashita, "Models of Boron redistribution during thermal oxidation with general oxidation rate", IEEE Transactions on Electron Devices, Vol. 47, No. 3, March 2000, pp. 523.

[86] PH Ladbrooke, "Boron segregation data for D.M.O.S. devices", Electronics Letter, Vol. 14, No. 5, 2 March 1978, pp. 128.

[87] CP Wu, EC Douglas and CW Mueller, "Redistribution of ion-implanted impurities in Silicon during diffusion in oxidizing ambients", IEEE Transactions on Electron Devices, Correspondence, September 1976, pp. 1095.

[88] S Margalit, A Neugroschel and A Bar-Lev, "Redistribution of boron and phosphorous in silicon after two oxidation steps used in MOST fabrication", IEEE Transactions on Electron Devices, Vol. ED-19, No. 7, July 1972, pp. 861.

[89] SP Murarka, "Diffusion and segregation of ion-implanted boron in dry oxygen ambient", Physical Review B, Vol. 12, No. 6, 15 September 1975, pg. 2502.

[90] AF Saavedra, KS Jones, ME Law, KK Chan and EC Jones, "Electrical activation in silicon-on-insulator after low energy implantation", Journal of Applied Physics, Vol. 96, No. 4, 15 August 2004, pp. 1891.

[91] R Hull, "Properties of Crystalline Silicon", Electronic Materials Information Service (EMIS) Datareviews series, No. 20, An INPEC publication, IEE, 1999, pg. 737.

[92] K Chen, J Huang, Z Ma, X Wang, Y Yao, J Wang, W Li, J Xu and X Huang, "Charge storage and light emission properties of three dimension controllable Si nanostructures", Phys. Status Solidi, Vol. C6, No. 3, 2009, pp. 721 – 727.

[93] W Haecker, "Infrared radiation from breakdown plasmas in Si, GaSb, and Ge: Evidence for direct free hole radiation", Phys. Status Solidi (a), Vol. 25, 1974, pg. 301.

[94] RH Dyck, "THPM 6.5: Avalanche Luminescence in Silicon and its Utilization in a Monolithic Light Source Array", International Solid-State Circuits Conference, Session VI: Radiative Interconnections, Irvine Auditorium, Univ. of Pennsylvania, 18 February 1965, pg. 64.

[95] N Akil, SE Kerns, DV Kerns, Jr., A Hoffmann and J-P Charles, "A multimechanism model for photon generation by silicon junctions in avalanche breakdown", IEEE Transactions on Electron Devices, Vol. 46, No. 5, May 1999, pp. 1022-1028.

[96] D Bisero, F Corni, G Ottaviani, R Tonini and L Pavesi, "Infrared Light Emission Due To Radiation Damage in Crystalline Silicon", Solid State Commun., Vol. 101, No. 12, 1997, pp. 889–891.

ADDENDUM A: PHYSICAL CONSTANTS

Table A.1 below lists the numeric values of all physical constants used in this work ([53], pg. 788 - 790).

Table A.1. Physical constants used in this document.

Constant	Description	Value	Unit
c	Speed of light in vacuum	$2.9979245805 \cdot 10^{8}$	m/s
d_{Si}	Si density	2.329	g/cm^3
ε_0	Free space permittivity	$8.85418781762 \cdot 10^{-14}$	F/cm
ε_{rSi}	Si relative permittivity	11.6 - 11.8	-
ε_{SiO2}	SiO_2 relative permittivity	3.8 - 3.9	-
Eg_{Si}	Si energy band-gap	1.12	eV
$\hbar$	Planck's constant	$6.6260994816 \cdot 10^{-34}$ $4.1356673310 \cdot 10^{-15}$	J·s eV·s
k_B	Boltzmann's constant	$1.380658 \cdot 10^{-23}$	J/K
k_{Air}	Air extinction coefficient	0	-
k_{SiO2}	SiO_2 extinction coefficient	0	-
m_e	Electron mass	$9.10939 \cdot 10^{-31}$	kg
n_{i0}	Si intrinsic concentration	$1.45 \cdot 10^{10}$	cm^{-3}
n_{Air}	Air refractive index	1.00029	-
n_{SiO2}	SiO_2 refractive index	1.43 - 1.47	-
n_{SixNy}	Si_xN_y refractive index	2.0	-
q	Electron charge	$1.60218 \cdot 10^{-19}$	C
T	Absolute temperature	300	K

ADDENDUM B: SPECTROMETER

B.1. Spectrometer Details

Manufacturer:	Avantes, Netherlands
Model:	AvaSpec-2048TEC
Type:	Thermo-electrically cooled fibre-optic spectrometer
Specifications:	
Range:	200 – 1100 nm
Peltier cooling:	-25 - -30 ºC below room temperature
Stray light:	< 0.1 %
Optical resolution:	< 8 nm
AD resolution:	16 bit
Maximum integration time:	10 Min
Sensitivity:	40 ph/count
	$2 \cdot 10^4$ counts/µW/ms
SNR:	200:1
Noise:	560 ph_{rms}
Hardware configuration:	
Detector:	2048 pixel Sony ILX554B
Detector coating:	>150 nm deep UV
Slit width:	200 µm
Grating:	UA
Grating lines:	300 grooves/mm
Blaze wavelength:	500 nm
Grating coating:	Order sorting OSC-UA 350 and 590 nm long-pass filter
Lens:	Quartz DCL-UV/VIS 200 – 1100 nm
Manufactured:	August 2007
Location:	Optical Laboratory, CEFIM, University of Pretoria
Software:	AvaSoft Full version 7.1 USB1

B.2. Spectrometer Calibration

The spectrometer was calibrated by first measuring the spectral irradiance of the Betham IL1 and M300 monochromator as shown Figure B.1.

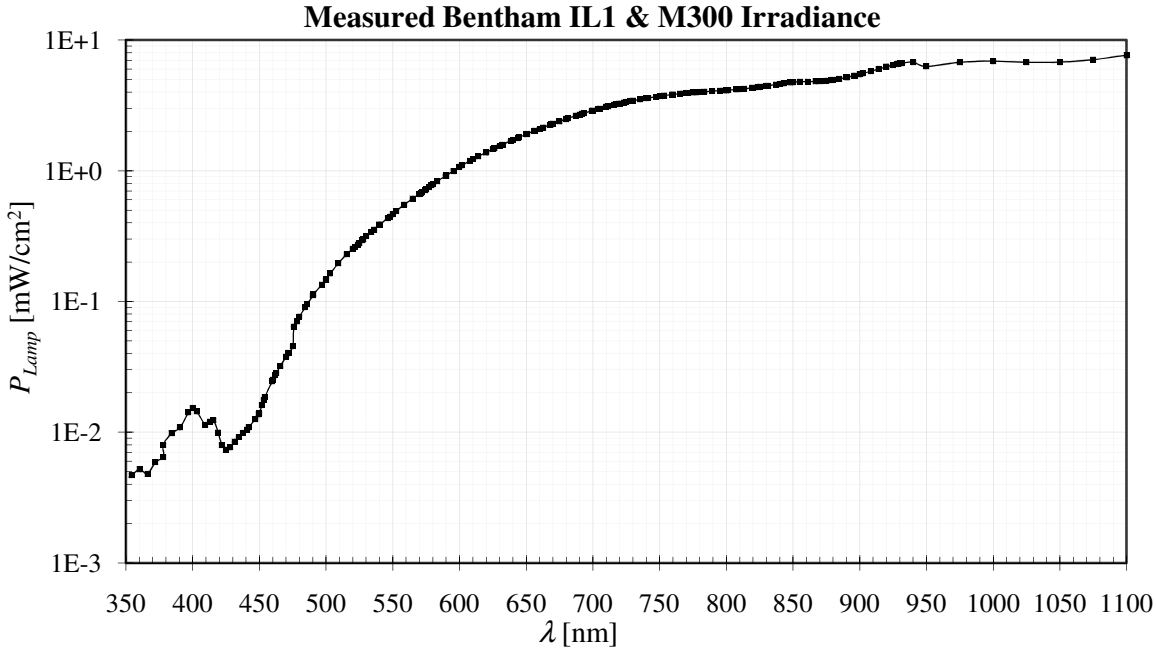

Figure B.1. Measured Bentham IL1 lamp and M300 monochromator output spectral irradiance.

The above optical source was then also measured with the spectrometer and the count per irradiance sensitivity calculated as shown Figure B.2.

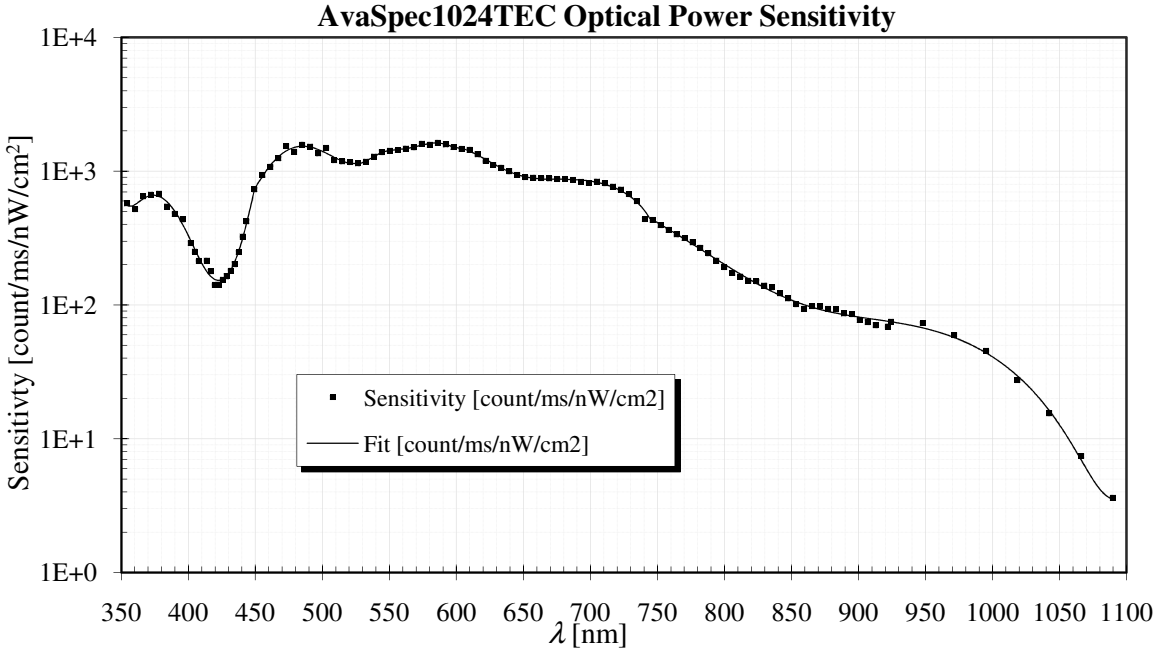

Figure B.2. Measured AvaSpec1024TEC spectral power sensitivity.

ADDENDUM C: DESIGN RULES

This addendum lists the self-determined design rules that were adhered to.

C.1. Si Island

Si islands remaining on BOx after etching.

1.1. Width	≥ 6 µm
1.2. Spacing	≥ 10 µm

C.2. Finger Spacing (EBL)

Island area between fingers etched away by RIE so that fingers remain.

2.1. Width (Finger spacing)	≥ 100 nm
2.2. Spacing (Finger width)	≥ 100 nm
2.3. Extension out of Si Island	≥ 2 µm
2.4. Extension out of As ≥ worst case(Rp_{As} + 3straggle$_{lateral}$ + w_d)	≥ 0.2 µm
2.5. Overlap into Si Island	≥ 2 µm

C.3. Oxidation (Photo)

Window to oxidize wide fingers and monitor finger oxidation.

3.1. Width	≥ 6 µm
3.2. Spacing	≥ 4 µm
3.3. Extension out of Si Island	≥ 2 µm
3.4. Overlap into Si Island	≥ 2 µm

C.4. Oxidation (EBL)

Window over fine fingers to be thinned by oxidation.

4.1. Width	≥ 100 nm
4.2. Spacing	≥ 540 nm
4.3. Extension out of Si Island	≥ 2 µm
4.4. Overlap into Si Island	≥ 2 µm

C.5. As (Photo)

Large-area As implant.

5.1. Width	≥ 6 µm
5.2. Spacing	≥ 4 µm
5.3 Spacing to Island	≥ 2 µm
5.4 Spacing to Finger Spacing	≥ 2 µm
5.5 Spacing to Oxidation (EBL)	≥ 2 µm
5.6. Extension out of Si Island	≥ 2 µm
5.7. Overlap of Si Island	≥ 2 µm
5.8. Overlap of Oxidation	≥ 2 µm

C.6. As (EBL)

Small-area As implant.

6.1. Width		≥ 100 nm
6.2. Spacing	≥ worst case{2(range + 3straggle$_{lateral}$) + w_d}	≥ 330 nm
6.3. Overlap of Si Island		≥ 2 µm
6.4. Overlap of Finger Spacing		≥ 10 nm
6.5. Overlap of Oxidation (EBL)		≥ 10 nm
6.6. Overlap of As (Photo)		≥ 2 µm

C.7. Contact

Metal contact to Island.

7.1. Width	≥ 6 µm
7.2. Spacing	≥ 10 µm
7.3. Spacing to Finger Spacing	≥ 2 µm
7.4. Spacing to (any) Oxidation	≥ 2 µm
7.5. Surround by Si Island	≥ 2 µm

C.8. Metal

Metal interconnect.

8.1. Width	≥ 10 µm
8.2. Spacing	≥ 10 µm
8.3. Spacing to Finger Spacing	≥ 2 µm
8.4. Spacing to (any) Oxidation	≥ 2 µm
8.5. Surrounding Contact	≥ 2 µm

ADDENDUM D: PROCESS CHARACTERIZATION DATA

This addendum characterizes the used processing equipment by plotting and analyzing self-measured rate information.

D.1. Oxidation Rates

Figure D.3 plots the measured thermal oxidation rate observed for the Lindburg furnace at the GT MiRC.

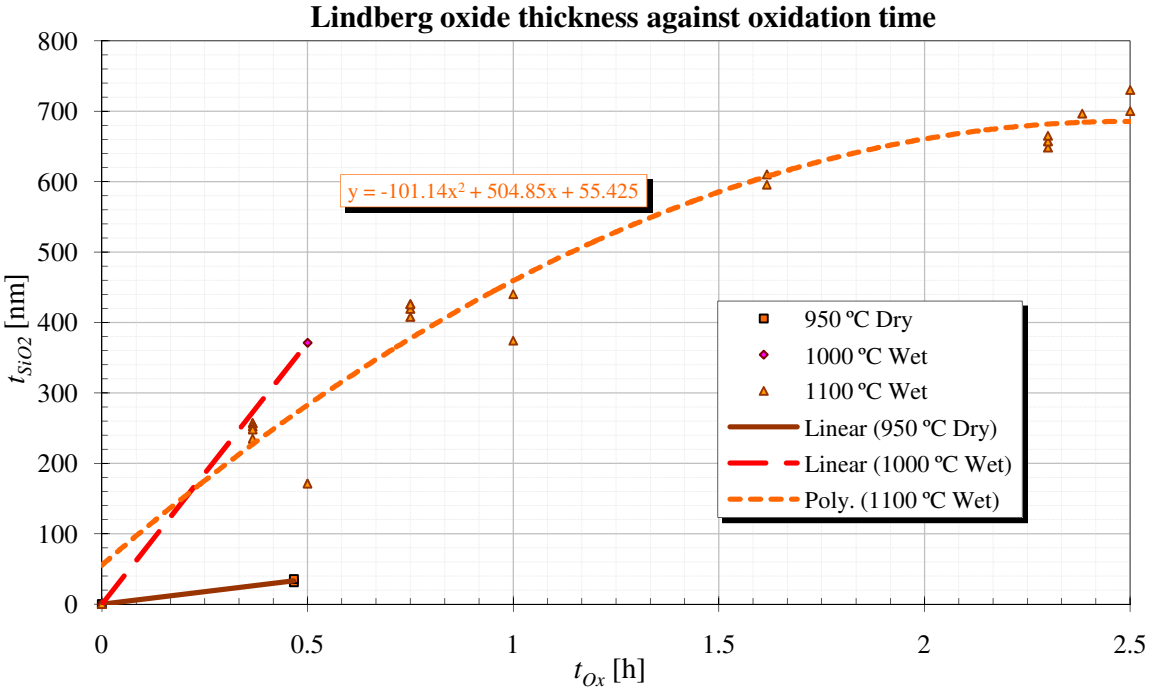

Figure D.3. Measured Lindburg furnace Si oxidation rates.

D.2. BOE Etch Rates

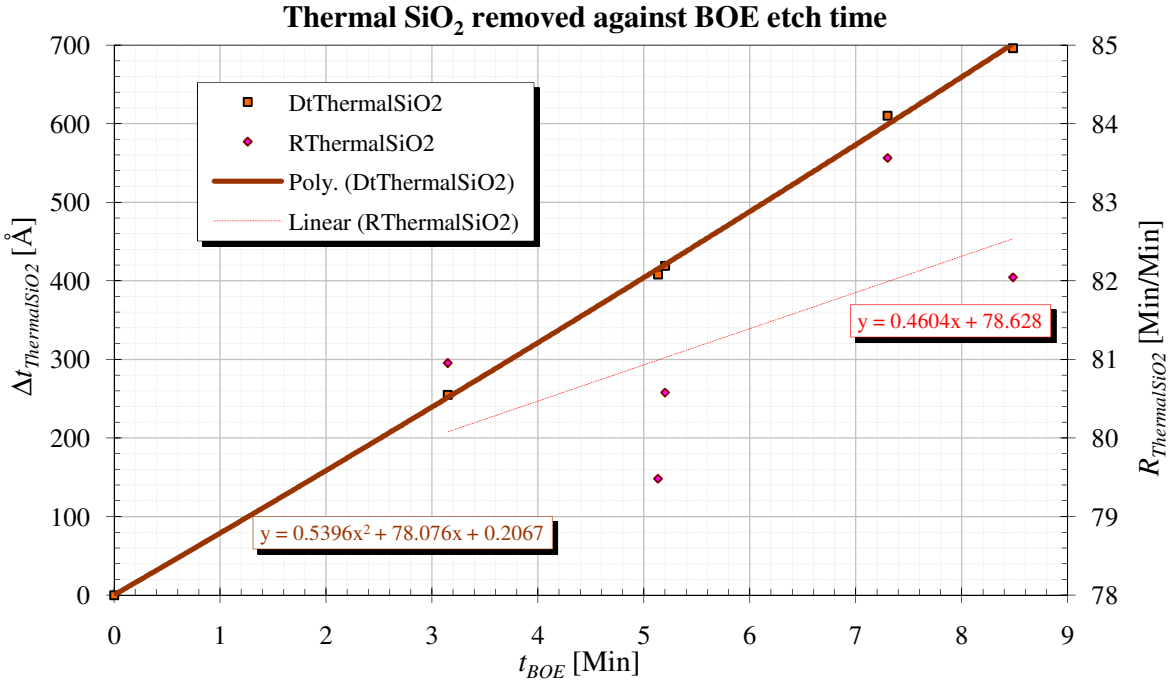

Figure D.4. Measured BOE etch rates of thermal SiO_2.

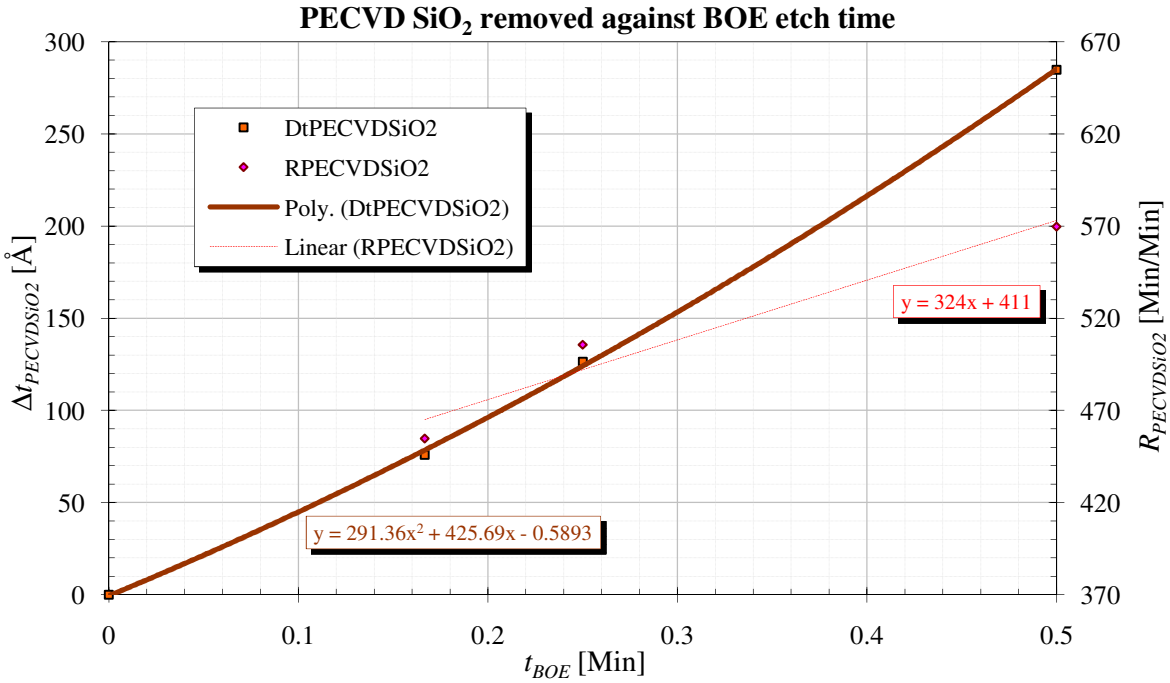

Figure D.5. Measured BOE etch rates of PECVD SiO_2.

D.3. Unaxis PECVD Deposition Rates

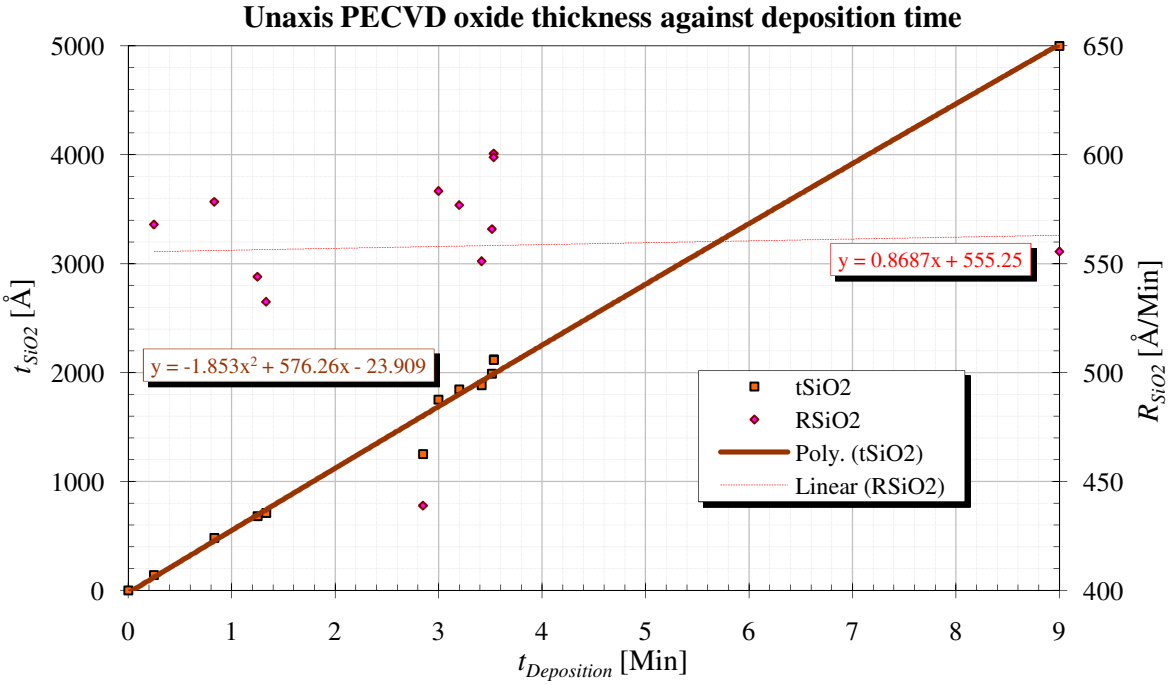

Figure D.6. Measured Unaxis PECVD SiO_2 deposition rates.

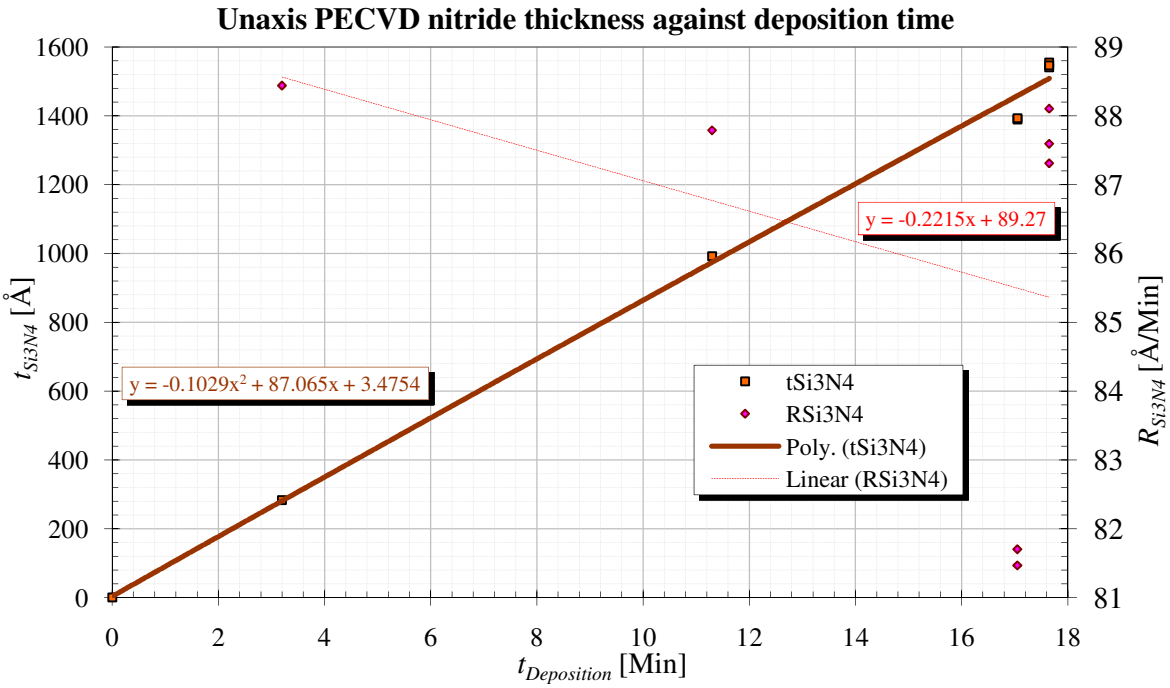

Figure D.7. Measured Unaxis PECVD Si_xN_y deposition rates.

D.4. Vision RIE Etch Rates

D.4.1. Summary

Table 8.2. Average Vision RIE etch rate summary.

Average Etch Rate [Å/Min]			Recipe		
			Si	Oxide	Nitride
Material	Si		2 297	127	
	SiO_2	PECVD	25	186	
		Thermal		129	80
	Si_xN_y		80	782	341
	SC1813		85	495	
	ZEP520A		114	252	

D.4.2. Silicon Recipe

D.4.2.1. Silicon

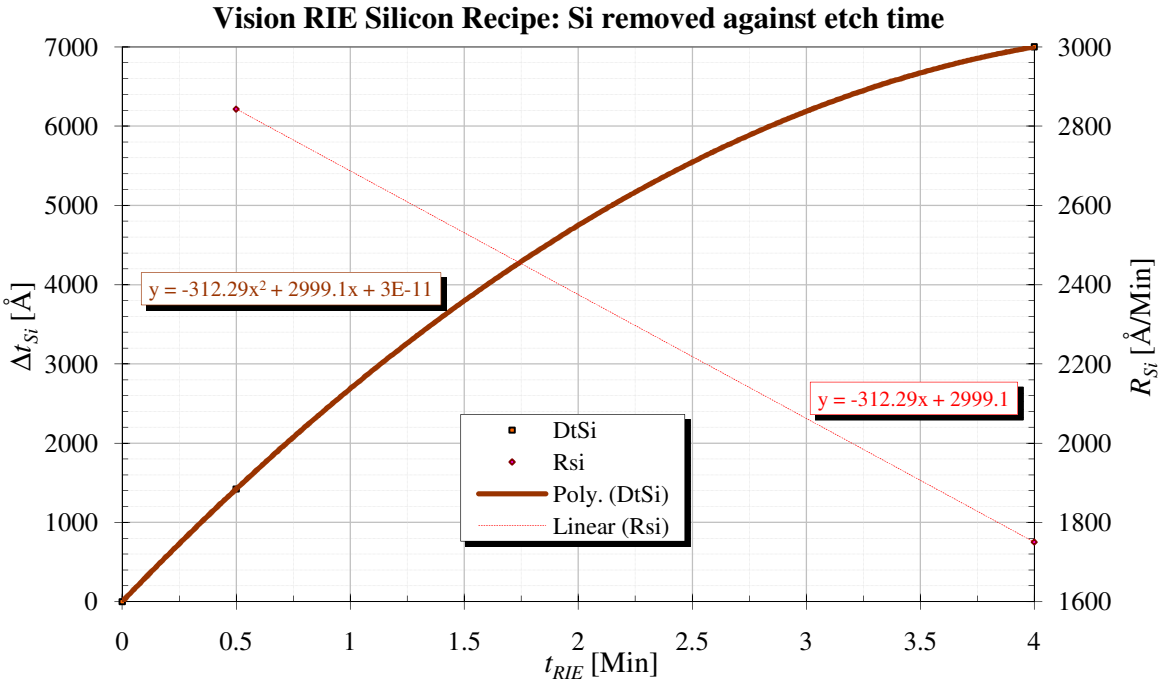

Figure D.8. Measured Si etch rate in Vision Oxide RIE Si recipe.

D.4.2.2. PECVD-SiO$_2$

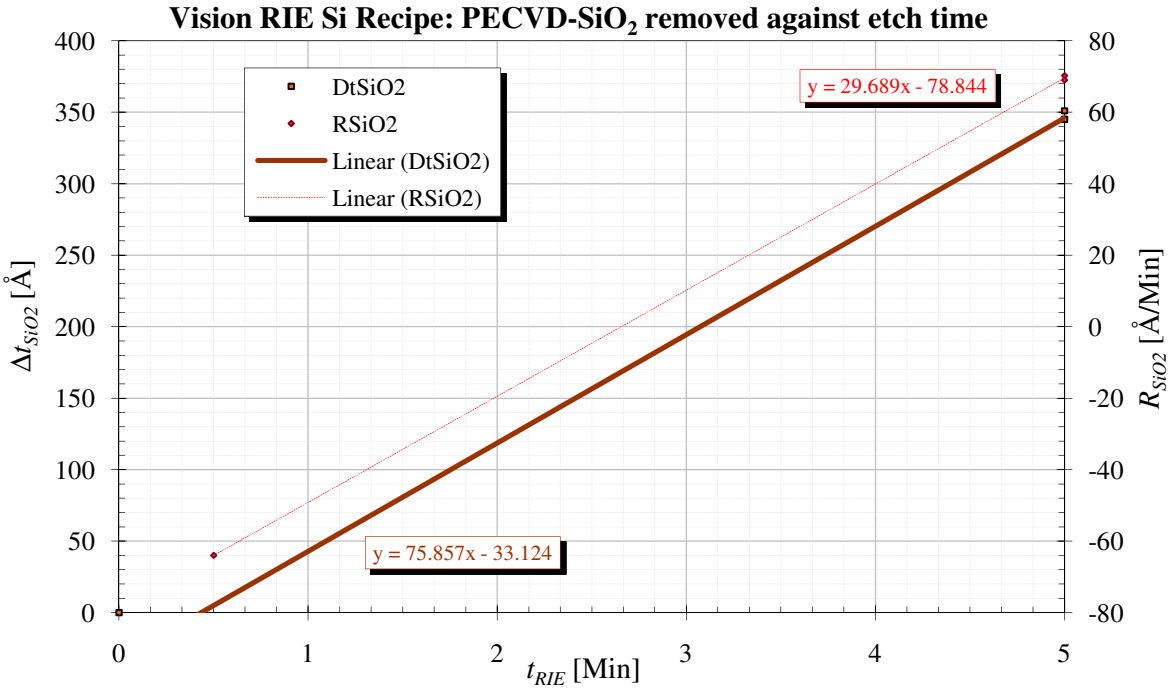

Figure D.9. Measured PECVD-SiO$_2$ etch rate in Vision Oxide RIE Si recipe.

D.4.2.3. Nitride

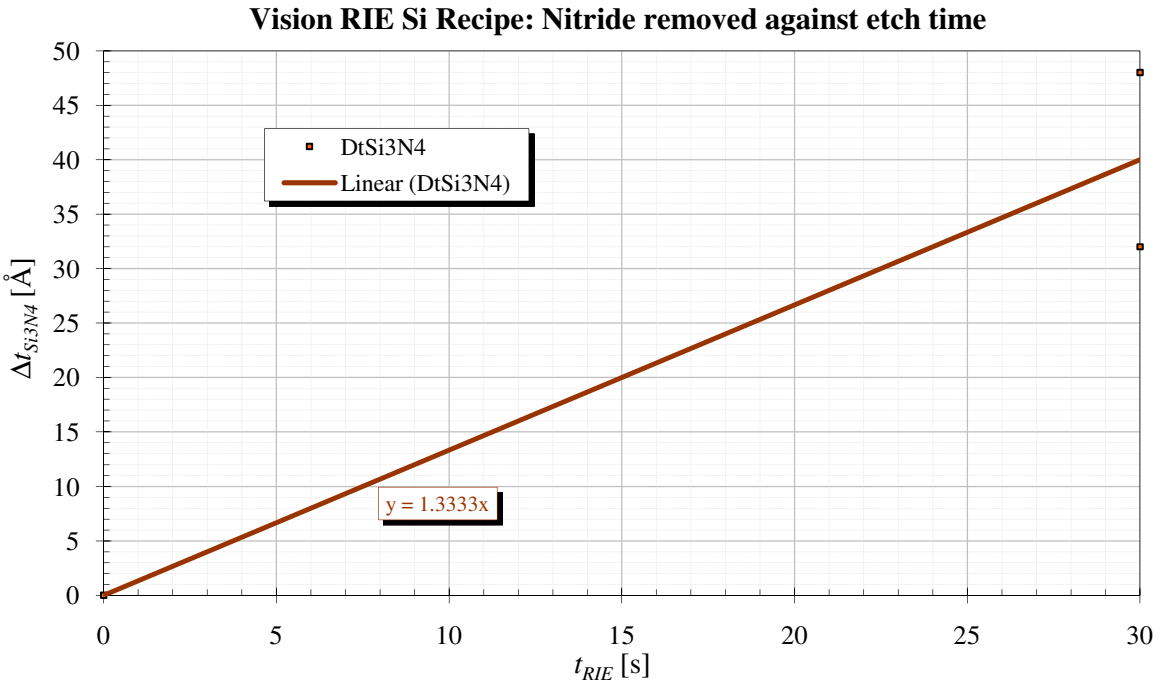

Figure D.10. Measured Si$_x$N$_y$ etch rate in Vision Oxide RIE Si recipe.

D.4.2.4. SC1813

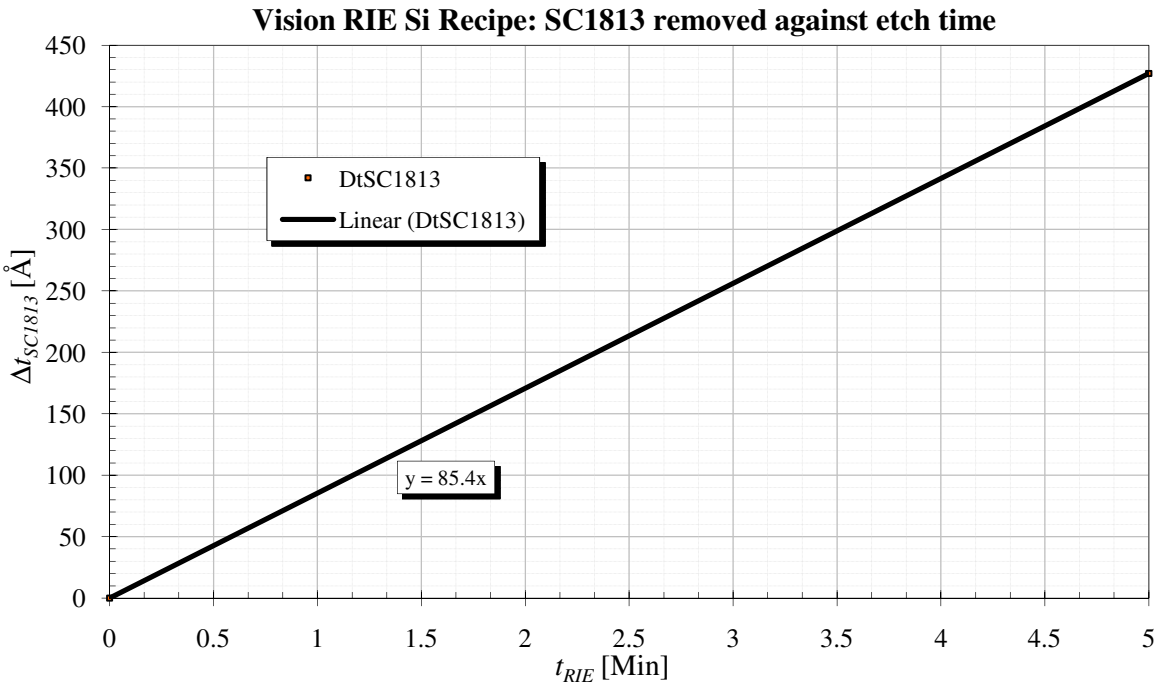

Figure D.11. Measured SC1813 etch rate in Vision Oxide RIE Si recipe.

D.4.2.5. ZEP520A

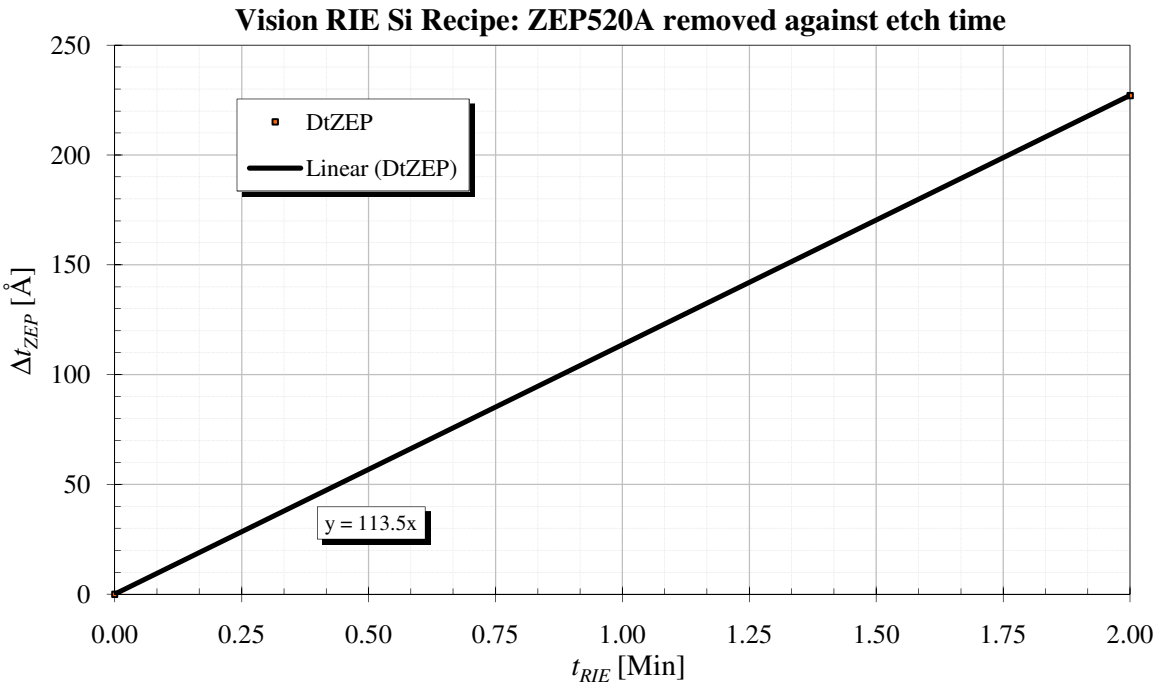

Figure D.12. Measured ZEP520A etch rate in Vision Oxide RIE Si recipe.

D.4.3. Standard Oxide Recipe

D.4.3.1. Silicon

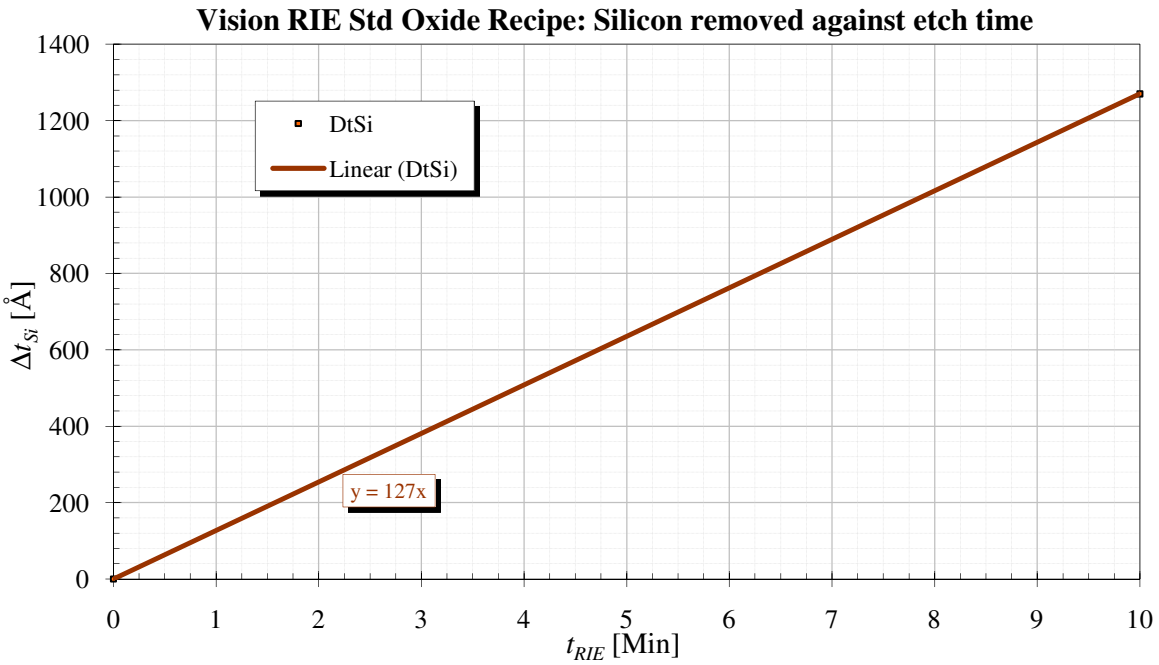

Figure D.13. Measured Si etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.2. PECVD-SiO_2

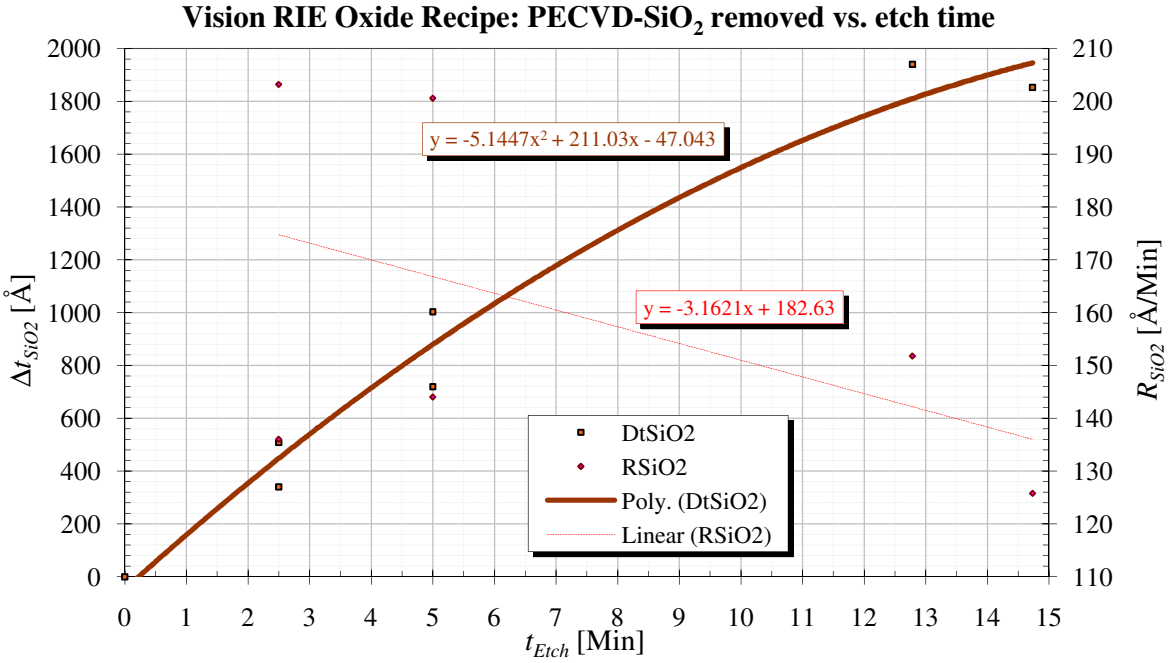

Figure D.14. Measured PECVD-SiO_2 etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.3. Thermal SiO_2

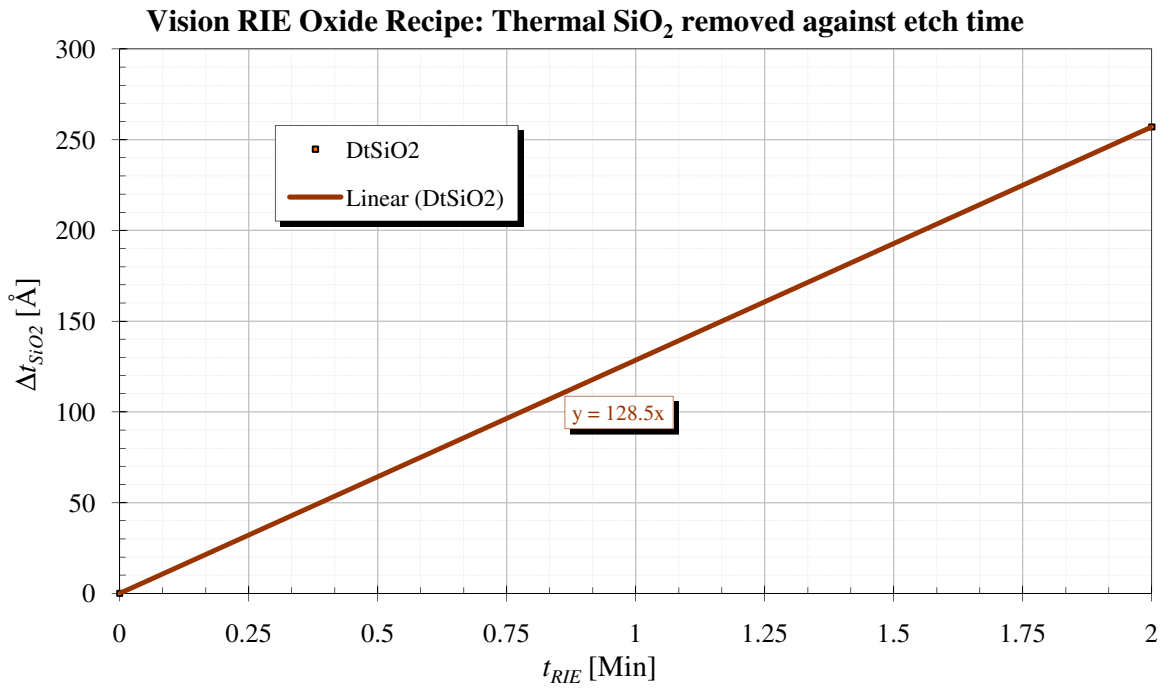

Figure D.15. Measured Thermal SiO_2 etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.4. Nitride

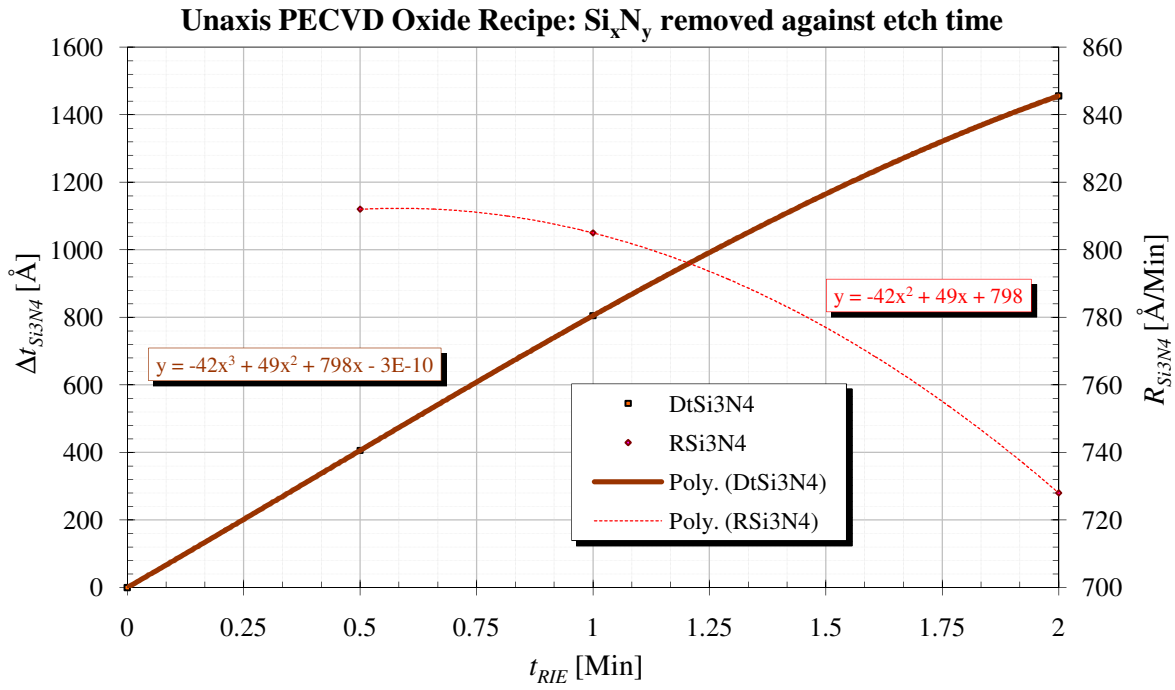

Figure D.16. Measured Si_xN_y etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.5. SC1813

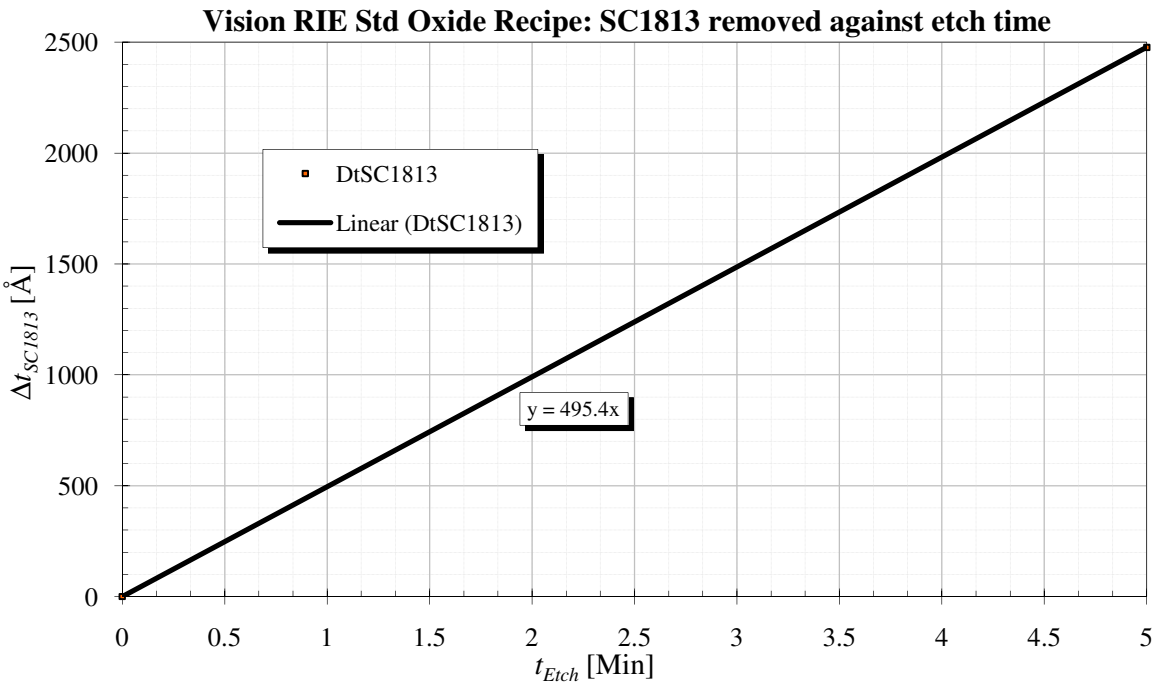

Figure D.17. Measured SC1813 etch rate in Vision Oxide RIE standard oxide recipe.

D.4.3.6. ZEP520A

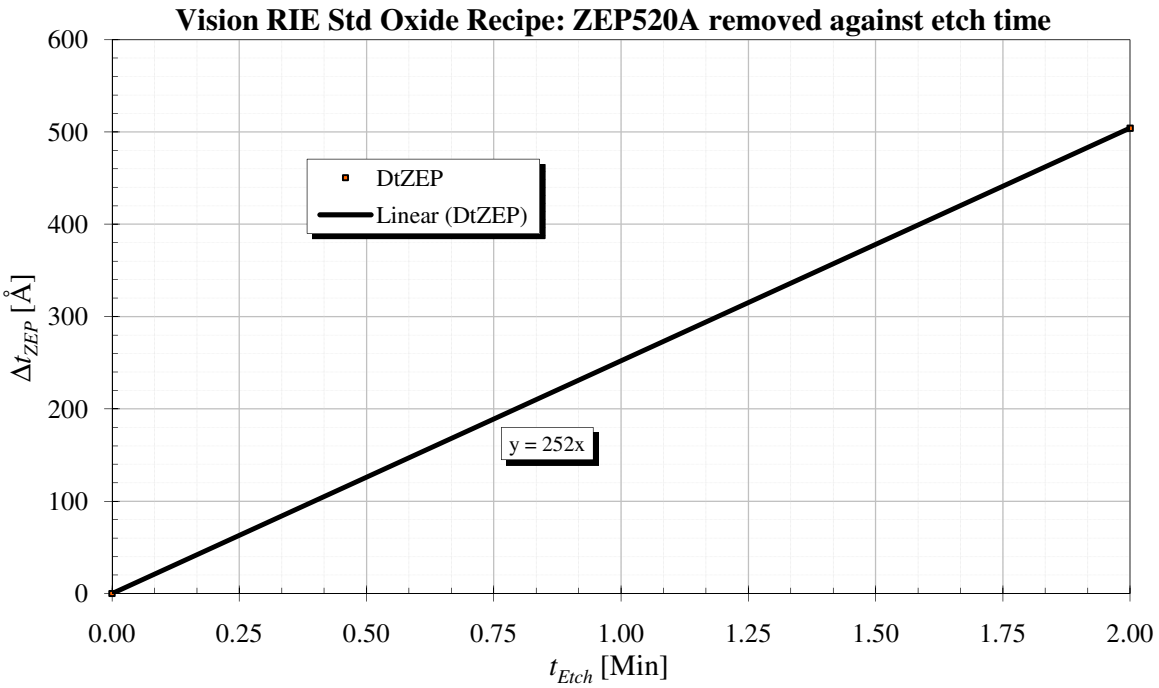

Figure D.18. Measured ZEP520A etch rate in Vision Oxide RIE standard oxide recipe.

D.4.4. Nitride Recipe

D.4.4.1. Thermal SiO_2

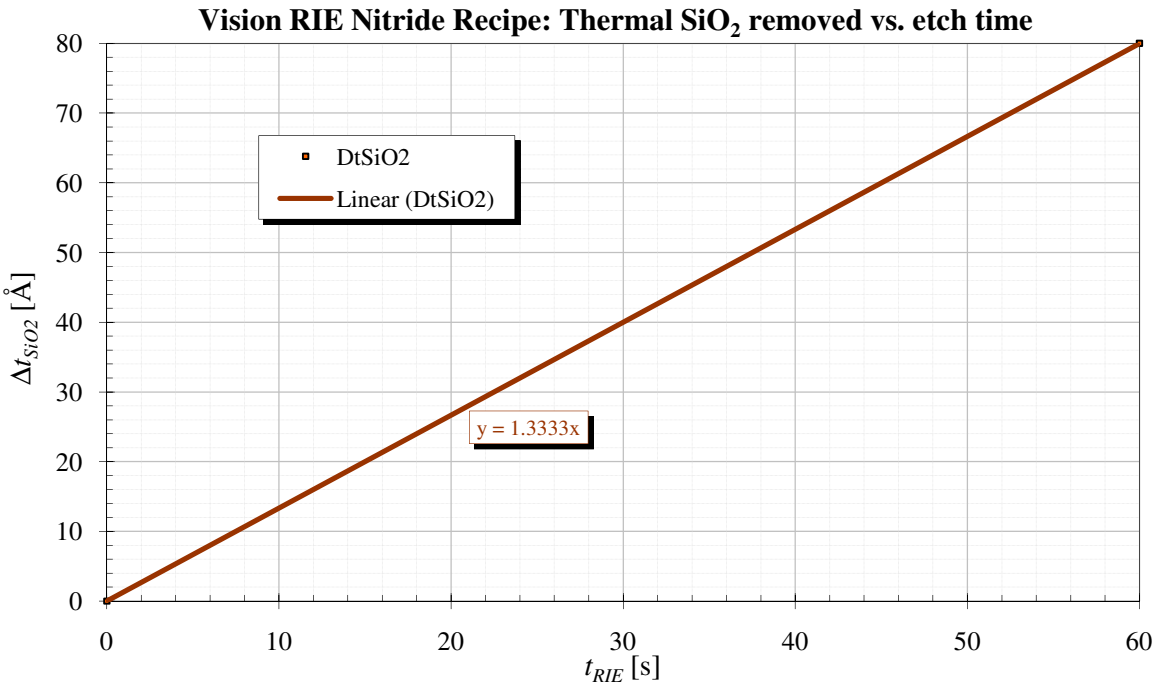

Figure D.19. Measured thermal SiO_2 etch rate in Vision Oxide RIE nitride recipe.

D.4.4.2. Si_xN_y

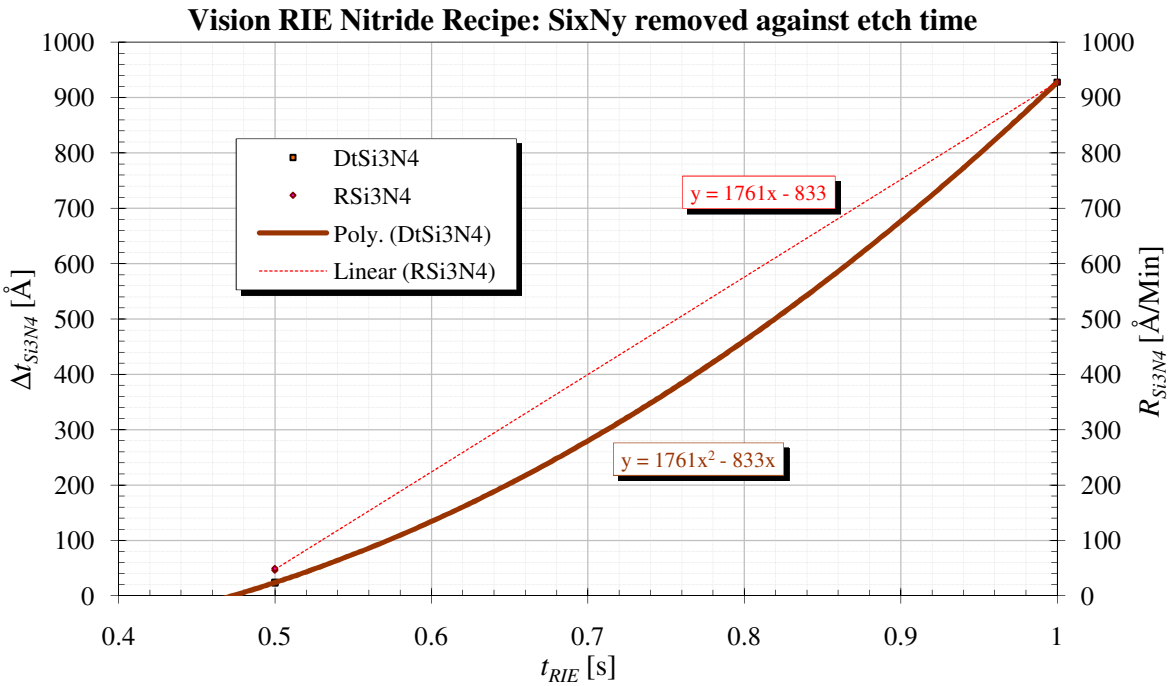

Figure D.20. Measured thermal Si_xN_y etch rate in Vision Oxide RIE nitride recipe.

ADDENDUM E: EBL WRITE TIMES

Table 8.3. EBL write time contributions per wafer.

Chip	Pattern					
	As	***Finger Spacing***	***Oxidation***	***As***	***Finger Spacing***	***Oxidation***
#	[µm^2]			[%] of Total		
1	118 437	279	22 665	13	0	2
2	60 772	284	3 484	7	0	0
3	227 898	25 285	50	25	3	0
4	429 400	25 274	61	47	3	0

	$A_{Cluster}$	836 507	51 122	26 260	[µm^2]
$n_{Clusters}$/wafer	4	3 346 029	204 489	105 038	
	A_{Wafer}	$3.3 \cdot 10^{-2}$	$2.0 \cdot 10^{-3}$	$1.1 \cdot 10^{-4}$	[cm^2]
	Dose	200			[µC/cm^2]
	I_{Beam}	2			[nA]
	t_{Write}	3 346	204	105	[s/wafer]
		56	3	2	[Min/wafer]
	t_{Align}	45			
	t_{Wafer}	101	48	47	
		1.7	0.8	0.8	[h/wafer]
n_{Wafer}	4	**7**	**3**	**3**	[h]
	t_{Total}	**13**			

Writing four wafers was estimated to take approximately 13 hours, but the final times were significantly longer since wafer and beam alignment and general set-up was found to be more time consuming than expected.