6. MEASUREMENTS

After completing the metallization, wafer inspection and electrical probing selected devices for optical characterization with a calibrated spectrometer (see Addendum B), which allowed comparing the optical power spectrum to regular *pn*-junction avalanche light sources manufactured in the AMS 0.35 µm CMOS process.

6.1. Electrical Probing and Device Selection

505 devices across 34 clusters on all four wafers were manually probed. It was found that only two wafers contained light-emitting devices: *S3* and *S5*. About half of all devices lost their fingers due to either over-oxidation or mechanical stress that seems to have pulled the fingers apart.

Furthermore, it was found that an oversight during the design phase caused the un-thinned devices to become resistors. Since the Si_xN_y masking layer protected these devices from oxidation, the anticipated B extraction and redistribution could not occur. The B therefore overshadowed the weaker As implant. An unexpected advantage of this oversight was that many oxidation-thinned process-monitoring resistors became p^+np^+ punch-through light sources.

It was also determined that the one micron thick Al experienced step coverage problems. This was caused by the fact that the BOX was etched deeper into than expected. In many places the BOX etch undercut the Si islands, which caused discontinuities in the Al metallization. This discontinuity was especially pronounced on the sides of the bonding pads, which meant that most pads could not be used for electrical connection. A simple remedy would have been to underlay all Al metallization with Si island tracks during the design phase, but this was not considered at that stage (but will be remembered for future designs). Although most functional devices could still be measured by positioning the probing needles on the Al tracks leading to the devices, this had the disadvantage that none of the chips could be packaged. This meant that the optical characterization also had to be done on wafer level.

After wafer inspection, electrical measurements and subjective evaluation by eye was used to select seven light-emitting devices located on cluster *EBL2* on wafer *S3* for optical characterization. The layout and estimated dimensions of these seven devices are indicated in Figure 6.1 and Table 6.1 respectively.

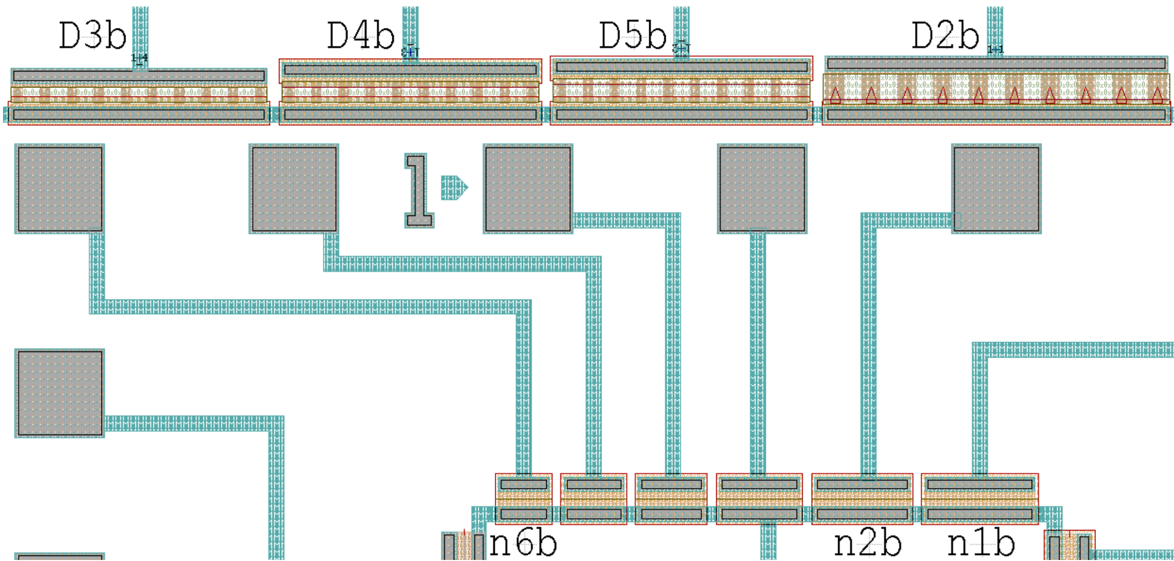

Figure 6.1. Devices in *Chip1* selected by electrical probing for comparative optical measurements.

Table 6.1. Estimated device and finger widths.

<table>
<tr><td>Dimension</td><td>w_{Device}</td><td>w_{Finger_Design}</td><td>Δ_{Finger}</td><td>w_{Finger_Final}</td></tr>
<tr><td>Device</td><td colspan="4">[μm]</td></tr>
<tr><td>D2b</td><td>228</td><td>12</td><td rowspan="4">0.1</td><td>11.9</td></tr>
<tr><td>D3b</td><td rowspan="3">168</td><td rowspan="3">6</td><td rowspan="3">5.9</td></tr>
<tr><td>D4b</td></tr>
<tr><td>D5b</td></tr>
<tr><td></td><td>[μm]</td><td colspan="3">[nm]</td></tr>
<tr><td>n1b</td><td>74</td><td>600</td><td rowspan="3">115</td><td>485</td></tr>
<tr><td>n2b</td><td>64</td><td>500</td><td>385</td></tr>
<tr><td>n6b</td><td>34</td><td>200</td><td>85</td></tr>
</table>

Although none of these devices have nanometre-scale finger widths, their average finger thickness is estimated to be around 17 nm. Since the devices between *n6b* and *n2b* were open circuit and, as shown later, *D4b* and *D5b* are thinner than *D3b* and *D2b*, it seems that the Si device layer thickness had a minimum around the horizontal centre of Figure 6.1. Since the exact thicknesses of selected devices can only be measured by cross-section and further testing of the devices is still planned, such destructive thickness measurements have not yet been performed.

Figure 6.2 depicts the electrical characteristic curves of the selected test light sources.

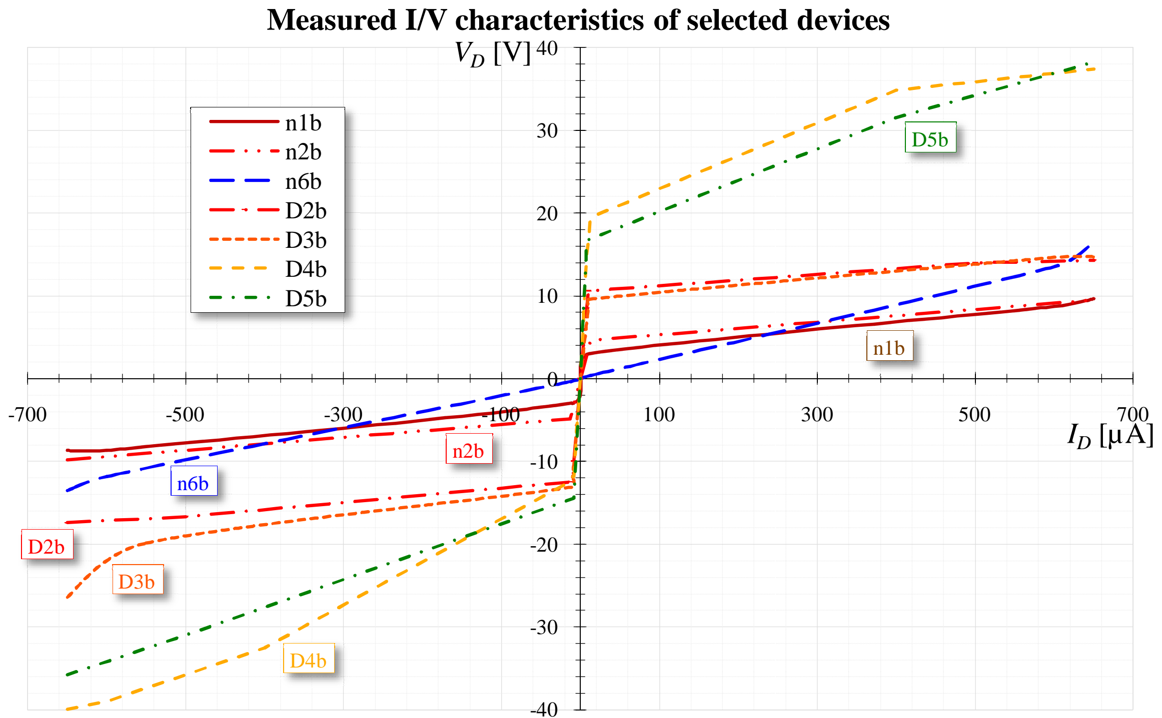

Figure 6.2. Measured current-voltage characteristic of selected punch-through SOI light source.

Although *n6b* emits light, its I-V curve shows that it has a resistance of about 20 kΩ in parallel. Since this resistance bypasses current through the device without contributing to the light generation, it is expected that *n6b* will have a low light emission efficiency. The voltage and resistance summary in Table 6.2 shows a higher breakdown voltage and higher series resistance for devices *D2b* to *D5b*.

Table 6.2. Voltages and resistance of selected devices at I_D = ±650 μA and ±11 μA.

Wafer	Location	Device	Reverse			Forward		
			$V_{D\text{-}11\mu A}$	$V_{D\text{-}650\mu A}$	$R_{\text{-}650\mu A}$	$V_{D11\mu A}$	$V_{D650\mu A}$	$R_{650\mu A}$
			[V]		[kΩ]	[V]		[kΩ]
S3	*EBL2*	*n1b*	-3.0	-8.7	3	3.0	9.7	3
		n2b	-4.9	-9.8	15	4.6	9.5	13
		n6b	-0.4	-11.8	19	0.4	16.5	39
		D2b	-12.5	-17.4	33	10.6	14.0	29
		D3b	-13.1	-26.4	54	9.6	14.7	39
		D4b	-12.1	-38.9	57	17.2	37.4	40
		D5b	-14.5	-35.7	74	16.7	38.3	77

Since a higher series resistance corresponds to a thinner Si device layer thickness and an increased breakdown voltage is characteristic of quantum-confinement, it is expected that especially *D4b* and *D5b* should have high light generation efficiencies.

Figure 6.3 shows a microphotograph of *D3b* emitting light at a bias of 650 µA.

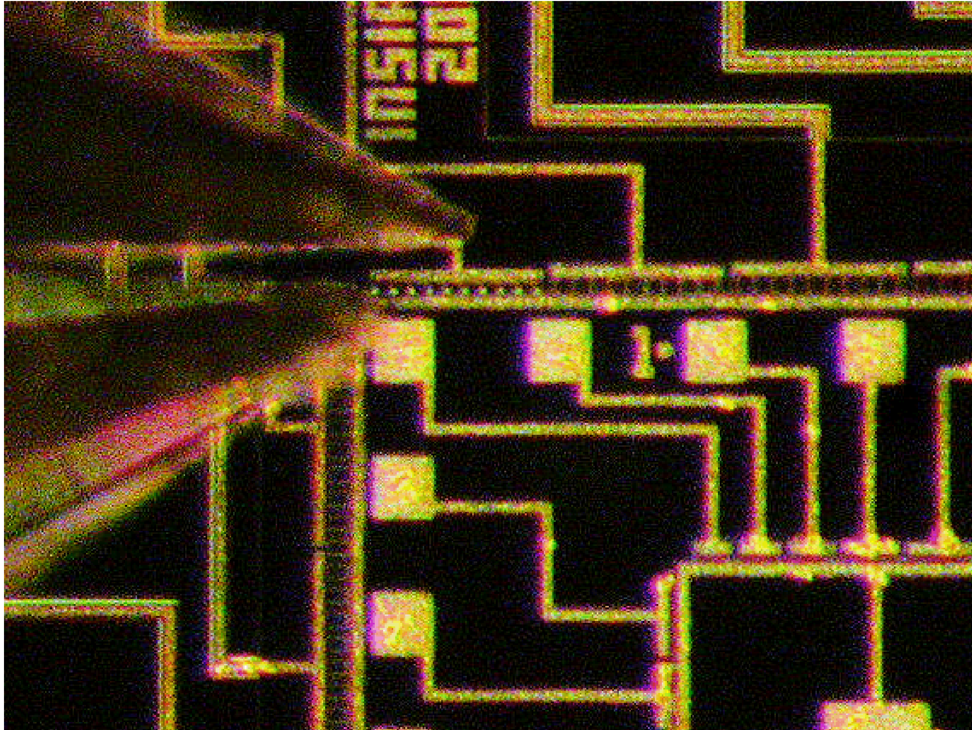

Figure 6.3. Electrical probing of test-device *D3b*.

Figure 6.4 shows the same view with the microscope light switched off.

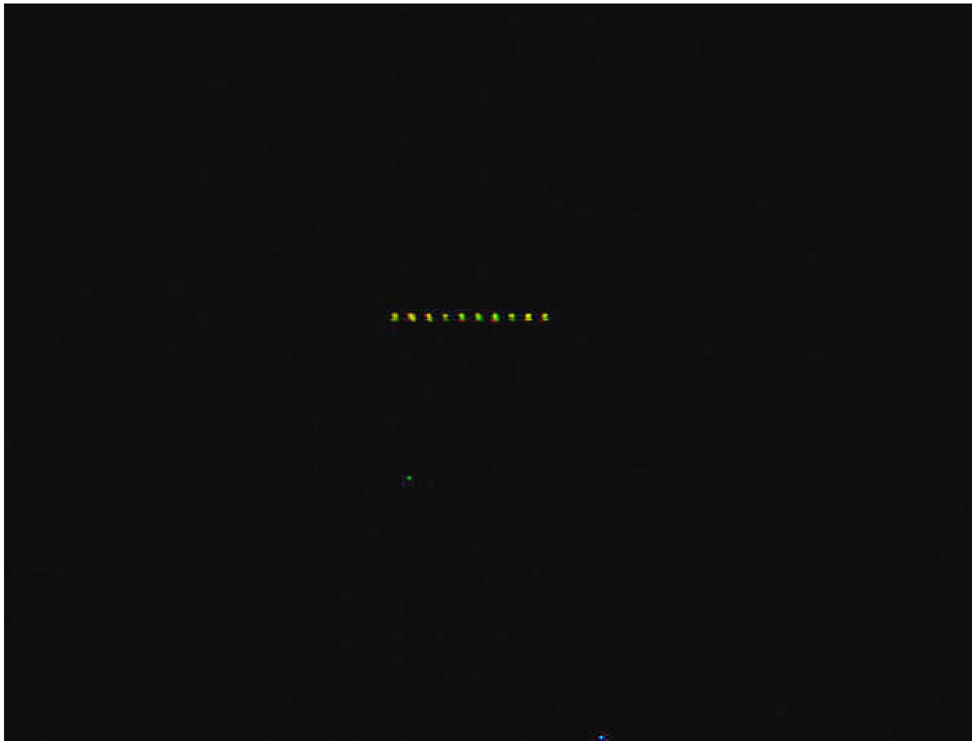

Figure 6.4. Light generation of the same *D3b* test-device.

The emitted light is homogenously spread across all punch-through fingers.

Figure 6.5 shows the light-emitting punch-through device *n2b* at $I_D = 650\ \mu A$.

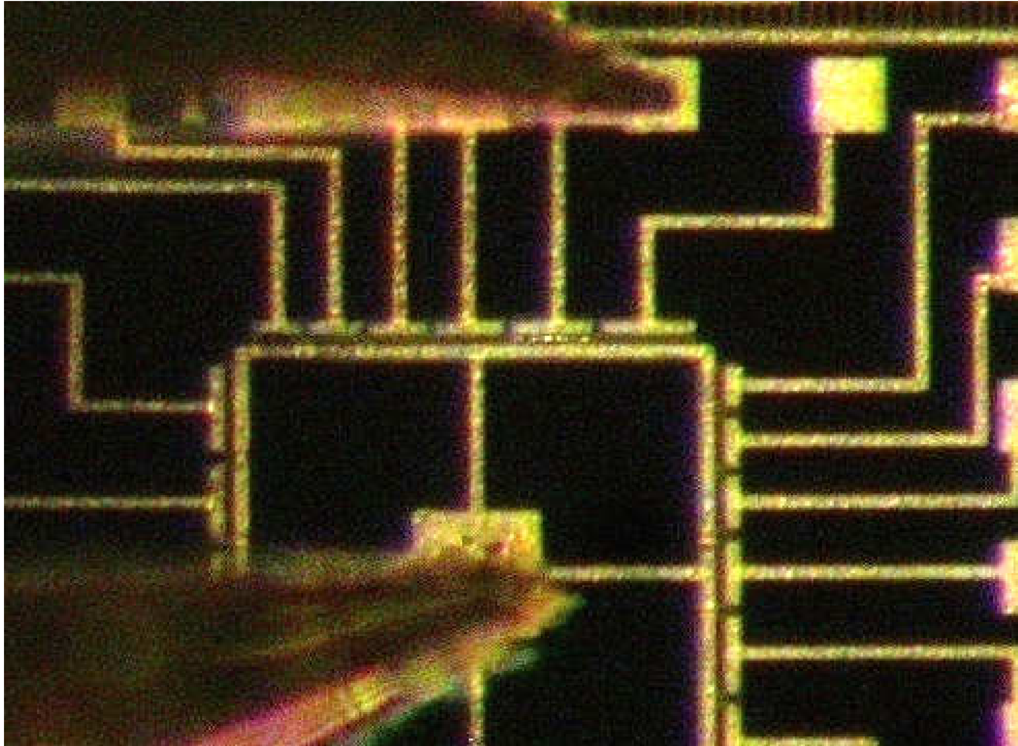

Figure 6.5. Probing of fingered punch-through device *n2b*.

Figure 6.6 shows the same view of *n2b*, but with the microscope light switched off.

Figure 6.6. Light generated by the fingered punch-through device *n2b*.

Above light emission is not homogenous and some fingers light up brighter than others do.

6.2. Optical Characterization

Since the mentioned Al metal step-coverage problem prohibits bonding and packaging of the manufactured SOI chips, the test light sources had to evaluated optically on the wafers. This was achieved by attaching a fibre-optic cable to one of the probing station manipulators. After successively stripping the fibre-optic cable of its shielding and protective sleeves, the 60-µm core of the cable was then aligned to point perpendicularly down on the wafer. As shown in Figure 6.7, this method allowed positioning the stripped core onto a specific SOI light source.

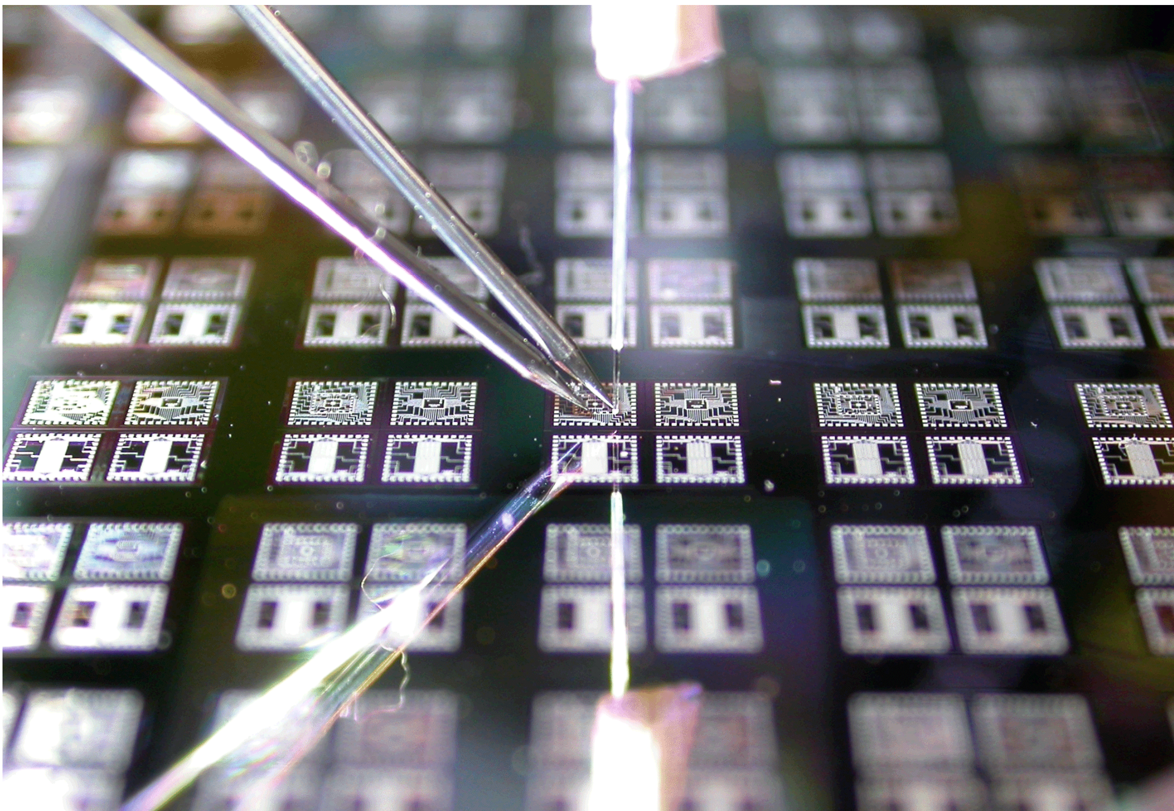

Figure 6.7. Spectroscopic probing of the SOI light-sources.

Since the emitted optical power was too low for a radiometer and photo-multiplier tube measurements only render a photon count without any spectral information, it was decided to connect the other end of the fibre-optic cable to a calibrated spectrometer (see Addendum B). Although the spectrometer could not measure accurate absolute optical power levels, the measured power spectra was used to compare the power spectra of the selected SOI test-devices to *pn*-junction avalanche light sources manufactured in the AMS 0.35 µm CMOS process.

Figure 6.8 compares the measured power spectra of test SOI light sources *D2b* to *D5b*. operating at I_D = 650 µA.

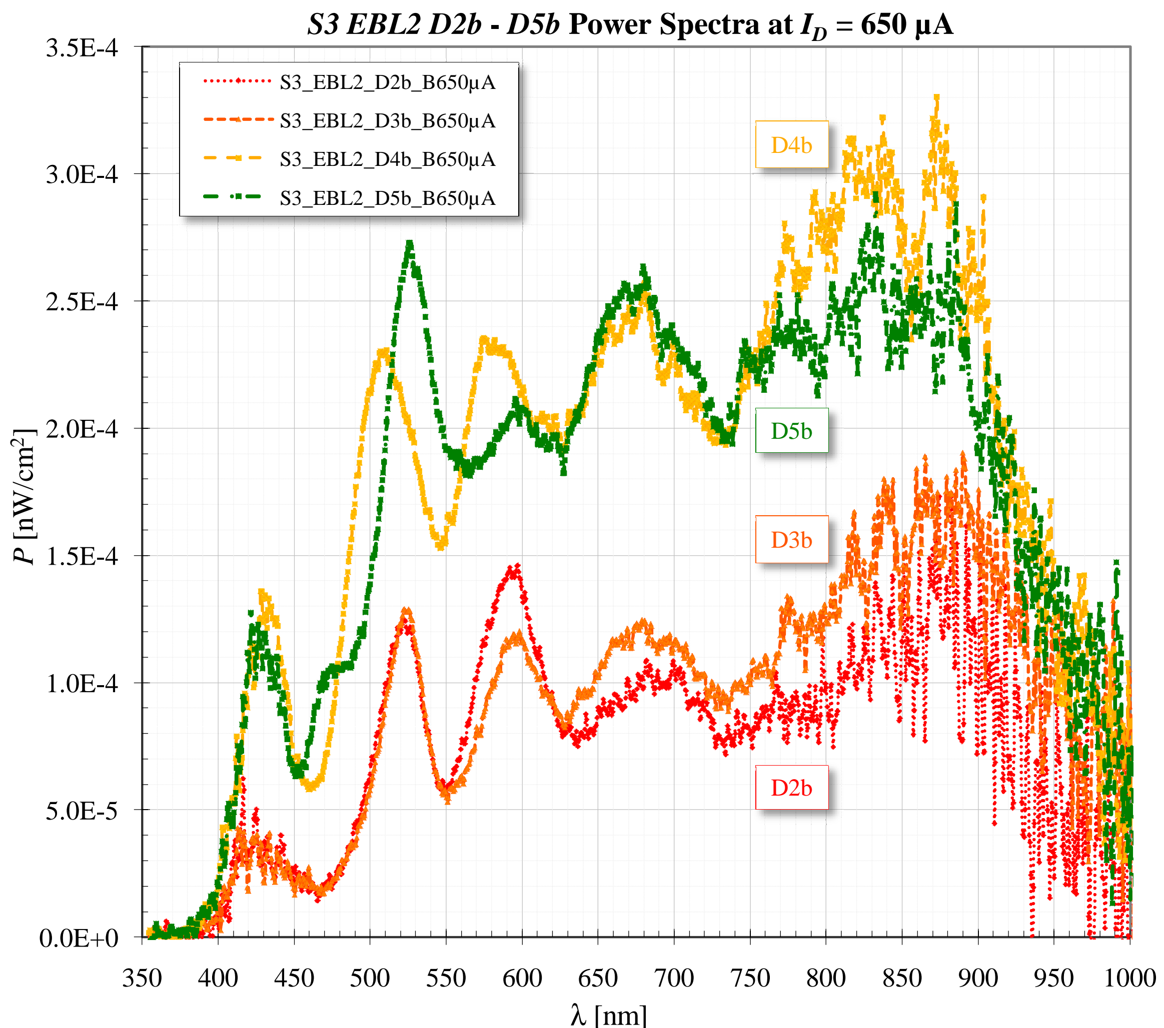

Figure 6.8. Measured power spectra of the *D2b – D5b* SOI light-sources.

In correlation to the observations made with respect to their current-voltage characteristics, *D4b* and *D5b* exhibit optical power outputs that are approximate 2.5 times higher than those measured on devices *D2b* and *D3b*. Their higher irradiance seems to confirm that *D4b* and *D5b* are already thin enough to experience quantum confinement effects that increase their optical power emission. The shifted peak of *D4b* in the UV spectrum (400 nm < λ < 600 nm) also seem to suggest that quantum confinement has shifted the band-gap structure of this device.

The large optical radiation power in the infrared (IR) spectrum range (750 nm < λ < 950 nm) though is unexpected.

Employing the same scaling as Figure 6.8, Figure 6.9 plots the measured optical power spectra of devices *n1b*, *n2b* and *n6b*.

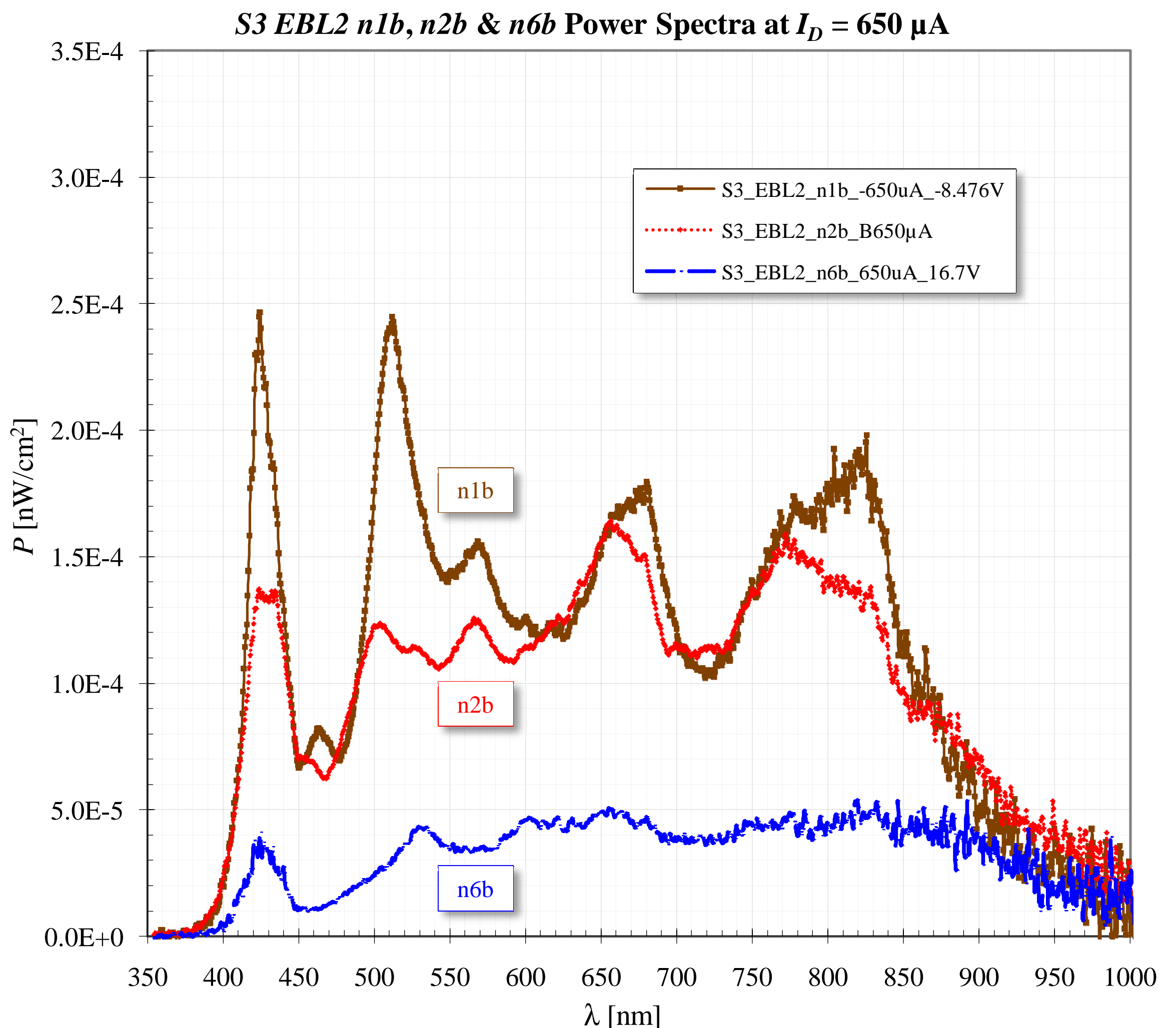

Figure 6.9. Measured power spectra of the *n1b, n2b* and *n6b* SOI light-sources.

The lower optical efficiency of *n6b* was already predicted from its current-voltage characteristic in Figure 6.2 that exhibited a parallel leakage resistance.

Since the optical power amplitudes of *n1b* and *n2b* are similar to those of *D2b* and *D3b* suggests that all these devices have about the same Si layer thickness, but in contrast to *D2b* and *D3b*, *n1b* and *n2b* exhibit less optical power in the infrared region.

The lack of UV peak shifting in above figure reinforces the suspicion that these devices are not yet thin enough to experience significant quantum confinement effects.

Figure 6.10 compares the "best" device from Figure 6.8 (*D4b*) to the "best" device from Figure 6.9 (*n1b*).

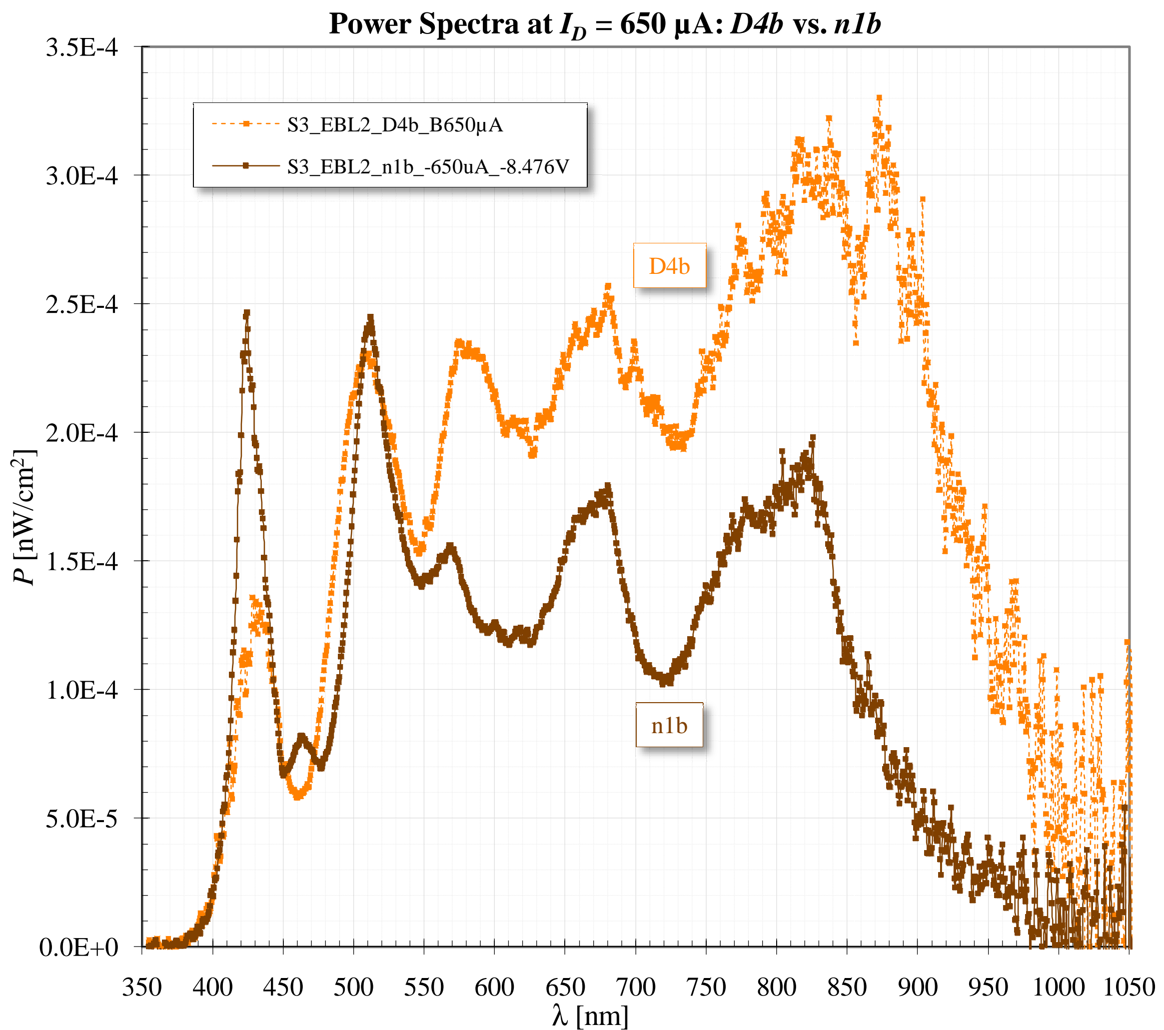

Figure 6.10. Measured power spectra comparison of the *n1b* and *D4b* SOI light-sources.

Both devices exhibit similar spectral peaks and have similar optical power in the UV side ($\lambda <$ 550 nm) of the spectrum.

D4b displays an optical power that increases with wavelength up to twice the optical radiation of *n1b* in the infrared.

Figure 6.11 compares the spectrum of the SOI punch-through light source with the highest optical power (*D4b*) to the average optical power of 25 avalanche CMOS *pn*-junction light sources also biased at $I_D = 650$ µA and measured with exactly the same characterization setup.

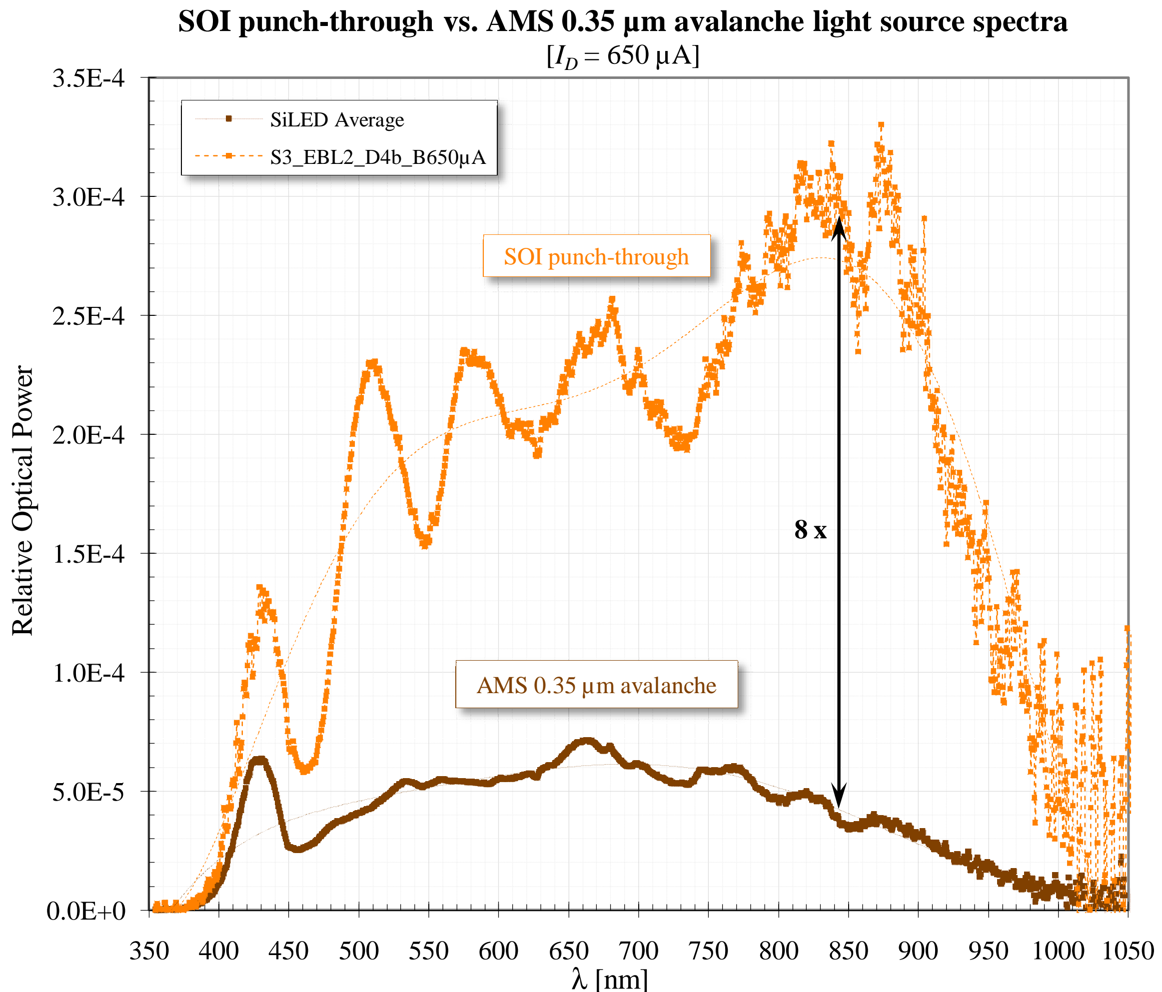

Figure 6.11. Spectra comparison of SOI punch-through and AMS 0.35 µm CMOS light-sources.

While the AMS 0.35 µm avalanche light source spectrum peaks around $\lambda \approx 660$ nm ($E_{Ph} \approx 1.88$ eV) the SOI punch-through light source peaks around $\lambda \approx 850$ nm ($E_{Ph} \approx 1.46$ eV).

It is evident that the SOI punch-through device radiates up to 8 times more optical power around 850 nm. Since significant IR radiation peaks have also been observed in Si nano-crystal EL and photoluminescence (PL) experiments ([92] and [57]), this could be indicative of quantum confinement.

Considering that photons at longer wavelengths have lower energies implies that more photons are required at longer wavelengths to achieve the same optical power as photons at lower wavelengths. It therefore seems that thickness-confined SOI light sources have significantly higher quantum conversion efficiencies than bulk-CMOS avalanche light sources.

IR spectral components were previously reported for forward-biased and avalanching junctions ([20], [27], [29], [56], [93] and [94]). The multi-mechanism Si avalanche photon-generation model [95] postulates that the optical radiation spectrum of an avalanching junction consists of three recombination paths: intra-band transitions (Bremsstrahlung), direct and indirect inter-band recombination. The relative strengths of these spectral contributions depend on electric field strength and ionization length of electrons and holes. While intermediate photon energies ($2\ \text{eV} < E_{Ph} < 2.3\ \text{eV}$) are attributed to indirect intra-band transitions, the low-energy photon emission ($E_{Ph} < 1.8\ \text{eV}$) is thought to originate from indirect inter-band (phonon-assisted) recombination of electrons and holes in high-field populations.

It therefore seems that the spectra of the AMS 0.35 μm avalanche light sources with their peak around 1.88 eV are caused by a combination of indirect intra- and inter-band recombination. The observed spectra of the SOI light sources peak at around 1.46 eV and are predominantly generated by indirect inter-band recombination of hot carriers.

Other possible reasons for the increased IR optical radiation could include the closer shifting of carrier distributions in the energy bands, the valance and conduction bands shifting closer to each other or the presence of defect- or impurity-assisted radiative recombination [96].

The periodic optical power variation of all measured SOI light sources is due to light reflection off the SiO_2 BOX covering the Si handle layer of the SOI wafer. Employing the mathematical stack transmission model of subsection 2.2.3.2, the reflection R (= 1 – T) of a Si-SiO_2-air stack can be simulated for varying SiO_2 thicknesses. Starting with the average measured BOX thickness t_{BOX} = 980 nm (Table 5.4) and decreasing t_{BOX} until the reflection peaks agree with the spectral peaks of the measured SOI light source power spectra revealed that the best fit was achieved for $t_{BOX} \approx$ 860 nm (see Figure 6.12).

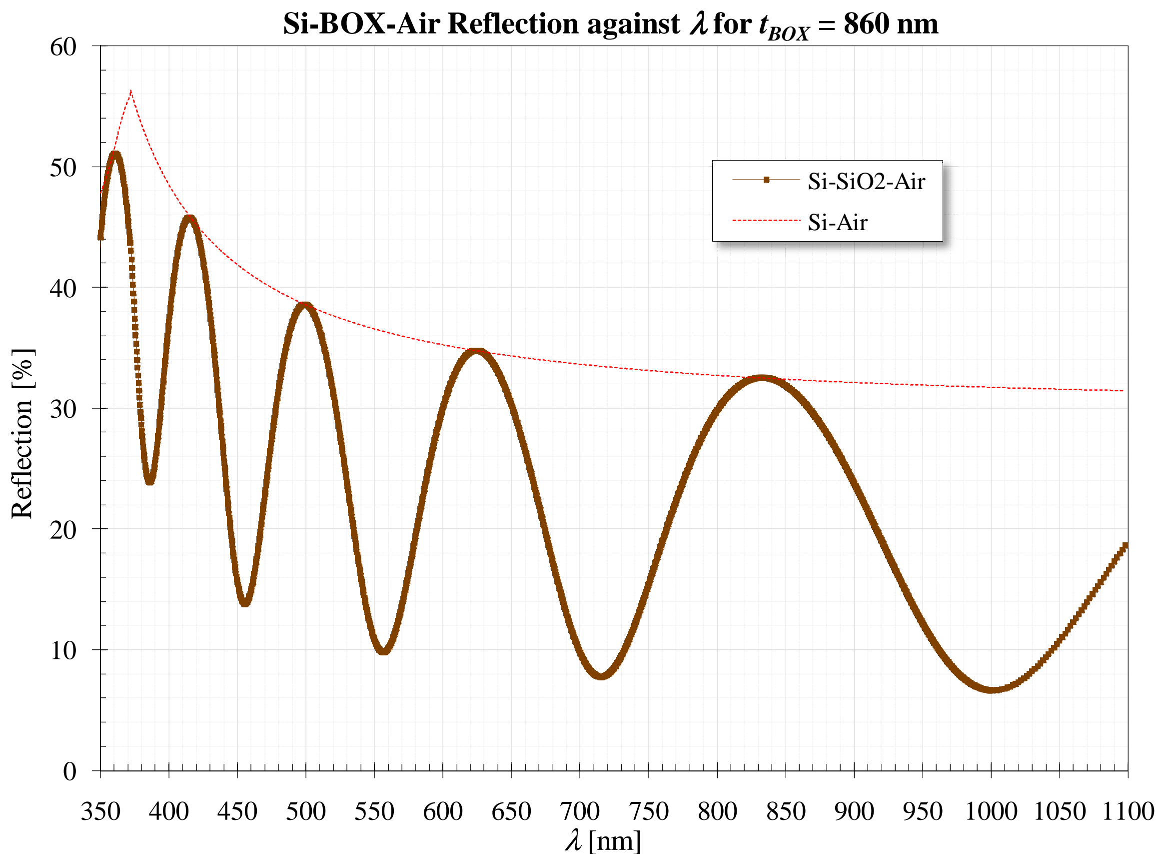

Figure 6.12. Simulated perpendicular BOX reflection for BOX thickness t_{BOX} = 860 nm.

Above plot shows that an average of 25 % of the light that would have been lost through downward radiation is reflected back up as useful light. Although this reflection and the efficiency improvement due to the finger shaping (see section 3.2) explain an increase in luminescence of the SOI light sources, they do not explain the increased infrared radiation measured as the average BOX reflection decreases with increasing wavelength.

Above also implies that about 120 nm of the BOX were etched away during processing. This was not considered during the design and explains the metal step coverage problem experienced.

7. CONCLUSION

This project was a first-iteration attempt at investigating quantum confinement in nanometre-scale SOI light sources as a method of increasing the quantum conversion and external power efficiency of Si light sources. For the author this was also the first exposure to clean-room self-processing and as far is known this was the first project in South Africa (and possibly at the MiRC) that employed EBL to define functional nanometre-scale semiconductor devices.

Although due to design and processing oversights only 29 out of 505 measured SOI light sources were useful light emitters, the design and manufacture of the SOI light sources was successful in the sense that enough SOI light sources were available to conduct useful optical characterization measurements. In spite of the fact that the functional light sources did not achieve the desired horizontal (width) confinement, measured optical spectra of certain devices indicate that vertical (thickness) confinement had been achieved.

All spectrometer-measured thickness-confined SOI light sources displayed a pronounced optical power for 600 nm < λ < 1 µm. The SOI light source with the highest optical power output emitted about 8 times more optical power around λ = 850 nm than a 0.35 µm bulk-CMOS avalanche light-source operating at the same current. Possible explanations for this effect were given. The expected dramatic increase in optical power in the UV spectrum region (λ < 600 nm) was not realized.

It was shown that the BOX layer in a SOI process could be used to reflect about 25 % of the light that would usually be lost to downward radiation back up, thereby increasing the external power efficiency of SOI light sources. Since it is estimated that the external power efficiency improvement factor due to the finger shaping and SOI box-handle interface reflection is about two, this leaves an improvement factor due to 17 nm thickness-confinement of about four, which agrees with results in Figure 1.2 previously reported at the University of Twente.

Since this first iteration attempt at quantum-confined light sources showed promising results, a following development phase is planned in which experience gained from this work is incorporated in creating even thinner 2D-confined SOI light sources.