4. DESIGN

To achieve the previously stated objective of creating Si wire junctions with diameters less than 50 nm, the SOI test-devices could not be manufactured in a standard process with supplied design rules. Instead, the layout and process design had to consider various equipment limitations and characteristics as well as physical effects occurring during the self-processing.

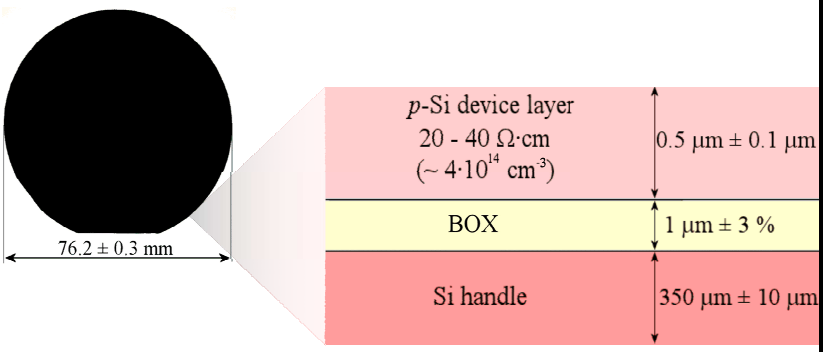
4.1. Starting Material

Before any design can commence the properties of the starting material need to be taken into consideration.

Table 4.1 shows the specifications of the SOI starting material wafers as supplied by Siegert Consulting e.K.[2].

Table 4.1. Siegert SOI Starting Material Specifications.

Parameter	Value	Graphical Representation
Type	Epitaxial Transfer SOI	
D_{Wafer}	76.2 ± 0.3 mm	
Doping	*p* (B)	
$t_{Device\ Layer}$	0.5 ± 0.1 µm	
$\rho_{Device\ Layer}$	20 - 40 Ω·cm ($\sim 4 \cdot 10^{14}$ cm^{-2})	
t_{Box}	1 µm ± 3 %	
ρ_{Handle}	0.01 – 0.02 Ω·cm	
t_{Handle}	350 µm ± 10 µm	
Edge exclusion	< 3 mm	



The 500 nm thick SOI active device layer above the BOX is the region where the light sources were implemented after its thickness was reduced to about 150 nm through thermal oxidation.

The 100 nm tolerance in SOI active device layer thickness might seem excessive, but is useful since a large variation in SOI light source thicknesses can be achieved with relative ease.

[2] Siegert Consulting e.K., TZA-Technologiezentrum Aachen, Dennewartstr. 25-27, Raum A 1.14, D-52068 Aachen, Germany.

4.2. Lithographic Patterning

As indicated in Table 4.2, the small geometries and precise pattern alignment of the current work required electron-beam lithography (EBL), but the single beam exposure scan of EBL is too slow to write all features across complete wafers.

Table 4.2. Photolithography and EBL Comparison.

Aspect	**Photolithography**	**EBL**
Wavelength/spot-size	≈ 300 nm	≈ 2 nm
Minimum feature size	≈ 0.5 µm	≈ 6 nm
Alignment accuracy	> 1 µm	> 6 nm
Exposure speed per wafer	Whole wafer at once Fast: Minutes	Serial scanning beam Very slow: hours

While photolithographic patterning is possible at the CEFIM, the Microelectronic Research Centre (MiRC) of the Georgia Institute of Technology was visited to make use of their JEOL JBX-9300FS EPG.

4.3. Mask Definitions

For the reasons in previous subsection, as Table 4.3 shows, different processing steps and geometry areas of the wafer selectively employed photolithography or EBL.

Table 4.3 Photolithographic and EBL Mask Detail.

Processing	**Document**	**GDS**	**Layout**	**Mask**			**Alignment**	
Step	**Section**	**No.**	**Rendering**	Name	Type	Polarity	Marker	Align to
3d	5.3	1		Si Island	Photo	Positive	-	-
4d	5.4	2		Arsenic (EBL)	EBL	Positive Tone	*AlignmentMarkerEBL*	Si Island
4j	5.4	3		Arsenic (Photo)	Photo	Negative	*AlignmentMarkerPhotoNoOx*	Si Island
5b	5.5	4		Finger Spacing	EBL	Positive Tone	*AlignmentMarkerEBL*	Si Island
6b	5.6	5		Oxidation (EBL)	EBL	Positive Tone	*AlignmentMarkerEBL*	Si Island
6c	5.6	6		Oxidation (Photo)	Photo	Negative	*AlignmentMarkerOx*	Si Island
7a	5.7	7		Contact	Photo	Negative	*AlignmentMarkerPhotoNoOx*	Si Island
7e	5.7	8		Metal	Photo	Positive	*AlignmentMarkerPhotoNoOx*	Contact
8	-	9		Si Isolation Spacing	Photo	Negative	*AlignmentMarkerPhotoNoOx*	Si Island

Six photolithographic plates and three EBL file masks were required. The photolithographic *Si Island* mask defines where Si islands remain on the BOX after reactive ion etching (RIE) removes the superfluous Si. The thin Si fingers are created by using the fine *Finger Spacing* EBL mask to RIE slits into the Si islands. The *Oxidation* mask was then used to selectively oxidize the Si between the slits into thin SOI fingers.

4.4. Design Rules

To facilitate the successful manufacture of the SOI light sources, self-made design rules had to be set-up. These design rules had considered possible mask alignment errors, limitations of the processing equipment and physical phenomena occurring during the wafer manufacturing process. These self-setup design rules are listed in Addendum C.

4.5. SOI Light Sources

Two types of SOI light sources were designed and manufactured:
2D-confined light sources are thin in two dimensions, thickness and width.
1D-confined light sources are only thin in one dimension, the thickness.

Both light source types were implemented for comparative purposes to investigate the possible increase in Si electroluminescence power efficiency improvement of 2D-confined device over 1D-confined Si light sources.

4.5.1. 2D-confined SOI Light Sources

Three types of 2D-confined SOI light sources were implemented:

1) n^+p finger junction avalanche light sources,
2) n^+pn^+ punch-through light sources and
3) Injection-enhanced light sources.

The design of these three types of 2D-confined Si light sources is described in the remainder of this sub-section.

4.5.1.1. n^+p Finger Junction Avalanche Light Sources

Figure 4.1 shows the pre-oxidized avalanche SOI finger light source layout.

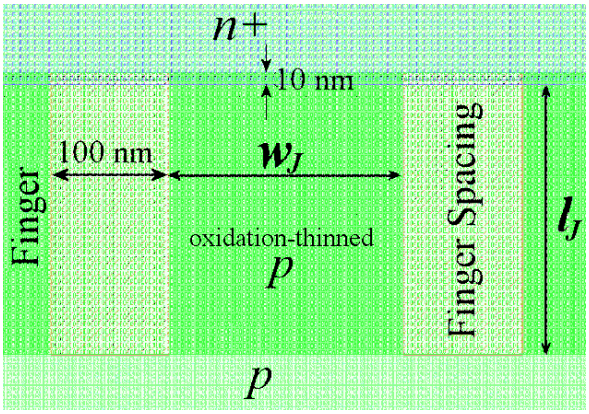


Figure 4.1. Avalanche finger layout dimensions.

The Si island regions above and below the fingers remained thick while an EBL-written oxidation mask opening across the fingers allowed the selective thinning through oxidation of the SOI finger junctions.

The dimensioning of the devices shown in Figure 4.1 had to comply with the following specifications to ensure proper functionality of the devices:

$$l_J \geq w_d + d_{Ox} + 3\Delta R_{\perp As} \approx 226 \text{ nm and} \quad (4.1)$$

$$w_J \approx 2t_{Si}, \quad (4.2)$$

where w_d is the reverse bias depletion region width at breakdown (see section 2.1.8), d_{Ox} is the worst-case As diffusion distance during all thermal oxidation steps after As implantation, $\Delta R_{\perp As}$ is the transverse As implantation straggle (Figure 5.4) and the initial Si thickness before oxidation was assumed to be 100 nm $\leq t_{Si} \leq$ 150 nm.

Relation (4.1) ensured that the fingers were long enough to accommodate the complete depletion region width after the implanted As (with its horizontal implant straggle) has diffused into the fingers after oxidation.

Equation (4.2) aimed to create semi-circular round fingers by assuming isotropic finger shaping oxidation that would thin the Si fingers equally from all sides.

Figure 4.2 depicts a 30 µm x 34 µm n^+p junction device with 100 parallel finger junctions.

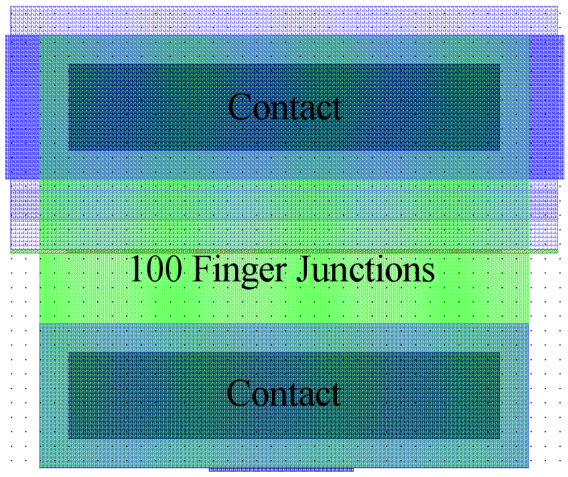


Figure 4.2. Finger junction device layout on a 1-µm grid.

Table 4.4 shows the dimensions of implemented n^+p avalanche SOI light sources.

Table 4.4. Implemented n^+p avalanche finger junctions.

Chip	**Group**	**Device**	**Pin**	**Type**	**Oxidized?**	w_J	l_J
#	*Name*		#			[nm]	
1	*FingerJunctions_Ox*	*100FingerJunctions200nm*	18	n^+p *Avalanche*	Oxidized	200	230
		100FingerJunctions220nm	17			220	
		100FingerJunctions240nm	16			240	
		100FingerJunctions260nm	15			260	
		100FingerJunctions280nm	14			280	
		100FingerJunctions300nm	13			300	
	FingerJunctions_NoOx	*100FingerJunctions200nm_NoOx*	24		Not oxidized	200	
		100FingerJunctions220nm_NoOx	23			220	
		100FingerJunctions240nm_NoOx	22			240	
		100FingerJunctions260nm_NoOx	21			260	
		100FingerJunctions280nm_NoOx	20			280	
		100FingerJunctions300nm_NoOx	19			300	

The common n^+ terminal to all above devices is connected to pad 5.

Figure 4.3 shows the 2D-confined finger junction avalanche SOI device layouts in *Chip1* (Figure 4.24) and the location of light source S with the narrowest pre-oxidized finger width (w_J = 200 nm).

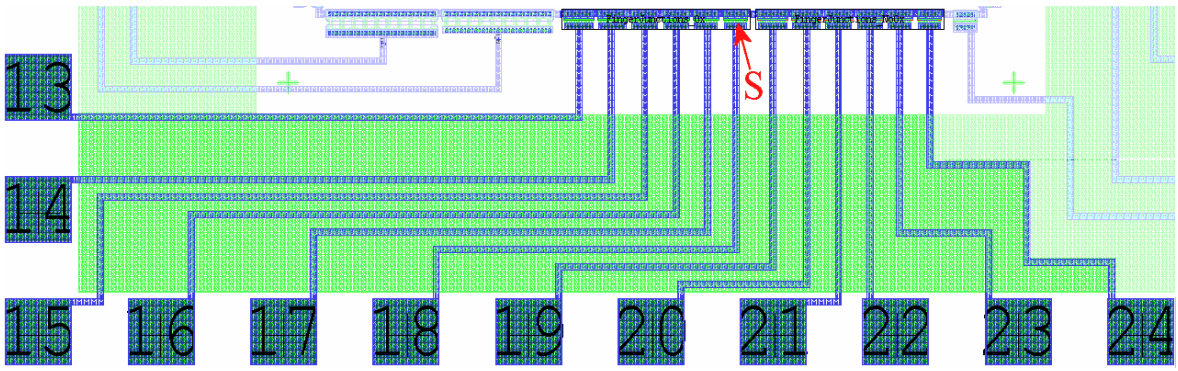


Figure 4.3. Finger junction devices layout.

4.5.1.2. n^+pn^+ Punch-through Light Sources

Figure 4.4 shows the designed layout dimension definitions of the punch-through SOI light source fingers.

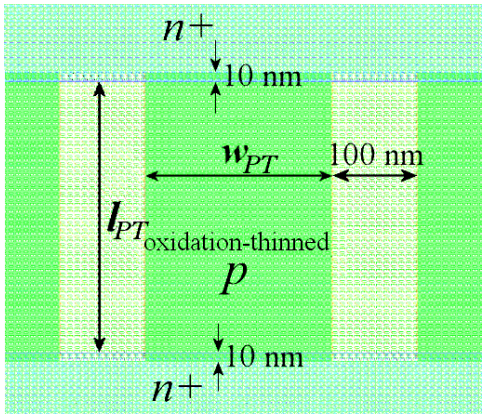


Figure 4.4. n^+pn^+ punch-through finger layout dimension definitions.

Similar to the avalanche breakdown devices the dimensioning of the devices shown in Figure 4.4 had to comply with the following specifications to ensure proper functionality of the devices:

$$l_{PT} \approx w_d + 2\left(d_{Ox} + 3\Delta R_{\perp As}\right) \approx 352 \text{ nm and} \tag{4.3}$$

$$w_{PT} \approx 2t_{Si}. \tag{4.4}$$

Figure 4.5 shows how 100 punch-through fingers shown in Figure 4.4 are placed in parallel between thicker and larger Si islands that allow electrical biasing through the interconnect metallization.

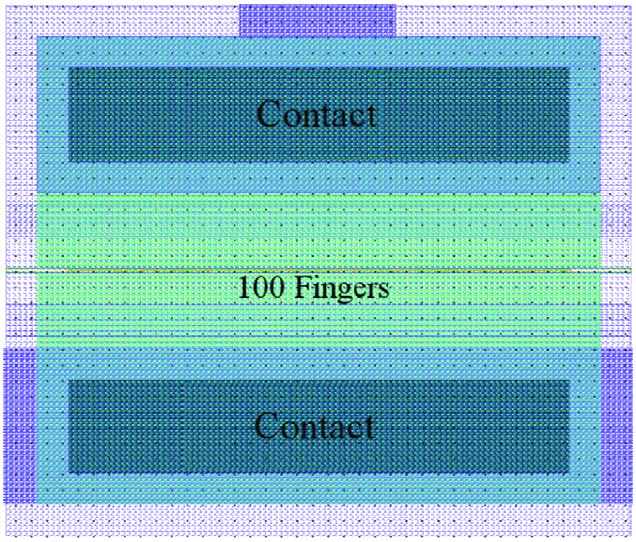


Figure 4.5. Device layout incorporating 100 parallel n^+pn punch-through fingers of Figure 4.4.

Table 4.5 and Table 4.6 show the implemented n^+pn^+ punch-through device dimensions.

Table 4.5. Oxidation-thinned punch-through device pin-out.

Oxidized		l_{PT} [nm]								
		320	330	340	350	360	370	380	390	400
w_{PT} [nm]	220	*34*	*25*	*29*	*35*	*26*	*30*	**38**	*27*	**33**
	260	*36*	**39**	*31*	**34**	*28*	*37*	**40**	*32*	**35**
	300	*38*	**3**	*33*	**1**	**4**	**36**	**2**	-	**37**

Legend: *pin on Chip1* **pin on Chip2**

Table 4.6. Non-thinned punch-through device pin-out.

Not oxidized		l_{PT} [nm]								
		320	330	340	350	360	370	380	390	400
w_{PT} [nm]	220	22	16	28	23	17	29	11	18	6
	260	24	12	30	7	19	26	13	31	8
	300	27	20	32	14	21	9	15	-	10

All pins on *Chip2*

The node common to all above devices is connected to pad 5.

Figure 4.24 shows *Chip2*, which is populated with the 2D-confined n^+pn^+ punch-through SOI light sources.

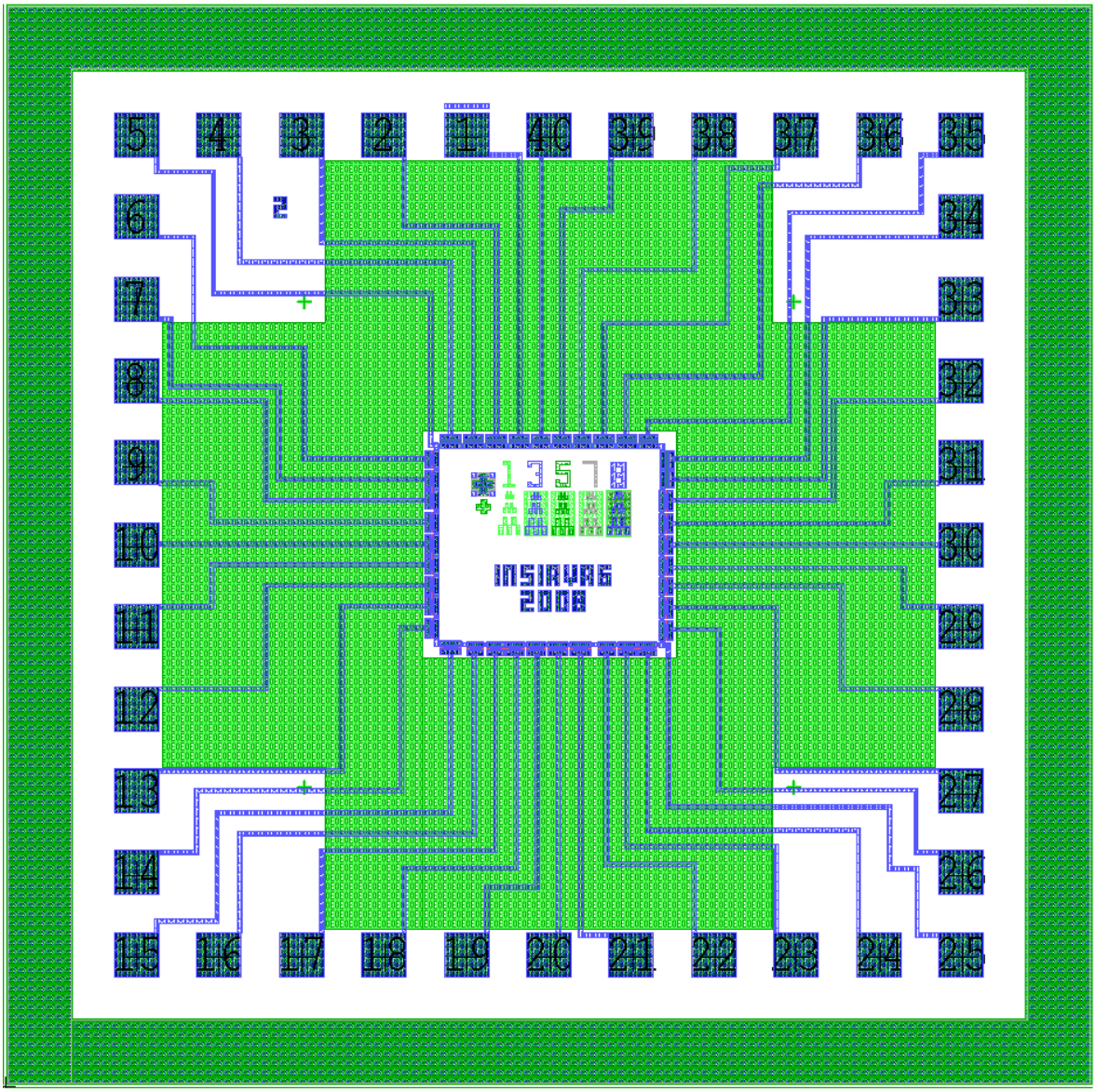


Figure 4.6. *Chip2* layout.

Chip1 and *Chip2* contain 2D-confined n^+pn^+ punch-through SOI light sources, but most are located on *Chip2*.

4.5.1.3. Carrier-injection Light Sources

Two different carrier-injection SOI light sources were designed and implemented: The *Opposite* injector configuration has a forward-biased injector and reversed-biased acceptor junctions opposite to each other and the *Side* configuration where two injection junctions are adjacent to the acceptor junction.

4.5.1.3.1 Opposite-injectors

Figure 4.7 shows that the opposite-injection SOI light source element has the forward-biased n^+p injector junction (interface between F and I regions) opposite to the reverse-biased n^+p acceptor junction (between R and I regions).

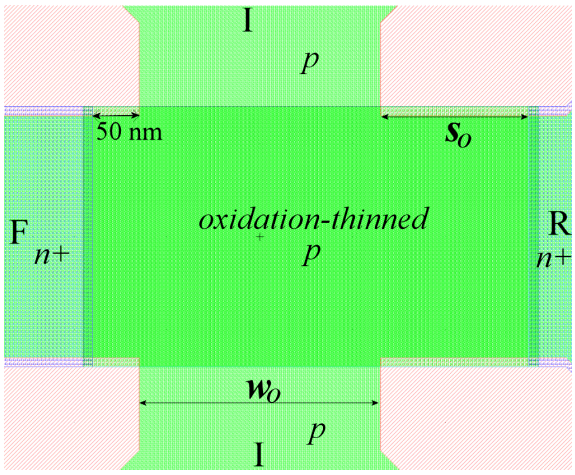


Figure 4.7. Opposite-injection SOI element layout dimension definitions.

It is expected that the reverse-bias depletion region extending from the R-I interface will stretch towards the forward-biased injector junction (F-I interface) from where it will receive cool electrons for radiative recombination with hot holes in its high electric field.

The dimensioning of the devices shown in Figure 4.7 had to comply with the following specifications to ensure proper functionality of the devices:

$$s_O \approx d_{Ox} + 3\Delta R_{\perp As} \approx 126\,\text{nm}, \tag{4.5}$$

$$w_O > w_d + \Delta Si, \tag{4.6}$$

where ΔSi is the Si thickness removed during the thinning oxidations. Equation (4.5) intends to advance the final (after all thermal processing) reverse-bias n^+ interface a distance s_O to the left, i.e. on the right side of the drawn intermediate (I) nodes. Relation (4.6) ensures that the final intermediate node widths are not completely covered by the reverse-bias depletion region so that the injector can still be forward-biased.

Single opposite-side injection elements are implemented in cells as shown in Figure 4.12, which allowed laying them out in interconnected arrays of 19 devices in parallel.

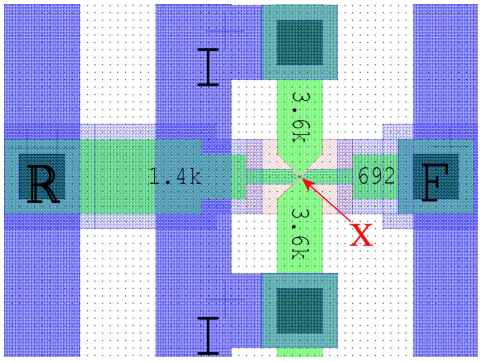


Figure 4.8. Single opposite-injector element layout on a 1-µm grid.

"X" demarcates the location of an injector type shown in Figure 4.7. R, F and I denote the reverse-biased acceptor, forward-biased injector and intermediate nodes respectively.

Table 4.7 lists the dimensions of the implemented opposite-side SOI injector light sources.

Table 4.7. Opposite-side injection devices pin-out.

Opposite-injectors				
Oxidized				
Dimension		s_O [nm]		
	Pin #	120	160	200
w_O [nm]	200	F: 11 I: 12	F: 14 I: 13	F: 15 I: 16
	260	F: 18 I: 17	F: 19 I: 20	F: 22 I: 21
	300	F: 23 I: 24	F: 26 I: 25	F: 27 I: 28
Non-oxidized				
Dimension		s_O [nm]		
	Pin #	120	160	200
w_O [nm]	200	F: 31 I: 32	F: 34 I: 33	F: 35 I: 36
	260	F: 38 I: 37	F: 39 I: 40	F: 2 I: 1
	300	F: 3 I: 4	F: 6 I: 5	F: 7 I: 8

The common reverse-biased node R of all devices is connected to pads 9 and 29.

Figure 4.9 shows how the nine differently dimensioned opposite-side injection light source arrays are arranged in a matrix.

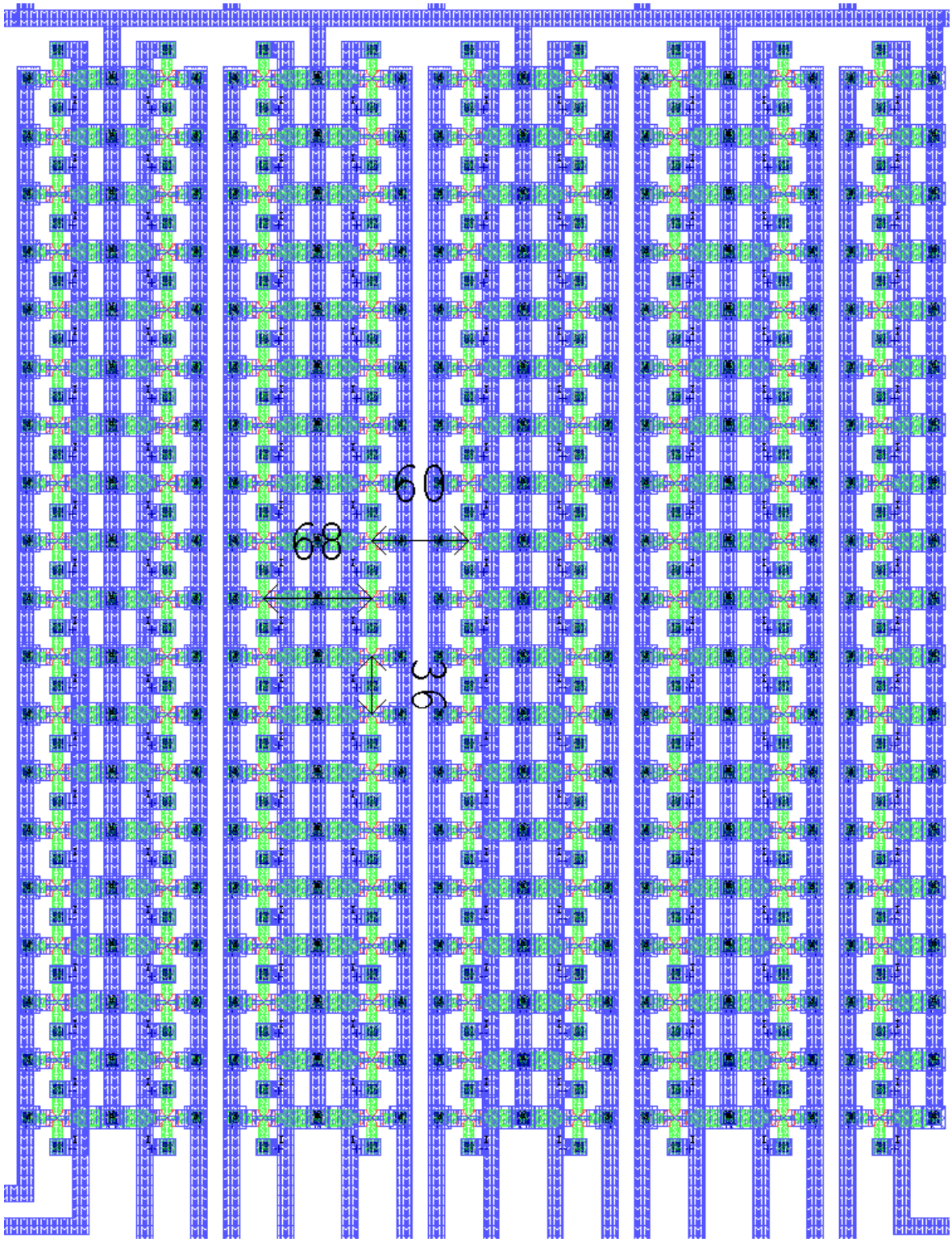


Figure 4.9. Nine columns of 19-element opposite-side injection device line-arrays.

Figure 4.10 shows *Chip3*, which contains the oxidized and non-oxidized opposite-side injection devices.

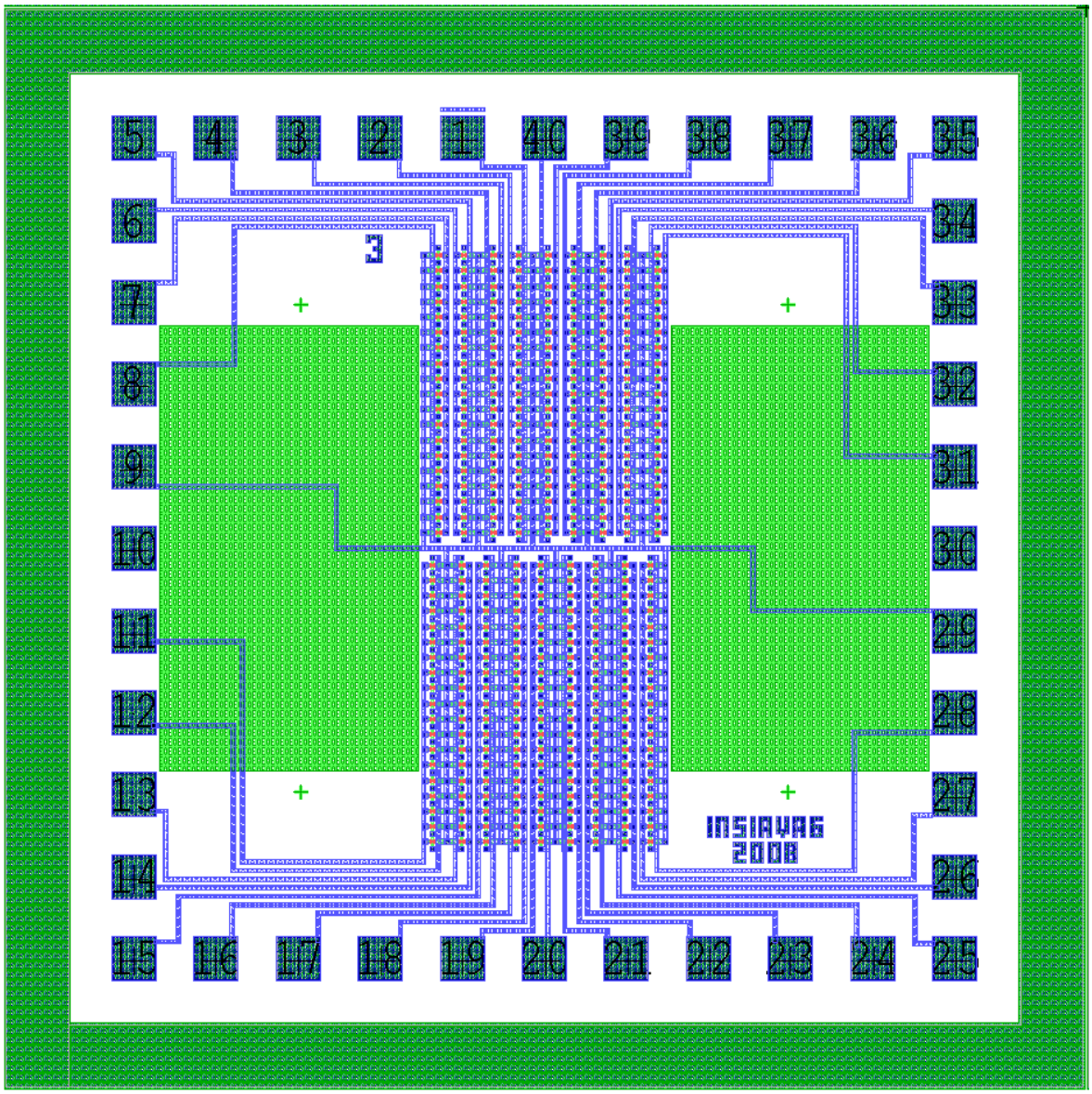


Figure 4.10. *Chip3* layout containing the *Opposite* injector light sources..

4.5.1.3.2 Side-injectors

As shown in Figure 4.11 the side-injection device has two injecting forward-biased junctions (F-I interface) adjacent to the reverse-biased acceptor junction (R-I interface).

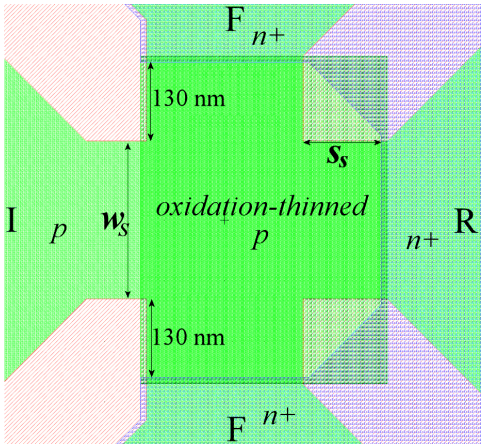


Figure 4.11. Side-injection SOI device layout dimension definitions.

The dimensioning of the devices shown in Figure 4.11 had to comply with the following specifications to ensure proper functionality of the devices:

$$s_S \approx d_{Ox} + 3\Delta R_{\perp As} \approx 86 \text{ nm and} \tag{4.7}$$

$$w_S = w + 2\Delta Si. \tag{4.8}$$

While relation (4.7) attempts to place the final reverse-biased R-I pn^+ acceptor interface a distance s_S to the left so that it borders in line with the right edge of the drawn forward-biased F-I injector interface, equation (4.8) intends to round the final Si strips.

The injection devices in Figure 4.11 are implemented in elemental cells as shown in Figure 4.12, which allowed laying them out in interconnected arrays of 19 devices in parallel.

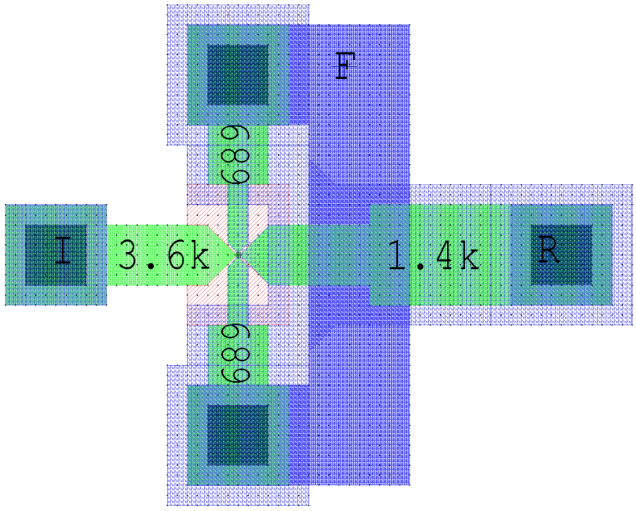


Figure 4.12. Single side-injection SOI injector element layout on a 1-µm grid.

Table 4.8 lists the dimensions of the implemented side-injection SOI light sources.

Table 4.8. Side-injection devices pin-out.

Side-injectors				
Oxidized				
Dimension		x_S [nm]		
	Pin #	50	90	130
w_S [nm]	200	F: 12 I: 11	F: 13 I: 14	F: 16 I: 15
	260	F: 17 I: 18	F: 20 I: 19	F: 21 I: 22
	300	F: 24 I: 23	F: 25 I: 26	F: 28 I: 27
Non-oxidized				
Dimension		x_S [nm]		
	Pin #	50	90	130
w_S [nm]	200	F: 32 I: 31	F: 33 I: 34	F: 36 I: 35
	260	F: 37 I: 38	F: 40 I: 39	F: 1 I: 2
	300	F: 4 I: 3	F: 5 I: 6	F: 8 I: 7

The common reverse-biased node R of all devices connects to pads 9 and 29 (Figure 4.13).

Figure 4.13 shows the layout of *Chip4*, which contains the oxidized and non-oxidized side-injection SOI light sources.

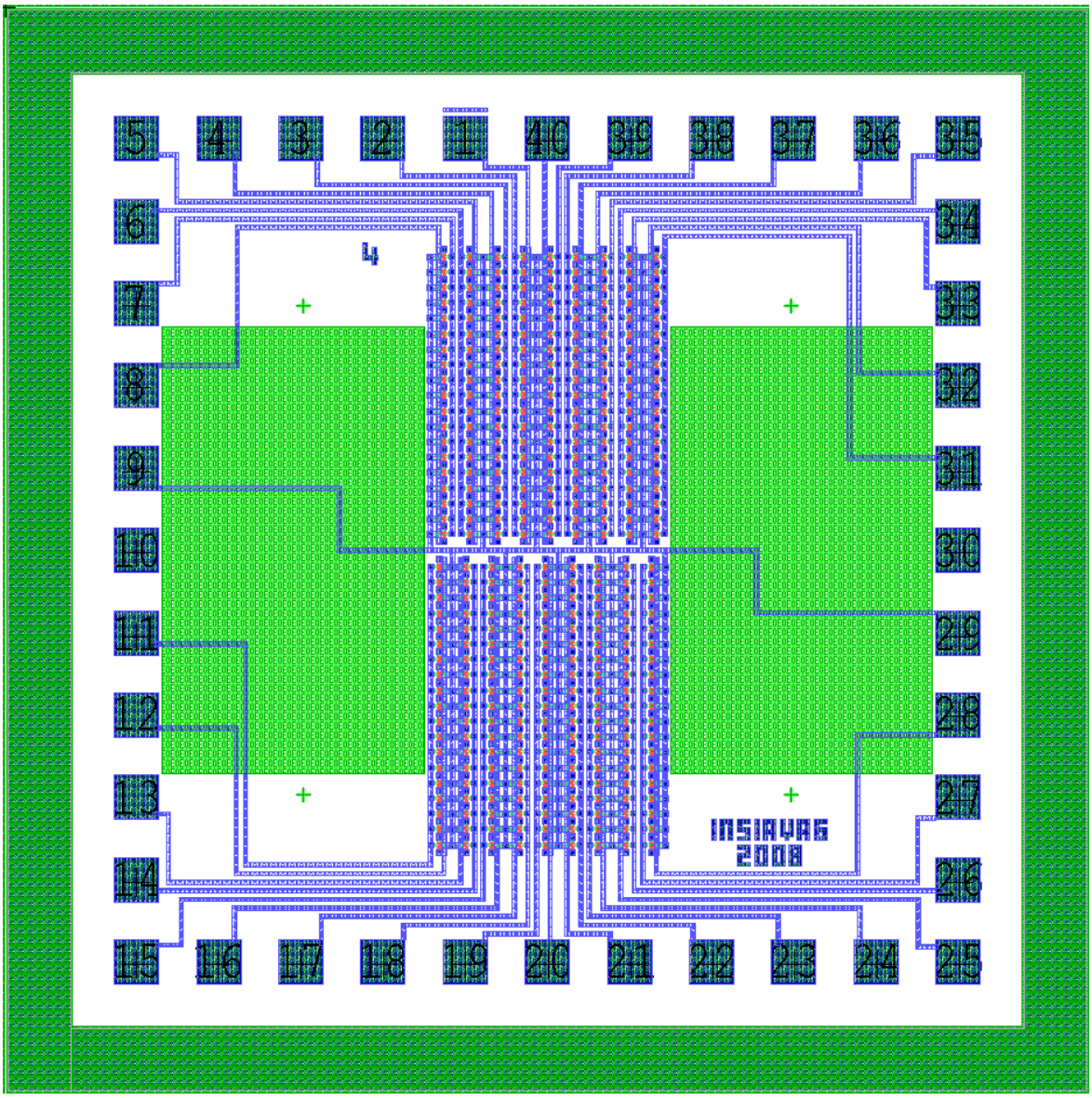


Figure 4.13. *Chip4* layout.

4.5.2. 1D-confined Comparison Light Sources

In parallel to the manufacture of the nanometre-scale SOI light sources, another SOI design (*INSiAVA1*) was manufactured entirely at the CEFIM. This test-chip did not make use of EBL or RIE processing steps and could only produce horizontally large (planar), but vertically thin SOI light sources.

For comparative purposes, some *INSiAVA1* avalanche and punch-through devices were implemented in this work. The implemented *INSiAVA1* devices are geometrically identical to *INSiAVA1* devices manufactured in the CEFIM clean-room, but exist in two variants: One version of *INSiAVA1* devices are oxidation-thinned to about 20 nm while the other set incorporates devices that remain at the initial silicon island thickness of about 150 nm.

4.5.2.1. n^+p Avalanche Light Sources

Figure 4.14 and Figure 4.15 show the dimensions of two *INSiAVA1* avalanche breakdown devices.

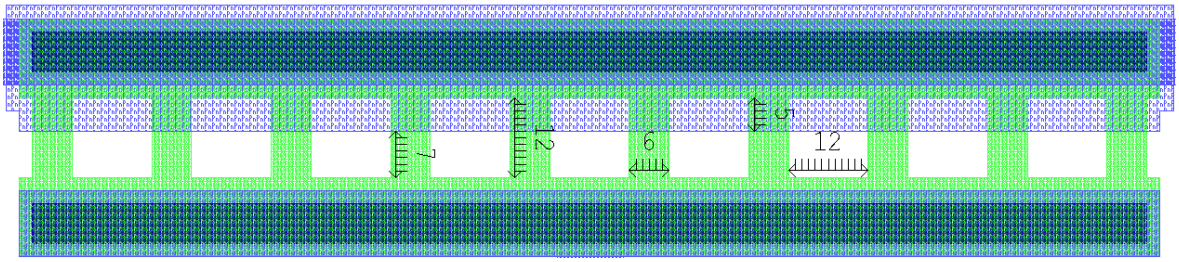


Figure 4.14. *INSiAVA1* n^+p avalanche breakdown device layout.

To possibly increase the light intensity with a higher electric field in a confined light generation area, the device in Figure 4.15 implemented triangular n^+ regions.

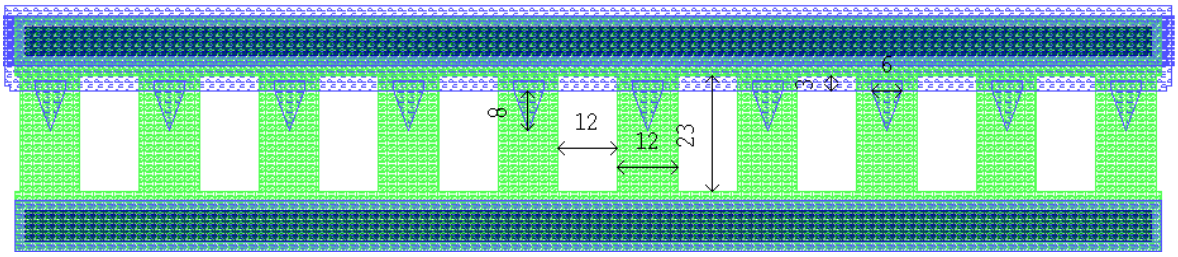


Figure 4.15. Triangular *INSiAVA1* n^+p avalanche breakdown device layout.

4.5.2.2. n^+pn^+ Punch-through Light Sources

Figure 4.16 and Figure 4.17 display the two types of *INSiAVA1* punch-through devices implemented.

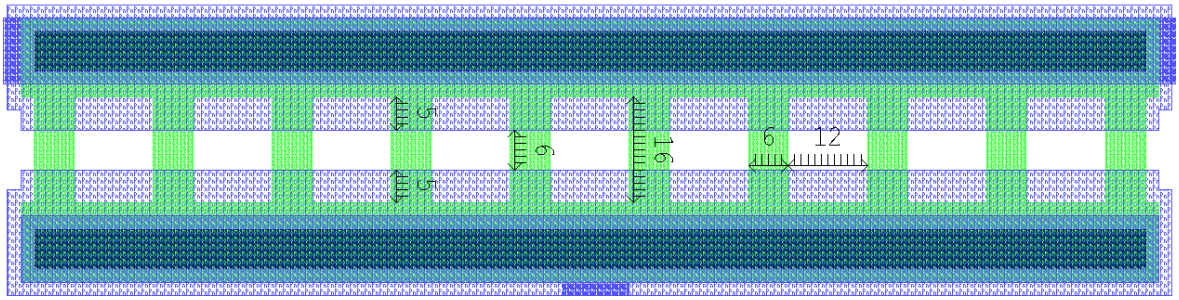


Figure 4.16. *INSiAVA1* n^+pn^+ punch-through device layout.

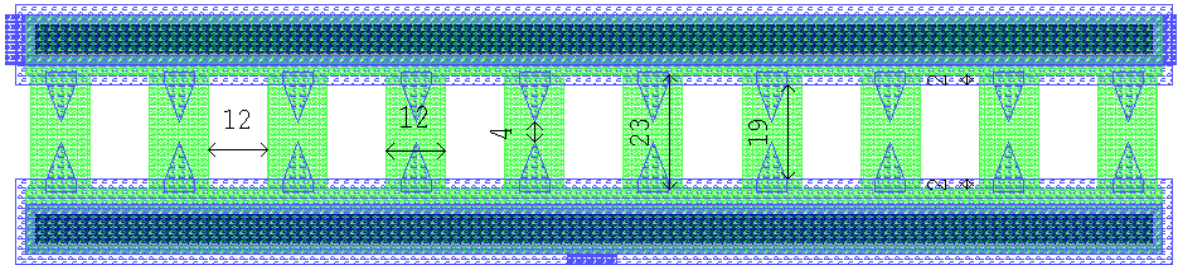


Figure 4.17. *INSiAVA1* triangular n^+pn^+ punch-through device layout.

4.6. Process Monitor Resistors

To measure process and material properties like finger thicknesses and doping concentrations, a matrix of n^+ and p resistor finger devices were included in the design. These resistors had similar dimensions to the avalanche-breakdown junction devices, but were either doped completely n^+ or p.

Figure 4.18 illustrates the process monitor resistor finger width w and length l definitions.

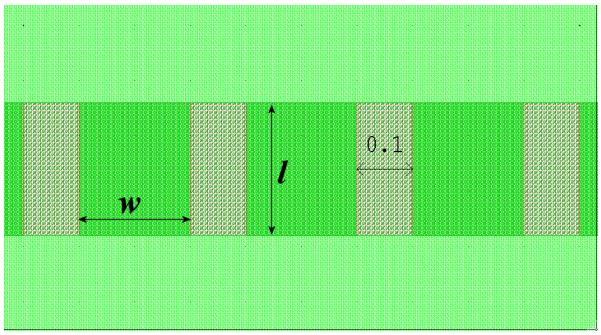


Figure 4.18. Process monitor resistor finger dimension definition.

Figure 4.19 shows a 100-finger process monitoring resistor device layout.

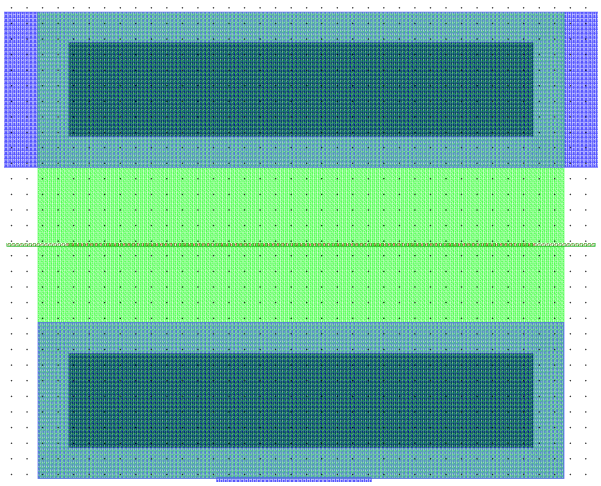


Figure 4.19. 100-finger process monitor resistor layout.

To enable the determination of doping concentration and thickness through resistive measurements, the n^+ and p resistors were each designed in two variants: While the one version had the fingers as shown above, the second version omitted the finger definition mask from the layout. In this way the resistance of various finger widths, as well as very wide, but thin silicon structures could be measured.

Figure 4.20 shows the configuration of the four different process-monitor resistor types.

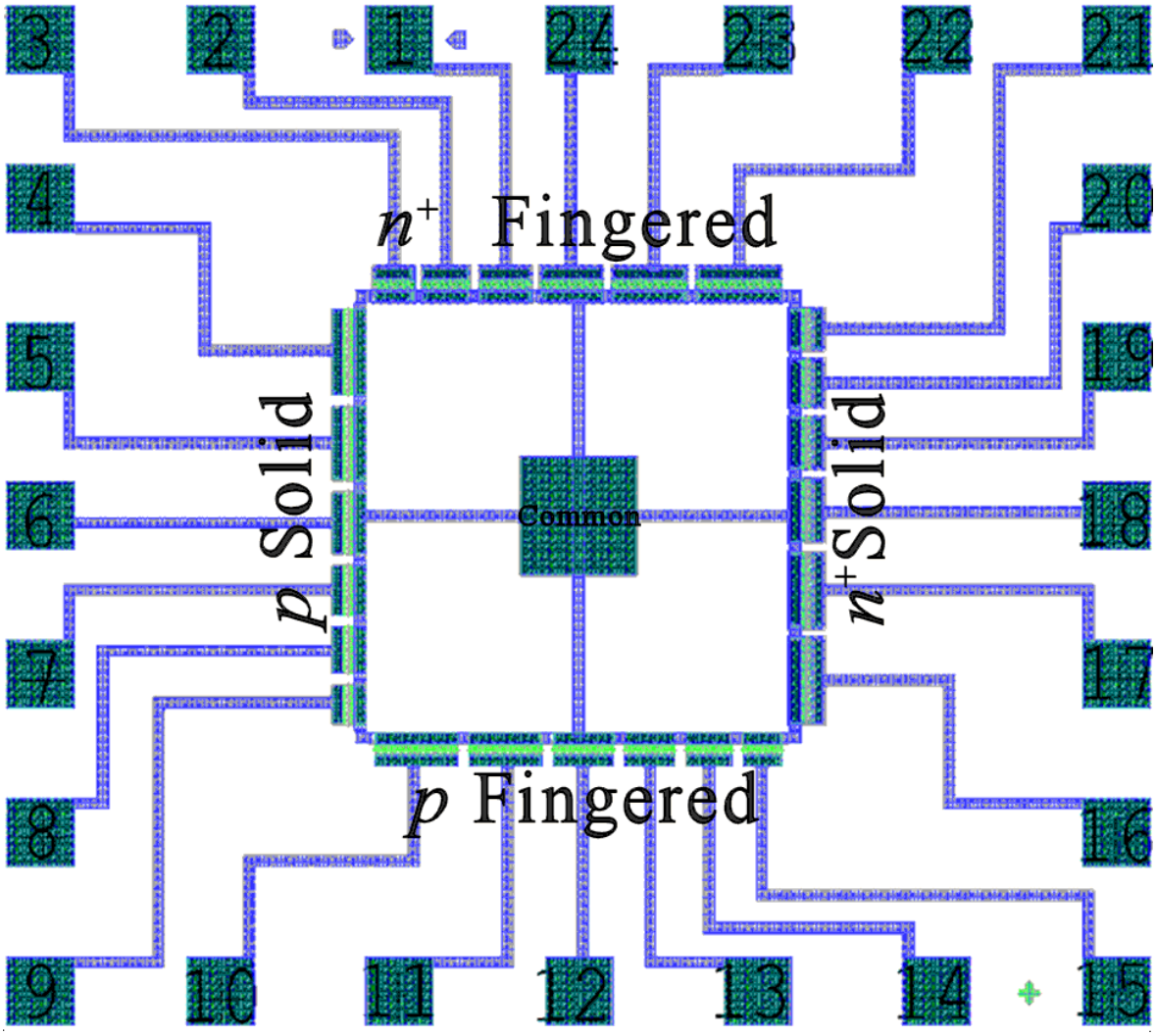


Figure 4.20. Process monitoring resistors.

Table 4.9 lists the dimensions and pin-out of all implemented resistor types.

Table 4.9. Implemented process-monitor resistors.

Chip No.	**Group**	**Device**	**Pin No.**	**Type**	**Oxidized?**	***w***	***l***
	Name					[nm]	
1 (*RsFramed*)	*RnOx*	*Rn200nmOx*	3	n^+	Oxidized	200	240
		Rn260nmOx	2			260	
		Rn300nmOx	1			300	
		Rn400nmOx	24			400	
		Rn500nmOx	23			500	
		Rn600nmOx	22			600	
	RnNoOx	*Rn200nmNoOx*	21		Not oxidized	200	
		Rn260nmNoOx	20			260	
		Rn300nmNoOx	19			300	
		Rn400nmNoOx	18			400	
		Rn500nmNoOx	17			500	
		Rn600nmNoOx	16			600	
	RpOx	*Rp200nmOx*	15	*p*	Oxidized	200	
		Rp260nmOx	14			260	
		Rp300nmOx	13			300	
		Rp400nmOx	12			400	
		Rp500nmOx	11			500	
		Rp600nmOx	10			600	
	RpNoOx	*Rp200nmNoOx*	9		Not oxidized	200	
		Rp260nmNoOx	8			260	
		Rp300nmNoOx	7			300	
		Rp400nmNoOx	6			400	
		Rp500nmNoOx	5			500	
		Rp600nmNoOx	4			600	

The common terminal to all above resistors is connected to a pad at the centre of the resistor cluster in Figure 4.20.

4.7. Alignment Markers

To achieve the required alignment accuracy when positioning the *Arsenic*, *Finger Spacing* and *Oxidation* masks relative to each other, EBL alignment marker crosses were initially etched into the SOI active layer and refined with the first EBL and etch step.

The marker in Figure 4.21 aligned *Finger Spacing* to *Si Island* and then the following EBL features to *Finger Spacing*.

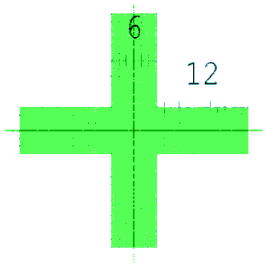


Figure 4.21. *AlignmentMarkerEBL* layout.

The marker in Figure 4.22 aligned *Oxidation (Photo)* to *Si Island*.

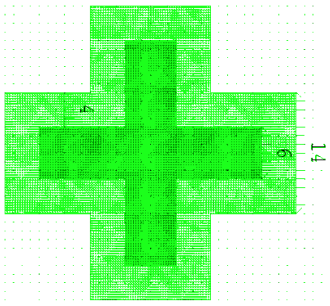


Figure 4.22. *AlignmentMarkerOx* layout.

The marker in Figure 4.23 aligned all photo masks, except *Oxidation (Photo)*, to *Si Island*.

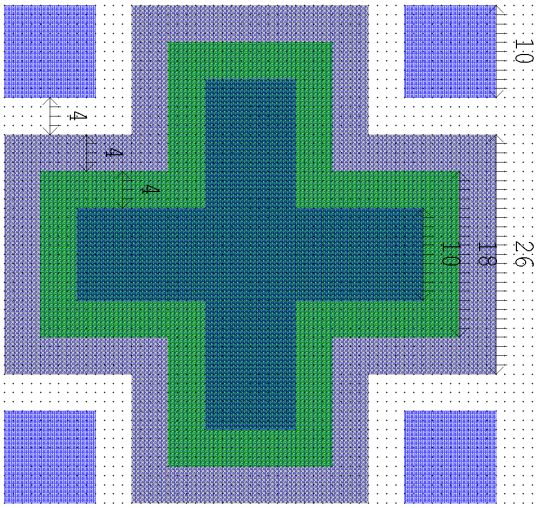


Figure 4.23. *AlignmentMarkerPhotoNoOx* layout.

4.8. Overall Layout

4.8.1. Chip1

Figure 4.24 shows the complete *Chip1* layout that contains the 1D-confined test-devices, the 2D-confined n^+p avalanche breakdown finger-junction light sources, some 2D-confined n^+pn^+ punch-through devices and all process-monitoring resistors

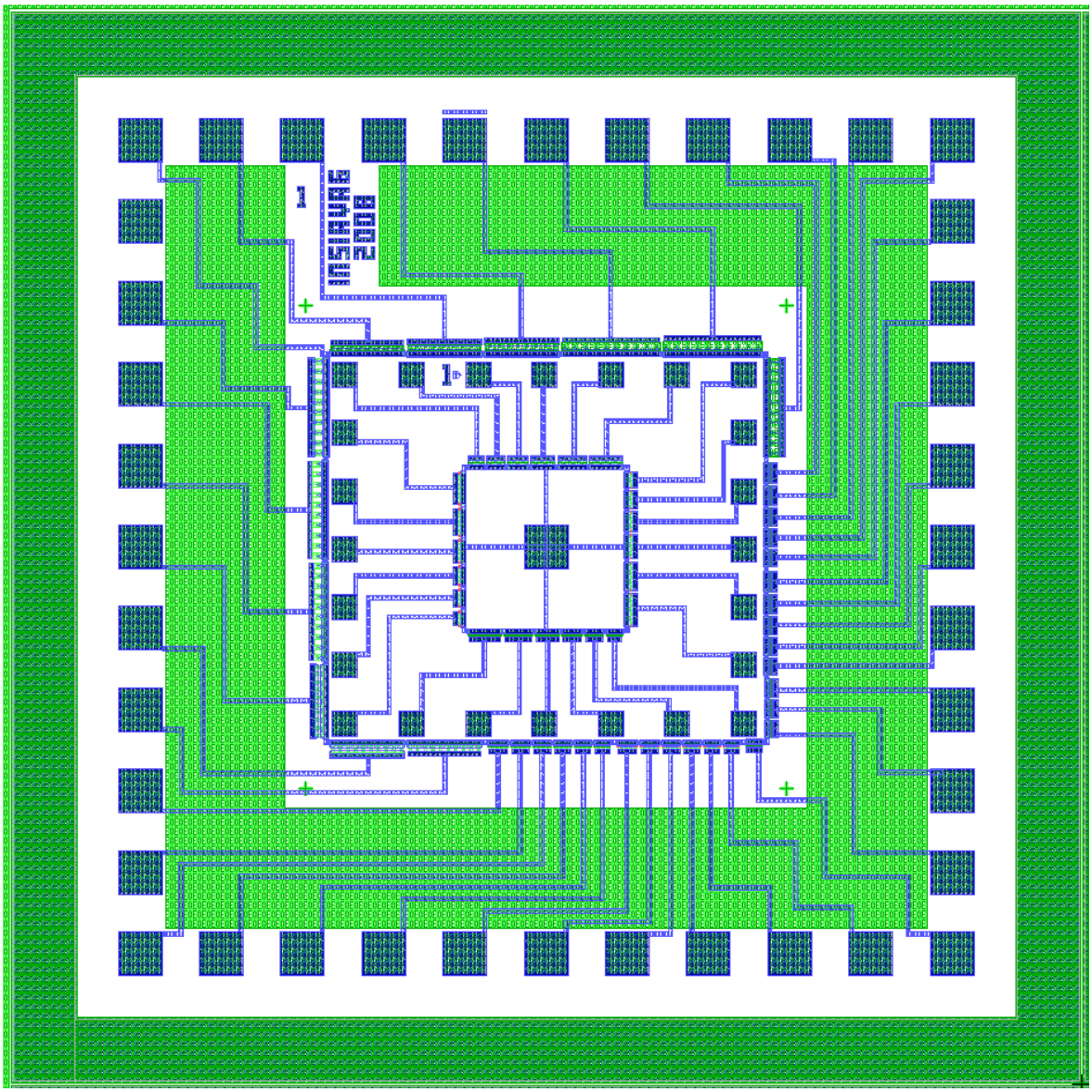


Figure 4.24. *Chip1* layout.

The other three chip layouts were already presented in the sections that described their constituent test devices.

Figure 4.24 depicts the complete four-chip test-cluster CAD layout that was used to manufacture the photolithographic masks and generate the EBL data files required by the JEOL JBX-9300FS electron-beam pattern generator EPG.

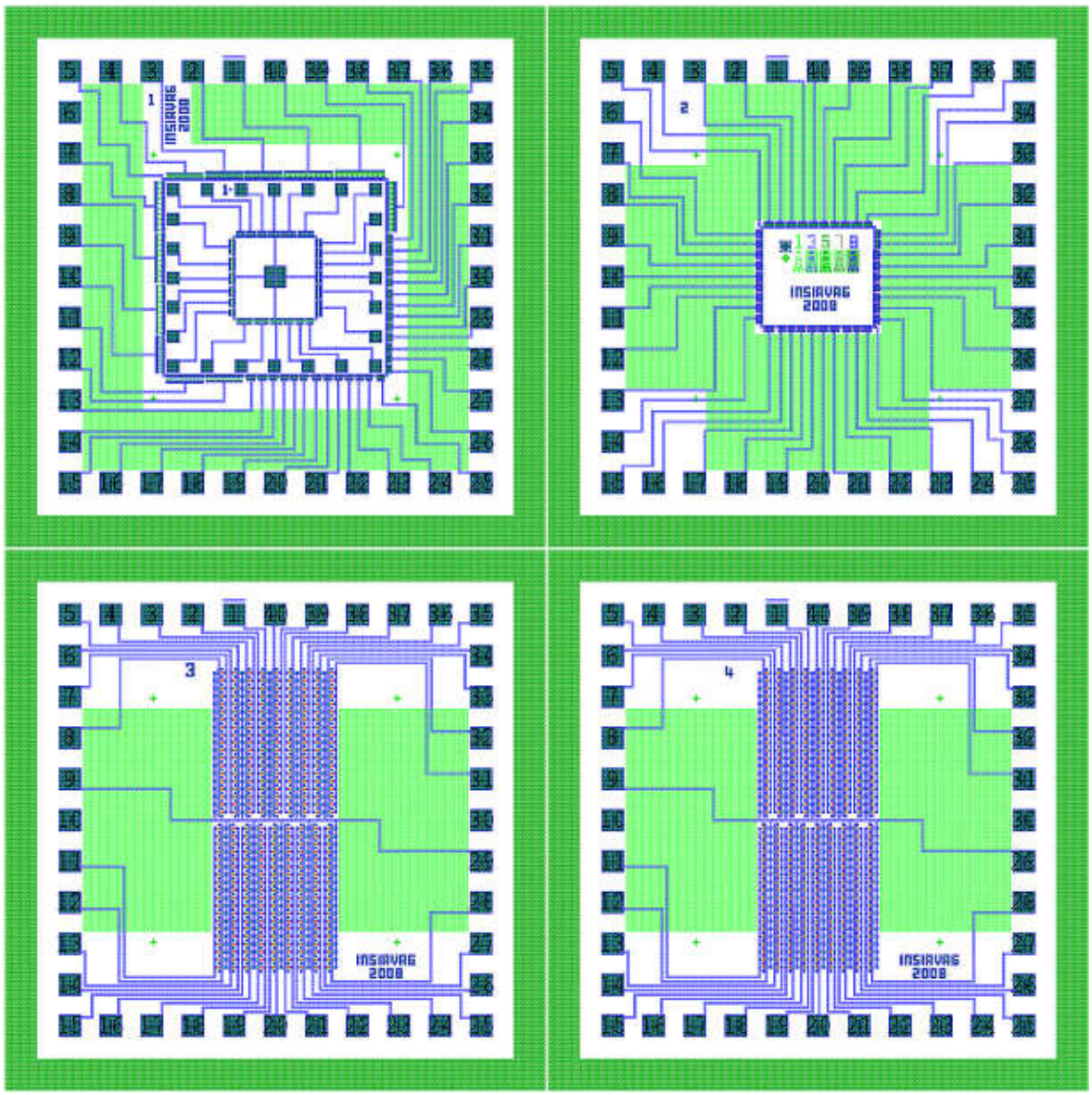


Figure 4.25 CAD layout showing the four chips in a 5.1 mm x 5.1 mm cluster.

Chip 1 in the top-left quadrant of the cluster contains 18 avalanche and 19 punch-through 100-finger SOI light source arrays, *Chip 2* (top right) contains 39 100-finger punch-through device arrays while *Chip 3* and *Chip 4* contain 36 19-element arrays of the two different injection light source types.

4.9. Photo-mask Layout

Figure 4.26 shows that 73 test-chip clusters fit on a 3-inch SOI wafer if 1.5 mm wide Si oxidation-monitoring areas are maintained between clusters.

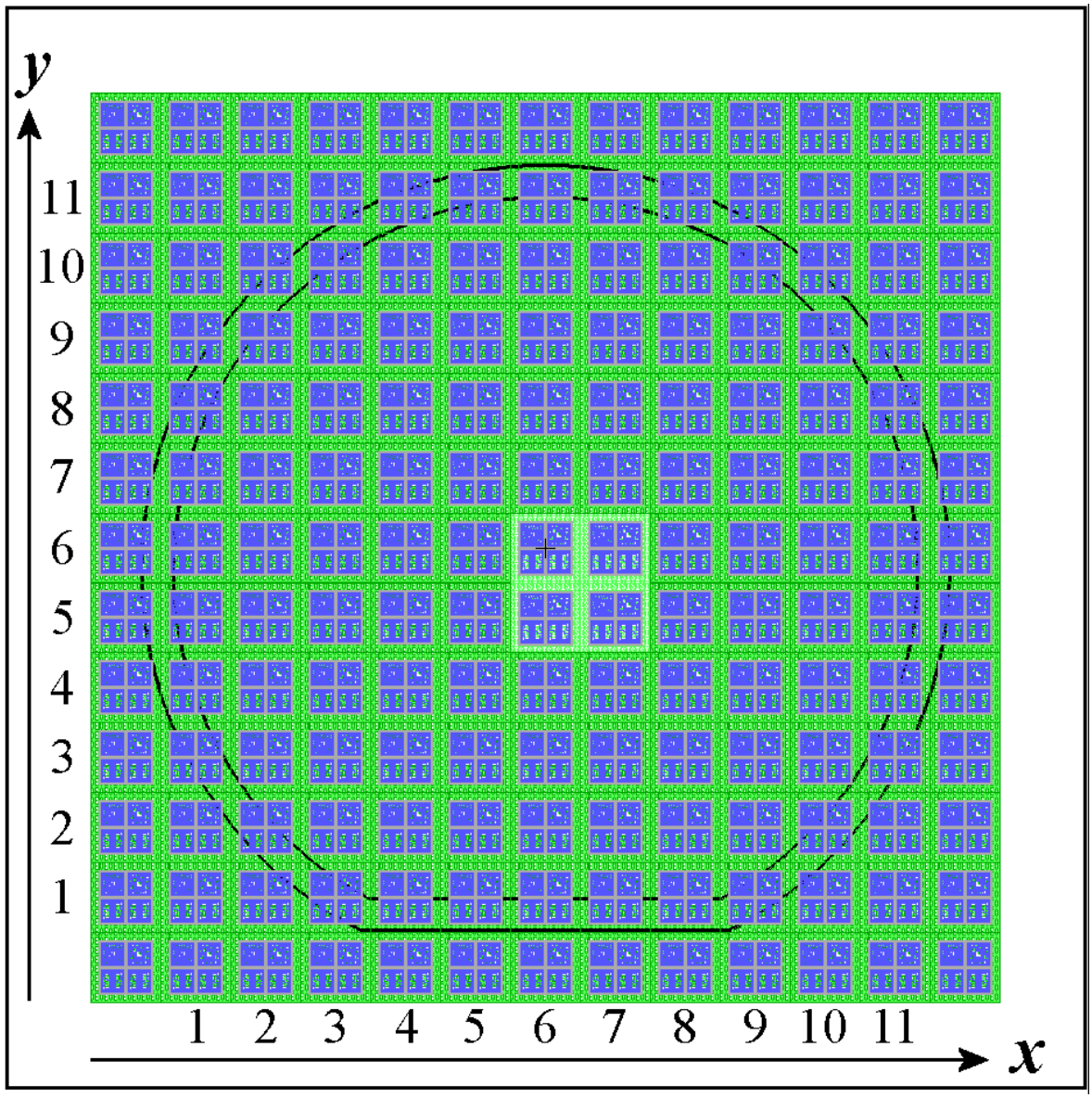


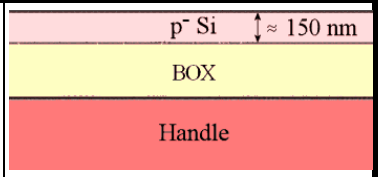
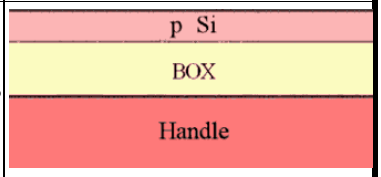
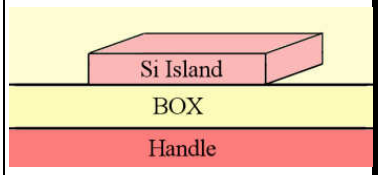
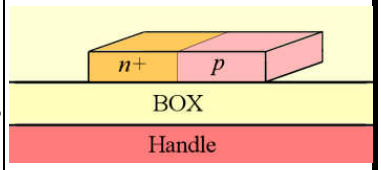
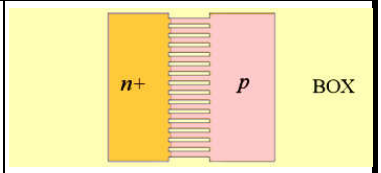
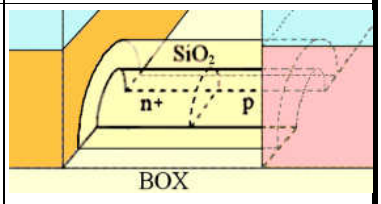
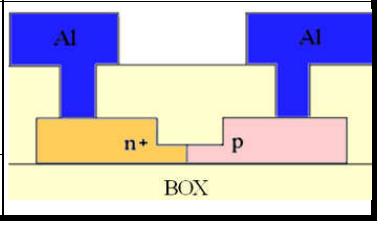
Figure 4.26. Layout and position denotation of the 73 test-chip clusters on a 3-inch wafer.

The four clusters in the approximate middle of the wafer (x = 6, 7; y = 5, 6) are the "*EBL clusters*" and are different from the surrounding "*Photo clusters*". While the *As* and *Oxidation* masks are duplicated on the photo and EBL masks (except for the omission of large oxidation control areas in the EBL files), the *photo-clusters* do not contain the 100 nm wide finger-spacing slits that could only be patterned through EBL.

5. MANUFACTURE

Table 5.1 gives a brief summary of the processing steps, equipment and facilities involved in the manufacture of the SOI light sources.

Table 5.1. Process flow overview.

Step	Section	Action	Equipment	Facilities	Graphical representation
1	5.1	Si thinning	Furnace, Reflective spectrometer	CEFIM, MiRC	
2	5.2	Blanket B implant	Ion implanter	Core Systems	
3	5.3	Si island definition	PECVD, Mask aligner, RIE	MiRC	
4	5.4	As implant	PECVD, EPG, Mask aligner, RIE, Ion implanter	MiRC, Core Systems	
5	5.5	Finger definition	EPG, RIE	MiRC	
6	5.6	Finger thinning oxidation	PECVD, EPG, Furnace	MiRC, CEFIM	
7	5.7	Metallization	PECVD, Mask aligner, Sputterer	CEFIM, Elume	
8	-	Si isolation spacing	Mask aligner	CEFIM	

Each of the manufacturing steps in Table 5.1 is discussed in more detail in the following subsections in the remainder of this chapter.

Since no standard process recipe was employable, the complete manufacturing process had to be designed on self-obtained equipment characterization data, material and chemical properties.

To ensure consistent results and confirm acceptable manufacturing performance, process control and monitoring was employed. This involved the simultaneous processing of monitor wafer pieces and the measurement of on-chip test-structures that could be analyzed with a SEM, a reflective spectrometer (to measure thin film thicknesses) and a profilometer.

The processing equipment was controlled by adapting machine-specific “recipe” variables like processing time, pressure, DC & AC (plasma) power, gas flows, etc.

5.1. Si Thinning

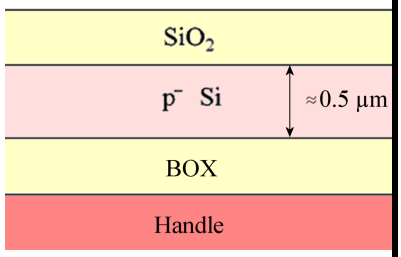
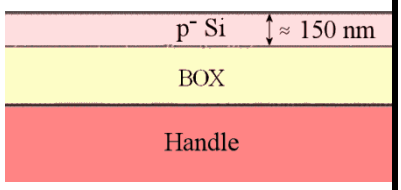
Since as shown in Table 4.1, the initial SOI wafer handle was too thick (0.5 µm ± 0.1 µm), the very first processing requirement was to thin down the SOI device layer. The requirements of the Si island thickness were:

1) The alignment marker thickness should be automatically recognizable by the EPG.
2) The step height from the BOX surface to the Si pad and contact area islands should not cause metal step coverage problems.
3) The difference between initial and final finger thickness (≈ 30 nm) should be easily be reduced through dry oxidation.
4) The Si island thickness should consider the possible handle thickness variation of about 100 nm so that that Si islands should remain after the thinning oxidation.

As a compromise to above requirements, it was decided to aim for an average Si island thickness of about 150 nm.

Table 5.2 lists the processing steps associated with thinning down the SOI wafer handle thicknesses down to about 150 nm.

Table 5.2. Si thinning processing steps.

Step	Action	Equipment	Material	Facilities	Graphical representation
1a	Si wet oxidation 1 h 48 Min @ 1050 ºC (oxidizes ~ 322 nm)	Furnace	H_2O	CEFIM / MiRC	
1b	SiO_2 etch	Fume hood	BOE		
1c	Measure t_{Si}	Reflective spectrometer Chemical scale	-		
Repeat steps 1a to 1c until t_{Si} of each wafer ≈ 150 nm					

The initial thinning oxidations were done in the CEFIM clean-room at UP. Since no reflective spectrometer was available and four-point probe measurements delivered vague Si thickness variation monitoring results during the oxidations, it was decided to use a highly sensitive chemical scale in the CEFIM clean-room to measure the change in wafer weight Δw_{Wafer} and use the wafer diameter D_{Wafer} (Table 4.1) and density of Si d_{Si} (Addendum A) in the relation

$$\Delta t_{Si} = \frac{\Delta w_{Wafer}}{\pi\left(\frac{D_{Wafer}}{2}\right)^2 d_{Si}}, \tag{5.1}$$

to determine the Si thickness Δt_{Si} removed during oxidation. Since Si was removed on both sides of the wafer, the Si device layer thickness reduction $\Delta t_{Device} = \frac{1}{2}\Delta t_{Si}$. Table 5.3 shows the estimated wafer thicknesses after wet oxidation in the CEFIM clean-room and which wafers were selected for further processing at the MiRC.

Table 5.3. Siegert SOI wafer thinning at CEFIM.

Wafer No.	**Start**	**After 1st oxidation** (60 Min wet)			**After 2nd Oxidation** (48 Min wet)				**Processed further at**
	w_{Wafer}		Δw_{Wafer}	Δt_{Device}	w_{Wafer}	Δw_{Wafer}	Δt_{Device}	$\Sigma\Delta t_{Device}$	
	[mg]			[nm]	[mg]		[nm]		
S1	**3616.24**	**3612.81**	**3.43**	**161**	**3609.66**	**3.15**	**148**	**310**	**MiRC**
S2	3632.64	3629.11	3.53	166	3625.95	3.16	149	315	CEFIM
S3	**3593.39**	**3589.85**	**3.54**	**167**	**3586.61**	**3.24**	**152**	**319**	**MiRC**
S4	3563.90	3560.36	3.54	167	3556.82	3.54	167	333	CEFIM
S5	**3605.66**	**3602.13**	**3.53**	**166**	**3598.82**	**3.31**	**156**	**322**	**MiRC**
S6	**3592.44**	**3588.92**	**3.52**	**166**	**3585.53**	**3.39**	**160**	**325**	**MiRC**
S7	3564.79	3561.26	3.53	166	3557.83	3.43	161	328	CEFIM
S8	**3609.29**	**3605.76**	**3.53**	**166**	**3602.46**	**3.30**	**155**	**321**	**MiRC**
S9	3630.30	3626.72	3.58	168	3623.40	3.32	156	325	CEFIM
S10	3647.60	3644.05	3.55	167	3640.69	3.36	158	325	CEFIM
MiRC Wafers **Max**	3616.24	3612.81	3.54	167	3609.66	3.39	160	325	=> $t_{Final} \geq$ 75 nm
Avg	3603.40	3599.89	3.51	165	3596.62	3.28	154	319	=> $t_{Final} \approx$ 181 nm
Min	3592.44	3588.92	3.43	161	3585.53	3.15	148	310	=> $t_{Final} \leq$ 290 nm
Δ [%]	0.66	0.66	3.13	3	0.67	7.32	7	5	

The five wafers to be processed further at the GT MiRC were optically selected to have the least thickness variation. This could be judged by counting the interference rings visible on the surface of the wafer.

Reflective spectrometer measurements at the MiRC showed that the SOI device layer thicknesses were in fact quite a bit thicker than estimated from wafer weights at the CEFIM. Table 5.4 shows the MiRC-measured SOI device layer thicknesses and the required oxidation times for each wafer to obtain the desired 150 nm layer thickness.

Table 5.4. Siegert SOI wafer thicknesses measured at the MiRC after oxidation at CEFIM.

		Measured									To be removed	After Removal		Desired t_{SiO2}	$T_{Oxidation}$ @ 1100 ºC
Wafer No.	**Measurement Set**	**BOX**	**Mid**	**N**	**E**	**S**	**W**	**Avg**	**Min**	**Max**		**Min**	**Max**		
		[nm]													
S1	1st	9795	312	460	392	259	260	338	258	461	**188**	70	273	426	49 Min
	2nd		308	459	387	258	279								
S3	1st	9829	280	211	291	340	167	261	167	340	**111**	56	230	251	21 Min
	2nd		260	229	331	317	180								
S5	1st	9811	444	408	401	467	417	432	393	468	**282**	111	186	640	1 h 37 Min
	2nd		463	409	393	468	448								
S6	1st	9826	525	560	436	423	513	497	423	599	**347**	76	252	789	2 h 19 Min
	2nd		536	599	439	430	512								
S8	1st	9763	299	348	258	295	392	316	258	392	**166**	93	227	376	40 Min
	2nd		297	349	282	293	343								
	Average	9805	372	403	361	355	351	369	167	599	219				

Above table also shows that the original device layer thicknesses averaged about 369 nm + 319 nm = 688 nm, which is above the maximum Siegert wafer thickness specification of 500 nm + 100 nm = 600 nm.

Table 5.5 shows the final measured silicon device-layer thicknesses after thermal oxidation in the Lindburg furnace.

Table 5.5. Wafer thicknesses after thinning oxidation (with aimed 150 nm average).

Wafer No.	**Thickness** [nm]								
	Centre	**North**	**East**	**South**	**West**	**Random**	**Min**	**Average** (Average – 150 nm)	**Max**
S1	124.8 129.9	255.8 273.9	174.2 188.2	44.8 50.2	63.6 77.3	106.6 143.6 112.5 133.5 107.6	44.8	**132.4** (-17.6)	273.9
S3	178.3 193.1	112.7 111.4	187.6 214.0	226.0 208.0	75.6 65.5	145.6 144.6 148.1 150.0	65.5	**154.3** (+4.3)	226.0
S5	152.1 154.4	139.9 133.5	119.5 162.0	173.3 197.7	171.6 167.8		119.5	**157.2** (+7.2)	197.7
S6	209.0 183.6	282.7 286.5	105.1 121.8	128.0 120.5	148.8 146.9		105.1	**173.3** (+23.3)	286.5
S8	138.2 118.0 131.6	186.3 216.3	102.6 98.7	105.3 120.5	148.7 157.7	123.3 132.1 104.0 132.8 100.1 148.3 144.3	98.7	**132.3** (-17.7)	216.3
Average	155.7	199.9	147.4	137.4	122.4	129.3	44.8	**149.9**	286.5

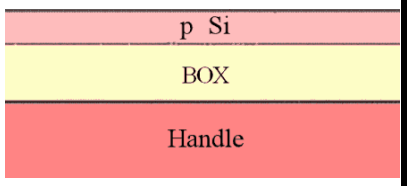
The average device-layer thicknesses are very close to the desired 150 nm, but *S1* and *S8* were about 18 nm thinner and *S6* was about 23 nm thicker than the desired 150 nm device layer thickness.

5.2. Blanket B Implant

Since the initial device-layer *p*-doping of $4 \cdot 10^{14}$ cm^{-3} of the supplied wafers (Table 4.1) was too low, a blanket B implant was necessary to achieve the desired impurity concentration of about 10^{18} cm^{-3}.

As shown in Table 5.6, the wafers had to be annealed after the B implantation at Core Systems[3] in California.

Table 5.6. Blanket B implant processing steps.

Step	Action	Equipment	Material	Facility	Graphical representation
2a	Blanket B implant $7 \cdot 10^{14}$ cm^{-2} @ 10 keV	Ion implanter	-	Core Systems	
2b	Annealing 30 Min @ 950 ºC	Tystar Furnace	N_2	MiRC	

The B implant was actually performed twice. The first implant ($7.24 \cdot 10^{14}$ cm^{-2} at 24 keV) occurred after the first oxidation thinning oxidation at CEFIM, but after receiving the wafers at the MiRC it was noticed that the first B implant was based on the erroneously derived Si thickness of about 181 nm. The resultant impurity concentration after Si thinning oxidation from about 369 nm to 150 nm was too low (see Table 5.7) and required another “top-up” B implant.

[3] Core Systems, A Subsidiary of Implant Sciences Corporation, 1050 Kiefer Road, Sunnyvale, CA

Table 5.7. 4-point probe measured SOI wafer resistivity and derived B doping.

Wafer No.	Resistivity										Doping N_A
	Centre	*North*	*East*	*South*	*West*	**Min**	**Avg**	**Max**	**Δ**		
	[Ω-cm]									[%]	[cm^{-3}]
S1	3.93E-1	3.74E-2	4.22E-2	2.34E-1	3.98E-1	3.74E-2	2.21E-1	3.98E-1	3.61E-1	163	8.27E+16
S3	1.79E-2	3.90E-2	2.06E-2	1.87E-2	1.97E-1	1.79E-2	5.86E-2	1.97E-1	1.79E-1	306	5.22E+17
S5	9.49E-2	1.98E-1	1.06E-1	7.91E-2	7.94E-2	7.91E-2	1.11E-1	1.98E-1	1.19E-1	107	2.14E+17
S6	9.11E-2	7.18E-2	2.12E-1	3.77E-1	1.16E-2	1.16E-2	1.53E-1	3.77E-1	3.65E-1	240	1.38E+17
S8	8.00E-2	6.28E-2	2.34E-1	1.45E-1	2.98E-2	2.98E-2	1.10E-1	2.34E-1	2.04E-1	185	2.17E+17
					Overall	1.16E-2	9.35E-2	3.98E-1	3.86E-1	413	2.73E+17

Wafers *S1*, *S3*, *S6* and *S8* (with average thickness of 144 nm) were sent to Core Systems for the top-up B implant. Wafer *S5* was arbitrarily chosen as a test-wafer with which to continue processing experiments.

Figure 3.1 shows that the average B concentration in the silicon is approximately reduced by a factor 45 during all oxidations (reducing the finger thickness from 150 nm to about 30 nm). This means that a final average B concentration of 10^{18} cm^{-3} (when the fingers are oxidized down to about 30 nm) requires an initial doping concentration of about $4.5 \cdot 10^{19}$ cm^{-3} when the fingers are still 150 nm thick. From Table 5.7 the geometrical mean B doping concentration of *S1*, *S3*, *S6* and *S8* was about $1.9 \cdot 10^{17}$ cm^{-3}. This means that the required implant dose $D = (4.5 \cdot 10^{19}\ cm^{-3} - 1.9 \cdot 10^{17}\ cm^{-3})(144\ nm) \approx 6.5 \cdot 10^{14}\ cm^{-2}$.

From Table 5.5 the implant energy is calculated for a range R_P equal to half the minimum Si thickness t_{Min}: $R_P = t_{Min}/2 = 44.8\ nm/2 = 224$ Å.

Data provided by Core Systems in Figure 5.1 shows that B ions implanted at their lowest acceleration energy of 10 keV penetrate to a range of about 400 Å, which was sufficient.

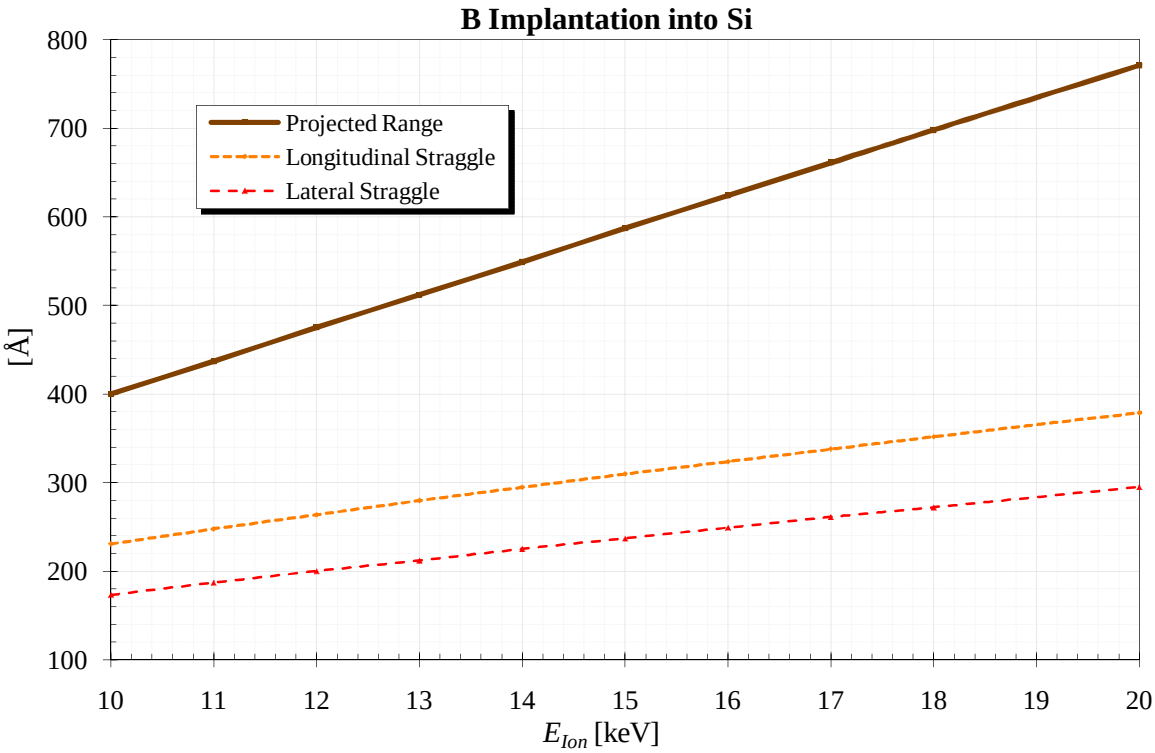


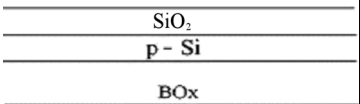
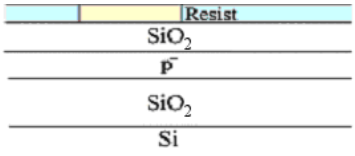
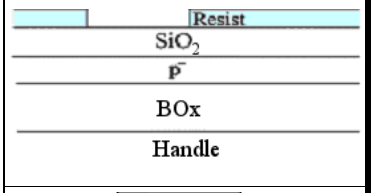
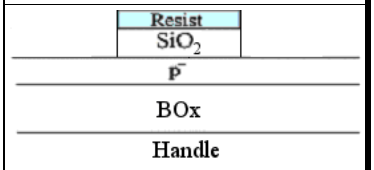
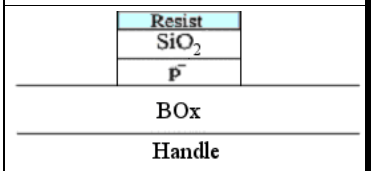
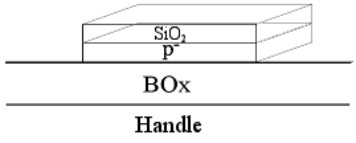
Figure 5.1. B implantation into Si range and straggle.

During wafer shipment to Core Implantation Systems in California for B implantation, wafer *S6* unfortunately broke and had to be excluded from subsequent processing.

5.3. Si Island Definition

Table 5.8 below shows the processing steps taken to create the Si islands on the BOX.

Table 5.8. Si island definition processing steps.

Step	Action	Equipment	Material	Facility	Graphical representation
3a	SiO_2 deposition 1 Min 20 s: 71 nm (Addendum D.3)	Unaxis PECVD	-	MiRC	
3b	Surface Dehydration (10 Min @ 120 ºC)	Oven	-		
3c	PR application (4 000 RPM: 1.2 µm)	Spin-coater	SC1813		
3d	Soft-bake PR (1 Min @ 115 ºC)	Hot-plate	-		
3e	Pattern transfer/ exposure ($t_{Exposure}$ = 3.6 s)	Karl Süss MA6 mask aligner	Si Island Photo-mask		
3f	Develop PR (1 Min)	Fume hood	FM319		
3g	Hard-bake PR (110 ºC, 30 Min)	Hot-plate	-		
3h	SiO_2 etch 5 Min: 71 nm (Appendix D.4.3.2)	Vision RIE	-		
3i	Si etch 2 Min: 286 nm (Addendum D.4.2.1)		-		
3j	PR strip	Fume-hood	10 Min Piranha 4:1 98 % H_2SO_4 : 30 % H_2O_2 560 ml + 140 ml = 700 ml		
3k	Wash wafers				

The first photolithographic Si island definition consumed three days due to problems with the Karl Süss MA6 TSA mask aligner. The initial photolithographic exposures were out of focus as shown in Figure 5.2.

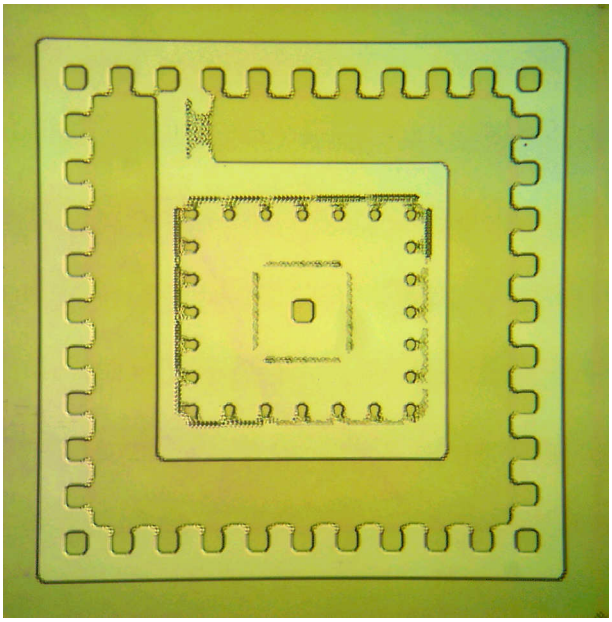


Figure 5.2. Bad *Chip1* Si Island exposure (step 3f).

After investigating many possible causes (including wafer warp and PR adhesion), it was found that the mask aligner had a cut in its wafer holder vacuum seal and that its wafer-holding screws were too far turned out for the thinner than usual Siegert SOI wafers. After faultfinding and fixing the mask aligner, decent photolithographic exposures, as shown in Figure 5.3, were achieved and subsequent photolithography was successful.

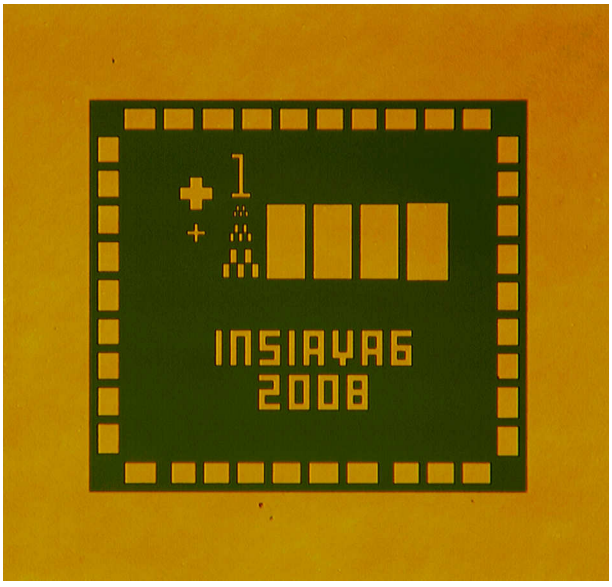
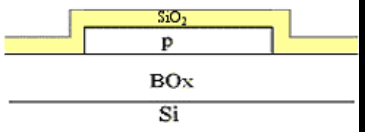
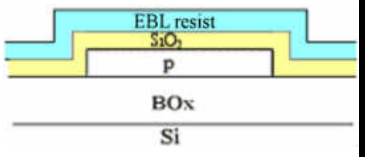
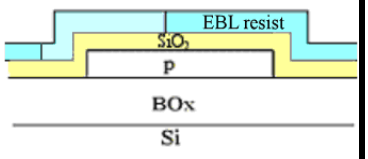
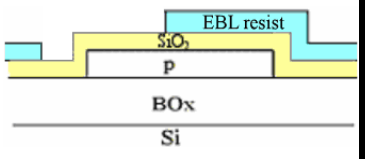
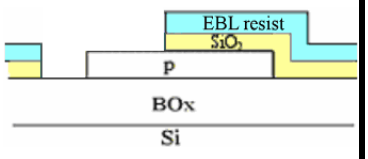
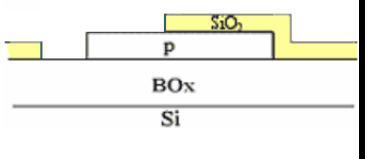


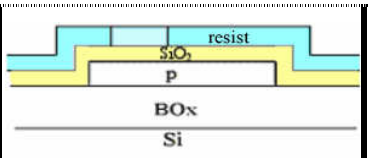
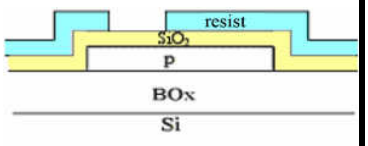
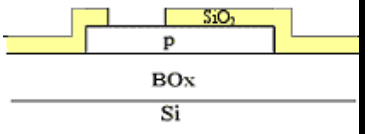
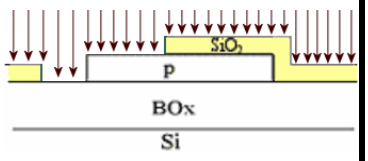
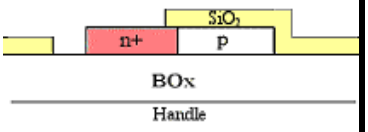
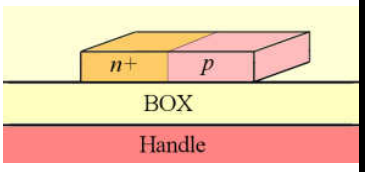
Figure 5.3. Proper *Chip2* Si Island exposure (step 3f).

5.4. As Implant

Table 5.9 lists the steps involved in implanting the As where n^+ diffusions are intended.

Table 5.9. Arsenic implantation processing steps.

Step	Action	Equipment	Material	Facility	Graphical representation
4a	SiO_2 deposition 3 Min 32 s: ≈ 200 nm (Addendum D.3)	Unaxis PECVD	Control wafer pieces	MiRC	
4b	Apply positive EBL resist (1 Min 2000 RPM: 500 nm)	Spin-coater	ZEP520A EBL resist		
4c	Soft-bake EBL resist (180 ºC for 2 Min)	Hot-plate	-		
4d	EBL exposure (200 µC/cm^2)	JEOL EPG	*As (EBL)* file		
4e	Develop EBL resist (2 Min)	Fume hood	Amyl Acetate		
4f	Wafer rinse (30 sec IPA immersion)		IPA		
4g	SiO_2 etch 13 Min: 210 nm (Addendum D.4.3.2)	Vision RIE	Control wafer pieces		
4h	ZEP de-scumming		O_2		
4i	Dehydration bake (10 Min @ 120 ºC)	Oven	-		
4j	PR application (4500 RPM: 1.1 um)	Spin-coater	SC1813		

4k	Pattern transfer exposure Mask EBL clusters with tape 4s	Mask aligner	As (Photo) mask	MiRC	
4l	Develop & hard-bake PR	Fume hood & oven	MF319 developer		
4m	SiO_2 etch (Si also etched!) 13 Min: 210 nm	Vision RIE	Control wafer pieces		
4n	PR removal & wafer clean	Fume-hood	Piranha H_2SO_4 & H_2O_2		
4o	As implant ($1.5 \cdot 10^{14}$ cm^{-2} @ 118 keV)	Ion implanter	As	Core Systems	
4p	Anneal 30 Min @ 950 ºC	AET RTP	N_2	MiRC	
4q	SiO_2 etch (Addendum D.2)	Fume hood	BOE		

Before the wafers could be sent to Core Systems for As implantation, holes had to patterned and etched into a SiO_2 masking layer that should be thick enough to prevent As from penetrating through it and reach the Si underneath it. Since it was determined that on some wafers an average of about 18 nm of the SiO_2 mask was not completely etched away in the n^+ implantation holes, it was decided to increase the As implantation acceleration energy to penetrate these thin SiO_2 layers.

Data supplied by Core Systems in Figure 5.4 shows that As implanted at E_{Ion} = 118 keV penetrates to a range Rp_{As_Si} of about 80 nm with lateral straggle $\Delta R\perp_{As\_Si}$ of about 18 nm.

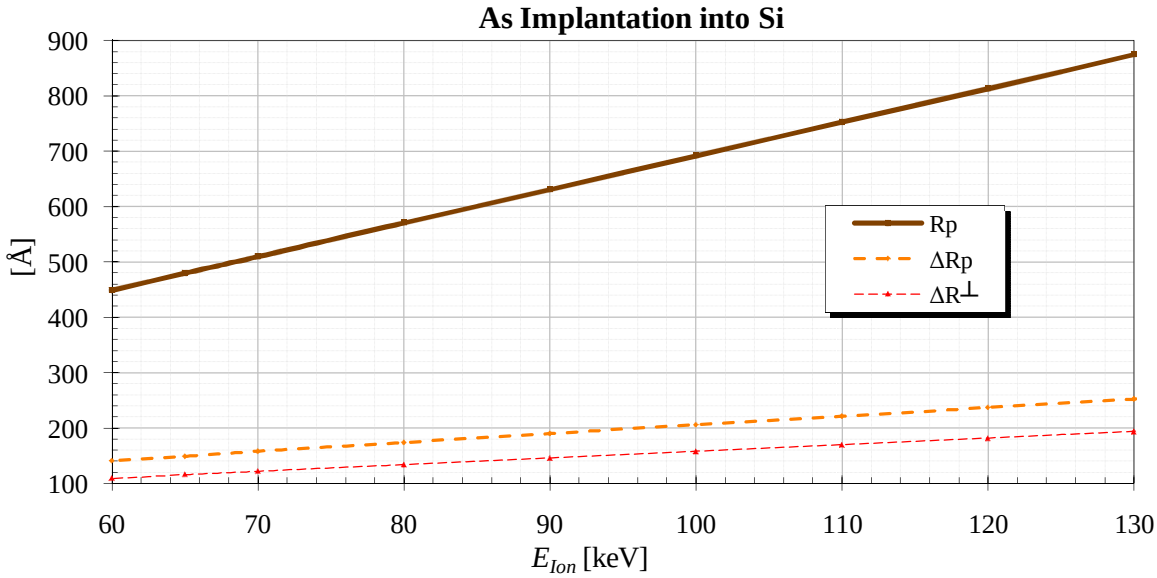


Figure 5.4. As implant range Rp_{As_Si}, longitudinal ΔRp_{As_Si} and transverse straggle $\Delta R\perp_{As\_Si}$ in Si.

Figure 5.5 shows that As implanted into SiO_2 at 118 keV will have a range of about 58 nm.

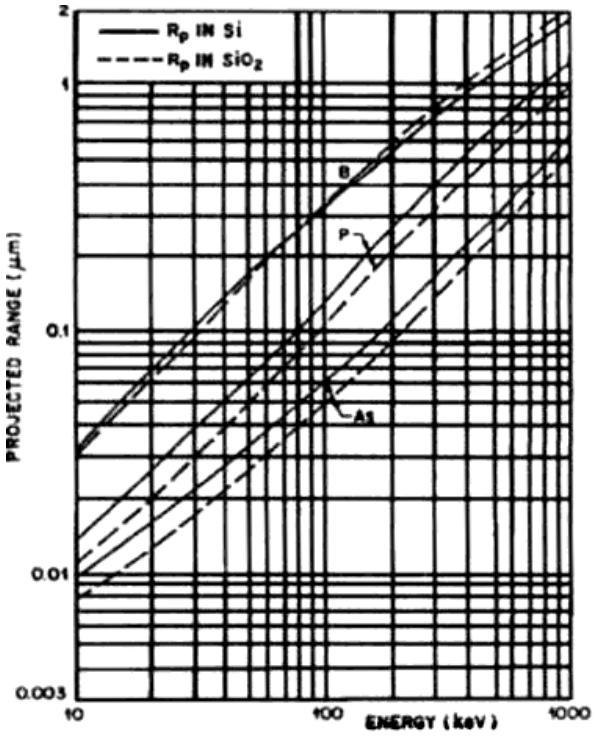


Figure 5.5. Projected ion implantation range Rp_{As_SiO2} in SiO_2 [91].

Since no straggle data was found for As implantation into SiO_2, it is assumed that a SiO_2 mask thickness of twice the projected range Rp_{As_SiO2} should be sufficient to block the As implant from reaching the underlying Si. Therefore $t_{SiO2} > 2Rp_{As\_SiO2}$ = 116 nm.

Figure 5.6 shows an *Opposite-injector* As mask pattern generated in the EBL resist during step 4f.

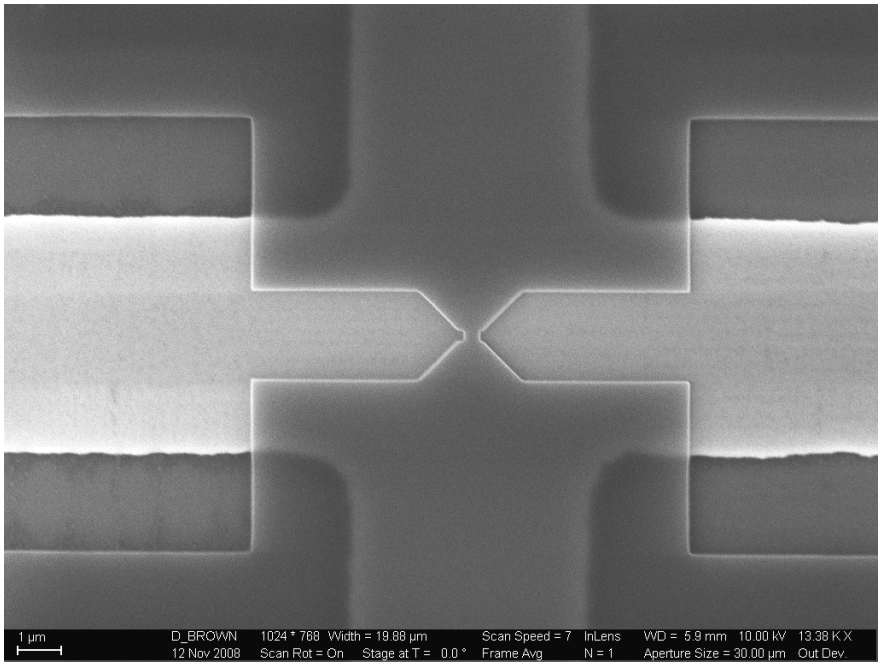


Figure 5.6. Arsenic EBL pattern in ZEP on oxide mask (step 4f).

Figure 5.7 shows the Arsenic mask spacing for the n^+pn^+ punch-through finger junctions after SiO_2 removal in the Vision RIE in step 4g.

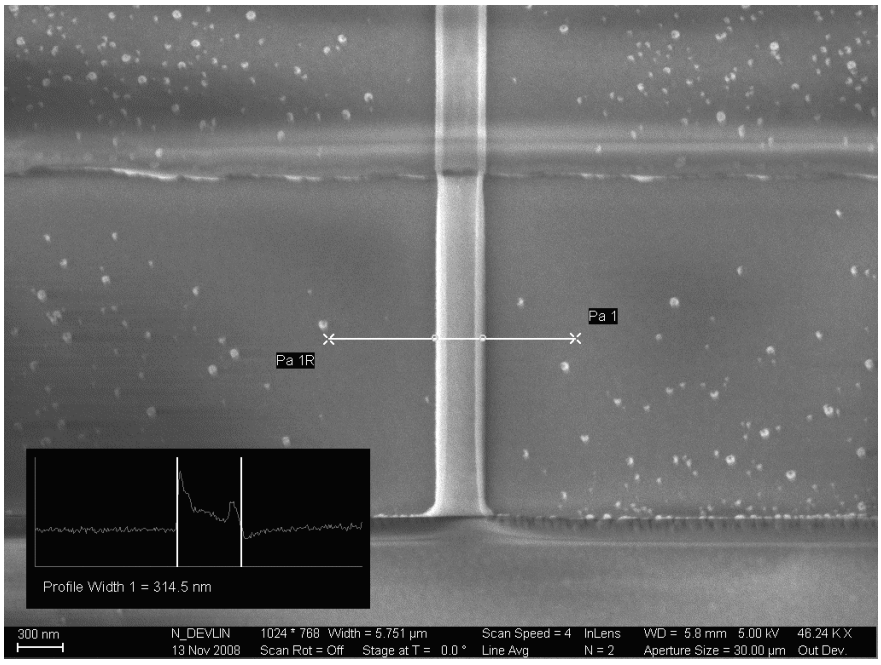


Figure 5.7. Arsenic EBL pattern after RIE (step 4g).

The 315 nm wide vertical stripe is the remaining SiO_2 that masks the intermediate region of the punch-through devices from the As implant.

Figure 5.8 shows an optical microscope image of patterned holes in the SiO_2 Arsenic masking layer at step 4h before Arsenic implant.

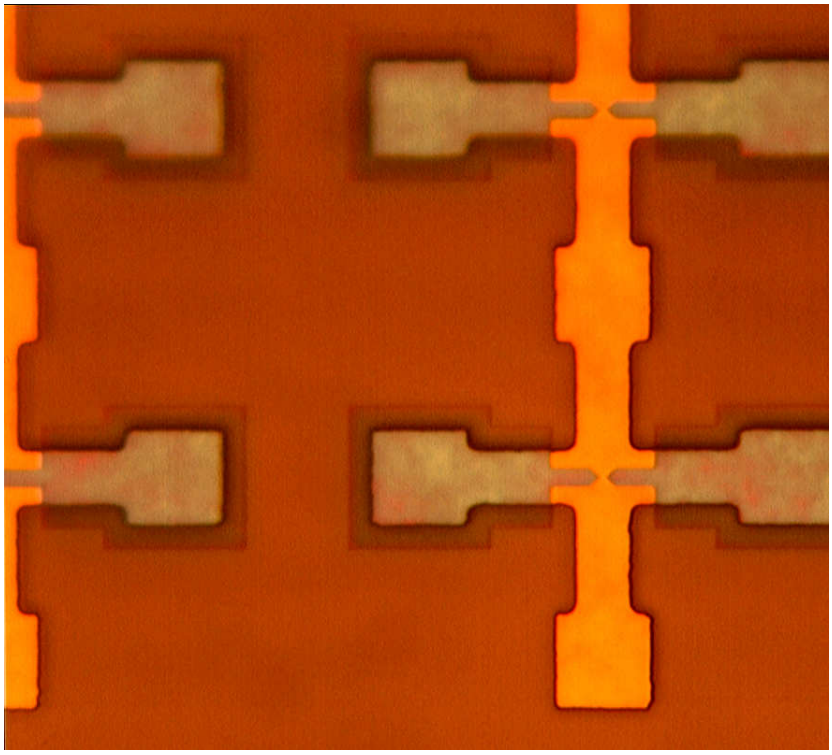


Figure 5.8. Arsenic EBL pattern before implant (step 4h).

Figure 5.9 shows the Arsenic implant holes etched into the SiO_2 mask generated by the photolithographic process at step 4m.

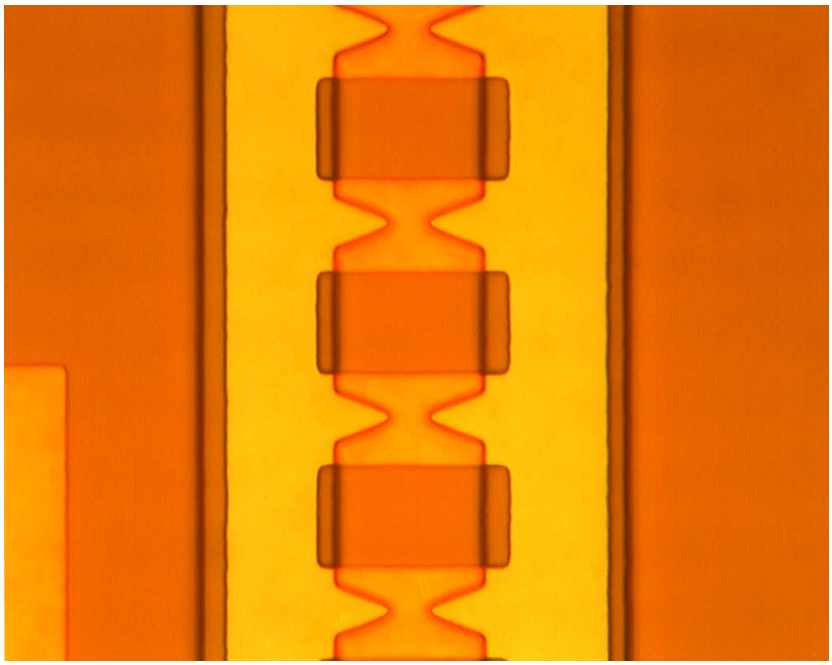
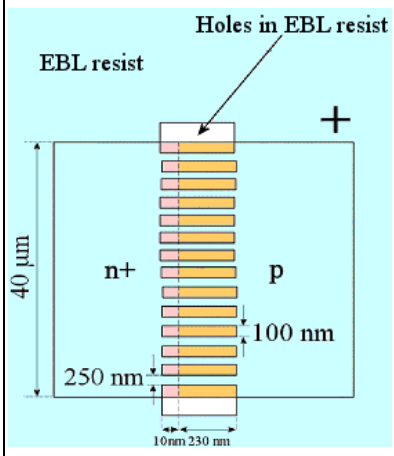
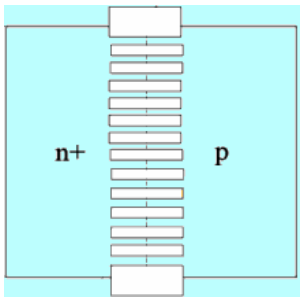
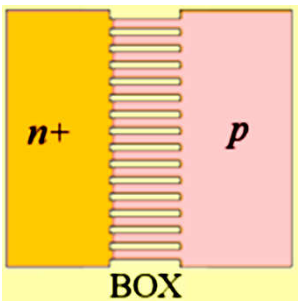


Figure 5.9. After Arsenic Photo RIE (step 4m).

5.5. Finger Definition

Table 5.10 shows the physical manufacturing steps involved in defining and etching the finger spacing strips into the Si.

Table 5.10. Finger definition process flow.

Step	Action	Equipment	Material	Facility	Graphical representation
5a	EBL: EBL steps 4b to 4h 600 nm ZEP Align to *Si Island* EBL marker (w_{Finger} = 2h_{Finger}, n_{Finger} = 100)	JEOL EPG	*Finger Spacing* EBL file	MiRC	
5b	Si etch	ICP	-		
5c	EBL resist removal	Vision RIE	O_2		
5d	Si finger width measurement	SEM	-		
5e	Wafer clean	Wet-bench	Piranha		

The SEM image in Figure 5.10 shows the finger spacing pattern in the ZEP EBL resist.

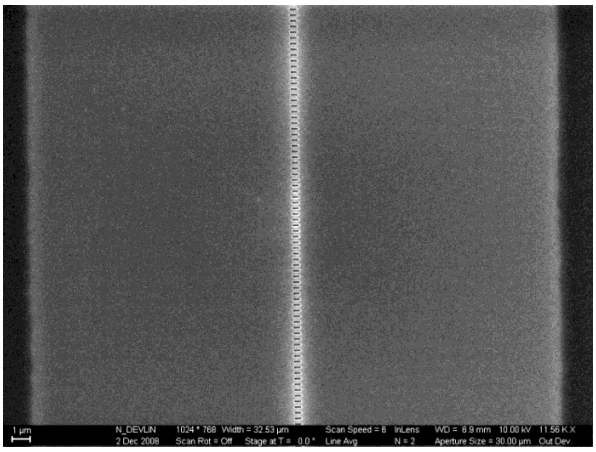


Figure 5.10. EBL finger spacing pattern (step 5a).

Figure 5.11 depicts a closer view of the EPG-written finger spacing pattern in the ZEP.

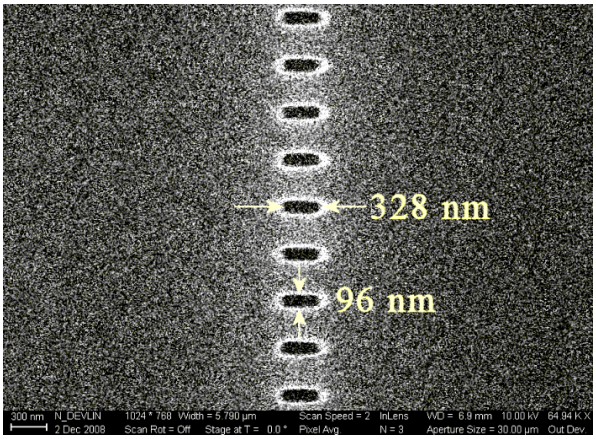


Figure 5.11. EBL finger spacing detail (step 5a).

Figure 5.12 shows the EBL-written ZEP holes that allow etching the superfluous Si away around the injector fingers.

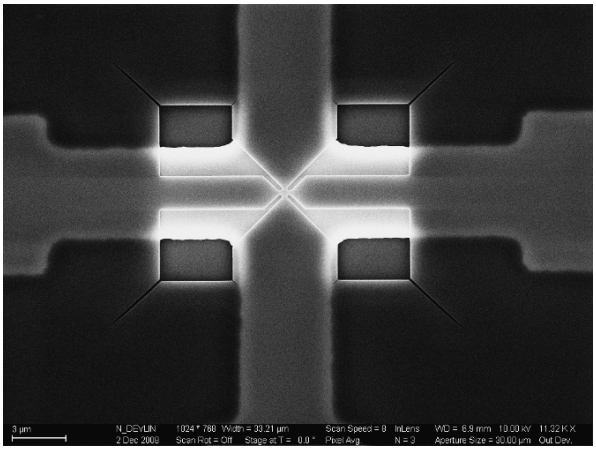


Figure 5.12. EBL injector spacing definition (step 5a).

The importance of characterizing the processing equipment to determine limitations and adapt the process accordingly can be illustrated by comparing the etch profiles of two different RIE systems.

While most oxidation and deposition steps delivered expected results, reactive ion-beam etching (RIE) on the recommended Vision Oxide RIE machine caused some uniformity and small-feature geometry etching variation problems. It was found that RIE etch rates were dramatically influenced by narrow masks and that dedicated etch and SEM cross-sectioning trial runs were necessary. Since the test designs, material and scanning electron microscope (SEM) availability were highly limited, this work had to rely on etch tests performed on a test wafer piece previously EBL-written by Devin Brown, the EBL specialist at the MiRC. Figure 5.13 shows that while the Vision Oxide RIE has an excellent etch selectivity towards Si when the ZEP EBL resist was used as a mask, its excessive horizontal etch-spread made it unsuitable for etching the 100 nm wide finger spacing slits.

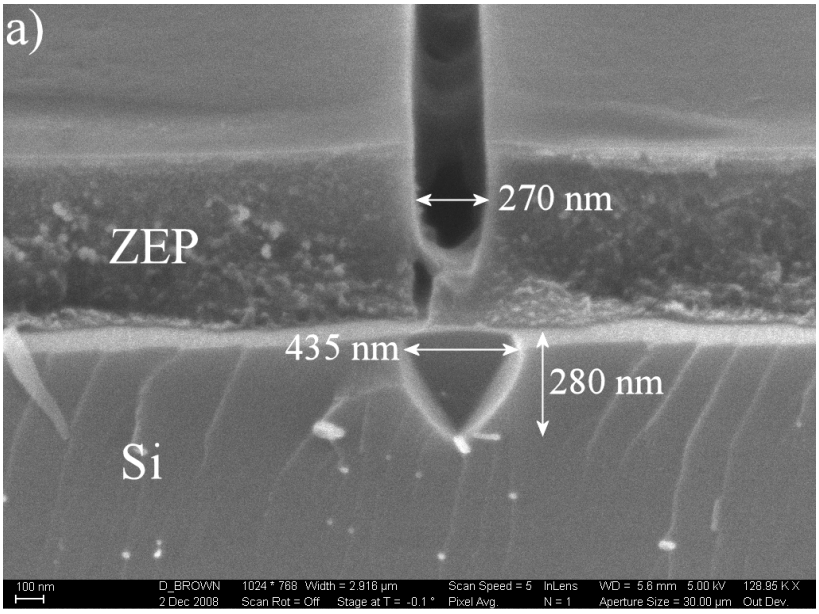


Figure 5.13. 100 nm Vision Oxide RIE Si groove etch test.

The Vision Oxide RIE is therefore not suitable for etching the 100 nm finger spacing slits into the Si since the resultant isotropic chemical etch width of up to 458 nm would completely remove the Si fingers. For this reason, the Plasmatherm ICP RIE, which was not included in the equipment training-program and was consequently not characterized extensively, had to be used.

Figure 5.14 shows that the PlasmaTherm ICP, which was eventually used for the finger spacing etching, exhibited a very narrow etch profile, but suffered from a relatively poor etch selectivity of only about 0.3.

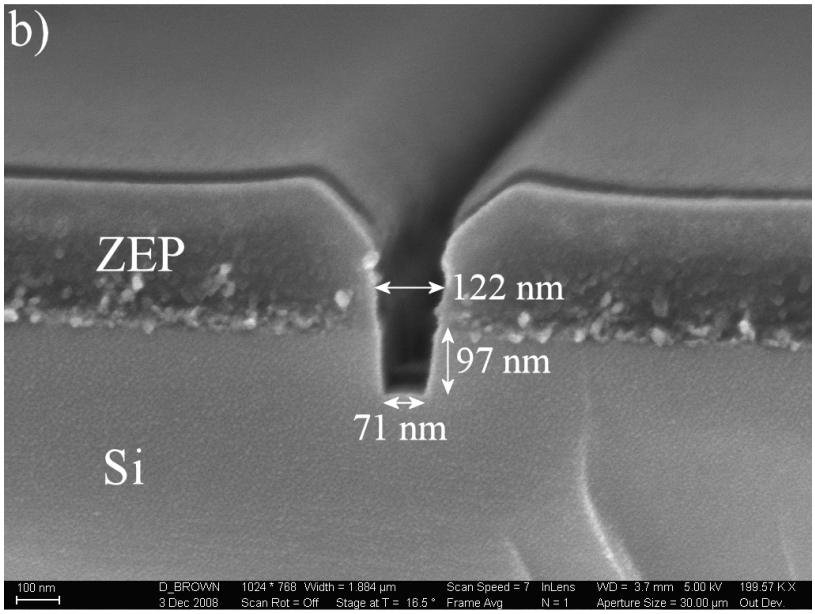


Figure 5.14. 100 nm ICP groove etch test.

The ICP could etch the 100 nm wide lines in the ZEP into about 71 nm wide and 97 nm deep grooves into the Si in 80 sec.

Figure 5.14 also shows the bad ICP etch selectivity of about 0.3. The etch selectivity is calculated as the etch rate ratio of desired material (in this case Si) to mask (in this case ZEP). The Plasmatherm ICP etched Si at an average rate of R_{Si} = 97 nm/80 sec = 73 nm/Min while removing the ZEP at the surface and sidewalls with an average rate of R_{ZEP} = (600 nm – 322 nm)/80 sec = 209 nm/Min. The ICP etch selectivity therefore is $R_{Si}/R_{ZEP} \approx 0.3$. Since the test-material used in above experiments had slightly different characteristics compared to the used wafers and the Plasmatherm ICP had a very low etch selectivity a best estimate etch time had to be compromised upon to etch sufficient silicon without completely removing the ZEP mask. It was decided that 2 Min 46 sec would only remove 582 nm of the 600 nm thick ZEP while still etching the thickest Si island thickness of 280 nm.

Due to Si island thickness variations, the finger definition ICP etch sufficiently formed all fingers but unfortunately the material around the injection devices was not completely removed before the ZEP EBL resist was also completely removed (see Figure 5.22).

The SEM image in Figure 5.15 shows the finger spacing holes ICP-etched into the Si that remained once the ZEP EBL resist was de-scummed after the finger definition RIE (before thinning oxidation).

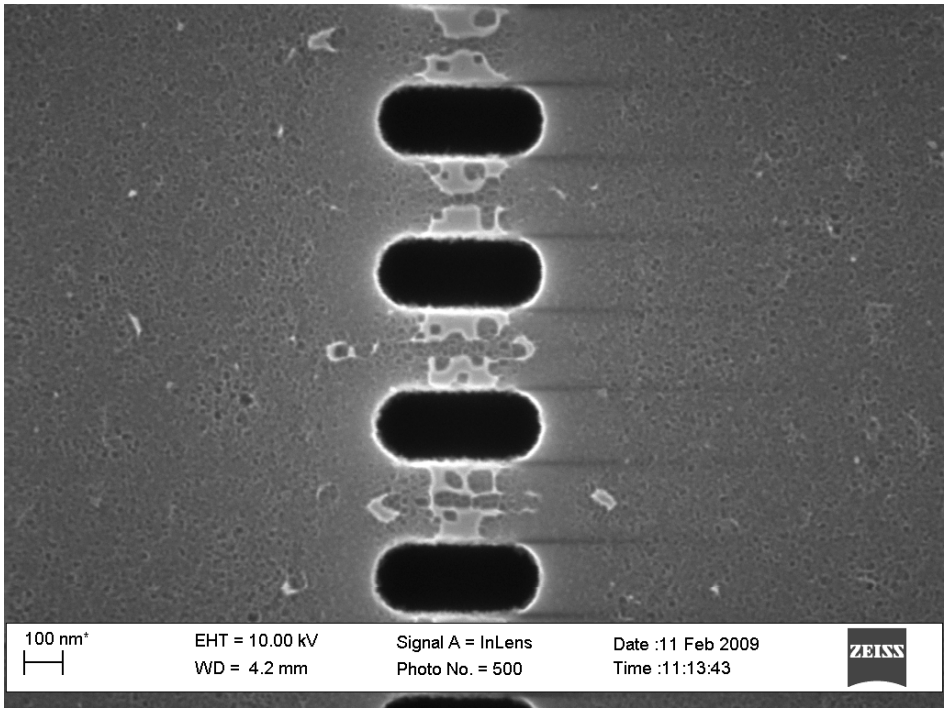


Figure 5.15. Finger spacing holes in the about 117 nm thick Si after RIE.

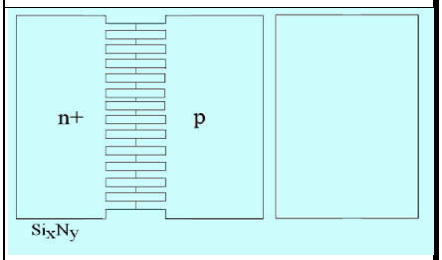
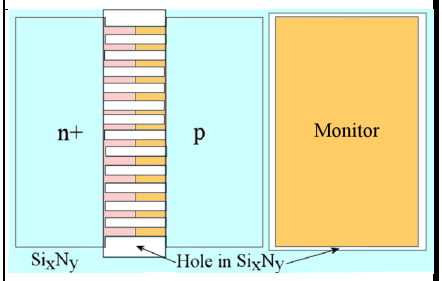
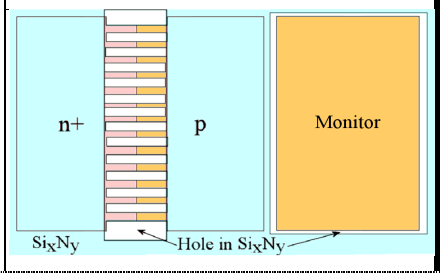
The device imaged above becomes a punch-through light source on wafer *S3*, cluster 1, *Chip 2*.

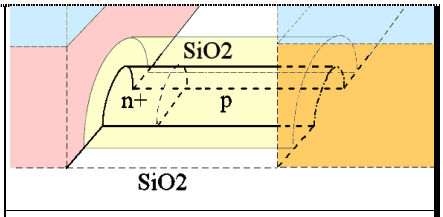
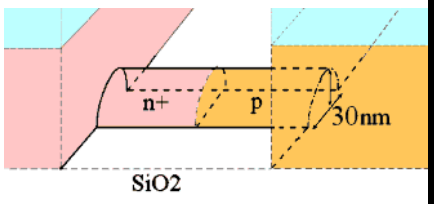
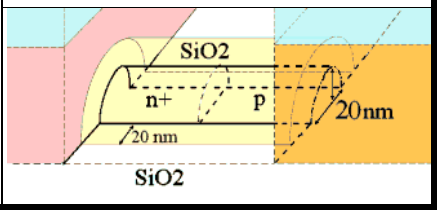
Although the EBL exposure and PlasmaTherm ICP etch resulted in rounded corners of the holes this is not critical to the junctions in the fingers.

5.6. Finger Thinning Oxidation

In the finger thinning oxidation processing steps in Table 5.11, the wafer was covered with a Si_xN_y masking layer. Oxidation windows were then etched into the Si_xN_y through which the Si fingers could be selectively oxidized thinner.

Table 5.11. Finger thinning oxidation process flow.

Step	Action	Equipment	Material	Facility	Graphical representation
6a	EBL data preparation	UNIX workstation	GDS data file	MiRC	
6b	Si_xN_y deposition Prior SiO_2 for adhesion 81 nm: 9 Min 52 s (Addendum D.3)	Unaxis PECVD	Chlorinated silane NH_3 Control pieces		
6c	PR application t_{SC1813} > 54 nm	Spinner	SC1813		
6d	Photolithography (see steps 3c to 3g)	Mask aligner	*Oxidation* photo-mask		
6e	Nitride etch 1 Min 6 s	Vision RIE	-		
6f	PR removal & wafer clean	Wet-bench	Piranha		
6g	Measure Si finger Width & height	Profilometer	-		
6h	Measure $w_{SiFinger}$	SEM	-		
6i	EBL (see steps 4b to 4h)	JEOL EPG	*Oxidation* EBL- file		
6j	Nitride etch 1 Min 20 s	Vision RIE	-		
6k	ZEP descum				

6l	Dry Si oxidation 27 Min @ 970 ºC $t_{SiO2} \approx 63$ nm; $\Delta t_{Si} \approx 28$ nm	Furnace	H_2O	CEFIM	
6m	Remove SiO_2 100 nm/Min (Addendum D.2)	Fume hood	BOE		
6n	Measure $w_{SiFinger}$ deduce $h_{SiFinger}$	SEM	-		
Repeat steps 6l to 6n until $h_{SiFinger} = w_{SiFinger} \sim 30$ nm					
6o	Dry Si oxidation 1 h 2 Min @ 970 ºC $h_{SiFinger} = 20$ nm $t_{SiO2} \approx 95$ nm	Furnace	O_2		

The thinning oxidation process parameters were determined with the help of the theory described in section 2.3.1 and the collected oxidation characterization data in Figure D.3.

Since the Si_xN_y mask deposited in step 6b will be the final passivation layer on light sources that are not oxidation-thinned, the thickness of the Si_xN_y layer can be set for maximum light transmission from the Si light source through the Si_xN_y into the air above. Employing the light transmission model derived in section 2.2.3.2, Figure 5.16 shows that maximum silicon-Si_xN_y-air light transmission for λ = 650 nm is achieved with a Si_xN_y thickness of 81 nm.

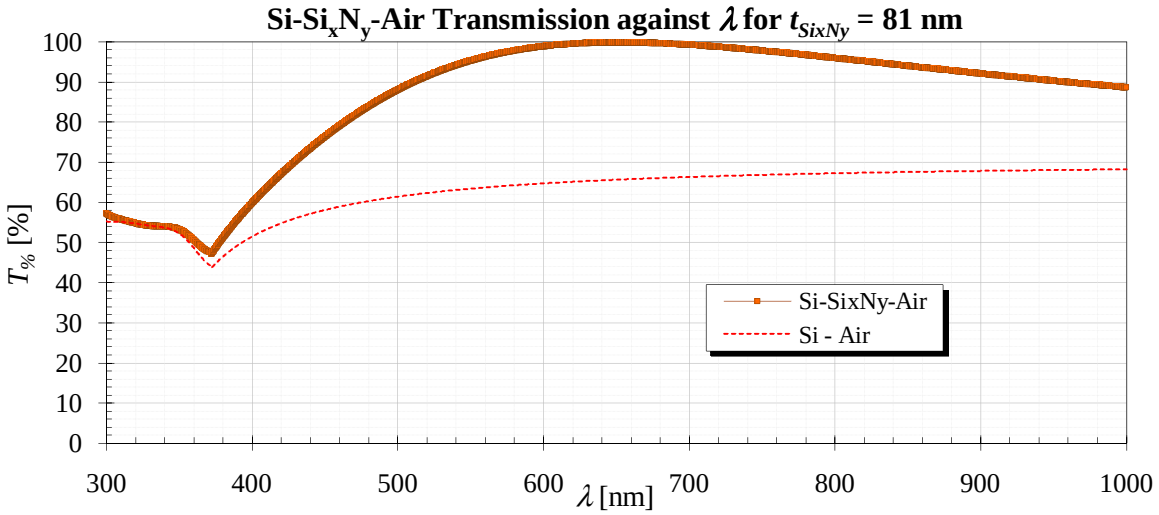


Figure 5.16. Si-Si_xN_y-air transmission at t_{SixNy} = 81 nm.

Figure 5.17 shows that the maximum overall silicon-Si_xN_y-air light transmission for 300 nm $\leq \lambda \leq$ 1 µm is realized with a Si_xN_y thickness of about 65 nm.

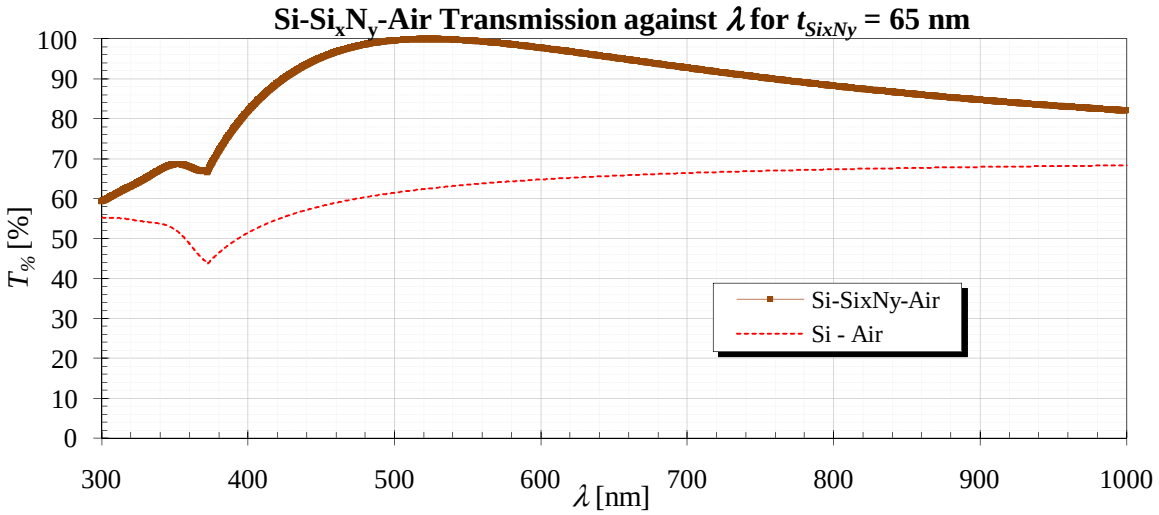


Figure 5.17. Si-Si_xN_y-air transmission at t_{SixNy} = 65 nm.

For maximum external light emission efficiency, the PECVD-deposited Si_xN_y thickness should therefore be between 65 and 81 nm. As described in section 2.2.3.2 adding a SiO_2 or Si_xN_y layer with refractive index between Si and air improves the light transmission over the Si-air interface transmission shown as a dotted line in Figure 5.16 and Figure 5.17.

Figure 5.18 shows the oxidation windows in the nitride over the wide 1D-confined Si fingers created through photolithography after step 6e.

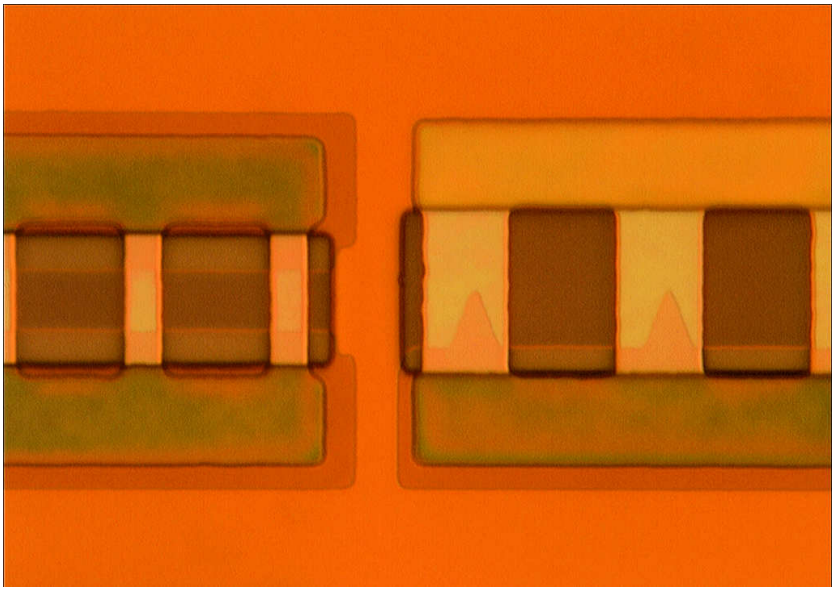


Figure 5.18. 1D-confined devices after finger oxidation (photo) RIE (step 6e).

The Si_xN_y oxidation window is visible as a darker box spreading across the fingers.

The SEM photo in Figure 5.19 shows the EBL-written oxidation windows in the Si_xN_y covering the Si finger devices as white lines in the top row and two top-most devices in the right row.

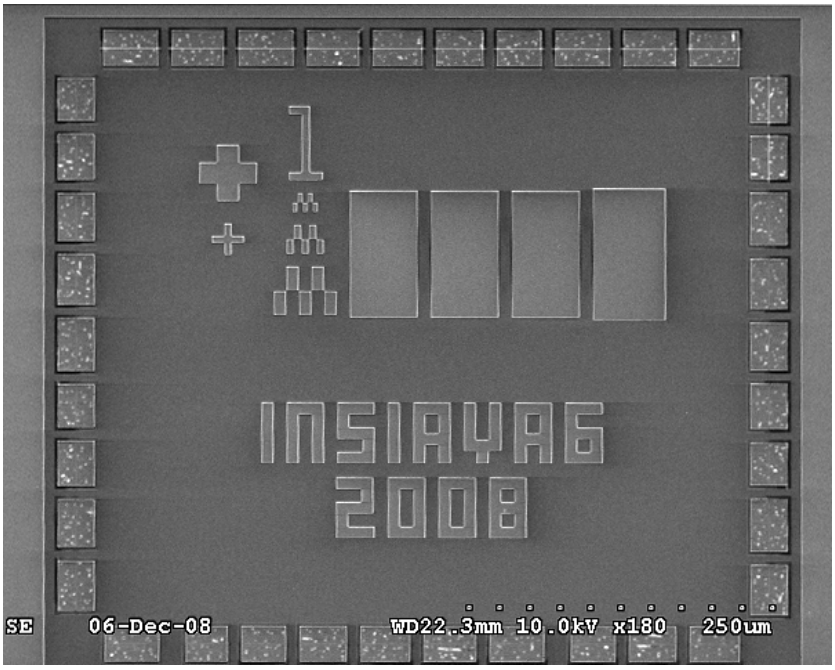


Figure 5.19. *Chip2* after oxidation EBL de-scum (step 6k).

The SEM image in Figure 5.20 shows the finger oxidation window overlaying the Si fingers (before thinning oxidation) as a bright horizontal band.

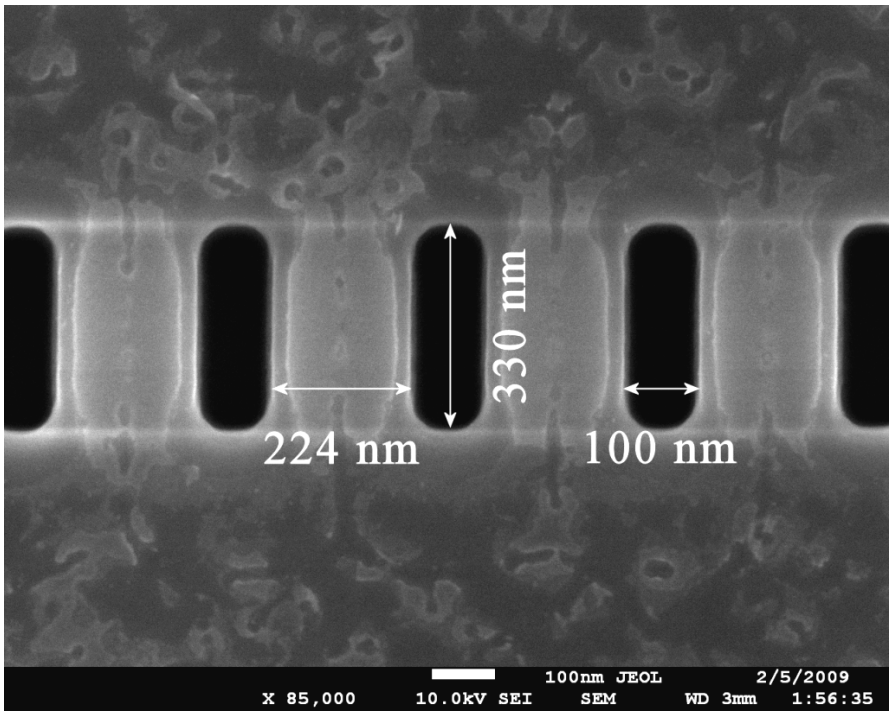


Figure 5.20. Oxidation window opening over the approximately 117 nm thick Si fingers.

The device imaged above is a punch-through light source on wafer *S8*, cluster 1, *Chip 2*, and was designed to have Si finger spacing slits 340 nm long, 100 nm wide and 260 nm apart. Although the EBL exposure and PlasmaTherm ICP etch resulted in rounded corners of the Si finger spacing holes, the dimensions of the holes are acceptably close to the layout dimensions.

Although all EBL exposures were completed, it was found that the last EBL exposure introduced a 50-µm alignment and exposure shift that resulted in the injection devices not obtaining oxidation-thinning windows at the correct locations (Figure 5.21 and Figure 5.22). The avalanche and punch-through finger junction SOI light sources obtained the correct oxidation-thinning window EBL exposure.

Figure 5.21 shows where the JEOL EPG scanned a transition to a Si monitor island instead of the alignment marker cross.

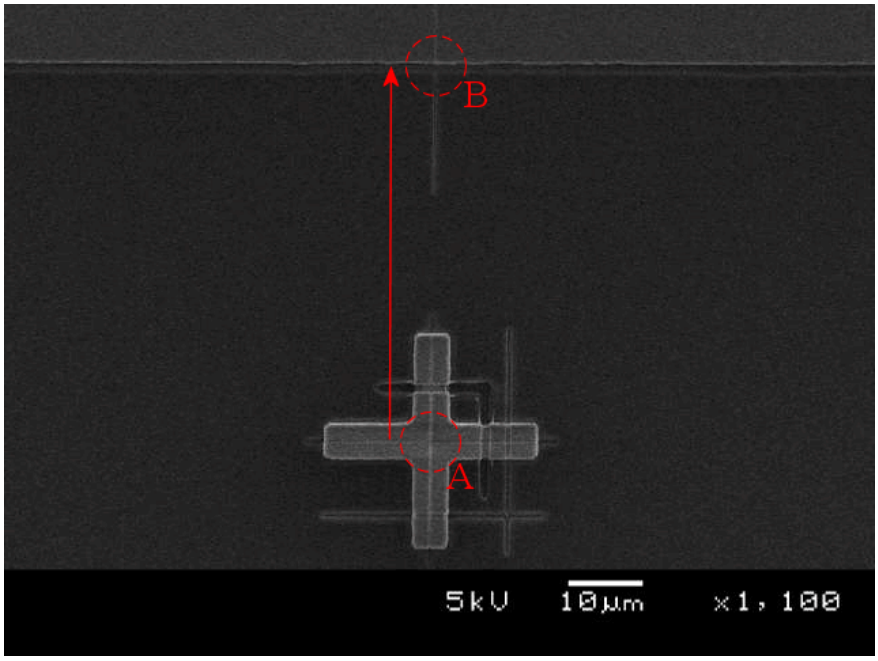


Figure 5.21. EPG scanning the wrong vertical edge causing misalignment.

This resulted in a 50 µm vertical offset of all oxidation windows over the injection-enhanced SOI light sources in *Chip3* and *Chip4* as shown in Figure 5.22

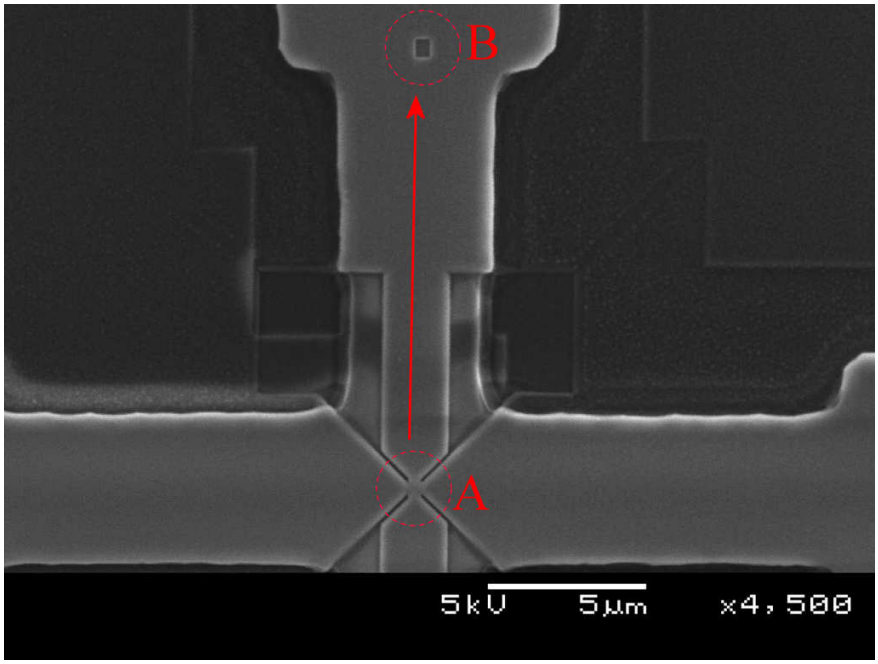


Figure 5.22. EBL oxidation window 50 µm vertical shift.

This meant that although the injection devices should still be functional, the effect of confining the dimensions of the injection region through oxidation could not be investigated anymore.

Since the SiO_2 grown on the fingers during the last thinning oxidation is usable as an anti-reflection layer between the Si finger and the air around it, the last SiO_2 layer thickness can be chosen to maximize the light transmission from the light source into the air above it. Figure 5.23 shows that maximum silicon-SiO_2-air light transmission for λ = 650 nm is achieved with a SiO_2 thickness of 112 nm.

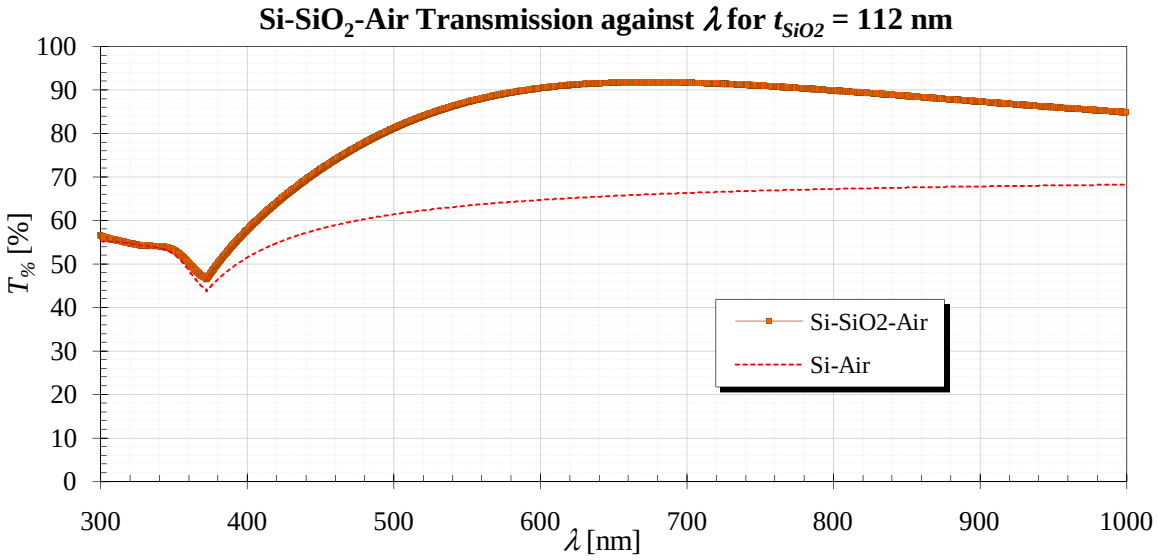


Figure 5.23. Si-SiO_2-Air transmission at t_{SiO2} = 112 nm.

Figure 5.24 shows that the maximum silicon-SiO_2-air light transmission for 300 nm $\leq \lambda \leq$ 1 µm is achieved with a SiO_2 thickness of about 65 nm.

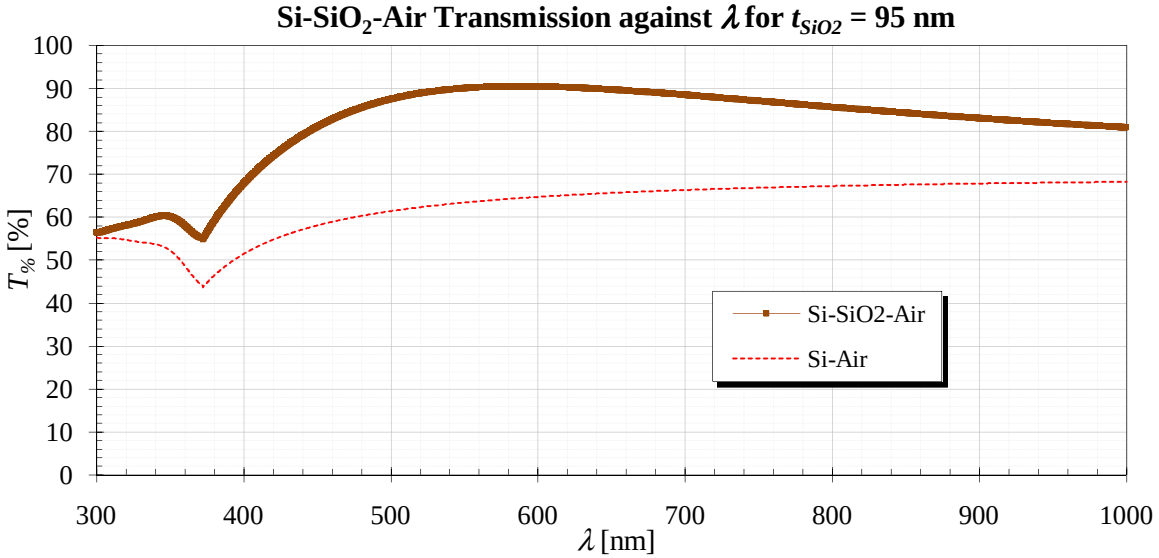


Figure 5.24. Si-SiO_2-Air transmission at t_{SiO2} = 95 nm.

For maximum external light emission efficiency, the PECVD-deposited SiO_2 thickness should therefore be between 95 and 112 nm.

The finger oxidation steps 6l and 6o were done in one of the oxidation furnaces in the clean-room of the CEFIM while the Zeiss Ultra SEM in the Centre for Microanalysis and Microscopy at UP was used to monitor the Si finger width reduction and deduce finger thickness.

Since the thinning oxidation and resultant Si finger dimensions were quite critical care was taken to slowly approach the desired finger thickness and width of around 20 nm without causing too much impurity redistribution, but still obtaining desired optical properties.

In spite of careful oxidation, it was found that many fingers were destroyed by mechanical stress that pulled the thin Si fingers apart. This is thought to have been caused by slightly differing expansion coefficients of the SiO_2 BOX and the Si on top of the BOX.

Figure 5.25 depicts three examples of final SOI finger junction dimensions achieved after the finger thinning oxidation.

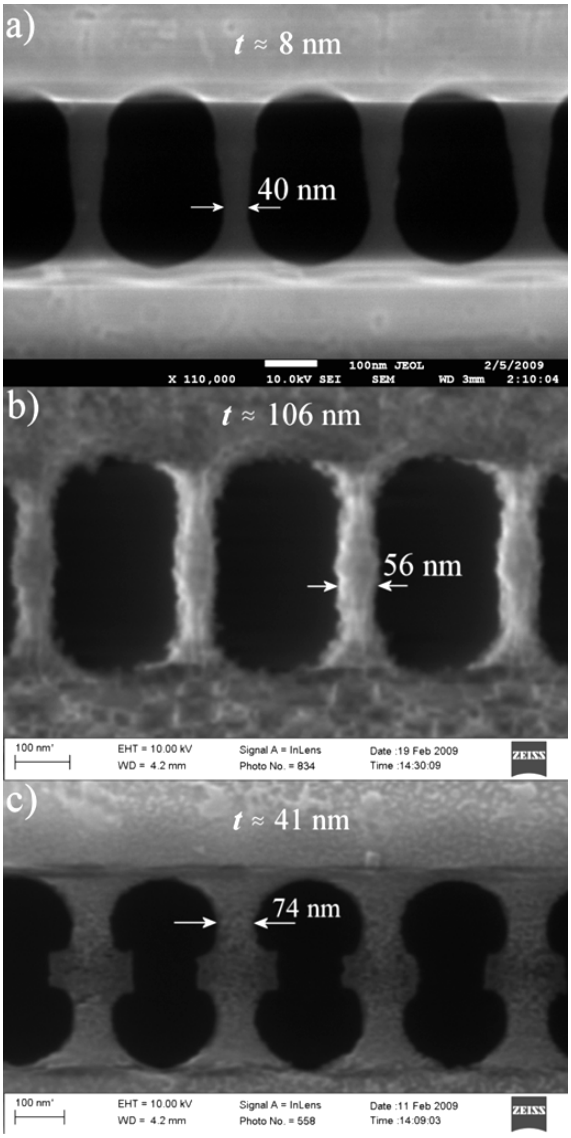


Figure 5.25. a), b) avalanche and c) punch-through SOI finger dimensions after thinning oxidation.

The Si finger thicknesses indicated in above images are estimates interpolated from reflective spectrometer measurements of the oxidation monitor islands. In contrast to the broad, but thin fingers in Figure 5.25 a), the fingers in Figure 5.25 b) are more thick than narrow.

The punch-through SOI light source in Figure 5.25 c) clearly shows how the heavily As doped Si oxidized faster than the lightly B-doped background (see subsection 2.3.2). This oxidation effect created a drift and recombination region that is slightly larger than the heavily doped contact region, which should result in higher useful light emission from the light sources since less light is lost due to internal reflection along the finger axis.

Table 5.12 shows the laid-out and final measured SOI finger dimensions.

Table 5.12. Achieved final SOI finger dimensions

Dimension	**Layout** [nm]	**Measured** [nm]
l_J	230	296 – 359
w_J	200, 220, 240, 260, 280, 300	38 – 101
l_{PT}	320, 330, 340, 350, 360, 370, 380, 390, 400	348 – 502
w_{PT}	220, 260, 300	30 – 210
s_S	50, 90, 130	Not measured
w_S	200, 260, 300	Not measured
s_O	120, 160, 200	Not measured
w_O	200, 260, 300	Not measured

5.7. Metallization

The successfulness of the wafer manufacture process could only be tested once the metallization allows electrical contact to the implemented devices.

It was initially planned to perform the metallization also at the MiRC, but since it was possible to sputter-deposit the Aluminium conductor onto the wafers by sending the wafers to Elume Inc[4]. in California, the micrometre-scale metal was chemically etched in the clean-room of the CEFIM at UP.

[4] ELume, Inc., Microchip Foundry, 587 N. Ventu Park Rd., Newbury Park, California 91320

Table 5.13. Metallization process flow.

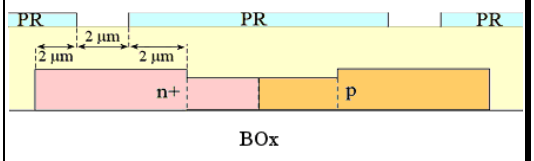
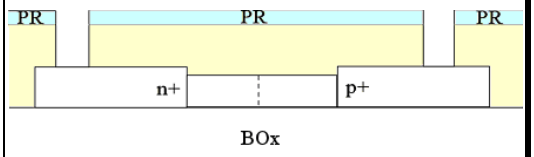
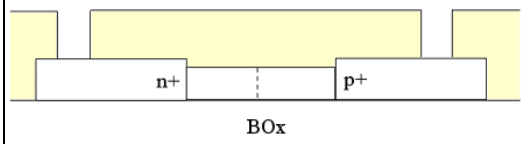
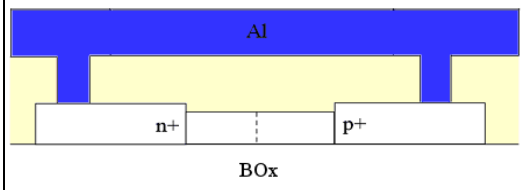
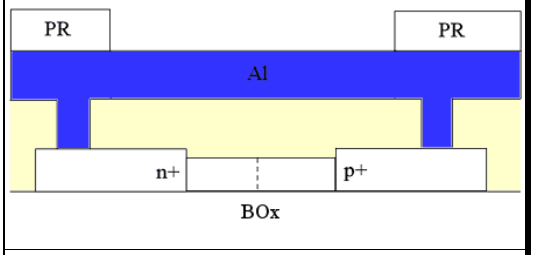
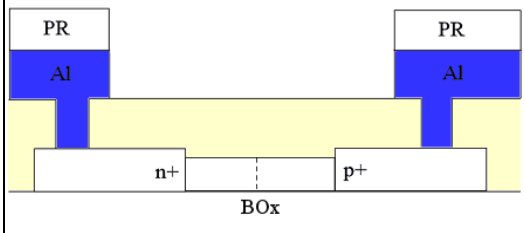
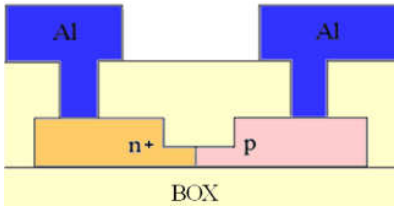
Step	Action	Equipment	Material	Facility	Graphical representation
7b	Photolithography (see steps 3c to 3g)	Karl Süss mask aligner	*Co* photo-mask SC1813	CEFIM	
7c	SiO_2 etch (Addendum D.2)	Wet-bench	BOE		
7d	Remove PR		Fuming Nitric Acid		
7e	Wafer clean	Spin-dryer	H_2O		
7f	Metallization 1 µm Al	Sputterer	Al	Elume	
7g	Pattern PR (see steps 3c to 3g)	Karl Süss mask aligner	*Metal* photo-mask SC1813	CEFIM	
7h	Al etch	Wet-bench	Al etch, BOE		
7i	Remove PR		Acetone,		
7j	Wafer clean No Acid (Metal)	Spin-dryer	H_2O		
7k	Al anneal 500 C 30 Min	Furnace	H_2N_2 forming gas		

Figure 5.26 to Figure 5.29 depict microphotographs of the final chips *Chip1* to *Chip4*.

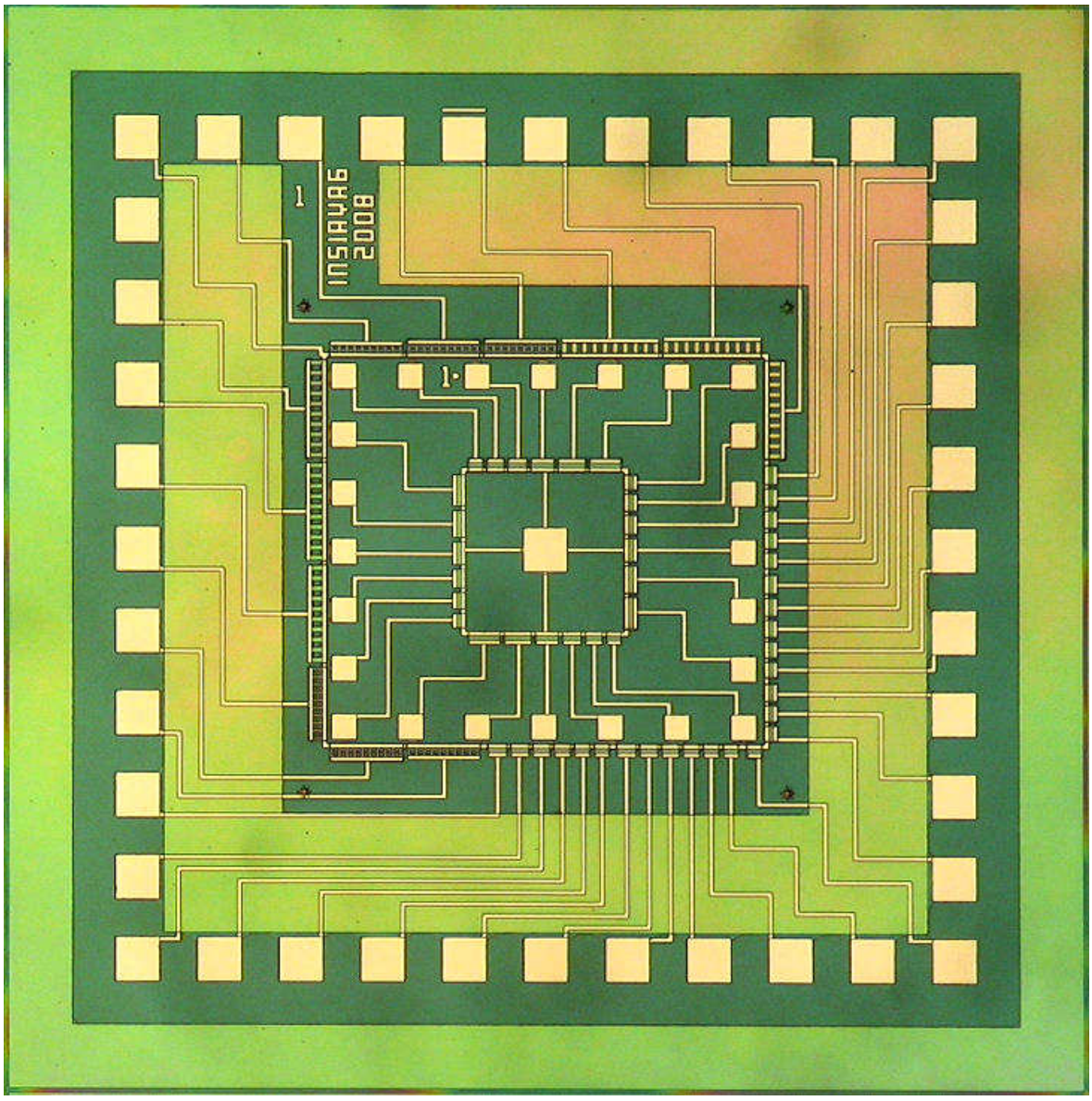


Figure 5.26. Micro-photograph of final *Chip1*.

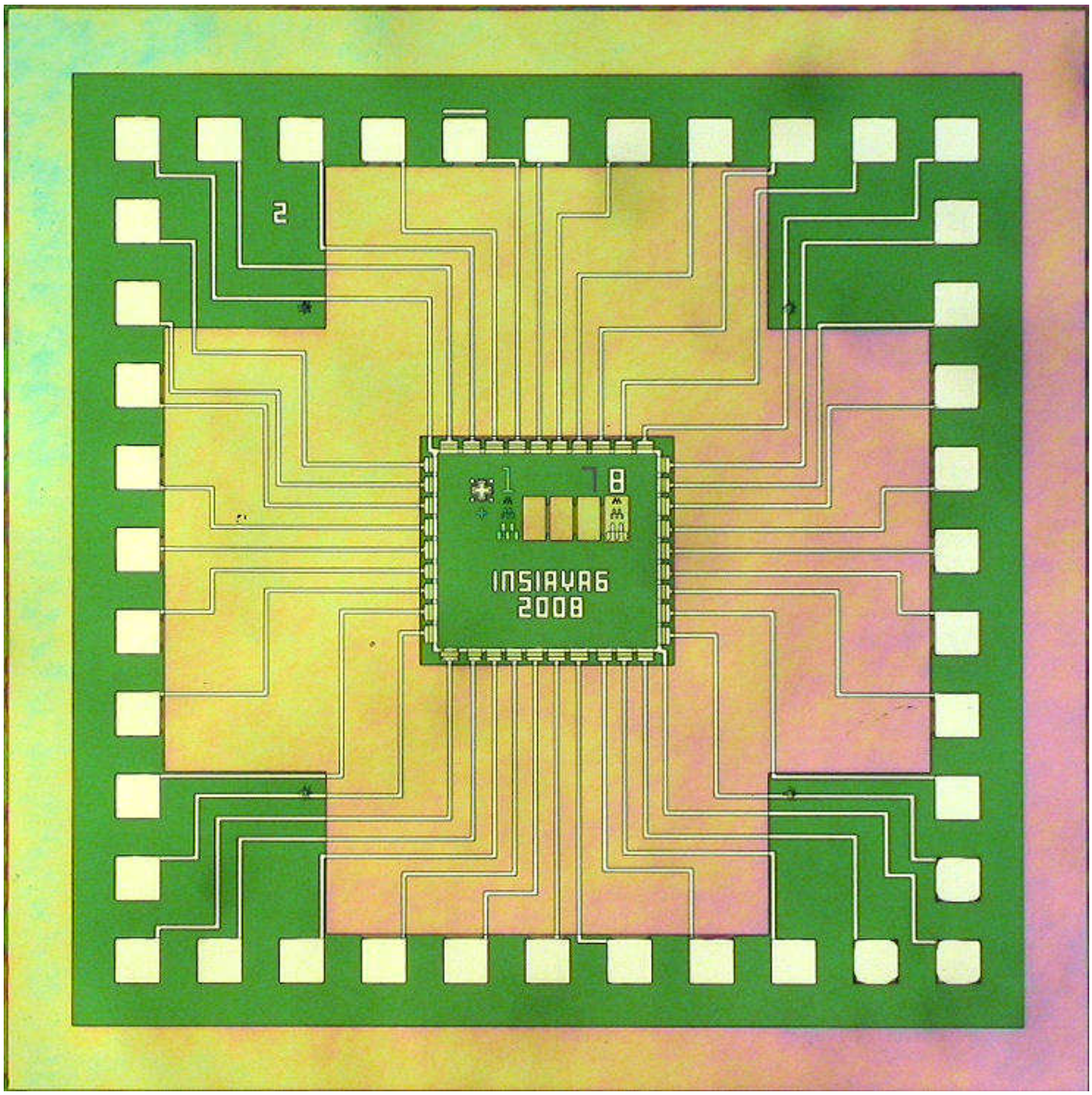


Figure 5.27. Micro-photograph of finalized *Chip2*.

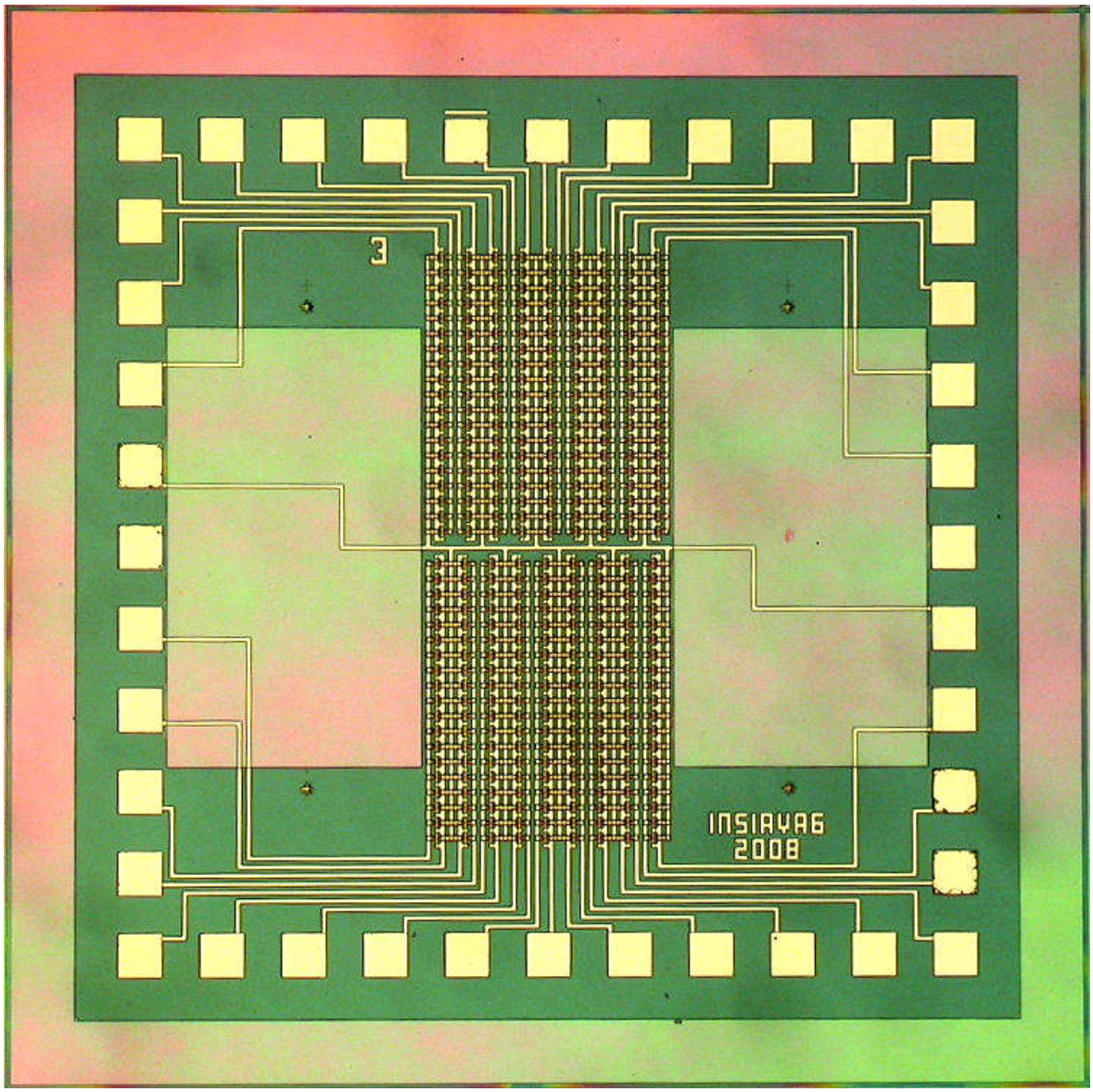


Figure 5.28. Micro-photograph of finalized *Chip3*.

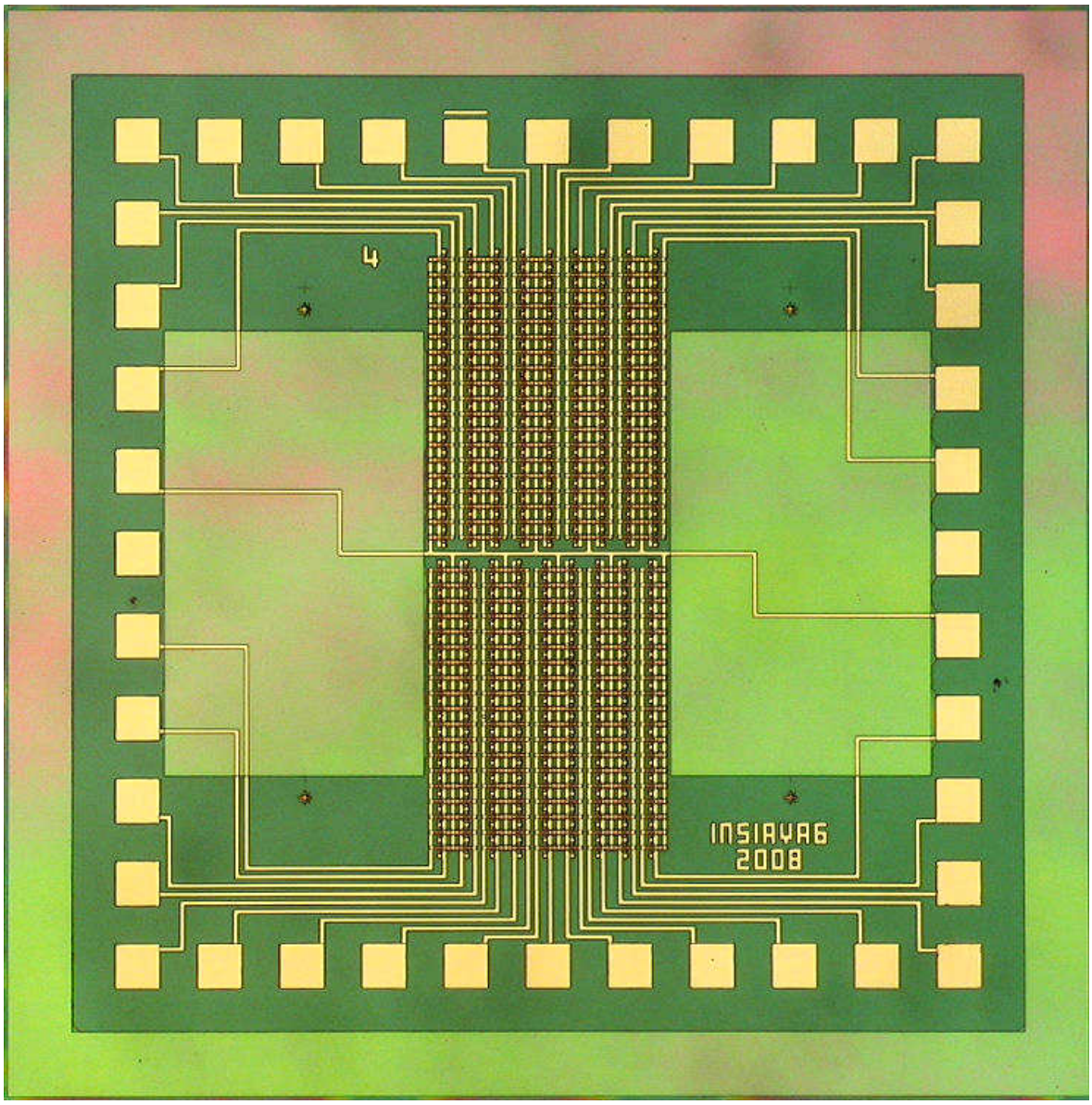


Figure 5.29. Micro-photograph of finalized *Chip4*.