Analytical Approach to Design of the Proportional-to-the-Absolute-Temperature Current Sources and Temperature Sensors Based on Heterojunction Bipolar Transistors

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***Abstract*—Embedded temperature sensors based on the proportional to the absolute temperature (PTAT) current source have a potential to lay a foundation for the low-cost temperature-aware integrated circuit (IC) architectures if they meet the requirements of miniaturisation, fabrication process match and precise estimation in a wide range of temperatures. This paper addresses an analytical approach to the minimum-element PTAT circuit design capitalising on the physics-based modelling of the heterojunction bipolar transistor (HBT) structures. It is shown that a PTAT circuit can be implemented on only two core HBT elements with a good accuracy. Derived parametric relations allow a straightforward specification of the thermal gain at the design stage that affects sensor sensitivity. Further derived current-to-temperature mapping expresses a temperature estimate based on the measured PTAT output current. Numerical examples indicate attainable estimation accuracy of 0.43 % in case of a measurement instance taken in the absence of measurement noise.**

***Index Terms*—BiCMOS integrated circuits, heterojunction bipolar transistors, temperature measurement**

I. Introduction

Real-time management of the temperature and the electrothermal effects has become an important concern for modern integrated circuits (ICs) characterised by the ultra-large scale of the number of circuit elements per silicon unit area, 3D packaging structures, etc. Temperature represents a non-linear function of time and the location on the die. It depends on both the ambient and the intra-circuit power dissipation that leads to emergence of strong hotspots at certain IC nodes where the power density is high [1]. Embedded temperature sensors and thermal compensation circuits are seen as one of the essential means to realise low-cost temperature-aware IC architectures with the built-in self-test (BIST) and runtime configuration capabilities. Information of the temperature distribution at tests helps to accomplish the physical design. Digital control means based on the electrothermal models enhance circuit performance and reliability.

Creation of a simple, miniature, power-efficient and process-matched on-chip temperature sensor calls for development of an accurate electrothermal model for a *system of transistor elements* constituting the sensor circuit. The simplicity requirement boils down to dc measurements preference to reduce complexity of the measurement setup and to ease integration. The two common approaches to the embedded sensor design capitalise on differential transducers and the proportional to the absolute temperature (*PTAT*) current sources [2]. The differential schemes are known for their sensitivity to the temperature variations across the IC surface. A number of recent works consider differential transducer implementations based on at least three bipolar junction transistors (BJTs) [3]-[5]. This class of sensors lacks unification due to their dependence on the corresponding IC area layout (and location of the hotspots relative to the transducers). The PTAT current sources represent highly integrated combinations of BJTs [6]-[8] or field effect transistors (FETs) [9]-[12], the output current of which is proportional to the absolute temperature at the sensing element location. A related but less common temperature measurement principle was reported in [13] where PTAT forward voltage drop was measured across a Schottky diode. FET-based sensor circuit variants are more wide spread due to the CMOS process standardisation, lower power consumption and self-heating avoidance, though their PTAT accuracy might be inferior in comparison with the BJT-based design. The core of the classic PTAT source consists of two transistors with distinct transconductance nominals (achieved by using different-size emitter areas in case of BJTs). Having different physical structures, the transistors are likely to be susceptible to the process variations and mismatching thermal trends of all main parameters that limits output precision against design expectations. This is exacerbated by a reliance of the sensing circuit theory on the over-simplified electrothermal models of the component transistors which are a poor match to the existing fabrication processes. Finally, both PTAT and differential sensors are traditionally powered by a constant current source, leaving out the voltage supply option

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discussions in most works on the topic.

This work is dedicated to modelling of the heterojunction bipolar transistor (*HBT*) based PTAT current source circuits in a wide range of operating temperatures (in contrast to relatively small temperature ranges reported). The principal difference from other related findings reported in the literature is adoption of the realistic physics-based HBT model – high current model (HICUM) [14]. This model features BiCMOS-inherent scale current and transconductance variation with temperature and addresses the self-heating effect which leads to thermal instability and breakdown at high current densities [15]. The biasing scheme design is closely related to the electrothermal model of the transistor. The work deduces PTAT circuits of a simple, minimum-element structure to serve as a temperature sensor core. It presents recommendations and closed-form analytical relations describing the parameter selection to yield temperature estimates based on the PTAT output measurements that is supposed to be followed by the analogue-to-digital conversion for post-processing. As the emphasis is on analytical modelling versus a complete sensor circuit design, the performance metrics feature modelling precision error rather than the commonly adopted sensor sensitivity.

The paper is organised as follows. Section II describes a PTAT output current law in a general formulation. Section III highlights theoretical specifics of the temperature-domain HBT modelling accompanied by an illustrative example. Section IV deals with derivations of the analytical relations which serve for the electrothermal characteristics prediction. A closed-form mapping from the measured voltage/current in the load to the corresponding temperature estimate is solicited. Section V presents several numerical examples with the aim to benchmark the proposed analytical electrothermal relations versus a comprehensive circuit model simulation.

II. General PTAT Definition

A traditional approach to the PTAT current mirror design is the underlying Widlar current mirror (CM) circuit architecture in which output current gain variation with temperature can be controlled by choosing an emitter degeneration resistance nominal in the mirroring current branch [16]. Depending on the element transistor properties and the essence of the power supply (biasing current or voltage) for the CM circuit, the skew of the output temperature-current characteristic may exhibit nonlinearities at different sections. This work considers a mathematical detail of the parametric reasons behind nonlinearities in the thermal dependence of the output current. An important CM design consideration is that the transistors are placed close enough to each other on the die so that they share the same temperature, i.e. they are thermally matched due to the integration.

A broader Widlar CM schematic specifies the common circuit elements as in Fig.1 (*npn* bipolar transistor based variant). The design of the circuit relies on the fact that the transistor Q1 (master, or driving transistor) and the transistor Q2 (slave, or mirroring transistor) are selected to have matched characteristics (realistic parametric descriptions of the device models applicable to different scenarios will be detailed in Sections III and IV). The output current notation is a function of the voltage difference across the transistors:

$$I_{OUT} = I_{C2} \approx (V_{BE1} - V_{BE2}) / R_E \,, \tag{1}$$

where V_{BEk} denotes the voltage across the BE junction of the kth transistor, and R_E is the emitter degeneration resistor in the Q2 branch, the nominal of which stays invariant (or approximately invariant) in the temperature range of interest (a package and layout engineering task).

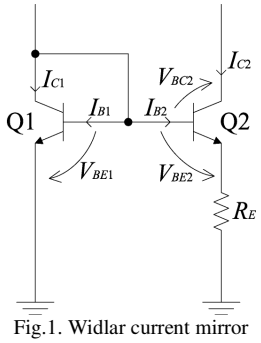


Fig.1. Widlar current mirror

Equation (1) is accurate with exception of the current through the base-emitter (BE) junction of Q2 since it is much (at least several magnitude orders) smaller than the transfer current I_{C2} forming the collector output. The classic theory of the bipolar transistor devices deals with collector current dependence on the biasing voltage through the proportionality of I_{Ck} to the exponential term $\exp(\eta V_{BEk}/V_T)$ which also contains the thermal voltage V_T and the nonideality factor η (usually a technology-specific parameter). The thermal voltage is known by the expression:

$$V_T = k_B T / q_e \,, \tag{2}$$

where $k_B = 1.38 \cdot 10^{-23}$ J/K, $q_e = 1.602 \cdot 10^{-19}$ C, and T is the temperature of the transistor that is affected by the ambient material temperature and the internal power dissipation observed across the transistor junctions.

Assumption of the equality between the matched (equal or strictly proportional) transistor parameters in a wide temperature range would advocate a classic thermal proportionality formula obtained from (1) by the substitution of $V_{BE1} - V_{BE2} = \eta^{-1} V_T \ln(I_{C1}/I_{C2})$ that has historically been used for the PTAT design description [8]:

$$I_{out} = \left(\frac{k_B}{\eta q_e R_E} \ln \frac{I_{C1}}{I_{C2}} \right) T \,. \tag{3}$$

Equation (3) would represent an ideal law of the output current proportionality to the temperature under the condition of the ratio I_{C1}/I_{C2} being constant across a wide range of temperatures. However, I_{C1}/I_{C2} is a nonlinear characteristic

in temperature and is also technology-dependent. The non-existence of the exact solution of (3) for I_{C2} in a strict sense makes the temperature range uncertainty and the technology-dependent factor devalue the empirical results of simulations and experimental tests (as each technology would define a different thermal nonlinearity for I_{C1}/I_{C2}).

Invention of the realistic physics-based transistor models has introduced a potential opportunity to find a closed-form unified expression for the PTAT current source output for a selected transistor technology. In the following description, a HICUM used for the HBT performance prediction will be scrutinised with the aim to describe the PTAT outputs in a wide range of temperatures.

III. Thermal-Domain HBT Description Based on HICUM/L0

A. HICUM/L0 Theoretical Background

The standard HICUM model of Level 0 or Level 2 details a method for computation of the Gummel characteristics for a bipolar or a HBT, given the set of fixed technology-specific parameters obtained by the parameter extraction procedures. This section emphasises description of the model part dealing with temperature dependences which influence the collector output (transfer) current and hence should be taken into account in the derivation of the CM currents.

The equivalent HICUM/L0 large-signal circuit diagram featuring the physics based vertical *npn* transistor description is shown in Fig.2. The HICUM Level 0 model is positioned as a variant of the comprehensive physics-based HBT HICUM Level 2 model that is lighter in the computational sense due to the use of an approximation in the high currents region of operation instead of an iterative solution of the charge control [17]. The presented model is scrutinised only in the context of the CM design, hence it omits the signal elements governing operating regimes other than the forward dc biasing of Q1 and Q2, namely the parasitic capacitances, tunnelling and avalanche effect included in the full HICUM/L2 description [18]. The external emitter, collector and base resistances are excluded from the consideration to simplify the analysis. It is assumed that these resistances can be made least thermally dependent in the temperature range of interest. Using the design method with the average-in-temperature resistance absorption, it is possible to neutralise these parasitic interconnect resistances, which are known to be quiescent point independent, by the source reference load connected in series. The internal base resistance, which is dependent on the carrier mobility in the neutral base region, is taken into account in the benchmarked simulation model, though it has a minor impact on the output current and hence does not partake in the closed-form temperature estimate derivations (in which it is assumed that $V_{BE_i} \approx V_{BE}$). The specifics of the HICUM are such that the influence of the internal collector resistance is taken into account by the model equations for the transfer current and is implicitly incorporated in the derivation process.

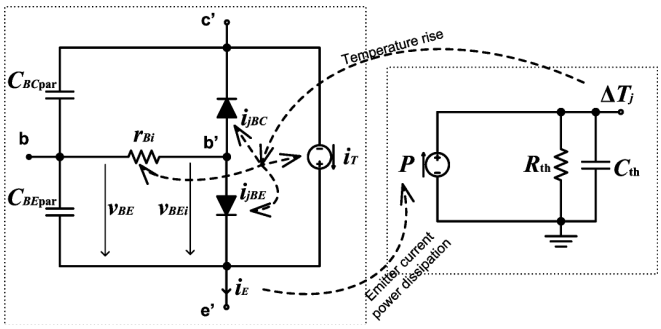


Fig.2. Equivalent HICUM/L0 large-signal circuit for the PTAT analysis: the self-heating effect due to the power dissipation across the BE junction is simulated as an iterative feedback

Thermal dependence of the main parameters in the HICUM is related to the physical quantities like the intrinsic charge carrier density and mobility. The intrinsic carrier density defines variation of the transfer current with temperature via the generalised integral charge-control relation's (GICCR) constant modelling function:

$$c_{10}(T) = c_{10nom}\left(\frac{T}{T_{nom}}\right)^{\zeta} \exp\left[\frac{v_{gB}}{V_T}\left(\frac{T}{T_{nom}} - 1\right)\right], \quad (4)$$

where c_{10nom} is the GICCR constant specified for the reference operating temperature T_{nom} at which most HICUM parameters are extracted (c_{10} takes the effective emitter area into account), V_{gB} is the effective base bandgap voltage extrapolated to $T = 0$ K, and $\zeta \equiv \zeta_{CT}$ is the exponent coefficient obtained via the extraction procedures that models mobility of the minority carriers in the base region.

The hole charge, another implicit parameter affecting the transfer current, has a much more complex functional dependence on temperature. Moreover, it is influenced by the voltages applied to the BE and the BC junctions (V_{BE_i} and V_{BC_i} respectively). For the sake of the analysis feasibility, V_{BC_i} impact is omitted from consideration because this dependence is very weak in case of the forward-biased CM circuit elements with the diode-connected Q1 (i.e., the BC voltage for Q1 is zero at all temperatures). Then the transport related hole charge at low-to-medium current densities (desirable thermal drift region for the quiescent point) can be represented by the sum:

$$Q_{pT} = Q_{p0} + h_{jEi}Q_{jEi} + Q_{fT}, \quad (5)$$

where Q_{p0} describes thermal dependence of the zero-bias hole charge, Q_{jEi} is the depletion charge which is stored within the BE junction and which is bias point (V_{BE_i}) dependent, h_{jEi} is the BE depletion charge weighting factor (an HBT-specific parameter) and Q_{fT} is the minority charge across the entire transistor constituting the forward transfer current that tends to

have more contribution than the hole and depletion charges at medium-to-high current densities. Given the interdependence between Q_{fT} and the transfer current under the conditions of $V_{BE_i} > 0$ and $V_{BC_i} = 0$, the bias-dependent hole charge is expressed in the form of the quadratic equation solution as

$$Q_{pT}(T) = \frac{Q_{pT,j}}{2} + \sqrt{\left(\frac{Q_{pT,j}}{2}\right)^2 + \tau_0 c_{10} \exp\left(\frac{V_{BE_i}}{m_{Cf} V_T}\right)}, \quad (6)$$

where $Q_{pT,j} = Q_{p0} + h_{jEi} Q_{jEi}$, c_{10} is given by (4), $m_{Cf} \equiv 1/\eta$ is the non-ideality factor, and the low-current forward transit time τ_0 is determined as in [19]:

$$\tau_0(T) = \tau_{0nom}[1 + \alpha_{\tau 0}(T - T_{nom}) + k_{\tau 0}(T - T_{nom})^2], \quad (7)$$

where the HICUM coefficients $\tau_{0nom} = \tau_0(T_{nom})$, $\alpha_{\tau 0}$ and $k_{\tau 0}$ are obtained via extraction.

The thermal dependence of the zero-bias hole charge, caused by the base width change with temperature, is described according to the formula:

$$Q_{p0}(T) = Q_{p0nom}[2 - (V_{DEi}(T)/V_{DEinom})^{z_{Ei}}], \quad (8)$$

where $Q_{p0nom} = Q_{p0}(T_{nom})$ is the zero-bias hole charge, $V_{DEinom} = V_{DEi}(T_{nom})$ is the diffusion voltage across the BE junction observed at the reference temperature, z_{Ei} is the internal BE grading coefficient, and

$$V_{DEi}(T) = V_{DEij}(T) + 2V_T \ln\left(0.5 + 0.5\sqrt{1 + 4\exp[-V_{DEij}(T)/V_T]}\right), \quad (9)$$

Here

$$V_{DEij}(T) = V_{DEijnom} T/T_{nom} - m_g V_T \ln(T/T_{nom}) - V_{gBE}(T/T_{nom} - 1) \quad (10)$$

is the auxiliary voltage which depends on the derived HICUM parameters: V_{gBE} - the effective BE bandgap voltage extrapolated to $T = 0$ K, m_g - the bandgap voltage coefficient, and $V_{DEijnom} = V_{DEij}(T_{nom})$.

The BE depletion charge in (6), observed at a given bias $V_{BE_i} > 0$, is described as

$$Q_{jEi}(T) = \frac{C_{jEi0nom} V_{DEinom}^{z_{Ei}}}{(1 - z_{Ei}) V_{DEi}^{z_{Ei}-1}(T)} \left[1 - \left(1 - \frac{V_{BEi}}{V_{DEi}(T)}\right)^{1 - z_{Ei}}\right], \quad (11)$$

where $C_{jEi0nom}$ is the internal BE zero-bias depletion capacitance at $T = T_{nom}$.

B. Thermal-Domain HBT Simulation Based on HICUM/L0

For convenience of the analysis scrutiny, each major model-descriptive stage outlined by equations (4)-(11) is accompanied by numerical examples of the selected technology. The numerical evaluation of the HICUM/L0 transistor model was done in accordance with the stable computation methods defined in the HICUM/L2 manual [18].

In our examples, we refer to the HICUM reference data extracted from the IBM 5HP technology node, part of which is listed in Table 1 [20]. Here only the parameters which influence the subsequently presented CM derivations are specified (short list). To see the rest of the parameter set, it is advised to refer to the HICUM/L2 manual [18].

TABLE 1
HICUM/L0 PARAMETERS EXTRACTED FOR THE IBM 5HP 0.32×16.8 μm^2 HBT STRUCTURE

Explicit parameters		Implicit parameters	
T_{nom}	298 K	m_g	4.189
c_{10nom}	$8.5\cdot10^{-31}$ A·C	V_{gBE}	1.147 V
V_{gB}	1.17 V	$V_{DEijnom}$	1 V
ζ_{CT}	3		
h_{jEi}	2		
m_{Cf}	1		
τ_{0nom}	$2.6\cdot10^{-12}$ s		
$\alpha_{\tau 0}$	$1\cdot10^{-3}$ K^{-1}		
$k_{\tau 0}$	$1\cdot10^{-5}$ K^{-2}		
Q_{p0nom}	$1.4\cdot10^{-13}$ C		
V_{DEinom}	1 V		
z_{Ei}	0.32		
$C_{jEi0nom}$	$3.5\cdot10^{-14}$ F		

The operating regions of the HBT used in the example are shown in Fig.3. Due to the specific linearity requirement to the CM output and the analytical description limitations in the PTAT circuit design, the bias-driven device (master HBT Q1) should be set to operate in the low-to-medium current region, i.e. below the critical current (I_{CK}) threshold. This is safely ensured via the choice of bias (supply current or voltage) that sets $V_{BE} < 0.95$ V for temperatures not exceeding the reference temperature T_{nom}. Fig.3 also shows sufficiency of the HICUM/L0 model choice (versus HICUM/L2) for the task of derivation of a CM operating in the PTAT mode since the HICUM/L0 accurately covers device behaviour in the medium-to-high current region while featuring realistic models of the thermal variation of transistor parameters.

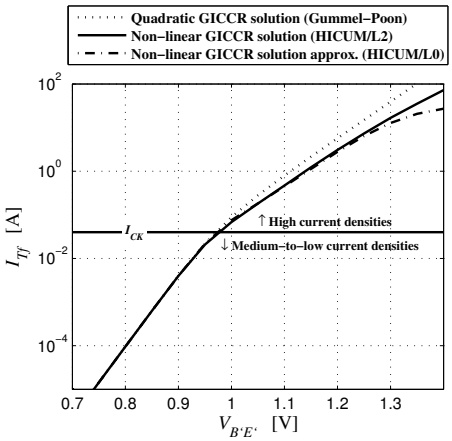


Fig.3. Transfer current regions for the IBM 5HP 0.32×16.8 μm^2 HBT (plotted for the reference temperature)

It is known that the use of HICUM is not recommended for the thermal modelling below 250 K unless the model parameters have been specifically tested for that temperature range [18]. On the other hand, 600 K is found to be the highest temperature mark available in the reported experimental data [18][21]. These figures are chosen to constitute the boundaries of the operating temperature range in the modelling presented in our work, i.e. the dynamic range of the temperature sensor under design consideration.

Fig.4 shows the Gummel plot for a variety of voltage-controlled bias settings defining operation at the low and medium current densities. It can be seen that the higher bias settings characterised by increased power dissipation may result in a destructive self-heating situation that might lead to a device breakdown. The self-heating effect becomes a problem at higher operating temperatures and particularly needs to be taken into account in the PTAT circuit design process. Fig.4 sets an upper limit on V_{BE} at the maximum temperature in the range that is for the given transistor example does not exceed 0.5-0.6 V (it will further be illustrated in the biasing scheme discussion for the CM with the constant voltage supply). In the absence of the self-heating effect, this value can be up to the medium-to-high currents threshold as in Fig.3.

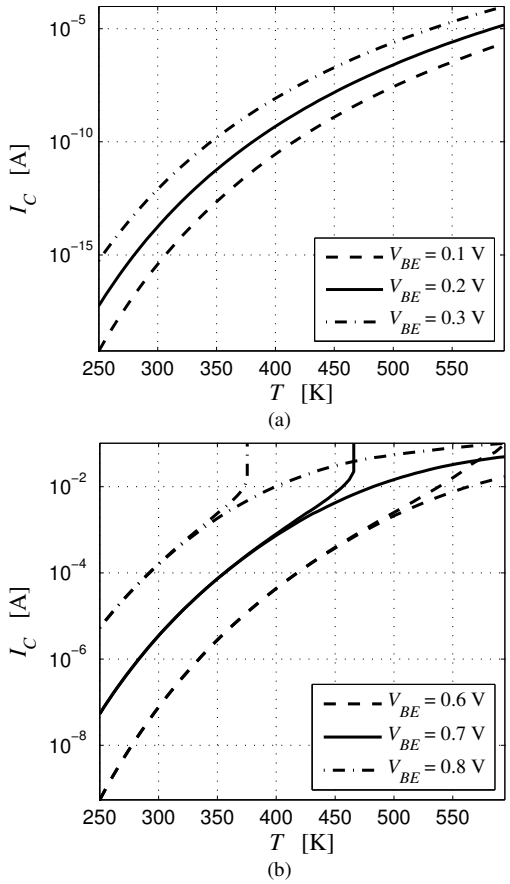


Fig.4. IBM 5HP 0.32×16.8 μm^2 HBT's collector output current at $V_{BC} = -3$ V: curve splitting at higher temperatures shows the self-heating effect (upper curve branches) versus the HICUM/L0 model with disabled self-heating (lower curve branches)

The transconductance is revealed to be a problematic parameter due to its high fluctuation in a wide temperature range. Fig.5 shows that a nearly-constant transconductance assumption is not suitable for the analysis-based PTAT circuit design and calls for accurate models to describe the current thermal variation. The BE voltage has little impact on the transconductance at the temperatures below the reference temperature (298 K). At higher temperatures the bias-induced difference becomes more pronounced. Furthermore, saturation in the transconductance thermal characteristic, followed by a breakdown as a result of the self-heating, occurs faster if the BE voltage is higher.

The $c_{10}(T)$ graph (Fig.6) shows that the thermal variation of the scale current is significant – spanning over a dozen of magnitude orders in the chosen temperature range. Hence equation (4) plays a vital role in the thermal modelling of any HBT based circuit.

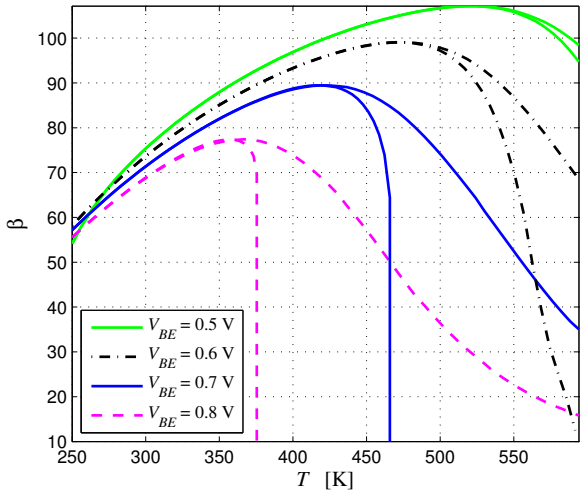


Fig.5. IBM 5HP 0.32×16.8 μm^2 HBT's transconductance variation with temperature for different BE voltage settings ($V_{BC} = -3$ V): curve splitting at higher temperatures shows the self-heating effect (lower curve branches with a steep descent) versus the model with disabled self-heating (upper curve branches)

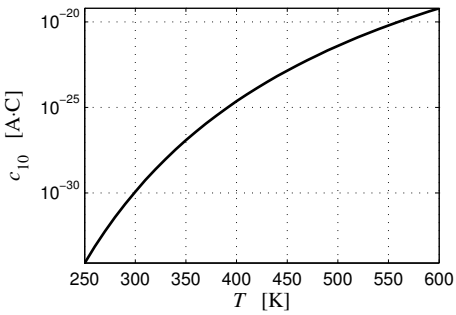


Fig.6. GICCR constant as a function of temperature (based on Table 1 data)

In contrast to $c_{10}(T)$, no major thermal variations are observed in the hole charge (6) which is the second thermally dependent parameter affecting the HBT transfer current. The functional dependence of the inverse hole charge on the temperature has a linearly declining character for a given BE

voltage in the low currents region ($V_{BE} < 0.4$ V). This conforms to a low-current-density case of the charge equation (5) when the minority charge Q_{fT} may be omitted from consideration (its influence is negligible). At higher biases, the decline is faster and deviates from the linear law due to the Q_{fT} impact that complicates analytical description of the transfer current. The latter reason is another factor dictating restriction of the quiescent point's thermal drift in the low-to-medium current region for the analysis-based PTAT circuit design.

IV. Current Mirror with Constant Voltage Supply

A. Output Current Derivation Based on General Transistor Model

In accordance with the historic terminology, we can define two major bipolar transistor parameters: the scale current, $I_{Sk} = I_{Bk}\exp(-\eta V_{BEk}/V_T)$, and the transconductance, $\beta_k = I_{Ck}/I_{Bk}$, where I_{Bk} is the base current ($k = 1, 2$). Both of these parameters are technology-specific in their functional dependence of the temperature and the voltage across the BE junction (bias point) and have no simple analytical description in the modern physics-based transistor models. Before the functional expansion, we can however use them as equation parameters to solve the CM circuit.

The CM-CVS circuit is straightforward in implementation on the die because it does not require a constant, thermally invariant supply current (Fig.7). The voltage supply nominal conformance to the thermal drift boundaries of the Q1 quiescent point can be ensured by using a simple voltage divider in most scenarios. The set of equations describing the CM-CVS circuit is as follows:

$$\begin{cases} V_{CC} = (\beta_1 + 1) R_{ref} I_{B1} + R_{ref} I_{B2} + V_{BE1} \\ V_{BE1} = V_{BE2} + (\beta_2 + 1) R_E I_{B2} \end{cases}, \quad (12)$$

where V_{CC} is the supply voltage.

To solve the first equation of (12) for V_{BE1}, we introduce substitutions $V_{CC}^* = V_{CC} - R_{ref} I_{B2}$ and $I_{B1} = I_{S1}\exp(\eta V_{BE1}/V_T)$, so that the equation becomes:

$$\exp\left(\frac{\eta V_{BE1}}{V_T}\right) = \frac{-V_{BE1} + V_{CC}^*}{(\beta_1 + 1) R_{ref} I_{S1}}. \quad (13)$$

The solution of the nonlinear equation having the form $p^x = cx + d$ ($p > 0$, $c \neq 0$), is known to be $x = -\frac{W(-c^{-1} p^{-d/c} \ln p)}{\ln p} - \frac{d}{c}$, where W is the Lambert W function [22]. Hence the solution of (13) can be expressed as

$$V_{BE1} = V_{CC}^* - \frac{V_T}{\eta} W\left[\frac{\eta(\beta_1 + 1) R_{ref} I_{S1}}{V_T} \exp\left(\frac{\eta V_{CC}^*}{V_T}\right)\right]. \quad (14)$$

The operational condition $I_{B2} < I_{B1} << (\beta_1 + 1) I_{B1} < V_{CC}/R_{ref}$ allows an approximation

$$V_{BE1} \approx V_{CC} - R_{ref} I_{B2} - \frac{V_T}{\eta} W\left[\frac{\eta(\beta_1 + 1) R_{ref} I_{S1}}{V_T} \exp\left(\frac{\eta V_{CC}}{V_T}\right)\right]$$
$$= V_{CC} - R_{ref} I_{B2} - V_0. \quad (15)$$

Substitution of (15) into the second equation of (12) yields:

$$\exp\left(\frac{\eta V_{BE2}}{V_T}\right) = \frac{-V_{BE2} + V_{CC} - V_0}{R_{0,cvs} I_{S2}}, \quad (16)$$

where $R_{0,cvs} = (\beta_2 + 1) R_E + R_{ref}$.

The solution is then expressed as

$$V_{BE2} = V_{CC} - V_0 - \frac{V_T}{\eta} W\left[\frac{\eta R_{0,cvs} I_{S2}}{V_T} \exp\left(\frac{\eta (V_{CC} - V_0)}{V_T}\right)\right]. \quad (17)$$

The output current can then be found using (16) as

$$I_{OUT,cvs} = I_{C2} = \beta_2 I_{B2} = \beta_2 I_{S2} \exp\left(\frac{\eta V_{BE2}}{V_T}\right)$$
$$= \frac{\beta_2 V_T}{\eta R_{0,cvs}} W\left[\frac{\eta R_{0,cvs} I_{S2}}{V_T} \exp\left(\frac{\eta (V_{CC} - V_0)}{V_T}\right)\right]$$
$$= \frac{\beta_2}{R_{0,cvs}} \frac{V_T}{\eta} W\left[\rho W\left[\frac{\eta}{V_T}(\beta_1 + 1) R_{ref} I_{S1} \exp\left(\frac{\eta}{V_T} V_{CC}\right)\right]\right], \quad (18)$$

where $\rho = \frac{R_{0,cvs}}{(\beta_1 + 1) R_{ref}} \frac{I_{S2}}{I_{S1}}$.

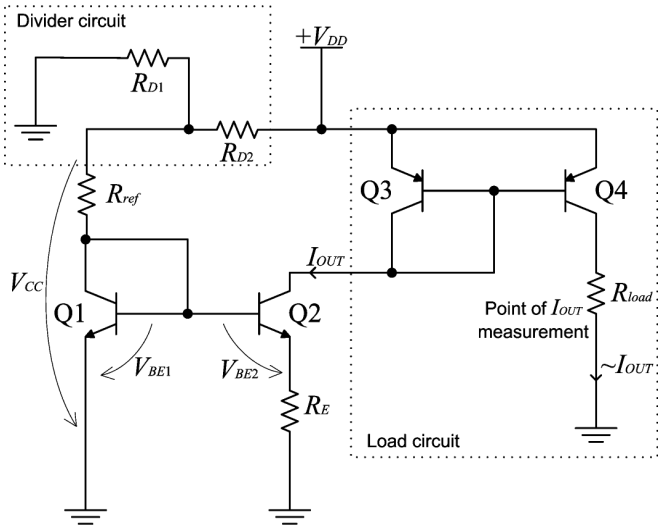


Fig.7. Current mirror with the constant voltage supply (CM-CVS). Dotted rectangles encompass optional voltage divider and load circuits

If the fabricated transistor devices are a good match in the temperature range of interest, one can with a reasonable accuracy consider that $I_{S1} \approx I_{S2} = I_S$ and $\beta_1 \approx \beta_2 = \beta$. Taking into account that $\beta >> 1$, (18) is simplified into

$$I_{OUT,cvs} \approx \frac{1}{(R_E + \beta^{-1} R_{ref})} \frac{V_T}{\eta} W\left[\rho W\left[\frac{\eta}{V_T} \beta R_{ref} I_S \exp\left(\frac{\eta}{V_T} V_{CC}\right)\right]\right], \quad (19)$$

where $\rho = R_E/R_{ref} + 1/(\beta + 1)$.

Referring to (3), for smaller R_{ref} nominals, the nonlinearity

in the output current's temperature characteristic is introduced due to the term $\ln\frac{I_{C1}}{I_{C2}} \approx W\left[\rho W\left[\frac{\eta}{V_T}\beta R_{ref} I_S \exp\left(\frac{\eta}{V_T}V_{CC}\right)\right]\right]$ which is dependent on the thermal voltage, the emitter degeneration resistance and the transistor parameters I_S and β which are thermally dependent in general.

The disadvantages of equation (19) are related to the necessity of a relatively accurate specification of I_S and β. It is also apparent that the approximation precision depends on the R_E/R_{ref} ratio: the condition $R_E/R_{ref} >> 1/(\beta+1)$ must hold to minimise an effect of inaccurate β specification or a non-negligent mismatch between Q1 and Q2 when $\beta_1 \neq \beta_2$.

B. Output Current Derivation Based on HICUM/L0 Model

In a simplified theoretical representation, a bipolar transistor can be seen as an ideal translinear element (TE) characterised by the thermally-invariant scale current and the thermally-invariant transconductance [23]. Such an assumption underlies some of the earlier large-signal transistor models – the Ebers-Moll model and its modifications [24] as well as the broadly used Gummel-Poon model [25]. If a fabrication technology could be selected which would allow for the transistor parameters to be invariant in temperature, the CM-CVS output current description in a wide range of temperatures would be straightforward by (18) or (19).

Modern compact physics-based transistor models explicitly or implicitly specify the scale current variation with temperature while the transconductance variation with temperature represents a complex functional case the analysis of which is hampered by multiple factors, e.g., self-heating. This work considers a widely adopted implicit HICUM description for the thermal variation of the scale current [18]. The complete nonlinear model of the CM-CVS output current is subjected to the second-order Taylor series approximation to derive a closed-form mapping between the measured voltage/current across the sensor load and the temperature estimate. Although the transconductance parameter cannot be specified accurately in a wide range of temperatures, we will show that the approximated model provides quite an accurate output current description.

By ensuring the biasing scheme design that the thermal drift of the quiescent point takes place only in the low- to medium-density current region, the forward transfer current in HICUM is computed as

$$i_{T_f} = \frac{c_{10}(T)}{Q_{pT}(T,V_{BE})}\exp\left(\frac{\eta}{V_T}V_{BE}\right), \qquad (20)$$

where the thermal variation is stipulated predominantly by the functional dependence of the GICCR constant c_{10} (4) (Fig.6) while the transport related hole charge Q_{pT} does not exceed in variation one order of a magnitude for a wide range of temperatures (Fig.8). The complex Q_{pT} description and the dependence on the voltage across the BE junction call for using a functional dependence approximation: the linear function of temperature is viewed as a sufficient variant for our purposes (the CM output current analysis). Let $T_{\min}$ and $T_{\max}$ denote the boundaries of the temperature range the CM circuit is subject to in operation. The value of the function $1/Q_{pT}(T,V_{BE})$ decreases with temperature (Fig.8) starting from $\Psi_0 = 1/Q_{pT}(T_{\min},V_{BE\max})$ where $V_{BE\max}$ denotes the beginning of the high current density region at $T = T_{\min}$ which the quiescent point should not cross (in the particular task of the analysis-based PTAT circuit design). The thermal drift of the quiescent point of both Q1 and Q2 in the CM results in a steady decrease of V_{BEi} with temperature that makes the proposed approximation viable: V_{BEi} is seen as being modulated by T (e.g., see Fig.9). The linear $1/Q_{pT}(T,V_{BE})$ approximation can be written as follows:

$$1/Q_{pT} \approx \Psi(T) = (\kappa T + \Delta - \kappa T_{\min})\Psi_0/\Delta, \qquad (21)$$

where $\Delta = T_{\max} - T_{\min}$ and the coefficient $\kappa > 0$ is assigned by means of empirical evaluation (refer to the subsequent examples).

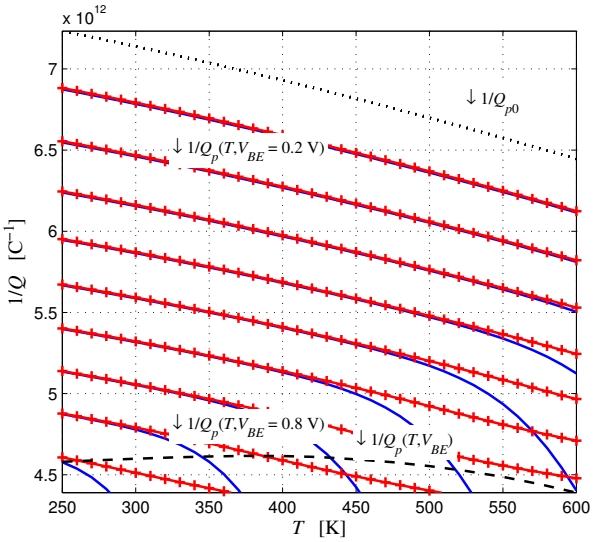


Fig.8. Inverse transport related hole charge (solid line set) as a function of the temperature and the BE voltage in 0.1 V steps ranging from 0.1 V to 0.9 V (based on Table 1 data): "+" markers denote the hole and the depletion charge contribution without the minority charge effect; the dotted line points at the zero-bias hole charge boundary; the dashed line corresponds to the thermal drift of the Q1 quiescent point in the CM-CVS circuit built on the considered HBT elements

Under the normal forward biasing operation conditions, the impact of the BC junction bias on the (reverse) transfer current can be neglected in the collector output current computation. Hence

$$I_C = \beta I_S \exp\left(\frac{\eta}{V_T}V_{BE}\right) \approx i_{T_f} \approx c_{10}(T)\Psi(T)\exp\left(\frac{\eta}{V_T}V_{BE}\right), \qquad (22)$$

Substitution of the product $\beta I_S \approx c_{10}(T)\Psi(T)$ into (19) clearly shows that inaccurate specification of the transconductance does not have much impact if

$R_E/R_{ref} >> 1/(\beta+1)$. This is the main idea behind reduction of the critical parameter set governing the CM-CVS output current description.

$$I_{OUT,cvs} \approx \frac{V_{CC}}{(R_E+\beta^{-1}R_{ref})}\frac{T}{\gamma_{cvs}} \times W\left[\rho W\left[\frac{\gamma_{cvs}}{T}\frac{c_{10}(T)\Psi(T)R_{ref}}{V_{CC}}\exp\left(\frac{\gamma_{cvs}}{T}\right)\right]\right] = \frac{V_{CC}}{(R_E+\beta^{-1}R_{ref})}\frac{T}{\gamma_{cvs}} \times W\left[\rho W\left[(\nu_\zeta T^\zeta+\nu_{\zeta-1}T^{\zeta-1})\exp\left(\sigma\frac{\gamma_{cvs}}{T}\right)\right]\right], \quad (23)$$

where $\gamma_{cvs}=\eta V_{CC}T/V_T=\eta q_e V_{CC}/k_B$, $\sigma=1-v_{gB}/(\eta V_{CC})$, $\nu_\zeta=\frac{\eta q_e c_{10nom}\Psi_0 R_{ref}\kappa}{k_B\Delta T_{nom}^\zeta}\exp\left(\frac{q_e V_{gB}}{k_B T_{nom}}\right)$,

$\nu_{\zeta-1}=\frac{\eta q_e c_{10nom}\Psi_0 R_{ref}(\Delta-\kappa T_{\min})}{k_B\Delta T_{nom}^\zeta}\exp\left(\frac{q_e V_{gB}}{k_B T_{nom}}\right)=(\kappa^{-1}\Delta-T_{\min})\nu_\zeta$

Note that $\zeta=0$, $\sigma=1$, $\nu_\zeta=0$ and $\nu_{\zeta-1}=\eta q_e c_{10nom}\Psi_0 R_{ref}/k_B$ in a special case of the TEs.

Let $I_{0,cvs}=V_{CC}/(R_E+\beta^{-1}R_{ref})$ and $f_{cvs}(T)=(T/\gamma_{cvs})W[\rho W[(\nu_\zeta T^\zeta+\nu_{\zeta-1}T^{\zeta-1})\exp(\sigma\gamma_{cvs}/T)]]$, then (23) can be expanded for a Taylor series approximation around the point $T=T_0$ as

$$I_{OUT,cvs}=I_{0,cvs}f_{cvs}(T) = I_{0,cvs}\left[f_{cvs}(T_0)+\sum_{k=1}^{\infty}\frac{f_{cvs}^{(k)}(T_0)}{k!}(T-T_0)^k\right], \quad (24)$$

where $f_{cvs}^{(k)}(T)=\frac{d^k}{dT^k}f_{cvs}(T)$.

Limiting the series by the second order, one can express:

$$f_{cvs}(T)\cong f_{cvs,2}(T) = f_{cvs}(T_0)+d_{1,cvs}(T_0)(T-T_0)+d_{2,cvs}(T_0)(T-T_0)^2, \quad (25)$$

where

$$d_{1,cvs}(T)=\frac{d}{dT}f_{cvs}(T) = \frac{W(\gamma_{cvs}/T)}{\gamma_{cvs}}\left[1+\frac{c_2T^2+c_1T+c_0}{T(\nu_\zeta T+\nu_{\zeta-1})[W(\gamma_{cvs}/T)+1](w_e+1)}\right], \quad (26)$$

$$d_{2,cvs}(T)=\frac{1}{2}\frac{d^2}{dT^2}f_{cvs}(T) = \frac{W(\gamma_{cvs}/T)(c_2T^2+c_1T+c_0)}{2\gamma_{cvs}T(\nu_\zeta T+\nu_{\zeta-1})[W(\gamma_{cvs}/T)+1](w_e+1)} \times\left[\frac{2c_2T+c_1}{c_2T^2+c_1T+c_0}-\frac{\nu_\zeta}{\nu_\zeta T+\nu_{\zeta-1}} +\frac{(c_2T^2+c_1T+c_0)}{T^2(\nu_\zeta T+\nu_{\zeta-1})(w_e+1)}\left(\frac{1}{[W(\gamma_{cvs}/T)+1]^2}-\frac{w_e}{w_e+1}\right)\right], \quad (27)$$

$$c_0=-\sigma\gamma_{cvs}\nu_{\zeta-1}, \quad (28)$$

$$c_1=(\zeta-1)\nu_{\zeta-1}-\sigma\gamma_{cvs}\nu_\zeta, \quad (29)$$

$$c_2=\zeta\nu_\zeta, \quad (30)$$

$$w_e=W[\rho W[(\nu_\zeta T^\zeta+\nu_{\zeta-1}T^{\zeta-1})\exp(\sigma\gamma_{cvs}/T)]]. \quad (31)$$

In a special case of the TEs,

$$d_{1,cvs}(T)=\frac{W(\gamma_{cvs}/T)}{\gamma_{cvs}}\left[1-\frac{\gamma_{cvs}+T}{T[W(\gamma_{cvs}/T)+1](w_e+1)}\right], \quad (32)$$

$$d_{2,cvs}(T)=\frac{W(\gamma_{cvs}/T)}{2\gamma_{cvs}T[W(\gamma_{cvs}/T)+1](w_e+1)} \times\left[\frac{(\gamma_{cvs}+T)^2}{T^2(w_e+1)}\left(\frac{1}{[W(\gamma_{cvs}/T)+1]^2}-\frac{w_e}{w_e+1}\right)-1\right]. \quad (33)$$

C. PTAT Tangent and the Maximum Thermal Gain

The skew of the output current thermal characteristic around the observation point $T=T_0$ gives an idea of its proximity to the ideal PTAT law. It also quantifies the thermal gain of the output current, i.e. the current increment with the temperature in the $T=T_0$ region of the characteristic. The skew is determined by the tangent at $T=T_0$:

$$f_{cvs,1}(T)=f_{cvs}(T_0)+d_{1,cvs}(T_0)(T-T_0) = \frac{W(\gamma_{cvs}/T_0)}{\gamma_{cvs}}\left[\left(1+\frac{c_2T_0^2+c_1T_0+c_0}{T_0(\nu_\zeta T_0+\nu_{\zeta-1})[W(\gamma_{cvs}/T_0)+1](w_{e0}+1)}\right)T -\frac{c_2T_0^2+c_1T_0+c_0}{(\nu_\zeta T_0+\nu_{\zeta-1})[W(\gamma_{cvs}/T_0)+1](w_{e0}+1)}\right], \quad (34)$$

where

$$w_{e0}=W[\rho W[(\nu_\zeta T_0^\zeta+\nu_{\zeta-1}T_0^{\zeta-1})\exp(\sigma\gamma_{cvs}/T_0)]]. \quad (35)$$

If the circuit is made on TEs, (34) becomes:

$$f_{cvs,1}(T)=\frac{W(\gamma_{cvs}/T_0)}{\gamma_{cvs}}\left[\left(1-\frac{\gamma_{cvs}+T_0}{T_0[W(\gamma_{cvs}/T_0)+1](w_{e0}+1)}\right)T +\frac{\gamma_{cvs}+T_0}{[W(\gamma_{cvs}/T_0)+1](w_{e0}+1)}\right]. \quad (36)$$

D. Temperature Estimate

Given the measured current at the CM-CVS circuit output, $\hat{I}_{OUT,cvs}$, one can determine the corresponding temperature. Let $T_\Delta=T-T_0$, then the temperature estimate can be calculated using the quadratic equation (25):

$$d_{2,cvs}(T_0)T_\Delta^2+d_{1,cvs}(T_0)T_\Delta+f_{cvs}(T_0)=\hat{I}_{OUT,cvs}/I_{0,cvs} \quad (37)$$

that results in

$$\hat{T}_{cvs}=T_0-\frac{d_{1,cvs}(T_0)}{2d_{2,cvs}(T_0)} +\frac{\sqrt{d_{1,cvs}^2(T_0)-4d_{2,cvs}(T_0)[f_{cvs}(T_0)-\hat{I}_{OUT,cvs}/I_{0,cvs}]}}{2d_{2,cvs}(T_0)}, \quad (38)$$

where $T_\Delta=T-T_0$.

To assess the accuracy of a temperature estimate $\hat{T}$ obtained using (38) or other methods, one can adopt the *mean relative estimation error* (MREE) metric:

$$\bar{\varepsilon} = \frac{1}{\Delta}\int_{T_{\min}}^{T_{\max}} \left|1 - \frac{\hat{T}}{T}\right| \mathrm{d}T \,, \tag{39}$$

where $\Delta = T_{\max} - T_{\min}$, and $T_{\min}$ and $T_{\max}$ denote the boundaries of the temperature range the CM circuit is subject to during operation.

V. Numerical Analysis

A. Biasing Conditions

A simulation example benchmarking the analytical findings from the preceding section represents the CM-CVS circuit (Fig.7) based on the IBM 5HP 0.32×16.8 μm^2 HBT (which was described in Section III). The entire circuit is powered by the supply voltage $V_{DD} = 3.3$ V which is standard for the selected HBT process. The CM-like load circuit consists of the matched *pnp* transistors with a symmetric emitter connection and is terminated by $R_{load} = 50$ Ω.

Biasing of the CM-CVS circuit has to be configured to prevent a thermal drift of the Q1 quiescent point into the self-heating region or the high current region. This is achieved by choosing corresponding settings of the supply voltage V_{CC} and the series reference resistance R_{ref}. At low temperatures (close to 250 K) the current through Q1 is very low, hence the voltage drop across R_{ref} $(I_B + I_C)R_{ref} << V_{CC}$, and the entire supply voltage is actually applied to the BE junction. As the current through Q1 and R_{ref} grows with the temperature, the BE voltage decreases due to an increasing voltage drop across the series resistor. This trend is shown in Fig.9, where a linear variation of V_{BE} with the temperature causes an exponential change in the current through the transistor. Smaller R_{ref} values set a higher current through Q1, which would also result in a higher mirroring current through Q2 in the CM-CVS configuration. However R_{ref} is bounded from beneath at the high temperatures (near 600 K) as it should be large enough to enable a sufficient drop in the BE voltage preventing the self-heating (cf. Fig.4(b) and Fig.5).

The thermal drift description from the preceding paragraph allows drawing a recommendation for the biasing scheme design. V_{CC} is set first, referring to the Gummel characteristics of the transistor at the lowest temperature in the range (Fig.4 (b)): $V_{CC} < V_{BE\max}$, where $V_{BE\max}$ denotes a BE voltage serving as a self-heating or high currents (compression) boundary. At the second step, the Gummel characteristics at the highest temperature in the range (Fig.4(b) and Fig.5) allow to determine $R_{ref} > (V_{CC} - V_{BE}^*)/I_C^*$, where V_{BE}^* and I_C^* denote an approximately chosen self-heating bound on the quiescent point at the highest temperature. To achieve the best possible CM efficiency, our example features $V_{CC} = V_{BE\max} = 0.95$ V and $R_{ref} \geq 100$ Ω. According to Fig.9, the self-heating impact becomes observable at $R_{ref} = 10$ Ω and smaller values.

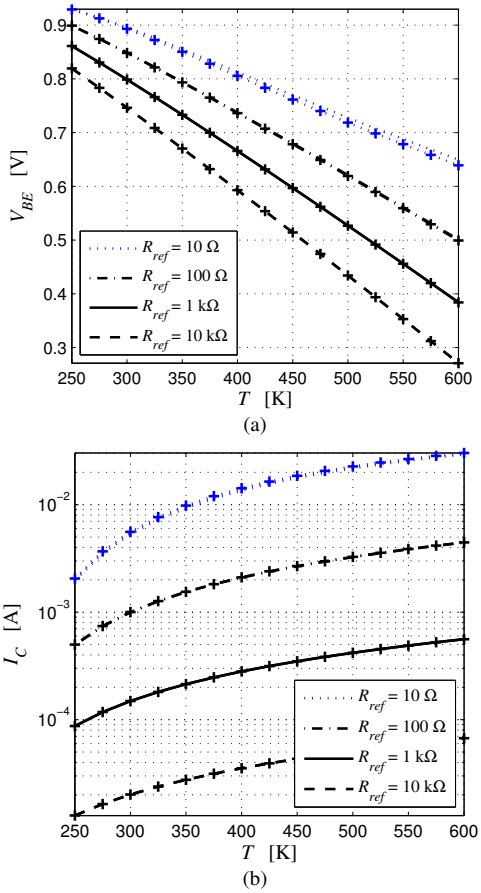


Fig.9. Biasing characteristics for the diode-connected transistor Q1 when Q2 is turned off, i.e. $I_{B2} = 0$ ($V_{CC} = 0.95$ V)

B. Circuit Parameters

The impact of the scale current parameter selection is shown in Fig.10. Smaller reference resistances necessitate more accurate specification of the scale current parameter for modelling at higher temperatures. This rule is relevant when the CM circuit is assembled on the TEs.

The thermal variation model for the normalised CM-CVS output current described by equations (23)-(24) is shown in Fig.11. The model is parameterised according to the HICUM/L0 specifications (Table 1). The characteristic appears to be a very close match to the PTAT law, especially at higher temperatures. The linearity of the characteristic is only marginally influenced by the Q2 emitter degeneration resistor R_E. Increase of R_E yields a higher thermal gain of the output current. However the magnitude of the CM output current declines since the normalising current $I_{0,cvs}$ is inversely proportional to R_E, thus reducing the CM efficiency.

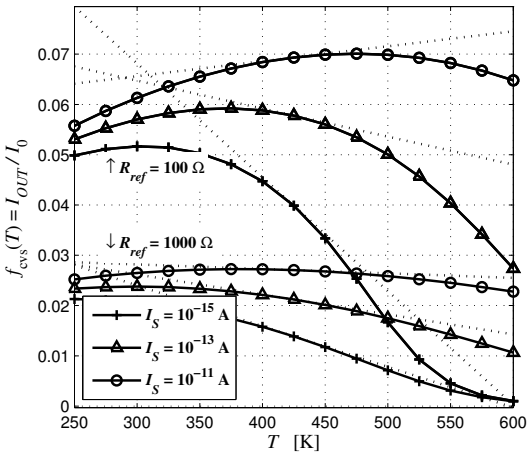


Fig.10. Scale current influence on the normalised CM-CVS output current, shown for two reference resistances: $R_{ref} = 100\ \Omega$ (top set of curves) and $R_{ref} = 1\ \text{k}\Omega$ (bottom set of curves)

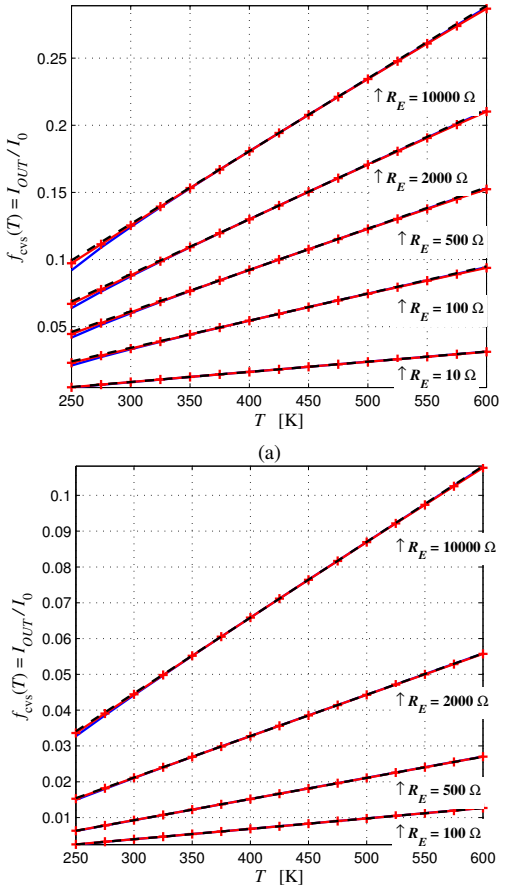


Fig.11. Normalised CM-CVS output current at (a) $R_{ref} = 100\ \Omega$ and (b) $R_{ref} = 10\ \text{k}\Omega$: "+" markers denote the second-order approximation; dashed lines denote PTAT tangents drawn at $T_0 = 425$ K

C. PTAT Current Output and Temperature Estimation

Simulation-based benchmarking of the analytical relations (19)-(25) leads to a conclusion that the empirical factor κ (parameter reflecting the thermal drift of the hole and minority charge) has no major effect on the HBT-based CM output current prediction (Fig.12). However κ adjusts precision of the PTAT skew that is important to produce accurate high temperature estimates. A visible deviation of the approximated characteristic from the simulated one takes place only at lower frequencies (below the reference temperature of 298 K); however no major nonlinearities are observed. A TE-based CM circuit resorting on the constant scale current fixed at the value corresponding to $T_0 = 425$ K exhibits a completely different, highly nonlinear thermal trend that sets applications of the TE and HBT thermal models apart. HBTs are seen as a particularly good match for the PTAT CM-CVS application. The TE-based CM-CVS output current is quite accurately described by the analytical approximation (23) being one of the special cases of the general solution.

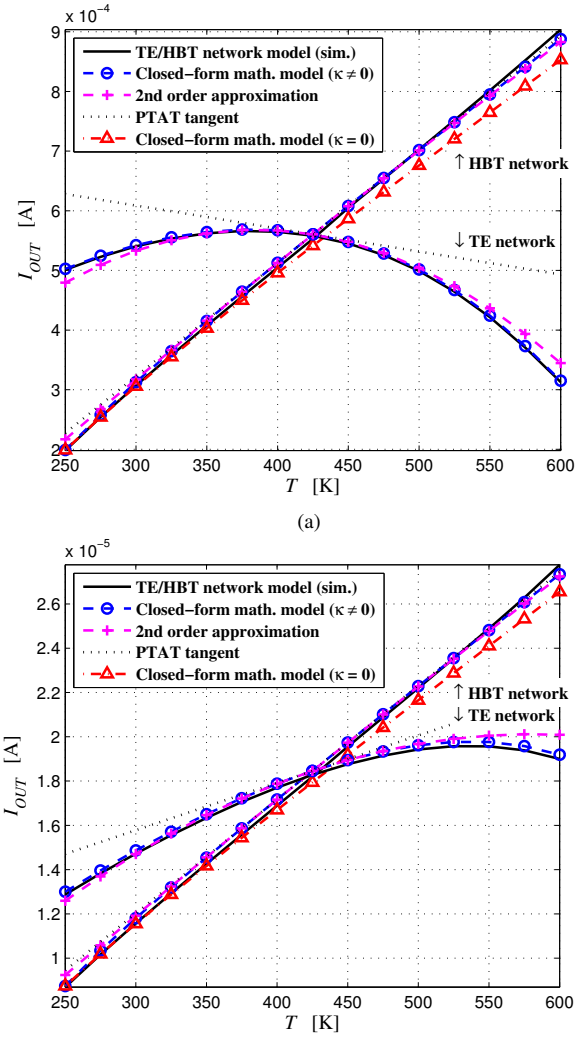


Fig.12. CM-CVS output current at $R_{ref} = 100\ \Omega$ and (a) $R_E = 100\ \Omega$, $\kappa = 2$, (b) $R_E = 10\ \text{k}\Omega$, $\kappa = 6$

A configuration scenario shown in Fig.13(a) represents a violation of the approximation validity condition deduced earlier: $R_E / R_{ref} >> 1/(\beta + 1)$. The result is a relatively large

deviation of the output current's analytical description from the simulated characteristic that is observed for both the circuit on TEs and the circuit on HBTs when $\kappa = 0$. At the same time the linearity of the simulated output current is found to be an almost perfect match to the PTAT law at both lower and higher temperatures. The approximated characteristic almost coincides with the PTAT tangent at $\kappa = 6$. The trends shown in Fig.13(a) resemble the trends in Fig.12(b), except for the reduced CM efficiency due to a higher R_{ref} nominal. Comparison of Fig.12(b) with Fig.13(a) also reveals that the adjustment of the reference resistance R_{ref} in the first instance followed by R_E selection might result in a bigger thermal gain than the adjustment of only R_E having R_{ref} set to the allowed minimum corresponding to the maximum CM efficiency.

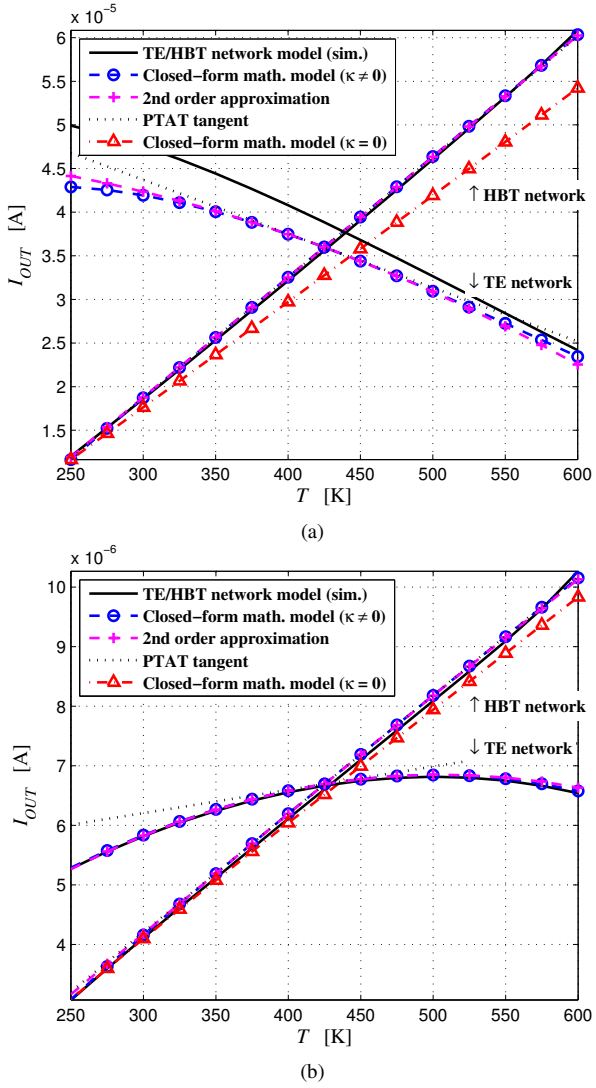


Fig.13. CM-CVS output current at $R_{ref} = 10$ kΩ and (a) $R_E = 100$ Ω, $\kappa = 6$, (b) $R_E = 10$ kΩ, $\kappa = 3$

The MREE of the temperature estimate (38) for the four considered CM-CVS operating schemes is listed in Table 2. The output currents were produced by simulating the CM-CVS circuit based on the HBTs (HICUM/L0). The circuit based on the TEs is not applicable to the PTAT current-driven sensor design. The temperature estimation error does not exceed an average of 1.3 % across the wide range from 250 to 600 K. The precision of the estimation deteriorates mainly towards the beginning of the temperature range.

TABLE 2
MEAN RELATIVE ESTIMATION ERROR BY THE THERMAL SENSOR BASED ON THE CM-CVS CIRCUIT

Circuit parameters		Temperature MREE
R_{ref}	R_E	
100 Ω	100 Ω	1.13 %
	10 kΩ	1.30 %
10 kΩ	100 Ω	0.43 %
	10 kΩ	0.95 %

D. Comparison between CM-CVS and CM-CCS as a PTAT Current Source

Fig.14 shows comparison between the CM circuits with the constant voltage and constant current supply (CM-CVS and CM-CCS, respectively) which are configured to produce output currents in two ranges with the difference constituting about two orders of magnitude. The emitter of Q2 in the CM-CCS circuit is loaded with the optimal resistance enabling the maximum thermal gain. Parameters of the CM-CVS circuit are repeated from the preceding section. The mirrored current branch in both types of circuits is powered by $V_{DD} = 3.3$ V. For comparative purposes, Fig.14 shows output currents of the CM-CVS with the voltage supply from an ideal source $V_{DD} = V_{CC} = 0.95$ V and from a voltage divider connected to the standard $V_{DD} = 3.3$ V.

For all current ranges the CM-CVS circuit exhibits a better PTAT linearity and much higher thermal gain of the output current than the CM-CCS circuit. As pointed out in the preceding section, variation of R_{ref} (primary circuit parameter) and R_E (secondary circuit parameter) can yield an even higher thermal gain than shown in the figure.

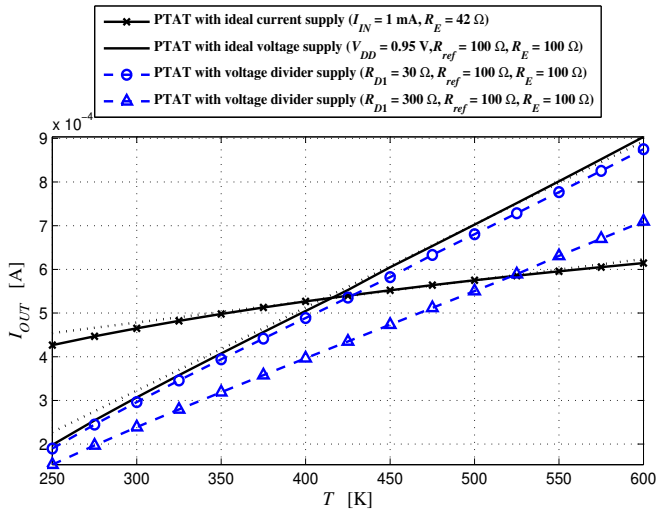
Design of the voltage divider necessitates $R_{D1} << R_{ref}$ maintaining a stable V_{CC} voltage across the range of temperatures. This condition can easily be fulfilled by setting a larger R_{ref} at the expense of a reduced CM efficiency (as in Fig.14(b)).

VI. CONCLUSION

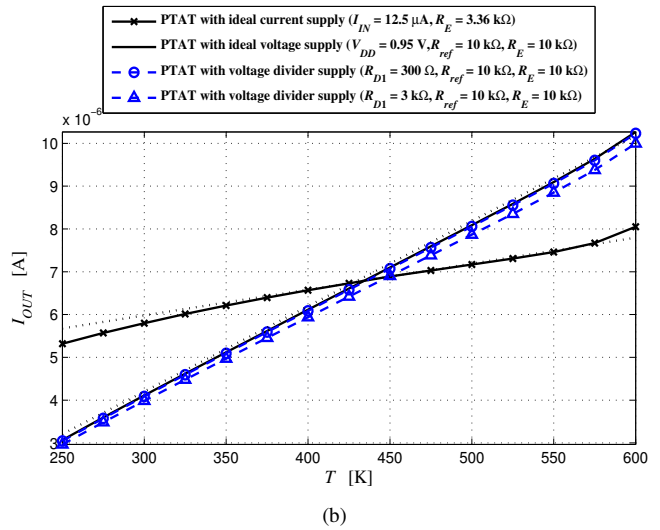
Analytical derivations presented in this work show that implementation of an IC-based PTAT thermal sensor is possible with only two HBTs joint into the Widlar CM network and sharing the same ambient temperature. The PTAT thermal gain of the CM circuit powered by the CVS is higher than the gain of the CM circuit powered by the CCS. The CM-CVS solution produces an output current in good conformance to the PTAT law. The CM-CVS output current can be

described using an accurate closed-form expression based on the HICUM physics principles featuring realistic thermal dependences of the main HBT parameters. Devised approximations substantially limit the number of HICUM parameters describing the output of the PTAT circuit model. Thus, the temperature sensor design in the technology-dependent CM-CVS circuit variant is represented by only a few analytical relations. Simulation-based verification of these relations on the IBM 5HP technology node example established 0.43 % achievable accuracy of the temperature estimates from the PTAT circuit output in the temperature range from 250 K to 600 K.

The presented CM structure and the corresponding analytical methods could also form a theoretical foundation for the analogue thermal compensation circuit design.



(a)



(b)

Fig.14. CM-CCS vs. CM-CVS at two output current ranges: dotted lines denote PTAT tangents

REFERENCES

[1] W. Huang, M. Allen-Ware, J. Carter, E. Cheng, K. Skadron, and M. Stan, "Temperature-aware architecture: Lessons and opportunities," *IEEE Micro*, vol. 31, no. 3, pp. 82-86, May-Jun. 2011.

[2] J. Altet, W. Claeys, S. Dilhaire, and A. Rubio, "Dynamic surface temperature measurements in ICs," *Proc. IEEE*, vol. 94, no. 8, pp. 1519-1533, Aug. 2006.

[3] J. Altet, A. Rubio, S. Dilhaire, E. Schaub, and W. Claeys, "BiCMOS thermal sensor circuit for built-in test purposes," *Electron. Lett.*, vol. 34, no. 13, pp. 1307-1309, Jun. 1998.

[4] E. Aldrete-Vidrio, D. Mateo, and J. Altet, "Differential temperature sensors fully compatible with a 0.35-µm CMOS process," *IEEE Trans. Compon. Packag. Technol*., vol. 30, no. 4, pp. 618-626, Dec. 2007.

[5] M. Onabajo, J. Altet, E. Aldrete-Vidrio, D. Mateo, and J. Silva-Martinez, "Electrothermal design procedure to observe RF circuit power and linearity characteristics with a homodyne differential temperature sensor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 3, pp. 458-469, Mar. 2011.

[6] S. Amon, M. Mozek, D. Vrtacnik, D. Resnik, U. Aljancic, and M. Cvar, "Compact BJT/JFET PTAT," *Adv. Electronic Materials and Packag. (EMAP)*, pp. 96-102, 2001.

[7] F. Alesii, M. Faccio, G. Ferri, C. Poduti, G. Stochino, and A. D'Amico, "A low voltage integrated temperature sensor," in *Proc. 26th European Solid State Device Research Conf. (ESSDERC)*, 1996, pp. 903-906.

[8] A. Fabre, "Bidirectional current-controlled PTAT current source," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl*., vol. 41, no. 12, pp. 922-925, Dec. 1994.

[9] C.-P. Liu and H.-P. Huang, "Experimental validation of PTAT for in situ temperature sensor and voltage reference," *Electron. Lett.*, vol. 44, no. 17, pp. 1016-1017, Aug. 2008.

[10] M. Sasaki, M. Ikeda, and K. Asada, "A temperature sensor with an inaccuracy of -1/+0.8 °C using 90-nm 1-V CMOS for online thermal monitoring of VLSI circuits," *IEEE Trans. Semicond. Manuf.*, vol. 21, no. 2, pp. 201-208, May 2008.

[11] M. Law and A. Bermak, "A 405-nW CMOS temperature sensor based on linear MOS operation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 12, pp. 891-895, Dec. 2009.

[12] P. Crepaldi, R. Moreno, and T. Pimenta, "Low-voltage, low-power, high linearity front-end thermal sensing element," *Electron. Lett.*, vol. 46, no. 18, pp. 1271-1272, Sep. 2010.

[13] M. Nishiguchi, M. Fujihara, A. Miki, and H. Nishizawa, "Precision comparison of surface temperature measurement techniques for GaAs IC's," *IEEE Trans. Compon., Hybrids, Manufact. Technol*., vol. 16, no. 5, pp. 543-549, Aug. 1993.

[14] H.-M. Rein and M. Schröter, "A compact physical large-signal model for high-speed bipolar transistors at high current densities - Part II: Two-dimensional model and experimental results," *IEEE Trans. Electron Devices*, vol . 34, pp. 1752-1761, 1987.

[15] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part I — Single-finger devices," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2009-2021, Sep. 2005.

[16] R. Widlar, "Some circuit design techniques for linear integrated circuits," *IEEE Trans. Circuit Theory*, vol. 12, no. 4, pp. 586-590, Dec. 1965.

[17] M. Schröter, S. Lehmann, S. Frégonèse, and T. Zimmer, "A computationally efficient physics-based model for circuit design – Part I: Model formulation," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 279-286, Feb. 2006.

[18] M. Schröter. (2011, Mar.). HICUM Level2 Version 2.23: A Complete Documentation [Online]. Available: http://www.iee.et.tu-dresden.de/iee/eb/hic_new/hic_doc.html

[19] M. Schröter and T.-Y. Lee, "Physics-based minority charge and transit time modeling for bipolar transistors," *IEEE Trans. Electron Devices*, vol. 46, no. 2, pp. 288-300, Feb. 1999.

[20] R. M. Malladi. *Silicon Heterostructure Handbook*: *Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy*. Edited by J. D. Cressler, CRC Press 2005, pp. A.4-1201–A.4-1210.

[21] C. Jacoboni, C. Canali, G. Ottaviani, and A. Alberigi Quaranta, "A review of some charge transport properties of silicon," *Solid-State Electronics*, vol. 20, no. 2, pp. 77-89, Feb. 1977.

[22] R. Corless, G. Gonnet, D. Hare, D. Jeffrey, and D. Knuth, “On the Lambert W function,” *J. Advances Comput. Math*., no. 5, pp. 329–359, 1996.
[23] B. Minch, “Analysis and Synthesis of Translinear Circuits,” Computer Syst. Lab., Cornell Univer., Ithaca, Tech. Rep. No. CSL-TR-2000-1002, Mar. 2000.
[24] D. Teeter, J. East, R. Mains, and G. Haddad, "Large-signal numerical and analytical HBT models," *IEEE Trans. Electron Devices*, vol. 40, no. 5, pp. 837-845, May 1993.
[25] H. Gummel and H. Poon, “An integral charge control model of bipolar transistors,” *Bell Syst. Tech. J.*, vol. 49, pp. 827-852, May-Jun. 1970.

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