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Abstract. Microdisplay technologies for near-to-eye applications mostly use a complementary metal-oxide semiconductor (CMOS) processing chip as backplane for pixel addressing, with extensive post-processing on top of the CMOS chip to deposit organic LED or liquid crystal layers. Here, we examine the possibility of integrating emissive microdisplays within the CMOS chip, with absolutely no post processing needed. This will dramatically reduce the manufacturing cost of microdisplays and may lead to new microdisplay applications. Visible electroluminescence is achieved by biasing *pn* junctions into avalanche breakdown mode. The most appropriate CMOS *pn* junction is selected and innovative techniques are applied to increase the light extraction efficiency from the CMOS chip using the metal layers of the CMOS process. An 8×64 dot matrix microdisplay was designed and manufactured in a 0.35-μm CMOS technology. The experimental results show that a luminance level of 20 cd/m^2 can be reached, which is an adequate luminance value in order to comfortably read data being displayed in relatively dark environments. The electrical power dissipation per pixel being activated is 0.9 mW/pixel. It is also shown that the pixels can be switched at a rate faster than 350 MHz.
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1 Introduction

According to their principle of operation, microdisplays can be classified as either modulating or emissive displays.[1] Modulating displays are illuminated by a separate light source and the incident light is then modulated in each pixel. The majority of modulating microdisplays utilize the liquid crystal on silicon (LCoS) technology and find use in both projection and near-to-eye applications. Emissive microdisplays emit light from each pixel on the surface of the array. The organic light emitting diode (OLED) technology is dominant in the emissive microdisplay market. Emissive microdisplays are mainly used in near-to-eye applications where the display is positioned near to the user's eye and viewed through an eyepiece.

Visible avalanche electroluminescent light emission from silicon *pn* junctions was reported for the first time in 1955.[2] Since then, significant progress has been made in increasing the efficiency of silicon based light emitting devices. Porous silicon avalanching electroluminescent devices were viewed as quite promising for microdisplay applications, especially since the internal quantum efficiencies achieved were relatively high.[3,4] However, porous silicon is a very reactive material and the long term stability of porous silicon microdisplays is problematic,[5] leading to reliability issues and short lifetimes. The porous silicon technology is also not fully compatible with the mature complementary metal-oxide semiconductor (CMOS) technology. Enhancing the efficiency of bulk CMOS avalanching junctions[6,7] resulted in external power efficiencies now approaching values where practical emissive microdisplay devices, visible to the naked eye, can be fully integrated in standard CMOS technology, with absolutely no process modifications or post processing.

While OLED and LCD technologies dominate the market for microdisplays, they have certain shortcomings. Compared to OLED and LCD displays, a fully integrated CMOS microdisplay does have a number of attractive advantages, especially considering cost, reliability, configurability, temperature range of operation, and frame rate. The widespread use of CMOS integrated circuits, added to the favorable cost, robustness and maturity of the technology, may lead to interesting applications in the microdisplay environment.

The combination of an image intensifier and CMOS avalanche electroluminescent *pn* junction devices for energy efficient display and projection applications has recently been proposed.[8] In this two-stage microdisplay architecture, a backplane IC implemented in standard 0.18 μm CMOS technology included a 360×200 pixel array of avalanche diodes, produced a faint optical image, and an image intensifier was then used to efficiently amplify the image to useful luminance levels. Although silicon light emitters have low efficiency, system efficiency in this case depended primarily on the image intensifier. In this application,[8] the maximum IC power dissipation was set to 1 W, and for a future 1 megapixel display, the full-scale pixel current was then 100 nA with a 10 V power supply. The image intensifier power dissipation was in the order of 300 mW.[9] It was shown that silicon light emitters and an image intensifier can be combined to produce high resolution images efficiently, and with adequate luminance for projection applications.

In this work, we present a full CMOS microdisplay[10] where no image intensification is utilized, making use of our improved internal quantum efficiency and light extraction efficiency techniques. This type of microdisplay may find applications in near-to-eye applications.

2 Silicon Light Sources

The silicon light sources used in our microdisplay are based on the principle of avalanche electroluminescence from reverse biased pn junctions. Our main aim was the complete integration of a microdisplay into a standard digital CMOS process, with no process modifications or post processing. The process used is a single n-well 0.35 μm CMOS process from *austriamicrosystems*. A number of diode structures are available in the CMOS process, namely n^+-to-p substrate, p^+-to-n well, p^+n^+ in well or substrate, and n-well to p-substrate diodes. The n-well to p-substrate junction breakdown voltage is too high (in excess of 25 V) to implement in a CMOS circuit. Although the n^+p^+ diodes exhibited low breakdown voltages (<5 V), the field emission or Zener breakdown mechanism reduced the internal quantum efficiency of the light generation process.[11] The only practical diode structures to be considered are the n^+p and p^+n junctions.

The n^+p and p^+n diode structures are shown in Fig. 1, not drawn to scale. In Fig. 1(a) is shown the cross section of the devices in the LOCOS (local oxidation of silicon) CMOS technology, and in Fig. 1(b) is shown the layout of the preferred p^+n light emitting junction. To increase the electric field and reduce the breakdown operating voltage somewhat, the junction is a point source as indicated in Fig. 1(b). Breakdown will eventually occur near the apex of the p^+ diffusion facing the n^+ contact, resulting in localized light emission and relatively high current density. Both p^+n and n^+p diodes exhibit a 9.2 V breakdown voltage.

In Fig. 2, the emitted integral light intensity as a function of avalanche reverse current is shown. It can be seen from Fig. 2 that both junctions exhibit a change in slope of the light emission intensity versus reverse current relationship, with the p^+n diode having a breakpoint at about 170 μA. It will not be advantageous to bias the point sources at current levels beyond the breakpoint in the light intensity versus reverse current slope. Using the p^+n junction, biasing currents up to 170 μA per point source can be achieved without a significant drop in efficiency. This will reduce the area of a pixel for a fixed optical output power. Although the breakpoint was used as a design constraint, the characteristic breakpoint in Fig. 2 became less significant when using the point sources in array configurations. This affords the design some robustness around the biasing design choice. The main advantage of the p^+n junction is that the junction is floating [see Fig. 1(a)], with neither terminal connected to a supply voltage. This facilitates the voltage of the lightly doped n-well region to be increased substantially more positive relative to the grounded p-substrate. The advantage of this degree of freedom is that the voltage of the p^+-region can be pulled negative to induce avalanche impact ionization, depending on the positive potential of the n-well, allowing the use of substrate-based n-channel metal-oxide semiconductor (NMOS) drivers in a single well process.

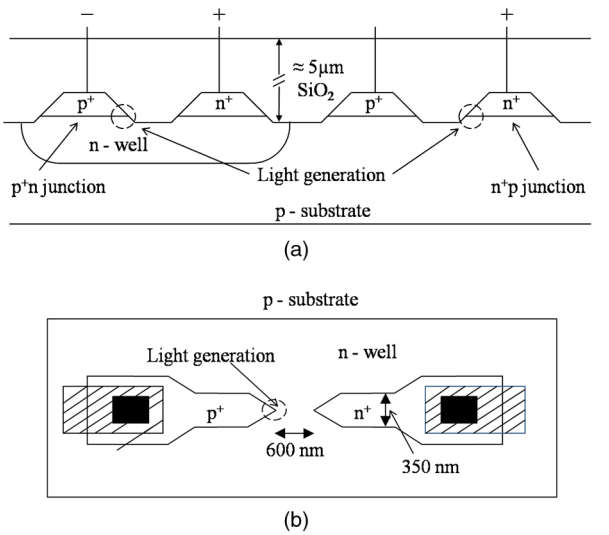

Fig. 1 (a) Cross section of junctions, and (b) layout design of a single point source using the p^+n junction.

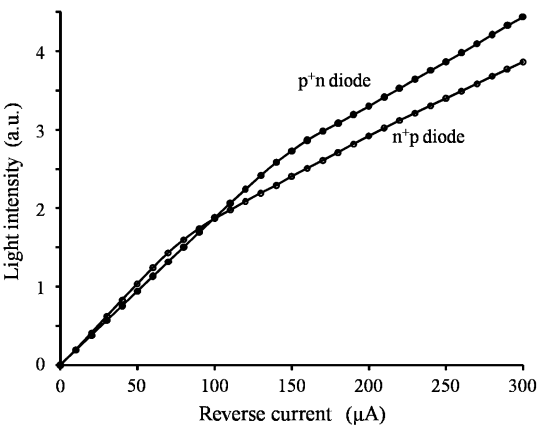

Fig. 2 Light intensity as a function of reverse current.

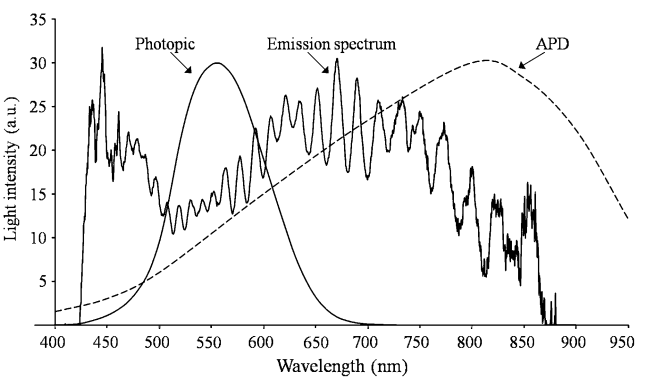

Fig. 3 The emission spectrum of the p^+n CMOS junction in avalanche, the normalized eye response and APD responsivity.

The pn junction in the avalanche impact ionization region of operation induces hot carrier radiative indirect interband recombination,[12,13] with a significant amount of radiation within the visible region. The normalized measured spectrum of the emitted light from a single p^+n point source is shown in Fig. 3. Also included in Fig. 3 are the normalized photopic

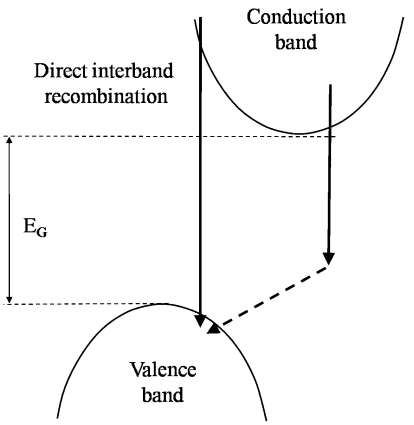

Fig. 4 Direct and indirect interband radiative recombination in avalanche electroluminescent silicon.

responsivity of the human eye and the responsivity of a Hamamatsu C5658 Silicon APD (avalanche photodiode) we used for switching speed measurements.

The emission spectrum of the p^+n junction exhibits an interference pattern as a result of the approximately 5 μm thick silicon dioxide layer covering the emitting junction. Our experimental emission spectrum shows two mechanisms involved in the photon generation. The first mechanism is the process of indirect interband hot carrier recombination[12,13] with a peak at 675 nm (1.84 eV photon energy) and a relatively wide emission spectrum ranging from 500 nm to 850 nm. We also observe a second mechanism with a narrower spectral band, peaking at 440 nm (2.8 eV photon energy) and ranging from 425 nm to 525 nm. We believe this to be the direct interband radiative recombination process within the silicon junction.[14] The two mechanisms are shown in Fig. 4.

3 Improving Light Extraction Efficiency

Although internal quantum efficiency is important, the light extraction efficiency from the generation site within a high refractive index material like silicon to air, through a low refractive index material like silicon dioxide, has a substantial impact on the external power efficiency. In order to enable more light to leave the silicon/oxide/air interface and surface, a light directing structure was formed in the interconnect layers of the CMOS process. By using interconnect vias and metal layers inherently available in the CMOS process; a parabolic reflector structure was created surrounding each light generation point.[15]

A photograph of the reflector structure is shown in Fig. 5 where the cross section scanning electron microscope (SEM) image was formed using a focused ion beam (FIB). The position of the point source in the cross section is indicated by the star. The cross section of the reflector structure shows the four metal layers, as well as the three metal interconnect vias.

The integrated reflector light extraction enhancement factor is shown in Fig. 6 as a function of wavelength. From this figure, it can be seen that the light extraction efficiency is increased by a factor of more than 5 in the wavelength range 450 nm to 650 nm, which overlaps the visual eye response spectral range shown in Fig. 3.

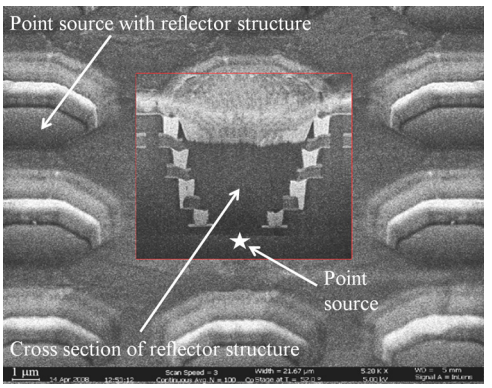

Fig. 5 Metal reflector structure to increase light extraction efficiency.

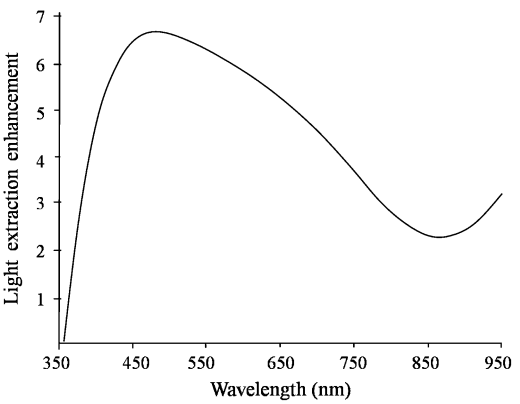

Fig. 6 Spectral enhancement of light extraction efficiency due to integrated reflectors.

4 Switching Speed of the CMOS Light Source

Initially aimed at on-chip optical interconnects, silicon avalanche electroluminescence light sources have experimentally been shown to be modulated up to a frequency of 20 GHz using streak camera techniques.[16] These experimental results indicate that any bandwidth limitations experienced with silicon light sources driven in avalanche breakdown are electrical in nature and not due to the underlying physical emission mechanism.

In our experiment, a sine wave was applied to the light emitting device driver circuit, and a multi-mode optical fiber was mechanically aligned to a light source array. The optical signal via the fiber was detected by a silicon APD module with responsivity of approximately 2.5×104 V/W and the APD output signal displayed on a spectrum analyzer. The Hamamatsu C5658 Silicon APD detector spectral response shown in Fig. 3 indicates that the APD basically detects the near infrared component of the emission spectrum.

Using the experimental setup as discussed above, a switching speed of 350 MHz was achieved, as demonstrated in Fig. 7. This is the fastest ever reported switching speed of electroluminescent silicon light sources implemented in a standard CMOS process.[17] This current switching speed benchmark of 350 MHz was limited by the electrical bandwidth of the driver circuitry and further improvements to the driving circuits should lead to switching speeds in excess of

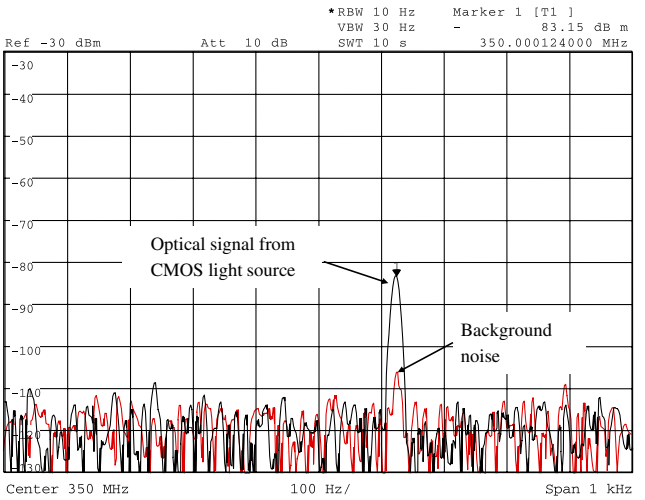

Fig. 7 350 MHz switching speed displayed on a spectrum analyzer.

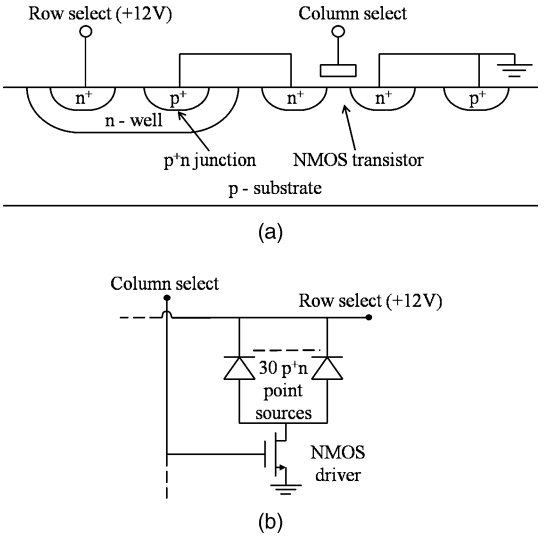

Fig. 8 (a) Pixel cross section, and (b) pixel circuit.

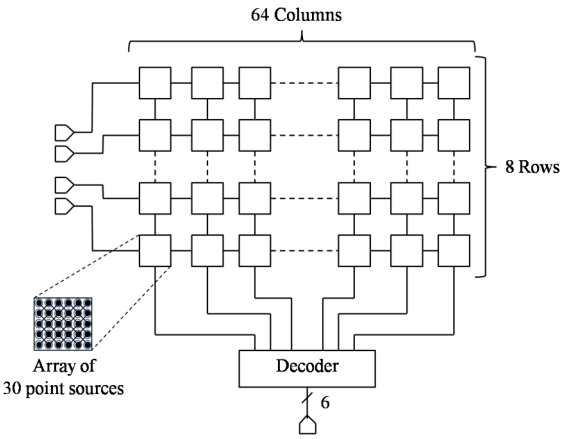

Fig. 9 Arrangement of 8×64 pixel array with inputs.

1 GHz. It should be noted that the light sources used in the switching speed experiment are the same devices used in the dot matrix display.

5 Pixel Design

A single pixel with dimensions approximately 50×50 μm^2 is formed by arranging 30 of the p^+n point light sources described above in a parallel array. Each pixel also has a single NMOS driver transistor capable of switching the p^+n junction array between the avalanche mode and an off mode. The sizing of the NMOS driver transistor is based on the maximum required pixel drive current (30×170 μA $= 5.1$ mA) and is designed to accept inputs directly from logic buffers available as standard cells in the AMS foundry cell library. This ensures easy integration with controller circuitry and therefore allows the display to enjoy the full benefit of the powerful digital design techniques afforded by CMOS. The pixel circuit and structural cross section is shown in Fig. 8.

In order to activate a pixel, a supply voltage sufficient to ensure avalanche breakdown needs to be applied to the n-well relative to the grounded p-substrate. In the current design, this requires a voltage of around $+12$ V applied to the n-well. Upon the application of logic 1 to the gate of the NMOS transistor, the p^+ node voltage is forced lower until breakdown occurs. This results in light emission from the pixel. Once the applied gate voltage is zeroed, the NMOS transistor switches off, and the voltage on the drain of the NMOS transistor rises and the voltage drop across the p^+n junction will decrease to switch off the light emission.

In this off condition, the leakage currents of the reverse biased junctions should be considered. Careful design is required to ensure that the drain node of the driving NMOS device does not exceed the allowable limits as gate oxide breakdown may occur at the overlap of the drain diffusion and the gate conductor. The ratio of the p^+n junction reverse leakage current to the NMOS drain junction reverse leakage currents is therefore important to ensure that the NMOS devices are not damaged and is designed to be much less than 1. The drain of the NMOS transistor will therefore not see a substantial rise in voltage when the high voltage row select scan line is applied while the NMOS device is off.

6 Dot Matrix Design

In Fig. 9 is shown the pixel arrangement of the dot matrix display. The driving circuitry is integrated on the same die as the active pixels. Columns are swept at a fixed refresh rate, while the rows are energized depending on the required output. The controller can be fully integrated with the display, exploiting the capability of CMOS for the microdisplays and drive circuit to be heavily customized. Silicon based active elements also ensure operation over an extended temperature range. The full CMOS implementation results in ease of integration and configurability, significant reduction in cost, and the benefit of a wide operating temperature range.

The display is comprised of 512 pixels, arranged in an 8×64 pixel array. The row select lines are externally driven for this prototype and multiple rows can be enabled at any given time. Column select is controlled by a logic decoder on chip, with a 6-bit word, selecting one column at a time. The current configuration allows the sequential sweeping of columns while activating the required rows in order to display

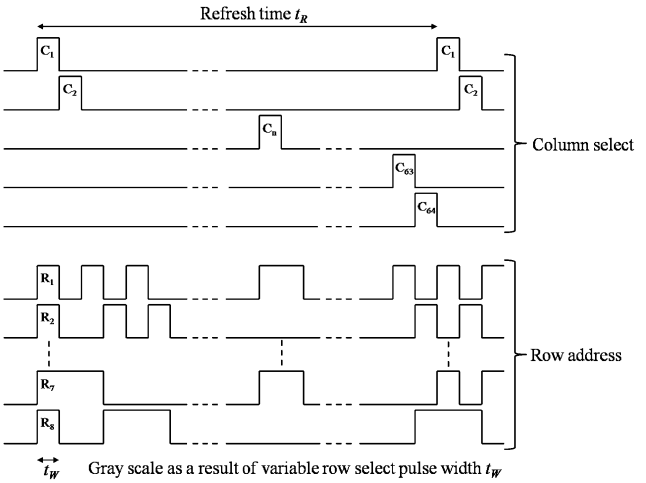

Fig. 10 Column and row select signals to generate display patterns.

an image or text on the display. The waveforms to address the pixels are shown in Fig. 10. As long as the refresh rate $= 1/t_R$ is more than approximately 40 Hz, the eye will observe the light emission as continuous.

The prototype depends on external control for the rendering of characters. The intensity of the pixel output can be modulated as a function of row signal duty cycle, varying the row address pulse width t_w in Fig. 10, thereby allowing grayscale images to be displayed. While not implemented as such on this prototype, the external controlling circuitry can easily be integrated on the same die as the display.

A photograph of the CMOS die is shown in Fig. 11, where two microdisplays are shown. In the figure, the 3.3 mm × 0.4 mm display area can be observed, as well as the row and column digital select circuits.

7 Results and Discussion

The experimentally observed visible image is shown in Fig. 12. The image itself is visible to the naked eye, and using a lens to view the alphanumeric microdisplay images, the 1.32 mm^2 active display area can easily be resolved. Unlike the display previously reported,[8,9] no image intensifier is required and the light generated by the CMOS display is sufficient for direct near-to-eye viewing purposes. As the transient response of the junctions in avalanche is very fast, the refresh rate of the screen is determined by the driving

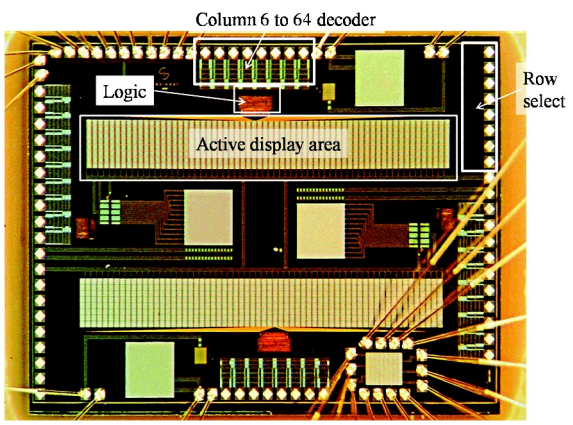

Fig. 11 Photomicrograph of CMOS die with microdisplay and logic circuits.

Fig. 12 An optical micrograph of the dot matrix display clearly shows the active pixels when illuminated.

Table 1 Electrical characteristics of the CMOS dot matrix display.

p^+n junction breakdown voltage	9.2 V
Display supply voltage	12 V
Current per point source	170 μA
Current per pixel	5.1 mA
Full column on maximum current	41 mA
Maximum power consumption (all pixels on)	492 mW
Refresh time t_R	23.4 ms
Refresh rate	42.8 Hz
Column/row select pulse width t_W	365 μs

transistor and controlled by the external peripheral circuitry. Motion rendering of text was also demonstrated by scrolling a predefined text message across the screen. Varying levels of intensity is shown in the region following the text in Fig. 12. The typical electrical characteristics of the prototype microdisplay are given in Table 1.

The radiation pattern of the CMOS light source with reflectors is shown in Fig. 13. It is evident that the reflector structure causes the visible light emission to be mostly in the vertical direction, thus improving the light being directed toward the eye in near-to-eye applications. From Fig. 13, it can be derived that the 50% viewing angle of the radiation pattern is 19-deg. This small viewing angle should not be a problem in the majority of near-to-eye display applications. Also shown in Fig. 13 is the radiation pattern for device structures with no reflectors. Due to the LOCOS nature of the device structure as shown in Fig. 1(a), light is generated along the sidewall of the LOCOS bird's beak resulting in a radiation pattern shown as a dotted line in Fig. 13. It is clear

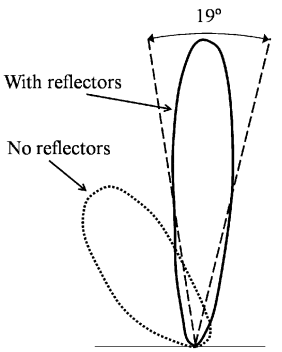

Fig. 13 Radiation pattern from the CMOS light source with and without integrated reflectors.

Table 2 CMOS LED microdisplay compared to generic OLED and LCoS technologies.

	CMOS LED	OLED	LCoS
Temperature	−50 °C to +125 °C	−40° C to +70° C	+10 °C to +70 °C
Response time	1 ns	1 μs	1 ms
Supply voltage	4 to 12 V	2 to 7 V	3 to 5 V
Technology	Emissive	Emissive	Reflective/ transmittive
Degradation	No	Yes	Yes
True black	Yes	Yes	No
Brightness	Low and variable	Variable	High
User configurability	Yes	No	No
Viewing angle	20°	160°	30° to 90°
Maximum frame rate	1 GHz	1 MHz	1 kHz
Minimum pixel size	5 μm	12 μm	5 to 8 μm
Cost	Very low	Medium	Medium
Power consumption	High	Low	Medium

that the reflectors are needed to direct the light toward the vertical.

Using the photopic lumen/Watt data, as well as optical power measurements using a silicon based radiometer, the luminance level within the viewing angle was experimentally determined as 20 cd/m^2. In order to comfortably read data being displayed in relatively dark environments, it was experimentally determined that a photopic luminance level of 20 cd/m^2 is adequate.[18] These are the conditions we expect for our CMOS dot matrix data display in a near-to-eye application. The temperature characteristics of the CMOS display were also characterized, and it was determined that over the temperature range −50° C to +125° C, no significant degradation in optical output could be observed. These limits were set by our thermal test equipment and not by the device. It is expected that the temperature range of CMOS displays will be much wider than reported here.

In Table 2, the OLED, LCoS, and CMOS display technologies are compared with reference to a number of parameters. Compared to OLED and LCD displays, a fully integrated CMOS microdisplay does have a number of attractive advantages, especially considering cost, reliability, configurability, temperature range of operation, and frame rate.

The cost benefits and flexibility of CMOS as a display platform are particularly attractive. The widespread use of CMOS integrated circuits, added to the favorable cost, robustness and maturity of the technology, may lead to interesting applications in the microdisplay environment. Having peripheral display capabilities on a CMOS die itself can be very useful, such as in diagnostic displays on integrated circuits.

Another advantage of the CMOS display is the fact that the pixels can be switched very fast. This makes the combination of display/data transfer using the same device a very interesting possibility.[19] The light emission spectrum, shown in Fig. 3, covers the visible region for display, as well as the near infrared region for data transfer.

8 Conclusions

The 512 pixel dot matrix display was configured in 8 rows and 64 columns, facilitating the display of alpha numerical characters and any other arbitrary graphic of the same format. A single pixel is composed from a number of point sources arranged in a square array. Each point source is optimized for optimal current density during avalanche breakdown, and light emission is further enhanced utilizing light directing structures integrated into the process back end stack, thereby improving both internal quantum efficiency and light extraction efficiency, respectively.

It was demonstrated that avalanche electroluminescence in reverse biased *pn* junctions in a standard CMOS technology, with no changes to the process or any post processing, can be used for microdisplay applications in low illumination settings. The perceived luminance of the microdisplay by the human eye was 20 cd/m^2, a luminance level at which the display data can be comfortably read in relatively dark environments.

Another advantage of this technology was demonstrated, namely the fast switching speed of the light emitting devices. A modulation frequency of 350 MHz was experimentally achieved, with limitations being the driving circuitry. This high modulation frequency may lead to interesting applications where optical display and data transfer functions are integrated into one array.

Future research possibilities include the optimization of the back end light directing structures for different circumstances, as well as improving the internal quantum efficiency of the light sources itself using reach-through techniques.[6,7,15] We expect a further factor 5 to 10 improvement in external power efficiency utilizing these methods, as well as a reduced supply voltage of 6 V.

Acknowledgments

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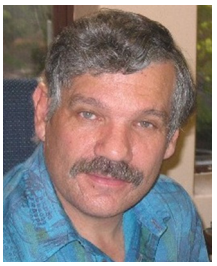

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