DESIGN APPROACH TO CMOS BASED CLASS-E AND CLASS-F POWER AMPLIFIERS

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Abstract: This paper presents the design flow for an integrated power amplifier. The flow is presented as a software routine. For a given set of amplifier specifications and CMOS process parameters, the routine computes the passive component values for a Class-E or Class-F based power amplifier. The routine includes the matching network for standard impedance loads. The routine also provides its user with a spiral inductor search algorithm, which can be used to generate layouts of inductors with Q-factors optimised at a desired frequency. For a typical power amplifier design case where several amplifiers are designed for application over different channels, the routine presented in this paper contributes by streamlining the design flow. The operation of the software routine was demonstrated by simulations in Austriamicrosystems 0.35 μm single-supply process for a 14 dBm, 2.4 GHz power amplifier design.

Keywords: Power Amplifier, CMOS, spiral inductor, Class-E amplifier, Class-F amplifier, impedance matching, SPICE netlist.

1. INTRODUCTION

The power amplifier (PA) technology has matured rapidly over recent years and has become highly integrated into several process technologies including SiGe BiCMOS, CMOS and GaAs [1]. Original PA designs were based around metal-oxide semiconductor (MOS) transistors, but after the introduction of a bipolar transistor with a wide-gap emitter, or HBT, bipolar transistors emerged as a preferred choice because of their higher gain and current densities at radio frequencies (RF). This resulted in transmitter systems that included at least two ICs in their implementation: a silicon CMOS based front end and, usually, GaAs based PA, which made them bulky and expensive. In the first decade of this century, SiGe HBT devices have emerged as an alternative to GaAs because they are able to bridge this integration gap by including both MOS transistors and HBTs on one die, which as a result reduces the cost of transmitter manufacturing. The costs can however be reduced by disregarding HBTs and implementing PAs in pure silicon CMOS processes using only MOS transistors.

In many RF modulation schemes, it is necessary to perform rapid design of several PAs in order to ensure the operation of a system over different channels of the same band. One such system is presented in [2], where transmission occurs over a number of channels in 2.4 GHz Industrial, Scientific and Medical (ISM) band. Additional to active devices (transistors), a number of passive components (inductors and capacitors) are included in PA design. When drawing mask layers on silicon wafer (layout design), designing of inductors poses a special problem, because the more affordable electronic design automation (EDA) software packages are not provided with built-in procedures for extraction of inductor netlist and layout from their models in schematics. This drawback requires manual modelling of inductors for the post-layout simulations. Inductor modelling becomes particularly important in the design of PAs at RF, due to the fact that even small differences between actual and designed values of inductance can strongly affect the centre frequency, gain or efficiency of an amplifier. Often, these mismatches can only be seen after the fabrication of the chip is completed, thus introducing additional unnecessary chip fabrication iterations which increase the design costs.

In this paper, a new design methodology for the rapid design of CMOS Class-E and Class-F PAs [3] is proposed. For a given set of specifications such as PA bandwidth, centre frequency and class of operation, the best possible PA is found and designed. This method is coined as a software routine. The same routine determines geometry of a spiral inductor that gives the highest possible quality factor, using process parameters for a particular process. Extracted layout and netlist can be exported by the routine and imported into layout design software for correct layout-level modelling. This work is the expansion of the work reported in [4].

To verify this software routine, Class-E and Class-F PAs have been designed and simulated in the C35 (0.35 μm CMOS) process from Austriamicrosystems (AMS).

2. POWER AMPLIFIER

2.1 Background

Class-E amplifiers [5] and Class-F amplifiers [6] have been used in communication ever since they were theorized in the nineteen-seventies. They are classified as switching amplifiers and as such they can exhibit efficiencies close to 100%.

2.2 Class-E Design Equations

Class-E amplifier uses combination of a series resonator and a shunt capacitor to shape the drain voltage and current waveforms in order to deliver the maximum power to the load. A single ended Class-E PA with matching is shown in Figure 1 [5]. Simple PA analysis can be performed if the following is assumed: inductance of the RF choke (*RFC*) L_1 is very high; output capacitance of the transistor is independent of the switching voltage and it can be included in C_1; and transistor is an ideal switch with zero resistance and zero switching time, open for half of the signal period. From [5], the value of the optimum load resistance to deliver the highest power to the load $P_{out\max}$ with peak voltage equal to supply voltage ($v_{peak} = V_{DD}$) is:

$$R_L = \frac{2}{\pi^2/4+1}\frac{{V_{DD}}^2}{P_{out\max}} = 0.577\frac{{V_{DD}}^2}{P_{out\max}} \tag{1}$$

For the desired Q-factor of the output resonant tank Q_L, inductance L_2 can be calculated:

$$L_2 = \frac{Q_L R_L}{2\pi f} \tag{2}$$

Where:

$f = f_o$ = the centre frequency of the channel

Shunt capacitance C_1 is given by:

$$C_1 = \frac{1}{2\pi f R_L\left(\pi^2/4+1\right)(\pi/2)} = \frac{1}{5.447(2\pi f R_L)} \tag{3}$$

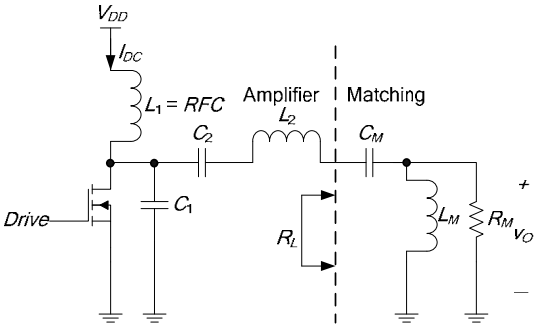


Figure 1: Complete Class-E PA schematic

Resonant capacitance C_2 is given by:

$$C_2 = \frac{1}{(2\pi f)^2 L_2}\cdot\left(1+\frac{1.42}{Q_L-2.08}\right) = C_1\left(\frac{5.447}{Q_L}\right)\cdot\left(1+\frac{1.42}{Q_L-2.08}\right) \tag{4}$$

2.3 Class-F Design Equations

Class-F amplifier includes waveform-shaping circuitry in its output network that shapes drain waveforms in such a way that load appears to be short at even harmonics and open at odd harmonics. As a result, the ideal drain voltage waveform approximates a square wave, while the drain current waveform approximates a half-sine wave. Shaping of waveforms can be done by means of transmission lines, but this is not a practical implementation for the low-gigahertz integration. Instead, several passive resonators are used. Monolithic implementations of the Class-F amplifiers would require an infinite number of resonators to correctly shape output waveforms. Most real life integrated Class-F amplifier implementations consider only a few harmonics, usually two or three. Figure 2 shows the Class-F PA, where bottom resonator constitutes the third harmonic peaking circuit and top two resonators constitute the amplifier with the resonators up to the fifth harmonic [7]. In this circuit, the tank at $3f_o$ provides an open circuit at $3f_o$ and short circuit at $2f_o$, whilst the tank at $5f_o$ provides an open circuit at $5f_o$ and short circuit at $4f_o$. Theoretical efficiencies for the two circuits are 81.7 % and 90.5 % respectively [8].

Similar to the case of the Class-E PA, the optimum load resistance can be determined [8]:

$$R_L = \frac{{\gamma_V}^2{V_{DD}}^2}{2P_{out\max}} \tag{5}$$

DC current needed for correct waveform shaping is given by:

$$I_{DC} = \frac{\gamma_V V_{DD}}{\gamma_I R_L} \tag{6}$$

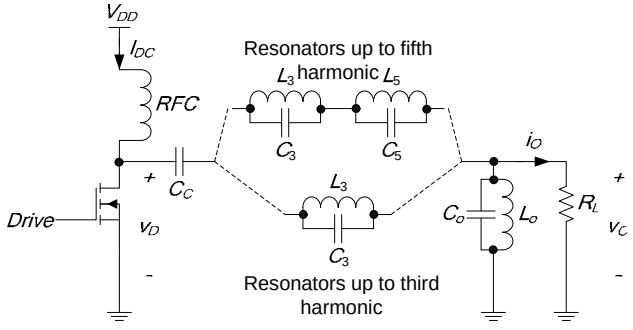


Figure 2: Class-F PA circuits with resonators up to third or fifth harmonics

Peaks of the drain voltage and current waveforms are given by:

$$v_{Dm} = \delta_V V_{DD} \tag{7}$$

And:

$$i_{Dm} = \delta_I I_{DC} \tag{8}$$

Coefficients γ_V, γ_I, δ_V and δ_I are maximum efficiency coefficients and are defined in Table I [8]. There is no generic equation that can relate L_o, L_3 and L_5 to other quantities, except to resonant capacitors (C_o, C_3 and C_5), which can be calculated, if the values for the inductors are chosen, by:

$$C_i = \frac{1}{(2\pi f_i)^2 L_i} \tag{9}$$

Where:

$i = o$, 3 or 5

Capacitor C_C is a coupling capacitor of an arbitrary value.

Table I: Maximum-Efficiency Waveforms Coefficients [8]

Coefficient	Value (Resonators up to third-harmonic)	Value (Resonators up to fifth-harmonic)
γ_V	1.1547	1.2071
δ_V	2	2
γ_I	1.4142	1.5
δ_I	2.1863	3

2.4 Design Algorithm

PA is designed around a single NMOS. Several input parameters are needed for the Class-E and Class-F design algorithm to converge successfully. These include the centre frequency of the channel (f_o), output power (P_{out}) and supply voltage (V_{DD}). In the case of Class-E design, loaded Q-factor (Q_L) is also required, and in the case of Class-F design, L_o, L_3 and L_5 must be specified. Centre frequency is determined by the specifications of the transmitter system of which the PA is a part. Output power (P_{out}) is also determined by the transmitter system specifications. The higher the output power requirement, the smaller the load (R_L) will have to be, which will pose higher demands on the output impedance matching. High output power can also result in the need for a higher supply voltage. Supply voltage can be arbitrarily chosen by the designer, but the choice must be constrained to prevent the transistor from entering the breakdown region. Quality factor is the Q-factor of the series resonator created by the inductance L_2 and capacitance C_2 of Class-E stage. The Q-factor can be chosen freely by the PA designer, but there is a tradeoff between high efficiency and power (low Q_L) on one side, and total harmonic distortion (THD) of the output signal on the other (high Q_L), which needs to be considered. A plausible Q-factor is in the range of 5 to 10 [9]. If the emphasis is on efficiency, a lower Q_L can be chosen and harmonics can be removed by additional filters at the output of the amplifier [5]. A narrowband output matching network can serve for this purpose.

The Class-E design algorithm utilizes (1) through (4) to calculate R_L, L_2, C_2 and C_1. DC current (I_{DC}), peak transistor voltage and current are also presented as the outputs of the software program. The Class-F algorithm utilizes (5) to (9) to calculate R_L, capacitors C_o, C_3 and C_5 and the required voltages and currents. As specified before, inductor values are chosen by the designer. The gain of both Class-E and Class-F output stages depends on the width of the RF NMOS available for specific design. In principle, very wide transistors should be used to support high power gains at high operating currents at RF frequencies. It is the responsibility of the designer to support the input of the PA with correct impedance matching and biasing depending on the available gain.

3. SPIRAL INDUCTOR

3.1 Background

Traditionally, capacitor and resistor implementations are easily accomplished in CMOS and these components are almost exclusively fabricated on-chip, which is not always the case with the inductors. Inductor size, low Q-factor of integrated passive inductors and other factors often result in alternative implementations, including external inductors, active integrated inductors, microelectromechanical systems (MEMS) inductors and bond wires. These implementations are normally too complex to implement or make the PA devices too bulky and expensive, leaving the passive spiral inductors as a reasonable choice for integration with PAs.

A square spiral, shown in Figure 3, has become more popular over some other spiral geometries [10] since some IC processes constrain all angles to 90° [11], but it generally has a lower Q-factor than the circular spiral, which most closely resembles the common off-chip solenoid inductors. It is fully specified by the number of turns (n), the turn width (w) and two of the following: inner, outer or average of inner diameter (d_{in}) and outer

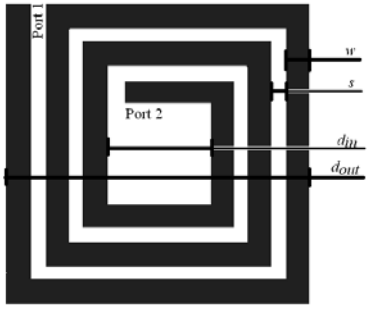


Figure 3: Square inductor spiral with geometry parameters shown

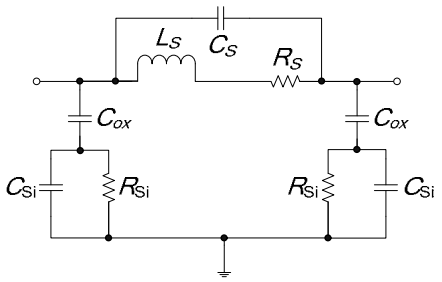


Figure 4: Nine-component spiral inductor model [8]

diameter (d_{out}). The parameter s is a pitch between the turns of the spiral.

3.2 Inductor Model

A lumped single-π nine-component inductor model shown in Figure 4 is sufficient to accurately model spiral inductors for frequencies below resonance [10]. In this model, L_S is the inductance at a given frequency, R_S is the parasitic resistance and C_S is parasitic capacitance of the spiral inductor structure. C_{ox} is parasitic capacitance due to oxide layers directly under the metal inductor spiral. Finally, C_{Si} and R_{Si} represent parasitic capacitance and resistance due to the silicon substrate, respectively.

The topology shown in Figure 4 correctly models the parasitic effects of the metal spiral and the oxide below the spiral, as well as for the substrate effects, but does not model the distributive capacitive effects.

The series inductance is calculated by data-fitted monomial expression that results in an error typically not greater than 3%. It has been developed by curve fitting over a family of 19000 inductors [10]. Inductance in nanohenries (nH) is calculated as

$$L_S = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \tag{10}$$

Where:

$\beta = 1.62 \cdot 10^{-3}$
$\alpha_1 = -1.21$
$\alpha_2 = -0.147$
$\alpha_3 = 2.40$
$\alpha_4 = 1.78$
$\alpha_5 = -0.030$

Different coefficients are used to implement other inductor geometries and/or symmetric inductor structures, which is beyond the scope of this paper. Although the inductance as specified in (10) is independent of frequency, parasitics add to the apparent value of inductance as well as decrease the quality factor of the inductor, as described later in this paper.

Parasitic resistance is dependent on the frequency of operation. At high frequencies, the resistance is dominated by the resistance resulting from eddy currents. Parasitic resistance depends on resistivity of the metal layer in which the inductor is laid out (ρ), total length of all inductor segments, as well as on the width and effective thickness (t_{eff}) of the inductor [12]:

$$R_S = \frac{\rho l}{w t_{eff}} \tag{11}$$

Where:

$$t_{eff} = \delta(1 - e^{-t/\delta}) \tag{12}$$

δ = skin depth dependent on frequency f via relation:

$$\delta = \sqrt{\frac{\rho}{\pi \mu_r \mu_0 f}} \tag{13}$$

And:

t = actual thickness of the conductor

μ_r = relative permeability of the metal layer

μ_0 = permeability of free space ($4\pi \cdot 10^{-7}$ H/m)

Parasitic capacitance is the sum of all overlap capacitances created between the spiral and all underpasses. For only one underpass of the same width as the spiral, the capacitance is equal to [12]:

$$C_S = nw^2 \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{14}$$

Where:

$t_{oxM1\text{-}M2}$ = oxide thickness between the spiral and the underpass

ε_{ox} = dielectric constant of the oxide layer between the two metals

The oxide and substrate parasitics are approximately proportional to the area of the inductor spiral ($l \cdot w$), but are also highly dependent on conductivity of the substrate and operating frequency. In order to calculate the oxide capacitance C_{ox} and substrate capacitance C_{Si}, effective thickness (t_{eff}) and effective dielectric constant (ε_{eff}) of either oxide or substrate must be determined. Effective thickness is in this case is calculated as [13]:

$$t_{eff} = w\left[\frac{w}{t} + 2.42 - 0.44\frac{t}{w} + \left(1 - \frac{t}{w}\right)^6\right]^{-1}, \text{ for } \frac{t}{w} \le 1 \tag{15}$$

And:

$$t_{eff} = \frac{w}{2\pi}\ln\left(\frac{8t}{w} + \frac{4w}{t}\right), \text{ for } \frac{t}{w} \ge 1 \tag{16}$$

Equations (15) and (16) are valid for both oxide and substrate. Effective dielectric constant is determined as:

$$\varepsilon_{eff} = \frac{1+\varepsilon}{2} + \frac{\varepsilon - 1}{2}\left(1 + \frac{10t}{w}\right)^{-1/2} \quad (17)$$

Then:

$$C_{ox} = \frac{wl\varepsilon_0\varepsilon_{effox}}{t_{effox}} \quad (18)$$

And:

$$C_{\mathrm{Si}} = \frac{wl\varepsilon_0\varepsilon_{eff\mathrm{Si}}}{t_{effox\mathrm{Si}}} \quad (19)$$

Similarly, to calculate R_{Si}, effective thickness (t_{eff}) and effective conductivity (σ_{eff}) of substrate are needed. As for the capacitance, effective thickness is given by Equation (15), and effective conductivity can be obtained from [13]:

$$\sigma_{eff} = \sigma\left[\frac{1}{2} + \frac{1}{2}\left(1 + \frac{10t}{w}\right)^{-1/2}\right] \quad (20)$$

Where:

σ = substrate conductivity

Therefore:

$$R_{\mathrm{Si}} = \frac{t_{eff\mathrm{Si}}}{\sigma_{eff} wl} \quad (21)$$

3.3 Quality Factor

Quality factor is the basic characterisation technique for inductors. For a single-π model, the inductor Q-factor can be calculated as [14]:

$$Q = \frac{\omega L_S}{R_S} \cdot \frac{R_P}{R_P + \left[\left(\omega L_S / R_S\right)^2 + 1\right]R_S} \cdot \left[1 - \left(C_P + C_S\right)\cdot\left(\omega^2 L_S + \frac{R_S{}^2}{L_S}\right)\right] \quad (22)$$

Where:

$$R_P = \frac{1}{\omega^2 C_{ox}{}^2 R_{\mathrm{Si}}} + \frac{R_{\mathrm{Si}}\left(C_{ox} + C_{\mathrm{Si}}\right)^2}{C_{ox}{}^2} \quad (23)$$

$$C_P = C_{ox} \cdot \frac{1 + \omega^2\left(C_{ox} + C_{\mathrm{Si}}\right)C_{\mathrm{Si}} R_{\mathrm{Si}}{}^2}{1 + \omega^2\left(C_{ox} + C_{\mathrm{Si}}\right)^2 R_{\mathrm{Si}}{}^2} \quad (24)$$

And:

$$\omega = 2\pi f \quad (25)$$

Low Q-factors of spiral inductors are attributed to the losses of the inductor spiral, substrate loss in the semiconducting silicon substrate and self resonance loss due to total capacitance $C_S + C_P$.

3.4 Inductance Search Algorithm

Although spiral inductors are a good choice for exclusively on-chip PAs, their usage is not as straight forward. All spiral inductor parameters are interrelated; hence a single parameter to be increased or decreased to change the inductance value in a set manner cannot easily be identified. This complexity of spiral inductor models is one of the reasons why it is a common practice to use an iterative process in their design [4]. As part of this process, one guesses the geometry parameters that could result in the required inductance (and Q-factor) value, calculates inductance and other relevant parameters given guessed parameters, thereafter repeating this process until satisfied with the performance of the inductor.

In this section, a new non-iterative routine is proposed that will result in an inductor of the specified value, with the highest possible Q-factor, occupying a limited area, and using the predetermined technology layers. The intention behind this routine is to find a square inductor geometry resulting in the highest Q-factor for the specified inductance given some design constraints. For accurate inductor modelling, the process parameters and frequency of operation of the inductor must be known. Geometry needs to be constrained by the minimum input diameter, maximum output diameter, and minimum turn spacing and turn width. The search algorithm looks into a range of geometries and identifies a geometry that results in the required inductance within certain tolerance by using (10). More than one geometry can result in the correct inductance at a given frequency and the geometry that gives the highest Q-factor is chosen by the algorithm as its output. Accuracy of the algorithm depends on the tolerance for the required inductance values and on the search grid resolution. A simplified flow diagram of the inductance search algorithm is shown in Figure 5.

3.5 Verification

In order to verify the correctness of the inductance search algorithm, eleven inductors were designed using parameters for the C35 BiCMOS process from AMS. The geometries of those inductors were the same as the inductors designed and measured by AMS. Their predicted behaviour was compared to the results obtained experimentally by the foundry, as well as to the results obtained by means of EM simulations. Comparison of the Q-factors of these inductors at their optimal frequencies is shown in Figure 6. The average relative errors between calculated values, values measured by the foundry and EM simulated values were determined to be less than 5 % for both inductance and quality Q-factor.

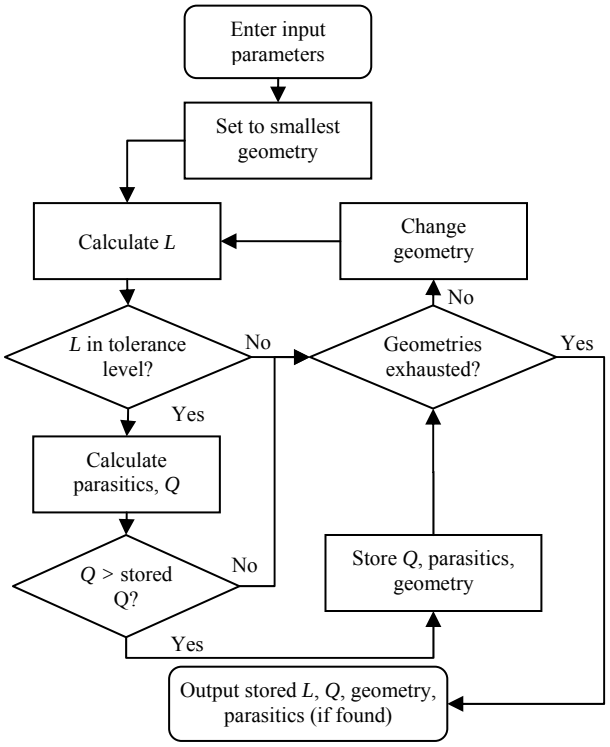


Figure 5: Flow diagram of the inductance search algorithm.

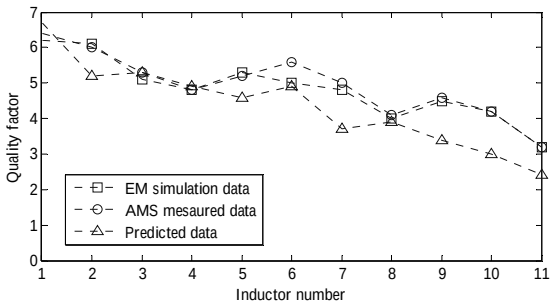


Figure 6: Comparison of Q-factors of eleven M3 inductors

4. PA DESIGN PROGRAM

Class-E and Class-F PA design algorithms as well as the inductor search algorithm are included into a C# program used to perform complete PA system integration.

The primary user interface of the software is shown in Figure 7. In this dialogue, the user is required to enter parameters for the Class-E or Class-F PA design. On the click of the `Calculate` button, either the Class-E or Class-F design subroutine, described in Section 2, is executed. After this, the user has a choice to perform output impedance matching to the standard impedance of 50 Ω. The program employs impedance matching using discrete components. Three impedance networks are available: a wideband two-component network (L network, Figure 1) and two narrowband three-component networks (T and Π networks). Finally, the user can choose to invoke another user form which will utilize the inductor search algorithm to design spiral inductors for all the inductors (including the matching

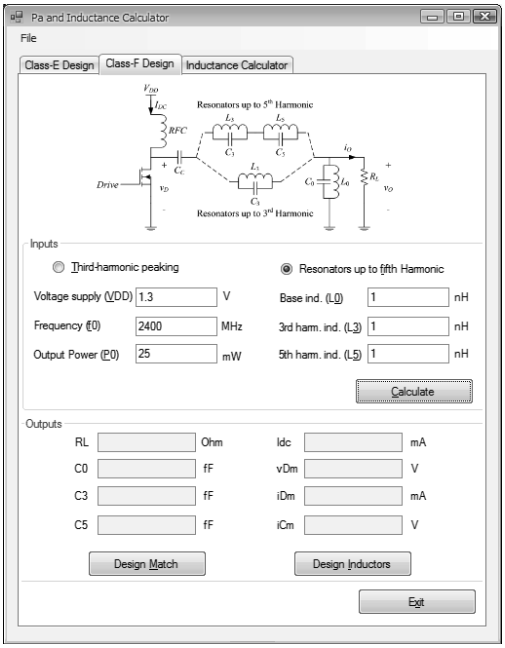


Figure 7: Primary user interface of the PA design software

ones), required for the full PA design. Process parameters can either be specified in a separate screen, or they can be loaded from a configuration file. For the AMS CMOS process, the process parameters for both 3-metal and thick-metal inductors are included. Furthermore, the program can also export SPICE netlist of each inductor structure, complete with the inductance value and the parasitics, and a GDSII file, which contains the mask geometry information of any inductor [15]. The netlist can be used in SPICE simulations without the need for one to draw the schematic of the inductor with its parasitics in the schematic editor. A typical inductor SPICE netlist is shown in [4]. The GDSII file can be imported into the layout software to eliminate the need for manually drawing inductor layout structures.

5. SIMULATION

One Class-E and one Class-F PA were designed using the program described in Section 4 in the AMS C35 process. For both PAs, an RF NMOS transistor was used with transistor width-to-length ratio equal to (200 μm)/(0.35 μm). The design was accomplished at 2.4 GHz to enable operation in the ISM band. A conservative value for output power (25 mW or 14 dBm) was chosen.

For the Class-E PA simulation, a moderate quality factor of the resonant tank (Q_L = 5) was used. The design was powered from 0.8 V in order to make sure that the transistor stays well away from its breakdown region. For the same design, an L-network was used for the matching for simplicity, as shown in Figure 1. Table II lists the calculated values for all required Class-E PA quantities.
For Class-F PA simulation, the circuit with resonators up to the fifth harmonic was chosen over the third-harmonic peaking circuit for better waveform shaping. The supply used in this stage was 1.3 V, higher than for Class E,

because the swing on the drain waveform is about 1.8 times lower, allowing for higher voltage supplies to be used. Such a high voltage supply also allowed for matching to be excluded without loss in output power. Table III lists the calculated values of all required Class-F PA quantities.

Output waveforms (v_O) of two simulated systems are shown in Figure 8 and Figure 9, respectively. In both cases, waveforms were shown for designs using both ideal and spiral inductors. The frequency response for the two PAs is shown in Figure 10, showing the relation between drains and output voltage waveforms. Table IV shows geometries, parasitics and Q-factor of thick-metal inductors L_2 and L_M used in Class-E amplifier design, as well as 1 nH inductors used in Class-F amplifier design, determined by the inductance search algorithm and used in simulations using spiral inductors. The layout of 4.9 nH created by importing of the GDSII file by layout design software is shown in Figure 11. Furthermore, it has been assumed that the RFC inductor for both designs is external to the integrated system, and has a very high inductance value.

Table II: Calculated Quantities for Class-E PA

Parameter	Value	Unit	Parameter	Value	Unit
R_L	14.8	Ω	I_{DC}	31.2	mA
C_2	1.33	pF	L_M	2.15	nH
L_2	4.90	nH	C_M	2.94	pF
C_1	0.82	pF	R_M	50	Ω

Table III: Calculated Quantities for Class-F PA

Parameter	Value	Unit	Parameter	Value	Unit
R_L	50	Ω	C_3	0.49	pF
L_o	1	nH	L_5	1	nH
C_o	4.4	pF	C_5	0.18	fF
L_3	1	nH	I_{DC}	21.2	mA

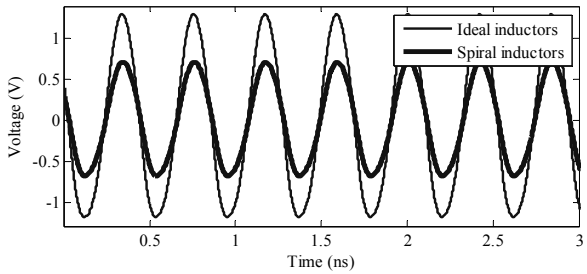


Figure 8: Output voltage waveforms for Class-E PA with ideal and spiral inductors.

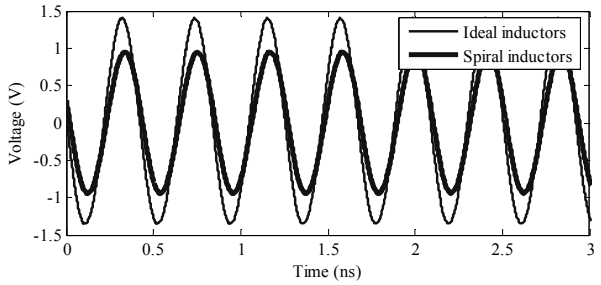
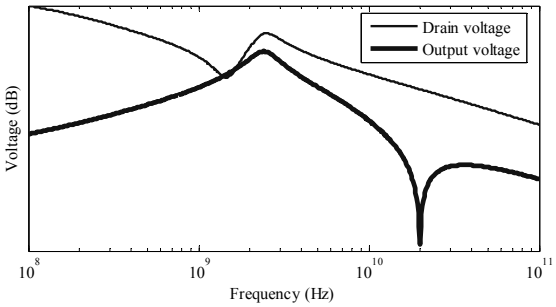
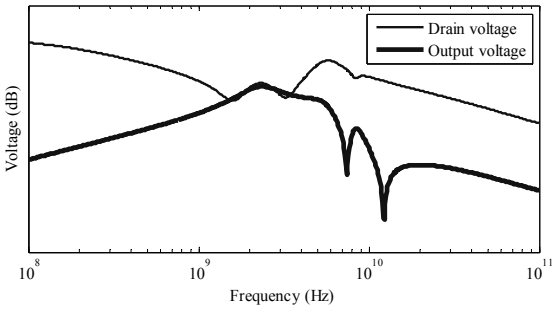


Figure 9: Output voltage waveforms for Class-F PA with ideal and spiral inductors.



(a)



(b)

Figure 10: Frequency domain representation of drain and output voltage waveforms for (a) Class-E PA (b) Class-F PA.

With ideal inductors, the output voltage has the peak of

Table IV: Geometry Parameters and Parasitics of Inductors

Parameter	Value (L_2)	Value (L_M)	Value (1 nH)	Unit
L_S	4.93	2.16	1.00	nH
L_{self}	4.38	2.01	0.94	nH
Q	6.8	9.96	13.0	-
w	11	25	48	μm
s	2	2	2	μm
d_{in}	121	206	90	μm
d_{out}	221	310	286	μm
n	4	2	2	-
R_S	5.26	1.77	0.72	Ω
C_S	17.1	44.2	163	fF
C_{Si}	82.6	73.9	67.0	fF
C_{ox}	153	209	280	fF
R_{Si}	257	287	315	Ω

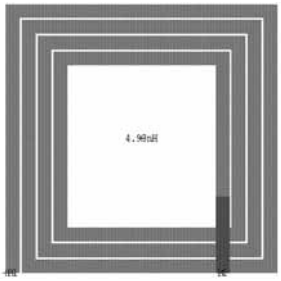


Figure 11: Layout of 4.9 nH inductor used in Class-E PA design.

about 1.2 and 1.4 V for Class-E and Class-F stages respectively, which is equivalent to powers of about 11.6 and 12.3 dBm. This is roughly 2 dBm decrease from the value the design was intended for. This can be attributed to the fact that transistor was assumed to be an ideal switch in both cases. With spiral inductors, Class-E amplifier has the peak of about 0.75 V, which results in the power of about 7.5 dBm. For Class-F amplifier, the peak is about 0.9 V, giving the power of 9.1 dBm. This is a further 3.5 dBm decrease in power for both classes, which can be attributed to the presence of parasitics in inductors. Although the search algorithm finds inductors with the highest Q-factors possible within the space and technology constraints, the Q-factors are still fairly low and highly influential to the total performance of the integrated PA.

For Class-E stage, the current drawn from the supply is 26.3 mA, slightly lower than the predicted value, resulting in efficiency of 64 % for ideal design and 24 % for the practical design with spiral inductors. For Class-F stage, the DC current drawn from the supply is 23.5 mA, which corresponds to the predicted value, resulting in drain efficiencies of 64 % for ideal design and 27 % for the practical design with spiral inductors. Evidently, a loss in efficiency of the PA is present in the design involving spiral inductors.

6. CONCLUSION

In this paper, a software routine for the design of CMOS PAs was presented. Apart from determining the optimum values of passives needed for correct waveform filtering for Class-E and Class-F PAs, the program handles output impedance matching and spiral inductor design. The inductor search algorithm has been used for filtering and matching inductor design. This allowed for obtaining of spiral inductors with Q-factors that are the highest within geometry and process constraints. The streamlined use of the software-aided design described in this paper was demonstrated by designing two complete 2.4 GHz PAs, which were subsequently simulated using the AMS C35 process. While the results were short of the goal parameters of the amplifier, the value of this paper is aimed to provide a starting point for more detailed analogue simulation of Class-E and Class-F amplifiers.

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