MATHEMATICAL MODELLING OF THE LC-LADDER AND CAPACITIVE SHUNT-SHUNT FEEDBACK LNA TOPOLOGY

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Abstract: In this paper a new low noise amplifier configuration is proposed to achieve wideband operation. This configuration consists of an LC-ladder filter and a common-emitter stage employing shunt-shunt capacitive feedback to realize wideband matching. Design equations for this configuration are derived, as well as equations for the important performance measures namely noise figure, gain and IIP3. The results of a design for achieving typical low noise amplifier specifications in the ultra-wideband are calculated from these equations and plotted. Without any optimization S_{11} of less than -10 dB over the entire frequency band and a minimum noise figure of 2.7 dB are predicted when achieving S_{21} of 20 dB. These results indicate that very good performance can be attained through the use of this technique. Simulations were also done to verify the calculated results.

Key words: low noise amplifier, ultra-wideband, input matching, LC-ladder filter, capacitive feedback.

1. INTRODUCTION

Low noise amplifiers (LNAs) play a vital role in any wireless receiver since it dominates the noise figure (NF) of the entire system [1] and as such has remained an active area of research for many years. While LNA design techniques in narrowband applications have been researched for some time, wideband techniques have received more thorough investigation in the last few years as well; especially since the approval of the application of ultra-wideband (UWB) technology for commercial use in 2002. The ultra-wideband ranges from 3.1 to 10.6 GHz and the implementation of UWB systems and its sub-systems has been a challenge for integrated circuit designers since its approval [2].

Wideband LNAs typically require a 50 Ω input impedance over the entire bandwidth to efficiently interface with antennas. A flat gain is also required over the entire frequency band of interest, as well as a low average NF. This poses unique design challenges compared to the narrowband case in addition to any further linearity or power consumption requirements.

Although improvements in transistor speed and device scaling has served to improve noise performance of LNAs over the past years, the NF ultimately depends on the input matching network [3]. Various traditional matching schemes exist; however the shortcomings of these techniques have been discussed in [4], and it was shown that narrowband techniques are often applied directly to wideband design resulting in suboptimal performance. Therefore a new implementation is proposed that combines a common-emitter (CE) amplifier employing capacitive shunt-shunt feedback and a LC-ladder configuration at the input providing wideband matching.

This work describes the design principles of this implementation in detail and straight forward design equations are also derived. A LNA designed for operation over the UWB is presented to illustrate the results that can be obtained using this configuration, based on the mathematical analysis presented; this is also validated with simulation results. Designing for the UWB was an arbitrary selection however since, as will be shown, such LNAs can be designed for an arbitrary bandwidth.

2. DESIGN PRINCIPLES

2.1 Input matching

Wideband input matching is achieved through the use of a fourth order LC-ladder filter allowing the realization of an arbitrary wide matched bandwidth at the input [5]. This is combined with the capacitive shunt-shunt feedback technique [2], [6] shown in Fig. 1, which is used to generate the resistance and capacitance of the series RLC part of the circuit, rather than using inductive emitter degeneration.

As shown in Fig. 2 the LC-ladder consists of four reactive elements where C_2 and L_1 determine the lower cut-off frequency of the matched band and C_1 and L_2 the upper cut-off frequency. The appropriate values for these components are given by [5]

$$L_1 \approx \frac{R_S}{2\pi f_L} \quad and \quad C_2 \approx \frac{1}{2\pi f_L R_S} \qquad (1a)$$
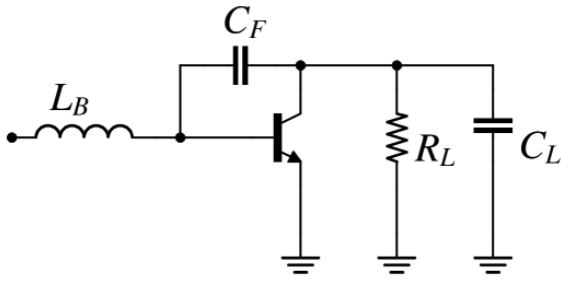
Figure 1: Schematic of a capacitive shunt-shunt feedback amplifier used to produce an equivalent series RLC circuit [2].

$$L_2 \approx \frac{R_S}{2\pi f_H} \quad and \quad C_1 \approx \frac{1}{2\pi f_H R_S} \qquad (1b)$$

where R_S is the source resistance and f_L and f_H the lower and upper cut-off frequencies of the matched bandwidth respectively.

A benefit of using this configuration is that it takes advantage of what would in many cases be regarded as unwanted parasitic components and incorporates them into the matching network. The shunt capacitor C_1 can be implemented as the pad capacitance, and the shunt inductor L_1 as the DC bias choke. Both inductors L_1 and L_2 are implemented using spiral inductors for which good optimization techniques exist [7]. The series capacitance however is derived from the equivalent capacitance resulting from the feedback network.

Through straight forward small signal analysis it is easily shown that, while $j\omega R_L C_L \ll 1 + g_m R_L$, the equivalent capacitance and resistance at the base of the transistor is respectively given by [2]

$$C_{eq} = C_2 = C_\pi + (1 + g_m R_L)(C_\mu + C_F)$$
$$= C_\pi + C_M \qquad (2a)$$

$$R_{eq} = \frac{R_L}{(1 + g_m R_L)}\left(1 + \frac{C_L}{C_{BC}}\right)\left(\frac{C_M}{C_\pi + C_M}\right)^2$$
$$\approx \frac{1}{g_m}\left(1 + \frac{C_L}{C_{BC}}\right) \qquad (2b)$$

With reference to Fig. 1 in these equations g_m is the transistor transconductance, C_π the base-emitter capacitance, C_μ the base-collector capacitance, and C_F an intentionally added capacitance in parallel with C_μ to increase the total base-collector capacitance (C_{BC}). R_L and C_L are the respective parallel connected load resistance and capacitance, including the input impedance of a
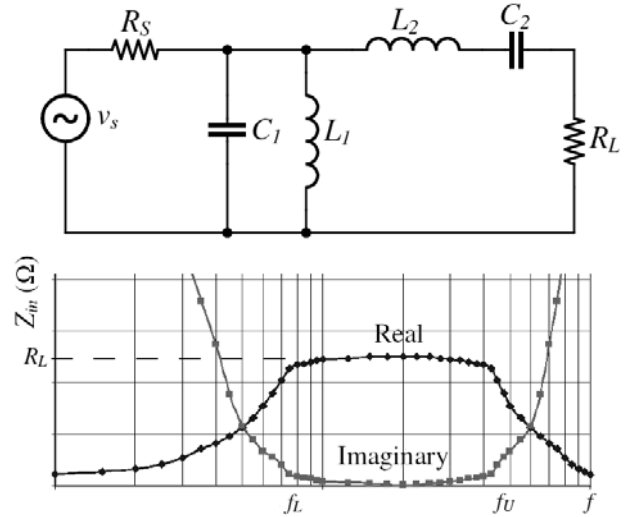

Figure 2: Fourth order LC-ladder filter used to generate an arbitrary wide resistive impedance [5].

following amplifier stage. The approximation of R_{eq} holds if $g_m R_L$ is much larger than one and the Miller-capacitance is much larger than C_π.

The result is similar to that achieved in [5] where inductive emitter degeneration was used to generate the series RLC circuit, however in this design the base-emitter voltage does not roll-off at 20 dB per decade. In the emitter degeneration case, the current flowing into the transistor is approximated as $v_S/(2R_S)$ over the band of interest. The voltage over the base-emitter capacitance and thus the base-emitter junction is then given by

$$v_\pi = \frac{v_s}{2R_S} \cdot \frac{1}{j\omega C_2},$$
$$= \frac{v_s}{2}\frac{f_L}{f} \qquad (3)$$

indicating the voltage roll-off [5].

In the capacitive feedback case however the transistor and feedback network, as opposed to the emitter inductor, is used to generate the resistive component and thus the voltage over the base-emitter junction is the voltage over both the equivalent resistance and capacitance, which results in

$$v_\pi = \frac{v_s}{2R_S}\left(R_S + \frac{1}{j\omega C_2}\right)$$
$$= \frac{v_s}{2}\left(\frac{j\omega R_S C_2 + 1}{j\omega R_S C_2}\right),$$
$$\approx \frac{v_s}{2} \qquad (4)$$

and is a decreasing function at -20 dB per decade from infinity to a corner at -6 dB at the lower cut-off frequency, from where the zero results in a constant voltage drop over the junction with frequency.

In this derivation the base series resistance (r_b) of the transistor was neglected, and thus it is worth noting whether this still applies in the super high frequency (SHF) range. The effect of this resistor becomes noticeable when the impedance of C_π drops at high frequencies, causing a greater portion of the input voltage to fall across r_b. This decreases the voltage gain by introducing a pole at

$$v_{be}' = \frac{1/j\omega C_\pi}{r_b + 1/j\omega C_\pi}$$
$$= \frac{1}{1 + j\omega C_\pi r_b} \tag{5}$$

However for a typical C_π of 40 fF and a base resistance of less than 50 Ω this pole is above 30 GHz and as such r_b can be safely neglected.

2.2 First stage gain

The gain of this amplifier stage, characterised as S_{21}, is given by

$$S_{21} = 2 \cdot A_{v,in} \cdot G_M \cdot Z_L, \tag{6}$$

where $A_{v,in}$ is the gain of the input ladder network, i.e. from the source to the base-emitter junction. G_M is the transconductance of the amplifier and Z_L the load impedance.

The complete transfer function of the ladder network is given by

$$A_{v,in} = \frac{Z_S}{R_S} \cdot \frac{Z_{T,in}}{Z_S + j\omega L_2 + Z_{T,in}}, \tag{7}$$

where a Norton and subsequent Thévenin transform was used to place the source in series with the impedance of the parallel RLC circuit (Z_S) comprised of R_S, L_1 and C_1. $Z_{T,in}$ is the total equivalent input impedance as defined in (2a) and (2b).

The transconductance and load impedance are given respectively by

$$G_M = g_m - j\omega C_{BC}, \tag{8}$$

$$Z_L = R_L \Big\| \frac{1}{j\omega(C_{BC} + C_L)} = \frac{R_L}{1 + j\omega R_L(C_{BC} + C_L)}. \tag{9}$$

Since the transfer function of the ladder network was shown to be approximately constant over the band of interest it is apparent that there is a single dominant pole at the output of the amplifier given by

$$\omega_{P1} = \frac{1}{R_L(C_{BC} + C_L)}. \tag{10}$$

Unfortunately a small collector current is required to generate the equivalent 50 Ω resistance (as shown in Section III), and as such a large R_L is typically required to achieve large gain. Therefore the pole is often within the band of interest resulting in a -20 dB per decade roll-off in the frequency response.

Even if this is not the case, the gain-bandwidth product (GBP) or f_T of the transistor will often not allow large gain for operation up to the high SHF range. If the gain is higher than f_T/f_H there will be a -20 dB per decade roll-off of gain regardless of the position of the output pole.

2.3 Gain flattening

From the preceding discussion it is desirable to equalize the gain of the amplifier by introducing a zero into the system to cancel the output pole of the first stage. This can be done by adding a second amplifier stage with an inductive load, resulting in the complete amplifier circuit shown in Fig. 3. The voltage gain of the second stage is

$$A_{v,2} = j\omega L_3 g_{m2}, \tag{11}$$

where g_{m2} is the transconductance of the second stage transistor and L_3 the load inductance. The overall gain can then be defined as

$$S_{21} = 2A_{v,in} \frac{R_{L1}(g_{m1} - j\omega C_{BC})(j\omega L_3 g_{m2})}{1 + j\omega R_{L1}(C_{BC} + C_{L1})} \tag{12}$$

where g_{m1} is usually sufficiently larger than the base-collector impedance for the frequency dependence of that term to be neglected.

If the second stage gain is designed to be unity at the peak of the first stage gain, the overall gain will have the value of that peak gain equalized over the entire band of interest. Alternatively, the overall gain can be distributed between the two stages with an arbitrary ratio and used to optimize the overall linearity or NF.
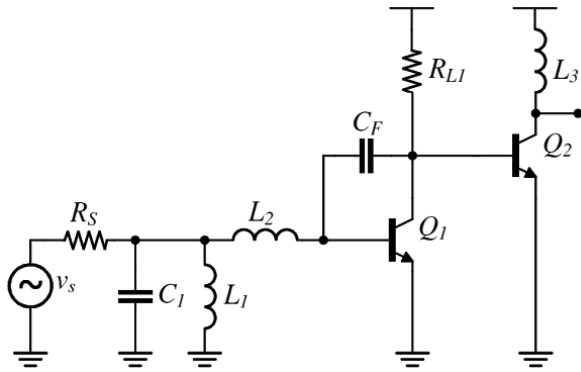
Figure 3: Schematic of the proposed amplifier showing the LC-ladder matching network, capacitive shunt-shunt feedback and the second amplifier stage used to generate a zero in the frequency response for pole-zero cancellation.

2.4 Additional gain stages

The LNA configuration of Fig. 3 provides wideband conjugate input matching as well as gain with a flat frequency response. Depending on the transistor process that is used it might however not be possible to achieve the desired gain specification. In such a case additional common-emitter stages employing resistive loads may be added to increase the overall gain further.

3. DESIGN EQUATIONS

For a given frequency band and gain specification, compact equations can be derived for the design of an amplifier using the configuration discussed in the previous section.

The frequency specification is met through proper selection of the reactive elements in the ladder input matching network. As an initial estimate (1a) and (1b) can be used; and through subsequent plotting of the various performance measures these values can be altered to optimize the design.

The characteristics of the first amplification stage are determined by the collector current (I_C) as well as three components: R_{L1}, C_{L1} and C_F in conjunction with the parasitic C_μ of the transistor. The load resistance together with the collector current is used to set the gain of the first stage.

In the design process this voltage gain (A_{v1}) is selected first. The equivalent capacitance used to synthesize C_2 is determined by C_F and A_{v1} and thus the equation for C_F can be derived from (2a) as

$$C_F = \frac{C_2 - C_{\pi 1}}{1 + A_{v1}} - C_{\mu 1}. \tag{13}$$

The equivalent resistance in (2b) is a function of the feedback and the load capacitance as well as g_m and thus can be used to derive an equation for I_C as

$$I_C \approx \left(1 + \frac{C_L}{C_{BC}}\right) \frac{V_T}{R_S}. \tag{14}$$

Although C_L also strongly affects R_{eq} it should not be used to alter R_{eq} but rather kept to a minimum to avoid making the dominant pole frequency even lower.

Once the collector current has been determined R_{L1} is set based on the initial selection of A_{v1}.

4. PERFORMANCE MEASURES

4.1 Noise figure

The circuit shown in Fig. 4 includes all the relevant noise sources of the first amplifier stage and could be used to calculate the NF. The analysis however is complicated by the presence of the feedback capacitance, as well as the R_S and R_1 noise sources which form part of the parallel RLC circuit. To simplify the final NF equation the equivalent circuit in Fig. 5 can be used.

Where shunt-shunt feedback is applied to an amplifier the equivalent noise voltage source is not affected [8] and is thus given by [9]

$$\overline{v_{EQ}^2} \approx \overline{v_{CE}^2} = 4kTr_b + \frac{2qI_C}{g_m^2} + \frac{2qI_C}{\beta_0} \cdot r_b^2$$
$$\approx 4kTr_b + \frac{2qI_C}{g_m^2} \tag{15}$$

where k is Boltzmann's constant, T is absolute temperature in degrees Kelvin and q is the electron charge; r_b is the base series resistance and β_0 is the DC current gain of the transistor.
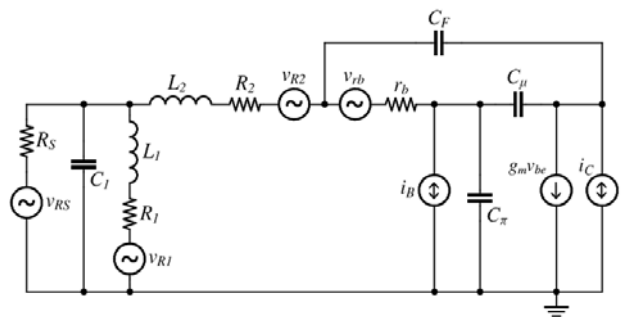

Figure 4: Equivalent circuit of the first amplification stage showing parasitic components and noise sources.
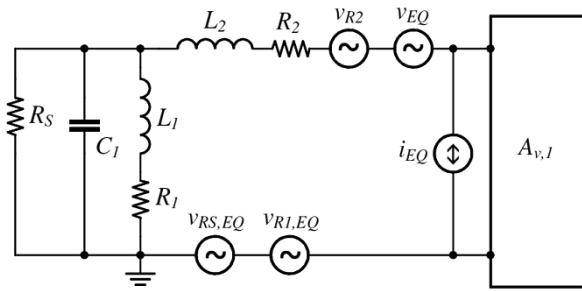
Figure 5: Equivalent circuit used in the derivation of the NF equation.

The equivalent noise current increases however due to the current flowing through the feedback network resulting from the equivalent noise voltage [8] and is given by [9]

$$\overline{i_{EQ}^2} \approx \overline{i_{CE}^2} + \left(\omega^2 C_F^2\right)\overline{v_{CE}^2}$$
$$= 2qI_C\left(\frac{1}{\beta_0} + \left(\frac{\omega(C_\pi + C_\mu)}{g_m}\right)^2\right) + \left(\omega^2 C_F^2\right)\overline{v_{CE}^2} \quad (16)$$

By first using a Norton and then Thévenin transformation the R_S and R_1 noise sources can be moved in series with the rest of the input loop as in Fig. 5 and results in

$$\overline{v_{RS,EQ}^2} = \frac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2} \quad and \quad \overline{v_{R1,EQ}^2} = \frac{|Z_S|^2}{|Z_1|^2}\overline{v_{R1}^2}, \quad (17)$$

where $Z_1 = R_1 + j\omega L_1$.

The noise factor of the first stage can now be defined as

$$F_1 = \frac{\overline{v_{\pi,veq}^2} + \overline{v_{\pi,ieq}^2} + \overline{v_{\pi,R1}^2} + \overline{v_{\pi,R2}^2} + \overline{v_{\pi,RS}^2}}{\overline{v_{\pi,RS}^2}}, \quad (18)$$

where each term represents the equivalent power spectral density of the respective noise sources over the base-emitter junction. From the discussion above with $Z_2 = R_2 + j\omega L_2$ the noise factor becomes

$$F_1 = 1 + \frac{\overline{v_{EQ}^2} + |Z_S + Z_2|^2\overline{i_{EQ}^2} + \frac{|Z_S|^2}{|Z_1|^2}\overline{v_{R1}^2} + \overline{v_{R2}^2}}{\frac{|Z_S|^2}{R_S^2}\overline{v_{RS}^2}}, \quad (19)$$

and with the further substitution of (15) and (16) and simple algebraic manipulation can be written as

$$F_1 = 1 + \left[\left(\frac{1}{|Z_S|^2} + \left|1 + \frac{Z_2}{Z_S}\right|^2\cdot|\omega C_F|^2\right)\overline{v_{CE}^2} + \left|1 + \frac{Z_2}{Z_S}\right|^2\overline{i_{CE}^2} + \frac{\overline{v_{R1}^2}}{|Z_1|^2} + \frac{\overline{v_{R2}^2}}{|Z_S|^2}\right]\cdot\frac{R_S^2}{\overline{v_{RS}^2}} \quad (19)$$

4.2 Linearity

Although NF and gain can be quantified relatively well using small signal analysis amplifier linearity, being a large signal phenomenon, is harder to evaluate. A Volterra-series can be used to analyze circuits operating in weak non-linearity [10], however the derivation of the Volterra-series is very laborious and offer little insight that cannot be gained through large signal circuit simulations. Therefore only an approximation that can be used as an initial estimate of the IIP3 is derived here.

The third order input intermodulation product (IIP3) voltage of a CE amplifier can be approximated as [11]

$$V_{IIP3(CE)} = 2\sqrt{2}V_T, \quad (20)$$

where V_T is the thermal voltage. Since the proposed amplifier consists of two cascaded CE stages in which the first stage acts as a pre-amplifier which reduces the linearity of the last stage, the final IIP3 voltage of the amplifier is given by

$$V_{IIP3(LNA)} = \frac{V_{IIP3(CE2)}}{A_{v,in}\cdot A_{v,1}},$$
$$\approx \frac{4\sqrt{2}V_T}{A_{v,1}} \quad (21)$$

resulting in

$$IIP3 = 10\log\left(\frac{16\cdot V_T^2}{A_{v,1}^2\cdot R_S}\cdot10^3\right) dBm. \quad (22)$$

5. RESULTS

To gain insight into the potential performance of this configuration an amplifier with S_{21} of 20 dB was designed using the equations derived in this paper for an arbitrary bandwidth of 3 to 10 GHz (the UWB). The IBM 8HP BiCMOS process with transistor emitter lengths of 12 μm was assumed. The component values that were obtained are given in Table 1 and the critical performance measures as calculated are plotted in Fig. 6 to Fig. 9.

Table 1: Component values used in the UWB LNA design.

Symbol	Value
C_1	320 fF
C_F	93 fF
L_1	2.65 nH
L_2	795 pH
L_3	561 pH
R_{L1}	325 Ω
I_{C1}	0.9 mA
I_{C2}	4 mA

Even without any optimization good results were obtained. The input reflection was calculated to be less than -10 dB over the entire frequency band, and as desired a flat S_{21} response of 20 dB was obtained. The calculated maximum NF of the first stage is 3.92 dB and the minimum 2.84 dB close to the centre of the frequency band. IIP3 increases linearly with the log of frequency from -27.4 dBm to -18.4 dBm over the band of interest. This improvement of IIP3 with frequency is due to the -20 dB per decade roll-off in the first stage voltage gain, thus causing less reduction of the overall IIP3.

To verify the equations derived in this paper the design was also simulated in Cadence using Spectre RF and the HIT-kits supplied by IBM. The comparison of the calculated results with the S-parameter simulations are shown in Fig. 10 and the NF comparison in Fig. 11 which shows that the simulated NF is better than predicted. In both cases there is good tracking between the results.

The calculated results were obtained with a β_0 of 300 and a pessimistic inductor quality factor of 5. A supply voltage of 1.5 V was used; thus the power consumption resulting from the collector currents in Table 1 is only 7.35 mW excluding biasing circuitry.
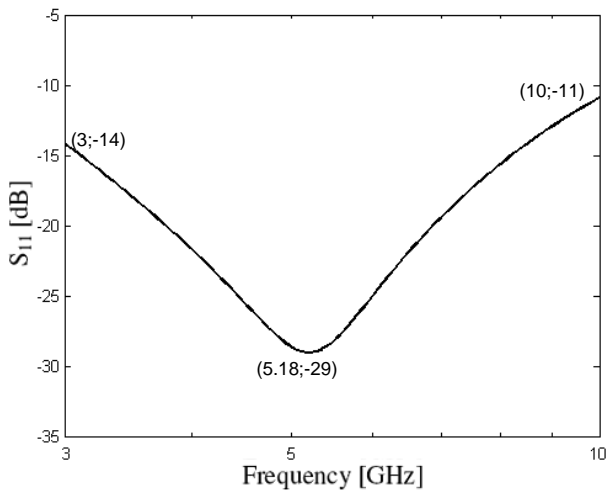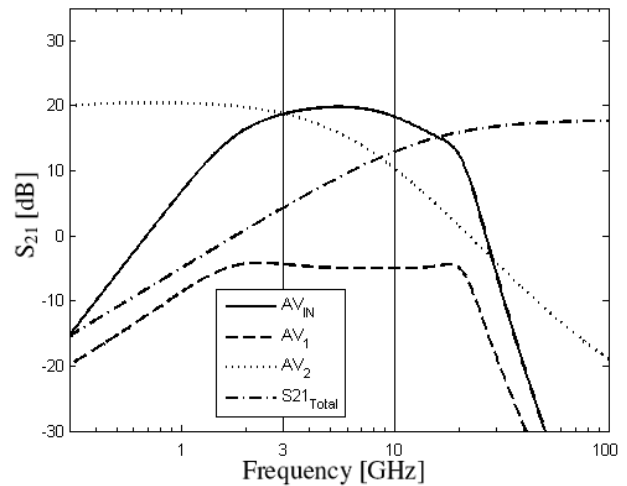

Figure 7: Calculated voltage gain of the individual stages as well as the overall S_{21} of the amplifier versus frequency.
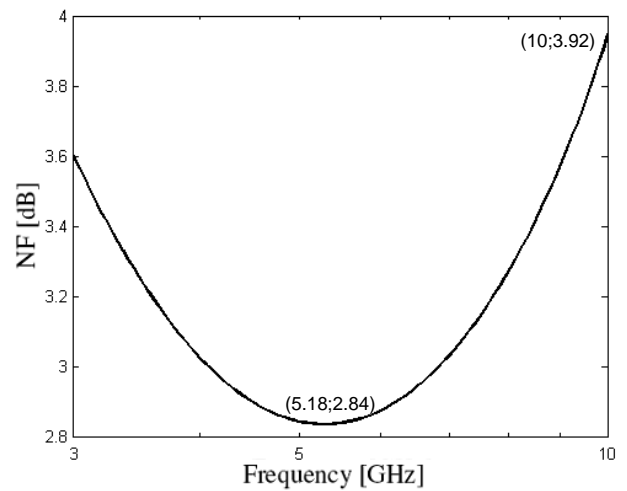

Figure 8: Calculated noise figure of the first amplifier stage versus frequency from 3 to 10 GHz.

Figure 6: Calculated input reflection coefficient versus frequency from 3 to 10 GHz.
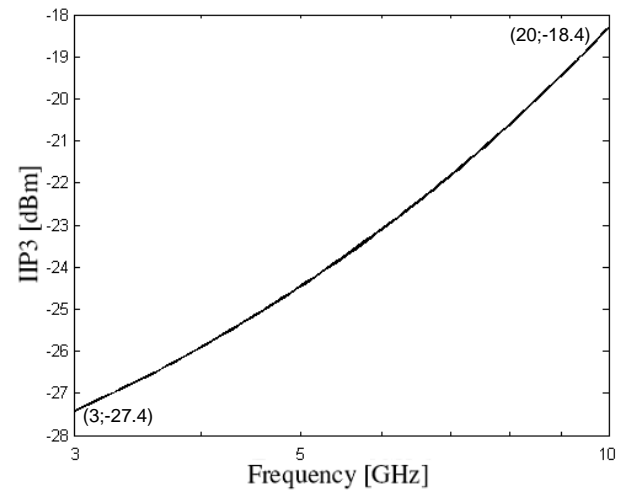

Figure 9: Calculated third order input intermodulation product versus frequency from 3 to 10 GHz.

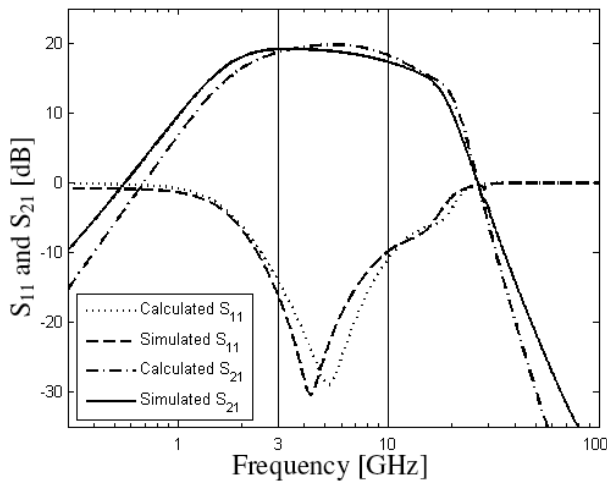Figure 10: Comparison of the calculated and simulated
S-parameter results.

Figure 11: Comparison of the calculated and simulated
noise figure results.

6.   CONCLUSION

The design principles of a newly proposed wideband LNA topology combining a LC-ladder network and capacitive shunt-shunt feedback were discussed and compact design equations were derived. Equations for the important performance measures were also given and verified with simulations using parameterized cells which include device parasitics. Based on this analysis, this configuration has great potential for achieving good performance, especially when component values are further optimized through simulation. A comparison of the results to other LNAs in literature is given in Table 2 and shows improved noise performance.

7.   ACKNOWLEDGMENT

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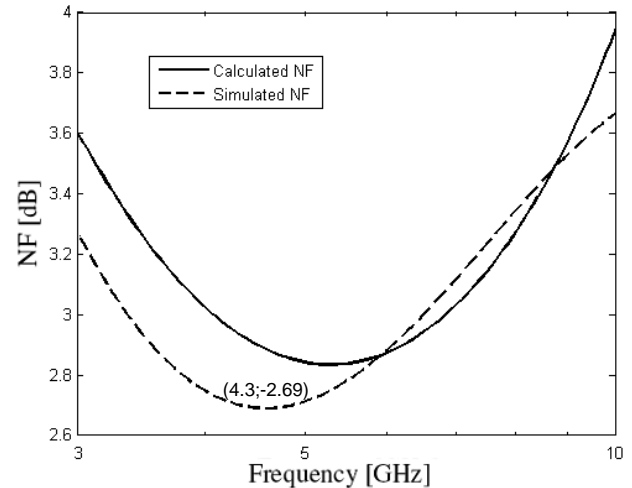
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Table 2: Comparison of results to state-of-the-art UWB LNA implementations

Ref.	Technique	Tech[a] [μm]	BW [GHz]	S_{11} [dB]	S_{21} [dB]	NF [dB]	IIP3 [dBm]	P [mW]
This work	LC-ladder & capacitive-feedback	0.13	3–10	< -10	20	2.8–3.9	-21.9 @ 5.4 GHz	7.4
[2]	Shunt-shunt capacitive-feedback	0.35	3–14	< -9	23	2.5–5.8	-17 @ 5 GHz	25.8
[5]	LC-ladder & emitter degeneration	0.18	3–10	< -9	21	2.5–4.5	-5.5 @ 3.4 GHz	30
[12]	Resistive feedback	0.18	3–10	< -10	20	3.4–4.7	-17 @ 3.5 GHz	42.5