



# The dependence of barrier height on temperature for Pd Schottky contacts on ZnO

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## ABSTRACT

Temperature dependent current–voltage ( $I$ – $V$ ) and capacitance–voltage ( $C$ – $V$ ) measurements have been performed on Pd/ZnO Schottky barrier diodes in the range 60–300 K. The room temperature values for the zero bias barrier height from the  $I$ – $V$  measurements ( $\Phi_{I-V}$ ) was found to be 0.52 eV and from the  $C$ – $V$  measurements ( $\Phi_{C-V}$ ) as 3.83 eV. From the temperature dependence of forward bias  $I$ – $V$ , the barrier height was observed to increase with temperature, a trend that disagrees with the negative temperature coefficient for semiconductor material. The  $C$ – $V$  barrier height decreases with temperature, a trend that is in agreement with the negative temperature coefficient of semiconductor material. This has enabled us to fit two curves in two regions (60–120 K and 140–300 K). We have attributed this behaviour to a defect observed by DLTS with energy level 0.31 eV below the conduction band and defect concentration of between  $4 \times 10^{16}$  and  $6 \times 10^{16} \text{ cm}^{-3}$  that traps carriers, influencing the determination of the barrier height.

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## 1. Introduction

ZnO is a group II–VI compound semiconductor with a wide and direct bandgap (3.37 eV at room temperature). Due to its large exciton binding energy of about 60 meV, which makes it highly efficient in excitonic emission, it has attracted much attention in researchers as it can also be used in ultraviolet and blue-range optoelectronic devices, including lasers [1]. It also has superior electronic parameters such as high breakdown voltage, high electron saturation velocity [2], high thermal conductivity [3] and high radiation tolerance [4], which are better than those of the classical semiconductors, such as Si and GaAs, and is also comparable with the wide band gap semiconductors, like SiC and GaN [5]. Good rectifying ZnO Schottky contacts have been difficult to achieve since the cleaning procedure of the ZnO samples prior to contacts deposition plays a major role. Due to this effect, studies on the quality of the metal/ZnO structures have been of considerable interest to researchers. The performance and reliability of the metal–semiconductor (MS) device is influenced by the quality of the contact between the metal and the semiconductor. This is because the Schottky barrier height of the MS device is given by the mismatch between the energy levels of the majority charge carriers across the metal–semiconductor interface [6]. The Schottky barrier height (SBH) is of vital

importance as it controls the electronic transport across the MS interface. Under different conditions of temperature and bias, the barrier height tends to vary as was observed by Karatas and Altindal [7] in GaAs Schottky barrier diodes. At times the barrier height (BH) measured using different techniques also tends to differ, though slightly. The performance of the MS device is also dependent on the formation of an insulative layer, which can strongly influence the device characteristics [7]. Device characteristics can also be influenced by the interface states which can lead to a large deviation from the ideal behaviour as they modify the nature of the barrier. The barrier height calculated at room temperature usually assumes the transport of carriers across the barrier to be thermionic, ignoring the effects of other current transport processes. The temperature dependence of barrier height has been studied by several researchers with conflicting results [8]. We have studied the variation of the barrier height by performing some temperature dependent  $I$ – $V$  and  $C$ – $V$  measurements on Pd/ZnO Schottky barrier diodes in the temperature range 60–300 K.

## 2. Experiment

Undoped n-type ZnO samples were used in this study. The samples were degreased in acetone for 5 min in an ultrasonic bath, then methanol for another 5 min in the ultrasonic bath and finally boiled in hydrogen peroxide for 3 min. After treatment with

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the peroxide, the samples were blown dry with nitrogen gas. Ohmic contacts of composition Ti/Al/Pt/Au and thicknesses of 20/80/40/80 nm were then deposited on the Zn-polar face in an electron beam deposition system under a vacuum of approximately  $1 \times 10^{-6}$  Torr. Annealing at a temperature of 200 °C under argon ambient was performed for 30 min. Schottky contacts with a diameter of 0.6 mm were then resistively evaporated on the O-polar face under a vacuum of approximately  $1 \times 10^{-5}$  Torr. Current-voltage ( $I$ - $V$ ) and capacitance-voltage ( $C$ - $V$ ) measurements were then performed in a closed cycle helium cryostat in the temperature range 60–330 K. Finally, DLTS measurements were performed in the same 20–300 K temperature range.

### 3. Results and discussion

In a case where an interfacial layer exists at the Schottky contact between the metal and semiconductor, the relationship between the applied voltage,  $V$  and current,  $I$  is given by [9],

$$I = I_0 \left[ \exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (1)$$

where  $n$  is the ideality factor,  $k$  is the Boltzmann constant,  $T$  is the Kelvin temperature and  $I_0$  the reverse saturation current defined by,

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_{b0}}{nkT}\right) \quad (2)$$

where  $A$  is the Schottky contact area,  $A^*$  is the effective Richardson constant,  $\phi_{b0}$  ( $=\phi_{I-V}$ ) is the zero bias barrier height. The ideality factor has been included to take into account the effects that cause deviation from ideality, i.e.  $n \neq 1$ . Fig. 1 shows the semilogarithmic plot of the forward  $I$ - $V$  characteristics of the Pd/ZnO Schottky barrier diodes in the temperature range 60–300 K. The 60–260 K curves indicate two regions where straight lines can be fitted by

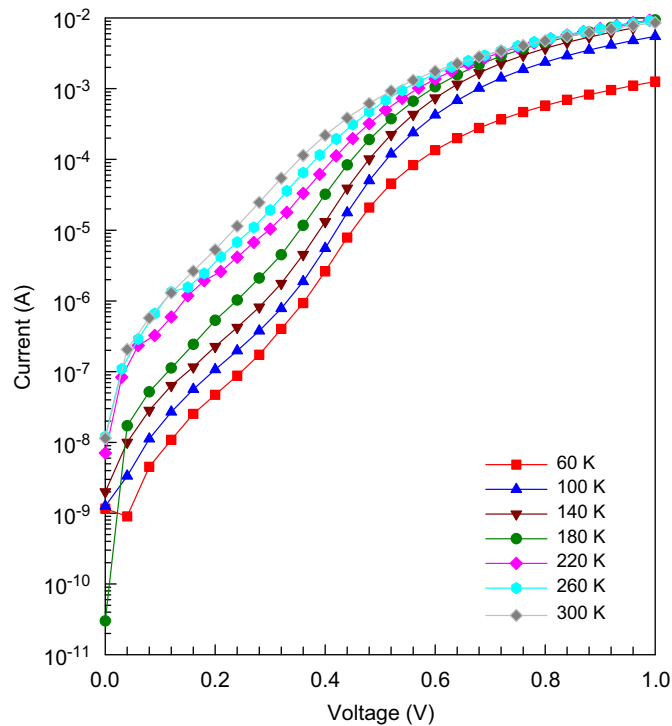


Fig. 1. Semilogarithmic current-voltage ( $I$ - $V$ ) characteristics as a function of temperature,  $T$ .

making use of Eq. (1). The lower part of the curves yield the generation recombination as the intercept on the current axis when the applied bias is zero while the intermediate part yields the thermionic emission current,  $I_0$  extrapolated to the current axis when the applied voltage is zero. From the values of the  $I_0$  obtained as intercepts after extrapolating the intermediate region to the current axis, the zero bias barrier height,  $\phi_{I-V}$  was calculated from the relationship,

$$\phi_{I-V} = \frac{kT}{q} \ln \frac{AA^*T^2}{I_0} \quad (3)$$

with  $A^* = 32 \text{ AK}^{-2} \text{ cm}^{-2}$ . The resulting barrier heights from Eq. (3) are plotted as a function of temperature in Fig. 2. The observed trend is an increase in zero bias barrier height with temperature which disagrees with the negative temperature coefficient of II-VI semiconductor material [10]. The same trend of an increase in zero bias barrier height with temperature was previously observed on GaAs Schottky contacts [11,7] and Si Schottky contacts [12]. The ideality factor,  $n$  was obtained from the gradient of the linear region of the  $I$ - $V$  plots at different temperatures, i.e.

$$n = \frac{q}{kT} \frac{\partial V}{\partial (\ln I)} \quad (4)$$

Fig. 2 indicates a decrease of  $n$  with increasing temperature from 7.55 (at 60 K) to 1.77 (at 300 K). This can be attributed to the change in the current transport process from generation recombination and other mechanisms at very low temperatures, i.e. 60–160 K to only generation recombination at the intermediate temperatures (180–260 K) and thermionic emission from 280 to 300 K. This is in agreement with what was suggested by [13]. Fig. 3 shows the variation of barrier height obtained from  $C$ - $V$  measurements,  $\Phi_b$  with temperature. The barrier height was obtained from [13],

$$\phi_{Bn} = V_i + V_n + \frac{kT}{q} - \Delta\phi \quad (5)$$

where  $V_n$  is the depth of the Fermi level below the conduction band, given by,

$$V_n = \frac{E_C - E_F}{q} = \frac{kT}{q} \ln \left( \frac{N_C}{N_D} \right) \quad (6)$$

$V_i$  is the built in potential which is obtained as the intercept on the voltage axis of the linear  $C$ - $V$  relationship plot of an intimate

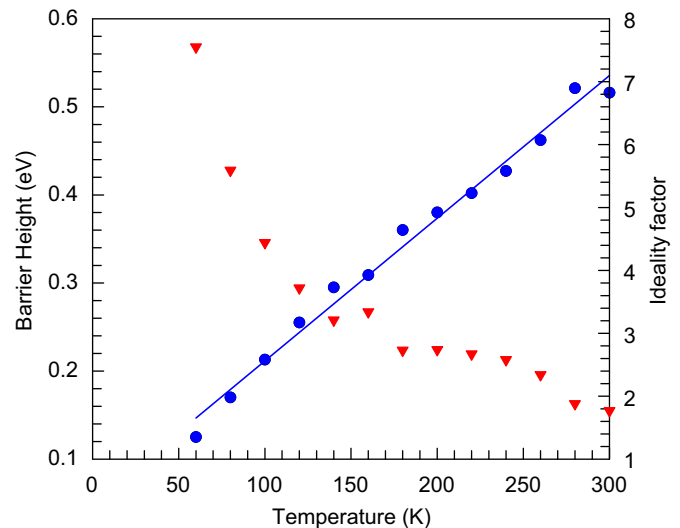


Fig. 2.  $I$ - $V$  barrier height and ideality factor versus temperature,  $T$ .

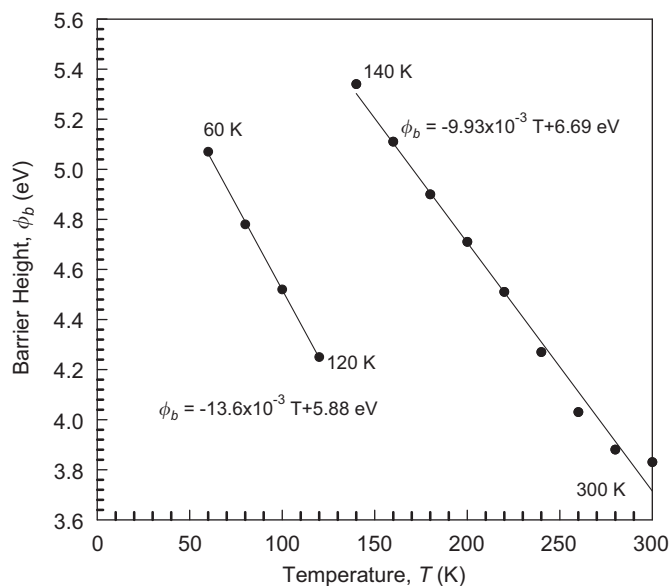


Fig. 3. Capacitance–voltage (C–V) barrier height,  $\Phi_{C-V}$  versus temperature,  $T$ .

Schottky barrier assuming a uniformly doped material, given by [14],

$$\frac{1}{C^2} = \frac{2V}{A^2 q \epsilon_s N_D} \quad (7)$$

where  $N_D$  is the impurity concentration obtained as the gradient of the  $C^{-2}$  versus  $V$  plot,  $A$  is the Schottky contact area and  $\epsilon_s$  is the semiconductor dielectric constant. The intercept on the voltage axis was found to be large, of the order of 5.05 V (at 60 K) to 3.67 V (at 300 K). This influenced the values of the measured C–V barrier heights to yield values larger than the energy gap,  $E_g$  of ZnO=3.37 eV at room temperature. Such large barrier heights, larger than the energy gap of semiconductor material have been observed by Chi et al. [15] on NiGe/n-Ge Schottky contacts, Dos Santos et al. [14] on the Schottky contacts deposited on PbSe, where the barrier height was obtained to be twice as large as the energy gap and Walpole and Nill (1971) on PbTe and InAs [16]. This behaviour of the barrier heights being larger than the band gap energy has been explained by some researchers [14,15], as being due to the existence of an inversion layer with high charge density that causes the maximum electric field in the space charge region to attain high values even with moderate doping concentrations [15]. The variation of the barrier height with temperature has enabled us to fit two linear regions to the barrier height values i.e. the first region being linear from 60 to 120 K and the second being linear from 140 to 300 K yielding equations of the form,

$$\phi_{C-V}(T_{60-120}) = \phi(T=0) + \alpha_1 T \quad (8)$$

where  $\alpha_1$  is the temperature coefficient of the semiconductor in the 60–120 K temperature range which was obtained as  $-13.6 \text{ meV K}^{-1}$ , and

$$\phi_{C-V}(T_{140-300}) = \phi(T=0) + \alpha_2 T \quad (9)$$

where  $\alpha_2$  is the temperature coefficient in the 140–300 K temperature range which was obtained as  $-9.93 \text{ meV K}^{-1}$ . The variation of carrier concentration with temperature in Fig. 4 also shows a sudden increase in carrier concentration from 120–140 K. We propose that the discontinuity resulting in the two distinct linear regions has been caused by a defect within the ZnO material which was observed using deep level transient spectroscopy (DLTS) at an energy level of 0.31 eV below the conduction band

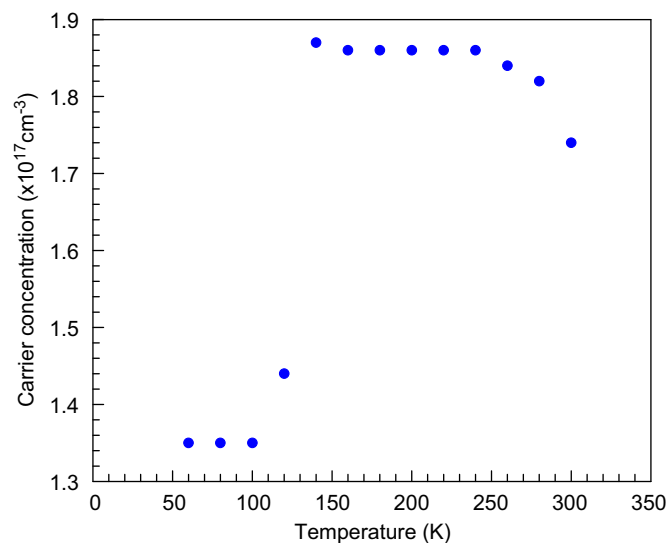


Fig. 4. Carrier concentration versus temperature,  $T$ .

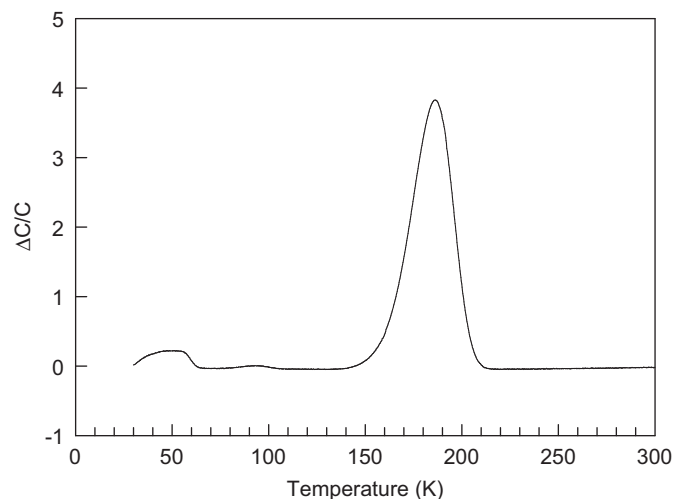


Fig. 5. DLTS signal for the as-deposited Pd/ZnO Schottky diode. This spectra was measured at quiescent reverse bias of  $-2 \text{ V}$ , filling pulse of  $V_p=0 \text{ V}$  and rate window of  $80 \text{ s}^{-1}$ .

with a trap concentration of between  $4 \times 10^{16}$  and  $6 \times 10^{16} \text{ cm}^{-3}$  as shown in Fig. 5. This defect traps carriers at low temperatures, i.e. it fills up at low temperatures and releases them at high temperatures causing the variation of the measured capacitance and hence a difficulty in obtaining the barrier height in the 120–130 K temperature range. The capacitance transient causes a sudden change in carrier concentration between 120 and 140 K.

#### 4. Conclusion

The barrier height of Pd Schottky contacts on ZnO from the  $I$ – $V$  measurements,  $\Phi_{I-V}$  has shown an increasing trend with an increasing temperature a trend that disagrees with the negative temperature coefficient of semiconductor material. From the C–V measurements, the variation of the barrier height  $\Phi_{C-V}$  with temperature agrees well with the negative temperature coefficient of semiconductor material. The temperature coefficients have been

calculated as  $-13.6 \text{ meVK}^{-1}$  (60–120 K) and  $-9.93 \text{ meVK}^{-1}$  (140–300 K). The barrier height that is larger than the band gap energy from  $C$ – $V$  measurements is due to the presence of an “inversion layer” in the semiconductor closer to the metal that modifies the electric field, influencing the junction capacitance and hence the value of the built in potential on the voltage intercept.

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