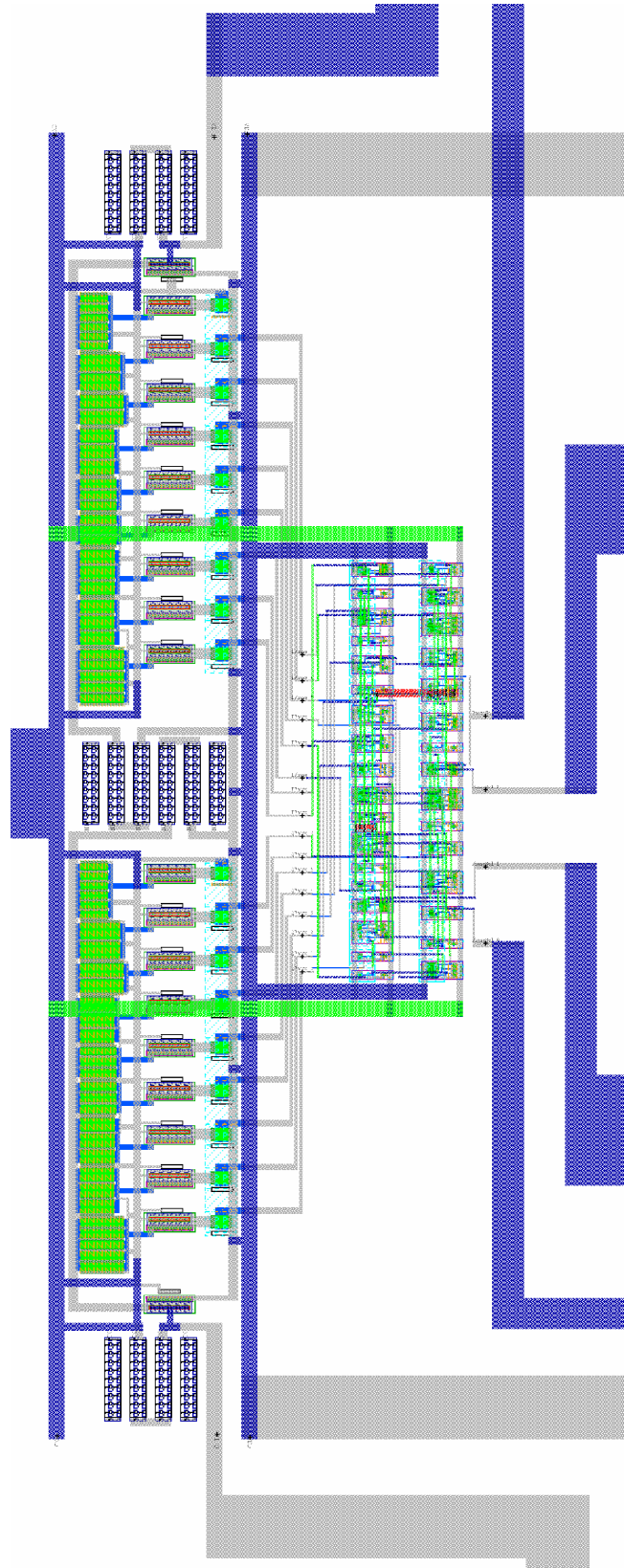Figure B.5. VGA biased using an 800 µA current source.

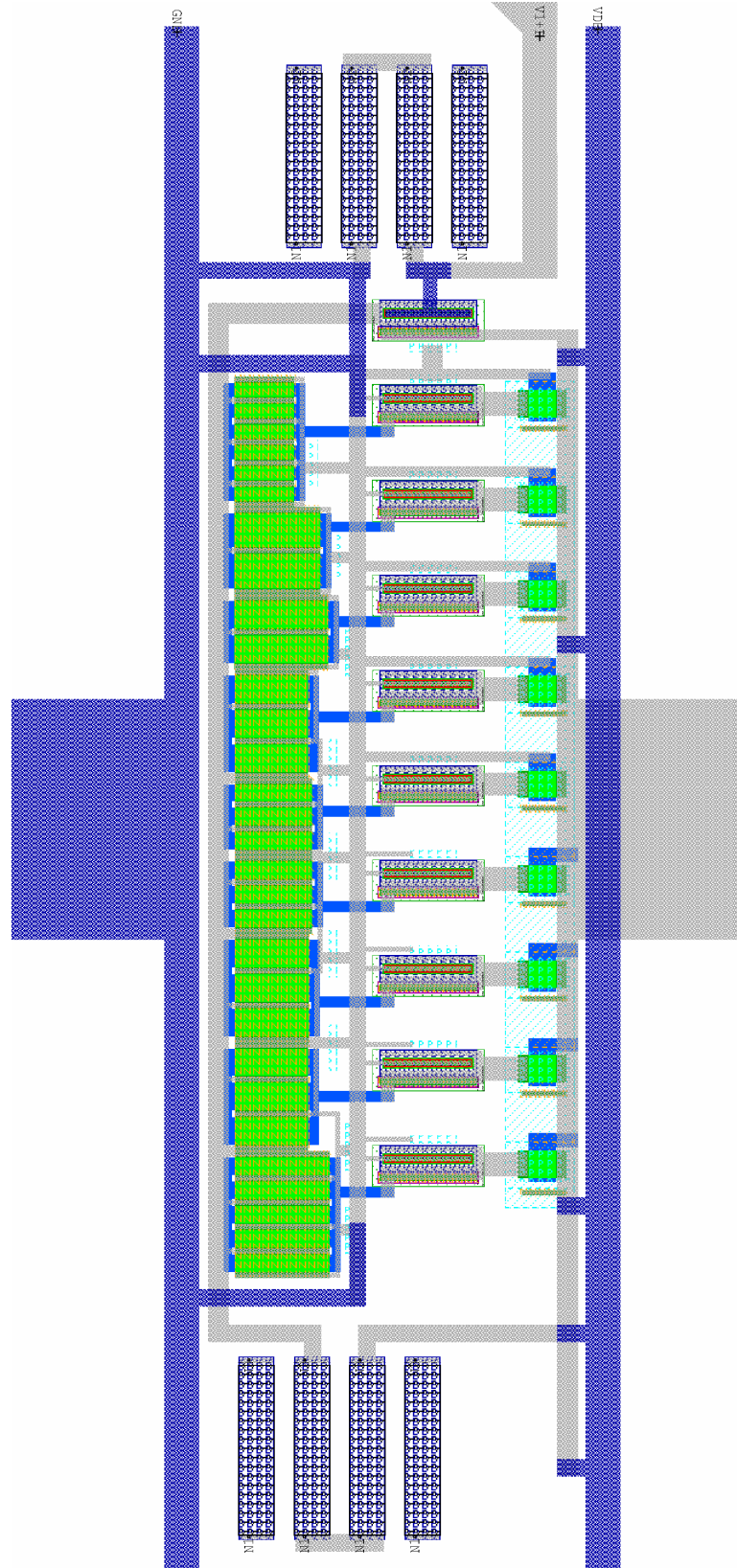Figure B.6. Complete digital phase tuner.
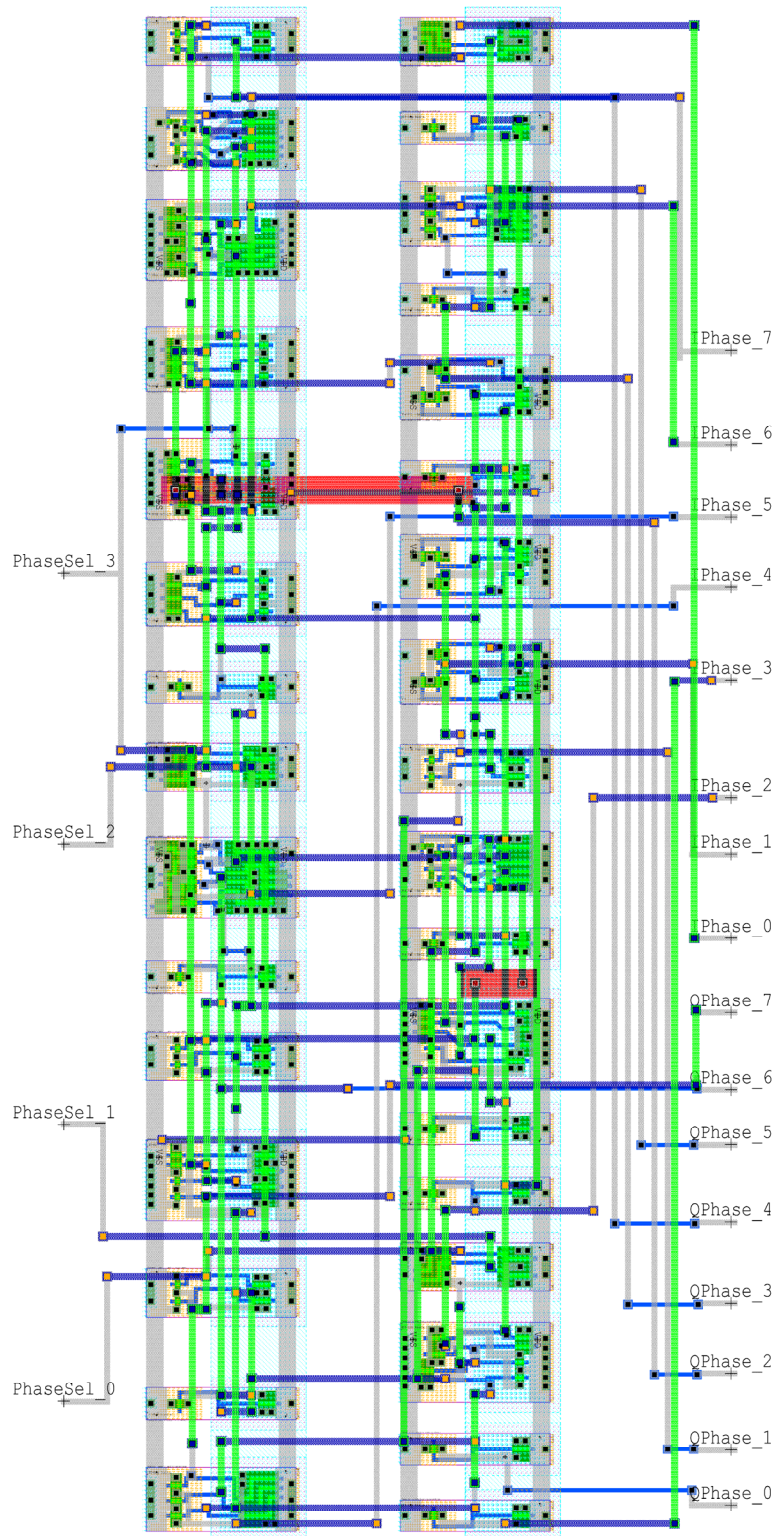
Figure B.7. Modified digital phase tuner.

Figure B.8. Detailed layout of the digital decoder. The layout was automated from VHDL code using the Mentor Graphics® package and corresponds to the circuit schematic in Figure A.2.
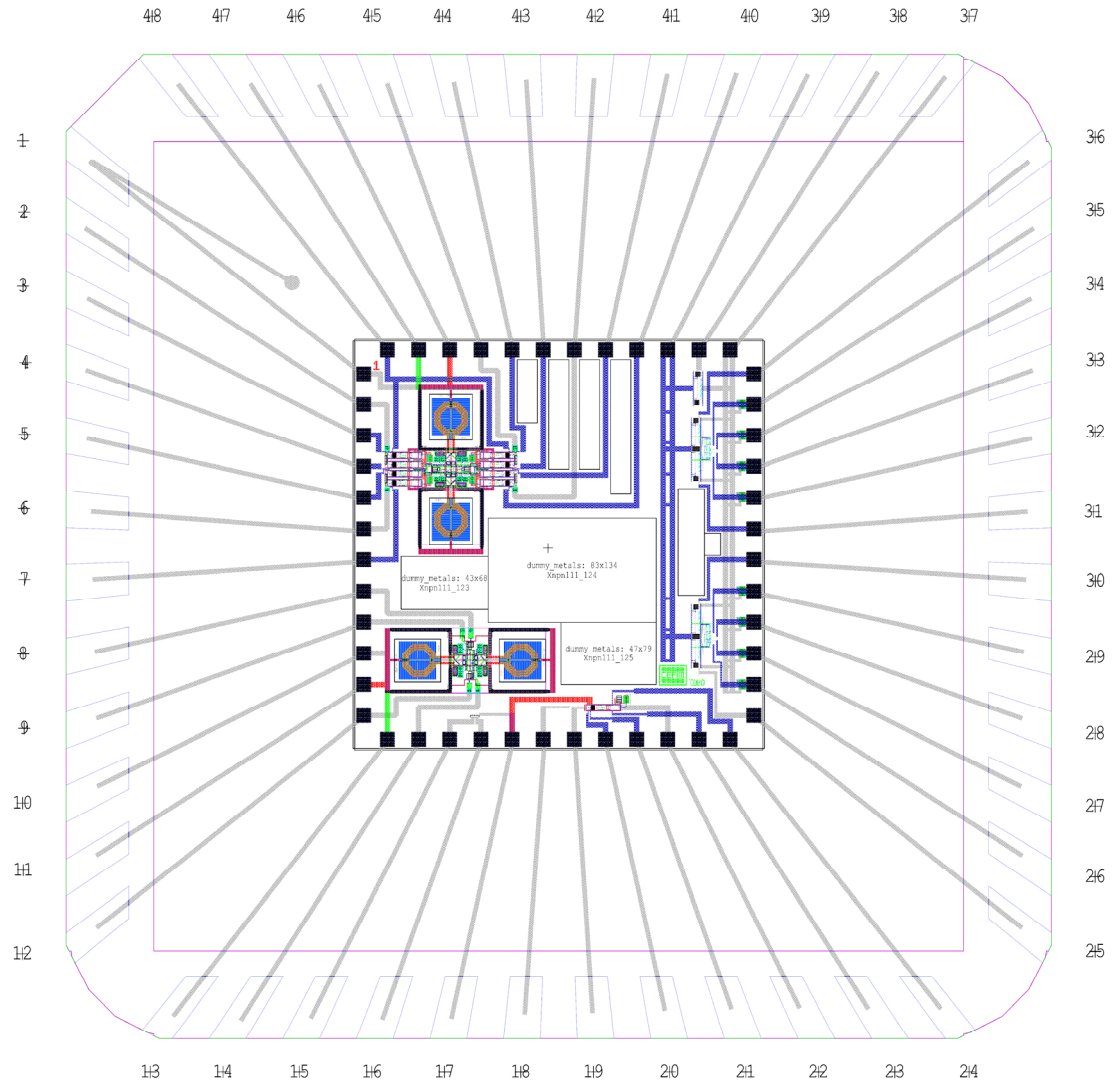
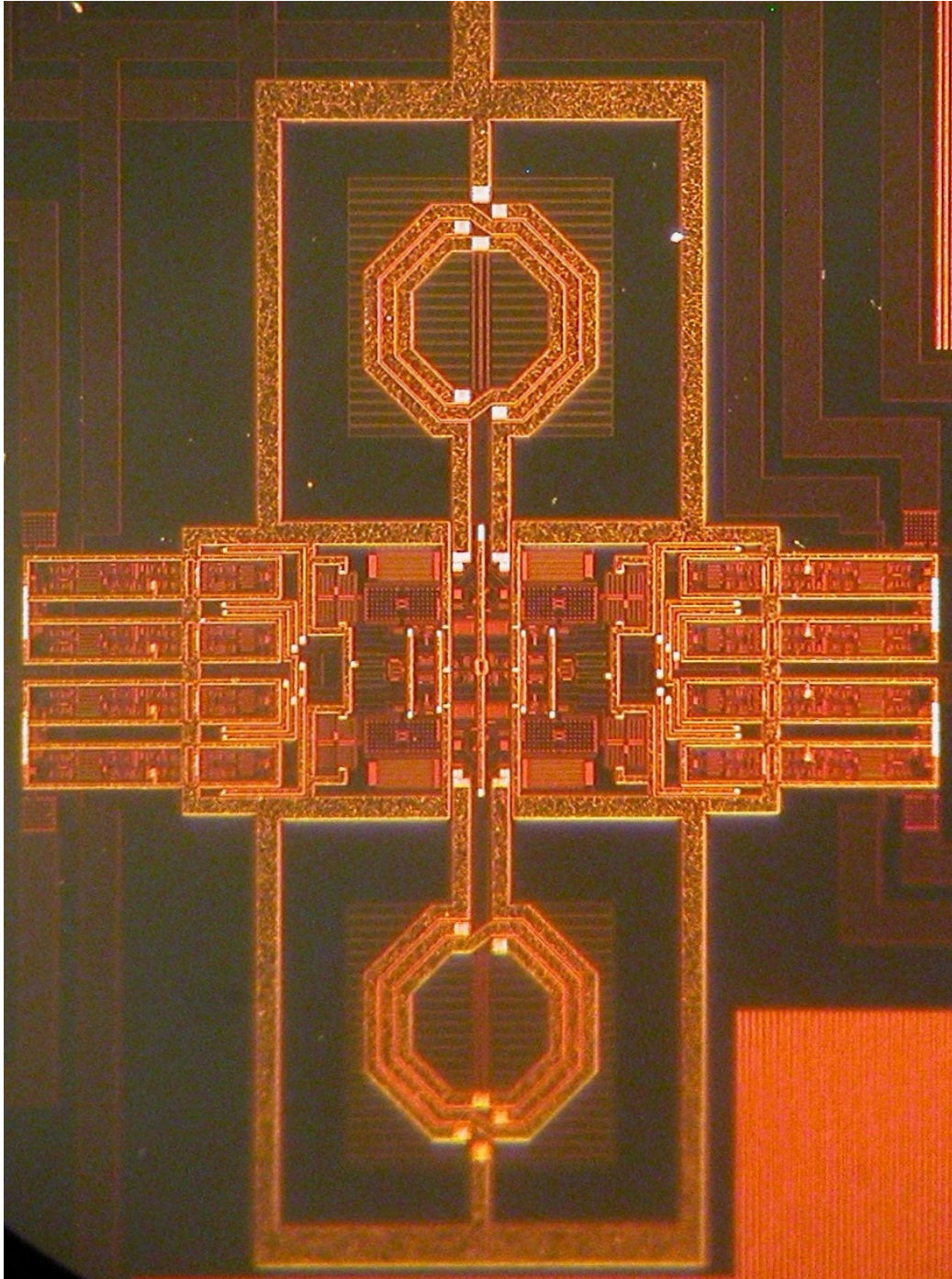Figure B.9. Bonding diagram of the QFN 48 package.

Figure B.10. Photograph of the complete circuit, excluding the digital phase tuner.
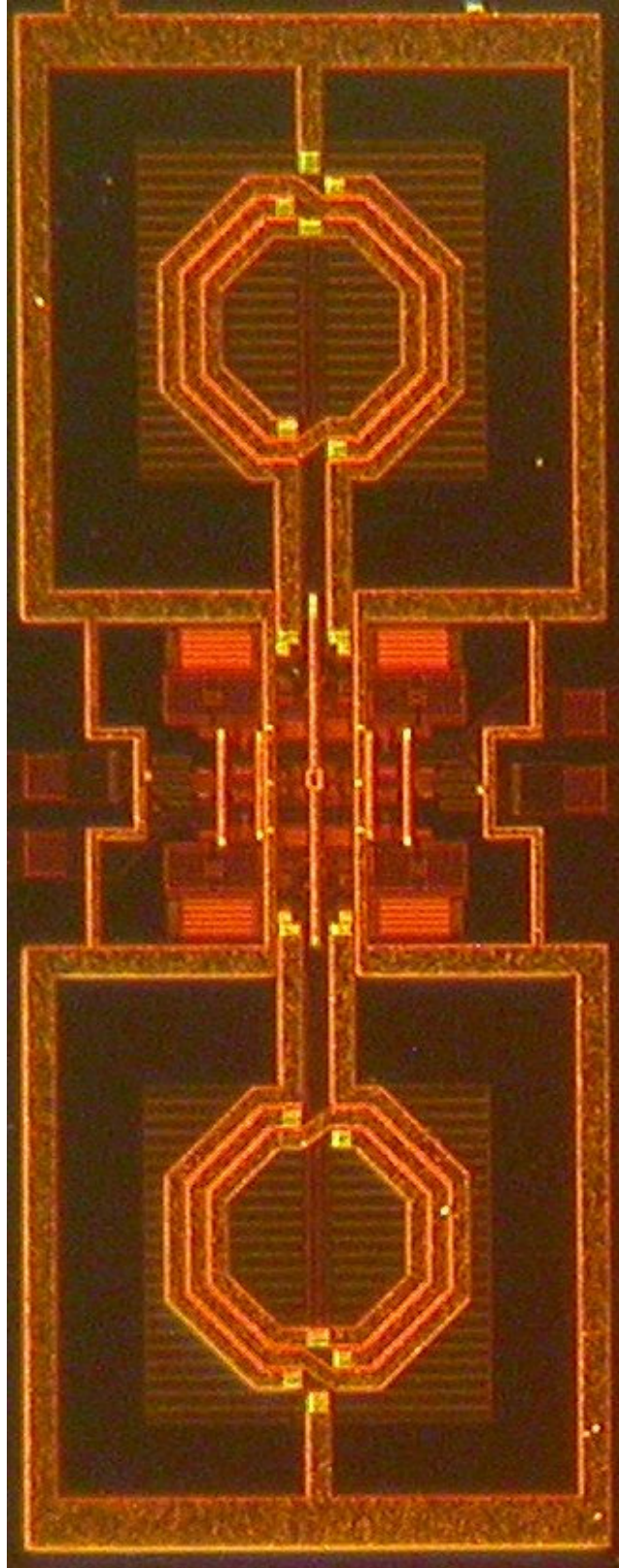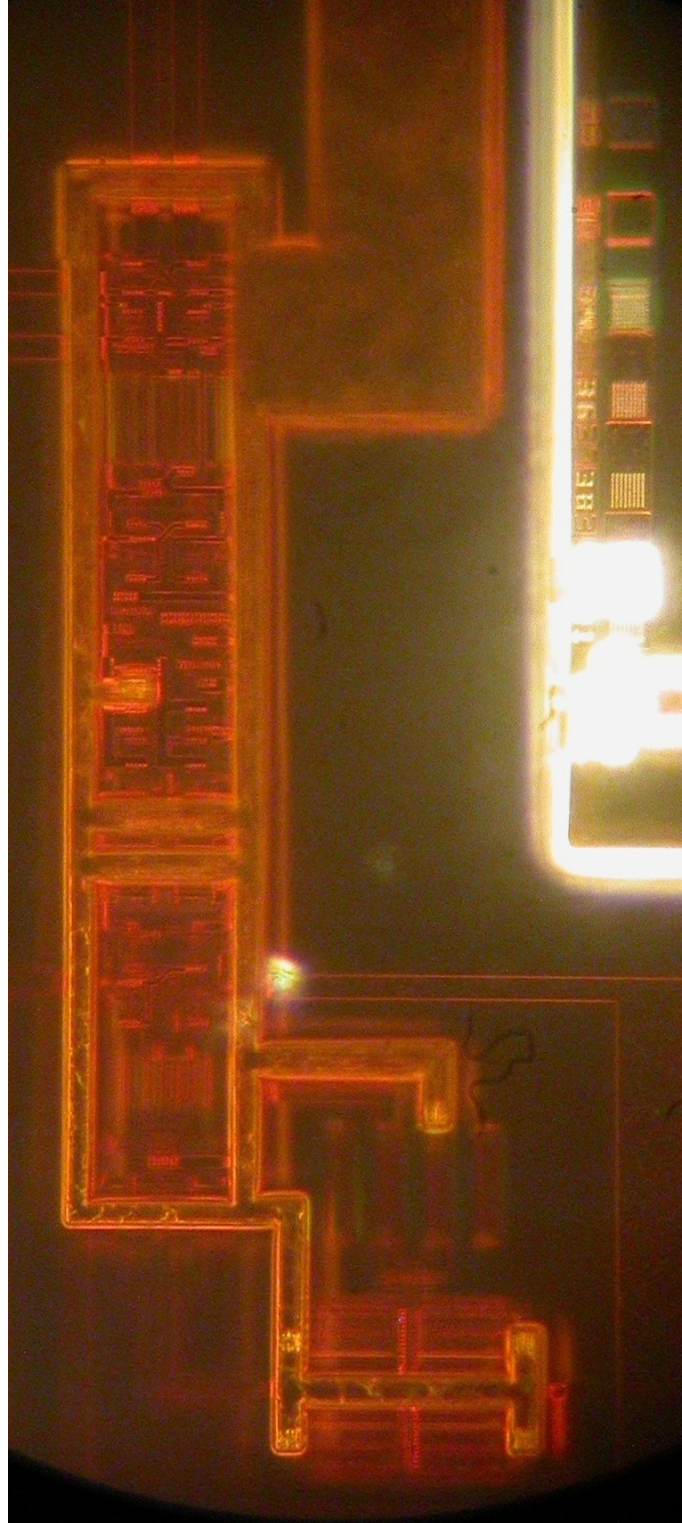
Figure B.11. Quadrature *LC*-VCO photograph.

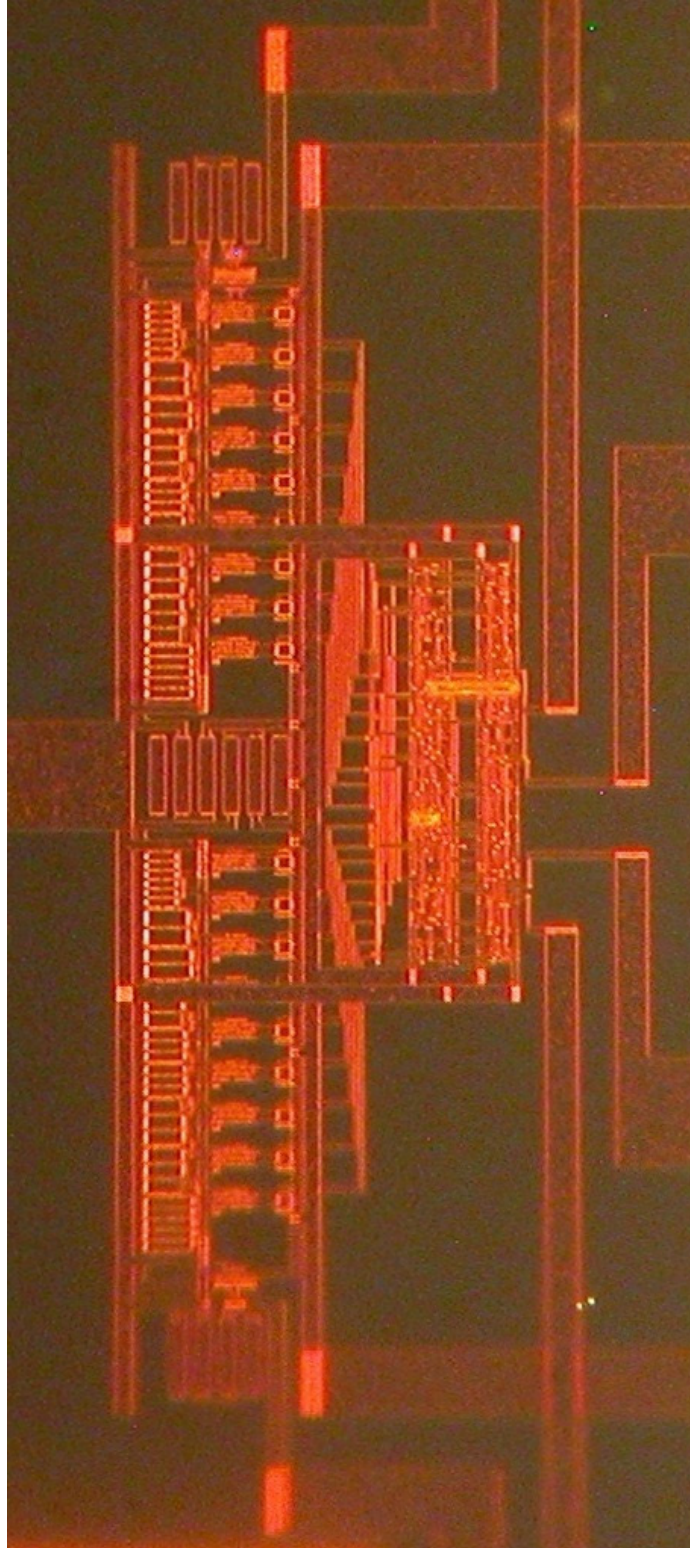Figure B.12. Photograph of the VGA biased using an 800 µA current source.

Figure B.13. Photograph of the complete digital phase tuner.