

Analysis of a DC Collector-based Power Converter Topology for an Offshore Wind Farm

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Keywords: DC collector, offshore wind farm, interleaved boost converter, voltage source converter topology, pulse-width modulation controller

Abstract—The conventional collection grids for offshore wind farm consist of internal AC link comprising of series-parallel connections of identical wind energy conversion units (WECUs). Each WECU includes a 60- or 50-Hz power transformer. The power transformers are replaced by the power converters in this article. The weight of a power converter is much lower compared to that of a power transformer of similar characteristics, thus reducing the weight of the offshore wind farm. Most of the studies being done to design DC collection grids use the conventional full-bridge voltage source converter as the topology of power converter. The efficiency of the wind farm is low due to the switching losses. In this article a cascade connection of a diode rectifier and an interleaved DC-DC boost converter is used for the converter topology. The switches duty cycle is reduced, thus improving the efficiency of the wind farm. The dynamic model of the proposed power converter is derived, including its control schemes. Power Simulator (The Powersim, Rockville, USA) and MATLAB Software (The MathWorks, Natick, Massachusetts, USA) are used to test the performances of the proposed converter model.

1. Introduction

The grid system consists of three main energy sectors: generation, transmission, and distribution. In the generation sector, wind energy is recognized as one of the most promising power generation technology for renewable energy [1]. It contributes positively to socio-economic and environmentally sustainable growth. Wind farms are not necessarily located close to the distribution sector or load centers. Increasingly, sites are being located offshore in coastal areas for the maximum wind energy tracking. The high-voltage DC (HVDC) system is more appropriate to use rather than the high-voltage AC (HVAC) system for long-distance transmission lines [2, 3]. The HVAC transmission line is expensive to build when transferring power over a long distance. The voltage and frequency all along the HVAC line are fluctuating [4]. Consequently, voltage regulators or reactive power compensators are installed at about every 258 miles (or 415.211 km) along the HVAC transmission line to boost the voltage and enhance power stability [2], increasing the cost of the HVAC system. Using an HVDC system that utilizes DC cables helps to overcome these problems. The HVDC

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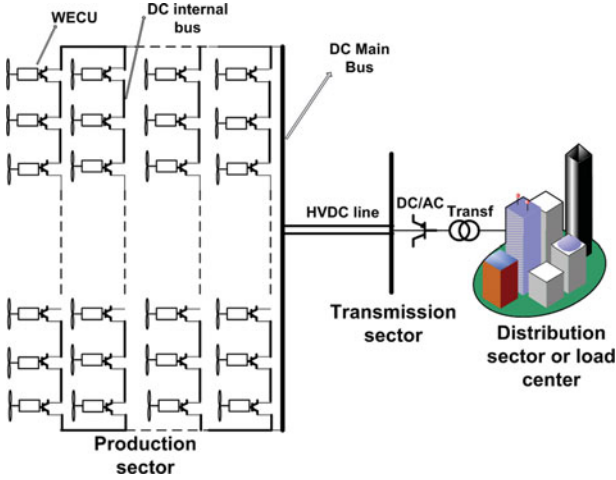


Figure 1. Topology of a DC grid system based on the concept proposed by P. Bresesti et al in *IEEE Trans. Energ. Conv.*, Vol. 22, No. 1, pp. 37-43, 2007.

system also provides better control of voltage and frequency. Consequently, there is no need to install reactive power compensators or voltage regulators along the HVDC transmission line. Only power converter stations are required at the terminals of the HVDC transmission line to control the voltage and frequency [5].

In the category of HVDC transmission systems, two groups exist at the moment: the HVDC system based on a line commutated converter (LCC) and HVDC “light” that utilizes a voltage source converter (VSC) and pulse-width modulation (PWM) control. The operating principle of these two systems has been well documented in the literature [6, 7]. HVDC light is very well suited for power conditioning, power compensation, and power filtering. An LCC-based HVDC system is still considered a better option for bulk power transmission, and it is also cheaper than HVDC light of a similar power rating. However, the control of voltage and frequency suffers because of parameters variations in the wind farm. The focus of this article is primarily on the energy production sector. An offshore wind farm feeding power to the distribution sector through an HVDC transmission line is considered. The grid system structure, which includes $n \times m$ series-parallel interconnections of wind energy conversion units (WECUs), is shown in Figure 1 [8, 9]. The n series connection of WECUs is needed to build up a voltage high enough for an HVDC transmission line. The m parallel branches on the other hand allows build up of the current and, hence, the required active power to sustain the distribution sector.

The traditional wind farm collector consists of AC internal links, with each WECU consisting of a wind turbine, a generator, and a 50- or 60-Hz power transformer. There are two existing types of conversion unit based wind turbine:

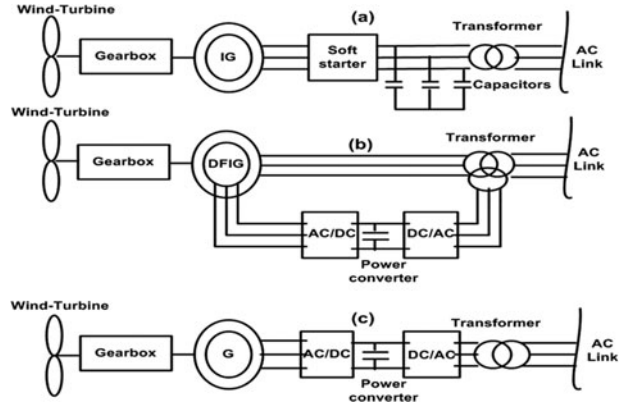


Figure 2. Topology of WECUs: (a) fixed-speed turbine with an IG, (b) variable-speed turbine with a DFIG, and (c) variable-speed turbine with an induction or synchronous generator. Based on the concepts described in Max, L., *Design and Control of a DC Collection Grid for a Wind Farm*, Ph.D. Thesis, Chalmers University of Technology, Sweden, November 2009.

fixed speed and variable speed [9]. A schematic diagram of a fixed-speed wind turbine with an induction generator (IG) is shown in Figure 2(a). The IG is connected directly to the grid, and the speed of the wind turbine is determined by the grid frequency, the gearbox, and the number of poles [10]. Due to the locked speed operation of the wind turbine, it is not possible to track the maximum wind power. Figure 2(b) shows a diagram of a variable-speed wind turbine with a doubly fed IG (DFIG). The stator of the DFIG is directly connected to the grid while the rotor is connected to a converter via slip rings. The operating speed of the wind turbine is coordinated through the power converter, which handles about 20–30% of the total power delivered. This reduces the power losses in the power converter. Figure 2(c) shows a diagram of a variable-speed turbine with an induction or synchronous generator; the operating speed of the wind-turbine is again coordinated through a power converter. The power loss in this case is higher because the power converter handles 100% of the power produced. The gearbox can be removed if the generator has a large number of poles. The variable-speed wind turbine with a permanent magnet synchronous generator (PMSG) is also much preferred in wind farm applications due to its low cost, high reliability, compact size, and low reactive power consumption [11].

To provide a DC link to the output of each WECU in the wind farm, Figure 3(a) gives the topology of a WECU that was proposed in [9, 12]. In this topology, the power transformer is replaced by a cascade connection of an AC/DC and a DC/DC converter. In [12], the AC/DC converter was a three-phase full-bridge diode rectifier, and the DC/DC converter was a conventional full-bridge boost converter. In [9], the DC/DC converter included a medium-frequency inverter, a medium-frequency

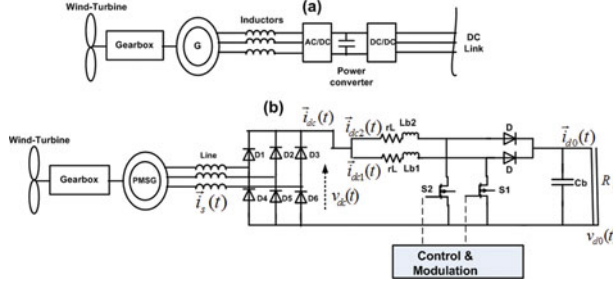


Figure 3. WECU with a DC output: (a) existing topology and (b) proposed topology.

transformer, and a medium-frequency rectifier. The medium-frequency transformer is compact and small in size compared to the 50- or 60-Hz power transformer. The power loss is very high because of the full-bridge VSCs included in the WECU.

In this article, a variable-speed wind turbine with a PMSG is considered. The DC link is provided at the output of a WECU through a cascade connection of a diode bridge rectifier and a DC/DC converter. The DC/DC converter considered is an interleaved boost converter to cater to the high power handling requirement. The proposed topology is shown in Figure 3(b). The layout of an interleaved boost converter is similar to par-allelling two single DC-DC boost converters. However, gate signals to the interleaved phases are generated in such a man-ner as to allow equal current sharing among the phases and also ensure ripple cancellation. The dynamic model and oper-ating principle of a single DC-DC boost converter is derived in [13]. The advantage of using the proposed topology com-pared to the conventional full-bridge VSC topology are that the switching losses that cause power losses are reduced due to the lower switching frequency or lower duty ratio. The in-terleaved topology also reduces switch stresses, power loss, and volume of magnetic components. Thus, improved effi-ciency of the WECU is realized. The diode bridge rectifier, if not cascaded with a boost converter, contributes to large harmonic distortions but generates low switching losses due to low switching frequency [14]. However, cascading a diode rectifier with a boost converter allows active rectification, thus improving total input power factor. The dynamic model of the proposed power converter topology is derived including its control schemes.

2. Power Loss Analyses

2.1. Full-bridge VSC

The most commonly used topology for HVDC light applications is the two-level full-bridge VSC. This topology has a number of advantages, such as low harmonic distortion gen-

eration, rapid control of active and reactive power, and better ability to sustain a weak grid system in maintaining fault ride-through capability of the grid [15, 16]. A three-phase full-bridge VSC topology uses six switches, e.g., insulated-gate bipolar transistors (IGBTs); an average of two IGBT switches conduct at any one given time respective to the 120° phase angle difference between legs [17]. The total power losses of a balanced three-phase full-bridge VSC is derived in Eq. (1) [18]:

$$P_{Loss} = 3r_L i_s^2(t) + 6V_{ce,sat} i_s(t) [2d(t) - 1] \quad (1)$$

where r_L is the inductor resistance, $V_{ce,sat}$ is the switch voltage saturation or voltage drop across the switch, $i_s(t)$ is the AC line current, and $d(t)$ is the duty ratio ($0 \leq d(t) \leq 1$). From Eq. (1), it is noted that the power losses increase or decrease proportionally with an increase or decrease of the duty ratio. For a full-bridge system, $d(t) = 0.5 + D \sin \omega t$ with $D < 0.5$ [19]. The conduction or switching loss is maximum when $d(t) \approx 1$; this is true for the full-bridge VSC because the switches operate continuously at $d(t) \approx 1$. Another factor that contributes to power losses is the recurrence of turn-on/-off; the switching sequences of IGBT cells in a full-bridge VSC are very high compared to the switching sequences of diodes in a full-bridge diode rectifier. Thus, the full-bridge VSC contributes to higher power losses than does the diode bridge rectifier.

2.2. Diode Bridge Rectifier with Interleaved Boost Converter

The interleaved boost converter consists of two single boost converters connected in parallel, as shown in Figure 3(b). The operation of the interleaved boost converter can be divided into the following time intervals: $0 < t_{on} < d_1(t)T_s$ and $0.5T_s < t_{on} < (0.5 + d_2(t))T_s$, switches S_1 and S_2 conduct simultaneously; $d_1(t)T_s < t_{on} < 0.5T_s$, S_1 conducts and S_2 turns off; $(0.5 + d_1(t))T_s < t_{on} < T_s$, S_1 turns off and S_2 conducts. With $d_1(t)$ and $d_2(t)$, respectively, the duty ratio of switches S_1 and S_2 , t_{on} is the conduction time interval. The total power loss of the system is derived in Eq. (2), the power converter is supplied by a balanced three-phase system:

$$P_{Loss} = 3r_L i_s^2(t) + 6V_{fwd} i_s(t) + V_{ce,sat} i_{dc1,2}(t) [2d_{1,2}(t) + 1] + V_{fwd} i_{dc1,2}(t) [1 - 2d_{1,2}(t)] \quad (2)$$

where $d_1(t) = d_2(t) = d_{1,2}(t)$ and $i_{dc1}(t) = i_{dc2}(t) = i_{dc1,2}(t)$; $i_{dc1}(t)$ and $i_{dc2}(t)$ are DC currents flowing in the two boost inductors L_{b1} and L_{b2} ; and V_{fwd} is the diode forward voltage drop. The magnitude of line current is given in Eq. (3):

$$i_s(t) = i_{dc}(t) = i_{dc1}(t) + i_{dc2}(t) = i_{s1}(t) \sqrt{1 + THD_I^2} \text{ with}$$

$$THD_I = \frac{1}{i_{s1}(t)} \sqrt{\sum_{h=2}^{\infty} i_h^2(t)} \quad (3)$$

where $i_{s1}(t)$ is the fundamental line current, $i_{dc}(t)$ is the DC line current, THD_I is the total current harmonic distortion, and $i_h(t)$ denotes the harmonics current components recorded in the AC/DC link [14, 20].

The diodes operate at low switching frequency compared to the IGBT switch. The amount of turn-on/off in a diode bridge rectifier is very small compared to full-bridge VSC-based PWM. The magnitude of DC current flowing through the switches is half of the total diode rectifier output DC current amplitude. Therefore, the combined second, third, and fourth terms of Eq. (2) is smaller than the second term in Eq. (1). By inspection of Eqs. (1) and (2), it can be observed that power losses in a full-bridge diode rectifier combined with an interleaved boost converter is lower than the power losses in a full-bridge VSC.

3. Dynamic Circuit Model

Based on Figure 3(b) of the proposed WECU topology, the input DC voltage to the interleaved boost converter or output of the diode bridge rectifier is derived in Eq. (4) for three-phase and single-bridge systems [21]:

$$v_{dc}(t) = \frac{3\sqrt{2}}{\pi} a_r V_{LLrms} - \frac{3}{\pi} X_c i_{dc}(t) \quad (4)$$

where

V_{LLrms} is the line-to-line RMS voltage,
 a_r is the converter transformer tap ratio,
 X_c is the commutation reactance,
 $X_c = 2\pi f_{50Hz} L$,
 $L = L_{line} + [(L_{b1} L_{b2}) / (L_{b1} + L_{b2})]$, and

L_{line} is the inductance of the line in expressed as Eq. (5) [4]:

$$L_{line} = 2 \times 10^{-7} \ell n \frac{D_m}{D_s} (\text{inH/m}) \quad (5)$$

where D_m is the geometric mean distance between conductors, and D_s is the geometric mean radius between conductors.

The steady-state and small-signal equivalent circuit model of the interleaved boost converter is shown in Figure 4. This is deduced from the average dynamic model derived in Eqs. (6)–(8). The duty ratio is given as $D = t_{on}/T_s$, where t_{on} represents the interval of time when switch is turned on:

$$L_{b1} \frac{d(i_{dc1}(t))}{dt} = v_{dc}(t) - r_L i_{dc1}(t) - V_{ce,sat} (0.5 + d_2(t)) - V_{fwd} (0.5 - d_2(t)) - v_{d0}(t)$$

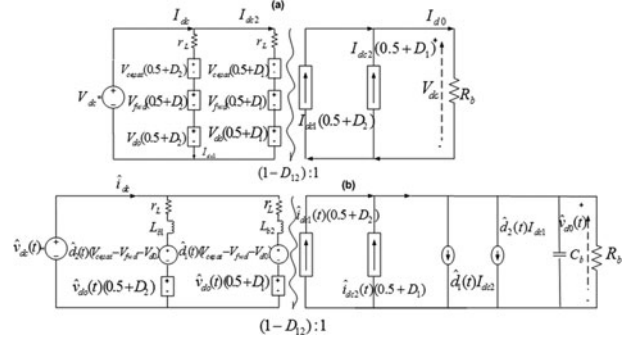


Figure 4. Equivalent circuit of an interleaved boost converter: (a) steady-state diagram and (b) small-signal circuit.

$$\begin{aligned} & \times (0.5 - d_2(t)), \quad (6) \\ L_{b2} \frac{d(i_{dc2}(t))}{dt} &= v_{dc}(t) - r_L i_{dc2}(t) - V_{ce,sat} (0.5 + d_1(t)) \\ & \quad - V_{fwd} (0.5 - d_1(t)) - v_{d0}(t) \\ & \quad \times (0.5 - d_1(t)) \quad (7) \\ C_b \frac{d(v_{d0}(t))}{dt} &= i_{dc2}(t) (0.5 - d_1(t)) + i_{dc1}(t) (0.5 - d_2(t)) \\ & \quad - \frac{v_{d0}(t)}{R_b}, \quad (8) \end{aligned}$$

where, $v_{d0}(t)$ is a non-constant DC-link voltage, C_b is the boost capacitor, and R_b is the resistance of DC bus or the load resistance. The small-signal model that gives details of the dynamics of the interleaved boost converter is derived in Eqs. (9)–(11), and the equivalent circuit is shown in Figure 4(b). These are obtained by adding signal variations to the averaged Eqs. (6)–(8). The second-order non-linear variations are assumed to be very small and are neglected in the derivations:

$$\begin{aligned} L_{b1} \frac{d\hat{i}_{dc1}(t)}{\partial t} &= \hat{v}_{dc}(t) - r_L \hat{i}_{dc1}(t) - \hat{d}_2(t) (V_{ce,sat} - V_{fwd} \\ & \quad \times - V_{d0}) - \hat{v}_{d0}(t) (0.5 - D_2), \quad (9) \\ L_{b2} \frac{d\hat{i}_{dc2}(t)}{\partial t} &= \hat{v}_{dc}(t) - r_L \hat{i}_{dc2}(t) - \hat{d}_1(t) (V_{ce,sat} - V_{fwd} \\ & \quad \times - V_{d0}) - \hat{v}_{d0}(t) (0.5 - D_1), \quad (10) \\ C_b \frac{d\hat{v}_{d0}(t)}{\partial t} &= \hat{i}_{dc2}(t) (0.5 - D_1) + \hat{i}_{dc1}(t) (0.5 - D_2) \\ & \quad \times - \hat{d}_1(t) I_{dc2} - \hat{d}_2(t) I_{dc1} - \frac{\hat{v}_{d0}(t)}{R_b}. \quad (11) \end{aligned}$$

The hat ($\hat{\cdot}$) stands for signal variations; $d(t) = D + \hat{d}(t)$, $i_{dc}(t) = I_{dc} + \hat{i}_{dc}(t)$, and $v_{d0}(t) = V_{d0} + \hat{v}_{d0}(t)$. The capital letters represent constant or steady-state parameters. The components of the interleaved boost converter are sized according to Eqs. (12)–(14); the steady-state circuit model in Figure 4(a)

is derived from Eqs. (15)–(17):

$$L_{b1} = \frac{(V_{dc} - r_L I_{dc1} - V_{ce,sat}) D_1 T_s}{\Delta i_{Lb1,peak-peak}}, \quad (12)$$

$$L_{b1} = \frac{(V_{dc} - r_L I_{dc2} - V_{ce,sat}) D_2 T_s}{\Delta i_{Lb2,peak-peak}}, \quad (13)$$

$$C_b = \frac{V_{d0} D_{1or2} T_s}{R_b \Delta v_{do,peak-peak}}, \quad (14)$$

$$V_{dc} - r_L I_{dc1} - V_{cesat} (0.5 + D_2) - V_{fwd} (0.5 - D_2) - V_{d0} (0.5 - D_2) = 0, \quad (15)$$

$$V_{dc} - r_L I_{dc2} - V_{cesat} (0.5 + D_1) - V_{fwd} (0.5 - D_1) - V_{d0} (0.5 - D_1) = 0, \quad (16)$$

$$I_{dc1} (0.5 - D_2) + I_{dc2} (0.5 - D_1) - \frac{V_{d0}}{R_b} = 0. \quad (17)$$

4. Circuit Model Simulation

The building block diagram in Power Simulator software (The Powersim, Rockville, USA) is based on the two groups of derived equations; the steady-state model in Figure 4(a) is based on Eqs. (15)–(17), and the AC model in Figure 4(b) is based on Eqs. (9)–(11). The PWM controller is included in the circuit to maintain the parameters variations within acceptable limits. The PWM controller has an inner current loop to control the frequency, mitigate the current/voltage ripple, and correct the power factor. An outer voltage loop regulates the DC link to follow the voltage reference. The PWM controller block di-agram is shown in Figure 5, where $G_1(s)$, $G_2(s)$, $G_3(s)$, and $G_4(s)$ are the open-loop transfer functions. These are derived by applying the Laplace transform method to Eqs. (9)–(11). Gate signals to the interleaved converter are properly coordi-nated. They are phase shifted from each other by $2\pi/N$, where N is the number of phases.

4.1. Open-loop and Closed-loop Signal Models

Detailed derivations method of the open-loop and closed-loop transfer functions of the DC-DC converter can be found in [13]. The two switches of the interleaved boost converter have

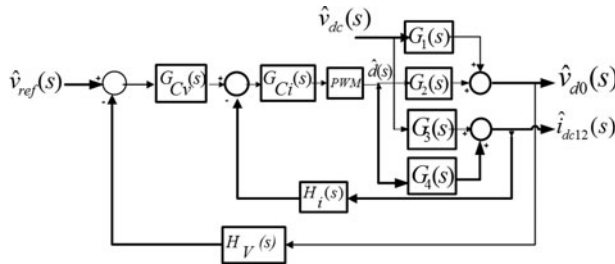


Figure 5. Structure of the PWM controller.

identical PWM controller schemes. Gate signals for switch S_1 on phase 1 are phase shifted by 180° from those for switch S_2 on phase 2. The open-loop transfer functions are derived in Eqs. (18)–(21) and the closed-loop functions in Eqs. (22)–(25):

$$G_1(s) = \frac{\hat{v}_{d0}(s)}{\hat{v}_{dc}(s)} = \frac{(1-D_{1,2})}{s^2 L_{b1,2} + s \left(r_L C_b + \frac{L_{b1,2}}{R_b} \right) + \frac{r_L}{R_b} + (1-D)}, \quad (18)$$

$$G_2(s) = \frac{\hat{v}_{d0}(s)}{\hat{d}_{1,2}(s)} = \frac{-s L_{b1,2} I_{dc1,2} + (1-D_{1,2}) V_{d0} - r_L I_{dc1,2}}{s^2 L_{b1,2} + s \left(r_L C_b + \frac{L_{b1,2}}{R_b} \right) + \frac{r_L}{R_b} + (1-D)}, \quad (19)$$

$$G_3(s) = \frac{\hat{i}_{dc1,2}(s)}{\hat{v}_{dc}(s)} = \frac{s C_b + \frac{1}{R_b}}{s^2 L_{b1,2} + s \left(r_L C_b + \frac{L_{b1,2}}{R_b} \right) + \frac{r_L}{R_b} + (1-D)}, \quad (20)$$

$$G_4(s) = \frac{\hat{i}_{dc1,2}(s)}{d_{1,2}(s)} = \frac{s V_{d0} C_b + D_{1,2} I_{dc1,2}}{s^2 L_{b1,2} + s \left(r_L C_b + \frac{L_{b1,2}}{R_b} \right) + \frac{r_L}{R_b} + (1-D)}, \quad (21)$$

$$G_{d-dc}(s) = \frac{\hat{d}_{1,2}(s)}{\hat{i}_{dc1,2}(s)} = \frac{1}{G_4(s)} \times \frac{T_C}{1 + T_C}, \quad (22)$$

$$G_{v_{d0}-d_{dc}}(s) = \frac{\hat{v}_{d0}(s)}{\hat{i}_{dc1,2}(s)} = \frac{T_C}{1 + T_C} \times \frac{G_2(s)}{G_4(s)}, \quad (23)$$

$$G_{d-v_{dc}}(s) = \frac{d_{1,2}(s)}{\hat{v}_{dc}(s)} = \frac{T_C}{1 + T_C} \times \frac{G_3(s)}{G_4(s)}, \quad (24)$$

$$G_{v_{d0}-v_{dc}}(s) = \frac{\hat{v}_{d0}(s)}{\hat{v}_{dc}(s)} = \frac{G_1(s)}{1 + T_C}, \quad (25)$$

$$G_{v_{ref}-v_{d0}}(s) = \frac{\hat{v}_{ref}(s)}{\hat{v}_{d0}(s)} = \frac{G_2(s)}{1 + T_V} \times \frac{G_2(s)}{G_4(s)}. \quad (26)$$

where

T_C is the current loop-gain, $T_C = G_{Ci}(s) \times 1/V_{sw} \times H_i \times G_4(s)$;

T_V is the voltage-loop gain, $T_V = G_{Cv}(s) \times 1/V_{sw} \times H_v \times G_2(s)$;

$G_{Ci}(s)$ and $G_{Cv}(s)$ are, respectively, the current and voltage compensators transfer functions;

$H_i(s)$ and $H_v(s)$ are, respectively, the current and voltage sensors; and

V_{sw} is the peak amplitude of the PWM triangular carrier signal.

The modulation indices of the two switches are given in Eqs. (27) and (28):

$$m_1(t) = \frac{v_{d0}(t)}{v_{dc}(t)} \approx \frac{1}{0.5 - d_1(t)} \text{ with } d_1(t) = \frac{t_{on1}}{T_s}$$

v_{LLrms} (t)	v_{dc} (t)	v_{d0} (t)	i_{d0} (t)	$d_{1,2}$ (t)	i_{dc12} (t)	L_{line}	$L_{b1,2}$	C_b
2.12 kV	2.8 kV	6 kV	166.6 A	0.3	175 A	0.00001 μ H	133 mH	927 μ F

TABLE 1. Input parameters for the simulation

$$= \frac{v_{c1}(t)}{V_{sw}}, \quad (27)$$

$$m_2(t) = \frac{v_{d0}(t)}{v_{dc}(t)} \approx \frac{1}{0.5 - d_2(t)} \text{ with } d_2(t) = \frac{t_{on2}}{T_s}$$

$$= \frac{v_{c2}(t)}{V_{sw}}, \quad (28)$$

where t_{on1} and t_{on2} are, respectively, the time intervals when switches S_1 and S_2 conduct, and $v_{c1}(t)$ and $v_{c2}(t)$ are the control signals output from the system compensators that are provided as input signals to S_1 and S_2 .

4.2. Sample System Description

The WECU consists of a variable-speed wind turbine with a three-phase PMSG. The DC link in the wind farm is provided through a full-bridge diode rectifier in cascade with an interleaved boost DC-DC converter. The active power delivered to the power converter via the PMSG is of 1 MW at a 3-kV peak-to-peak line-to-line voltage. The input RMS line-to-line voltage to the active rectifier is calculated as $v_{LLrms}(t) = 3/\sqrt{2} = 2.12$ kV. The output DC voltage of the diode bridge rectifier and input to the interleaved DC/DC converter in Figure 3(b) are obtained by means of Eq. (4) in which $a_r = 1$ due to having no transformer on the AC lines. The out-put DC current of the diode bridge rectifier is calculated using Eq. (3). The fundamental AC line current is given by $i_{ls}(t) = SCC/v_{LLrms}(t)$, where SCC is the short-circuit capacity (in MVA), $SCC = P_{in}/PF$ with $P_{in} = 1$ MW, and PF is the power factor. The power factor definition is given in Eq. (29) [14, 22]:

$$PF = \frac{1}{\sqrt{1 + THD_i^2}} = DPF \quad (29)$$

where $DPF = \cos \phi$ is the displacement power factor, and $PF \approx 1$ due to the presence of an inner current loop controller that corrects DPF and mitigates the current ripples.

Boost inductors L_{b1} and L_{b2} are sized using Eqs. (12) and (13). The DC-link voltage, which is the output voltage of the interleaved DC/DC converter, is given as $v_{d0}(t) = 6$ kV; note that $i_{d0}(t) = P_0/v_{d0}(t)$. The losses in the power converter are assumed to be small, $P_0 \approx P_{in} = 1$ MW, where $i_{d0}(t)$ and P_0 are, respectively, the DC current and power outputs from the interleaved boost converter. From Eqs. (15)–(17), the following statement is true for the interleaved converter: $D_1 =$

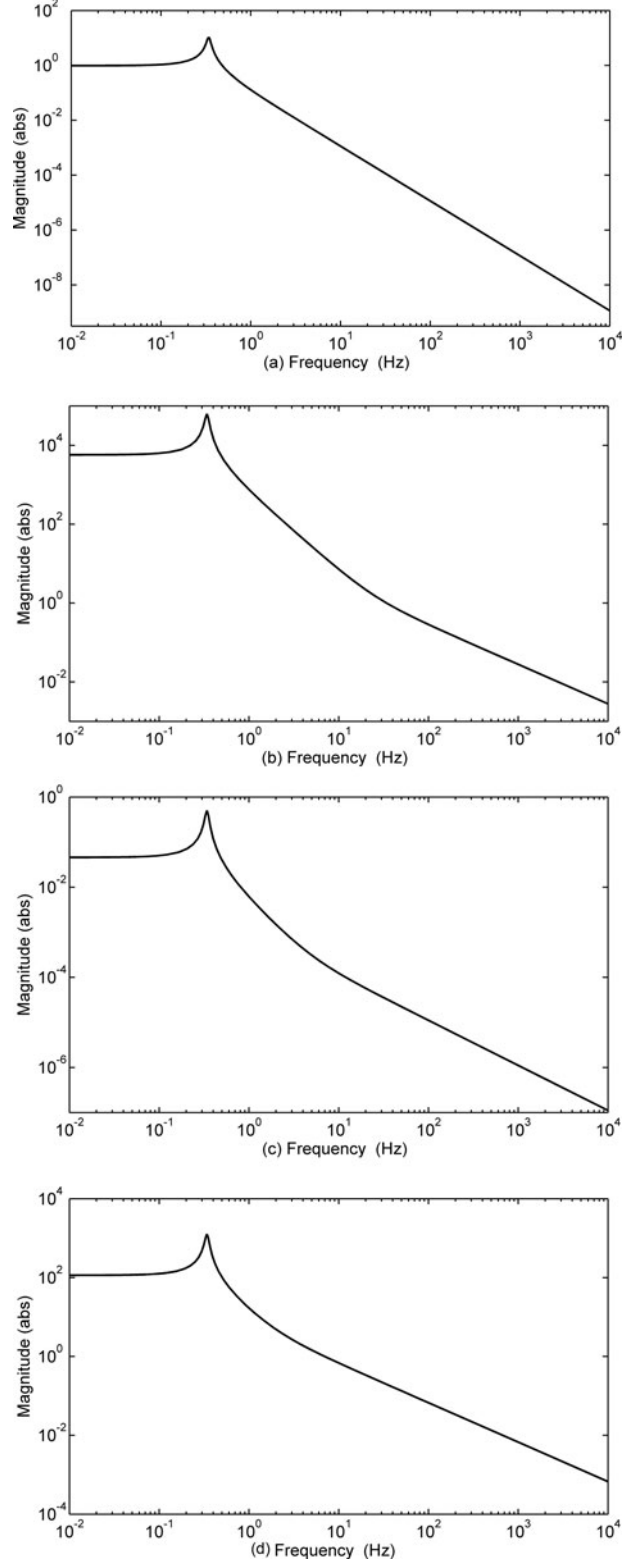


Figure 6. Open-loop transfer function: (a) signal model of $G_1(s)$, (b) signal model of $G_2(s)$, (c) signal model of $G_3(s)$, and (d) signal model of $G_4(s)$.

$D_2 = D_{1,2}$, $L_{b1} = L_{b2} = L_{b1,2}$, and $I_{dc1} = I_{dc2} = I_{dc12}$. An assumption made is that $V_{ce,sat} = V_{fwd} = 1V$ and $r_L \approx 0.5 \Omega$, and there are established methods to estimate these values found in [20]. The voltage and current ripples are expected to be maintained at approximately $\Delta i_{L_{b1}pk-pk} = \Delta i_{L_{b2}pk-pk} \leq 0.02 I_{dc12}$ and $\Delta v_{d0pk-pk} \leq 0.005 V_{d0}$. A switching frequency of 3 kHz is selected. The calculated values are given in Table 1. Note that in the analyses, the instantaneous values are used to represent the average quantities.

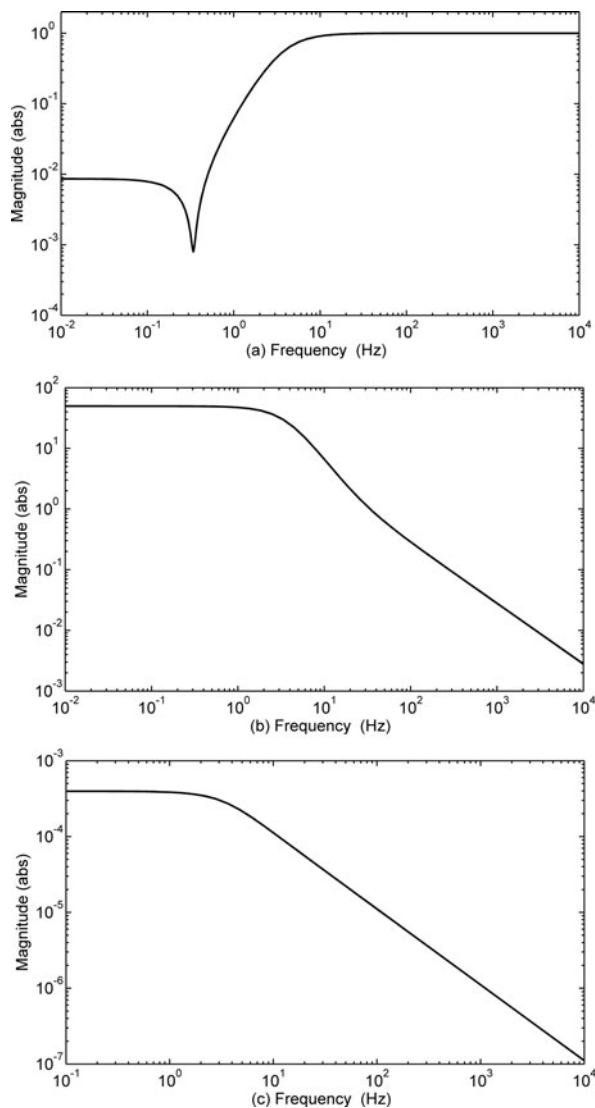


Figure 7. Closed-loop transfer function: (a) duty ratio and boost inductor current, (b) DC-link voltage and boost inductor current, (c) duty ratio and DC line voltage, (d) DC line voltage and DC-link voltage, and (e) voltage reference and DC-link voltage.

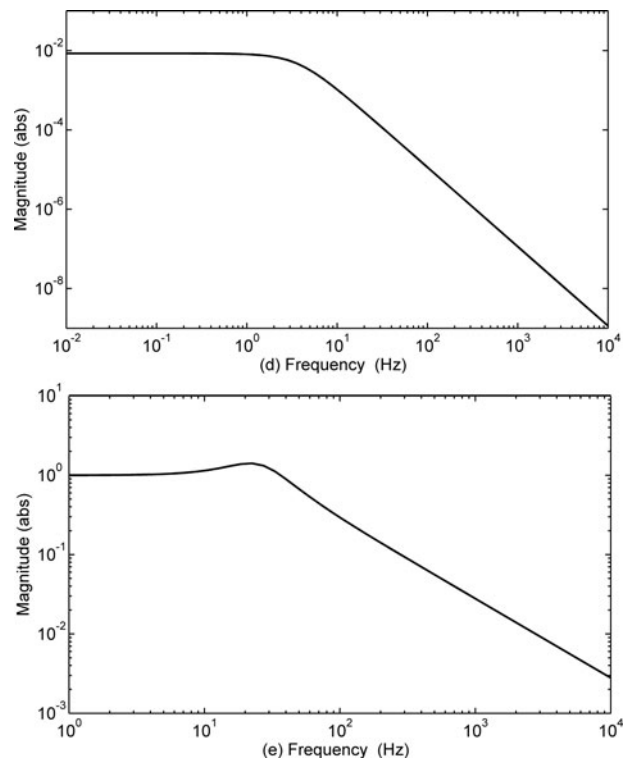


Figure 7. Continued

5. Discussion

The system performances of a WECU without a feedback controller in the power converter circuit are plotted in Figure 6. High disturbance amplification within the low-frequency regions and small amplification within the high-frequency regions are evident. The system presents a peak resonance at about 0.4 Hz. The amplification factor or rate of amplification recorded at the steady-state point around the switching frequency (3 kHz) are $|G_1(s)|_{3\text{kHz}} = 10^{-8}$, $|G_2(s)|_{3\text{kHz}} = 10^{-2}$, $|G_3(s)|_{3\text{kHz}} = 10^{-6.5}$, and $|G_4(s)|_{3\text{kHz}} \approx 10^{-3}$. In practice, each WECU in the wind farm has a PWM control loop in the power converter. The closed-loop signal models that include a PWM controller are derived in Eqs. (22)–(26), which are plotted in Figure 7. In the simulations, lossless sensors are assumed, and $H_i(s) = H_V(s) = 1$ is selected. The compensators are not included; hence, $G_C(s) = G_V(s) = 1$. There are stages in the operating process to decide whether to trigger or not to trigger the compensators in the feedback loops. For example, when power flow unbalance occurs between the generation and distribution systems, the compensators within the power converter in each WECU may be activated to balance power flow in the grid.

From Figure 7, the disturbances amplification within the low-frequency region is improved except for the transfer function, which links the boost inductor current and the DC-link

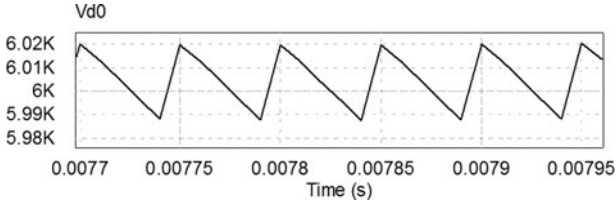


Figure 8. DC-link voltage output to the WECU.

voltage in Figure 7(b), where the amplification factor is about 80 (abs) up to 6 Hz. A small peak resonance is recorded at about 3 Hz in Figure 7(e). At the steady-state operating point or at 3 kHz, the amplification factors are recorded as follows: $A(t) = 1$ in Figure 7(a), $A(t) = 10^{-3}$ in Figure 7(b), $A(t) = 10^{-7}$ in Figure 7(c), $A(t) = 10^{-8}$ in Figure 7(d), and $A(t) = 10^{-2}$ in Figure 7(e). There is no attenuation of variations in Figure 7(a) and Eq. (22); thus, a current compensator is needed in the loop to mitigate the current variations.

The output DC-link voltage of the WECU is plotted in Figure 8 using Psim (The Powersim, Rockville, USA). The average DC-link voltage is recorded about $v_{d0}(t) = 5.965kV$; the peak-to-peak voltage ripple is $\Delta v_{d0 \text{ peak-peak}} = 0.03kV$. The small ripples in the DC-link voltage can be completely mitigated by selecting a large boost capacitor.

6. CONCLUSION

The investigations done in this article introduce a DC collector into an offshore wind farm to replace the currently used AC collectors. The studies that have been previously done in this area use the full-bridge VSC topology to replace the power transformer in which high power loss is experienced due to the high switching rate of semiconductor cells. This article proposed the use of a cascade connection of a diode rectifier and an interleaved boost converter to replace the power transformer. The power loss is expected to be lower due to the reduction of conduction and switching losses. The peak and RMS DC current flowing through switches is also reduced as a result of interleaving. The dynamic model of the proposed topology is derived, and the control system performance is tested. It is observed that disturbance amplification is very high within the very low-frequency region. The amplification factor is improved when operating within the high-frequency region. A current compensator needs to be integrated in the PWM controller circuit to mitigate the DC current variations. The voltage compensator should also be included in the PWM control circuit to prevent any risk of DC-link voltage variations. The design of voltage and current compensators to be integrated in the PWM controller loops is part of further investigations.

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