A 6-bit, 500-MS/s current-steering DAC in SiGe BiCMOS technology and considerations for SFDR performance

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Abstract

This paper presents a six-bit current-steering digital-to-analogue converter (DAC), which optimises the spurious free dynamic range (SFDR) performance of high-speed binary weighted architectures by lowering current switch distortion and reducing the clock feedthrough effect. A novel current source cell is implemented that comprises heterojunction bipolar transistor current switches, negative-channel metal-oxide semiconductor (NMOS) cascode and NMOS current source to overcome distortion by specifically enhancing the SFDR for high-speed DACs. The DAC is implemented using silicon-germanium (SiGe) BiCMOS 130 nm technology and achieves a better than 21.96 dBc SFDR across the Nyquist band for a sampling rate of 500 MS/s with a core size of 0.1 mm^2 and dissipates just 4 mW compared to other BiCMOS DACs that achieve similar SFDR performance with higher output voltages, resulting in a much larger power dissipation.

Keywords: Digital-analogue conversion, BiCMOS integrated circuits, Dynamic range, Analogue-digital integrated circuits, Mixed analogue digital integrated circuits, Wideband.

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Article outline

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1. Introduction

The spurious free dynamic range (SFDR) of high speed, digital-to-analogue converters (DACs) is a key specification in a variety of applications such as electronic warfare (EW), wideband communications and software-defined radio. Unwanted spurious signals generated by the DAC degrade the bit error rate of wideband communication systems and the effectiveness of wideband EW systems [1], [2].

Requirements for meeting the desired SFDR performance of sampled signals close to the Nyquist rate will become more stringent because of the trade-off between the SFDR and sampling rate [3]. The degradation of the SFDR performance can be attributed to static and dynamic non-linearity [1], [4]. Static non-linearity arises from the mismatch between transistors, while dynamic non-linearity can be attributed to switching characteristics and finite output impedance of the current source cells [1]. The dynamic non-linearity worsens as the sampling rate increases and is usually the limiting factor in achieving good SFDR in high-speed DACs [1].

The most widely used architecture in high speed applications is the current-steering DAC, fabricated using complementary metal-oxide semiconductor (CMOS) technology [3]. The

current source cell finite output impedance, switch distortion and clock feedthrough are the greatest contributors to dynamic non-linearity and are difficult to improve with the use of MOS devices alone [3], [5] and [6]. Bipolar and CMOS (BiCMOS) technology offers high-speed and high-gain heterojunction bipolar transistors (HBT) that, when combined with MOS devices, are able to improve on the linearity of the current-steering DAC and hence, improve the SFDR.

This paper focused on the use of silicon-germanium (SiGe) BiCMOS technology to lower distortion, increase output impedance and reduce the clock feedthrough effect, to improve the SFDR in comparison to a CMOS-only implementation for EW applications where SFDR and high speed are the primary concerns while power is a secondary concern. The mathematical and system design of a high-speed, low spurious DAC is considered and an experimental or design approach that places emphasis on constraints in modern fabrication processes is synthesised. This approach is then applied to the design of a six-bit current-steering binary weighted DAC. Subsequently, the layout and measurement of the DAC are presented for experimental verification and validation.

2. Mathematical and System Design

2.1 Architecture Selection

The primary functions of the DAC are current generation, current steering and control of the current steering. The secondary functions of the DAC are signal conditioning, biasing and high-speed digital inputs. The application, speed and area specifications of the DAC determine the optimal weighting of the current source cells which are unary or binary weighted.

The circuit configuration for the current source cell is shown in Fig. 1. The current source cell comprises a current source, cascode and switch transistors. The input word controls the number of current source cells that are connected to the DAC output.

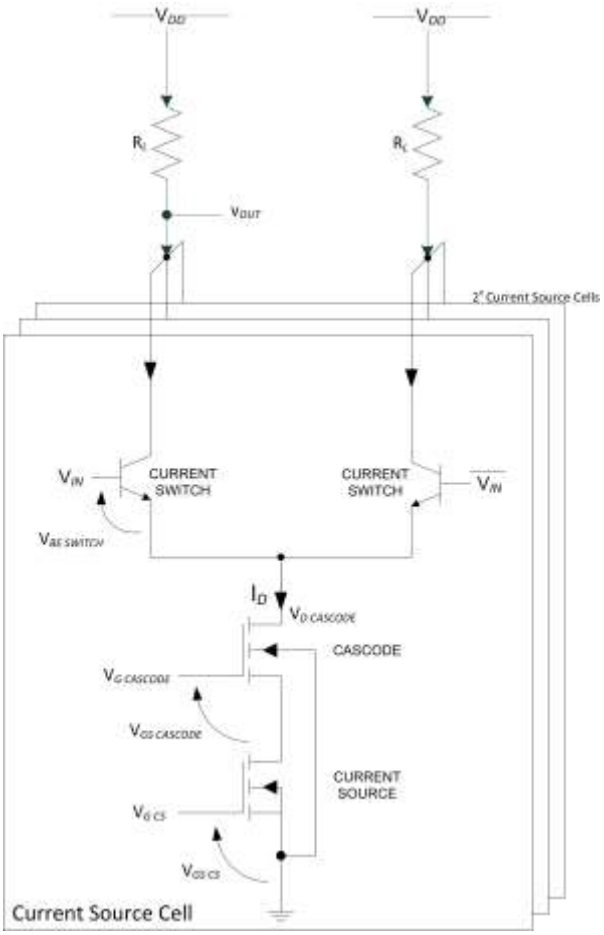


Fig. 1: Current source cell.

The unary weighted DAC employs a thermometer decoder to control each of the current sources individually, relaxing matching requirements and lowering the glitch energy at the expense of increased area and design complexity. In a binary weighted DAC, the current sources are directly controlled from the DAC input, resulting in a smaller area, decreased design complexity and more importantly, increased speed. These benefits come at the expense of worse differential non-linearity (DNL) and glitch energy owing to the stringent matching requirements and input-dependent non-linearity.

While a thermometer-decoded unary weighted DAC will achieve better linearity and reduce glitch energy, a binary weighted implementation is selected as the architecture for improved speed. The selection of the number of bits places a finite restriction on the DACs dynamic range owing to the amplitude quantization effect approximated by:

$$\frac{S}{N} = 6.02\,N + 1.76\,dB \quad (1)$$

For every bit increase, the required current source cell matrix area will double. In addition to this, to meet the matching requirements, the area occupied by a single current source cell will also double. For each bit increase, the total layout area increases by a factor of four. The layout and decoding also become more complex with higher resolution.

The number of input-output (I/O) pins also increases for every bit increase. As this design was processed as a multi-project wafer (MPW), the chip area and I/Os are shared across multiple designs. The layout, bonding wire and pad constraints limit this design to six bits because of the availability of a maximum of 21 I/O pads. A resolution of six bits is chosen, which places a limit of approximately 37.88 dB on the signal-to-noise ratio. The choice is however appropriate for testing the key SFDR principle proposed through this paper.

2.2 Matching Requirements for DNL

The DNL is the worst case deviation from an ideal least significant bit (LSB) step between two subsequent output codes and is of particular importance when generating small signals. A monotonic DAC meets the criterion that for each subsequent digital input code, the output analogue value increases. The DAC design must be constrained to guarantee the desired monotonic behaviour.

In all practical DACs, the quantization steps have limited accuracy because of a mismatch between design elements such as transistors. The DNL specification is architecture-dependent [5]. In a binary weighted converter, the maximum DNL must be less than twice the maximum integral non-linearity (INL) [5]. In order to guarantee monotonic behaviour for a binary weighted converter, the following relationship must be satisfied [5]:

$$\mathrm{DNL} < 2 * INL = 2 * 0.5\,LSB = 1\,LSB \quad (2)$$

However the DNL specification is usually specified to be more stringent:

$$\mathrm{DNL} < 0.5\ LSB\ . \tag{3}$$

The DNL specification together with the INL will impose a requirement on the matching accuracy. While every transition of the input digital word will need to satisfy this requirement, the most stringent matching requirement is architecture-dependent.

For a binary weighted converter, the midscale transition is the most stringent. For an *N* bit binary weighted converter, the midscale transition is between word (2^{N-1}) and $(2^{N-1} - 1)$. At this transition, $(2^{N-1} - 1)$ current sources must match within 0.5 LSB of (2^{N-1}) unrelated current sources. The current sources are assumed to exhibit an approximately normal distribution according to the central limit theorem.

A good approximation for the DNL is the standard deviation of current for a single increase in the quantization level, which is represented by $\sigma(\Delta I)$. The DNL is calculated at the worst case scenario, which occurs at the DAC mid-scale transition:

$$\begin{gathered}\sigma^2(\Delta \mathrm{I}) = \sigma^2(2^{N-1}I - (2^{N-1} - 1)I) \\ \frac{\sigma(\Delta \mathrm{I})}{\mathrm{I}} < 0.063\ or\ 6.3\%\end{gathered} \tag{4}$$

The result is that the standard deviation for each current source must be within 6.3% to meet the DNL specification.

2.3 Matching Requirements for INL

The INL is the worst case deviation of the actual DAC output from an ideal DAC output across all quantization levels. The INL determines the overall DAC linearity and is important for large signals [5]. In order to guarantee monotonic behaviour, relationship (5) must be satisfied:

$$INL < 0.5\ LSB \tag{5}$$

The matching is influenced by the process gradient of the manufacturing process. The INL yield is the percentage of DACs manufactured that meet the INL linearity specification. The INL yield was introduced to compute the standard deviation of a unit current source quantitatively to meet INL specifications [7]. In order to characterise the INL yield statistically, Monte Carlo simulations are typically required. Monte Carlo simulations are processor-intensive, time-consuming and do not provide the designer with insight into the trade-offs required to improve the INL yield [7].

A more insightful yet accurate method resulting in parametric expressions was introduced in [7] and will be followed to derive the matching requirements to meet the INL specification. The problem may be approached in two ways. The first is to specify the required INL and then derive the minimum required current-matching accuracy and INL yield. The alternative and more useful approach, which is to specify the required INL yield and then derive the minimum required current matching-accuracy, is followed. Following the approach in [7], the standard deviation for a unit current source cell is:

$$\sigma < \frac{A}{\sqrt{2}^{N}} Z(Y) \tag{6}$$

The parameter *A* represents the INL specification in the units of LSB, which is 0.5 for this design. The parameter *N* represents the number of bits resolution of the DAC. The INL yield requirement determines *Z(Y),* which is well tabulated in the literature and is derived via Monte Carlo simulations. An INL yield of 99% is selected for this design, resulting in a *Z(99%)* of 0.5. Substituting the INL yield and *Z(99%)* into Eq. (6) results in 3.12%. The INL matching requirement therefore results in the required standard deviation of each current source being within 3.12%. The INL matching requirement is more stringent than the DNL matching requirement for this design and will be used to design the current sources.

2.4 Current Source Transistor Design

2.4.1 General considerations

Based on the Pelegrom model, for a given technology the relative standard deviation of a current source is determined by its overdrive voltage and gate area [7]. Three degrees of

freedom are available to achieve the required matching, namely the current source width, length and overdrive voltage.

The available voltage headroom, which is determined by the output voltage swing and voltage drop over the switch transistors, places a constraint on the overdrive voltage. Ideally, the overdrive voltage would be made as large as possible to achieve the required current with minimal transistor area. However the matching constraints require the transistor width and length to be made as large as possible to increase the gate area.

In this particular design, the *IBM 8HP* technology, which is a 130 nm SiGe BiCMOS process, imposes very low voltage headroom at 1.2 V. Unlike designs in the 1990s and early 2000s, the voltage headroom has become the most stringent constraint and will be prioritised over matching constraints. The output impedance is 50 Ω and for a 100 mV output full scale voltage swing results in a total output current of 2 mA. Each unit current source supplies 31.25 μA of current.

Because of the available voltage headroom, a metal oxide field effect transistor (MOSFET) is the only practical choice for the current source transistor. As the performance and matching of the NMOS is better than its positive-channel metal-oxide semiconductor (PMOS) counterpart, a current sink design is selected. The current source transistor would ideally produce a constant current independent of the voltage across it, which is closely represented by a MOSFET biased in the constant-current region.

The variation in threshold voltage and current gain determines the transistor matching. The analysis of MOS matching models in [5] derives two matching models based on the current density of the transistor. For small current densities, the threshold voltage matching primarily determines the current matching. For large current densities, the slope mismatch primarily determines the current matching. The small and large current density mismatch equations may be combined to form a single equation:

$$\frac{\Delta I_D}{I_D} = \left(\frac{\Delta\beta}{\beta} + \frac{2\Delta V_{th}}{V_{gs} - V_{th}}\right)\frac{1}{\sqrt{WL}} \quad (7)$$

A higher transistor gate area improves matching. There are two conflicting constraints on the overdrive voltage [8]. The first is that the overdrive voltage is made larger in order to minimise the transistor dimensions and thus the overall area. The second is that the overdrive voltage is limited by the amount of available voltage headroom determined by the output voltage swing, drain to source voltage of cascode, and collector-to-emitter voltage of the switch transistors.

Based on the design manual for the process, for identical devices with the same orientation separated by less than 200 µm, the mismatch in the device current at the final wafer test has been characterised. Adjacent MOSFET devices are modelled as in the published literature by a combination of threshold voltage and mobility mismatch terms that varies in proportion to the inverse root of the area product.

There are also further factors influencing the calculation in submicron technology. The short-channel effects, such as drain-induced barrier lowering, mobility reduction and interdependence of threshold voltage on transistor dimensions and gate voltage, complicate the design process.

2.4.2 Transistor dimensions and voltages

From the design manual for the *IBM 8HP* process, the threshold voltage to bias an NMOS into the constant-current region is 0.355 V. The power supply voltage, V_{DD}, in this design is 1.2 V. The output voltage swing, v_{out}, is 100 mV. This leaves a total of 1.1 V to be used by the current source, current switch transistors and possibly a cascode transistor. The $V_{GS\ CS}$ is chosen to be approximately equal to the classical threshold voltage at 350 mV, as the voltage headroom is severely limited. The classical threshold voltage will be lowered by the drain-induced barrier-lowering (DIBL) effect.

At submicron process nodes, the influence of the drain potential on the channel region can have a serious impact on the performance of submicron MOS transistors. The drain current

is controlled not only by the gate voltage, but also by the drain voltage. For device-modelling purposes, DIBL can be accounted for by a threshold voltage reduction depending on the drain voltage.

The drain voltage of the current source transistor is required to calculate the DIBL effect but can be estimated by assuming the voltages over the cascode NMOS and switch HBT transistor. The total voltage across the drain of the cascode transistor to ground is:

$$V_{D\,cascode} = V_{DD} - V_{BE\,Switch} = 1.2 - 0.726 = 0.474\ \mathrm{V} \tag{8}$$

The next assumption is that the drain-to-source voltage of the current source and the cascode are equal, which will be realised later in this design. Hence the $V_{DS\,CS}$ of the current source is 0.236 V. With these assumptions, the effect of DIBL on the current source threshold voltage may be estimated:

$$\begin{aligned} \mathrm{DIBL} &= \frac{\Delta V_{th}}{\Delta V_{ds}} \\ V_{th|Vds=0.25} &= 284.65\ mV \end{aligned} \tag{9}$$

The transistor dimensions to achieve the required current per unit current source from the equation for an n-channel device operating in the constant-current region is:

$$\frac{W}{L} \cong 5 \tag{10}$$

In digital designs, the transistor area is minimised in order to integrate more transistors on the die. However in analogue and mixed signal design, the gate density is not the primary concern. It has already been established that a higher gate area improves matching, which is the primary reason to avoid minimum dimension transistors. The secondary reason to avoid minimum dimension transistors is that second-order short-channel effects are more pronounced at channel lengths below 1 µm. The selection of the transistor drawn length is

chosen to be 2 µm to avoid short-channel effects and increase the gate area for matching purposes. This leaves the drawn width at 10 µm.

2.4.3 Matching Requirements

The current matching for a unit current source may now be calculated closing the loop of parameters for the current source transistor, using the mismatch equation (7). The overall device mismatch is calculated to be 0.921%, satisfying the matching requirements of static linearity. A matching analysis is conducted to verify the above calculations.

A corner simulation would allow the designer to verify the design functionality at the global process boundaries. In the DAC current source cell matrix, the effect of the local process mismatch primarily determines the SFDR performance. As the DAC design is primarily an analogue design, a Monte Carlo analysis is a more useful tool, as a corner simulation would only provide insight on the global process variations, but a Monte Carlo simulation allows for variance of local and global process parameters.

Monte Carlo statistical simulations provide the best approximation of the circuit performance variation over the manufacturing process window. Multiple simulations are run to vary the temperature, process and device parameters within the expected distribution. Statistical simulations can also explore the effects of mismatch between like devices within a chip. The Monte Carlo analysis predicts a device mismatch variance of 0.6 %, which is better than the calculated mismatch.

2.5 Cascode Transistor Design

The effect of finite output impedance on the DAC is distortion, as the effective load impedance is dependent on the digital input code. Equation (11) is used to predict the effect of finite output impedance on SFDR [9], [10] and [11]:

$$SFDR = 20log\left(\frac{R_{OUT}}{R_L}\right) - 6.02(N-2) \quad (11)$$

R_{OUT} is the total output resistance of the current source cell, while R_L is the load resistance. The single transistor current source has an output impedance of 44 kΩ, limiting the SFDR to 34 dB. The output impedance also affects the static linearity of the DAC, as shown in [5], [12] and [13]:

$$INL = \frac{I_{unit} {R_L}^2 N^2}{4R_{OUT}} \tag{12}$$

However, the dynamic requirements impose more stringent requirements and hence the static case is not pursued further. In order to increase the output impedance, a cascode current source is used. With the addition of an active load, the output impedance is increased. The cascode transistor may either be a common-source NMOS or common-base HBT. Both have a multiplier effect on the output impedance of the current source.

The cascode transistors should be biased in the constant-current region [12]. The total allowable voltage for the cascode and current source transistors are 0.5 V. This is due to the current switch transistors, which consume half of the available voltage headroom. This leaves a remainder of 0.25 V for the cascode transistor.

An HBT exhibits higher transconductance in comparison to the NMOS, which results in a higher achievable output impedance. If the HBT is selected, the HBT base voltage of the cascode transistor would be approximately 0.95 V. In order to keep this transistor in the saturation, an HBT collector voltage of at least 0.95 V is required, which cannot be handled within the available voltage headroom.

An NMOS would however be able to operate within the constant-current region with a gate overdrive voltage of greater than 0.25 V. The gate voltage would need to be greater than 0.5 V in order to keep the cascode NMOS in the constant-current region. Selecting a $V_{GS\ CASCODE}$ of 0.35 V; similar to the current source transistor, results in a gate voltage, $V_{G\ CASCODE}$ of 0.6 V. The predicted SFDR with the inclusion of the cascode transistor is 56.5 dB because of the increase in output impedance to 560 kΩ.

2.6 Current Switch

Most modern high-speed DACs with resolution under 8 bits operate on the principle of current steering [14]. Based on the input word, current is steered to either the positive or negative output. The steering of current as opposed to switching of current improves performance. The current switches are designed with HBT devices owing to the switching speed. The device biasing needs to ensure that the transistors always operate within the forward active region to avoid distortion.

If the input voltage, V_{IN} is selected to equal V_{DD}, the emitter voltage of the switching transistors is 450 mV. The worst case conditions that the device needs to operate within the forward active region occur when all the current sources are simultaneously on or off. In this case, the collector voltage of the switch transistor may fall to 1.1 V. The current switch transistors will operate within the forward active region even in the worst case condition, as the saturation voltage is 0.2 V.

The performance of the HBT-based current switch design is compared to a typical NMOS-based current switch. A transient simulation is run with a square wave stimulus on the HBT and NMOS-based current switch circuit configurations. The voltage output of the HBT-based current switch and NMOS-based current switch is shown in Fig. 2, illustrating the clock feedthrough effect.

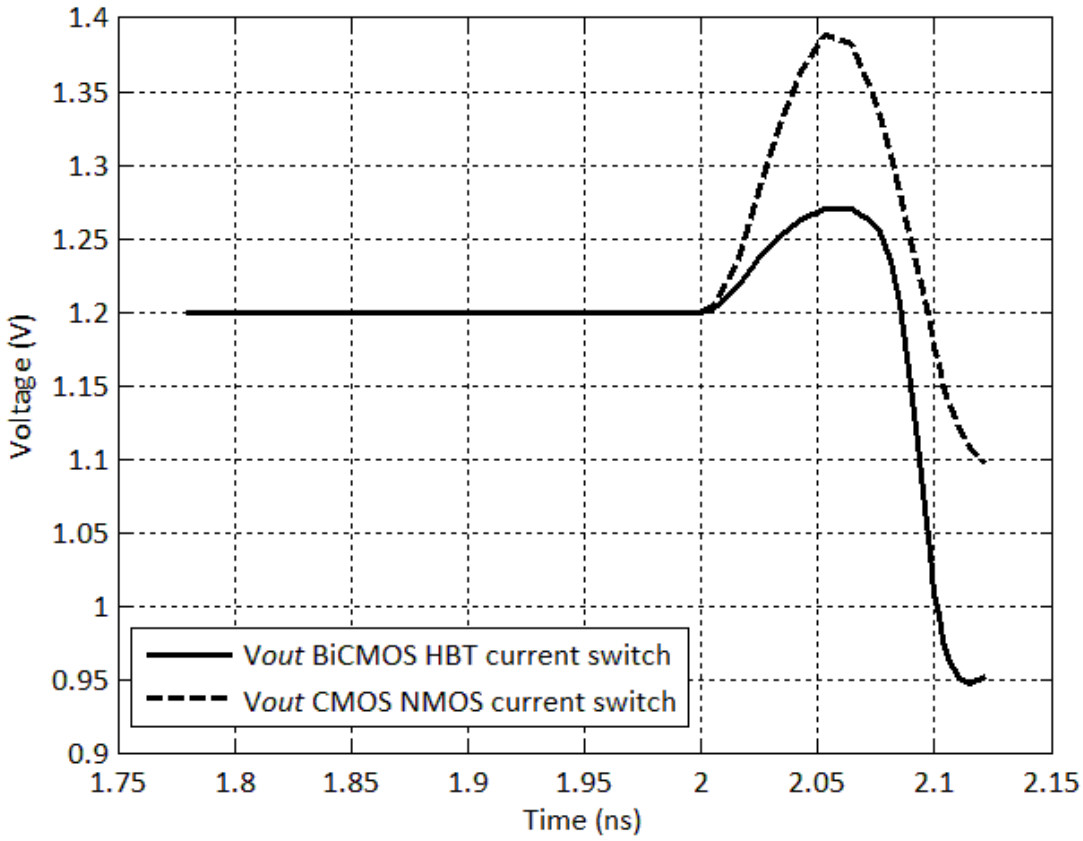


Fig. 2: Transient response of BiCMOS HBT-based current switch (solid) and CMOS NMOS-based current switch (dash).

In order to quantify this effect, the area between the actual voltage and ideal voltage curves may be used. The HBT-based current switch transient response is closer to the ideal response in comparison to the NMOS current switch. Table 1 summarises the total clock feedthrough distortion simulation results.

TABLE 1.

Clock feedthrough distortion measurements.

Current Switch Implementation	**Clock Feedthrough Distortion**
BiCMOS (HBT current switch)	~ 3.75 pV/s
CMOS (n-channel current switch)	~ 8.65 pV/s

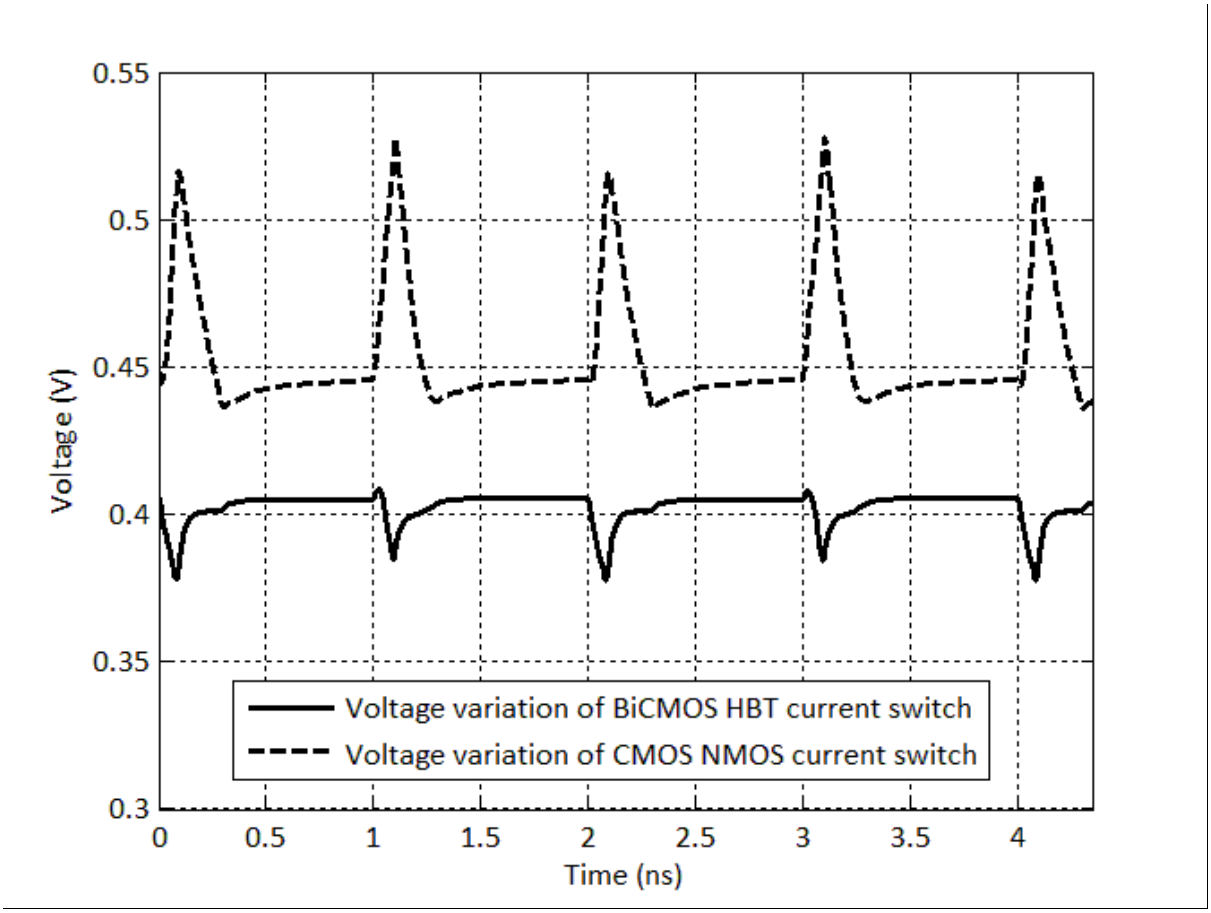


Fig. 3: Voltage variation of the drain of the current source transistors in BiCMOS HBT-based current switch (solid) and CMOS NMOS current switch (dash) illustrating clock feedthrough distortion.

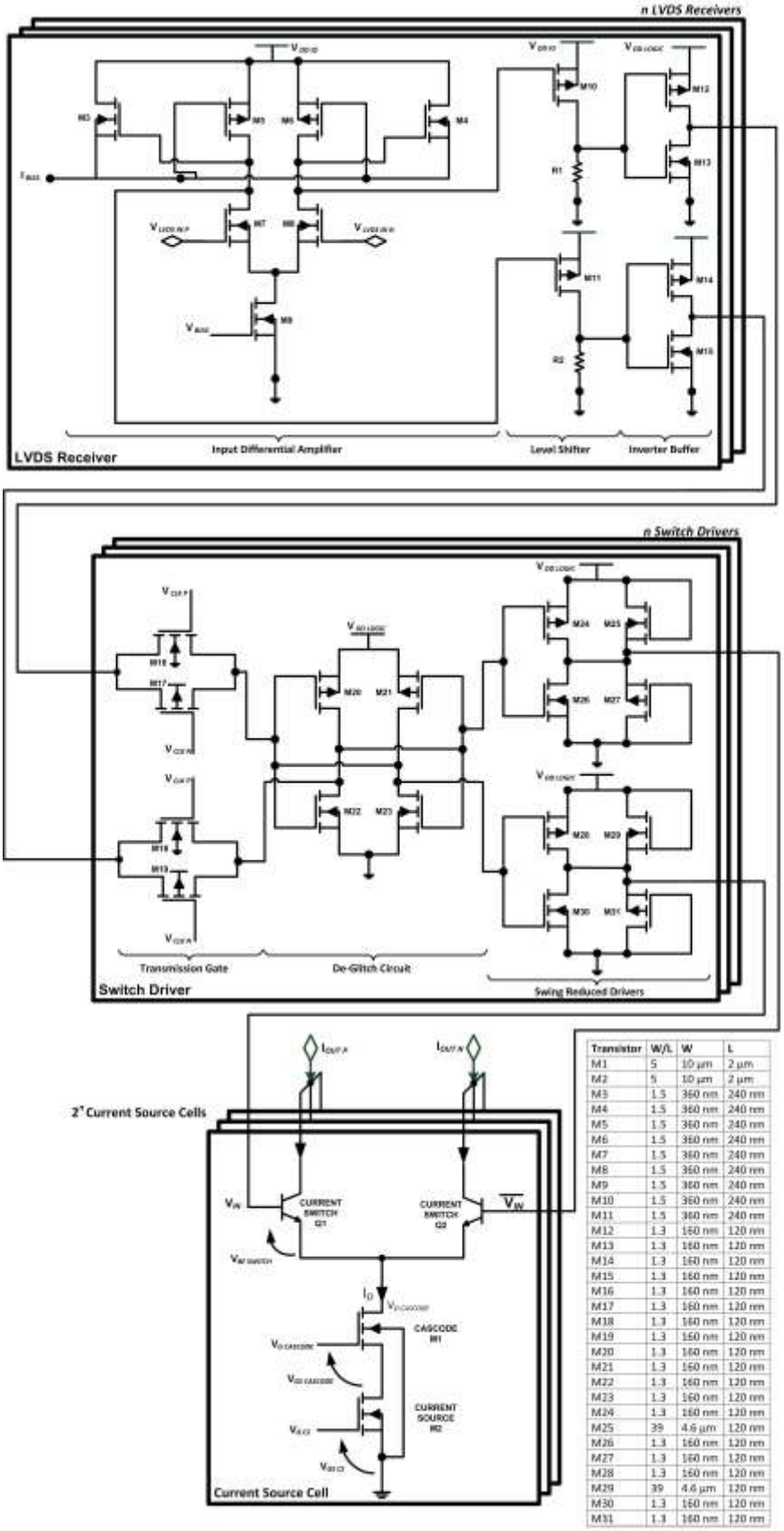
Clock feedthrough distortion is improved in the BiCMOS HBT-based current cell when there is less voltage variation at the drain of the current source transistors, as shown in Fig. 3. The BiCMOS HBT-based current source cell improves performance in comparison to a CMOS-only current source cell, as the clock feedthrough distortion are improved for a BiCMOS HBT-based implementation.

2.7 Complete DAC

The current source cell design is replicated multiple times for each quantization level and arranged in a matrix to form a current source cell matrix. Bias, switch driver and low-voltage differential signalling (LVDS) receiver circuits are designed using standard CMOS logic.

To enable the DAC to operate at high sampling rates, an LVDS input stage was designed based upon [10], [15] and [16], that consists of a differential amplifier followed by a level shifter and inverter buffer. The LVDS circuit transfers the signals from the I/O signal voltage to the internal digital logic voltage. On-chip termination of the LVDS signals was used to reduce reflections on the high speed inputs.

A switch driver was designed to transfer the full scale control signals from the LVDS receiver and derive signals that swing in a limited range to drive the current switches. The switch driver comprises of a latch and swing reduced driver (SRD). The CMOS latch design is based on [12] as it creates the steepest transition and shortest delay in comparison to common mode logic latches. The SRD design is based on [17] and drives the current switches with signals from 0.55 V to 1.1 V to minimize the clock feedthrough effect. The complete annotated DAC design is shown in Figure 4. A transient simulation of the DAC output when switching between digital codes 0 to 63 is graphed in Fig. 5 that illustrates the dynamic switching of the full DAC circuit.



Transistor	W/L	W	L
M1	5	10 µm	2 µm
M2	5	10 µm	2 µm
M3	1.5	360 nm	240 nm
M4	1.5	360 nm	240 nm
M5	1.5	360 nm	240 nm
M6	1.5	360 nm	240 nm
M7	1.5	360 nm	240 nm
M8	1.5	360 nm	240 nm
M9	1.5	360 nm	240 nm
M10	1.5	360 nm	240 nm
M11	1.5	360 nm	240 nm
M12	1.3	160 nm	120 nm
M13	1.3	160 nm	120 nm
M14	1.3	160 nm	120 nm
M15	1.3	160 nm	120 nm
M16	1.3	160 nm	120 nm
M17	1.3	160 nm	120 nm
M18	1.3	160 nm	120 nm
M19	1.3	160 nm	120 nm
M20	1.3	160 nm	120 nm
M21	1.3	160 nm	120 nm
M22	1.3	160 nm	120 nm
M23	1.3	160 nm	120 nm
M24	1.3	160 nm	120 nm
M25	39	4.6 µm	120 nm
M26	1.3	160 nm	120 nm
M27	1.3	160 nm	120 nm
M28	1.3	160 nm	120 nm
M29	39	4.6 µm	120 nm
M30	1.3	160 nm	120 nm
M31	1.3	160 nm	120 nm

Fig. 4: Annotated DAC schematic illustrating the full DAC chain from the DAC digital input to the DAC analogue output.

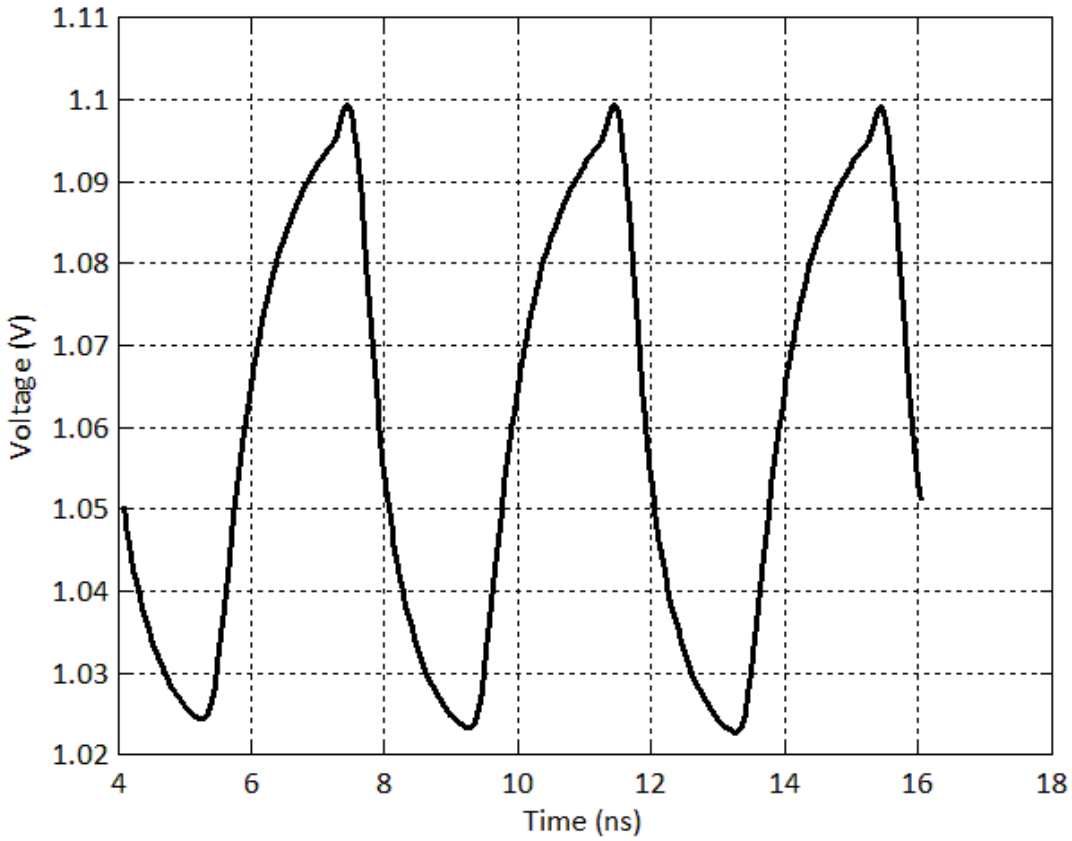


Fig. 5: Voltage variation at the DAC output with input code switching between lowest and highest values.

3. Layout

A full custom layout methodology is followed. The DAC layout was combined with three other designs to form the layout used for fabrication. The layout of each sub-circuit is constructed as a cell and reused across the design. This is especially useful for the current source cell matrix that consists of many current source cells which are laid out as a matrix. Packaging, bonding and fill requirements are considered during the layout stage. Ground and power pads are distributed to ensure minimal ground bounce, lower inductive noise coupling and better heat dissipation. Power and signals are routed across separate metal levels. Nets that are common to current source cells such as power, switch inputs and current outputs are routed vertically or horizontally fully across the layout from edge to edge allowing for reuse.

The overall layout area is 2 mm by 2 mm, which includes the dummy fill cells. The active DAC area is significantly smaller and is approximately 500 µm by 200 µm or 0.1 mm^2. The completed layout was fabricated via the MOSIS Educational Program through an IBM foundry. A micrograph of the unpackaged die is shown in Fig. 6 with the DAC quadrant of the MPW annotated.

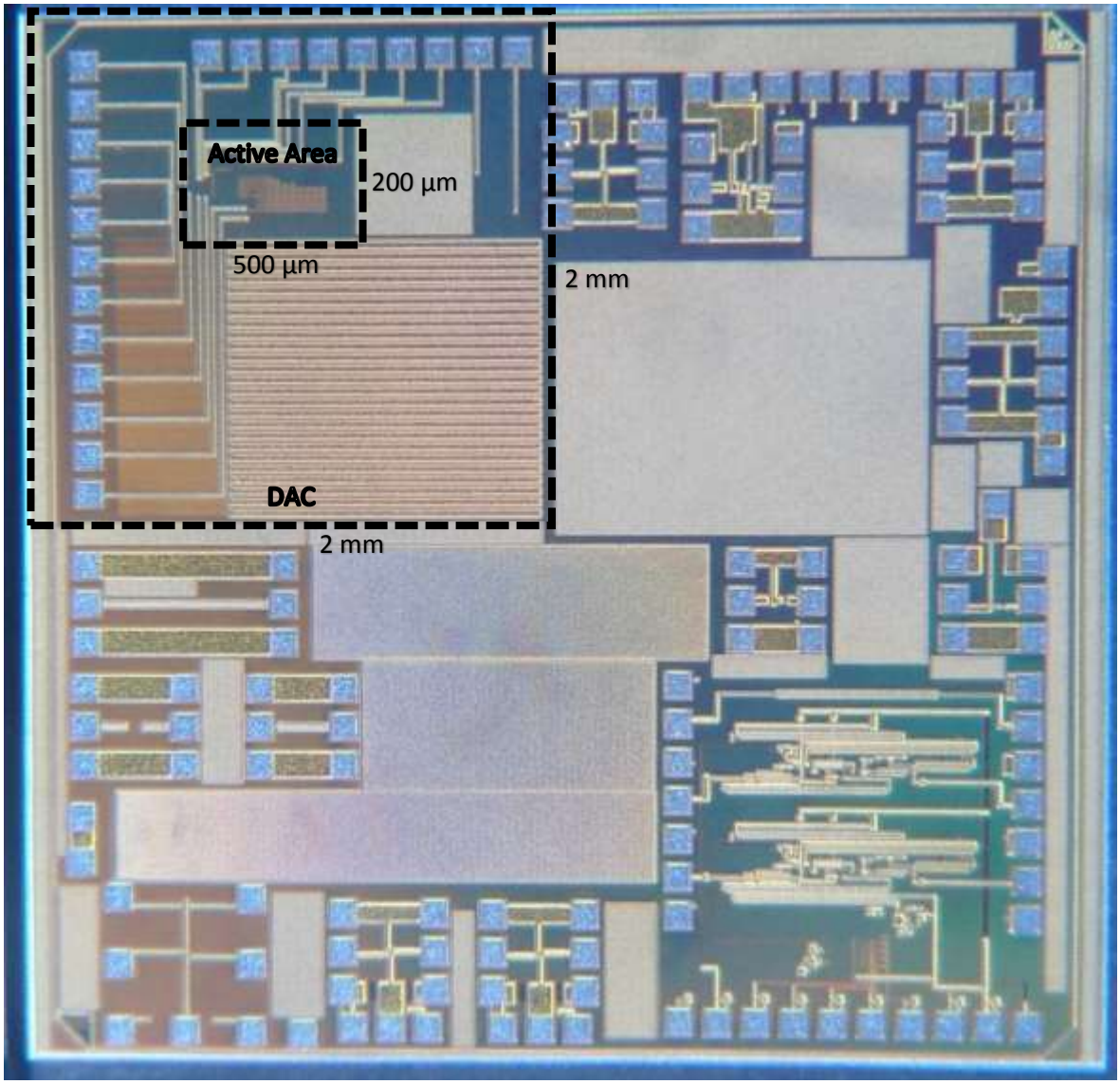


Fig. 6: Micrograph of complete MPW integrated circuit with DAC on the upper left quadrant.

4. Measurement and Results

The fabricated DAC is packaged in a quad flat no leads package and mounted on a printed circuit board. The PCB conforms to the FPGA mezzanine card (FMC) form factor and supplies power and signal interconnections to the DAC. For this design, the DAC FMC card is

connected to a processor motherboard. The processor motherboard drives the FMC signals with high-speed LVDS signals from an FPGA. The measurement setup is shown in Fig. 7.

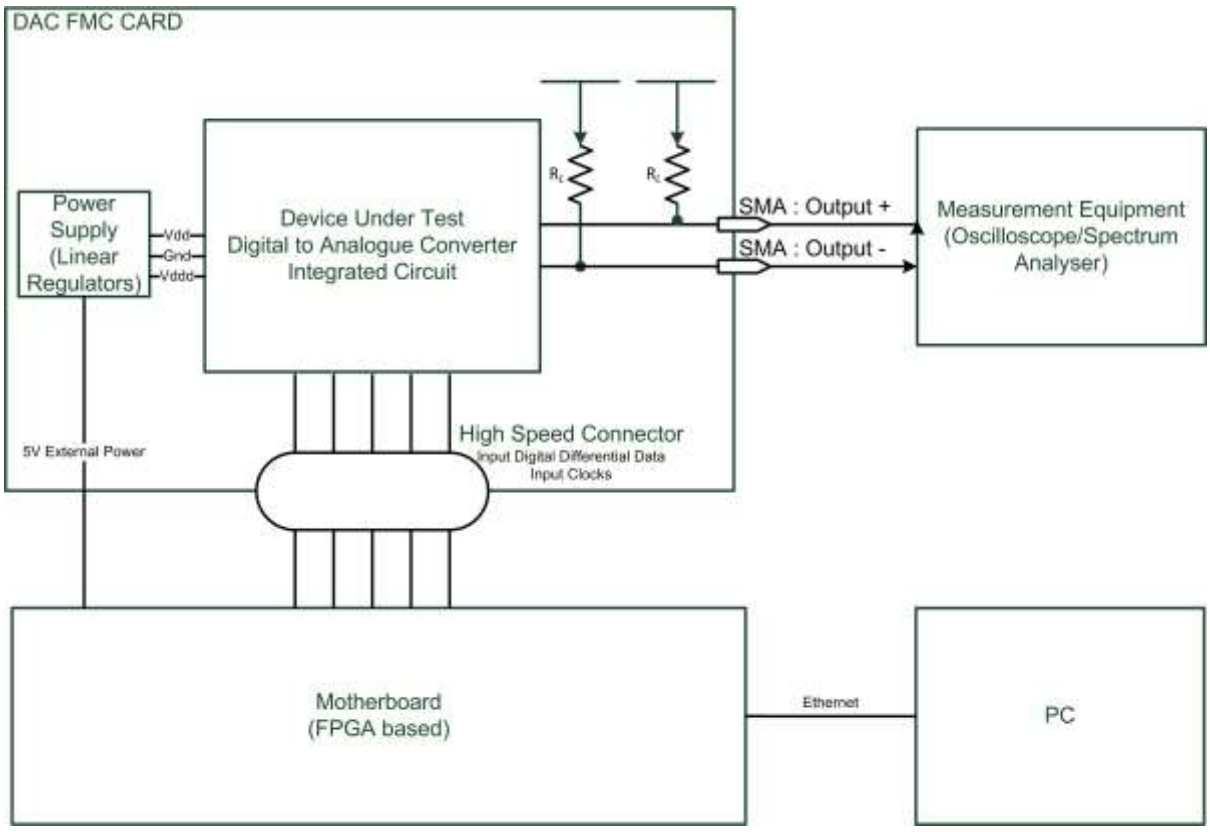


Fig. 7: Measurement setup.

In order to generate waveforms through the DAC, a waveform table is generated on a standard PC and downloaded onto the FPGA based motherboard over an Ethernet connection. The FPGA is triggered to read the waveform values and drive the DAC digital interface and clock signals. The DAC FMC card derives the power signals for the DAC IC using linear regulators for signal integrity from the motherboard external power connection. The processor motherboard is shown in Fig. 8.

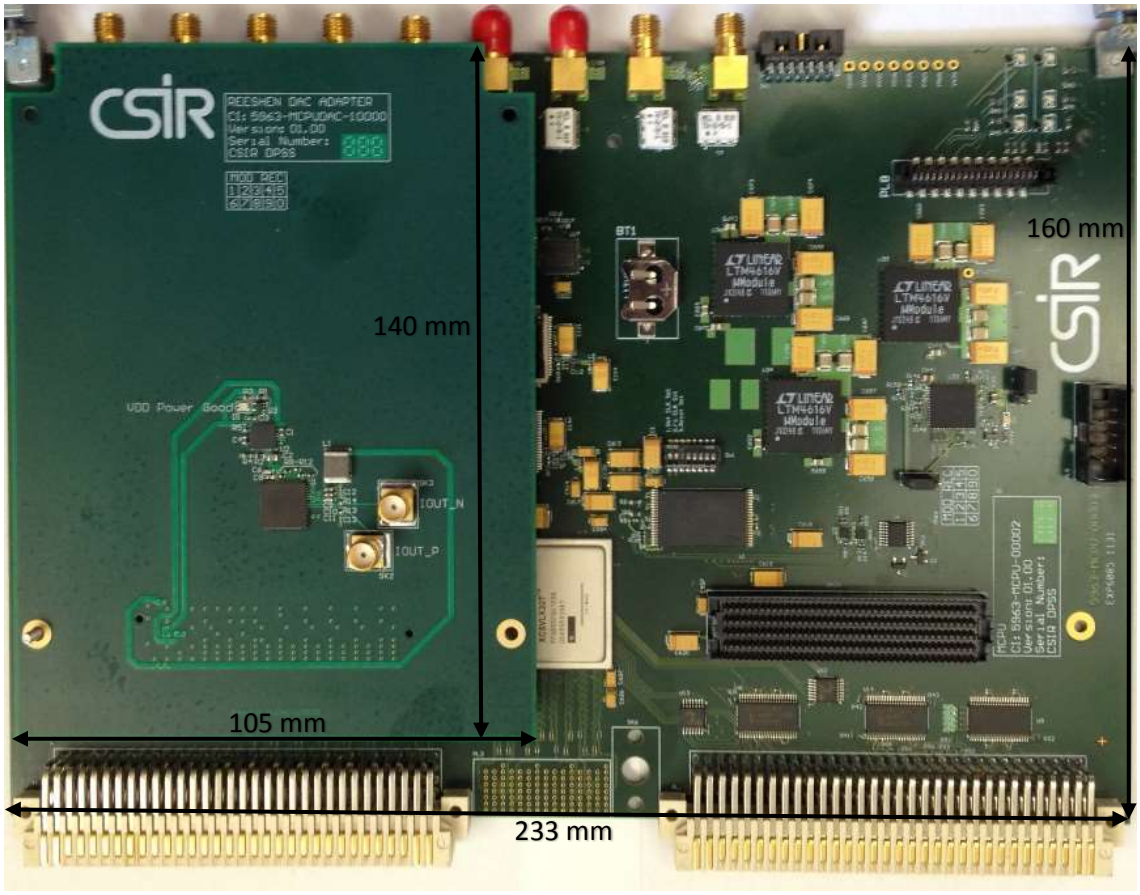


Fig. 8: Processor motherboard with FMC mezzanine card mounted.

A Tektronix DSA 71254 digital phosphor oscilloscope and Agilent E4447A PSA Spectrum Analyser were used to perform the time and frequency domain measurements respectively. The measured DNL and INL are shown in Fig. 9 and Fig. 10 respectively.

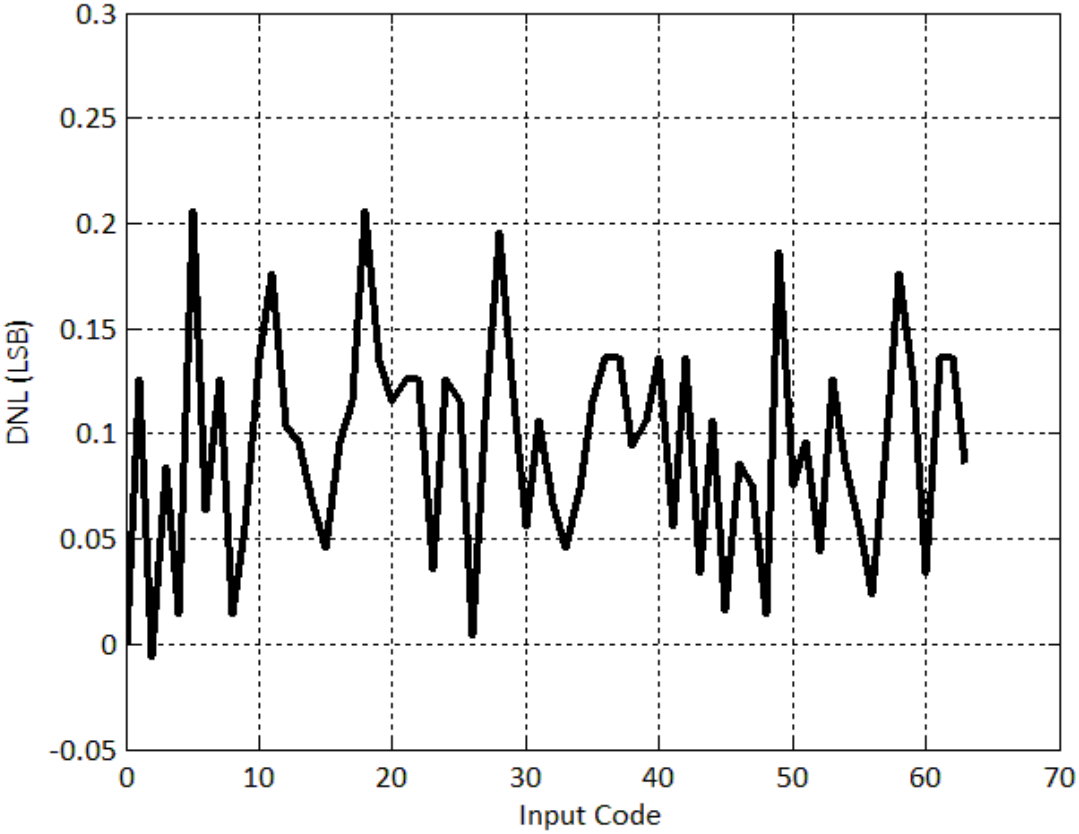


Fig. 9: DNL of the DAC measured using Tektronix oscilloscope.

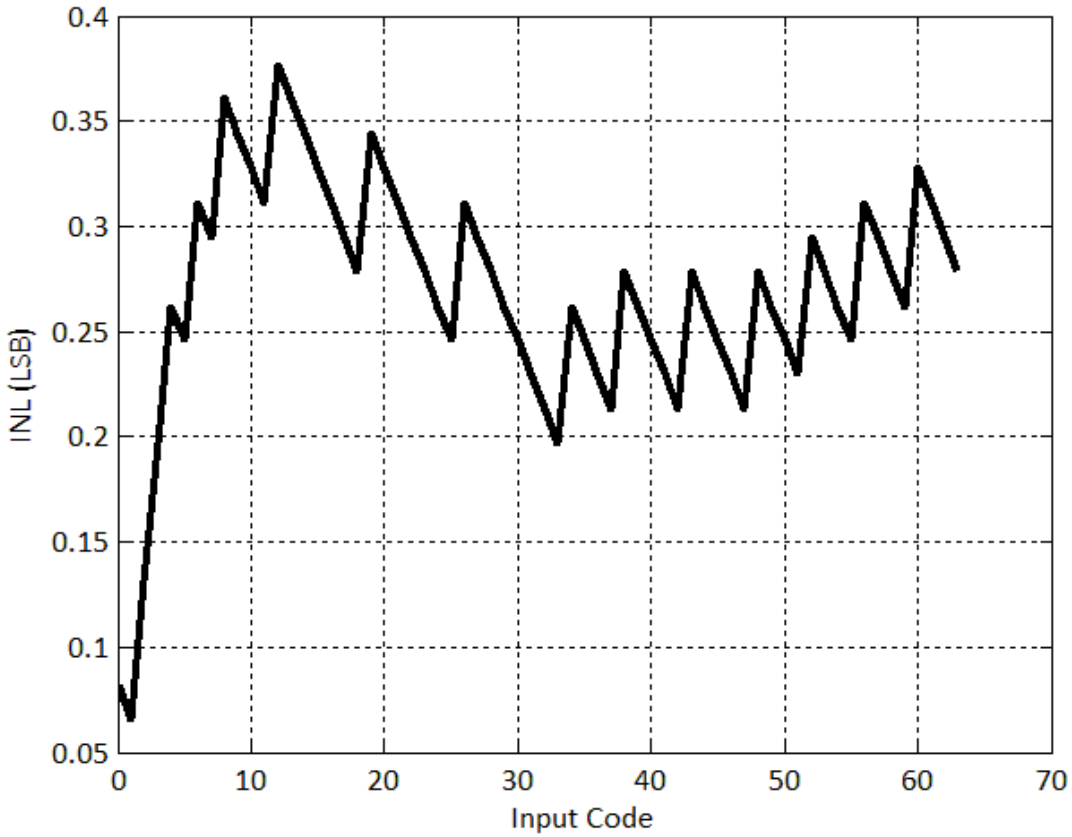


Fig. 10: INL of the DAC measured using Tektronix oscilloscope.

The DAC is monotonic, as the INL and DNL measurements satisfy the constraints for monotonicity and matching goals. The definition of SFDR used here is the ratio of the amplitude of the DAC output averaged spectral component at the input frequency to the amplitude of the largest unwanted spectral component observed over a specified frequency band [18]. The simulated and measured SFDR as a function of input frequency is shown in Fig. 11.

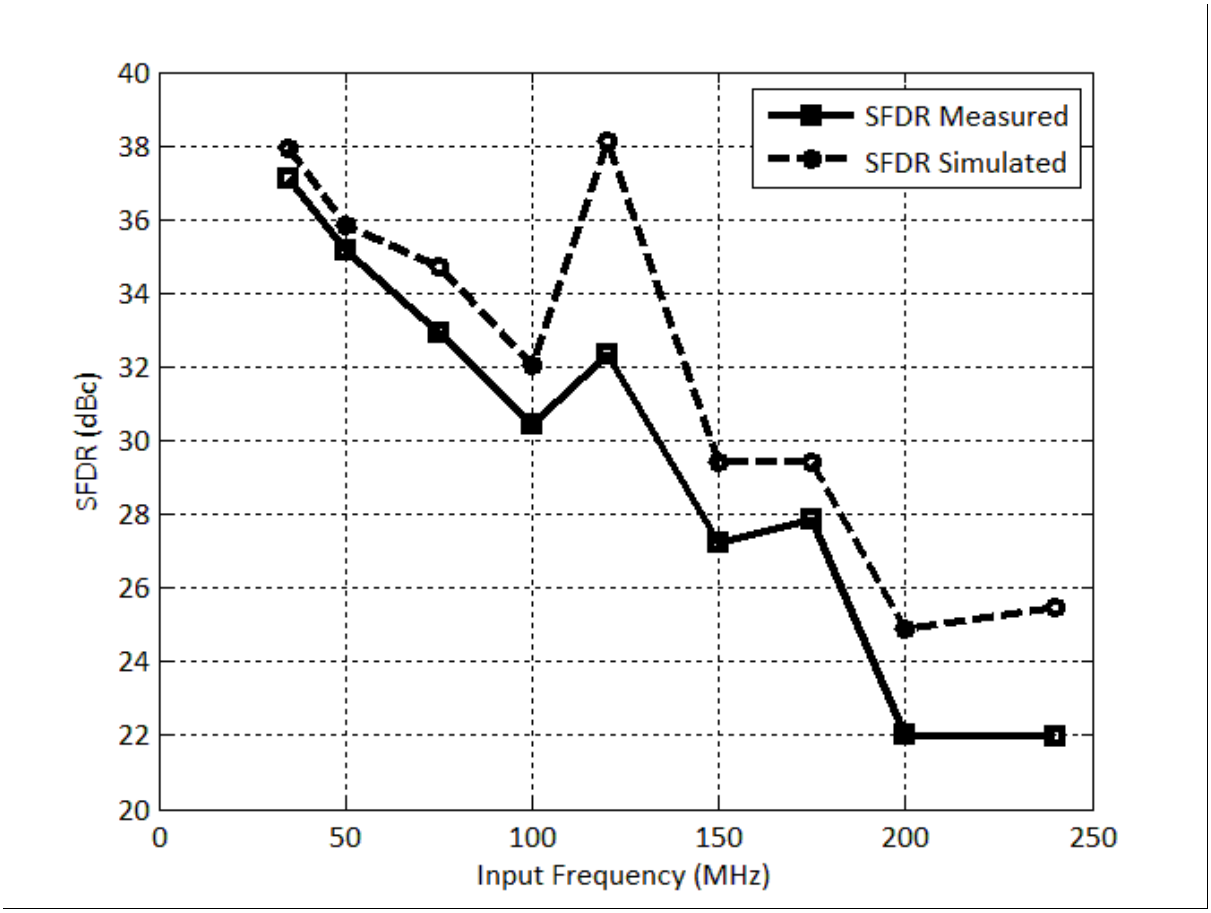


Fig. 11: Simulated and measured SFDR of the DAC measured using an Agilent spectrum analyser.

As expected, the SFDR worsens as the input frequency increases and is at a worst case of 21.96 dBc at 240 MHz. The measured results follow the trend of the simulated results generally but are 2 to 3 dB worse in all measurements. This may be attributed to the chip packaging, bonding wire and PCB trace mismatch effects. In addition, at higher frequencies the limits of the LVDS transceivers are also reached. The power consumption and area of the DAC core of this work are very low at under 4 mW and 0.1 mm^2 respectively. The specifications of the fabricated DAC are documented in Table 2.

TABLE 2.

DAC specifications.

Specification	**Value**
Technology	IBM 8HP
Process	130 nm SiGe BiCMOS
Total Area	4 mm^2
Active Area	0.1 mm^2
Sampling Frequency	500 MS/s
Power Dissipation (Core)	3.97 mW
Resolution	6 bits
INL	0.38 LSB
DNL	0.21 LSB
SFDR (worst case)	21.96 dBc

In order to compare to different DAC designs, the figures of merit (FOM) in [10] are used. The first FOM is:

$$\boldsymbol{FOM_1 = \frac{Power}{2^N . Sample\ Rate}} \tag{13}$$

The FOM_1 is often used as it is simple and the information required is often published. However, FOM_1 does not account for SFDR performance and hence a FOM that accounts for resolution, power and frequency domain performance is additionally used:

$$\boldsymbol{FOM_2 = \frac{2^N \cdot f_{sig}|@SFDR = 6(N-1)}{POWER}} \tag{14}$$

The FOM_2 is more appropriate for this work and high speed DACs. It accounts for the linearity of the device over the Nyquist frequency. The parameter f_{sig} is the input signal frequency where the SFDR has dropped 1 bit or 6 dB in comparison with the quantization

limited dynamic range. The figures of merit for this work and other works are tabulated in Table 3.

TABLE 3.

Comparison with other DACs published.

	This work	**[10]**	**[12]**	**[20]**	**[21]**	**[22]**
Technology	130 nm BiCMOS	130 nm CMOS	0.35 µm CMOS	0.25 µm BiCMOS	0.18 µm BiCMOS	0.25 µm BiCMOS
Sampling	500 MS/s	3 GS/s	1 GS/S	30 GS/s	10 GS/s	13.4 GS/s
Core Area	0.1 mm^2	0.2 mm^2	-	1.8 mm^2	1.5 mm^2	0.9 mm^2
Resolution	6 bit	6 bit	10 bit	4 bit	5 bit	6 bit
Power Dissipation	3.97 mW	29 mW	110 mW	455 mW	10.2 mW	1050 mW
Frequency (SFDR = 6N-1)	170 MHz	1.5 GHz	-	-	-	6 GHz
FOM_1	0.125 pJ	0.15 pJ	0.11 pJ	0.95 pJ	0.031 pJ	1.22 pJ
FOM_2	2.72 GHz/ mW	3.3 GHz/ mW	4.7 GHz/ mW	-	-	0.36 GHz/ mW

This work compares favourably in FOM_1 due the extremely low power dissipation. Many designs that make use of SiGe technology achieve the frequency performance by using large external power supply voltages at the DAC output at the expense of power.

In the FOM_2, this work is not the best but does achieve good results. This can be attributed to a lower sampling rate when compared to other works which can be achieved with LVDS receivers with deserialization. This type of technology is commercially available but was not available for this scholarly work. Regardless, the sampling rates were still adequate for the purposes of this work.

The power and area of the DAC presented in this work is the lowest of any in the comparison, partially due to the process technology but also due to the compact layout, smaller transistor sizes and binary weighted architecture. The low power and area are particularly suitable for system on chips requiring a DAC. The DAC in this work is able to achieve the SFDR performance of better than an effective number of bits of 5 bits up to around 130 MHz. The SFDR performance degrades for input frequencies above 170 MHz.

5. Conclusion

A BiCMOS six-bit binary weighted DAC was designed and implemented using the *IBM 8HP* SiGe 130 nm technology node and was shown to have an SFDR of 21.96 dBc at the Nyquist input frequency and a sampling rate of 500 MS/s.

BiCMOS technology is shown to have advantages over conventional CMOS technology in the design of high-speed DACs by reducing the clock feedthrough effect in the current switches which was achieved using a novel current source cell implementation that comprises HBT current switches, NMOS cascode and NMOS current source. However in a number of design areas such as the current source cell, the voltage headroom available in modern fabrication processes favours the use of NMOS devices as opposed to HBT transistors.

The use of BiCMOS technology in high-speed DAC design theoretically offers higher performance over CMOS technology but in practice, system considerations such as area and voltage headroom limit its use to specific areas in the DAC architecture.

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