HIGH VOLTAGE BOOST DC-DC CONVERTER SUITABLE FOR VARIABLE VOLTAGE SOURCES AND HIGH POWER PHOTOVOLTAIC APPLICATION.

by

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SUMMARY

HIGH VOLTAGE BOOST DC-DC CONVERTER SUITABLE FOR VARIABLE VOLTAGE SOURCES AND HIGH POWER PHOTOVOLTAIC APPLICATION.

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Keywords: Tapped-coupled-inductor, interleaving, high step-up DC-DC converter, coupling coefficient, photo-voltaic, digital control, voltage regulation

Important considerations of a photovoltaic (PV) source are achieving a high voltage and drawing currents with very little ripple component from it. Furthermore, the output from such a source is variable depending on irradiation and temperature. In this research, literature review of prior methods employed to boost the output voltage of a PV source is examined and their limitations identified. This research then proposes a multi-phase tapped-coupled inductor boost DC-DC converter that can achieve high voltage boost ratios, without adversely compromising performance, to be used as an interface to a PV source. The proposed converter achieves minimal current and voltage ripple both at the input and output. The suitability of the proposed converter topology for variable input voltage and variable power operation is demonstrated in this dissertation. The proposed converter is also shown to have good performance at high power levels, making it very suitable for high power applications.

Detailed analysis of the proposed converter is done. Advantages of the proposed converter are explained analytically and confirmed through simulations and experimentally. Regulation of the converter output voltage is also explained and implemented using a digital controller. The simulation and experimental results confirm that the proposed

converter is suitable for high power as well as variable power, variable voltage applications where high voltage boost ratios are required.

OPSOMMING

HOOGSPANNING-AANJAER GS-GS OMSETTER GESKIK VIR VERANDERLIKE SPANNINGSBRONNE EN HOË-KRAG-FOTOVOLTAÏESE TOEPASSINGS.

deur

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Sleutelwoorde: Tapgekoppelde induktor, tussenlaag, hoë spanningsverhoging- GS-GS-omsetter, koppel-koëffisiënt, foto-voltaïese, digitale beheer, spanning regulering,

Die belangrikste oorwegings vir 'n fotovoltaïese (FV) bron is die bereiking van hoë spanning en die lewering van stroom met 'n baie klein rimpeling-komponent. Die uitset van so 'n bron is 'n veranderlike wat afhang van bestraling en temperatuur. In hierdie navorsing word literatuur oor metodes wat vantevore gebruik is om die uitsetspanning van 'n FV-bron te versterk, ondersoek en die beperkings geïdentifiseer. Hierdie navorsing stel dan 'n multi-fase tapgekoppelde induktor aanjaer GS-GS omsetter voor wat hoë spanning versterker verhoudings kan bereik, sonder om prestasie nadelig te raak, om gebruik te word as 'n koppelvlak na 'n FV-bron. Die voorgestelde omsetter handhaaf minimale stroom en spanning-rimpeling by sowel die inset as die uitset. Die geskiktheid van die voorgestelde omsetter topologie vir veranderlike inset-spanning en veranderlike krag-werking word in hierdie verhandeling gedemonstreer. Die voorgestelde omsetter het getoon dat dit baie geskik is vir hoë krag-toepassings.

Gedetailleerde analise van die voorgestelde omsetter is gedoen. Die voordele word analities verduidelik en deur middel van simulasies asook eksperimenteel bevestig. Regulering van die uitsetspanning word verduidelik en geïmplementeer met behulp van 'n digitale kontroleerder. Die simulasie en eksperimentele resultate bevestig dat hierdie

omsetter uiters geskik is sowel hoë as veranderlike krag, en veranderlike spanning toepassings waar hoë-spanningversterker verhoudings vereis word.

LIST OF ABBREVIATIONS

PV	Photovoltaic
MPP	Maximum Power Point
AC	Alternating current
DC	Direct current
RMS	Root mean squared
EMI	Electromagnetic interference
DSP	Digital signal processor
PWM	Pulse width modulation
RCD	Resistor-capacitor-diode
MOSFET	Metal oxide semiconductor field effect transistor

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CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Background and context

Renewable energy has been thrust to the spotlight due to the rising oil prices, concern of environmental pollution around the world such as the greenhouse gas effect, acid rain and the eminent exhaustion of fossil-fuel reserves. Renewable energy sources such as solar, wind, tidal have become one of the most important renewable energy sources since they are clean, pollution free, and inexhaustible [1]

Solar cells convert sunlight directly into electricity through the photovoltaic effect of semiconductors. Solar photovoltaic (PV) can be used in a wide range of applications including power supplies for satellite communications or large solar power stations feeding electricity into the grid. A solar array consists of solar panels connected in series and/or shunt configurations. A solar panel consists of solar cells, also connected in series and/or parallel configurations.

The most important considerations on PV energy generators are to obtain a high voltage gain and sourcing of minimal reactive power by drawing currents with very little ripple component. Most currently available PV modules have low open-circuit and maximum power point (MPP) voltages [2]. Efficient power conversion is not achieved with a low voltage source. Some stand-alone applications operate at high power levels which require many PV modules to be connected in series to provide a high voltage. The utility grid voltage is also high including 220 or 110 V_{AC}, hence a PV generator needs to produce a high DC voltage in case of PV solar-grid integration. A PV array output voltage and current also varies a lot depending on solar radiation and temperature.

Today's PV system cost mainly depends on the cost of the panels. One priority is to reduce the installation overhead by reducing the number of panels in series, while still maintaining a high power output by having parallel panel connections. Connection of large number of PV panels in series also lead to limitations like mismatch errors which cause low conversion efficiencies.

Mismatch errors are caused by circumstances in PV arrays such as load mismatching, mismatching of PV modules, shadows and obscurances [3].

DC-DC converters are being integrated to the PV sources to improve the conversion efficiencies. It is also possible to integrate a DC-DC converter with a maximum power point tracking (MPPT) algorithm that makes a PV array deliver its maximum available power. The buck, boost and buck-boost converters are commonly used with the MPPT [4].

Other than providing the MPPT, a boost DC-DC converter can be used to provide a high voltage amplification of the PV array output. PV panels also have very low current dynamics. It is hence always important to keep the current ripple very low. By controlling the DC-DC converter, a regulated converter output can be obtained despite the frequent fluctuations in the PV array output. Theoretically, conventional boost converters are able to achieve high step-up voltage gain at a high duty ratio. The voltage gain is however limited in practice due to losses in the inductor, filter capacitor, active switch and the output diode. With an high duty ratio, the output diode conducts for only a short time during each switching cycle, thus resulting in serious reverse-recovery problems and increase in the rating of devices[10]-[12].

1.1.2 Research gap

The problem addressed in this research lies in finding a way of efficiently stepping up the small intermittent output voltage of a PV array by at least ten times to a constant high voltage DC bus. Current from the PV array should also be drawn with minimal ripple. The

high output DC voltage can then be used for high power applications or integrated to the utility grid.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

The research questions to be addressed in this thesis include:

1. How can the output voltage of a small PV array be boosted to high values using a DC-DC converter without extreme duty ratios?
2. How can the input and output current and voltage ripple be reduced, hence a lower reactive power demand and an increase in the efficiency of a PV system?
3. Is it possible to obtain a converter topology suitable for variable input voltage and power operation to be used in an application such as solar PV?
4. What are the effects of the coupling coefficient on a boost converter with a tapped-coupled inductor?
5. How can a converter with an advantage of low output current ripple suitable for charging a battery from a PV source be obtained?

The main objectives of the research are to develop a novel DC-DC converter that is capable of ensuring:

1. A high voltage boost ratio of a PV source output or a similar type of source such as wind, for a high voltage and power application or integration to the grid. The high boost ratios should be achieved without adversely compromising performance.
2. Minimal ripple in the input and output of the converter, hence an improvement of performance and efficiency. This will make the converter suitable for interface with a PV source where it is important to draw currents with very little ripple component.
3. Suitability for variable power and voltage operation.
4. A regulated output is obtained from the PV source at all times despite the changing environmental conditions.

1.3 HYPOTHESIS AND APPROACH

The hypothesis as stated as;

A multi-phase interleaved tapped-coupled-inductor boost converter would:

I. Be capable of achieving a high voltage boost ratio of a PV source without adversely compromising performance.
II. Result to minimal ripple in the input and output of the converter which will hence lead to an improvement of performance and efficiency.
III. Be suitable for variable power and voltage operation.
IV. Be capable of ensuring that a regulated output is obtained from the PV source at all times despite the changing environmental conditions.

The approach to be used is given as follows;

I. Literature review; a study of the existing PV array output boosting methods will be done. This will aid in choosing a suitable topology for a PV application that ensures a high voltage boost ratio, minimal ripple and a high efficiency. A suitable power-electronics converter that has better performance characteristics is selected to be connected to the PV array output.
II. Analysis and modelling of the selected boost converter is done which verifies the hypothesis and helps in the design.
III. Design; The converter components will be designed and selected for optimal performance.
IV. Control of the proposed converter is then done to regulate the output of the converter.
V. Simulations of the proposed converter are done using PSIM software. With the simulations, the proposed converter's current and voltage waveforms are obtained which further verify the hypothesis.
VI. Practical implementation; the designed converter will be implemented in hardware to validate simulation and analytical results.

1.4 RESEARCH GOALS

a) To formulate a new, efficient and low cost method of boosting the output voltage of a small PV array or a similar type of source.
b) To design a simple, novel, highly efficient boost DC-DC converter that can be used as a sub-system in the integration of a renewable energy source to the grid or for high power applications.
c) To design a converter that has minimal output current ripple hence suitable for an application such as battery charging.
d) To design a DC-DC converter that is suitable for variable input voltage and power operation to be used in an application such as solar PV.

1.5 RESEARCH CONTRIBUTION

Output voltage of a solar array is low and it needs to be boosted to feed high power applications or integration to the grid. This however has to be done with high efficiency, while still ensuring maximum power is extracted from the PV array. Many techniques that try to boost the output voltage of a PV source have been identified, but these present limitations due to low efficiencies, complexity and cost. By use of the proposed DC-DC converter, high boost ratios can be attained at high efficiency and a low cost of the entire PV system. The proposed converter is also suitable for high and variable power applications.

1.6 OVERVIEW OF STUDY

This chapter introduces the background and context of the research problem. It identifies the research gap, briefly explains the research objectives, questions, and hypothesis and briefly describes the research approach.

In Chapter 2, the existing PV array voltage boost topologies are discussed and their advantages and limitations examined. Maximum power point tracking and PV array characteristics are also covered. A single-phase tapped-coupled inductor boost converter's operation is discussed and a detailed characterisation presented in Chapter 3. In Chapter 4,

the proposed interleaved tapped-coupled inductor boost converter is discussed. A two-phase interleaved tapped-coupled-inductor boost converter is analysed and modelled.

In Chapter 5, sizing of components constituting the proposed converter is done. The proposed converter circuit design is also discussed in this chapter. Control of the proposed converter is discussed in Chapter 6, where the design of a digital feedback control loop is explained. This control ensures that the output voltage is regulated despite the any input voltage and load variations.

In Chapter 7, the proposed multi-phase interleaved tapped-coupled-inductor boost converter up to six-phases is simulated. Comparison of the different multi-phase converters is done and discussed to show how converter performance is affected by the number of phases used. In Chapter 8 practical results from the built single-phase and two-phase tapped-coupled-inductor boost converters are presented and discussed. These are compared with the simulation results. Chapter 9 concludes and makes recommendations for further research.

CHAPTER 2 LITERATURE STUDY

2.1 CHAPTER OBJECTIVE

This chapter covers the literature survey. It examines the existing techniques that have been used in stepping up of a PV output voltage, minimising ripple in the current drawn from the PV and the different methods which have been used to ensure MPPT. A brief discussion of the proposed converter is also included at the end of this chapter.

2.2 BOOSTING THE VOLTAGE OF THE PV ARRAY

PV cells produce direct current (DC) power at only a fraction of a volt. Alternating current (AC) power with voltage greater than 100 V is used by the utility grid and most of the equipment in homes. To connect PV systems to the grid, an inverter is required to convert power from DC to AC. The input DC voltage to the inverter must be large, about 300V to 400V, for an efficient conversion to the AC-line voltage.

Some stand-alone applications also require high DC voltages which cannot be obtained directly from small PV arrays. To achieve these high voltages from the PV array, high voltage amplification is necessary. A number of ways to amplify the output of a PV system have been studied and are discussed below:

2.2.1 The photovoltaic series string

PV panels have previously been placed in series to obtain high output voltage, maintaining lower currents and higher efficiencies [7]. However, the long strings of panels have a lot of complications especially when the string is operating under non-uniform conditions of radiation.

Series connected PV panels are never exactly identical, though they are constrained to all conduct the same current. In case of shading of some of the panels, thus unequal radiation, then the following may occur:

I. The shaded cells or panels will try to drive the once not shaded into operating at a lower current level. As a result, the least efficient panel sets the string current. The system output power is limited by the current produced by the cell or panel generating the lowest output current. This means that the total efficiency of the array is limited to the efficiency of this cell.

   Also, the PV panels in a string must be of the same size and orientation [7].

II. The cells or panels which are not shaded try to drive the shaded ones into operating at a higher current level. Current through a PV cell is directly proportional to irradiance, and the only way the cell can operate at a higher current than its short circuit current is by becoming reverse biased. The cell moves into the negative voltage region of the cell's I-V curve. This causes a phenomenon known has hot-spot heating, as power generated by the unshaded cells is dissipated in the shaded cells, leading to possible cell damage [5]. During this time, however, the panel's backplane diode(s) become forward biased, limiting the reverse bias and the power dissipation in the shaded cell. The disadvantage of this is that now the shaded cells are bypassed, thus they have a zero power contribution to the PV array and a lower string voltage.

2.2.2 PV array- inverter connection

The use of a single stage inverter is also another method that has been used as an interface to the PV arrays. A single stage inverter feeding the utility grid from a PV array has the following functions:

a) To invert the PV current in to an AC current.
b) If the PV array voltage is lower than the grid voltage, the PV array voltage has to be boosted by an extra element such as a line frequency step-up transformer.

Protection and filtering components have to be included in such a system which increases complexity and cost [7]. Inclusion of a transformer also has a disadvantage of large size and weight and low efficiency [2].

2.2.3 Conventional boost DC-DC converter interface of PV array

Due to the varying voltage levels of a PV array, a dc-dc converter can be connected to the array output for voltage regulation as well as boosting. The boost converter should have a high step-up voltage gain and a high efficiency. A conventional boost converter is shown in Figure 2.1.

Theoretically, conventional boost converters are able to achieve high step-up voltage gain in heavy duty load conditions. The voltage gain is however limited in practice due to losses

in the inductor, filter capacitor, active switch and the output diode. Due to these losses, the high voltage gain in a conventional boost converter can only be achieved with an extreme duty ratio. With an high duty ratio, the output diode conducts for only a short time during each switching cycle, thus resulting in serious reverse-recovery problems and increase in the rating of devices[10]-[12]. Under this condition, the EMI (electromagnetic interference) is severe. As a result of this, the conversion efficiency is degraded.

Furthermore a conventional boost converter has a low input voltage, hence large input currents result. High current and voltage rated switches, which have high parasitic resistance, are hence required. The draw backs of this include increased conduction loss, cost and size [6], [37]. Furthermore, this converter is not suitable for charging a battery from a PV source due to the discontinuous nature of its output current.

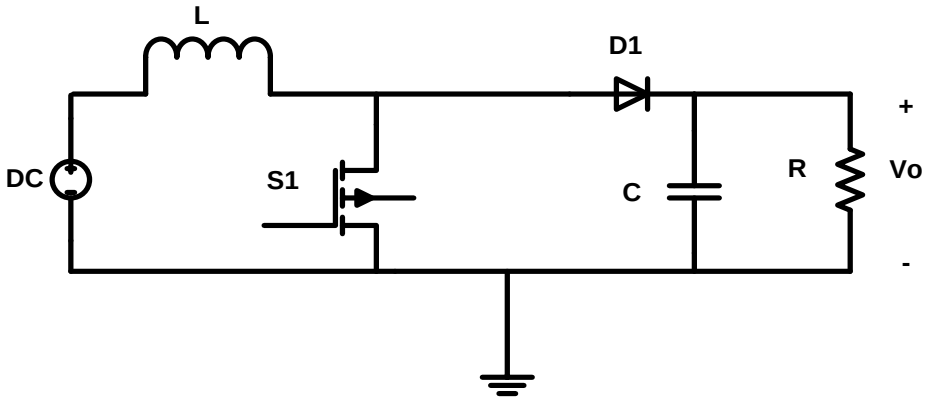


Figure 2.1. Conventional boost converter.

2.2.4 Cascaded converters

Another way of increasing the voltage gain of a PV array output would be cascading DC-DC boost converters [7] as shown in Figure 2.2. As proposed in [7], every panel has its own DC-DC converter, and the panels with their associated converters are still placed in series to form a string. It was however concluded in [7] that the configuration is not capable of always delivering the full amount of output power from a mixture of shaded panels and those delivering full power. This is because if a PV panel is shaded, its current

falls and the current in the entire string must fall to the value of the lowest converter module input current. Another limitation of the cascaded converters is the complexity due to the higher number of switches and the magnetic components and the controllers which must be synchronized. Another concern of the cascaded converters is their stability. The output diode of the last boost stage converter has a severe reverse recovery problem due to the high levels of both output power and output voltage. This degrades efficiency and causes EMI noise [6].

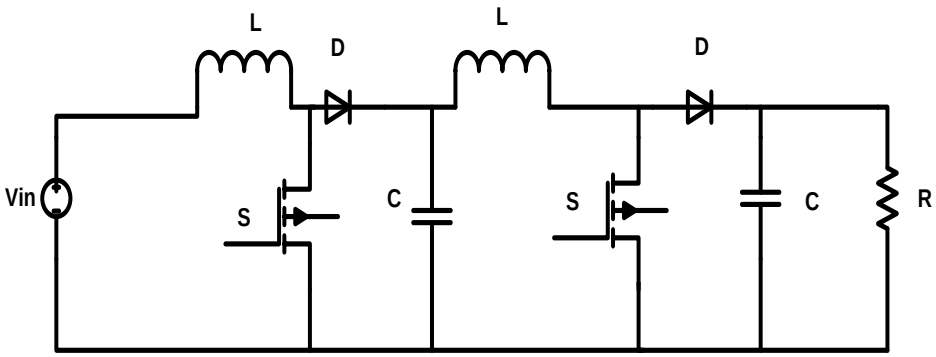


Figure 2.2. Cascade boost converter.

2.2.5 A DC-DC flyback converter

A DC-DC flyback converter in Figure 2.3 can be used to provide a high voltage boost. It has a transformer, used for voltage isolation as well as for better matching between the input and the output voltage and current requirements. Although the flyback converter has an advantage of a very simple structure, it suffers a high switch voltage stress due to the leakage inductance of the transformer. A snubber circuit is required to dissipate or recycle the energy stored in the leakage inductance of the primary winding when the switch is turned off. A flyback converter also does not offer a mechanism of ripple reduction in the input current [38].

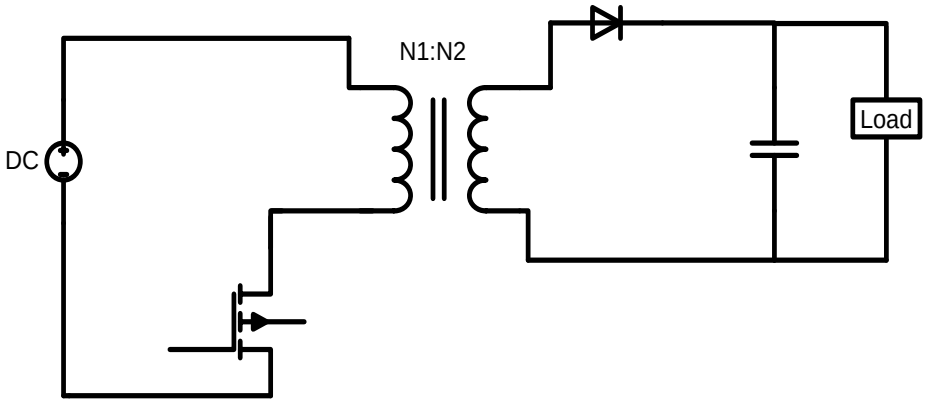


Figure 2.3. Flyback converter

2.2.6 Step-up converters with coupled inductors

Coupled inductors, without tapping, can serve as a transformer to extend the voltage gain in DC-DC converters [2], [6], [9]-[11]. Voltage stress of the switch is reduced and the peak current of the power devices is minimized. This improves the circuit performance in high step-up DC-DC converters. Two coupled inductors include two windings wound on the same core. Coupled-inductor techniques involve simultaneous parallel energy transfer both electrically and magnetically.

The current specifications for a coupled inductor differ depending on whether its windings are physically connected in series or in parallel. When the windings are connected in series as in Figure 2.4, the equivalent inductance is more than L_1+L_2 due to the mutual inductance.

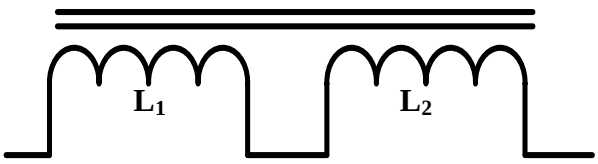


Figure 2.4. Two coupled inductors connected in series.

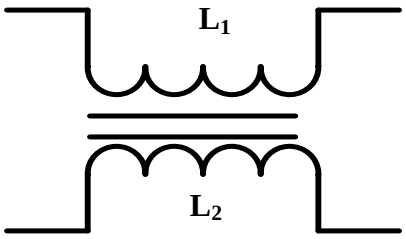


Figure 2.5. Two coupled inductors connected in parallel.

The mutual inductance, *M* of the two coils is related to the two coupled inductance and the coupling coefficient.

$$M = k\sqrt{L_1 L_2} \tag{2.1}$$

The coupling coefficient represents the flux linkage between the two windings. Coupling coefficient has values of $0 < k < 1$ and is dependent on the portion of the total flux lines that cuts both the first and second coil. For a coupling coefficient of 1, then all the flux generated by the second winding cut the first winding and maximum energy would be transferred across the windings. The extreme duty cycle is avoided by the proper design of the turns ratio of the coupled inductor.

The leakage inductance of the coupled inductor can also be employed to control the diode turn-off current falling rate and hence alleviating the diode reverse-recovery problem [6], [9]. However, the leakage energy results in high voltage ripple across the switch due to a resonance phenomenon induced by the leakage currents and severe EMI problems which degrades efficiency [11]. This in turn requires the converter to employ a high voltage switch to sustain variations in order to protect the switch or a snubber circuit to deplete the leakage energy. A resistor-capacitor-diode (RCD) clamp circuit can reduce the voltage stress but at the cost of high power losses. In [6], a high step-up DC-DC utilising coupled inductors is described. The leakage energy in this converter is recycled by the use of a diode and a capacitor. A step-up converter with coupled-inductor described in [11] a passive regenerative snubber circuit is adopted to promote the voltage gain.

Another method of reducing the switch voltage stress due to the leakage inductance is by use of an active-clamp circuit [2], [8], [9], [10], and [39]. An active-clamp circuit recycles the leakage energy with minimal voltage stress across the switch, leading to a higher output voltage. However, limitations of the active-clamp circuit include topology complexity, increased cost and losses due to the clamp circuit. An overlap between the main and active-clamp switch gate-drive signals could lead to a failure of the circuit [6].

2.2.7 Interleaved boost converters

Multi-phase boost converters with interleaved switching have received considerable interest in PV applications [2], [12]-[14]. In interleaved converters, boost converters are paralleled to improve energy efficiency by reducing the amount of reactive power drawn from the source. The interleaved boost converters have the same duty ratio but with a $2\pi/N$ phase shift, where N is the number of phases. Compared to conventional boost converters, the interleaved converters have the following advantages:

a) Lower input- current ripple due to current sharing.
b) Lower output-voltage ripple.
c) A lower value of ripple amplitude and a high ripple frequency in the resulting input and output waveforms.
d) Enhanced transient performance as a result of smaller filter components.
e) More compact in size due to smaller filter components and heat-sink.
f) Improved reliability due to structural redundancy.
g) Reduced electromagnetic interference because of low ripple amplitude of the input current.

Interleaved converters however have limitations that include:

a) They have a more complex control since the active switches are controlled by complementary signals.
b) A higher number of components are required.
c) A higher number of switches and gate drive circuits are required.

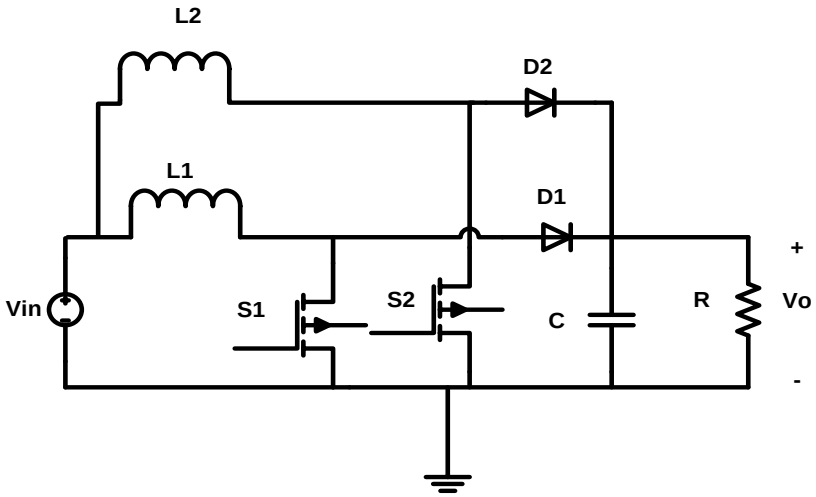


Figure 2.6. Two-phase interleaved boost converters

Although there is an increase in the number of components in the interleaved converter, the actual increase of cost may not be significant compared to the un-interleaved converter [40]. This is because of the current sharing in the inductors and the switching devices, leading to lower rated components in the interleaved converter.

A combination of interleaved and coupled inductors has been shown to produce high performance in the boost converters [2], [12]-[17], [40]. The coupling, which is a form of an integrated magnetic component, reduces the core number. This overcomes the shortcoming of interleaving, which increases the number of inductors compared to a conventional converter. The benefits of strongly coupled inductors in interleaved boost converters is presented in [15], where it is demonstrated that the topology has superior current sharing characteristics even in the presence of relatively large duty cycle mismatch and small input current ripple.

In [14], a two-cell interleaved boost converter with coupled inductors is used to match the photovoltaic system to the load and operate the solar cell array at a maximum point.

A ZVT interleaved boost converter, with a winding-coupled inductor structure is proposed in [12]. This converter offers a method to extend the voltage gain using the turns ratio

selection. The turn-off voltage of the main switch is clamped and leakage energy recycled by use of an active-clamp circuit. This ensured that the voltage spikes across the switch are suppressed and leakage energy recovered.

Analytical models describing the steady-state operation of multi-phase boost converters with interleaved switching for PV applications are derived in [18]. The analyzed topology in [18] included the non-ideal characteristics and a switching scheme based on ripple correlation control is deployed to maximise the power output of the photovoltaic source.

2.2.8 Tapped-coupled boost converter

Tapped inductors have been investigated to provide high step-up and step-down ratios with good efficiency with no requirement for isolation [24]-[34]. The two windings N_1 and N_2 of the tapped inductor are on the same core and therefore magnetically coupled as shown in Figure 2.7. A large step-up conversion can be achieved by selecting the turn-ratio of the tapped-inductor windings. Tapping the inductor has the benefits that the duty cycle of the converter can be optimized so as to achieve maximum efficiency. Tapping of the inductor also allows a different mix of voltage and current ratings for various components in the converter [24].

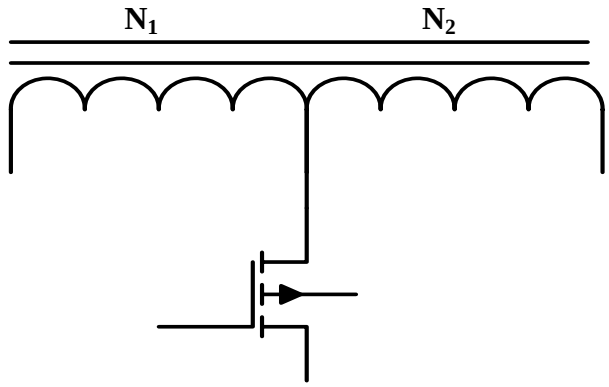


Figure 2.7. Tapped-coupled inductors.

In [24] and [25], a matrix of tapped inductor configurations is discussed which includes:

a) Switch-to-tap, where the switch is connected to the tapping point of the inductor, rather than to one of the extremity of the inductor.

b) Diode-to-tap, where the diode is connected to the tapping point of the inductor, rather than to one of the extremity of the inductor.
c) Rail-to-tap, where the tap is connected to one of the power rails.

High-step-down converters using the tapped inductor have been investigated in [26] and [27]. Recent studies have also shown the tapped inductor application in high-step-up converters [28], [30] and [34]. In [28], it is shown that the boost converter with the tapped inductor has a higher transfer ratio than the classical boost converter for the same duty ratio. The converter in [28] also has lower voltage stress across the buffer capacitor, but a higher current stress on the input shunt capacitor. In [30], a tapped-inductor boost converter for high boost application is described and analysed, where it was also concluded that the converter is a good option for solving high boost requirements.

Application of tapped inductor converter on PV systems has been discussed in [31], [32] and [34]. In [31], a buck-boost converter with tapped inductor is studied, aiming at selecting the converter appropriate for an integrated PV inverter applied for residential use with connection to a single-phase grid. In this study, it was verified that the gain of the buck-boost with tapped-Inductor was higher than obtained with the classical buck-boost converter. It was also concluded in [31] that the application of the buck-boost with tapped inductor without ground is feasible in a small single-phase inverter within photovoltaic systems interconnected to the grid.

Study in [31] was extended in [32], where a tapped inductor buck-boost converter with a non-grounded output is discussed. In [32], it is concluded that connection of the PV to the grid for residential use could be done using a tapped inductor buck-boost converter operating in three modes: Continuous conduction mode, critical mode and the discontinuous mode.

A possibility of using tapped-inductor boost converter as a module integrated converter for PV sources has been discussed in [34].

A tapped-inductor boost converter with zero current switching (ZVS) is proposed. It is concluded that the proposed boost converter can allow voltage step-up of ten times its

input without an extreme duty ratio. Switching losses were also reduced and an increased efficiency achieved [34].

2.2.9 Other proposed boost converters in the literature.

Other high step-up converters include those utilising the switched-inductor technique [38], whereby two inductors with same level of inductance are charged in parallel during switch-on period and are discharged in series during switch-off period.

A basic cell with winding-cross-coupled inductors (WCCIs) and interleaved structure is proposed in [41]. A family of DC-DC converters is deduced from this basic cell which is suitable for high step-up conversions.

The wide-input-wide-output (WIWO) DC-DC converter [42] is formed by the integration of buck and boost converters via a tapped inductor. The WIWO converter achieves both high buck and boost features by application of proper control to the two active switches. The capacitor-diode voltage multiplier converter [43] has been proposed and can be used to drive voltage amplifiers. These types of converters however, are all complex and have a higher cost.

2.3 SOLAR RESOURCE

2.3.1 Solar array characteristics

A PV array has non-linear voltage-current characteristics as shown in Figure 2.8. Its output depends on the load voltage and weather conditions, which are unpredictable. The characteristics are divided into two sections: (i) constant voltage section and (ii) constant-current section [15]. The current from the array is proportional to the radiation level and completely independent from temperature, while the voltage is completely independent from the radiation level and has negative coefficient with the temperature. Thus, an increase in solar irradiation and a decrease in array temperature results in an increase in maximum power output of the array. Due to the intermittent nature of the PV array, it is necessary to employ an efficient power electronic interface, with a maximum power point tracker (MPPT), between the array and the loads or the AC grid. The maximum power

point (MPP) region in Figure 2.8 shows a unique operating point where the array delivers maximum power. An MPPT ensures that the PV array operates at this maximum power point. This would ensure maximum utilisation of the PV source.

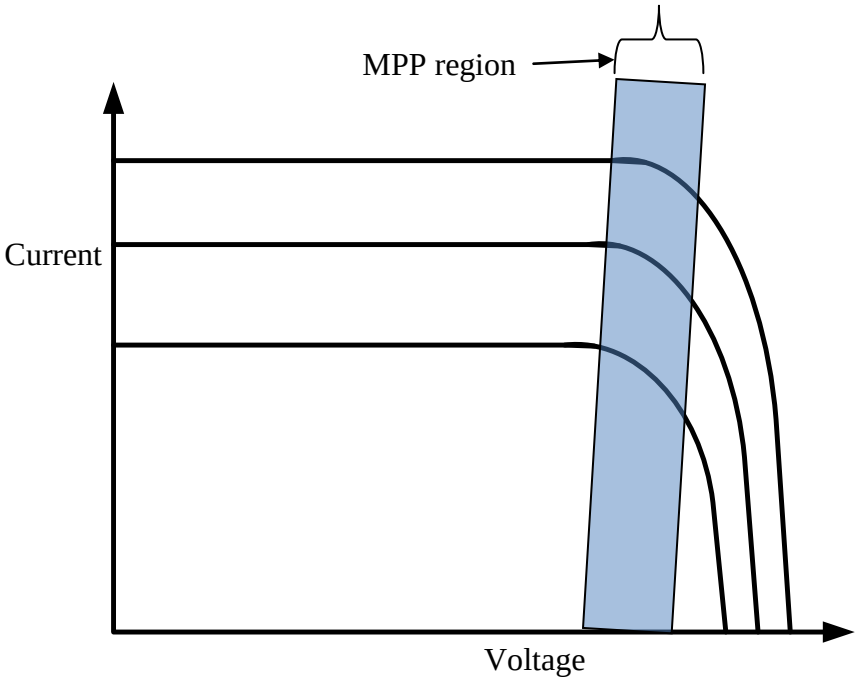


Figure 2.8. Voltage-Current characteristics of a PV- array

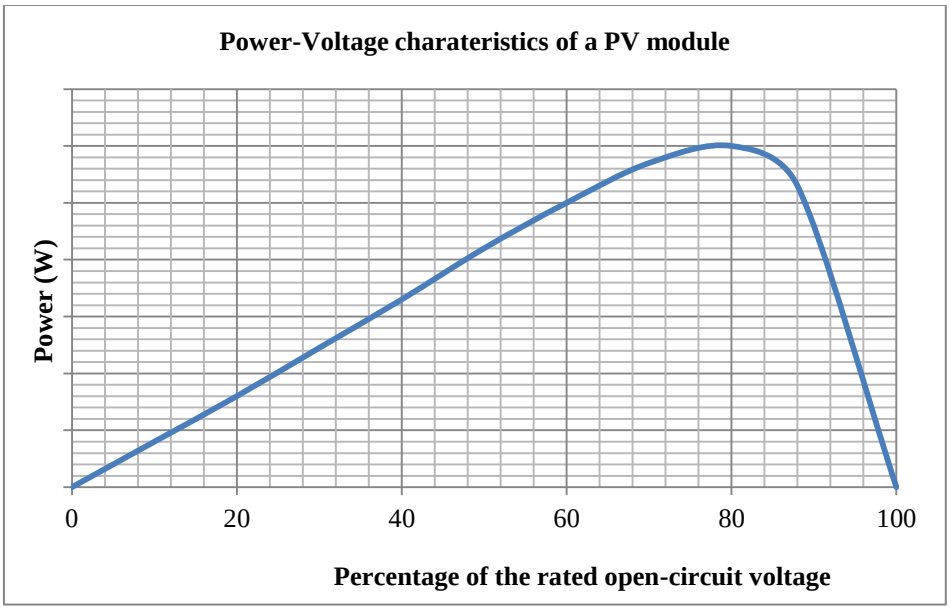


Figure 2.9. PV array power curve

2.3.2 Mismatch errors

Mismatch in a PV array occurs due to the interconnection of modules with different performance characteristics. This result in to detrimental effects like: power loss and reliability degradation. Mismatch losses in solar PV arrays can be due to a variety of reasons including:

I. Differences in the working temperature of PV modules.
II. Shadowing of some cells or PV modules.
III. Different I-V characteristics of the cells during manufacture.
IV. Aging of the PV modules.
V. Inclination or orientation angles of the PV modules.

Due to mismatch loss, lower power than the array rating is delivered [5]. Incorporating a highly efficient DC-DC converter with MPPT function leads to a significant reduction of these power losses. Many MPPT solutions are developed to ensure the optimal utilization of PV modules [19], [22] and [23]. The implementations generally involve sensing the output current and voltage of PV modules, and the MPPT algorithms use the information to maximize power drawn from the PV modules. An example of this is shown in Figure 2.10.

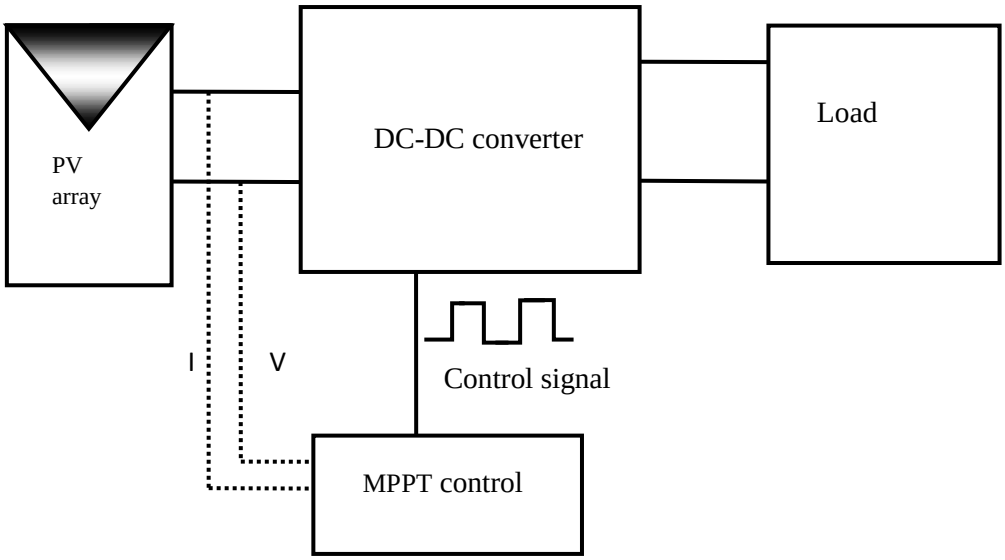


Figure 2.10. Block diagram showing MPPT control in a PV array-Converter connection

2.3.3 MPPT schemes

An MPPT usually consists of a converter under the control of a maximum-power-point-seeking algorithm. Inserting an MPPT between the PV array and the load ensures that the array's operating point is controlled to deliver maximum power. Many MPPT methods have been developed and implemented [19]. Some of the MPPT schemes include:

1) *The Fixed Duty Cycle*- It is the simplest of the methods. It does not require a feedback and the load impedance is adjusted only once for the maximum power point [35].
2) *Fractional Open-Circuit Voltage or Constant voltage method*-This method is based on the fact that there is a near linear relationship between V_{MPP} and V_{OC} of the PV array, under varying irradiance and temperature levels. V_{MPP} is around 0.7 to 0.8 of the V_{OC}. In this scheme, V_{OC} is measured periodically by momentarily shutting down the power converter. An advantage of this scheme is that only voltage needs to be measured. However, it has a disadvantage in that it incurs temporary loss of power each time V_{OC} has to be measured [19], [35].
3) *Perturb and Observe*- This is one of the most popular schemes. The output terminal voltage of the PV array is periodically incremented or decremented while comparing the power obtained in the current cycle with the power of the previous cycle. If there is an increase in power, the subsequent perturbation is kept the same to reach the MPP and if there is a decrease in power, the perturbation should be reversed [19]. This scheme is easy to implement and has a good performance. However, it has a disadvantage that it takes a long time before reaching MPP in case of an irradiation change [36]. A modified version of this scheme is obtained when the perturbation steps are changed according to the distance of the MPP, hence a higher efficiency [35]. DSP and microcontroller control is suitable for this scheme [19].
4) *Hill Climbing*- This scheme involves perturbation in the duty ratio of the power converter. Perturbing the duty ratio then perturbs the PV array current and consequently perturbs the PV array voltage.

5) *Incremental Conductance*- In this scheme, the derivative of power is calculated to get the correct direction for perturbing the array's reference variable. The slope of the PV array power curve on figure 2.8 is zero at the MPP, positive on the left of the MPP and negative on the right [19].

$$\begin{cases} dP/dV = 0, & \text{at MPP} \\ dP/dV > 0, left\ of\ MPP \\ dP/dV < 0, right\ of\ MPP \end{cases}$$

The Incremental Conductance scheme suffers from large sampling periods, though it does not suffer from fast transients in environmental conditions [35]. DSP and microcontroller control can be applied in this scheme; hence a track of previous values of voltage and currents can be kept [19].

6) *Fuzzy Logic Control*- This scheme consists of three stages: a) fuzzification, where numerical input variables are converted in to linguistic variables based on a membership function. b) Rule base table look up and c) defuzzification, where the fuzzy logic controller output is converted from a linguistic variable to a numerical variable, still using a membership function [19], [40]. The MPPT fuzzy logic controllers perform well under varying atmospheric conditions. However, this scheme is complex and needs additional hardware hence a limitation in low cost system design.

7) *Neural Network*- A PV array is tested over a period and the patterns between the inputs and outputs of the neural network are recorded, through a training process. PV arrays have different characteristics so a neural network has to be specifically trained for the PV array with which it will be used. The characteristic of a PV array also change with time, hence the neural network has to be periodically trained for an accurate MPPT [19].

8) *Other MPPT schemes include*: Ripple correlation control, Current sweep, DC-Link Capacitor Droop Control, Load Voltage Maximization and the Beta method [19], [35], [36].

In the choice of the MPPT scheme to use, the following aspects should be put in to consideration: cost, complexity, required sensors, convergence speed, hardware requirement, and effectiveness.

2.4 MULTI-PHASE INTERLEAVED-TAPPED-COUPLED-INDUCTOR BOOST CONVERTER WITH DIGITAL CONTROL.

Most of the study done so far on high boost of a PV array voltage is either inefficient or is complex and expensive to implement. These drawbacks associated with existing boost converters and series connection of PV panels encourage a search for a high boost converter topology. There has been no study thus far on interleaving a tapped-coupled-inductor-boost converter, and also applying it to efficiently boost the PV array voltage. This thesis presents a novel step-up converter for boosting a low voltage of a PV array to a high DC-bus voltage which can be used to feed a grid connected inverter or can be applied on a standalone application. It combines the advantages of both interleaving and tapped-coupled inductors. With digital control, the multi-phase converter switching signals can be re-configured efficiently in case of changes in the PV array output, which may be due to an open circuit of a panel string due to shading.

Compared to the proposed converters in the literature, the proposed converter has the following merits:

a) Circuit simplicity since a conventional interleaved boost converter comprising of two series coupled inductors with a switch tapping is used.
b) High boost ratios are ensured by both the interleaving and the tapped-coupled-inductor turns ratio.
c) By use of a turns ratio, the duty ratio is kept within a reasonable range, hence avoiding an extreme duty ratio. This results to alleviation of severe reverse-recovery and EMI problems which leads to a high conversion efficiency. An extreme duty ratio is also not desirable as it leaves no room for control which is needed to compensate changes in input and load.
d) The proposed converter enjoys all the advantages of interleaving as mentioned in section 2.2.7. This increases the conversion efficiencies greatly.

e) In the proposed converter the output current ripple is suppressed which makes it suitable for an application such as battery charging which demand current with low ripple.

f) The required number of PV modules in series is reduced since high boosting is done by the proposed converter. This leads to a lower cost of the PV system and reduced mismatch errors on the PV array.

g) By having high voltage boosting of the PV array voltage, the PV system power can be controlled in a wide range by just changing the number of parallel branches in the array. The proposed converter is also suitable for high and variable power operation.

h) It is possible to integrate an MPPT control algorithm to the proposed converter which ensures that maximum power is extracted from the PV array despite the changing environmental conditions, hence maximizing PV conversion efficiency.

i) The proposed converter is suitable for variable input voltage operation by making a trade-off between the choice of turns ratio and duty ratio.

Detailed characterisation of a single-phase tapped-coupled-inductor boost converter and a two-phase interleaved-tapped-coupled-inductor boost converter are also presented in this thesis. Simulations of a single-phase up to a six-phase tapped-coupled-inductor boost converter are also presented for comparison of performance and number of phases. This thesis also goes into detail on the design considerations of a two-phase interleaved-tapped-coupled-inductor boost converter. This includes modelling, simulations, hardware implementation, control algorithms and experimental testing.

CHAPTER 3 BOOST CONVERTER WITH TAPPED-COUPLED-INDUCTORS

In this chapter, a single-phase boost converter with tapped-coupled inductors is described and analysed. Although this converter has previously been proposed, detailed analyses presented in this chapter is not available in the literature. Analysis is done for both ideal and non-ideal single-phase tapped-coupled-inductor boost converter operating in the continuous conduction mode (CCM). Expressions for the voltage boost ratio as well as factors affecting the boost ratio will be presented. Converter waveforms in CCM will be presented and analytical expressions for input average, RMS and ripple current as well as output capacitor RMS current will be derived.

3.1 OPERATION OF THE CONVERTER

A tapped-coupled-inductor boost converter is shown in Figure 3.1. The circuit components include a MOSFET S, a diode D, tapped-coupled inductors, L_1 and L_2, a filter capacitor C and a load resistance R. The MOSFET is turned on by a pulse-width modulator output through a gate drive circuit, at a duty ratio, $= \frac{t_{on}}{t_{on}+t_{off}}$, where t_{on} is the time when the MOSFET is conducting and t_{off} is the time when the MOSFET is not conducting.

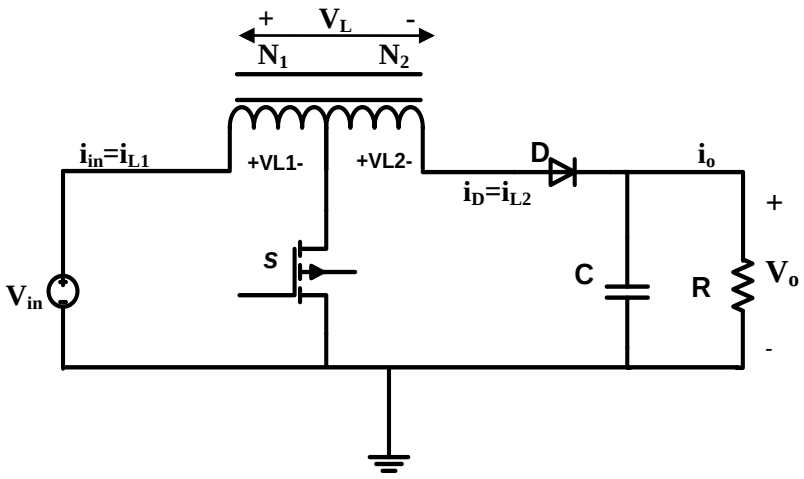


Figure 3.1. Tapped-coupled-inductor boost converter

The windings N_1 and N_2 are on the same core, hence magnetically coupled. When N_2 =0, the configuration reduces to that of a conventional boost converter. The relationship between L_1 and L_2 is determined by the turns ratio of the magnetic element, that is: $\frac{L_2}{L_1} = \left(\frac{N_2}{N_1}\right)^2 = n^2$ [30]. N_1 is the number of turns in the first inductor, L_1 and N_2 is the number of turns in the second inductor, L_2. The converter operates with two states, when the switch is on and off in continuous conduction mode.

3.3.1 Ideal characteristics

In this case, analysis is done with idealized components, thus neglecting the influence of parasitic components and power losses, and for the continuous mode in steady-state.

a) When the switch is conducting,0<t<DTs

When the switch is conducting, the diode D is reversed biased and the equivalent circuit is as shown in figure 3.2.

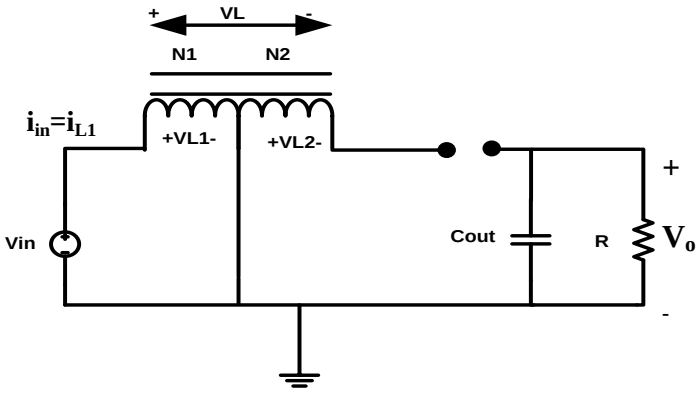


Figure 3.2. Tapped-coupled-inductor boost converter when the active switch is conducting.

With the diode not conducting, the voltage across N_1 is equal to the input voltage V_{in} and energy is stored in the inductor L_1.

$$V_{in} = V_{L1} \tag{3-1}$$

$$V_{L1} = L_1 \frac{di_{L1}}{dt} = V_{in} \tag{3-2}$$

Due to magnetic coupling, a voltage is induced in the second inductor, L_2, due to current i_{L1} flowing through the first inductor L_1, though no current flows through L_2 during this interval.

$$V_{L2} = M\frac{di_{L1}}{dt} \tag{3-3}$$

Where mutual inductance, $M = k\sqrt{L_1 L_2}$, and k is the coupling coefficient.

$$\frac{L_2}{L_1} = \left(\frac{N_2}{N_1}\right)^2 = n^2 \Rightarrow L_2 = n^2 L_1 \tag{3-4}$$

Where n is the turns ratio defined as $\frac{N_2}{N_1}$.

$$M = k\sqrt{n^2 {L_1}^2} \Rightarrow knL_1 \tag{3-5}$$

$$\therefore V_{L2} = M\frac{di_{L1}}{dt} = nkL_1\frac{di_{L1}}{dt} = nkV_{L1} = nkV_{in} \tag{3-6}$$

$$V_L = V_{L1} + V_{L2} = (1 + nk)V_{L1} \tag{3-7}$$

$$\Rightarrow V_{L,on} = (1 + nk) \times V_{in} \tag{3-8}$$

Where, $V_{L,on}$ is tapped-coupled-inductor voltage when the switch is conducting.

Expression for current through the capacitor C_{out} in figure 3.2 is obtained as:

$$i_c = C\frac{dV_o}{dt} = -\frac{V_o}{R} \tag{3-9}$$

Input current during this interval is given as:

$$i_{in} = i_{L1} \tag{3-10}$$

b) When the switch is off, $DT_s<t<T_s$

When the switch is off, the diode is forward biased. Energy stored in the inductors and from the input is supplied through the conducting diode to the output. Both windings N_1 and N_2 conduct the same current i_L. The voltage across both inductors is equal to $(V_{in} - V_o) = V_1 + V_2$, where V_1 and V_2 are shown in equations (3-11) and (3-12). As it can be seen

in these two equations, the voltage across each of the inductors has an induced voltage component.

$$V_1 = L_1 \frac{di_L}{dt} + M \frac{di_L}{dt} \Rightarrow (L_1 + M) \frac{di_L}{dt} \tag{3-11}$$

$$V_2 = L_2 \frac{di_L}{dt} + M \frac{di_L}{dt} \Rightarrow (L_2 + M) \frac{di_L}{dt} \tag{3-12}$$

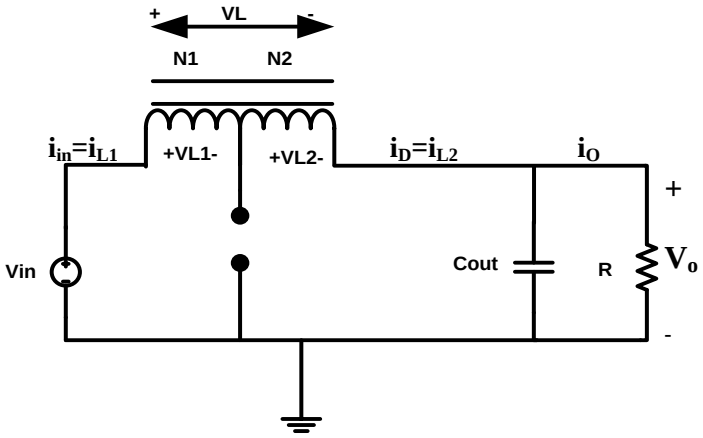


Figure 3.3. Tapped-coupled-inductor boost converter with the output diode conducting.

This induced voltage across each of the inductors is due to the mutual inductance between the coupled inductors. The induced voltage leads to an increased voltage across both inductors, hence a higher boost ratio.

$$\frac{V_1}{L_1 + nkL_1} = \frac{V_2}{n^2 L_1 + nkL_1} \tag{3-13}$$

Since $M = nkL_1$ and $L_2 = n^2 L_1$

$$V_2 = \left(\frac{n^2 + nk}{1 + nk}\right) \times V_1 \tag{3-14}$$

Referring to figure 3.3,

$$(V_{in} - V_o) = V_1 + V_2 \tag{3-15}$$

$$(V_{in} - V_o) = V_1 + \left\{\left(\frac{n^2 + nk}{1 + nk}\right) \times V_1\right\} \tag{3-16}$$

$$\Rightarrow \{V_{in} - V_o\} = V_{L,off} = V_1 \times \left\{\frac{n^2+2nk+1}{1+nk}\right\} \quad (3\text{-}17)$$

Where, $V_{L,off}$ is tapped-coupled-inductor voltage when the switch is not conducting.

An expression for the output capacitor current during this interval is given as:

$$i_c = C\frac{dV_o}{dt} = i_L - \frac{V_o}{R} \quad (3\text{-}18)$$

Input current during this interval is given as:

$$i_{in} = i_L \quad (3\text{-}19)$$

In steady-state, the average voltage across the two coupled inductors over a switching period should be equal to zero, hence

$$\langle V_L \rangle = 0 = D\{(1+nk) \times V_{in}\} + \{(1-D)(V_{in} - V_o)\} \quad (3\text{-}20)$$

$$0 = V_{in}(1+nkD) - V_o(1-D) \quad (3\text{-}21)$$

From equation (3-21) the voltage transfer ratio (the ratio of the output voltage, V_o to the input voltage V_{in}) is obtained as

$$\frac{V_o}{V_{in}} = \frac{1+nkD}{1-D} \quad (3\text{-}22)$$

For a k of 1, $\frac{V_o}{V_{in}} = \frac{1+nD}{1-D}$ (3-23)

From equation (3-22), it can be seen that the voltage transfer ratio of the tapped-coupled boost converter depends on:

- Duty ratio, D
- Turns ratio, n
- Coupling coefficient, k

When n is equal to zero, the tapped-coupled boost converter is reduced to the conventional boost converter which has a voltage gain $\frac{V_o}{V_{in}} = \frac{1}{1-D}$.

Re-arranging equation (3-22) yields an expression for duty ratio as,

$$D = \frac{\left({}^{V_0}/_{V_{in}} - 1\right)}{\left({}^{V_0}/_{V_{in}} + nk\right)} \tag{3-24}$$

From equation (3-24), it is shown that as *n* increases, for a given voltage gain, (V_o/V_{in}), there will be a non-linear decrease in *D*.

Figure 3.4 shows the relationship between voltage gain, duty ratio, *D*, and turns ratio, *n*, for a coupling coefficient, *k*, of 0.98.

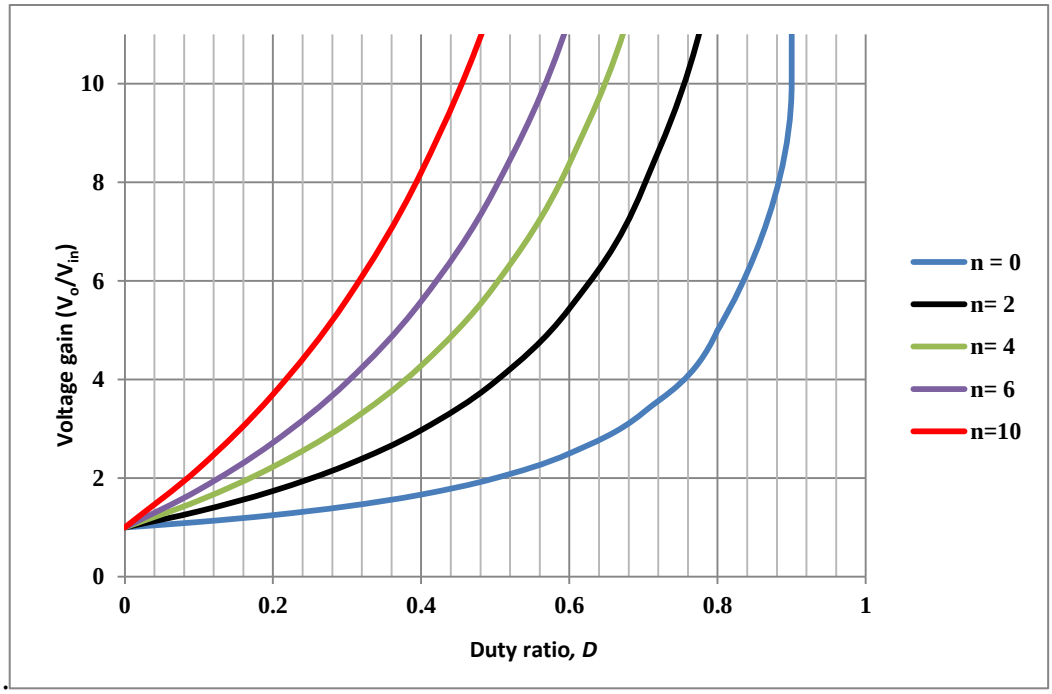


Figure 3.4. Voltage gain against duty ratio D

It can be seen that the conventional boost converter with *n* = 0 requires an extremely high duty ratio to achieve a high voltage gain. With an extreme duty ratio, the output rectifier diode conducts for a very short period sustaining a short pulse width current with a high amplitude. This results in severe reverse-recovery problems and increased device stress. An extreme duty ratio leads to requirements of a high current and voltage rated switch, increasing conduction losses, switching losses and cost. As a result, the conversion efficiency is degraded, EMI problem is likely to be severe and the power level of the

converter is limited. The switch also becomes under-utilised. Furthermore, an extreme duty ratio does not leave room for control to compensate changes in the input or the load [37].

However, the use of the tapped-coupled inductor boost converter with a higher turns ratio makes it possible to achieve high step-up ratios with a low duty ratio. As shown in Figure 3.4, a voltage gain of 10 is achieved with a duty ratio of 0.9 in the classical boost converter. However, with a duty ratio of just 0.56, the same voltage gain can be achieved by the tapped-coupled boost converter with a turns ratio of 6 and even a lower duty ratio of 0.46 with a turns ratio of 10. The selection of number of turns however, should be a trade off since with a very high turns ratio a high boost ratio is achieved but; (1) losses in winding N_2 increase leading to a lower efficiency, (2) a small input variation leads to a large output variation which makes control difficult, (3) inductor L_2 value would be large leading to reduced dynamic response (4) the input current peak-to-peak ripple increases.

The coupling coefficient, k, is a measure of the magnetic coupling between two coils and lies in the range $0 \leq k \leq 1$. When the two windings are tightly coupled so that all the flux linking the primary winding also links the secondary winding, there is no leakage inductance and k=1. This is an ideal situation because it is impossible to wind two coils so that they share precisely the same magnetic flux. High values of coupling coefficient of about 0.98 can however be obtained by tight coupling of the windings thus reducing the leakage inductances in the tapped-coupled inductors.

It can be seen that a high boost ratio is obtained with a high coupling coefficient in the tapped-coupled boost converter from equation (3-22). A low value of k also means high leakage inductance which results in high voltage spikes across the switch during turn-off. This results in efficiency degradation due to the increased switching losses.

3.1.2 Non-ideal characteristics

The model analysed in this section is shown in Figure 3.5 and accounts for winding resistances in the tapped-coupled inductors, r_{L1} and r_{L2}, voltage drop across the conducting active switch and the forward voltage drop across the output diode. Through analysis, the effects of these parasitic components and voltage drops are demonstrated.

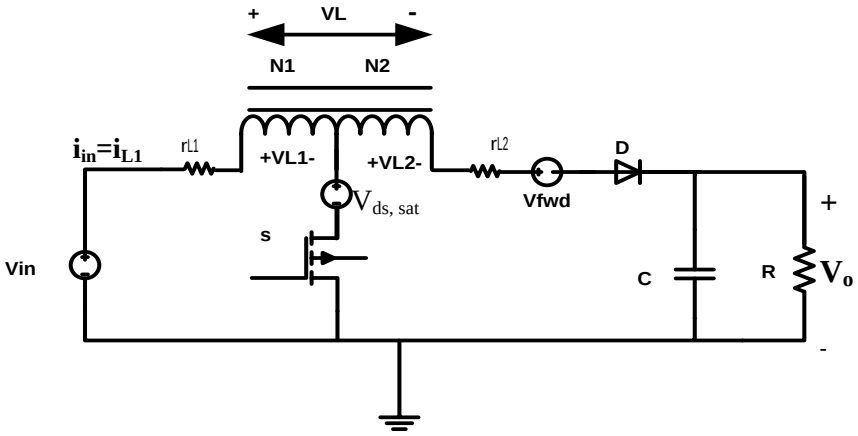


Figure 3.5. A tapped-coupled-inductor boost converter with non-ideal components.

a) When the switch is conducting, 0<t<DTs

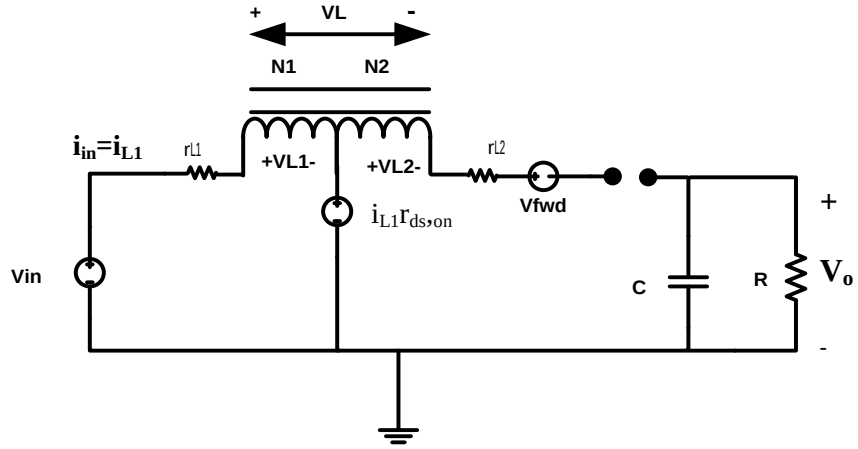


Figure 3.6. A non-ideal tapped-coupled-inductor boost converter when the active switch is conducting.

During this interval, the output diode D is reverse biased while the active switch conducts as shown in Figure 3.6. The input voltage V_{in} is thus described as,

$$V_{in} = V_{L1} + i_{L1}r_{L1} + i_{L1}r_{ds,on} \tag{3-25}$$

$$\therefore V_{L1} = L_1 \frac{di_{L1}}{dt} = \left(V_{in} - i_{L1}r_{ds,on} - i_{L1}r_{L1}\right) \tag{3-26}$$

No current flows through the second inductor during this interval, but due to coupling, a voltage V_{L2} appears across this inductor given as,

$$V_{L2} = M\frac{di_{L1}}{dt} = nkL_1\frac{di_{L1}}{dt} = nkV_{L1} = nk\left(V_{in} - i_{L1}r_{ds,on} - i_{L1}r_{L1}\right) \quad (3\text{-}27)$$

The total voltage across the two tapped-coupled inductors during this interval, V_L is thus given by

$$V_L = V_{L1} + V_{L2} = (1 + nk)V_{L1} \quad (3\text{-}28)$$

$$\Rightarrow V_{L,on} = (1 + nk) \times \left(V_{in} - i_{L1}r_{ds,on} - i_{L1}r_{L1}\right) \quad (3\text{-}29)$$

Where, $V_{L,on}$ is tapped-coupled-inductor voltage when the switch is conducting.

An expression for the output capacitor current in figure 3.6 is obtained as:

$$i_c = C\frac{dV_o}{dt} = -\frac{V_o}{R} \quad (3\text{-}30)$$

Input current during this interval is given as:

$$i_{in} = i_{L1} \quad (3\text{-}31)$$

Where, i_{L1} is the inductor current when both windings N_1 and N_2 are conducting.

c) When the switch is off, $DT_s<t<T_s$

During this interval, the same current, i_L, flows through both inductors. The voltage across the tapped-coupled inductors includes a voltage due to mutual inductance between the two inductors. Referring to Figure 3.7, the voltage across the coupled inductors is expressed as,

$$V_1 = L_1\frac{di_L}{dt} + M\frac{di_L}{dt} \Rightarrow (L_1 + M)\frac{di_L}{dt} \quad (3\text{-}32)$$

$$V_2 = L_2\frac{di_L}{dt} + M\frac{di_L}{dt} \Rightarrow (L_2 + M)\frac{di_L}{dt} \quad (3\text{-}33)$$

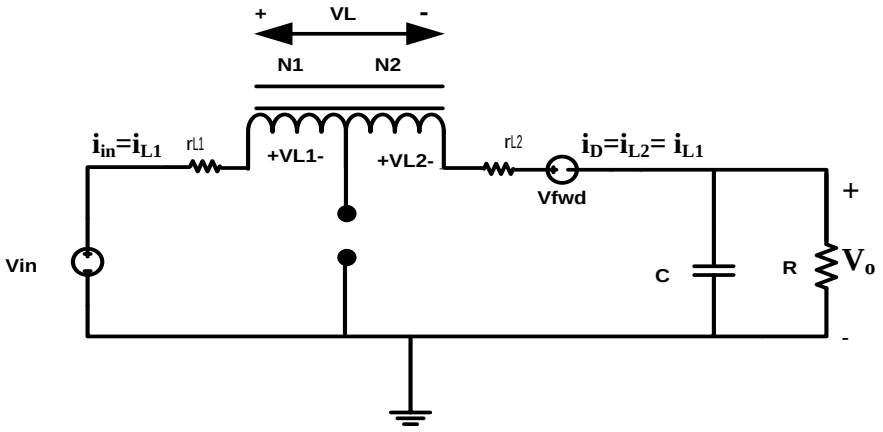


Figure 3.7. Tapped-coupled-inductor boost converter with the output diode conducting.

Since the same current is flowing through both inductors during this interval its rate of change $\frac{di_L}{dt}$ is also equal, thus,

$$\frac{V_1}{L_1+nkL_1} = \frac{V_2}{n^2L_1+nkL_1} \tag{3-34}$$

Since $M = nkL_1$ and $L_2 = n^2L_1$

$$V_2 = \left(\frac{n^2+nk}{1+nk}\right) \times V_1 \tag{3-35}$$

Referring to Figure 3.7, the input and output voltage can be related to inductor voltage as,

$$(V_{in} - V_o) = V_1 + V_2 + i_L\,(r_{L1} + r_{L2}) + V_{fwd} \tag{3-36}$$

Then using equation (3-34), an expression for the tapped-coupled-inductor voltage when the switch is off is obtained as,

$$(V_{in} - V_o) = V_1 + \left\{\left(\frac{n^2+nk}{1+nk}\right) \times V_1\right\} + i_L\,(r_{L1} + r_{L2}) + V_{fwd} \tag{3-37}$$

$$V_{L,off} = \{V_{in} - V_o - V_{fwd} - i_L\,(r_{L1} + r_{L2})\} = V_1\left\{\frac{n^2+2nk+1}{1+nk}\right\} \tag{3-38a}$$

Referring to Figure 3.7

$$V_{L1} = \left(\frac{N_1}{N_1+N_2}\right) \times V_{L,off} = \left(\frac{1}{1+n}\right) \times \{V_{in} - V_o - V_{fwd} - i_L\,(r_{L1} + r_{L2})\} \quad (3\text{-}38b)$$

$$V_{L2} = \left(\frac{N_2}{N_1+N_2}\right) \times V_{L,off} = \left(\frac{n}{1+n}\right) \times \{V_{in} - V_o - V_{fwd} - i_L\,(r_{L1} + r_{L2})\} \quad (3\text{-}38c)$$

An expression for current through the output capacitor during this interval is given as:

$$i_c = C\frac{dV_o}{dt} = i_L - \frac{V_o}{R} \quad (3\text{-}39)$$

Input current during this interval is given as:

$$i_{in} = i_L = i_{L1} \quad (3\text{-}40)$$

Equations (3-28) and (3-37) are averaged for the two time intervals using duty ratio as a weight to obtain one voltage equation applicable over one switching period:

$$\begin{aligned} V_L = L\frac{di_L}{dt} = {} & \left[D \times \{(1+nk) \times (V_{in} - i_{L1}r_{ds,on} - i_{L1}r_{L1})\}\right] \\ & + \left[(1-D) \times \{V_{in} - V_o - V_{fwd} - i_L\,(r_{L1} + r_{L2})\}\right] \end{aligned} \quad (3\text{-}41)$$

The equation for the output voltage is obtained as:

$$\begin{aligned} V_o = \frac{1}{(1-D)}\{ & V_{in}(1+nkD) + V_{fwd}(D-1) - Di_{L1}r_{ds,on}(1+nk) \\ & - Dni_L\,r_{L1}\big(1+k(1+n)\big) - i_L\,(r_{L1} + r_{L2})\} \end{aligned} \quad (3\text{-}42)$$

The ripple current through the capacitor over one switching period is:

$$i_c = C\frac{dv_c}{dt} = \left[D \times \left(-\frac{V_o}{R}\right)\right] + \left[(1-D) \times \left(i_L - \frac{V_o}{R}\right)\right] \quad (3\text{-}43)$$

The average input current over one switching period is given as:

$$I_{in,ave} = I_L(nkD + 1) \quad (3\text{-}44)$$

The key waveforms of a single phase tapped-coupled inductor boost converter are shown in Figure 3.8.

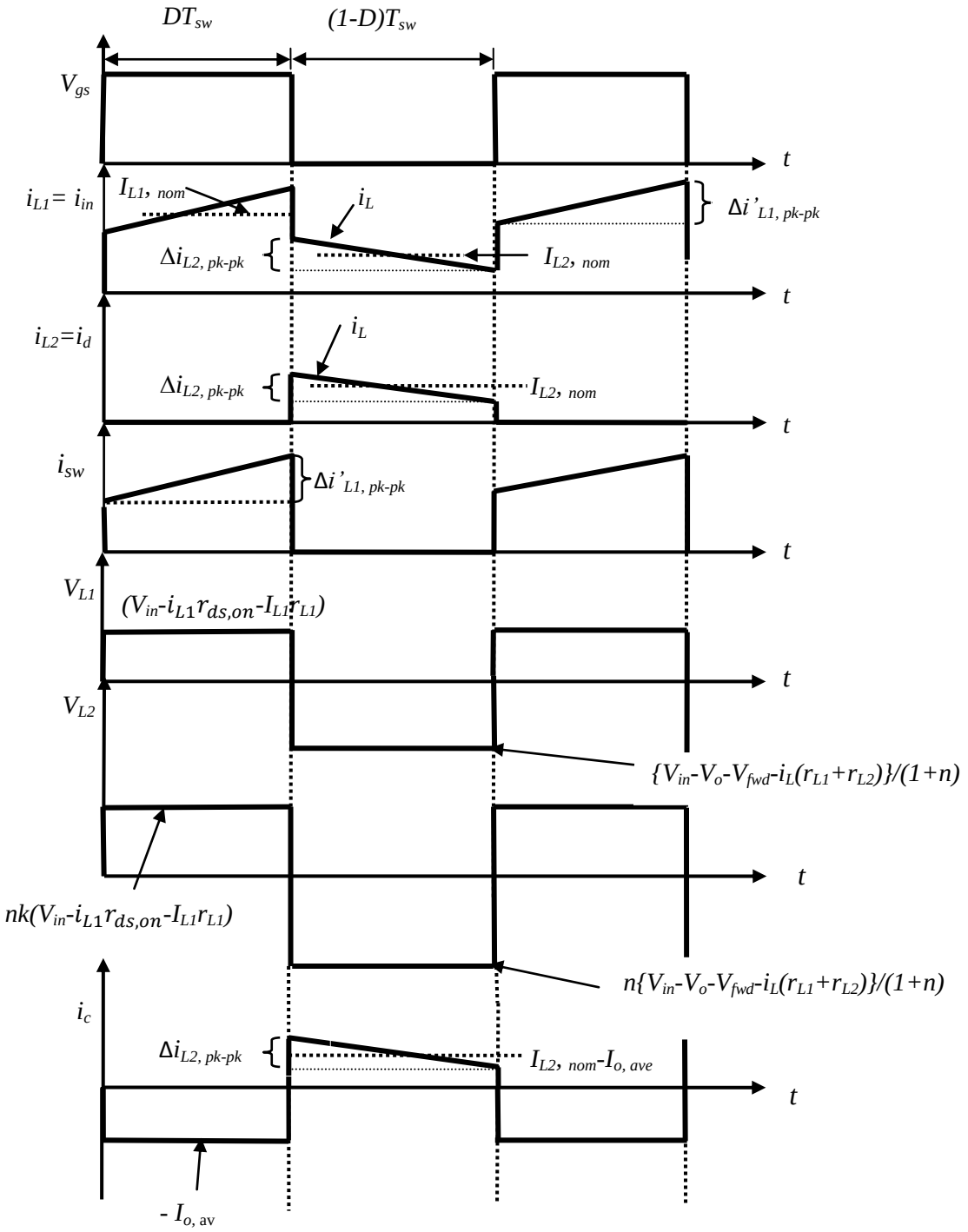


Figure 3.8. Key waveforms for the single-phase tapped-coupled inductor boost converter.

Due to the tapped-coupled inductor, the shape of the current through the inductor is quite different from that for a conventional boost converter. When the active switch is conducting, the current through the first inductor winding N_1 ramps up linearly from an initial value until when the switch goes off. At this interval, no current flows through the second winding N_2 since the diode is reverse biased.

During the switching transitions, the flux through the core cannot change instantaneously, therefore the current through N_1 steps down immediately when the switch is turning off. When the active switch stops conducting, the diode becomes forward biased and the same current flows through both sections N_1 and N_2 of the tapped inductor.

3.1.3 Input and capacitor current RMS ripple derivation

In this section, expressions for the input current peak-to-peak ripple, RMS current, RMS ripple and the output capacitor RMS current are obtained. With reference to Figure 3.8, the following expressions are obtained,

$$I_{L2,ave} = I_{o,ave} = I_{L2,nom}(1 - D) \tag{3-45}$$

$$I_{L2,nom} = \frac{I_{o,ave}}{(1-D)} \tag{3-46}$$

If operating conditions are ideal,

$$P_{in} = P_o \Rightarrow V_{in,ave} I_{in,ave} = V_{o,ave} I_{o,ave} \tag{3-47}$$

But from equation (3-22),

$$V_{o,ave} = V_{in,ave} \frac{1+nkD}{1-D} \tag{3-48}$$

$$V_{in,ave} \frac{1+nkD}{1-D} I_{o,ave} = V_{in,ave} I_{in,ave} \tag{3-49}$$

$$I_{in,ave} = \frac{1+nkD}{1-D} I_{o,ave} = I_{L1,ave} \tag{3-50}$$

$$I_{in,ave} = I_{L1,ave} = I_{L1,nom} D + I_{L2,nom}(1 - D) = \frac{1+nkD}{1-D} I_{o,ave} \tag{3-51}$$

Substituting equation (3-46) into (3-51) yields,

$$I_{L1,nom}D + \frac{I_{o,ave}}{(1-D)}(1-D) = \frac{1+nkD}{1-D}I_{o,ave} \tag{3-52}$$

$$I_{L1,nom}D = \left(\frac{1+nkD}{1-D} - 1\right)I_{o,ave} = \left(\frac{D+nkD}{1-D}\right)I_{o,ave} \tag{3-53}$$

Expressions for $I_{L1,\,nom}$ and $I_{in,\,ave}$ are obtained in terms of $I_{L2,\,nom}$ as,

$$I_{L1,nom} = \left(\frac{1+nk}{1-D}\right)I_{o,ave} = (1+nk)I_{L2,nom} \tag{3-54}$$

$$I_{in,ave} = I_{L1,ave} = (1+nk)I_{L2,nom}D + I_{L2,nom}(1-D) = (nkD+1)I_{L2,nom} \tag{3-55}$$

From equations (3-26) and (3-38),

$$\Delta i'_{L1,pk-pk} = \frac{(V_{in} - i_{L1}r_{ds,on} - i_{L1}r_{L1})DT_{sw}}{L_1} \tag{3-56}$$

$$\Delta i_{L2,pk-pk} = \frac{n\left(V_{in} - V_o - V_{fwd} - i_L\,(r_{L1}+r_{L2})\right)(1-D)T_{sw}}{(n+1)L_2} \tag{3-57}$$

An expression for the input RMS current in a single-phase tapped-coupled-inductor boost converter is then obtained as,

$$I_{L1,rms} = \sqrt{\left\{\left(I_{L1,nom}\right)^2 D\left[1 + \frac{1}{3}\left(\frac{\Delta i'_{L1,pk-pk}}{2I_{L1,nom}}\right)^2\right] + \left(I_{L2,nom}\right)^2(1-D)\left[1 + \frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2I_{L2,nom}}\right)^2\right]\right\}} \tag{3-58a}$$

Substituting equations (3-46) and (3-54) in to (3-58a), the expression for the input RMS current is obtained as,

$$I_{L1,rms} = I_{in,rms} =$$

$$\sqrt{\left\{\left(\left(\frac{1+nk}{1-D}\right)I_{o,ave}\right)^2 D\left[1 + \frac{1}{3}\left(\frac{\Delta i'_{L1,pk-pk}}{2\left(\frac{1+nk}{1-D}\right)I_{o,ave}}\right)^2\right] + \left(\frac{I_{o,ave}}{(1-D)}\right)^2(1-D)\left[1 + \frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2\left(\frac{I_{o,ave}}{(1-D)}\right)}\right)^2\right]\right\}} \tag{3-58b}$$

From equation (3-58b), it is seen that input RMS current is dependent on turns ratio, coupling coefficient and duty ratio and tends to infinity as duty ratio approaches to unity. For a given duty ratio, a high value of turns ratio and coupling coefficient results to a high value of input RMS current.

The input RMS current ripple can then be obtained with reference to figure. 3.8 and equations (3-51) and (3-58b) as.

$$I_{in,ripple,rms} = I_{o,ave}\sqrt{\left\{D\left(\frac{1+nk}{1-D}\right)^2\left[1+\frac{1}{3}\left(\frac{\Delta i'_{L1,pk-pk}}{2\left(\frac{1+nk}{1-D}\right)I_{o,ave}}\right)^2\right]+\frac{1}{(1-D)}\left[1+\frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2\left(\frac{I_{o,ave}}{(1-D)}\right)}\right)^2\right]-\left(\frac{1+nkD}{1-D}\right)^2\right\}} \quad (3\text{-}59)$$

It is seen from equation (3-59) that the input RMS current ripple expression tends to infinity as the duty ratio approaches unity. The input ripple also is seen to depend on turns ratio, coupling coefficient, duty ratio and load current. A high value of duty ratio, turns ratio, coupling coefficient and load current result to a high input ripple current.

The input current peak-to-peak ripple can be expressed as,

$$i_{in,pk-pk} = \left[I_{L1,nom}+\frac{1}{2}\left(\Delta i'_{L1,pk-pk}\right)\right]-\left[I_{L2,nom}+\frac{1}{2}\left(\Delta i_{L2,pk-pk}\right)\right] \quad (3\text{-}60)$$

Substituting equations (3-46), (3-54), (3-56) and (3-57) into (3-60), the peak-to-peak ripple is obtained as,

$$i_{in,pk-pk} = \left[\left(\frac{nk}{1-D}\right)I_{o,ave}+\left(\frac{(V_{in}-i_{L1}r_{ds,on}-i_{L1}r_{L1})DT_{sw}}{2L_1}\right)\right]+\left(\frac{n\left(V_{in}-V_o-V_{fwd}-i_L\left(r_{L1}+r_{L2}\right)\right)(1-D)T_{sw}}{2(n+1)L_2}\right) \quad (3\text{-}61)$$

The input peak-to-peak current in expression (3-61) is seen to increase with increase in turns ratio, coupling coefficient, inductor value, duty ratio and load current. This expression tends to infinity as duty ratio approaches unity.

Referring to the capacitor current waveform in Figure 3.8 and equation (3-46), an expression for capacitor RMS current is obtained as,

$$I_{c,rms} = \sqrt{\left\{\left(I_{o,ave}\right)^2 D + \left(I_{L2,nom} - I_{o,ave}\right)^2 (1-D)\left[1 + \frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2\left(I_{L2,nom} - I_{o,ave}\right)}\right)^2\right]\right\}} \quad (3\text{-}62a)$$

$$I_{c,rms} = \sqrt{\left\{\left(I_{o,ave}\right)^2 D + \left(\frac{DI_{o,ave}}{(1-D)}\right)^2 (1-D)\left[1 + \frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2\left(\frac{DI_{o,ave}}{(1-D)}\right)}\right)^2\right]\right\}} \quad (3\text{-}62b)$$

It is seen from equation (36) that capacitor RMS current is almost independent of turns ratio and coupling coefficient for a fixed load current except for the term $\Delta i_{L2,\,pk\text{-}pk}$.

3.2 SMALL-SIGNAL MODEL OF THE SINGLE-PHASE TAPPED-COUPLED-INDUCTOR BOOST CONVERTER.

The converter equations were linearized to obtain small-signal expressions as follows:

$$L\frac{d\tilde{\imath}_{L(t)}}{dt} = \left(D + \tilde{d}(t)\right)(1+nk)\left[V_{in} + \tilde{v}_{in}(t) - (I_{L1} + \tilde{\imath}_{L1})r_{ds,on} - (1+n)r_{L1}I_L - (1+n)r_{L1}\tilde{\imath}_L(t)\right] + \left(1 - D - \tilde{d}(t)\right)\left[V_{in} + \tilde{v}_{in}(t) - V_o - \tilde{v}_o(t) - V_{fwd} - I_L(r_{L1} + r_{L2}) - \tilde{\imath}_L(t)(r_{L1} + r_{L2})\right] \quad (3\text{-}63)$$

$$C\frac{d\tilde{v}_c}{dt} = \left(I_L + \tilde{\imath}_L(t)\right)\left(1 - D - \tilde{d}(t)\right) - \frac{V_o}{R} - \frac{\tilde{v}_o(t)}{R} \quad (3\text{-}64)$$

$$V_O + \tilde{v}_o = \left(\frac{1+nkD}{1-D}\right)(V_{in} + \tilde{v}_{in}) \quad (3\text{-}65)$$

$$I_{in} + \tilde{\imath}_{in}(t) = \left(I_L + \tilde{\imath}_L(t)\right)\left(nk\left[D + \tilde{d}(t)\right] + 1\right) \quad (3\text{-}66)$$

DC-terms were obtained from equations (3-63) to (3-66) as,

$$0 = D(1+nk)\left[V_{in} - I_{L1}r_{ds,on} - (1+n)r_{L1}I_L\right] + (1-D)\left[V_{in} - V_o - V_{fwd} - I_L(r_{L1} + r_{L2})\right] \quad (3\text{-}67)$$

$$0 = (I_L)(1-D) - \frac{V_o}{R} \tag{3-68}$$

$$V_O = \left(\frac{1+nkD}{1-D}\right) \times (V_{in}) \tag{3-69}$$

$$I_{in} = I_L(nkD+1) \tag{3-70}$$

AC- terms were obtained from equations (3-63) to (3-66) as,

$$\begin{aligned} L\frac{d\tilde{\imath}_{L(t)}}{dt} = {} & D(1+nk)\left[\tilde{v}_{in}(t) - (1+n)r_{L1}\tilde{\imath}_L(t) - \tilde{\imath}_{L1}r_{ds,on}\right] \\ & + \tilde{d}(t)(1+nk)\left[V_{in} - I_{L1}r_{ds,on} - (1+n)r_{L1}I_L\right] \\ & + (1-D)[\tilde{v}_{in}(t) - \tilde{v}_o(t) - \tilde{\imath}_L(t)(r_{L1}+r_{L2})] - \tilde{d}(t)[V_{in} - V_o - V_{fwd} \\ & - I_L(r_{L1}+r_{L2})] \end{aligned} \tag{3-71}$$

$$C\frac{d\tilde{v}_c(t)}{dt} = \tilde{\imath}_L(t)(1-D) - \tilde{d}(t)I_L - \frac{\tilde{v}_o(t)}{R} \tag{3-72}$$

$$\tilde{v}_o(t) = \left(\frac{1+nkD}{1-D}\right) \times (\tilde{v}_{in}(t)) \tag{3-73}$$

$$\tilde{\imath}_{in}(t) = \tilde{\imath}_L(t)(nkD+1) + \tilde{d}(t)nkI_L \tag{3-74}$$

The AC terms were transformed into the S-domain to yield,

$$\begin{aligned} sL\tilde{\imath}_L(s) = {} & D(1+nk)\left[\tilde{v}_{in}(s) - (1+n)r_{L1}\tilde{\imath}_L(s) - \tilde{\imath}_{L1}(s)r_{ds,on}\right] \\ & + \tilde{d}(s)(1+nk)\left[V_{in} - I_{L1}r_{ds,on} - (1+n)r_{L1}I_L\right] \\ & + (1-D)[\tilde{v}_{in}(s) - \tilde{v}_o(s) - \tilde{\imath}_L(s)(r_{L1}+r_{L2})] - \tilde{d}(s)[V_{in} - V_o - V_{fwd} \\ & - I_L(r_{L1}+r_{L2})] \end{aligned} \tag{3-75}$$

$$sC\tilde{v}_o(s) = \tilde{\imath}_L(s)(1-D) - \tilde{d}(s)I_L - \frac{\tilde{v}_o(s)}{R} \tag{3-76}$$

$$\tilde{v}_o(s) = \left(\frac{1+nkD}{1-D}\right) \times (\tilde{v}_{in}(s)) \tag{3-77}$$

$$\tilde{\imath}_{in}(s) = \tilde{\imath}_L(s)(nkD+1) + \tilde{d}(s)nkI_L \tag{3-78}$$

Equations (3-73) and (3-74) can be rearranged as:

$$sL\tilde{\imath}_L(s) = \tilde{v}_{in}(s)[D(1+nk)+(1-D)] + \tilde{d}(s)[(1+nk)\big(V_{in} - I_{L1}r_{ds,on} - (1+n)r_{L1}I_L\big) - (V_{in} - V_o - V_{fwd} - I_L(r_{L1}+r_{L2}))] + \tilde{v}_o(s)(D-1) - \tilde{\imath}_L(s)[D(1+nk)(1+n)r_{L1} + (1-D)(r_{L1}+r_{L2}) - (1+nkD)r_{ds,on}] \quad (3\text{-}79)$$

$$\tilde{\imath}_L(s) = \left[\frac{sCR+1}{R(1-D)}\right]\tilde{v}_o(s) + \tilde{d}(s)\left[\frac{I_L}{(1-D)}\right] \quad (3\text{-}80)$$

Substituting equation (3-80) into (3-79), the following is obtained:

$$\left(\left[\frac{sCR+1}{R(1-D)}\right]\tilde{v}_o(s) + \tilde{d}(s)\left[\frac{I_L}{(1-D)}\right]\right) \times (sL + [D(1+nk)(1+n)r_{L1}] + [(1-D)(r_{L1}+r_{L2})]) - \tilde{v}_o(s)(D-1) = \tilde{v}_{in}(s)[D(1+nk)+(1-D)] + \tilde{d}(s)[(1+nk)\big(V_{in} - \tilde{\imath}_{L1}r_{ds,on} - (1+n)r_{L1}I_L\big) - (V_{in} - V_o - V_{fwd} - I_L(r_{L1}+r_{L2}))] \quad (3\text{-}81)$$

Defining

A =

$$s^2CRL + s[CRD(1+nk)(1+n)r_{L1} + CR(1-D)(r_{L1}+r_{L2}) + L] + D(1+nk)(1+n)r_{L1} + (1-D)(r_{L1}+r_{L2}) + R(1-D)^2$$

B= $[(1+nk)\big(V_{in} - \tilde{\imath}_{L1}r_{ds,on} - (1+n)r_{L1}I_L\big) - (V_{in} - V_o - V_{fwd} - I_L(r_{L1}+r_{L2}))]$

From this analysis, two significant transfer functions required to analyse the dynamic performance of the single-phase tapped-coupled-inductor boost converter are obtained.

$$G_{v_o d} = \frac{\tilde{v}_o(s)}{\tilde{d}(s)}\Big|_{\tilde{v}_{in}(s)=0} = \frac{B}{A} \quad (3\text{-}82)$$

Equation (3-82) is used to determine how the converter control input disturbances, $\tilde{d}(s)$ influence the output voltage, $\tilde{v}_o(s)$ while equation (3-83) provides information used to show how the converter input voltage disturbances, $\tilde{v}_{in}(s)$ affect the output voltage. Regulation of the DC output voltage of the single-phase tapped-coupled-inductor boost converter depends on the response of the transfer function in equation (3-82) relating the output voltage to control.

$$G_{v_o\tilde{v}_{in}} = \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)}\Big|_{\tilde{d}(s)=0} = \frac{\{[1+nkD]R(1-D)\}}{A} \tag{3-83}$$

Compared to the conventional boost converter transfer functions, the tapped-coupled-inductor boost converter transfer functions in (3-82) and (3-83) are affected by the turns ratio, *n* and the coupling coefficient, *k*. These parameters increase the DC gain of the transfer functions. Converter transfer functions shown in equations (3-82) and (3-83) can be used to construct bode plots. From the bode plots, parameters such as the gain- margin, phase-margin, quality factor and resonant frequency can be obtained. The stability and the dynamic performance of the converter can then be inferred from these parameters. A suitable controller that ensures converter stability under all operating conditions can then designed.

3.3 CHAPTER CONCLUSION

This chapter discusses the operation of a single-phase tapped-coupled-inductor boost converter. Detailed analyses and key waveforms presented in this chapter are not currently available in the literature. The effects of tapped-coupled-inductor on performance are explained. Analysis was done for an ideal and a non-ideal converter and the key waveforms for the converter presented. A small-signal model of the converter is derived.

The voltage transfer ratio of this DC-DC converter is shown to depend on duty ratio, turns ratio and the coupling coefficient between the two coupled inductors. In the previous studies of this converter by other researchers, the effects of the coupling coefficient were ignored. As the turns ratio increases for a given voltage gain, the duty ratio decreases. A trade-off has to be made between the turns ratio and the duty cycle. It is necessary to

reduce the leakage inductance in the tapped-coupled-inductor by ensuring tight coupling between the inductors. This will lead to a high coupling coefficient which is shown to translate in to a high voltage boost. Compared to the conventional boost converter, the single-phase tapped-coupled-inductor boost converter achieves a high voltage boost ratio at lower duty ratios.

Analytical expressions for average, RMS and ripple input current, as well as the output capacitor RMS current are derived and their dependency on turns ratio, coupling coefficient, duty ratio and load current shown**.** These expressions can be used to determine the input and output performance characteristics of this converter and sizing of the converter components.

The single-phase tapped-coupled-inductor boost converter was modelled and two significant transfer functions obtained. The control-to-output and the line-to-output transfer functions were obtained which demonstrated the effects of the turns ratio and the coupling coefficient, parameters not present in the conventional boost converter.

CHAPTER 4 PROPOSED MULTI-PHASE BOOST CONVERTER WITH TAPPED-COUPLED-INDUCTORS

In this chapter, the operation of the proposed N-phase interleaved boost converter with tapped-coupled inductors is described, where N is the number of phases. In the proposed converter identical single-phase tapped-coupled-inductor boost converters described in chapter 3 are connected in parallel, hence sharing the input current. Each interleaved single-phase converter is referred to as a phase. Each phase processes $1/N^{th}$ of the rated power of the complete DC-DC converter. Advantages of both tapped-coupled-inductors and interleaving are hence obtained by using this converter. Analysis is done for a two-phase interleaved tapped-coupled-inductor boost converter in this chapter and voltage gain equations obtained. Modelling of a two-phase converter is also done to obtain the transfer functions needed for closed-loop controller design as well as converter performance analysis. A prototype of a two-phase interleaved tapped-coupled-inductor boost converter was also built to illustrate practically the advantages of the tapped-coupled-inductors and interleaving.

4.1 TOPOLOGY DERIVATION OF THE PROPOSED INTERLEAVED MULTI-PHASE BOOST CONVERTER WITH TAPPED-COUPLED INDUCTORS.

The proposed interleaved converter is shown in Figure 4.1. The circuit components for the N-phase tapped-coupled-inductor boost converter include MOSFETS S_1 to S_N, diodes D_1 to D_N, N sets of coupled inductors with a switch tap, an output filter capacitor, C and a load resistor R. Inductors L_{11} and L_{21} are coupled together and switch tapped and belong to the first converter while L_{1N} and L_{2N} are coupled together and also switch tapped and belong to the nth converter. The windings of the coupled inductors are connected in a series adding mode, thus cumulatively coupled and they have a coupling coefficient *k*. An RCD snubber circuits are used to absorb the leakage energy and suppress the voltage spikes across the MOSFETs when they are turned off.

The voltage gain is extended by selecting a proper turns ratio between the first and the second inductors of each of the coupled inductors.

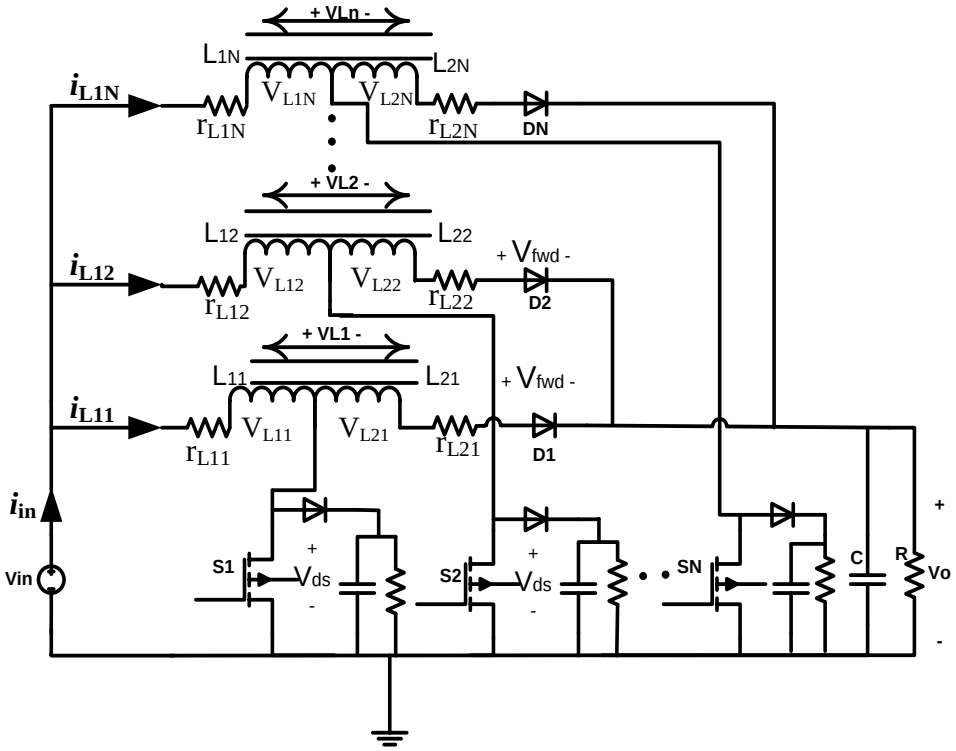


Figure 4.1. Proposed interleaved multi-phase boost converter with tapped-coupled inductors.

In the proposed interleaved converter in Figure 4.1, the interleaved converters have the same duty ratio but with a $^{2\pi}/_{N}$ phase shift. The converters are thus controlled by complementary signals, with the same switching frequency.

It will be shown later in this document that due to the current sharing by the phases in the proposed converter, the inductors current harmonics are cancelled, reducing the ripple in the input current. At the same time, the output voltage ripple is mitigated and the electromagnetic interferences would be expected to reduce. For an N-phase interleaved tapped-coupled-inductor converter, there is an N-fold increase in fundamental ripple frequency in both the input and output waveforms compared to the single-phase converter.

The input current is shared between the N-interleaved phases. This, in turn, reduces the peak, RMS and average currents per phase. Copper losses, switch losses, diode losses and voltages drop across the inductors are also reduced leading to a higher voltage boost ratio and efficiency compared to a single-phase converter. For the same voltage boost ratio therefore, the value of duty ratio required decreases non-linearly with an increase in N. Table 4.1 shows the influence of N on converter losses assuming identical components on each phase

Table 4.1. Loss comparison with increase in number of interleaved phases.

	Copper loss	Switch conduction loss	Switching loss
1-Phase	$I_L{}^2 r_L$	$(I_{ds,rms})^2 R_{ds,on}$	$[V_{ds,block} I_{ds} f_{sw}(t_{r1} + t_{f1})2]$
2-phase	$2\left(I_L/_2\right)^2 r_L = \{(I_L{}^2) r_L\}/_2$	$\{(I_{ds,rms})^2 R_{ds,on}\}/_2$	$\left[\frac{V_{ds,block} I_{ds}}{2 \times 2} f_{sw}(t_{r1} + t_{f1})2\right] \times 2$
3-phase	$3\left(I_L/_3\right)^2 r_L = \{(I_L{}^2) r_L\}/_3$	$\{(I_{ds,rms})^2 R_{ds,on}\}/_3$	$\left[\frac{V_{ds,block} I_{ds}}{2 \times 3} f_{sw}(t_{r1} + t_{f1})2\right] \times 3$
4-phase	$4\left(I_L/_4\right)^2 r_L = \{(I_L{}^2) r_L\}/_4$	$\{(I_{ds,rms})^2 R_{ds,on}\}/_4$	$\left[\frac{V_{ds,block} I_{ds}}{2 \times 4} f_{sw}(t_{r1} + t_{f1})2\right] \times 4$
5-phase	$5\left(I_L/_5\right)^2 r_L = \{(I_L{}^2) r_L\}/_5$	$\{(I_{ds,rms})^2 R_{ds,on}\}/_5$	$\left[\frac{V_{ds,block} I_{ds}}{2 \times 5} f_{sw}(t_{r1} + t_{f1})2\right] \times 5$
6-phase	$6\left(I_L/_6\right)^2 r_L = \{(I_L{}^2) r_L\}/_6$	$\{(I_{ds,rms})^2 R_{ds,on}\}/_6$	$\left[\frac{V_{ds,block} I_{ds}}{2 \times 6} f_{sw}(t_{r1} + t_{f1})2\right] \times 6$
N-phase	$N\left(I_L/_N\right)^2 r_L = \{(I_L{}^2) r_L\}/_N$	$\{(I_{ds,rms})^2 R_{ds,on}\}/_N$	$\left[\frac{V_{ds,block} I_{ds}}{2 \times N} f_{sw}(t_{r1} + t_{f1})2\right] \times N$

Duty ratios $D1>D_2>D_3>D_4>D_5>D_6>D_N$. The switch rise time, t_r and fall time, t_f also decrease with an increase in N hence a decrease in energy dissipated E_{on} and E_{off} resulting to lower switching losses as N increases.

In the proposed interleaved tapped-coupled-inductor boost converter, ripple reduction will be shown to be a function of phase number, N and the duty ratio. The degree of ripple overlap is a function of the duty ratio. Minimum ripple in interleaved converters is obtained whenever the duty ratio matches the ratio of the low-side voltage relative to the high-side voltage of the converter [51]. It will be shown that minimum ripple in the proposed converter is obtained whenever the duty ratio, $D \approx {}^{1}/_{\mathrm{N}}, {}^{2}/_{\mathrm{N}}\ {}^{3}/_{\mathrm{N}} \ldots\ldots {}^{(\mathrm{N}-1)}/_{\mathrm{N}}$

and that complete ripple cancellation can however not be achieved in the interleaved tapped-coupled-inductor boost converters. This is an inherent feature of these converters which is due to the different gradients of the two-coupled inductors' currents. For a two-phase interleaved tapped-coupled-inductor boost converter, minimum ripple in the input and output current and voltage is therefore achieved at a duty ratio of approximately 0.5 while a three-phase converter has minimum ripple at duty ratios of approximately 0.33 and 0.67.

As the number of phases is increased, the ripple amplitude is also reduced over the full range of the switching period. Hence a three-phase interleaved tapped-coupled-inductor converter will have lower ripple amplitude in both its input and output, compared to a two-phase interleaved tapped-coupled-inductor boost converter for a given set of operating conditions.

Magnetic energy storage requirements of a single-phase boost converter with tapped-coupled-inductors L_1 and L_2, and current i_{L1} through the inductors as shown in figure 3.1 are:

$$E_{ind} = \frac{1}{2}\,(L_1 + L_2)\,(i_{L1})^2 \qquad (4\text{-}1)$$

Consider a two-phase converter shown in the multi-phase interleaved boost converter in

Figure 4.1. Further consider a converter with equal power ratings as the single-phase converter and inductors L_{11}, L_{21} and $L_{12,}$ L_{22}, the magnetic energy storage requirements are:

$$E_{2-phase\ Interleaved} = \frac{1}{2}\ (L_{11} + L_{21})\ (i_{L11})^2 + \frac{1}{2}\ (L_{12} + L_{22})\ (i_{L12})^2 \quad (4\text{-}2)$$

i_{L11} and i_{L12} are currents in the first phase and second phase respectively.

Where i_{L11} and i_{L12} are equal to $\frac{1}{2}\ i_{L1}$ and $L_1 + L_2 = L_{11} + L_{21} + L_{12} + L_{22}$

Hence, $$E_{2-phase\ Interleaved} = \frac{1}{2}\left(\frac{1}{2}\ (L_1 + L_2)\ (i_{L1})^2\right) \quad (4\text{-}3a)$$

For an N-phase interleaved converter,

$$E_{N-phase\ Interleaved} = \frac{1}{N}\left(\frac{1}{2}\ (L_1 + L_2)\ (i_{L1})^2\right) \quad (4\text{-}3b)$$

It is seen from equation (4-3a) that the magnetic energy storage requirements when two interleaved converters are used is 50% that of the single converter. For an N-phase interleaved converter, the magnetic energy storage requirements is (100/N) % that of the single converter as seen from equation (4-3b). The physical size of an inductor is directly proportional to the energy storage. By interleaving, small size inductors are employed, leading to better dynamic behaviour since small inductors can change their current in a shorter time.

4.2 ANALYSIS OF A TWO-PHASE INTERLEAVED TAPPED-COUPLED INDUCTOR BOOST CONVERTER.

4.2.1 Operation Analysis

In the proposed converter shown in figure 4.1,

$$V_{L1} = V_{L11} + V_{L21} \quad (4\text{-}4)$$

$$V_{L2} = V_{L12} + V_{L22} \quad (4\text{-}5)$$

$$i_{in} = i_{L11} + i_{L12} \quad (4\text{-}6)$$

The operation of the proposed converter can be divided into four switching intervals per switching period. Non-linear differential equations describing the operation of the proposed converter were obtained from the four switching intervals as follows:

a) *For the interval $0<t<D_1T_{sw}$ when the first converter's switch (S_1) conducts and switch S_2 is off.*

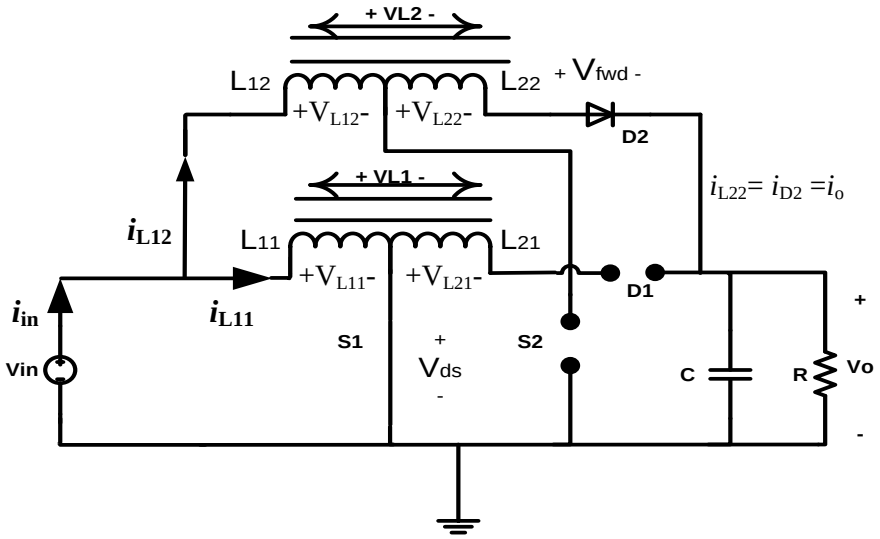


Figure 4.2. Converter during the first switching interval.

During this interval, diode D_1 is reverse biased while diode D_2 is forward biased. The current i_{L11} flows through L_{11} while no current flows through inductor L_{21}. Current i_{L12} flows through both tapped-coupled inductors L_{12} and L_{22}. The following expressions are therefore applicable,

$$V_{in} = V_{L11} = \frac{V_{L1}}{1+nk} \Rightarrow V_{L1} = L_1 \frac{di_{L11}}{dt} = (1+nk)V_{in}$$

$$V_{in} = V_o + V_{L2} \Rightarrow V_{L2} = L_2 \frac{di_{L12}}{dt} = V_{in} - V_o$$

$$i_{s1} = i_{D1} = i_{L21} = 0 \qquad (4\text{-}7)$$

$$i_{D2} = i_{L22} = i_C + i_o \Rightarrow i_C = C\frac{dV_C}{dt} = i_{L22} - \frac{V_o}{R}$$

$$i_{in} = i_{L21}(1 + nk) + i_{L22}$$

$$i_{s1} = i_{L11}$$

b) *For the interval D_1T_{sw} <t<0.5T_{sw} when none of the switches conducts.*

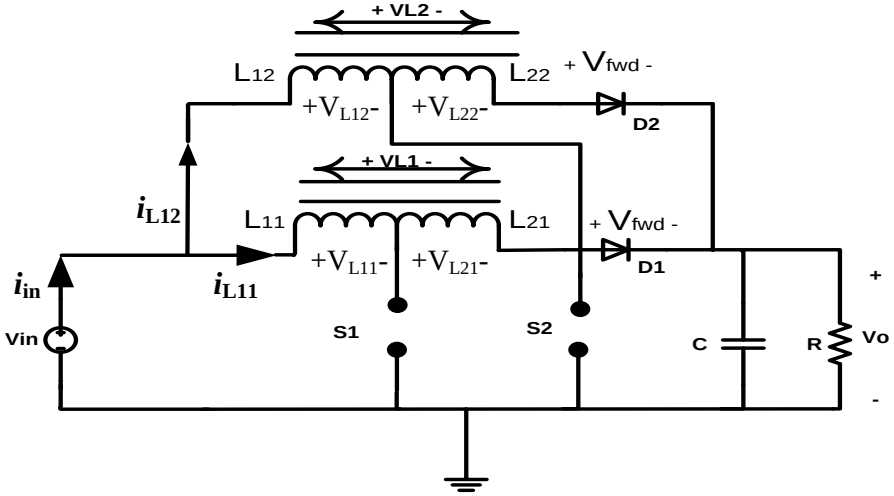


Figure 4.3. The proposed converter during the second switching interval.

As shown in Figure 4.3, none of the active switches conducts and both output diodes are forward biased. Current i_{L11} flows through L_{11} and L_{21} while current i_{L12} flows through inductors L_{12} and L_{22} during this interval. The following expressions are hence applicable,

$$V_{in} = V_{L1} + V_o \Rightarrow V_{L1} = L_1\frac{di_{L11}}{dt} = V_{in} - V_o$$

$$V_{in} = V_{L2} + V_o \Rightarrow V_{L2} = L_2\frac{di_{L12}}{dt} = V_{in} - V_o$$

$$i_{in} = i_{L11} + i_{L12} \tag{4-8}$$

$$i_{s1} = i_{s2} = 0$$

$$i_{D1} = i_{L11} = i_{L21}$$

$$i_{D2} = i_{L12} = i_{L22}$$

$$i_C = i_{L21} + i_{L22} - i_o \Rightarrow C\frac{dV_C}{dt} = i_{L21} + i_{L22} - \frac{V_o}{R}$$

c) *For the interval $0.5T_{sw}$ <t< $(0.5+D_2)\,T_{sw}$ when the second converter's switch(T_2) conducts and the first converter switch (T_1) is off.*

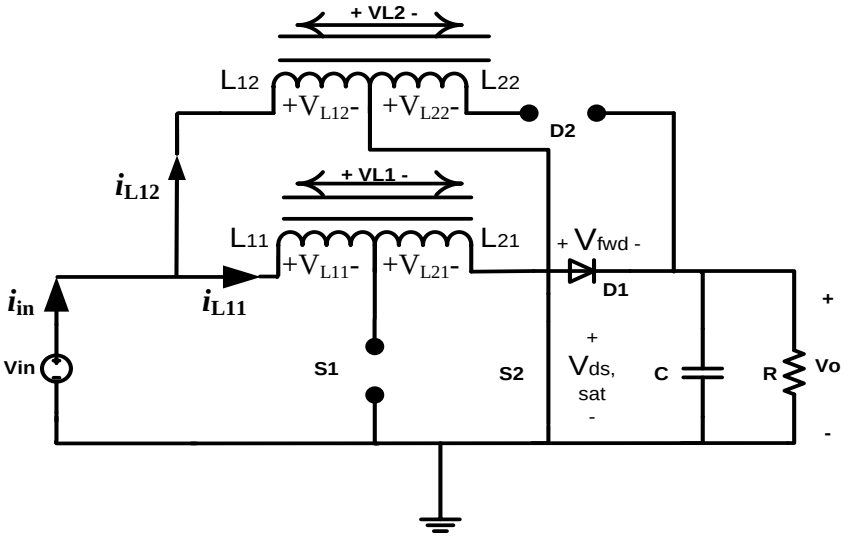


Figure 4.4. The proposed converter during the third switching interval.

During this interval, diode D_2 is reverse biased while diode D_1 is forward biased as shown in Figure 4.4. The current i_{L11} flows through inductors L_{11} and L_{21}. Current i_{L12} flows through inductor L_{12} but not through L_{22}. The following expressions are hence applicable,

$$V_{in} = V_{L1} + V_O \Rightarrow V_{L1} = L_1 \frac{di_{L11}}{dt} = V_{in} - V_o$$

$$V_{in} = V_{L12} = \frac{V_{L2}}{1+nk} \Rightarrow V_{L2} = L_2 \frac{di_{L12}}{dt} = (1+nk)V_{in}$$

$$i_{D1} = i_{L21} = i_{L11}$$

$$i_{s1} = i_{D2} = i_{L22} = 0$$

$$i_{s2} = i_{L22}\,(1+nk) \qquad (4\text{-}9)$$

$$i_{in} = i_{L11} + i_{L22}(1+nk)$$

$$i_C = i_{L21} - i_o \Rightarrow C\frac{dV_C}{dt} = i_{L21} - \frac{V_o}{R}$$

d) For the interval (0.5+ D_2) T_{sw} <t<T_{sw} when none of the switches conduct.

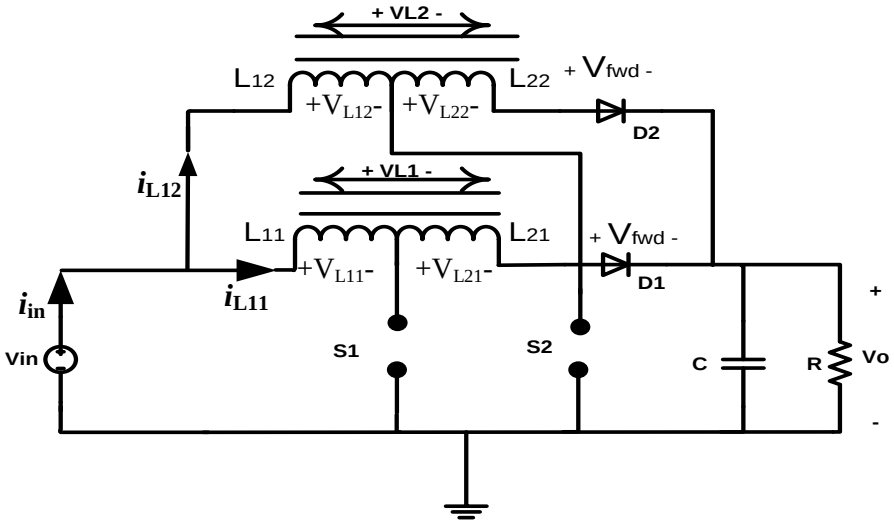


Figure 4.5. The proposed converter during the fourth switching interval.

During this interval, none of the active switches conducts and both output diodes are forward biased as shown in Figure 4.5. Current i_{L11} flows through L_{11} and L_{21} while current i_{L12} flows through inductors L_{12} and L_{22}. The following expressions are therefore valid,

$$V_{in} = V_{L1} + V_o \Rightarrow V_{L1} = L_1 \frac{di_{L11}}{dt} = V_{in} - V_o$$

$$V_{in} = V_{L2} + V_o \Rightarrow V_{L2} = L_2 \frac{di_{L12}}{dt} = V_{in} - V_o$$

$$i_{in} = i_{L11} + i_{L12} \tag{4-10}$$

$$i_{s1} = i_{s2} = 0$$

$$i_{D1} = i_{L11} = i_{L21}$$

$$i_C = i_{L21} + i_{L22} - i_o \Rightarrow C \frac{dV_C}{dt} = i_{L21} + i_{L22} - \frac{V_o}{R}$$

The differential equations applicable to the four time intervals were then averaged using duty ratio as a weight. This was in order to obtain one set of differential equations that is applicable over one switching period. For the interleaved converter under consideration,

duty ratios D_1 and D_2 are complementary to each other. An expression for inductor voltage over a switching period is,

$$\langle L_1 \frac{di_{L11}}{dt} \rangle = (1+nk)V_{in}D_1 + (V_{in}-V_o)(0.5-D_1) + (V_{in}-V_o)D_2 + (V_{in}-V_o)(0.5-D_2)$$

$$\therefore \langle L_1 \frac{di_{L11}}{dt} \rangle = D_1(V_o + nkV_{in}) + (V_{in}-V_o) \quad (4\text{-}11)$$

$$\langle L_2 \frac{di_{L12}}{dt} \rangle = (V_{in}-V_o)D_1 + (V_{in}-V_o)(0.5-D_1) + (1+nk)V_{in}D_2 + (V_{in}-V_o)(0.5-D_2)$$

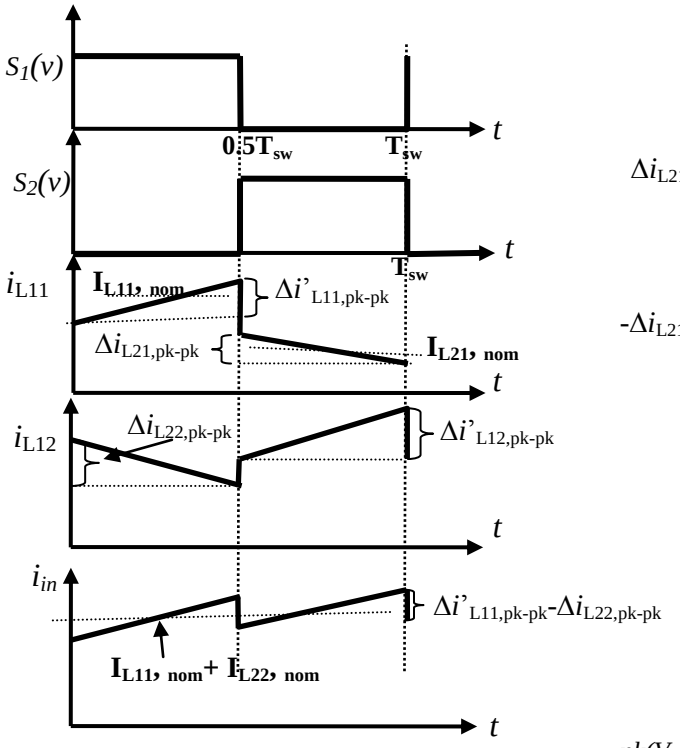
$$\therefore \langle L_2 \frac{di_{L12}}{dt} \rangle = D_2(V_o + nkV_{in}) + (V_{in}-V_o) \quad (4\text{-}12)$$

Additionally, an expression for capacitor current over a switching period is,

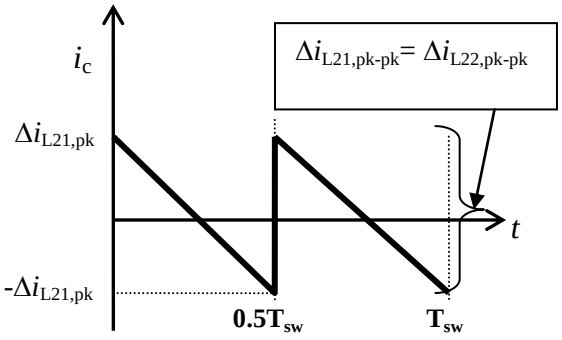
$$\langle C\frac{dV_C}{dt} \rangle = \left(i_{L12} - \frac{V_o}{R}\right)D_1 + \left(i_{L11} + i_{L2} - \frac{V_o}{R}\right)(0.5-D_1) + \left(i_{L11} - \frac{V_o}{R}\right)D_2 + \left(i_{L11} + i_{L12} - \frac{V_o}{R}\right)(0.5-D_2)$$

$$\therefore \langle C\frac{dV_C}{dt} \rangle = i_{L11}(1-D_1) + i_{L12}(1-D_2) - \frac{V_o}{R} \quad (4\text{-}13)$$

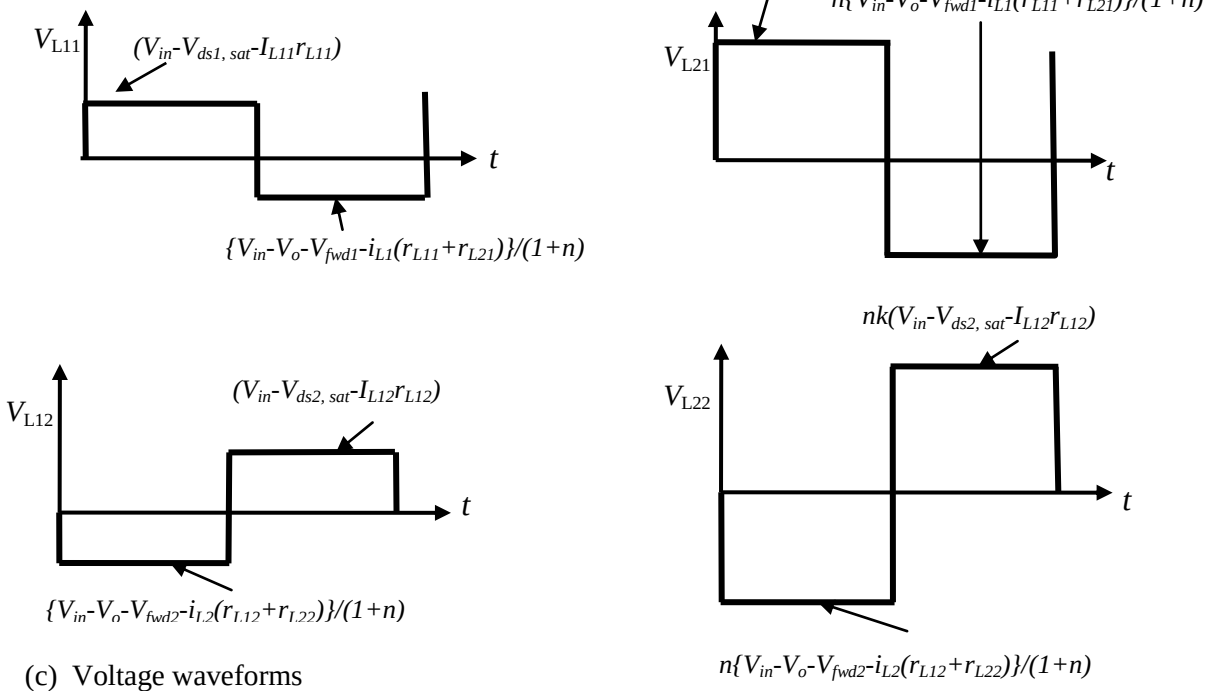
Figure 4.6 shows the switching signals for the two MOSFETs' S_1 and S_2, phase currents i_{L11} and i_{L12}, input current, i_{in}, capacitor current, $i_{c,}$ and inductor voltage waveforms in a two-phase interleaved tapped-coupled-inductor boost converter at a duty ratio of 0.5. The phase currents are overlapped due to the complementary switching signals S_1 and S_2 leading to a reduction in the input current ripple. As seen in Figure 4.6, complete input current ripple cancellation cannot be achieved in the tapped-coupled-inductor boost converter due to the different gradients of the phase currents. However, minimum ripple in a two-phase converter can be achieved at a duty ratio≈0.5 as shown in Figure 4.6. For this converter topology, complete ripple cancellation would require infinitely large inductors which is not practical.



(a) Phase and input current



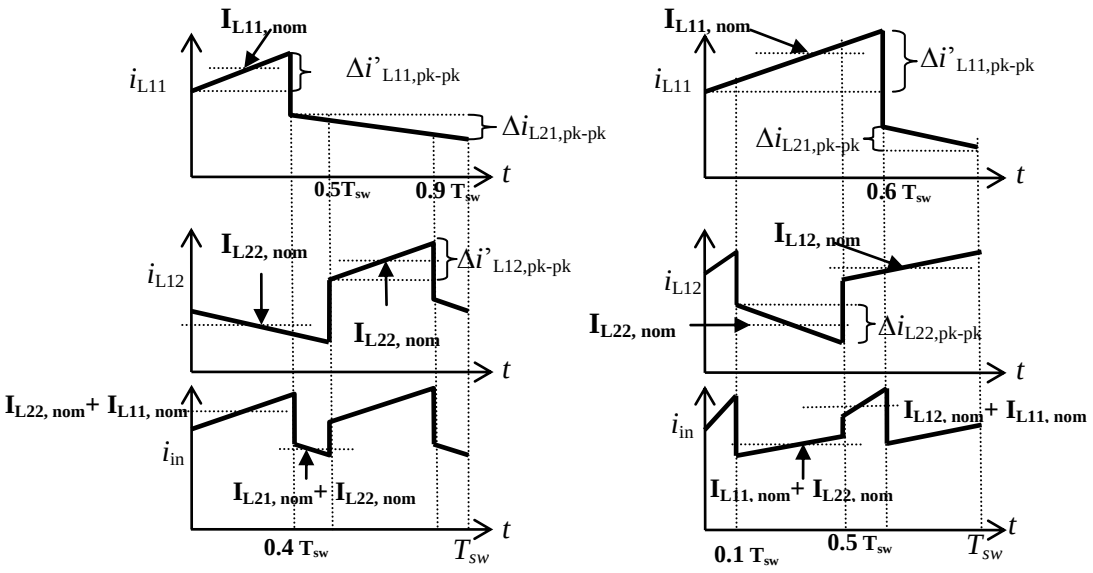
(b) Capacitor current



(c) Voltage waveforms

Figure 4.6. Input, capacitor and inductor current and voltage across the tapped-coupled inductors in a two-phase boost converter at a duty ratio of 0.5

For comparison purposes, phase and input current waveforms at a duty ratio below and above 0.5 in a two-phase converter are shown in Figure 4.7. Figure 4.8 on the other hand shows waveforms for currents through inductors L_{21} and L_{22}, output current and the capacitor current in a two-phase tapped-coupled-inductor boost converter at a duty ratio of 0.4 and 0.6. Figure 4.8 shows how ripple is cancelled at the output of this boost converter. Figures 4.6 to 4.8 show how current sharing in both the input-and-output-side depends on duty ratio.



(a) *D=0.4* (b) *D=0.6*

Figure 4.7. Input and inductor current waveforms in a two-phase boost converter at a duty ratio (a) below and (b) above 0.5.

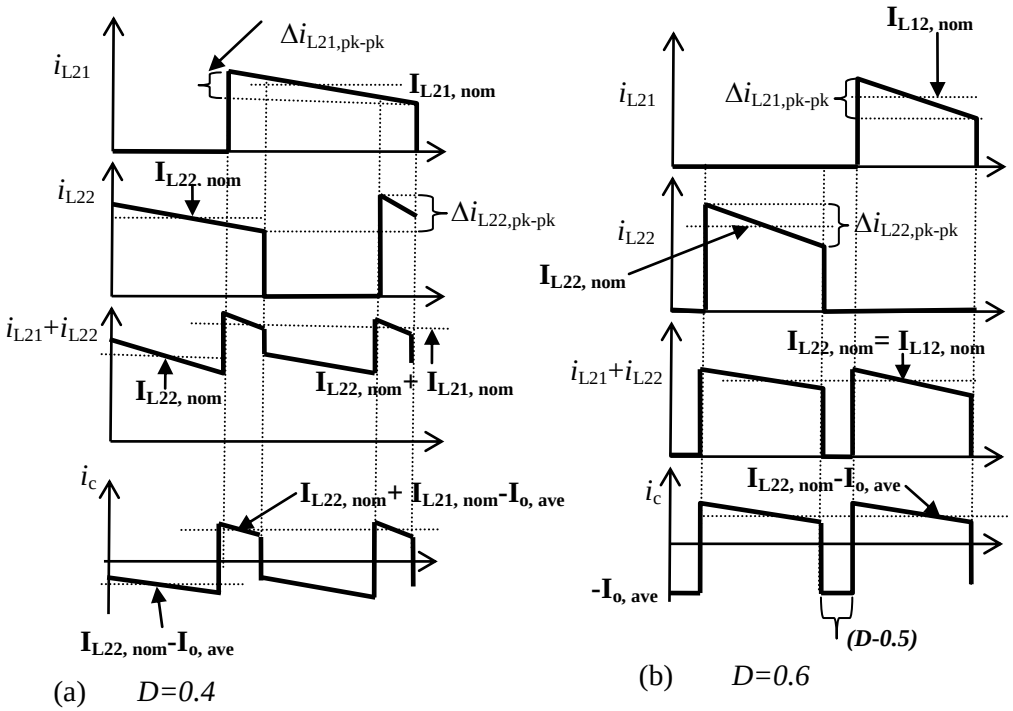


Figure 4.8. Output side inductor and capacitor current waveforms in a two-phase tapped-coupled-inductor at a duty ratio (a) below and (b) above 0.5.

4.2.2 Derivation of analytical expressions for average, RMS and ripple input current, and output capacitor RMS current.

In this section, expressions for input average and RMS current and capacitor RMS current in a two-phase converter are derived. With these expressions input-and-output-side performance characteristics of this converter can be determined. With reference to figures 4.6 to 4.8, the various expressions are derived.

For a two-phase converter, an expression for average output power could be obtained in terms of inductor winding currents as follows,

$$I_{o,ave} = \frac{P_o}{V_{o,ave}} = I_{L21,ave} + I_{L22,ave} = 2I_{L21,ave} = 2I_{L22,ave} = I_{D1} + I_{D2} \quad (4\text{-}14)$$

$$I_{o,ave} = I_{L21,ave} + I_{L22,ave} = I_{L21,nom}(1-D) + I_{L22,nom}(1-D) \quad (4\text{-}15)$$

$$I_{L21,nom} = I_{L22,nom} = \frac{I_{o,ave}}{2(1-D)} = \frac{I_{L21,ave}}{2(1-D)} = \frac{I_{L22,ave}}{2(1-D)} \quad (4\text{-}16)$$

If losses are assumed to be negligible, $P_{in} = P_o$, therefore, $V_{o,ave}I_{o,ave} = V_{in,ave}I_{in,ave}$,

An expression for average phase inductor current is obtained in terms of output-side inductor nominal current as,

$$I_{L11,ave} = \frac{1+nkD}{(1-D)} I_{L21,ave} = I_{L21,nom}(1 + nkD) \quad (4\text{-}17)$$

$$V_{in,ave} = \frac{V_{o,ave}I_{L21,ave}}{I_{L11,ave}} = \frac{V_{o,ave}(1-D)}{1+nkD} \quad (4\text{-}18)$$

An expression for average phase inductor current is obtained in terms of output-side inductor average current as,

$$I_{L11,ave} = I_{L11,nom}D + I_{L21,nom}(1-D) = \frac{1+nkD}{(1-D)} I_{L21,ave} = I_{L21,nom}(1 + nkD) \quad (4\text{-}19)$$

An expression for nominal phase inductor current is obtained in terms of output average current as,

$$I_{L11,nom} = I_{L12,nom} = I_{L21,nom}(1 + nk) = I_{L22,nom}(1 + nk) = \frac{I_{o,ave}(1+nk)}{2(1-D)} \quad (4\text{-}20)$$

Input and output-side phase current peak-to-peak ripple is expressed as,

$$\Delta i'_{L11,pk-pk} = \frac{(V_{in} - i_{L11}r_{ds,on} - i_{L11}r_{L11})DT_{sw}}{L_{11}} \quad (4\text{-}21)$$

$$\Delta i_{L21,pk-pk} = \frac{n\left(V_{in} - V_o - V_{fwd} - i_{L21}(r_{L11} + r_{L21})\right)(1-D)T_{sw}}{(n+1)L_{21}} \quad (4\text{-}22)$$

An expression for phase RMS current is then obtained as,

$$I_{L11,rms} = \sqrt{\left\{\left(I_{L11,nom}\right)^2 D\left[1+\frac{1}{3}\left(\frac{\Delta i'_{L11,pk-pk}}{2I_{L11,nom}}\right)^2\right]+\left(I_{L21,nom}\right)^2(1-D)\left[1+\frac{1}{3}\left(\frac{\Delta i_{L21,pk-pk}}{2I_{L21,nom}}\right)^2\right]\right\}} \quad (4\text{-}23)$$

Substituting equation (4-20) into (4-23), expressions for the phase RMS currents are obtained as,

$$I_{L11,rms} = I_{L21,nom}\sqrt{\left\{(1+nk)^2 D\left[1+\frac{1}{3}\left(\frac{\Delta i'_{L11,pk-pk}}{2I_{L21,nom}(1+nk)}\right)^2\right]+(1-D)\left[1+\frac{1}{3}\left(\frac{\Delta i_{L21,pk-pk}}{2I_{L21,nom}}\right)^2\right]\right\}} \quad (4\text{-}24a)$$

$$I_{L12,rms} = I_{L22,nom}\sqrt{\left\{(1+nk)^2 D\left[1+\frac{1}{3}\left(\frac{\Delta i'_{L12,pk-pk}}{2I_{L22,nom}(1+nk)}\right)^2\right]+(1-D)\left[1+\frac{1}{3}\left(\frac{\Delta i_{L22,pk-pk}}{2I_{L22,nom}}\right)^2\right]\right\}} \quad (4\text{-}24b)$$

Where, $I_{L21,nom} = I_{L22,nom} = \frac{I_{o,ave}}{2(1-D)}$

The peak values of the phase currents are obtained as,

$$i_{L11,peak} = i_{L12,peak} = I_{L11,nom} + \frac{1}{2}\Delta i'_{L11,pk-pk} \quad (4\text{-}25a)$$

$$i_{21,peak} = i_{22,peak} = I_{L21,nom} + \frac{1}{2}\Delta i'_{L21,pk-pk} \quad (4\text{-}25b)$$

From figures 4.6 to 4.8, expressions for input and capacitor current are,

$$i_{in} = i_{L11} + i_{L12} \quad (4\text{-}26)$$

$$i_c = i_{L21} + i_{L22} - I_{o,ave} \quad (4\text{-}27)$$

Referring to Figures 4.6 to 4.8 and summing the phase currents i_{L11} and i_{L12} waveforms and neglecting current variations due to $\Delta i'_{L11,pk-pk}$, $\Delta i'_{L12,pk-pk,}$ $\Delta i_{L22,pk-pk}$ and $\Delta i_{L21,pk-pk}$ the following expressions for average and RMS input current are obtained,

For D < 0.5,

$$I_{in,ave} = \frac{I_{o,ave}(2+nk)D}{(1-D)} + 2(0.5-D)\frac{I_{o,ave}}{(1-D)} \tag{4-28}$$

$$I_{in,rms} \approx \sqrt{2D\left(\frac{I_{o,ave}(2+nk)}{2(1-D)}\right)^2 + 2(0.5-D)\left(\frac{I_{o,ave}}{(1-D)}\right)^2} \tag{4-29}$$

For D = 0.5, expressions for average and RMS input current are,

$$I_{in,ave} = \frac{I_{o,ave}(2+nk)}{2(1-D)} = I_{o,ave}(2+nk) \tag{4-30}$$

$$I_{in,rms} \approx \sqrt{2D\left(\frac{I_{o,ave}(2+nk)}{2(1-D)}\right)^2} = I_{o,ave}(2+nk) \tag{4-31}$$

Similarly, for D > 0.5,

$$I_{in,ave} = 2(D-0.5)\left(\frac{I_{o,ave}(1+nk)}{(1-D)}\right) + I_{o,ave}(2+nk) \tag{4-32}$$

$$I_{in,rms} \approx \sqrt{2(D-0.5)\left(\frac{I_{o,ave}(1+nk)}{(1-D)}\right)^2 + 2(1-D)\left(\frac{I_{o,ave}(2+nk)}{2(1-D)}\right)^2} \tag{4-33}$$

From equations (4-28) to (4-33), it is seen that the average and RMS input current is dependent on turns ratio, coupling coefficient, duty ratio and load current and tends to infinity as duty ratio approaches to unity. For a given duty ratio, a high value of turns ratio and coupling coefficient results to a high value of input average and RMS currents.

Referring to equations (4-28) to (4-33), input current RMS ripple can then be obtained as,

For D < 0.5,

$$I_{in,ripple,rms} \approx \sqrt{2D\left(\frac{I_{o,ave}(2+nk)}{2(1-D)}\right)^2 + 2(0.5-D)\left(\frac{I_{o,ave}}{(1-D)}\right)^2 - \left(\frac{I_{o,ave}(2+nk)D+2(0.5-D)I_{o,ave}}{(1-D)}\right)^2} \tag{4-34a}$$

Similarly, for D > 0.5,

$$I_{in,rms,ripple} \approx \sqrt{2(D-0.5)\left(\frac{I_{o,ave}(1+nk)}{(1-D)}\right)^2 + 2(1-D)\left(\frac{I_{o,ave}(2+nk)}{2(1-D)}\right)^2 - \left(\frac{2(D-0.5)I_{o,ave}(1+nk)+I_{o,ave}(1-D)(2+nk)}{(1-D)}\right)^2}$$

(4-34b)

For the ideal expressions derived, the input current RMS ripple is zero at a duty ratio of 0.5. Summing the phase currents i_{L21} and i_{L22} then subtracting the average output current as shown in equation (4-27) and neglecting current variations due to $\Delta i'_{L11,pk-pk}$, $\Delta i'_{L12,pk-pk,}$ $\Delta i_{L22,pk-pk}$ and $\Delta i_{L21,pk-pk}$ the output capacitor RMS current for a two-phase converter are obtained as,

For D < 0.5,

$$I_{c,rms} \approx \sqrt{2D\left(\frac{I_{o,ave}(2D-1)}{2(1-D)}\right)^2 + 2(0.5-D)\left(\frac{DI_{o,ave}}{(1-D)}\right)^2} \quad (4\text{-}35)$$

For D > 0.5,

$$I_{c,rms} \approx \sqrt{\left(I_{o,ave}\right)^2(D-0.5) + 2(1-D)\left(\frac{I_{o,ave}(2D-1)}{2(1-D)}\right)^2} \quad (4\text{-}36)$$

Ideally, the capacitor RMS current at a duty ratio of 0.5 is zero. It is seen from equation (4-35) and (4-36) that capacitor RMS current depends on duty ratio and load current. For a fixed load current, an increase in the duty ratio will lead to a non-linear increase in the capacitor RMS current.

4.3 MODELLING OF A TWO-PHASE INTERLEAVED TAPPED-COUPLED-INDUCTOR BOOST CONVERTER

In order to determine the dynamic response of the proposed converter as well as design compensators for closed-loop control purposes, it is necessary to obtain a small signal

model of the converter. The technique of circuit averaging has been used in this thesis to obtain transfer functions that describe the converter during the switching intervals.

The non-linear differential equations (4-11), (4-12) and (4-13) are linearized so as to separate the various parameters and variables into DC and AC components. The following small-signal expressions are then obtained from equations (4-11), (4-12) and (4-13).

$$L_1\frac{d\tilde{\imath}_{\mathrm{L}11}(t)}{dt}=\left\{\left(D_1+\tilde{d}_1(t)\right)\left[V_O+\tilde{v}_o(t)+nk\left(V_{in}+\tilde{v}_{in}(t)\right)\right]\right\}+\left[V_{in}+\tilde{v}_{in}(t)-V_O-\tilde{v}_o(t)\right] \tag{4-37}$$

$$L_2\frac{d\tilde{\imath}_{\mathrm{L}12}(t)}{dt}=\left\{\left(D_2+\tilde{d}_2(t)\right)\left[V_O+\tilde{v}_o(t)+nk\left(V_{in}+\tilde{v}_{in}(t)\right)\right]\right\}+\left[V_{in}+\tilde{v}_{in}(t)-V_O-\tilde{v}_o(t)\right] \tag{4-38}$$

$$C\frac{d\tilde{V}_c(t)}{dt}=\left(I_{\mathrm{L}11}+\tilde{\imath}_{\mathrm{L}11}(t)\right)\left(1-D_1-\tilde{d}_2(t)\right)+\left(I_{\mathrm{L}12}+\tilde{\imath}_{\mathrm{L}12}(t)\right)\left(1-D_2-\tilde{d}_2(t)\right)-\frac{V_O}{R}-\frac{\tilde{v}_o(t)}{R} \tag{4-39}$$

From equations (4-37), (4-38) and (4-39), the DC terms are obtained as,

$$0=D_1(V_O+nkV_{in})+(V_{in}-V_O)\Rightarrow V_O=V_{in}\frac{(1+nkD_1)}{1-D_1} \tag{4-40}$$

$$0=D_2(V_O+nkV_{in})+(V_{in}-V_O)\Rightarrow V_O=V_{in}\frac{(1+nkD_2)}{1-D_2} \tag{4-41}$$

$$0=I_{\mathrm{L}11}(1-D_1)+I_{\mathrm{L}12}(1-D_2)-\frac{V_O}{R}\Rightarrow\frac{V_O}{R}=I_{\mathrm{L}11}(1-D_1)+I_{\mathrm{L}12}(1-D_2) \tag{4-42}$$

The AC terms are obtained as,

$$L_1\frac{d\tilde{\imath}_{\mathrm{L}11}(t)}{dt}=D_1[\tilde{v}_o(t)+nk\tilde{v}_{in}(t)]+\tilde{d}_2(t)[V_O+nkV_{in}]+[\tilde{v}_{in}(t)-\tilde{v}_o(t)] \tag{4-43}$$

$$L_2\frac{d\tilde{\imath}_{\mathrm{L}12}(t)}{dt}=D_2[\tilde{v}_o(t)+nk\tilde{v}_{in}(t)]+\tilde{d}_2(t)[V_O+nkV_{in}]+[\tilde{v}_{in}(t)-\tilde{v}_o(t)] \tag{4-44}$$

$$C\frac{d\tilde{V}_c(t)}{dt}=(1-D_1)\tilde{\imath}_{\mathrm{L}11}(t)-\tilde{d}_2(t)I_{\mathrm{L}11}+(1-D_2)\tilde{\imath}_{\mathrm{L}12}(t)-\tilde{d}_2(t)I_{\mathrm{L}12}-\frac{\tilde{v}_o(t)}{R} \tag{4-45}$$

In s-domain, the AC terms are obtained from equations (4-43) to (4-45) as:

$$sL_1\tilde{\imath}_{\mathrm{L}11}(s) = D_1[\tilde{v}_o(s) + nk\tilde{v}_{in}(s)] + \tilde{d}_1(s)[V_O + nkV_{in}] + [\tilde{v}_{in}(s) - \tilde{v}_o(s)] \quad (4\text{-}46)$$

$$sL_2\tilde{\imath}_{\mathrm{L}12}(s) = D_2[\tilde{v}_o(s) + nk\tilde{v}_{in}(s)] + \tilde{d}_2(s)[V_O + nkV_{in}] + [\tilde{v}_{in}(s) - \tilde{v}_o(s)] \quad (4\text{-}47)$$

$$sC\tilde{V}_o(s) = (1 - D_1)\tilde{\imath}_{\mathrm{L}11}(s) - \tilde{d}_1(s)I_{\mathrm{L}11} + (1 - D_2)\tilde{\imath}_{\mathrm{L}12}(s) - \tilde{d}_2(s)I_{\mathrm{L}12} - \frac{\tilde{v}_o(s)}{R} \quad (4\text{-}48)$$

The s-domain equations (4-46) to (4-48) can be rearranged to yield,

$$sL_1\tilde{\imath}_{\mathrm{L}11}(s) = (nkD_1 + 1)\tilde{v}_{in}(s) + \tilde{d}_1(s)[V_O + nkV_{in}] - \tilde{v}_o(s)[1 - D_1] \quad (4\text{-}49)$$

$$sL_2\tilde{\imath}_{\mathrm{L}12}(s) = (nkD_2 + 1)\tilde{v}_{in}(s) + \tilde{d}_2(s)[V_O + nkV_{in}] - \tilde{v}_o(s)[1 - D_2] \quad (4\text{-}50)$$

$$\tilde{v}_o(s)\left[\frac{sCR+1}{R}\right] = (1 - D_1)\tilde{\imath}_{\mathrm{L}11}(s) - \tilde{d}_1(s)I_{\mathrm{L}11} + (1 - D_2)\tilde{\imath}_{\mathrm{L}12}(s) - \tilde{d}_2(s)I_{\mathrm{L}12} \quad (4\text{-}51)$$

An s-domain expression for converter 1 inductor current is obtained with reference to equation (4-51) as,

$$\tilde{\imath}_{\mathrm{L}11}(s) = \left[\frac{sCR+1}{R(1-D_1)}\right]\tilde{v}_o(s) + \tilde{d}_1(s)\frac{I_{\mathrm{L}11}}{(1-D_1)} - \tilde{\imath}_{\mathrm{L}12}(s)\frac{(1-D_2)}{(1-D_1)} + \tilde{d}_2(s)\frac{I_{\mathrm{L}12}}{(1-D_1)} \quad (4\text{-}52)$$

Substituting, equation (4-52) into equation (4-49), the following expression is obtained:

$$sL_1\left[\frac{sCR+1}{R(1-D_1)}\right]\tilde{v}_o(s) + \tilde{d}_1(s)\frac{I_{L1}}{(1-D_1)} - \tilde{\imath}_{\mathrm{L}12}(s)\frac{(1-D_2)}{(1-D_1)} + \tilde{d}_2(s)\frac{I_{\mathrm{L}12}}{(1-D_1)} =$$

$$(nkD_1 + 1)\tilde{v}_{in}(s) + \tilde{d}_1(s)(V_O + nkV_{in}) \quad (4\text{-}53)$$

Equation (4-53) is rearranged to yield,

$$\{s^2L_1CR + sL_1 + R(1 - D_1)^2\}\tilde{v}_o(s) = \{(nkD_1 + 1)(1 - D_1)R\}\tilde{v}_{in}(s)$$

$$+\{(V_O + nkV_{in})(1 - D_1)R - sL_1RI_{\mathrm{L}11}\}\tilde{d}_1(s)$$

$$+\{(1 - D_2)sL_1R\}\tilde{\imath}_{\mathrm{L}12}(s) - \{sL_1I_{\mathrm{L}12}R\}\tilde{d}_2(s) \quad (4\text{-}54)$$

From equation (4-54), the control-to-output transfer-function of the first converter is obtained as:

$$G_{v_o d_1} = \frac{\tilde{v}_o(s)}{\tilde{d}_1(s)} \Big|_{\tilde{v}_{in}(s)=\tilde{i}_{L12}(s)=\tilde{d}_2(s)=0} = \frac{\{(V_O + nkV_{in})(1-D_1)R - sL_1 R I_{L11}\}}{\{s^2 L_1 CR + sL_1 + R(1-D_1)^2\}} \tag{4-55}$$

The control-to-output transfer-function of the second converter is obtained as:

$$G_{v_o d_2} = \frac{\tilde{v}_o(s)}{\tilde{d}_2(s)} \Big|_{\tilde{v}_{in}(s)=\tilde{d}_1(s)=\tilde{\imath}_{L12}(s)=0} = \frac{\{(V_O + nkV_{in})(1-D_2)R - sL_2 R I_{L12}\}}{\{s^2 L_2 CR + sL_2 + R(1-D_2)^2\}} \tag{4-56}$$

The control-to-output transfer functions in (4-55) and (4-56) provides information on how the first converter control input variations $\tilde{d}_1(s)$ and the second converter control input variations $\tilde{d}_2(s)$ influences the output voltage $\tilde{v}_o(s)$ respectively. In these two equations, $\tilde{v}_o$ and $\tilde{d}_1$ are small perturbations in the output voltage and duty ratio respectively. Regulation of the DC output voltage of the proposed converter depends on the response of these transfer functions relating the output voltage to control. These transfer functions are a key component of the loop gain and have a significant effect on the converter performance.

Unlike in a conventional boost converter, there is presence of the turns ratio, input voltage and the coupling coefficient in these transfer functions in equation (4-55) and (4-56). These parameters increase the DC gain of the transfer functions. This is desirable at low frequencies as it limits the controller gain to low values [21], [43]. However, just as in the conventional boost converter, these transfer functions have a right half-plane zero (RHP). The converter small-signal transfer-function relating input voltage to output voltage is obtained as:

$$G_{v_o v_{in}} = \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} \Big|_{\tilde{d}_1(s)=\tilde{d}_2(s)=\tilde{\imath}_{L12}(s)=0} = \frac{\{(nkD_1 + 1)(1-D_1)R\}}{\{s^2 L_1 CR + sL_1 + R(1-D_1)^2\}} \tag{4-57}$$

The line-to-output function in (4-57) describes how variations in the converter input voltage $\tilde{v}_{in}(t)$ lead to variations in the output voltage $\tilde{v}_{out}(t)$.

Compared to the line-to-output function of a conventional boost converter, this transfer-function has a higher value of DC gain due to effects of turns ratio, *n*, coupling coefficient, *k* and the duty ratio, *D*. A very high turns ratio will result to a high magnitude of this transfer-function hence a small disturbance in the input voltage will lead to a larger disturbance in the output voltage which is not desirable. A trade-off between the boost ratio and converter control response should hence be made during selection of the turns ratio.

Transfer function relating inductor current of second converter to output is obtained as:

$$G_{v_o i_{L2}} = \frac{\tilde{v}_o(s)}{\tilde{\imath}_{\mathrm{L12}}(s)}\Big|_{\tilde{d}_1(s)=\tilde{d}_2(s)=\tilde{v}_{in}(s)=0} = \frac{\{(1-D_2)sL_1R\}}{\{s^2L_1CR + sL_1 + R(1-D_1)^2\}} \tag{4-58}$$

From equation (4-51), the following expression is obtained,

$$\tilde{v}_o(s) = \{(1-D_1)\tilde{\imath}_{\mathrm{L11}}(s) - \tilde{d}_1(s)I_{\mathrm{L11}} + (1-D_2)\tilde{\imath}_{\mathrm{L12}}(s) - \tilde{d}_2(s)I_{\mathrm{L12}}\}\left[\frac{R}{sCR+1}\right] \tag{4-59}$$

Substituting for output voltage (4-59) in the inductor dynamics equations (4-49) and (4-50) yields,

$$sL_1\tilde{\imath}_{\mathrm{L11}}(s) = (nkD_1 + 1)\tilde{v}_{in}(s) + \tilde{d}_1(s)[V_O + nkV_{in}] - \{(1-D_1)\tilde{\imath}_{\mathrm{L11}}(s) - \tilde{d}_1(s)I_{\mathrm{L11}} + (1-D_2)\tilde{\imath}_{\mathrm{L12}}(s) - \tilde{d}_2(s)I_{\mathrm{L12}}\}\frac{R[1-D_1]}{sCR+1} \tag{4-60}$$

$$sL_2\tilde{\imath}_{\mathrm{L12}}(s) = (nkD_2 + 1)\tilde{v}_{in}(s) + \tilde{d}_2(s)[V_O + nkV_{in}] - \{(1-D_1)\tilde{\imath}_{\mathrm{L11}}(s) - \tilde{d}_1(s)I_{\mathrm{L11}} + (1-D_2)\tilde{\imath}_{\mathrm{L12}}(s) - \tilde{d}_2(s)I_{\mathrm{L12}}\}\frac{R[1-D_2]}{sCR+1}$$

Rearrange equation (4-60) to get,

$$\begin{aligned}\tilde{\imath}_{\mathrm{L11}}(s)\{s^2CRL_1 + sL_1 + R(1-D_1)^2\} \\ = \tilde{v}_{in}(s)\{(nkD_1+1)(sCR+1)\} \\ + \tilde{d}_1(s)\{(V_O + nkV_{in})(sCR+1) + I_{\mathrm{L11}}R[1-D_1]\} - \tilde{\imath}_{\mathrm{L12}}(s)\{(1-D_2)(1-D_1)\} \\ + \tilde{d}_2(s)\{I_{\mathrm{L12}}R(1-D_1)\}\end{aligned} \tag{4-61}$$

$$\begin{aligned}\tilde{\imath}_{\mathrm{L12}}(s)\{s^2CRL_2 + sL_2 + R(1-D_2)^2\} \\ = \tilde{v}_{in}(s)\{(nkD_2+1)(sCR+1)\} \\ + \tilde{d}_2(s)\{(V_O + nkV_{in})(sCR+1) + I_{\mathrm{L12}}R[1-D_2]\} - \tilde{\imath}_{\mathrm{L11}}(s)\{(1-D_1)(1-D_2)\} \\ + \tilde{d}_1(s)\{I_{\mathrm{L11}}R(1-D_2)\}\end{aligned}$$

From this analysis, the following transfer functions are obtained,

$$G_{i_{\mathrm{L11}}v_{in}} = \frac{\tilde{\imath}_{L11}(s)}{\tilde{v}_{in}(s)}\Big|_{\tilde{d}_1(s)=\tilde{d}_2(s)=\tilde{\imath}_{\mathrm{L12}}(s)=0} = \frac{(nkD_1+1)(sCR+1)}{s^2CRL_1 + sL_1 + R(1-D_1)^2} \tag{4-62}$$

Equation (4-62) can be used to determine how variations in the input voltage affect the first tapped-coupled-inductor current.

$$\begin{aligned}G_{i_{\mathrm{L11}}d_1} &= \frac{\tilde{\imath}_{\mathrm{L11}}(s)}{\tilde{d}_1(s)}\Big|_{\tilde{v}_{in}(s)=\tilde{d}_2(s)=\tilde{\imath}_{\mathrm{L12}}(s)=0} \\ &= \frac{(V_O + nkV_{in})(sCR+1) + I_{\mathrm{L11}}R(1-D_1)}{s^2CRL_1 + sL_1 + R(1-D_1)^2}\end{aligned} \tag{4-63}$$

Equation (4-63) can be used to determine how variations in the first interleaved converter duty ratio affect the first tapped-coupled-inductor current.

$$G_{i_{\mathrm{L11}}d_2} = \frac{\tilde{\imath}_{\mathrm{L11}}(s)}{\tilde{d}_2(s)}\Big|_{\tilde{v}_{in}(s)=\tilde{d}_1(s)=\tilde{\imath}_{\mathrm{L12}}(s)=0} = \frac{I_{\mathrm{L12}}R(1-D_1)}{s^2CRL_1 + sL_1 + R(1-D_1)^2} \tag{4-64}$$

Equation (4-64) can be used to determine how variations in the second interleaved converter duty ratio affect the first tapped-coupled-inductor current. Equation (4-65) describes how disturbances in the second tapped-coupled-inductor current affect the first tapped-coupled-inductor current.

$$G_{i_{\mathrm{L11}}i_{\mathrm{L22}}} = \frac{\tilde{i}_{\mathrm{L11}}(s)}{\tilde{i}_{\mathrm{L12}}(s)}\Big|_{\tilde{v}_{in}(s)=\tilde{d}_1(s)=\tilde{d}_2(s)=0} = \frac{(1-D_2)(1-D_1)}{s^2CRL_1 + sL_1 + R(1-D_1)^2} \tag{4-65}$$

Equation (4-66) to (4-69) can be used to determine how input voltage disturbances, second interleaved converter duty ratio disturbances, first interleaved converter duty ratio disturbances and first tapped-coupled-inductor current disturbances affect the second tapped-coupled-inductor current respectively.

$$G_{i_{\mathrm{L12}}v_{in}} = \frac{\tilde{i}_{\mathrm{L12}}(s)}{\tilde{v}_{in}(s)}\Big|_{\tilde{d}_1(s)=\tilde{d}_2(s)=\tilde{i}_{\mathrm{L11}}(s)=0} = \frac{(nkD_2+1)(sCR+1)}{s^2CRL_2 + sL_2 + R(1-D_2)^2} \tag{4-66}$$

$$G_{i_{\mathrm{L12}}d_2} = \frac{\tilde{i}_{\mathrm{L12}}(s)}{\tilde{d}_2(s)}\Big|_{\tilde{v}_{in}(s)=\tilde{d}_1(s)=\tilde{i}_{\mathrm{L11}}(s)=0} = \frac{(V_O + nkV_{in})(sCR+1) + I_{\mathrm{L12}}R[1-D_2]}{s^2CRL_2 + sL_2 + R(1-D_2)^2} \tag{4-67}$$

$$G_{i_{\mathrm{L12}}d_1} = \frac{\tilde{i}_{\mathrm{L12}}(s)}{\tilde{d}_1(s)}\Big|_{\tilde{v}_{in}(s)=\tilde{d}_2(s)=\tilde{i}_{\mathrm{L11}}(s)=0} = \frac{I_{\mathrm{L11}}R(1-D_2)}{s^2CRL_2 + sL_2 + R(1-D_2)^2} \tag{4-68}$$

$$G_{i_{\mathrm{L12}}i_{\mathrm{L11}}} = \frac{\tilde{i}_{\mathrm{L12}}(s)}{\tilde{i}_{\mathrm{L11}}(s)}\Big|_{\tilde{v}_{in}(s)=\tilde{d}_1(s)=\tilde{d}_2(s)=0} = \frac{-\{(1-D_1)(1-D_2)\}}{s^2CRL_2 + sL_2 + R(1-D_2)^2} \tag{4-69}$$

Bode plots of some of the above derived transfer functions are plotted in chapter 6. From these bode plots, converter parameters such as the DC-gain, gain- margin, phase-margin, quality factor, right half-plane zero and resonant frequency are be obtained. The stability and the dynamic performance of the two-phase tapped-coupled-inductor boost converter are inferred from these parameters. A suitable controller that ensures converter stability under all operating conditions can then designed.

4.4 CHAPTER CONCLUSION

This chapter describes and discusses in detail the proposed multi-phase interleaved tapped-coupled-inductor boost converter which can be used to efficiently boost a PV array voltage. By use of both interleaving and tapped-coupled-inductors, high voltage boost ratios can be achieved. The advantages of this DC-DC converter such as ripple cancellation in both the input and output current and voltage waveforms are explained, which leads to high efficiency.

Through the multi-phase converter loss analysis, current sharing in the phases is also shown to translate to reduced switch losses and voltage drops hence higher efficiencies and voltage boost capabilities compared to the single-phase converter described in chapter 3. Sharing of currents in the phases also results to reduction in peak currents, translating into lower EMI noise generation.

It is also demonstrated that in the proposed interleaved tapped-coupled-inductor boost converter, ripple reduction is a function of phase number, N, and the duty ratio, *D*. Minimum ripple is obtained whenever the duty ratio matches the ratio of the low-side voltage relative to the high-side voltage of the converter. It was shown that the magnetic energy storage requirements for the proposed multi-phase interleaved converter reduce by a factor equal to the phase number. As the number of interleaved phases increase, the physical size of the required inductors is reduced, hence improved transient response of the converter.

Analytical expressions for average and RMS input current as well as capacitor RMS current in a two-phase tapped-coupled-inductor boost converter are derived. These

expressions can be used to determine the input and output performance characteristics of this converter as well as in sizing of components. Input current ripple is shown to depend on duty ratio, output current, turns ratio and the coupling coefficient. The capacitor ripple is shown to depend on duty ratio and the load current.

The working of a multi-phase interleaved tapped-coupled-inductor boost converter was demonstrated by analysing a two-phase tapped-coupled-inductor boost converter. The two-phase converter was then modelled and transfer functions obtained. Just as in the case of a single-phase tapped-coupled-inductor boost converter in chapter 3, these transfer functions differed from a conventional boost converter due to the presence on turns ratio and the coupling coefficient.

CHAPTER 5 SYSTEM DESIGN

In this chapter, the design of a two-phase interleaved tapped-coupled-inductor boost converter to be used in efficient voltage boosting of a PV voltage is explained. The selection of key components such as semiconductor and passive devices is discussed. Sizing and design of the coupled inductors is discussed in detail.

5.1 SYSTEM SPECIFICATIONS

A 1kW prototype of the proposed converter is designed and simulated to confirm the hypothesis of this research. In a PV module or array, the rated maximum power point voltage (V_{mpp}) needed to achieve maximum PV array power is attained at approximately 80% of the rated open-circuit voltage as shown in Figure 5.1. To ensure operation at around the maximum power point at all irradiation levels, the PV array output voltage should vary between 75% -85% of the rated PV array open-circuit voltage. A PV module with a V_{mpp} of 40V was chosen in the design of the converter. To operate around the MPP region, this input voltage into the converter should vary between 37.5V-42.5V. A nominal V_{mpp} of 40V was hence was used in the design of the 1kW prototype.

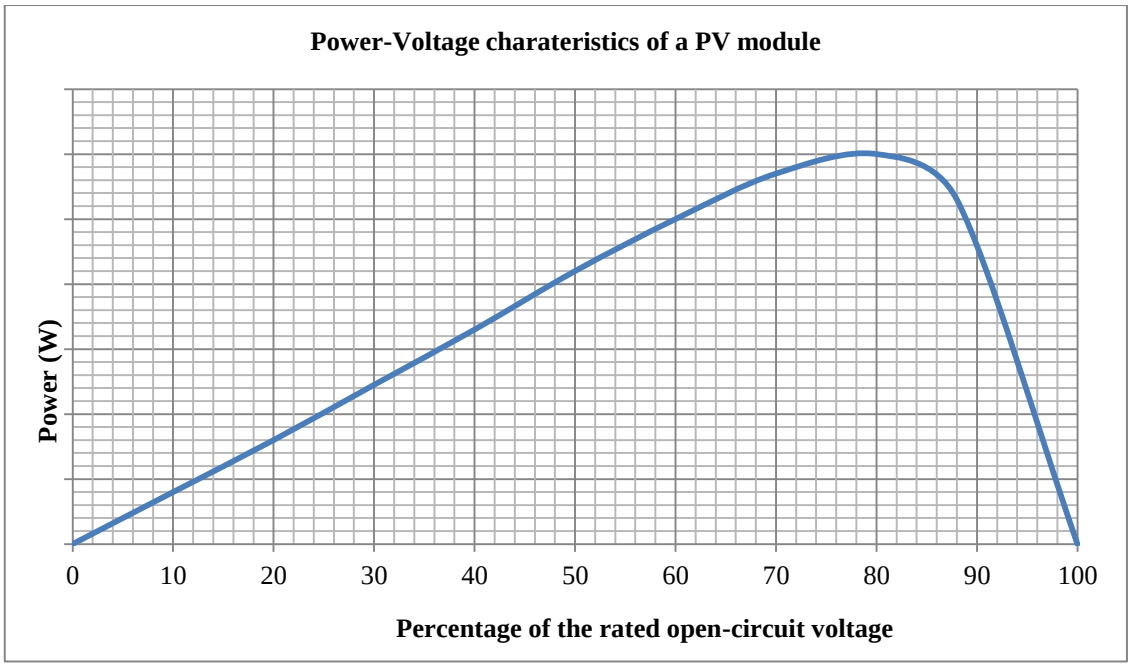


Figure 5.1. Power-Voltage PV characteristics.

The switching and core losses are proportional to the switching frequency, which is inversely proportional to magnetic and capacitor component size. Small inductors and capacitors in converter design result in a fast transient response and a high power density. Striking a balance between the losses and component size a frequency of 100 kHz was selected. The proposed converter is required to boost the input voltage to 400V. To avoid the extreme duty ratio, turns ratio, *n* of 10 was selected. Since a high coupling coefficient, *k* is necessary to achieve a high boost ratio, a value of 0.98 was used in component sizing. Using output voltage equations (4-17) and (4-18) of an ideal two-phase converter, the duty ratio range varies from 0.472 to 0.438 for the given input voltage range. In sizing the converter components, nominal duty ratio was chosen to be 0.5 to take account of the losses and also since it gives minimum ripple in converters with even number of phases.

5.2 COMPONENT SELECTION

The interleaved tapped-coupled boost converter that was designed is shown in figure 5.2.

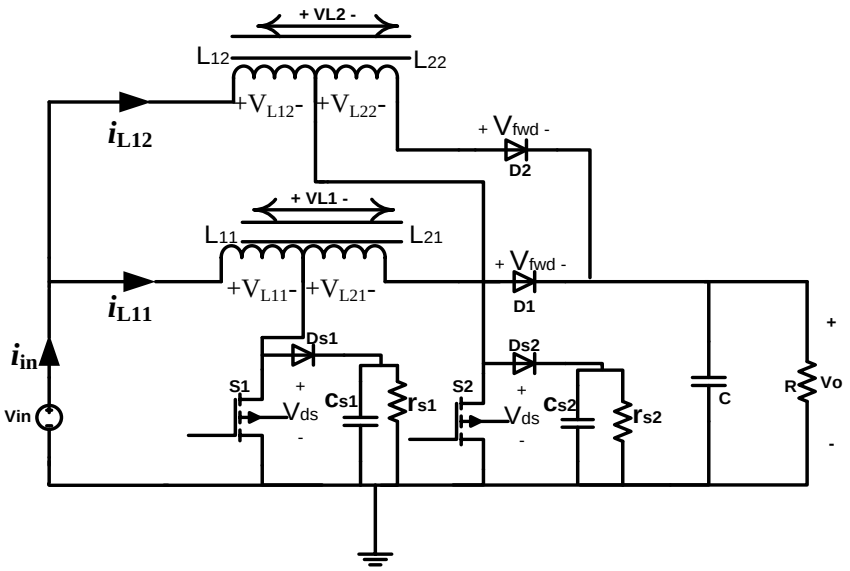


Figure 5.2. Two-phase interleaved tapped-coupled inductor boost converter

The components to be sized include the active switches, the output diodes, the output capacitor the coupled inductors and the snubber circuit consisting on a diode, a capacitor and a resistor. Switches S_1 and S_2 are similar and the diodes D_1 and D_2 are also similar.

The tapped-coupled inductors on each of the converters are also similar. Sizing is therefore done for components on converter 1 which are replicated to the second converter.

5.2.1 Coupled Inductors sizing and design

Sizing of the inductors was done for a single-phase tapped-coupled boost converter and the same values obtained were used in the interleaved converter. The current through the first inductor of each phase is shown in Figure 5.3. The current variation marked ‘a’ occurs when the switch is conducting and depends on the size of the first inductor. Current variation marked ‘b’ is dependent on turns ratio and load while current variation marked ‘c’ occurs when the switch turns off and depends on the size of both coupled inductors in series plus the mutual inductance. For the tapped-coupled-inductor boost converter, therefore, inductor size alone cannot decrease the inductor current ripple substantially due to this nature of the waveform. This is unlike in a conventional boost converter. Sizing of the inductor is hence based on both input current ripple minimisation and conditions for discontinuous inductor current shown in Figure 5.4.

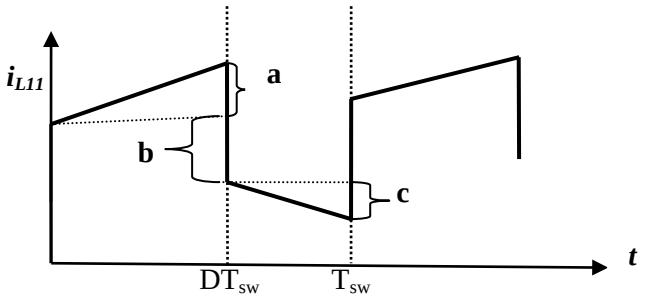


Figure 5.3. Inductor i_{L11} current waveform: continuous conduction mode

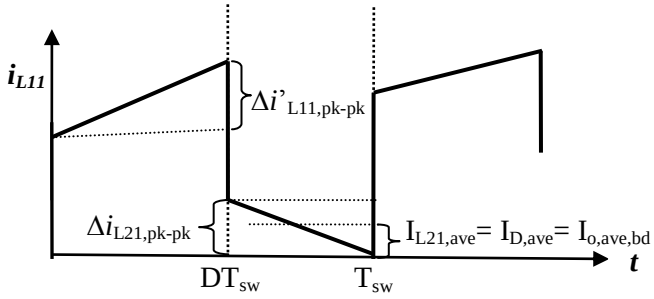


Figure 5.4: Inductor i_{L11} current waveform: boundary of continuous- discontinuous conduction.

As shown in Figure 5.4, when operating at the boundary between continuous and discontinuous conduction, the tapped-coupled-inductor boost converter average output current is equal to half the peak-to-peak current variation denoted as 'c'. For an operating condition with a given set of values of: T_{sw}, V_{in}, V_o, L, n and D, if the average output current becomes less than 0.5c, then the inductor current becomes discontinuous. The inductors are thus sized to ensure that inductor current never becomes discontinuous for as long as output power is greater than a predetermined value.

$$I_{o,ave,bd} = \frac{1}{2}\Delta i_{L21,pk-pk} = \frac{1}{2}\left[\frac{n(V_{in}-V_o)(1-D)T_{sw}}{(1+n)L_{21}}\right] \quad (5\text{-}1)$$

For V_{in}= 40V, V_o= 400V, n=10, D = 0.5, f_{sw} = 100kHz and P_o= 1 kW,

$$I_{o,ave,bd} = \left[\frac{8.812\times10^{-4}}{L_2}\right] \quad (5\text{-}2)$$

Selecting a current variation, $\Delta i_{L21,pk\text{-}pk}$, of 15% of $I_{o,ave}$, ensures continuous conduction mode as long as load is greater than 7.5% of rated value.

$$\Delta i_{L21,pk-pk} = 15\% \times 2.5\text{A} = 0.375\text{A} \approx 0.4\text{ A} \quad (5\text{-}3)$$

$$I_{o,ave,bd} = \left[\frac{0.4}{2}\right] = 0.2\text{A} \quad (5\text{-}4)$$

Output power at the boundary is $0.2\text{A} \times 400\text{V} = 80\text{W}$. Working below this power level will lead to a discontinuous inductor current.

$$L_2 = \left[\frac{8.812\times10^{-4}}{0.2}\right] \approx 4m\text{H} \quad (5\text{-}5)$$

$$\frac{L_{21}}{L_{11}} = \left(\frac{N2}{N1}\right)^2 = n^2 \quad (5\text{-}6)$$

For n =10, $L_{11}=\frac{4m\text{H}}{10^2} = 40\mu\text{H}$

Mutual inductance, $M=k \times \sqrt{L_{11} \times L_{21}}$, where k is the coupling coefficient.

For k = 0.98, M = 392μH

Designing the DC-coupled-inductor.

A design procedure similar to that in [21] was adopted in designing the inductors.

Step 1: Design inputs

L_{11}=40µH, L_{21}=4mH.

Using equations (4-24), (4-19), (4-25a) and (4-25b) the inductor current values are obtained as,

$\hat{I}_{L11}$=30.88A, $I_{L11,av}$ =17.04A, $I_{L11,rms}$=21.48A, $\hat{I}_{L21}$=2.81A, $I_{L21,av}$ =1.25A, $I_{L21,rms}$=1.79A.

Frequency = 100 kHz, maximum temperatures T_s= 125°C and T_a=50°C

Step 2: Stored energy

The starting point for inductor design is the energy storage capability. Inductors store energy in magnetic fields.

$$L\hat{I}_L I_{rms} = k_{cu} J_{rms} \hat{B} A_w A_{core} \text{ [21]} \quad (5\text{-}7)$$

Where, L is inductance, $\hat{I}_L$ is the peak current, $I_{L,rms}$ is the rms current, k_{cu} is the Copper Fill Factor, J_{rms} is current density, $\hat{B}$ is the peak flux density, A_w is the winding area and A_{core} is the core area.

$$L_{11}\hat{I}_{L11}I_{11,rms} = (40\mu) \times (30.88) \times (21.48) = 2.65 \times 10^{-2}H - A^2 \quad (5\text{-}8)$$

$$L_{21}\hat{I}_{L21}I_{21,rms} = (4m) \times (2.81) \times (1.79) = 2.012 \times 10^{-2}H - A^2 \quad (5\text{-}9)$$

Since the two inductors are coupled on the same core, the total stored energy that the core should handle is $2.65 \times 10^{-2} + 2.012 \times 10^{-2} \approx 0.04752\text{H} - \text{A}^2$.

Step 3: Core material, shape and size.

The converter is operating at a frequency of 100 kHz and the current through the tapped-coupled inductor has a high ripple component. Eddy current loss is a function of the ripple component of the inductor current. To suppress the eddy current loss and due to the high frequency operation, a ferrite material is selected for the core. This is because ferrites have a high electrical resistivity. Ferrites however have low saturation flux densities. The readily available material chosen is N87. A double-E core is chosen for the core shape.

Since the A_{Cu} is directly proportional to k_{cu} a round conductor with a k_{cu} of 0.4 is assumed. The core size with the nearest value of $k_{cu}J_{rms}\hat{B}A_wA_{core}$, which is larger than $L\hat{I}_LI_{rms}$ is chosen. The core chosen is E42/21/15 from Epcos with the following effective dimensions: a= 12.2mm, b=8.65mm, h=29.6mm, d=15.2mm.

$$A_w = b \times h = 256.04mm^2 \quad (5\text{-}10)$$

$$A_{core} = a \times d = 185.44 \times 10^{-6}m^2 \quad (5\text{-}11)$$

From the N87 datasheet, the allowable specific power density, P_{sp}, which can be dissipated in the core and the winding at 100 kHz, 0.2T is 375kW/m^3.

The power dissipated in a copper winding due to resistance is given by

$$P_{cu} = I^2 \times R = (A \times J_{rms})^2 \times \frac{\rho_{cu} l}{A} = J^2{}_{rms} \rho_{cu} Al \quad (5\text{-}12)$$

Where A is the cross-sectional area of the winding, R is the resistance, l is the length, J_{rms} is current density and ρ is the resistivity.

The power dissipated per unit of copper volume in a copper winding due to its DC resistance is given by [21],

$$P_{cu,sp} = \rho_{cu} J^2{}_{rms} \quad (5\text{-}13)$$

Defining copper fill factor as k_{cu},

$$k_{cu} = \frac{Total\ copper\ area}{Winding\ window\ area} = \frac{NA_{cu}}{A_w} \Rightarrow A_w = \frac{NA_{cu}}{k_{cu}} \quad (5\text{-}14)$$

Defining V_{cu} as the total volume of copper and V_w as the total winding volume,

From (5-14), $V_w = \frac{V_{cu}}{k_{cu}}$ (5-15)

The power dissipated per unit of winding volume is given as [21],

$$\therefore P_{w,sp} = k_{cu} \rho_{cu} J^2{}_{rms} \quad (5\text{-}16)$$

The resistivity of copper at 100°C (2.2×10^{-8} Ω-m) is used in equation (5-16) and the value of current density becomes

$$J_{rms} = \left(\frac{P_{sp}}{22 k_{cu}}\right)^{1/2} = \left(\frac{375}{22 \times 0.4}\right)^{1/2} = 6.53\ A/mm^2 \quad (5\text{-}17)$$

B_{max} for a ferrite material is taken to be 0.3 Tesla to avoid core saturation.

$$k_{cu} J_{rms} \hat{B} A_w A_{core} = (0.4) \times (6.53) \times (0.3) \times (256.04) \times (185.44 \times 10^{-6}) = 0.03721$$

This value is slightly greater than 0.024573 for a k_{cu} of 0.4, hence the core selected would effectively handle the stored energy in both inductors.

Step 4: Winding parameters

Copper conductor area, $A_{cu} = \frac{I_{rms}}{J_{rms}}$ (5-18)

$$A_{cu1} = \frac{21.48}{6.53} = 3.29mm^2 \Rightarrow \text{Diameter} = 2.05mm \quad (5\text{-}19)$$

$$A_{cu2} = \frac{1.79}{6.53} = 0.274mm^2 \Rightarrow \text{Diameter} = 0.591mm \quad (5\text{-}20)$$

The skin depth in copper at a frequency of 100 kHz and at 100°C is obtained as [43];

$$\delta_{depth} = \sqrt{\frac{\rho}{\pi \mu_0 f}} = \sqrt{\frac{2.2\times10^{-8}}{\pi\times100\times10^3\times4\pi\times10^{-7}}} = 0.236 \times 10^{-3}m \quad (5\text{-}21a)$$

$$2 \times \delta_{depth} = 0.472mm \quad (5\text{-}21b)$$

Since the conductor diameters of both windings calculated in (5-19) and (5-20) are greater than two times the skin depth, there was need to consider utilising stranded wire conductors to minimise the copper loss. The number of strands needed was calculated as [54]. For the first inductor winding, 0.5mm diameter strands (i.e. AWG# 25; 0.106Ω/m) would be appropriate.

$$N_{1,strands} = \frac{A_{cu1}}{\pi\delta^2{}_{depth}} = \frac{3.29}{\pi\times0.25^2} = 16.76 \approx 17 \quad (5\text{-}22)$$

For the second inductor winding, 0.4mm diameter strands (i.e. AWG# 26; 0.134Ω/m) would be appropriate.

$$N_{2,strands} = \frac{A_{cu2}}{\pi\delta^2{}_{depth}} = \frac{0.24}{\pi\times0.2^2} = 1.9 \approx 2 \quad (5\text{-}23)$$

Mean length of flux for the E-E core, $lm \cong 2(b+h) + 2.5a = 107mm$ (5-24)

Mean length of one turn, $MLT = 4b + 2(a+d) = 89.4mm$ (5-25)

From the core datasheet, the relative effective permeability for a DC current operation is obtained as $\mu_r \approx 1690$ @ 200mT, 100 kHz, 100^0C.

Air gap length, $l_g = \left(\frac{L_{11} \times I_{L1,av} \times \mu_o}{A_c \times {B_c}^2}\right) - \left(\frac{l_m}{\mu_r}\right)$ [54] (5-26)

Air gap length = $\left(\frac{40\mu \times 17.04^2 \times 4\pi \times 10^{-7}}{185.44\mu \times 0.2^2}\right) - \left(\frac{107 \times 10^{-3}}{1690}\right) = 1.1831\text{mm}$ (5-27)

Total reluctance, $\Re_{total} = \frac{l_m}{\mu_r \mu_o A_c} + \frac{l_g}{\mu_o A_c}$ [54] (5-28)

$$= \frac{107 \times 10^{-3}}{1690 \times 4\pi \times 10^{-7} \times 185.44 \times 10^{-6}} + \frac{5.22 \times 10^{-5}}{4\pi \times 10^{-7}}$$

$$= 0.27174 \times 10^6 \text{ turns/wb}$$

Number of turns, N = $\sqrt{L \times \Re_{total}}$ [54] (5-29a)

Number of turns on inductor L_1= $\sqrt{40\mu \times 0.27174 \times 10^6} \cong 3.3$ (5-29b)

Choosing number of turns on inductor L_{11} to be 4 turns, with $\frac{N_{L21}}{N_{L11}} = n = 10$, then number of turns on the second inductor L_{21} is $4 \times 10 = 40$turns.

Winding resistance of the inductor windings is given as [43];

$$r_{L11} = \frac{MLT \times N \times R_{AWG,13}}{N_{1,strands}} = \frac{89.4 \times 10^{-3} \times 4 \times 0.106}{17} = 2.23 \times 10^{-3}\Omega \quad (5\text{-}30)$$

$$r_{L21} = \frac{MLT \times N \times R_{AWG,22}}{N_{2,strands}} = \frac{89.4 \times 10^{-3} \times 40 \times 0.134}{2} = 0.24\Omega \quad (5\text{-}31)$$

$R_{AWG,13}$ and $R_{AWG,22}$ are the resistances of the copper wires per meter obtained from the American Wire Gauge table [59].

5.2.2 Active switch.

When the switch is off, the voltage that it can block, ignoring the voltage spike due to leakage inductance was calculated as shown below so as to determine its ratings.

During the interval when the switch is not conducting, the same current i_{L11} flows in both coupled-inductors L_{11} and L_{21} and the following equations are obtained,

$$V_{in} = V_{L11} + V_{ds} \tag{5-32}$$

$$V_{ds} = V_{in} - V_{L11} \tag{5-33}$$

Since inductors L_{11} and L_{21} are coupled, when the switch is off the voltage across each of them is:

$$V_{L11} = L_{11}\frac{di_{L11}}{dt} + M\frac{di_{L11}}{dt} = (L_{11} + M)\frac{di_{L11}}{dt} \tag{5-34}$$

$$V_{L21} = L_{21}\frac{di_{L11}}{dt} + M\frac{di_{L11}}{dt} = (L_{21} + M)\frac{di_{L11}}{dt} \tag{5-35}$$

$$\frac{V_{L11}}{L_{11}+nkL_{11}} = \frac{V_{L21}}{n^2L_{11}+nkL_{11}} \tag{5-36}$$

Since $M = nkL_{11}$ and $L_{21} = n^2L_{11}$

where M is the mutual inductance, k is the coupling coefficient and $n = \frac{N2}{N1}$

$$\frac{V_{L11}}{L_{11}(1+nk)} = \frac{VL_{21}}{L_{11}(n^2+nk)} = \frac{V_{L11}}{1+nk} = \frac{V_{L21}}{n^2+nk} \tag{5-37}$$

$$V_{L21} = \frac{n^2+nk}{1+nk} \times V_{L11} \tag{5-38}$$

$$V_{L1} = V_{L11} + V_{L21} \tag{5-39}$$

$$V_{L1} = V_{in} - V_o = \left(\frac{1+2nk+n^2}{1+nk}\right) \times V_{L11} \tag{5-40}$$

$$V_{L11} = \left(\frac{1+nk}{1+2nk+n^2}\right) \times (V_{in} - V_o) \tag{5-42}$$

Substituting equation (5-42) into equation (5-33),

$$V_{ds} = V_{in} - \frac{(V_{in}-V_o)(1+nk)}{1+2nk+n^2} \tag{5-43}$$

The voltage blocked by the MOSFET when it is not conducting, ignoring the spike due to the leakage inductance of the coupled-inductors, is hence obtained as,

$$V_{ds} = \frac{V_{in}(nk+n^2)+V_o(1+nk)}{1+2nk+n^2} \quad (5\text{-}44a)$$

$$\text{For } k = 1, V_{ds} = \frac{nV_{in}+V_o}{1+n} \quad (5\text{-}44b)$$

$For\ n = 10, k = 0.98, V_o = 400V, P_o = 1kW, I_{o,ave} = 2.5A$

$For\ V_{in}\ of\ 40V, V_{ds} = \frac{40(109.8)+400(10.8)}{120.6} = 72.24\text{V}$

A power MOSFET with a V_{DSS} of 300V is selected to provide a safety margin due to the spike caused by the leakage inductance in the coupled inductor. A snubber to suppress the voltage spike is designed later in this chapter.

From figure 4.6, MOSFET peak current value is given by,

$$i_{ds,peak} = I_{L11,nom} + \frac{1}{2}\Delta i'_{L1,pk-pk} \quad (5\text{-}45a)$$

$$i_{ds,peak} = \frac{I_{o,ave}(1+nk)}{2(1-D)} + \frac{1}{2}\left(\frac{V_{in}DT_{sw}}{L_{11}}\right) \quad (5\text{-}45b)$$

The MOSFET RMS value is given by,

$$I_{ds,rms} = \sqrt{\left\{\left(\frac{I_{o,ave}(1+nk)}{2(1-D)}\right)^2 D\left[1+\frac{1}{3}\left(\frac{\Delta i'_{L11,pk-pk}}{2\left(\frac{I_{o,ave}(1+nk)}{2(1-D)}\right)}\right)^2\right]\right\}} \quad (5\text{-}45c)$$

From equations (5-45b) and (5-45c), an increase in *n* gives rise to a linear increase in both the switch RMS and peak current, despite the reduction in *D*. This would lead to an increase in both switching and conduction losses in the active switch. A compromise hence needs to be made between the turns ratio and duty ratio to ensure that a choice leading to low switching losses is used.

Power losses in the selected MOSFET

Total switching losses, $P_{sw,total}=P_{sw,on} + P_{sw,off} = 0.5\times V_{ds}\times I_{ds,peak}\times(t_{ri}+t_{fv}+ t_{rv}+t_{fi})\times f_{sw}$ (5-46)

Where, V_{ds} is the voltage blocked by the switch, neglecting the voltage spike due to leakage inductance, I_{ds} is the current through the switch. t_{ri} is the current rise-time, t_{fv} is the voltage fall-time during the turn-on transition of the MOSFET. t_{rv} is the voltage rise-time, and t_{fi} is the current fall-time during the turn-off transition of the MOSFET. f_{sw} is the switching frequency.

Conduction losses, $P_{on} = V_{on} \times I_{ds} \times D = \left(i_{ds,rms}\right)^2 r_{ds,on}$ (5-47a)

Where V_{on} is the on-state voltage and D is the duty ratio.

For a V_{in} of 40V, Vds=72.24V, $i_{ds,rms}$= 19.15A, $i_{ds,peak}$= 31.88A, Duty ratio =0.5

The values of $t_{ri,}$ $t_{fv,}$ t_{rv} and t_{fi} were obtained from the IXFH 69N30P power MOSFET data sheet [58].

$$P_{sw,total} = 0.5 \times 72.24 \times 30.88 \times (52n \times 2) \times 10^5 = 11.6\text{W} \quad (5\text{-}47b)$$

$$P_{on} = r_{ds,on} \times (I_{ds})^2 = 0.058 \times (19.15)^2 = 21.27\text{W} \quad (5\text{-}47c)$$

$$P_{total} = P_{sw} + P_{on} = 32.87\text{W} \quad (5\text{-}47d)$$

Thermal resistance of a switch package is the measure of the package's ability to transfer heat generated by the switch to the circuit board or the ambient. By knowing the thermal resistance of the package, the switch junction temperature, T_j can be calculated for a given power dissipation and its reference temperature [21].

From the datasheet [58], $R_{th(j\text{-}c)}$ =0.25°C/W, $R_{th(c\text{-}s)}$ =0.21°C/W, $T_{j,max}$= 150°C , where $R_{th(j\text{-}c)}$ is the junction-to-case thermal resistance, $R_{th(c\text{-}s)}$ is the case-to-sink thermal resistance.

$$R_{th(j-C)} = \frac{\Delta T}{P_{total}} = \frac{T_j - T_c}{P_{total}} \quad (5\text{-}47e)$$

Thus, $$T_j = \left(P_{total} \times R_{th(j-C)}\right) + T_c \quad (5\text{-}47f)$$

$$= (32.87 \times 0.25) + 125 = 133.22°\text{C} \quad (5\text{-}47g)$$

Hence the junction temperature does not exceed the maximum allowable value of 150°C.

5.2.3 Output diode

The output diode blocks voltage V_d when it is off and the switch is conducting, hence,

$$V_{ds,sat} + V_{L21} + V_d + V_o = 0 \tag{5-48}$$

Where, $V_{ds,sat}$ is the voltage across the switch, V_{L21} is the voltage across the second inductor when the switch is conducting ,V_d is the voltage across the diode and V_{out} is the output voltage.

$$V_{ds,sat} = R_{ds,on} \times I_{ds} \tag{5-49}$$

$$V_d = -(V_{ds,sat} + V_{L21} + V_o) \tag{5-50}$$

When the switch is conducting,

$$V_{in} = V_{L11} = L_{11}\frac{di_{L11}}{dt} \tag{5-51}$$

$$V_{L21} = M\frac{di_{L1}}{dt} = nkL_{11}\frac{di_{L11}}{dt} = nkV_{L11} = nkV_{in} \tag{5-52}$$

Where, i_{L11} is the current through the first inductor when the switch is conducting.

Substituting equation (5-52) into (5-50),

$$V_d = -(V_{ds,sat} + nkV_{in} + V_{out}) \tag{5-53a}$$

For n=10, k=0.98, Vin=40V and V_{out} =400V ,

$$V_d = -(0.8232 + (10 \times 0.98 \times 40) + 400) = -792.8V \tag{5-53b}$$

From Figure 4.6, output diode peak current value is given by,

$$i_{D1,peak} = i_{D2,peak} = I_{L21,nom} + \frac{1}{2}\Delta i'_{L2,pk-pk} \tag{5-54a}$$

$$i_{D,peak} = \frac{I_{o,ave}}{2(1-D)} + \frac{1}{2}\left(\frac{n(V_o - V_{in})(1-D)T_{sw}}{(n+1)L_{21}}\right) \tag{5-54b}$$

For D =0.5, I_{ave} = 2.5A, V_{in} = 40V, V_o =400V, L_{21} = 4mH, $i_{D,peak}$ = 2.7A.

Based on the above voltage and current values, a 1200V, 15A Hyperfast diode was selected.

5.2.4 Output Capacitor

The output capacitor was sized as follows:

$$C_o = \frac{I_o \times D \times T_{sw}}{\Delta V_{c,pk-pk}} \tag{5-55a}$$

To achieve an output voltage ripple of at most 5V, a voltage ripple of 1.25% of the capacitor voltage is selected,

$$V_{c,pk\text{-}pk} = 1.25\% \times 400 = 5V \tag{5-55b}$$

With I_o=2.5, D=0.5 and T_{sw}=10μs,

$$C_o = \frac{2.5 \times 0.5 \times 10\mu}{5} = 2.5\mu F \tag{5-55c}$$

The Voltage across the capacitor, $V_c = V_{out}$=400V. (Ignoring r_{esr}).

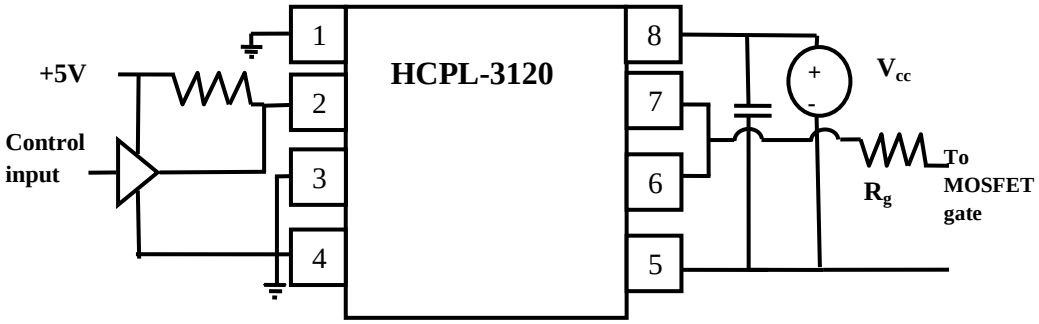
The capacitor RMS current is obtained from equation (3-62b) as,

$$I_{c,rms} = \sqrt{\left\{ \left(I_{o,ave}\right)^2 D + \left(\frac{DI_{o,ave}}{(1-D)}\right)^2 (1-D)\left[1 + \frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2\left(\frac{DI_{o,ave}}{(1-D)}\right)}\right)^2\right]\right\}} \tag{5-55d}$$

A safety factor of about 2 was used and based on the above values of capacitance and voltage, a 2.5μF, 850V capacitor was selected. The high safety factor chosen was to ensure that voltage overshoots following step changes in load are catered for.

5.2.5 Switch gate drive

A MOSFET requires the correct external gate signal for turn-on and turn-off. The MOSFET gate must be held high throughout the ON state. A gate drive must be fast, efficient and reliable for a suitable dynamic response of a converter. The gate drive selected is the MOSFET optocoupler, HCPL3120 [55], shown in Figure 5.5.



. **Figure 5.5.** MOSFET optocoupler, HCPL3120 gate drive

The value of the gate resistor, R_g is selected such that the maximum peak output current rating of the gate driver optocoupler ($I_{OL(peak)}$) is not exceeded.

$$R_g \geq \frac{V_{CC}-V_{EE}-V_{OL}}{I_{OL(PEAK)}} \quad \text{(5-56a)}$$

Where:

V_{OL}= low-level output voltage of the gate driver optocoupler

A V_{OL} of 2V is obtained from the HCPL3120 at a $I_{OL(PEAK)}$ of 2.5A.

$$R_g \geq \frac{15-0-2}{2.5} = 5.2\Omega \quad \text{(5-56b)}$$

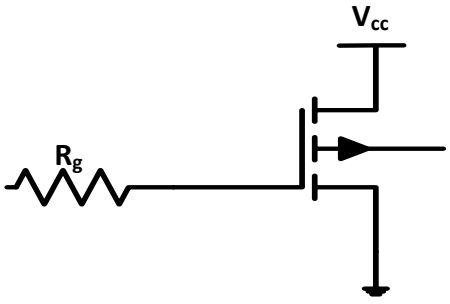


Figure 5.6. A MOSFET with the gate resistance.

5.2.6 Voltage clamp snubber.

The leakage inductance, L_ℓ in the tapped-coupled-inductor induces high voltage spikes on the switch resulting to degradation in efficiency as shown in Figure 5.7. The leakage inductance is effectively in series with the MOSFET. When the MOSFET switches off, the current flow thorough L_ℓ is interrupted and a voltage spike $v_\ell = L_\ell \frac{di_\ell}{dt}$, is induced. If the peak magnitude of the voltage spike exceeds the voltage rating of the MOSFET, then this active switch will fail.

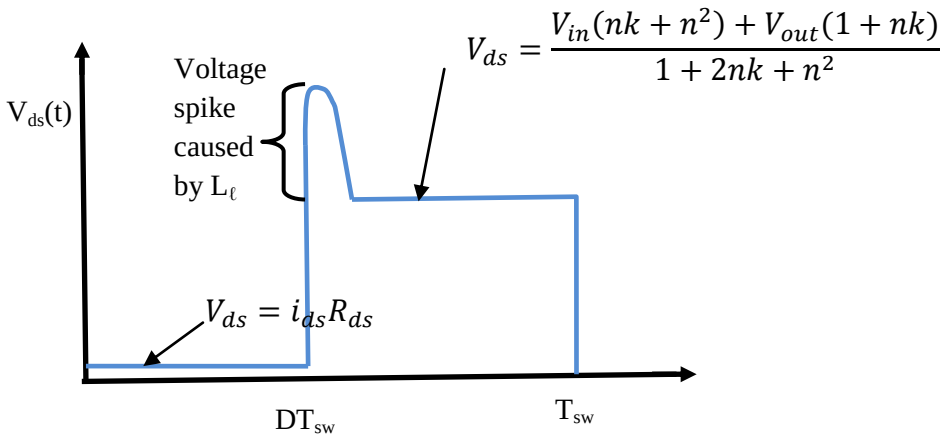


Figure 5.7. Voltage across the MOSFET showing the spike caused by the leakage inductance.

A lossless active-clamp snubber [37], [39] can be used to recycle the leakage energy and reduce the switch voltage stress. Although this method improves the converter efficiency significantly, it requires more active switches and gate driver making the circuit complex and expensive.

Since the main focus was to clamp the voltage and minimize the voltage, a simple RCD snubber, which dissipates the leakage inductance energy, was designed by selecting values of R_S and C_S. The peak switch voltage is clamped at $V_{in}+V_s=150V$, where V_{in} is the input voltage and V_s is the snubber capacitor voltage.

For the designed coupled inductor, the leakage inductance can be approximated as,

$$L_\ell = L_{11} \times (1 - k) = 40\mu H \times (1 - 0.98) = 0.8\mu H \quad (5\text{-}57)$$

Energy stored in L_ℓ during $0< t < DT_{sw}$ is,

$$W_\ell = \left(\frac{1}{2}\right) \times (L_\ell) \times (I_{L1})^2 = \left(\frac{1}{2}\right) \times (0.8\mu) \times (21.48)^2 = 0.185mJ \quad (5\text{-}58)$$

Average power transferred from L_ℓ to snubber is,

$$P_\ell = W_\ell f_{sw} = 0.185mJ \times 100kHz = 18.46W \quad (5\text{-}59)$$

To clamp the spike to 150V, the voltage V_s should be,

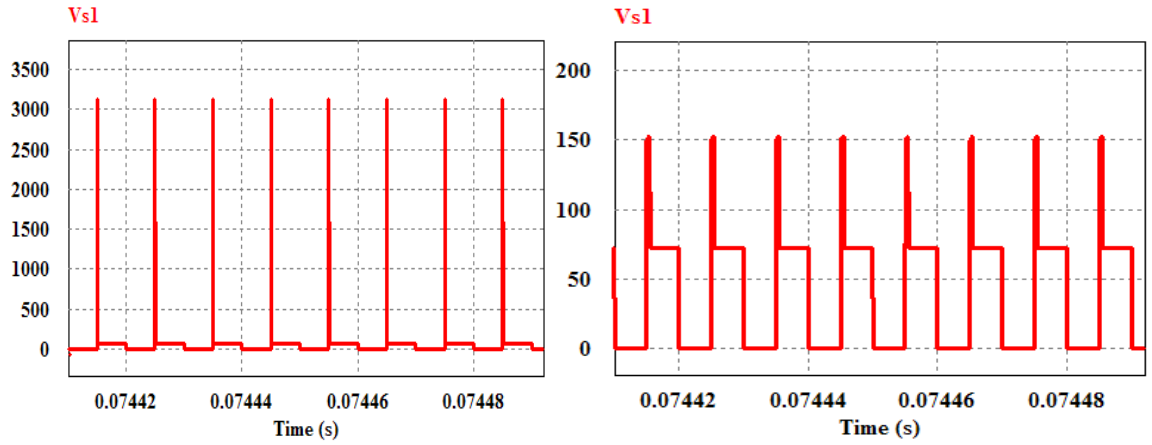
$$V_S = 150V - 40V = 110V \quad (5\text{-}60)$$

R_s is chosen as, $R_S = \frac{{V_S}^2}{P_\ell} = 655\Omega$ (5-61)

C_s is chosen such that $C_S \gg \frac{T_{sw}}{R_S} = \frac{10\mu S}{655\Omega} = 15.3nF$ (5-62)

R_s and C_s are chosen such that V_s is low. A 200Ω, 30W MP930 power film resistor was selected as the snubber resistor, R_s, a 2.2µF, 250V KK2501 capacitor for the snubber capacitor, C_s and the RHRP 15120 as the snubber diode, D_s.

Figure 5.8 shows a simulation of the voltage across the MOSFET S_1 (a) without a snubber and (b) with the designed snubber in the two-phase tapped-coupled-inductor boost converter. Voltage spike suppression by the designed snubber is evident. With the high value of the voltage spike in a converter without snubber, the MOSFET switching loss will be high and a high rated switch with a high $R_{ds(on)}$ will be required which also results to increased conduction loss as well.



(a) Without snubber (b) With the designed snubber

Figure 5.8. Voltage across MOSFET, S_1.

5.3 CHAPTER CONCLUSION

In this chapter, a 1kW two-phase interleaved tapped-coupled-inductor boost converter is designed. The converter is designed to provide a voltage boost ratio of at least ten times. Considerations in selecting the power MOSFETs and the output diode like the blocking voltage, RMS and peak currents and switch losses were determined through analysis. The output capacitor and the coupled-inductor sizing was done and the coupled-inductor design procedure explained. The inductor current ripple is shown to depend on the inductor size, coupled-inductor turns ratio and load. To reduce the effective resistance of the inductor winding conductors due to skin effect, stranded wires were used. Selection of the switch gate drive needed to switch the MOSFET was shown. A simple RCD snubber was designed to clamp the switch voltage and alleviate the voltage stress of the switch. In turn, leakage inductance energy is dissipated in the RCD snubber as opposed to the MOSFET. An active snubber such as the one proposed in [69] can however be used to improve the converter efficiency by recycling the leakage inductance energy.

CHAPTER 6 SYSTEM CONTROL

The output voltage of a switch-mode converter depends on the duty cycle, input voltage, load current and converter circuit components values. The proposed DC-DC converter has to maintain a constant output voltage even in the presence of input voltage and load current variations [43]. Variations in the input voltage and input current in the proposed converter would be due to changes in the temperature and solar radiation on the PV array. Load current variations may be due to step changes in load.

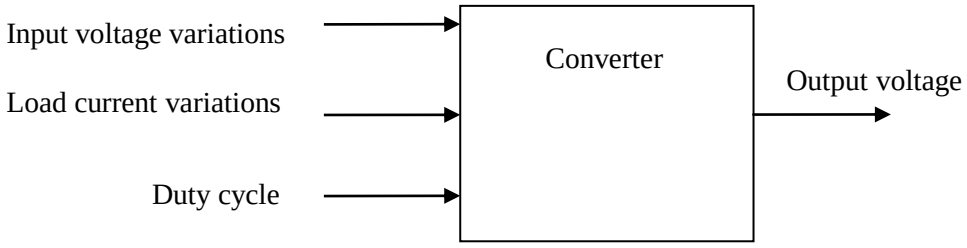


Figure 6.1. Output voltage dependence on variations and duty cycle.

Due to these variations, a negative feedback controller is employed to achieve a converter that automatically adjusts the duty ratio as required to maintain a constant output voltage. The control circuit hence reduces the effect of unwanted input signals on the output. The desired response is known, hence a signal proportional to the error between the desired and the actual response is generated. The output voltage of the DC-DC converter is regulated by sensing the output, comparing it with a stable reference, compensating the error, and then using this error signal to control the input to output power transfer through a pulse – width modulator (PWM). A feedback loop can cause a converter to have oscillations and overshoots, making the system unstable. The compensator network helps to achieve a small error and maintain stability of the switching converter. To improve the phase-margin and extend the bandwidth of the feedback-loop, a lead compensator can be used. A lag compensator can, on the other hand, be used to increase the low-frequency loop gain, hence a better rejection of low-frequency disturbances and low steady-state error [43].

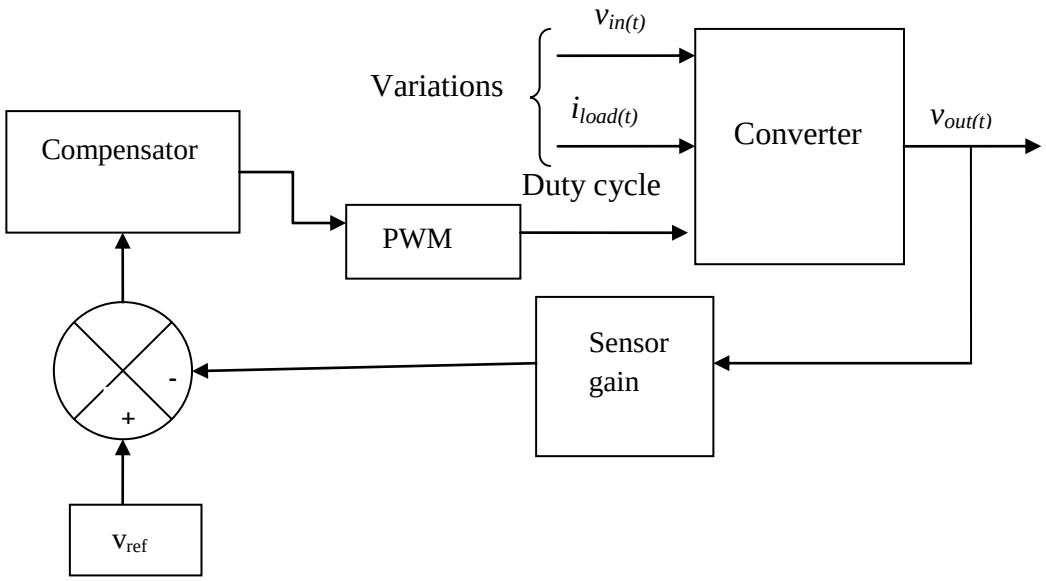


Figure 6.2. Block diagram representing a converter employing a voltage feed-back control.

Other than the voltage-mode control shown in Figure 6.2, another control scheme is the peak current mode. In peak current control, the output is controlled by sensing the peak switch current peak. The PWM saw-tooth ramp is actually the inductor ripple current as it rises while the switch is conducting, translated in to a voltage by a current sense resistor [44]. In the peak current control, an external ramp is added to the sensed current to ensure stability when duty ratio exceeds 0.5.

Average-current mode control is another control scheme that differs from the peak current mode control in that it controls the average value of the current as opposed to controlling the switch peak current. Average current control achieves better accuracy as slope compensation is not required as compared to the peak current control [52].

6.1 BODE PLOTS AND DISCUSSION

A prototype of the two-phase interleaved tapped-coupled-inductor boost converter was built. This converter was tested and controlled at an output power of 225W due to limitations of the available power supplies. Transfer functions required for voltage and

current-mode control schemes were used to obtain bode plots. The bode plots were then employed to evaluate the converter performance as well as to design the controller.

Bode plots were obtained for the following specifications: $V_{o,nominal}$=300V, V_{in}=21V, n=10, L_1= L_{11}+L_{21}=4.04mH, R_{load}=400 Ω, D_1 = D_2 =0.55, C= 2.5µF, $I_{L1,\,av}$= 5.97A, $I_{L2,\,av}$=5.99A. On building the coupled-inductor a coupling coefficient, k of 0.99 was achieved.

The above values were substituted into the control-to-output transfer-function in equation (4-32), describing the first converter and a bode plot constructed as shown in Figure 6.3. This transfer-function describes how the converter control input variations $\tilde{d}_1(s)$ influences the output voltage $\tilde{v}_o(s)$. Regulation of the DC output voltage of the built converter depends on the response of this transfer-function.

$$G_{v_o d_1} = \frac{\tilde{v}_o(s)}{\tilde{d}_1(s)}\Big|_{\tilde{v}_{in}(s)=\tilde{i}_{L12}(s)=\tilde{d}_2(s)=0} = \frac{9.142\times10^4-9.648s}{(4.04\times10^{-6})s^2+0.00404\,s+81} \qquad (6\text{-}1)$$

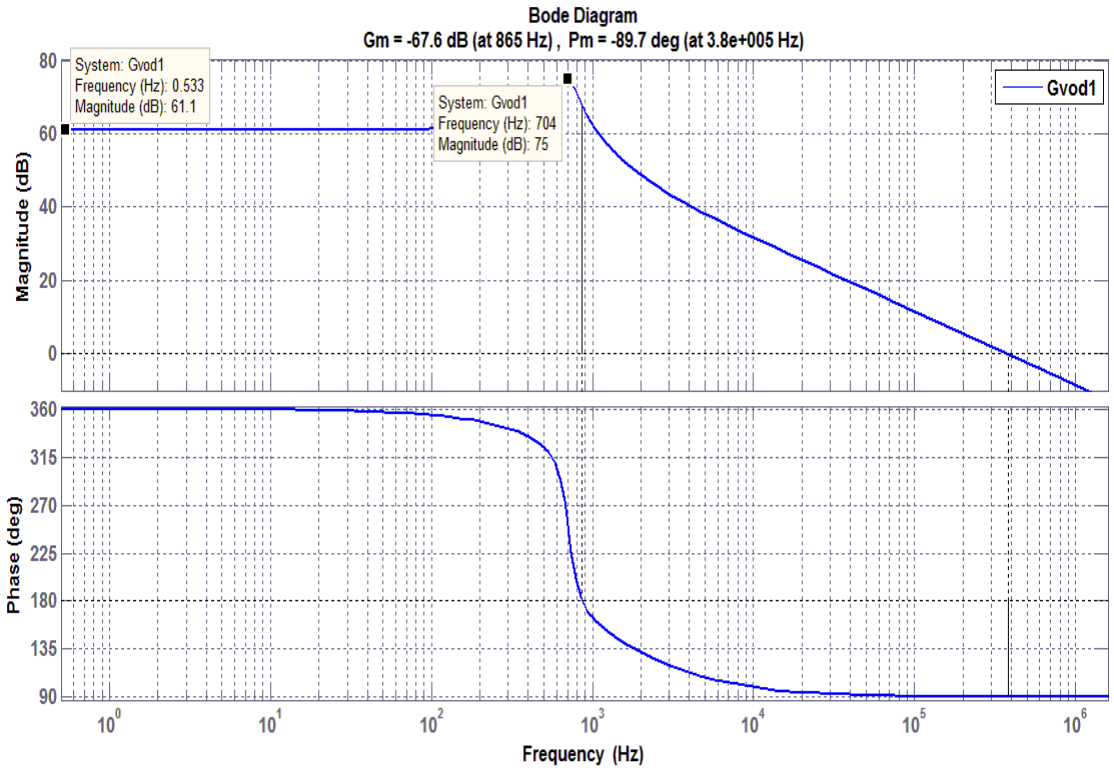


Figure 6.3. Converter control-to-output transfer-function plot

Since the two interleaved converters are identical, the control-to-output response describing the second converter will be similar to the one in Figure 6.3.

Resonant poles exist at a frequency of 700Hz, having a quality factor of 13.8dB or a magnitude of 4.898. These resonant poles cause a 180° phase-lag as can be seen from figure 6.3. The transfer function shows the presence of a right half-plane (RHP) zero at≅ 1.5 kHz. The RHP zero causes a 90° phase-lag on the phase plot. The cause of the (RHP) zero is the phenomenon where the average diode current decreases before it can finally increase with a rise in duty cycle during a continuous inductor current-mode [45]. The phase lag introduced by the RHP zero makes the feedback control-loop more difficult to stabilise, especially as the RHP zero frequency varies with load current [45], [46].

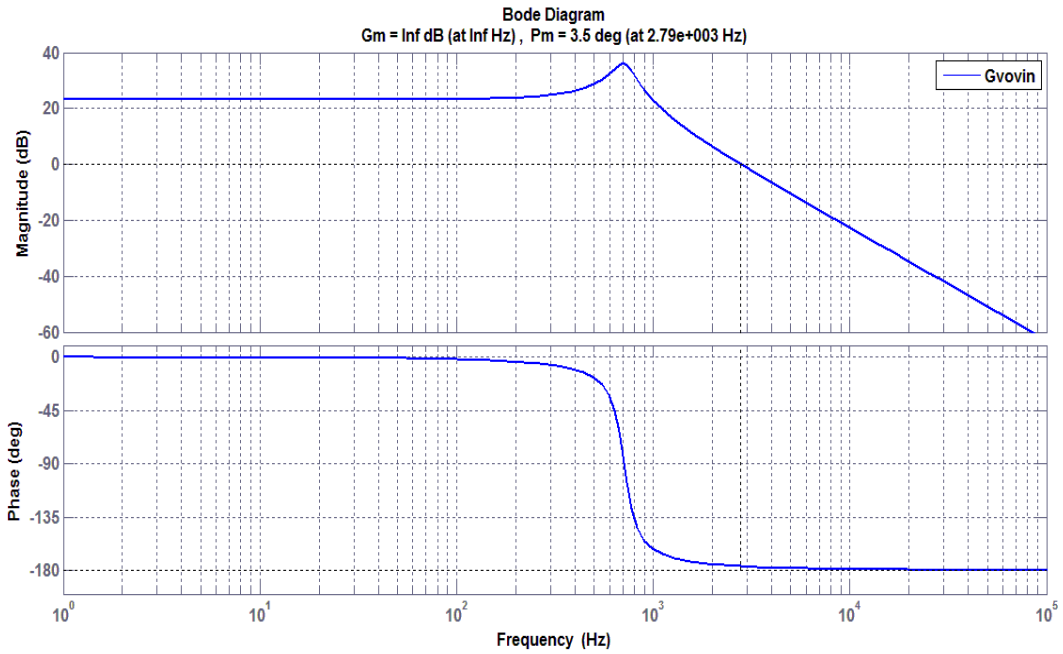


Figure 6.4. Input voltage to output voltage plot.

The converter specifications were substituted into the transfer-function relating input voltage to output voltage in equation (4-34) and a bode plot constructed as shown in Figure 6.4. This transfer-function describes how variations in the converter input voltage $\tilde{v}_{in}(t)$ lead to variations in the output voltage $\tilde{v}_{out}(t)$.

$$G_{v_o v_{\text{in}}} = \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} \Big|_{\tilde{d}_1(s)=\tilde{d}_2(s)=\tilde{\imath}_{L12}(s)=0} = \frac{1160}{(4.04\times10^{-6})s^2+0.00404\,\text{s} + 81} \qquad (6\text{-}2)$$

Similar to the G_{vod1} and the G_{vod2} plots, the G_{vovin} bode plot has the same resonant poles at 700Hz, but has no RHP zero.

The converter specifications were substituted into the transfer functions relating inductor currents i_{L1} and i_{L2} to the duty cycle as described in equations (4-40) and (4-44) are and bode plots constructed.

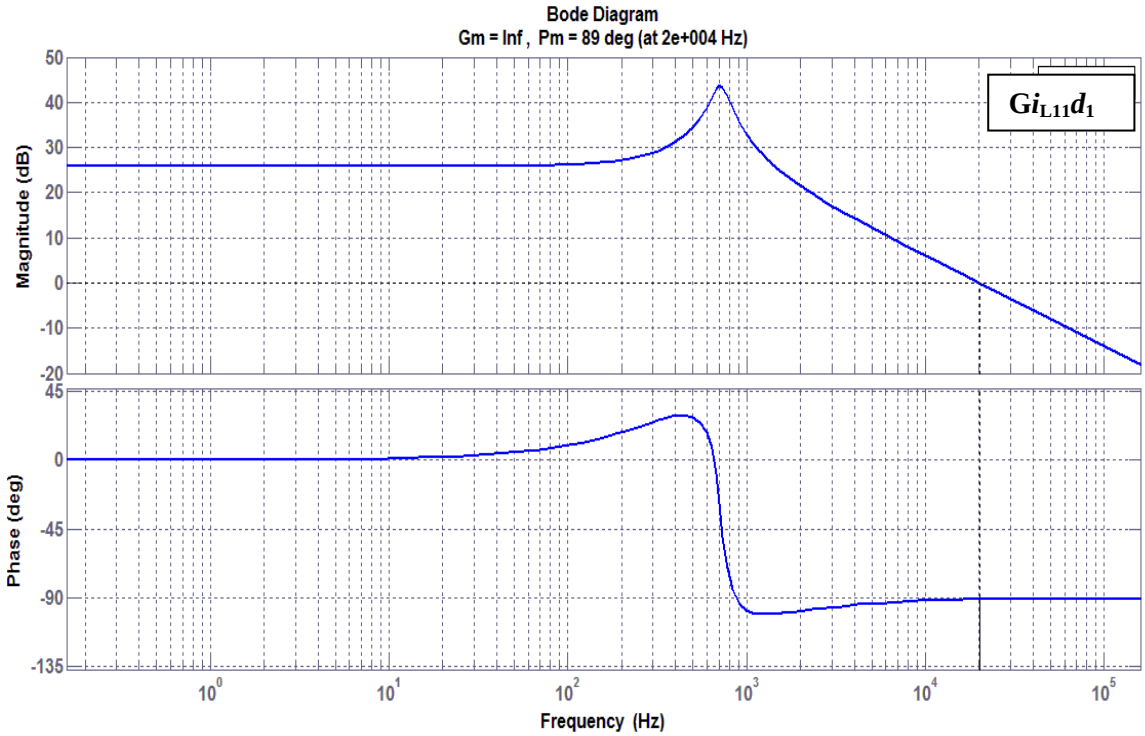


Figure 6.5. Inductor current to duty ratio plot.

This transfer-function describes how the converter control input variations $\tilde{d}_1(s)$ influences the inductor currents.

$$G_{i_{L11}d_1} = \frac{\tilde{\imath}_{L11}(s)}{\tilde{d}_1(s)} \Big|_{\tilde{v}_{in}(s)=\tilde{d}_2(s)=\tilde{\imath}_{L12}(s)=0} = \frac{0.5079\,s + 1583}{(4.04\times10^{-6})s^2+0.00404\,\text{s} + 81} \qquad (6\text{-}3)$$

The G_{iLd} plot presents the same resonant poles as the G_{vod} plot at a frequency of ≅700Hz, which cause a phase-lag of 180°, and a zero that boosts the phase plot as shown in figure 6.3. The G_{iLd} transfer-function has a DC gain of 25.8dB or a magnitude of 19.5 and a phase- margin of 89° at a cut-off frequency of 20 kHz.

6.2 DIGITAL CONTROL

With the reduction in the cost of components such as microprocessors, analogue to digital converters (ADCs) and digital to analogue converters (DACs), digital control of power electronic converters has become popular in the recent past. Moreover, microprocessors with high clock speeds have emerged, leading to a possibility of having digital controllers with a high bandwidth. Digital signal processors (DSPs), micro-controllers and field-programmable gate arrays (FPGAs) are being applied extensively in motor drive controllers and high voltage and high frequency converters [47], [49]. Compared to analogue control, digital control has the following advantages which lead to increased efficiency [50], [60], [61]:

a) Easy to implement computational functions and sophisticated control schemes.
b) Flexible in that code can be modified for other applications.
c) Digital components are less prone to aging, noise and environmental variations.
d) There is improved sensitivity to parameter variations.
e) By using adaptive power management schemes based on digital control technology, significant power savings can be achieved.
f) Reduction in electromagnetic levels.

If the proposed multi-phase interleaved converter is used to interface a large PV array to a load or a DC-bus, digital control would be advantageous in case a string in the array becomes open. By sensing the currents in each string, digital control can be used to reconfigure the multi-phase converter by reducing the phases and the switching signals. Furthermore, in case of a power change in the PV array, digital control can be used to

adjust the converter to work at lower power level or reduce the number of phases. This ensures that the converter operates optimally at all times.

Digital control however has some limitations including:

a) Limited Analog-to-Digital conversion (ADC) resolution and range – numerical values corresponding to the sensed signals in a digital system are limited to a finite number of discrete values depending on the number of bits used in the digital processor. For instance, an 8-bit ADC has 255 discrete levels while a 12-bit ADC has 4095 discrete levels. For a typical reference voltage of 5V, the 12-bit ADC presents a better resolution of 5/4095 or 1.22mV compared to that of an 8-bit ADC of 5/255 or 19.6mV. Loss of resolution leads to an increase in the steady-state error and limit cycles [62], [68].
b) Limited Digital PWM (DPWM) resolution – Hardware timers cause PWM resolution limitation in digital controllers. The output voltage accuracy of the DC PWM is finite, the amplitude modulating resolution of synchronized PWM (SPWM) is limited and the total harmonic distortion (THD) of SPWM is higher than natural sampled PWM. Double PWM has been introduced [63] to improve DPWM resolution. The limit of DPWM should therefore be considered to achieve stable operation.
c) Limit cycles (Steady-state oscillations) – These are steady-state oscillations of output voltage and other system variables at frequencies lower than the converter switching frequency. These oscillations result from the presence signal quantizers such as the ADC and DPWM in the feedback loop. The limit cycles appear when the DPWM tries to regulate the output voltage into a desired level for which there is no close ADC level. The ADC therefore distinguishes this as a steady-state error and the DPWM is forced to change the discrete duty ratio to fix the problem. The DPWM results in not providing the desired output voltage and due to the sequential interaction of between the ADC and the DPWM, the limit cycles are generated.

Undesirable effects of the limit cycles occur when there exists large, unpredicted output voltage variations [64], [65].

d) Time delay- ADC conversion, control algorithm computation by the processor and PWM generation results in a time delay. The time delay is modelled by the function e^{-Ts} , where T is the sampling period of the digital controller. Due to the delay, the phase margin and the control loop bandwidth are decreased. Reduction of the bandwidth degrades the transient response of the system [66], [67].

Figure 6.6 shows a block diagram of a power electronics converter with a digitally controlled feedback loop.

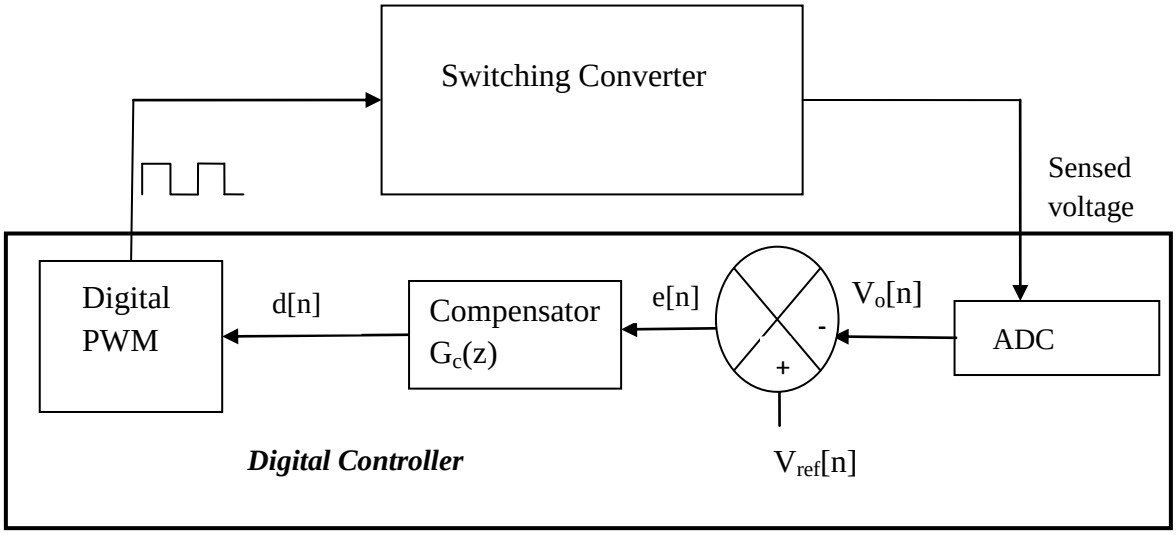


Figure 6.6. Block diagram of a digitally controlled switching converter.

The four blocks including the ADC, a digital compensator and a high-resolution digital pulse-width modulator (DPWM) are all integrated in the processing unit, either a microcontroller or a DSP. In Figure 6.6, a scaled value of the output voltage is digitized and the result is compared with a constant reference. The resulting digital error, e[n] is the input to the digital compensator. A duty cycle is generated which passed through the DPWM to generate a switching signal [47], [48].

There are two commonly used approaches to design a digital controller:

a) Digital redesign/ Emulation
b) Direct digital

In digital redesign, the controller is designed in the continuous s-domain. The analogue controller is then converted to a discrete-time compensator by approximate discretization methods [50], [66], [68]. The advantage of this method is that engineers are more used to thinking clearly in the s-plane than the z-plane. However, it has a disadvantage in that during discretization, the z-plane poles are distorted [68]. Some known discretization methods are shown in table 6.1:

Table 6.1. Discretization Methods

Transformation method	s-Domain	z-Domain.
Forward Euler	s	$(z-1)/T_s$
Backward Euler	s	$(1-z^{-1})/T_s$
Bilinear (Tustin)	s	$2\times(1-z^{-1})/T_s\times(1+z^{-1})$
Prewarp	s	$\left(w/\tan(\frac{wT}{2})\right)(z^{-1}/z+1)$
Step Invariant	$G_c(s)$	$Z\,(1-e^{T_s s}/s)G_c(s)$
Pole/Zero match	$(s+a)/(s+a\pm jb)$	$(1-z^{-1}e^{-aT_s})/(1-2z^{-1}\,e^{-aT_s}cosbT_s + z^{-1}e^{-aT_s})$
Matched pole/zero	e^{sT}	z

The backward Euler method does not preserve the impulse and frequency response of the analogue controller although it is easy to apply. The Bilinear method transforms the whole left-hand-side s-plane into the unit circle in the z-plane; hence there is no aliasing effect. This method preserves both the gain and phase properties of the controller below 1/10 of the sampling frequency. Step response is preserved in the Step Invariant method but the impulse and frequency response are not preserved. Although aliasing is possible if frequencies of zeros are greater than Nyquist frequency in the pole/zero Match transformation, the pole-zero location is preserved [50].

In direct digital however, the converter functions are transformed into z-domain. The controller is then designed directly in the z-domain using methods such as discrete time

frequency response method, root locus method, deadbeat method among others [50]. An advantage of the direct digital approach is that the poles and zeros of the discrete compensator are located directly. A disadvantage however, is that it is difficult for the designer to visualize exactly where the z-domain poles and zeros need to be located for a satisfactory system performance [50], [66].

The digital controller for the two-phase tapped-coupled-inductor boost converter was implemented using the digital redesign approach with the pole/zero match for discretization. The effects of the sampling and hold associated with the ADC and DPWM are ignored.

6.3 PROPOSED CONVERTER DIGITAL CONTROL DESIGN

The control of the proposed interleaved tapped-coupled-inductor boost converter was implemented using digital control. Although a two loop control consisting of an inner current loop and an outer voltage loop has better performance [45], a one-loop voltage control is implemented to validate the design. Digital control was selected to achieve a high-performance and high efficient regulation of the proposed converter. A 32-bit DSP controller, the TMS320F2812, with processor speed up to 150MHz and enhanced peripherals such as, high resolution PWM module, 12-bit A/D converter with conversion speed up to 160nSec, 32x32-bit multiplier, 32-bit timers and real-time code debugging capability was used to implement the controller practically [53]. The digitally controlled two-phase interleaved tapped-coupled-inductor boost converter was interfaced to the TMS320F2812 controller as shown in Figure 6.6 to implement a voltage-mode control.

The instantaneous output voltage was sensed and conditioned using a sensing circuit and then input to the DSP through the ADC. After digitization, the output voltage was compared to V_{ref}. A voltage loop compensator was designed to make the output voltage track the reference V_{ref} while maintaining the desired dynamic performance. The digitized output of the compensator provided the duty cycle command for the interleaved tapped-coupled inductor boost converter. This command output was used to calculate the

appropriate values for the timer compare registers in the on-chip PWM module. The PWM module used this value to generate the 180° phase-shifted gate signal for the two-phase interleaved converter. The frequency of the PWM is 100 kHz and hence the sampling frequency of the voltage-loop was chosen to be 100 kHz.

6.3.1 Analogue compensator design

The controller was designed to achieve specifications shown in table 6.2:

Table 6.2. Controller design specifications.

Loop bandwidth	Settling time	Percentage overshoot	Output voltage regulation	Phase-margin	Gain-margin
At least 1.5kHz	Less than 5ms	Less than 30%	Should not exceed 3% of the nominal voltage.	At least 45^0	At least 5dB

The loop gain of the feedback voltage-loop, T_s is given as:$H(s) \times G_c(s) \times G_{vod} \times 1/V_m$, where *H(s)* is the sensor gain, $G_c(s)$ is the compensator transfer-function, G_{vod} is the converter control to output voltage transfer-function and V_m is the amplitude of the analogue PWM saw-tooth signal.

Output voltage regulation not exceeding 3% of the nominal voltage was targeted; hence the maximum output voltage should not exceed 309V. This output voltage was scaled down by the sensor to a voltage between 0 and 3V, which is then, becomes the ADC input. With the 12-bit ADC, a voltage resolution of $3\text{V}/4095 = 0.732m\text{V}$ per bit is obtained. The value of *H(s)* was therefore calculated as;

$$H(s) = \frac{3}{309} = 0.00971 \qquad \text{(6-4a)}$$

To make the DC output voltage accurately follow the DC reference, V_{ref} was calculated as:

$$V_{ref} = 300 \times 0.00971 = 2.913\text{V} \qquad \text{(6-4b)}$$

The value of V_m was chosen as 4V.

The uncompensated loop gain, $T(s)_{uncompensated}$ with $G_c(s) = 1$ is obtained as:

$$T(s)_{uncompensated} = \frac{221.9 - 0.02342s}{(4.04\times10^{-6})s^2 + 0.00404\,s + 81} \qquad (6\text{-}4c)$$

A bode plot was constructed as shown in Figure 6.7. The uncompensated T_s has the following characteristics: phase margin of -39.2 at a cut-off frequency of 1.58 kHz, a DC gain of 8.76dB or a magnitude of 2.74, a gain margin of -15.3dB at 865 Hz and a quality factor of 4.98. This presents an unstable loop. The presence of the RHP zero also worsens the feedback response as explained in section 6.1.

A compensator, $G_c(s)$ was designed to improve this response and achieve the specifications in table 6.2.

$$Gc(s) = \frac{(5.464\times10^{-5})s^2 + (0.05752)s + 15.14}{s} \qquad (6\text{-}5)$$

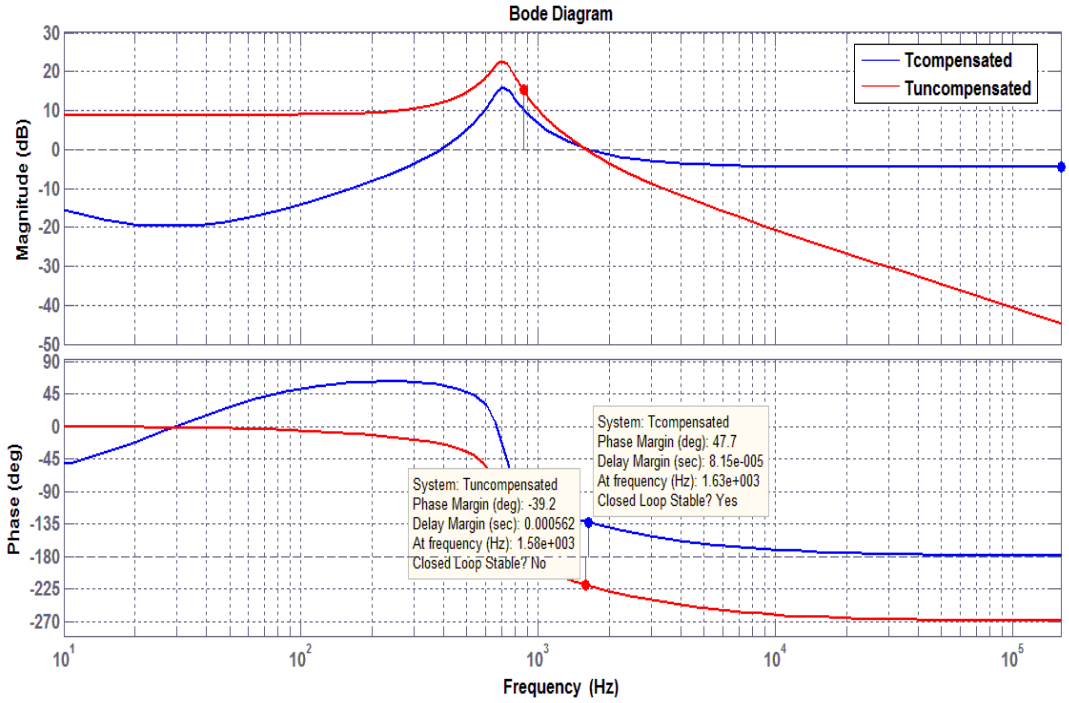


Figure 6.7. Plot of the uncompensated and the compensated loop-gain.

A stable compensated loop gain with a phase margin of 48° at a cut-off frequency of 1.63 kHz, a gain margin of 4.49dB, at an infinity frequency was achieved as shown in Figure 6.5.

6.3.2 Discretization of the analogue compensator.

Since digital design by emulation is used, the designed analogue controller, $G_c(s)$ is discretized using the pole/zero matching method in MATLAB to obtain the digital filter, $G_c(z)$. This is done using the MATLAB script:

```
G(s) = tf([0.0001029 0.03742 3.402],[1 0]);

Ts= 1e-5;

G(z) =c2d(compensator_s,Ts,'matched');
```

In the above script, T_s is the sampling period. The sampling was done at the switching frequency as it gives good trade-off between under sampling and oversampling [56]. The following z-domain transfer-function was generated:

$$Gc(z) = \frac{d}{e} = \frac{10.3z^2 - 20.57z + 10.27}{z - 1} = \frac{10.3 - 20.57z^{-1} + 10.27z^{-2}}{z^{-1} - z^{-2}} \quad (6\text{-}6)$$

In equation (6-6), the multiplier z^{-n} represents a unit delay by one sample period. The difference equation representing the digital compensator is derived from equation (6-6) as:

$$d(n) = d(n-2) - d(n-1) + 10.27e(n-2) - 20.57e(n-1) + 10.3e(n) \quad (6\text{-}7)$$

Where, *d* is the output of the digital compensator and *e* is the error voltage.

6.3.3 Simulation results of the output voltage regulation of a two-phase tapped-coupled inductor boost converter.

To verify the controller operation, the built two-phase interleaved tapped-coupled-inductor converter in Figure 6.8 was simulated. The output voltage was observed for a 5V step change in the input voltage, representing a 23.8% step change, and 50% step change in load. The nominal input voltage is 21V and the nominal load resistance is 400Ω hence a nominal average output current of 0.75A.

A step change of up to 26V was simulated in the input voltage as shown in figure 6.9. A 50% step change in load, representing a variation between 225W and 450W is depicted in Figure 6.10.

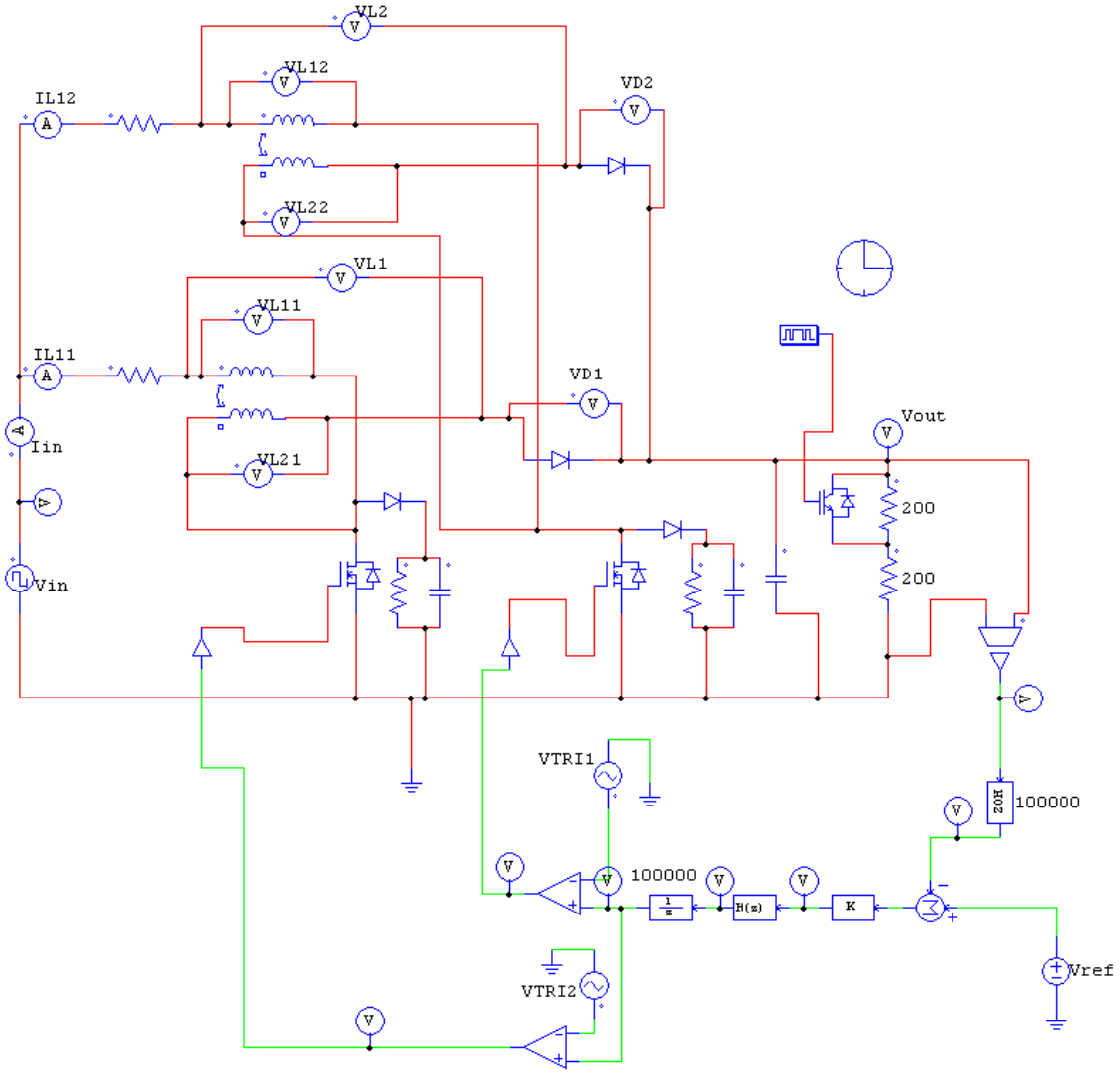


Figure 6.8. Simulated circuit diagram with the digital voltage loop control system.

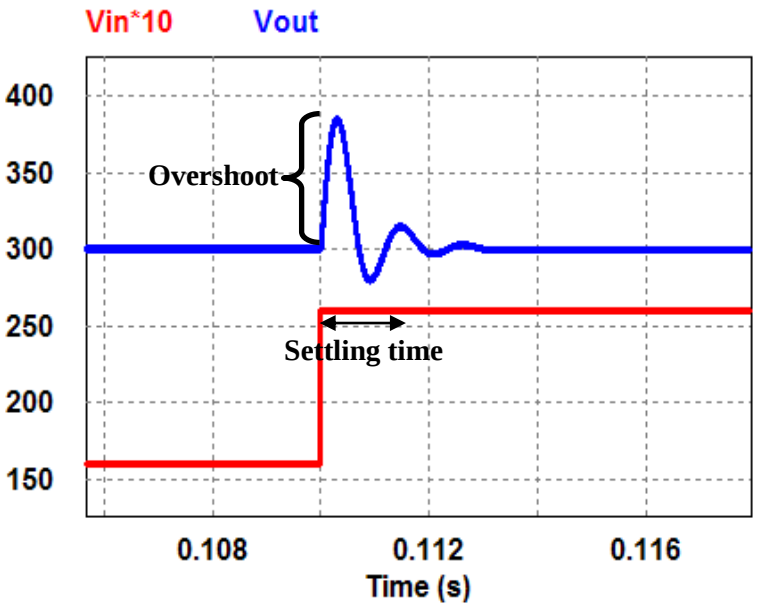


Figure 6.9. Output voltage response (converter with output voltage regulation) for a step input voltage from 16V- 26V.

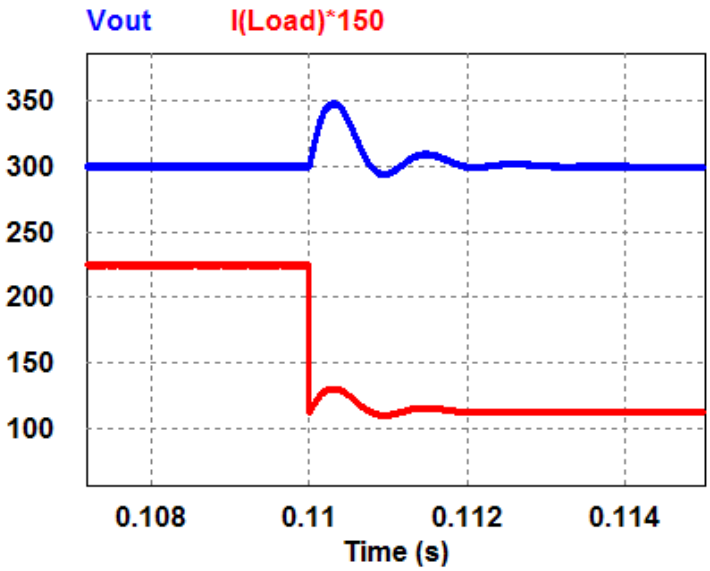


Figure 6.10. Output voltage and current response for a 50% step change in load in the converter with output voltage regulation.

The step response in the input voltage and load results are shown in table 6.3.

Table 6.3. Converter output voltage response to a step change in input voltage and load.

	% overshoot	Settling time	Peak time
23.8% Step change in input voltage	28.51%	1.85ms	0.282ms
50% Step change in load	16.28%	1.7ms	0.271ms

6.3.4 Compensator implementation using the TMS320F2812 DSP

This compensator was implemented practically using the TMS320F2812 DSP instruction set. A software code based on C language calculates a new value of *d(n)*, then the current input sample *e(n)* is moved to *e(n-1)* and then *e(n-2)*, creating room for the new input sample. The oldest sample is discarded. The output values, *d* also are shifted in a similar manner. The program code was implemented using the Code Composer Studio Integrated Design Environment for the C2000 - Family of Texas Instruments Digital Signal Processors.

The first step in using the DSP was setting up the clock module. The C28x is driven outside by a slower external oscillator to reduce electromagnetic disturbances. The DSP used was running at 30MHz externally. An internal frequency of 150MHz was achieved by programming the PLL control register (PLLCR). The general purpose input output (GPIO) ports were then set up. All the GPIO ports are controlled by their own multiplex registers, the GPxMUX (where x stands for the port number). By clearing a bit position to zero, a digital I/O function was selected while setting a bit to 1 meant selecting the special function. The direction of I/O was then set up using the GPxDIR registers. By clearing a bit position to zero, a line was configured as an input while setting a bit position to 1 configures the line as an input [53].

The ADC was then configured using the ADC Control Register 1 (ADCTRL1), ADC Control Register 2 (ADCTRL2), ADC Control Register 3 (ADCTRL3), ADC MAX CONV Register (ADCMAXCONV) and the ADC Input Channel Select Sequencing Control register 1 (ADCCHSELSEQ1) [53]. By using ADCTRL1, bits SEQ_CASC,

CONT_RUN and CPS were set to 0. SEQ_CASC enabled the "Dual Sequencer Mode" of the ADC, CONT_RUN ensured that the ADC stopped and waited for trigger after reaching end of sequence while the CPS bit was for frequency conversion prescaling, where the

ADC clock was set to 25MHz. ADCMAXCONV register was set up to 1 to allow conversions on Sequencer1 (SEQ1). Bits EVA_SOC_SEQ1, INT_ENA_SEQ1 and INT_MOD_SEQ1 in ADCTRL2 were set to enable EVASOC to start SEQ1 and to enable SEQ1 interrupts. The ADCCHSELSEQ1 register was then configured setting input channel ADCINA0 as the first SEQ1 conversion. In the ADCTRL3 register, only the ADCCLKPS bits were setup to 0011b hence adjusting the ADC clock to 25MHz.

To obtain the DPWM, the "Event Manager (EV)" module of the C28x DSP was used. The EV has four timer units which are totally independent of the core timers. An EV is able to produce hardware signals directly from an internal time event, hence most often used to generate time based digital hardware signals. Using the EV-logic, the frequency and/or the pulse width of these signals can be modified [53]. Since the two signals (which are 180^0 out of phase) were required in the two-phase interleaved tapped-coupled-inductor boost converter, compare units 1 and 2 in the EV were used. The EV registers that were set up include;

- General purpose Timer Control Register (GPTCONA) which was used to control polarity of timer compare output
- Timer 1 Control Register (T1CON), which specified the continuous-up/down mode, hence a symmetric PWM. This register also specified the internal clock source, prescaled the clock frequency and enabled the compare operation.
- The Timer period register 1 (T1PR), a 16 bit register was loaded with a value of 750 to set the timer period to 10µs required by the PWM switching period. The value of 750 was determined by using the external oscillator of 30MHz and scaling it using the PLLCR register, the High speed clock prescaler (HSPCP) and the T1CON prescaler.

- With the compare registers CMPR1 and CMPR2 two different switching patterns were specified based on T1PR. The value loaded in CMPR1 was obtained after executing the compensator algorithm. This same value is then phase-shifted by 180^0 in the C-language code and then loaded to CMPR2. The output of the "Output Logic" modules in the EV, which are PWM signals, are then obtained from pins PWM1 and PWM3 for CMPR1 and CMPR2 respectively.
- The Action Control Register (ACTRA) and the Compare Control Register (COMCONA) were used to adjust the shape of the physical PWM output signal. The Dead-Band Timer Control Register (DBTCONA) was then set to zero to disable the deadband.

Operating at a low DPWM resolution results in limit cycles mentioned in section 6.2. In this controller design, the DSP that was used has a standard PWM. At 150MHz CPU frequency, 100 kHz converter switching frequency, a DPWM effective resolution of 9.55 bits was achieved. A higher DPWM resolution can however be achieved by using a DSP with a high-resolution DPWM (HR-DPWM) module.

6.3.5 Tapped-coupled inductor converter interfacing with the DSP controller.

The LEM LV 25-P voltage transducer was used to sense the output voltage from the two-phase tapped-coupled-inductor boost converter. The output voltage of about 300V was scaled down by the transducer to a voltage between 0 and 3V. The input voltage into the ADC can however be up to a maximum of 3.3V.

For proper operation of the ADC, the analogue signal from the output voltage sensor output should be free from noise. Presence of noise degrades the performance of the converter, leading to inaccurate and unstable converted counts [57]. An op-amp driver circuit can be used for signal conditioning of the analogue signal and as a buffer [57].

The voltage level of the gating control signal from the PWM pins of the DSP is 3.3V [57]. A buffer and an optocoupler were used as an interface between the DSP PWM pins and the

MOSFET gate drives. With this isolation, digital voltage level translation and DSP protection from faults in the converter were achieved.

6.4 CHAPTER CONCLUSION.

This chapter presents the digital control of a two-phase interleaved tapped-coupled-inductor boost converter. Reasons for converter control, to regulate the output and improve converter response are explained. The significant transfer functions for the voltage regulation were discussed and bode plots constructed. Digital control of power converters was introduced and advantages and disadvantages compared to analogue control discussed.

Digital control is identified to have better performance and flexibility, and is thus chosen for control. The two common approaches of designing a digital controller were explained and their advantages and disadvantages discussed. The controller desired specifications are identified. Due to prior familiarity with analogue control, digital design by emulation was selected and the steps to obtain the difference equation which represents the digital filter are shown. In a PV array, by sensing the currents in each string, digital control can be used to reconfigure the multi-phase converter by reducing the phases and the switching signals. Furthermore, in case of a power change in the PV array, digital control can be used to adjust the converter to work at lower power level or reduce the number of phases. This ensures that the converter operates optimally at all times.

The controlled controller was simulated and results presented. The controller simulation results show that objectives were met in the voltage regulation loop design. Due to the closed-loop control, the output voltage sensitivity to input and load variations is reduced significantly. The values of percentage overshoot, settling time and peak time achieved from simulation are lower for both step change in input voltage and step change in load compared to the desired values.

Practical controller implementation using the DSP was explained, which included programming the DSP registers and interfacing the DSP controller to the converter.

CHAPTER 7 SIMULATIONS

In this chapter, multi-phase interleaved tapped-coupled-inductor boost converters were simulated. Six DC-DC converters, starting with a single-phase to a six-phase tapped-coupled-inductor boost converter were simulated for performance analysis and comparing their suitability for PV application. Simulation specifications used, including a snubber, are those designed for in chapter 5. The six simulated converters have the same circuit specifications which are V_{in} = 40V, V_{out} = 400V, P_o= 1000W, f_{sw}= 100kHz, output voltage ripple of 1.25% of the capacitor voltage, k = 0.98, n=10, r_{L1}= 2.23mΩ, r_{L2}=240mΩ and $R_{ds(on)}$= 49mΩ. The waveforms are obtained for the non-ideal converters including the inductor winding losses and the switch and diode voltage drops. Equation (3-42) is used to calculate the turns ratio, n, to achieve the required voltage boost ratio of about ten times, at a low duty ratio less than 0.5 in the single-phase converter. A turns ratio of 10 was hence used in the design. The tapped-coupled inductor values used are, L_{1N}=40µH, L_{2N}=4mH, and mutual inductance of 392 µH while the output capacitor has a value on 2.5 μF.

The performance parameters used to compare the six simulated converters include:

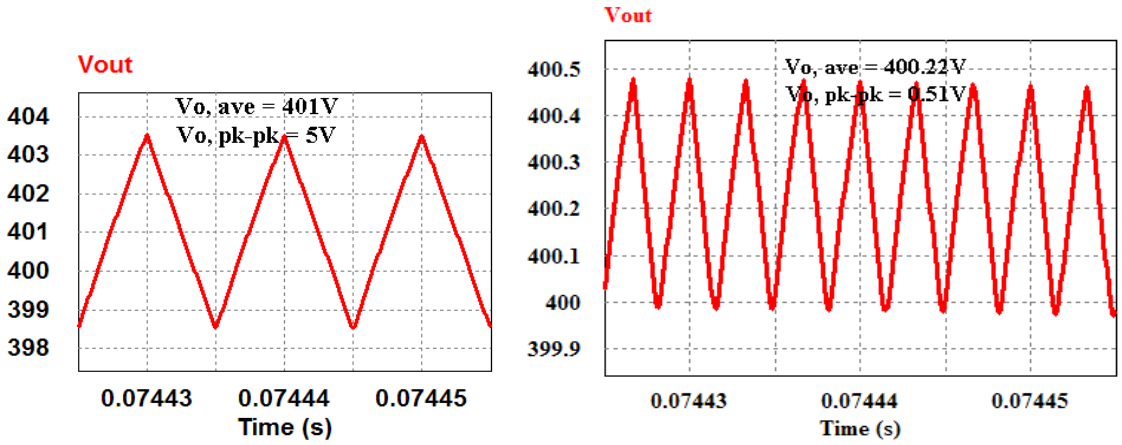
a) Boost ratio
b) Input current, output voltage and load current ripple
c) RMS input current ripple
d) Output capacitor RMS current
e) Peak values of input and switch current
f) Efficiency

Waveforms of converters with odd number of phases are grouped together and likewise for even number of phases for performance comparison.

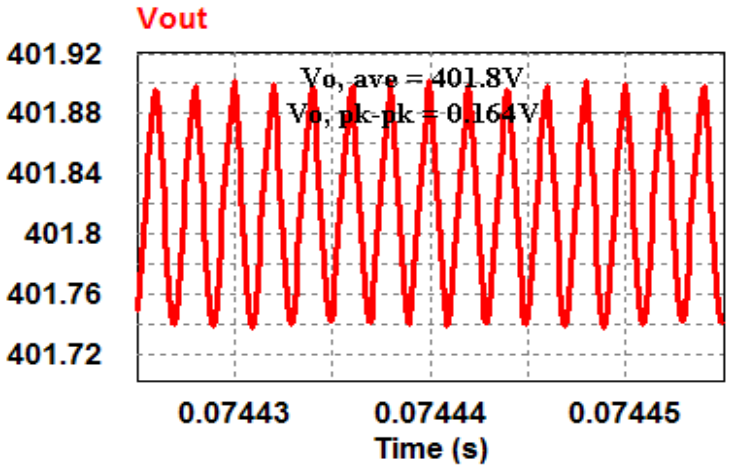
7.1 WAVEFORMS OF MULTI-PHASE TAPPED-COUPLED-INDUCTOR BOOST CONVERTERS WITH ODD NUMBER OF PHASES.

Waveforms of the output voltage and current, input and capacitor current for the single-phase, three-phase and five-phase tapped-coupled-inductor boost converters are presented in this section. Figure 7.1 shows the output voltage waveforms.

The values of the average output voltage and the peak-to-peak output voltage ripple for each converter are also shown.



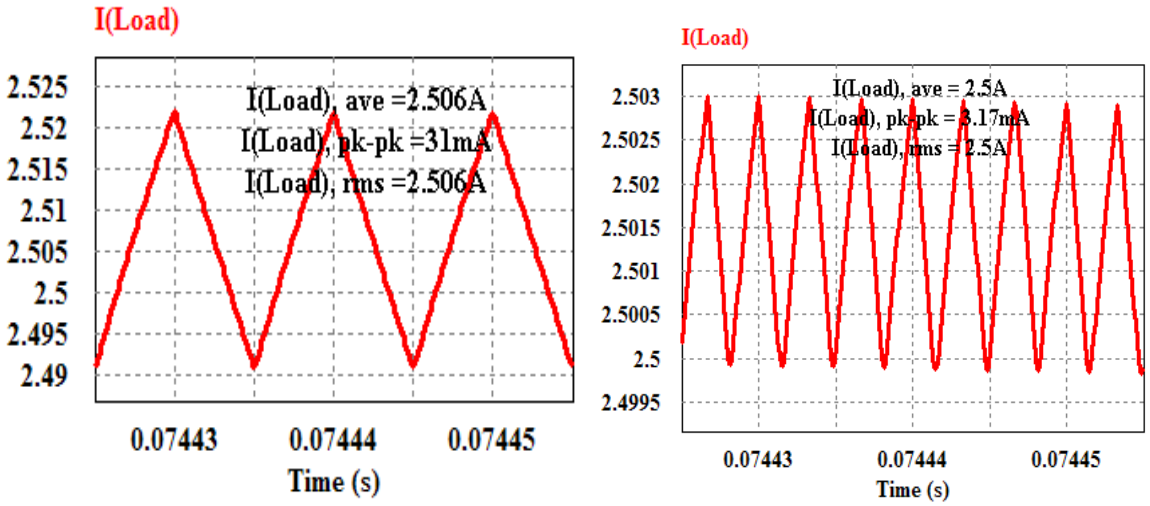
(a) single-phase (b) three-phase



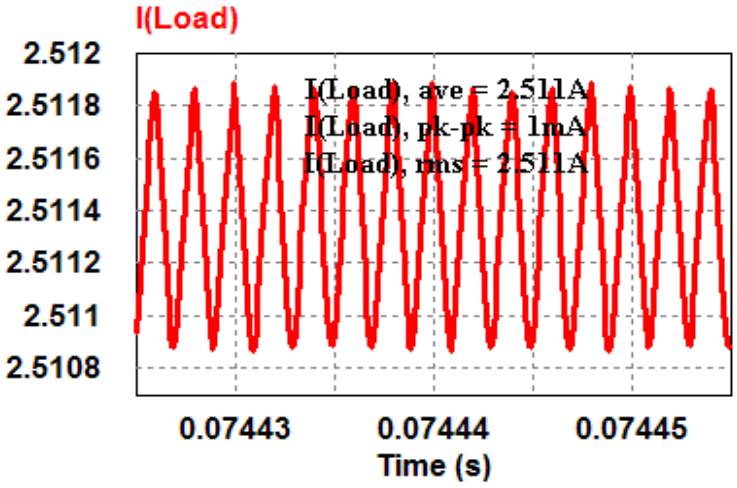
(c) five-phase

Figure 7.1. Output voltage of the tapped-coupled-inductor boost converters.

Figure 7.2 shows the output current waveforms for the three converters. The values of the average, RMS and ripple currents are also shown for each waveform.



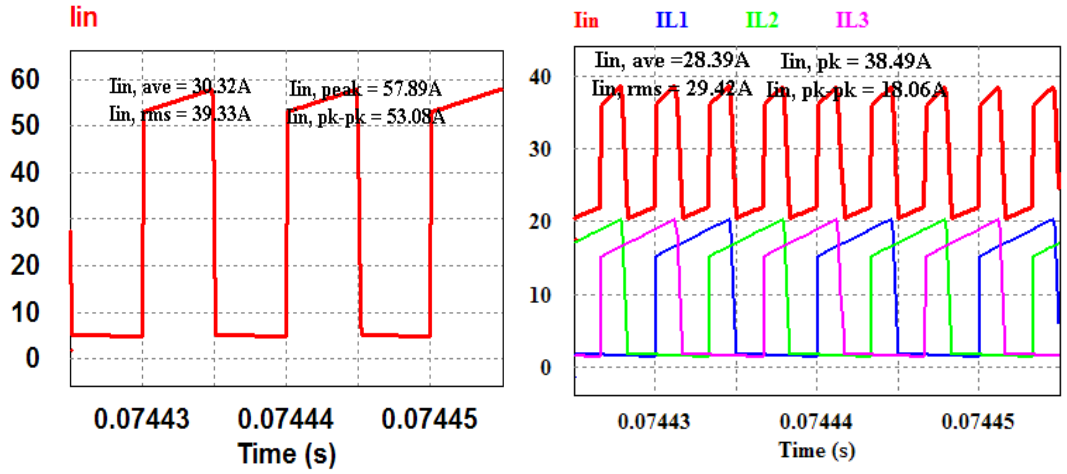
(a) single-phase (b) three-phase



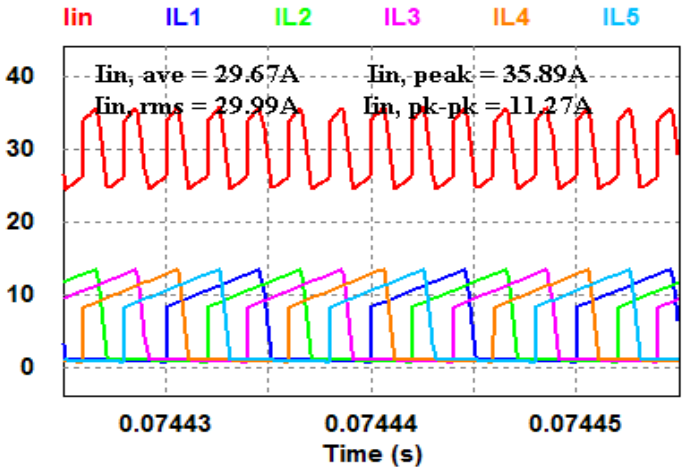
(c) five-phase

Figure 7.2. Output current waveforms of the tapped-coupled-inductor boost converters.

Figure 7.3 shows the input and phase currents for the three converters. The average input and phase currents, RMS input and phase currents, the input peak current and the input current peak to peak values are also shown for each converter.



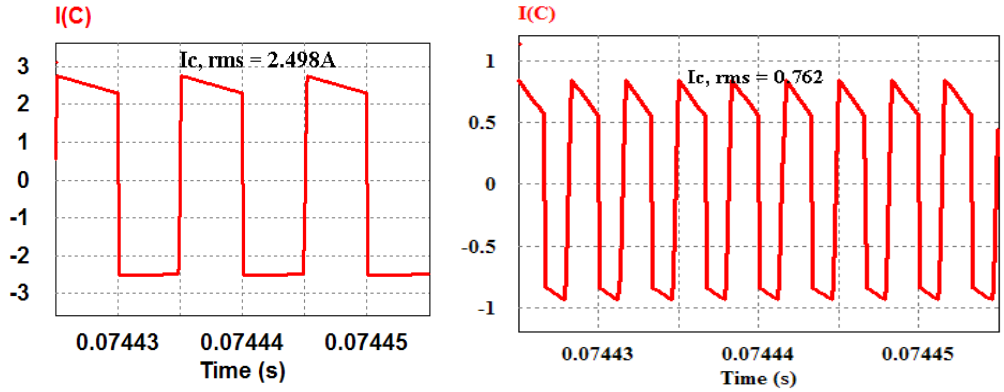
(a) single-phase (b) three-phase



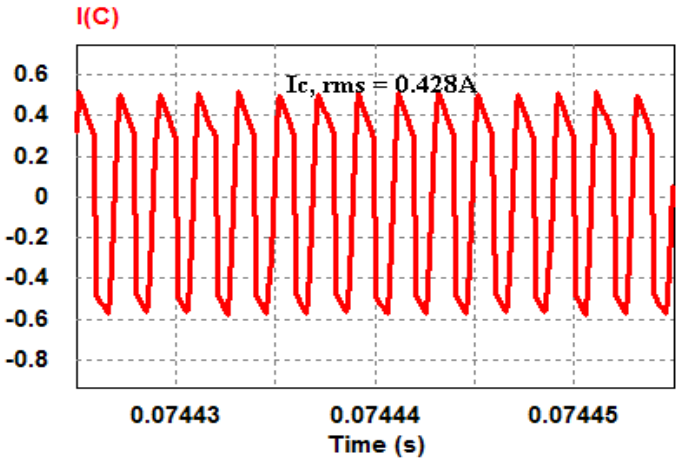
(c) five-phase

Figure 7.3. Input and phase current waveforms of the tapped-coupled-inductor boost converters.

Figure 7.4 shows the output capacitor waveforms and the RMS values for the three converters with odd number of phases.



(a) Single-phase (b) three-phase



(c) five-phase

Figure 7.4. Capacitor current waveforms.

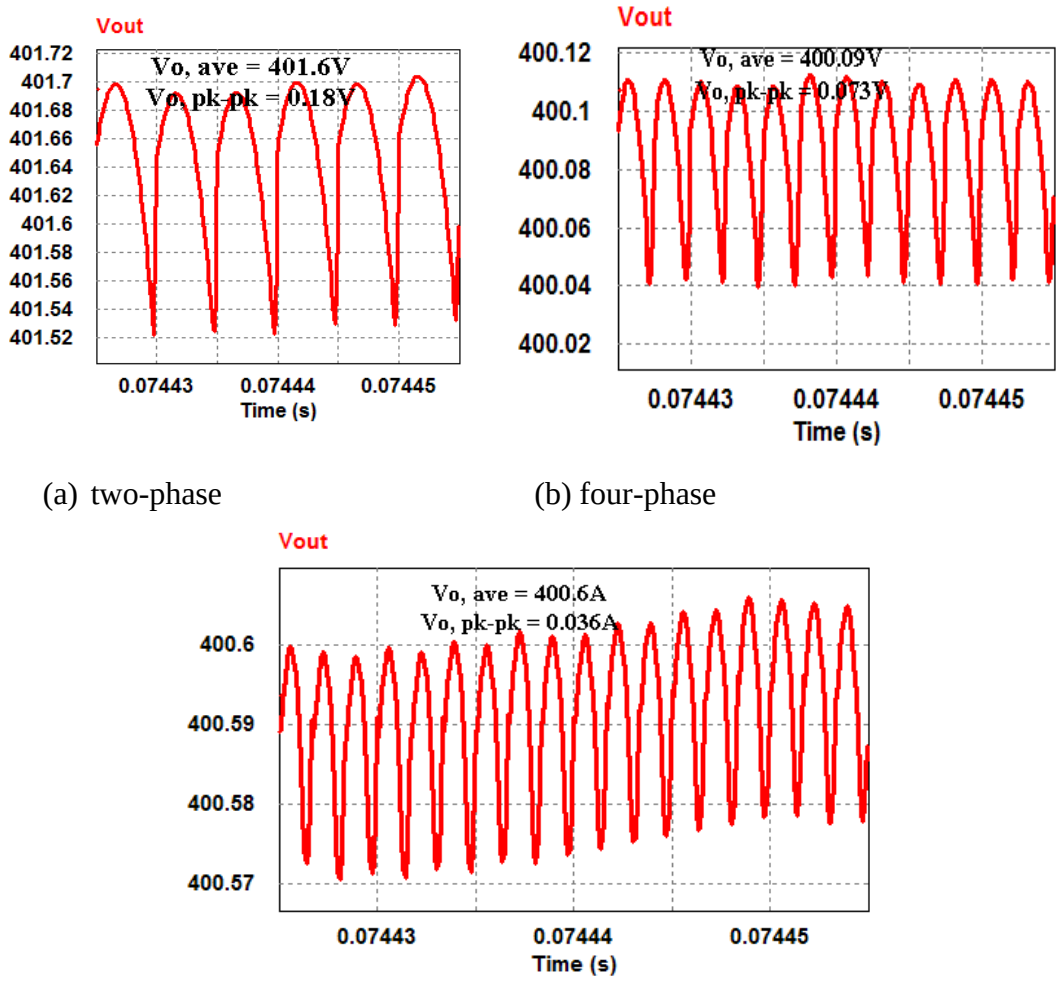
Different parameter values obtained from the simulated waveforms in Figures 7.1 to 7.4 are summarized in table 7.1.

Table 7.1. Characteristics for converters with odd number of phases

	$I_{in,\ rms}$	$I_{in,\ rms\ ripple}$	$I_{c,\ rms}$	$V_{o,\ pk\text{-}pk}$	$I_{o,\ pk\text{-}pk}$	$I_{in,\ pk\text{-}pk}$	$I_{switch,\ peak}$	D
1-phase	39.3A	25.05A	2.49A	5V	31mA	53.08A	57.89A	0.494
3-phase	29.4A	7.72A	0.76A	0.51V	3.17mA	18.06A	20.36A	0.464
5-phase	29.99A	4.37A	0.43A	0.16V	1mA	11.27A	13.59A	0.461

7.2 WAVEFORMS OF MULTI-PHASE TAPPED-COUPLED-INDUCTOR BOOST CONVERTERS WITH EVEN NUMBER OF PHASES.

The output voltage and current, input and capacitor current waveforms for the two-phase, four-phase and six-phase tapped-coupled-inductor boost converters are presented in this section. Figure 7.5 shows the output voltage waveforms. The values of the average output voltage and the peak to peak output voltage ripple for each converter are also shown.

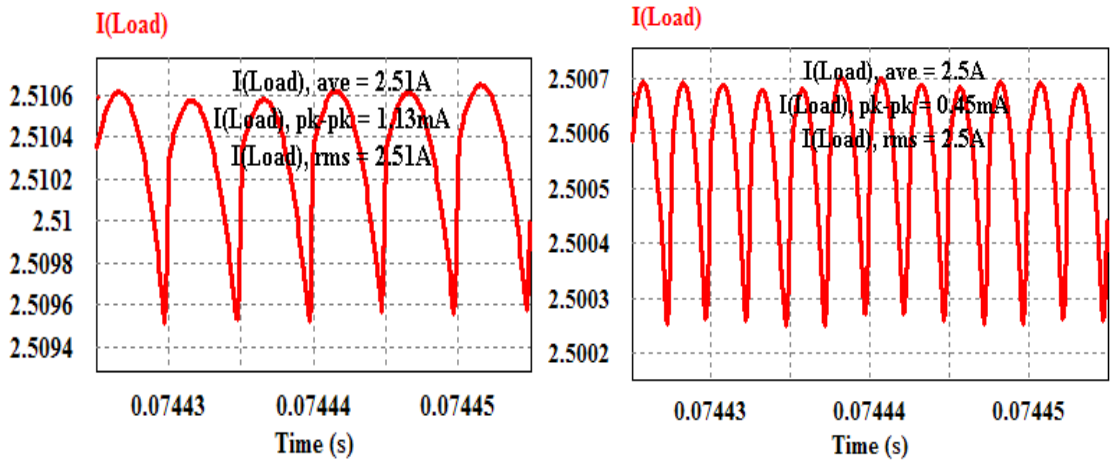


(a) two-phase (b) four-phase

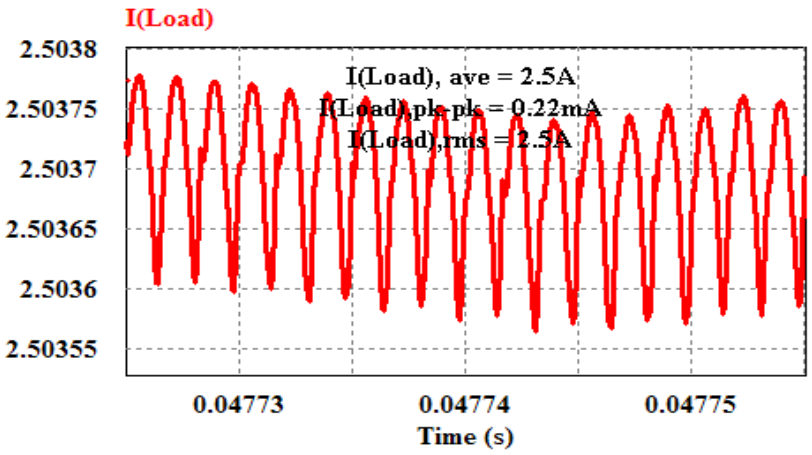
(c) six-phase

Figure 7.5. Output voltage of the tapped-coupled-inductor boost converters with number of phases.

Figure 7.6 shows the output current waveforms for the three even-phase converters. The values of the average, RMS and ripple currents are also shown for each waveform.



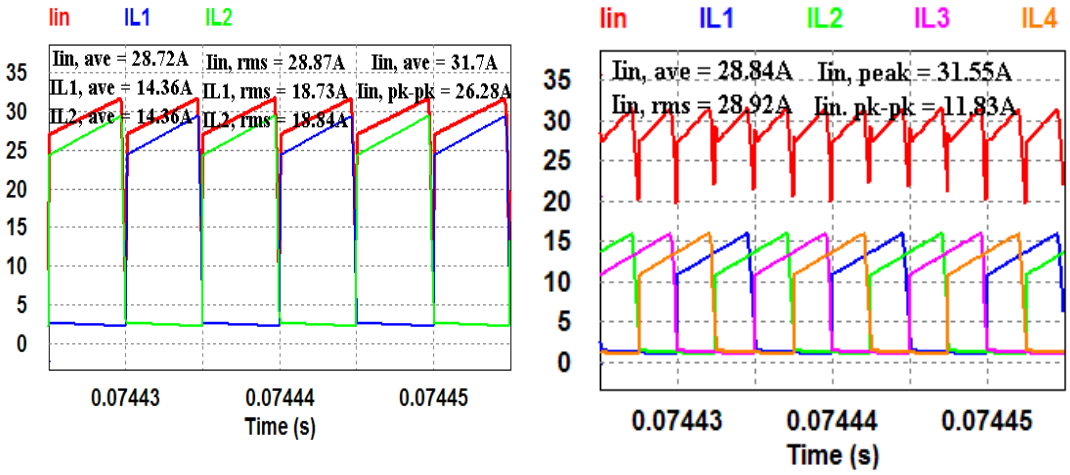
(a) two-phase (b) four-phase



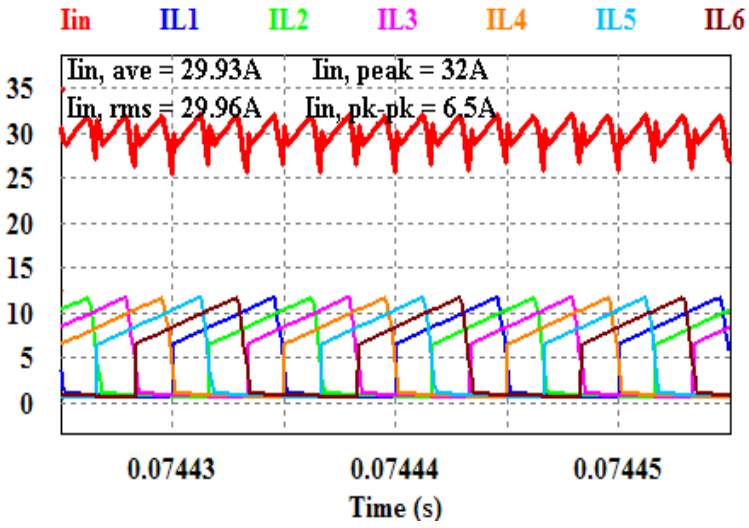
(c) six-phase

Figure 7.6. Output current of the tapped-coupled-inductor boost converters with even number of phases.

Figure 7.7 shows the input currents and the phase currents in the three even-phase converters. The average input and phase currents, RMS input and phase currents, the input peak current and the input current peak to peak values are also shown for each converter.



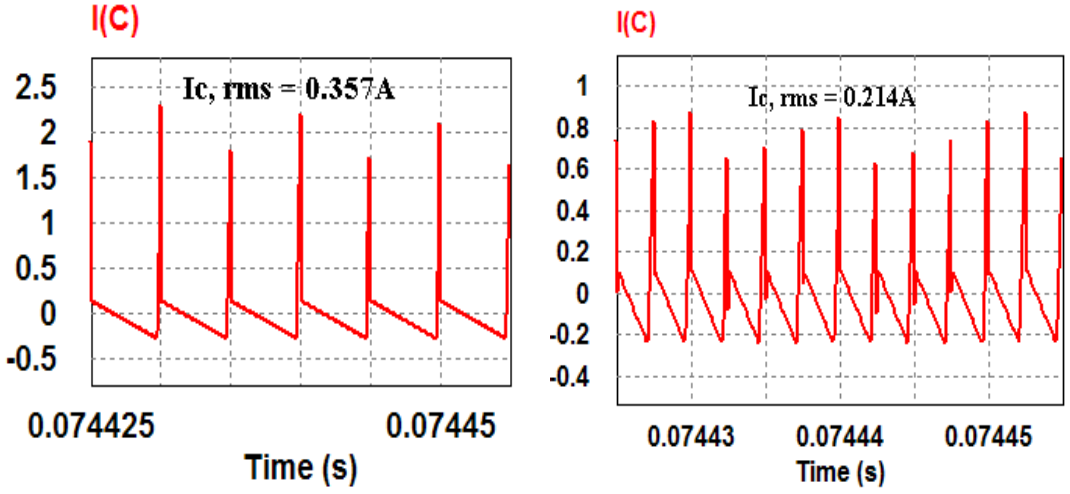
(a) two-phase (b) four-phase



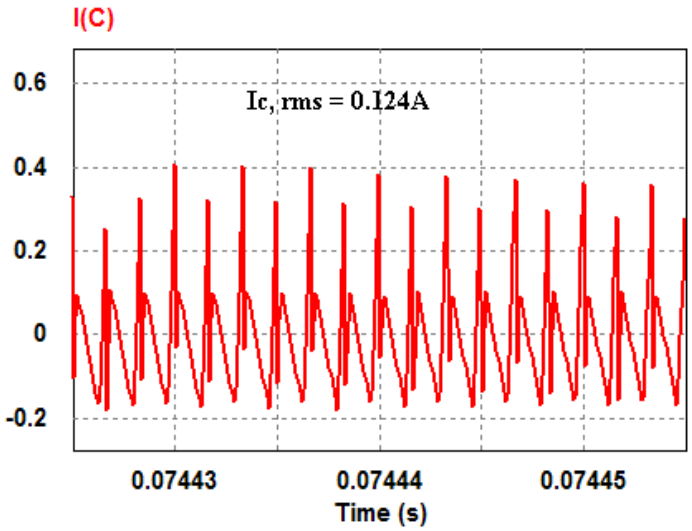
(c) six-phase

Figure 7.7. Input current of the tapped-coupled-inductor boost converters with even number of phases.

Figure 7.8 shows the output capacitor current waveforms and the RMS values for the three converters with even number of phases.



(a) Two-phase (b) four-phase



(c) six-phase

Figure 7.8 Capacitor current waveform.

Different parameter values obtained from the simulated waveforms in figures 7.5 to 7.8 are summarized in Table 7.2.

Table 7.2. Characteristics for converters with even number of phases.

	$I_{in,\ rms}$	$I_{in,\ rms\ ripple}$	$I_{c,\ rms}$	$V_{o,\ pk\text{-}pk}$	$I_{o,\ pk\text{-}pk}$	$I_{in,\ pk\text{-}pk}$	$I_{switch,\ peak}$	D
2-phase	28.87A	3.39A	0.36A	0.18V	1.13mA	26.28A	29.47A	0.472
4-phase	28.92A	2.15A	0.21A	0.073V	0.45mA	11.83A	16.06A	0.461
6-phase	29.96A	1.34A	0.12A	0.036V	0.22mA	6.5A	11.77A	0.458

7.3 SIMULATION DISCUSSION AND PERFORMANCE ANALYSIS OF THE SIX SIMULATED TAPPED-COUPLED-INDUCTOR BOOST CONVERTERS

The simulations in sections 7.1 and 7.2 indicate similarities in the shape of waveforms for the odd number of phases as well as the even number of phases for the duty ratio chosen. From Figures 7.1 and 7.2 showing output voltage and current waveforms respectively for odd N, it can be seen that the waveforms have a triangular shape. This can compared to the output voltage and current waveforms from converters with an even N in Figures 7.5 and 7.6 which have a rounded shape. Input current waveforms from converters with an odd N in Figure 7.3 have waveforms with a similar shape and likewise for converters with even N in Figure 7.7. The converters with the odd number of phases thus present input and output waveforms with higher order harmonics compared to converters with even number of phases for the chosen duty ratio.

The ripple frequency increases by a factor of N as shown in Figures 7.1 to 7.8. For example, the six-phase converter has six times the ripple frequency of the single-phase converter. The increase in ripple frequency with increase in the number of phases leads to reduction in current variations dependent on inductor size as it was shown in figure 5.3. Lower sized inductors can hence be used with increase in N resulting to a higher power density and improved transient response. However inductor ripple is also dependent on the coupled-inductors turns ratio and load as shown in equations (3-59) and (3-61) hence they also need to be considered to ensure minimal input current ripple.
Other performance parameters used to compare the simulated multi-phase converters are explained in the following sections.

7.3.1 Boost ratio

From the output voltage waveforms in Figures 7.1 and 7.5, and values in tables 7.1 and 7.2, it can be seen that a high boost ratio of about 10 times can be achieved by all the tapped-coupled-inductor boost converters without an extreme duty ratio. However, a single-phase converter requires a higher duty ratio of 0.494 compared to the interleaved converters. The duty ratio required for the same boost ratio decreases nonlinearly with N, where a six-phase converter requires the least value of 0.458. This shows that by interleaving the tapped-coupled-inductor boost converter, even higher boost ratios can be achieved, where the boost ratio increases with N.

As a result of current sharing in the interleaved converters, the current flowing through each phase is reduced by a factor of N. Copper and switch conduction losses are in turn reduced as the RMS value of per-phase current decreases with an increase in N as can be seen analytically in table 4.1. The voltage drops across the series resistance of the inductors, the switches and diodes when they are conducting are hence reduced nonlinearly with an increase in N. As it can be seen from tables 7.1 and 7.2, the peak switch current decreases nonlinearly as N increases, from a value of 57.89A in the single-phase converter to 11.77A in the six-phase converter. This results to a reduction in converter switching losses as N increases. These reduced converter components voltage drops and losses with increase in N are the reasons for the increase in boost ratio as N increases.

7.3.2 Capacitor current

From Figures 7.4 and 7.8 showing the capacitor current waveforms and values in tables 7.1 and 7.2, it is shown that the RMS value of capacitor current is lower in the converters with an even value of N as compared to those with an odd value of N for the chosen duty ratio. This RMS value however decreases non-linearly with N for each case. The converter with the smallest even value of N= 2, is shown to have a capacitor RMS current value of 0.36A. This value is lower than the value obtained from the converter with the highest odd value of N=5, which has a value of 0.43A. The lower capacitor RMS current values in the

converters with even number of phases as compared to those with odd number of phases means that smaller output capacitors are required in the converters with even number of phases as compared to those with odd number of phases for the considered duty ratio range.

Capacitor RMS currents in the multi-phase tapped-coupled-inductor boost converters hence depends on number of phases and duty ratio which is also confirmed by the derived single-phase and two-phase analytical expressions of equations (3-62b), (4-35) and (4-36). Low capacitor RMS currents can be achieved by increasing the number of phases and working at a duty ratio $D \approx {}^{1}/_{\mathrm{N}}, {}^{2}/_{\mathrm{N}}, {}^{3}/_{\mathrm{N}} \ldots\ldots {}^{(\mathrm{N}-1)}/_{\mathrm{N}}$. Reduction in capacitor size will have advantages such as reduction in cost and size of the converter.

7.3.3 Output current and voltage ripple

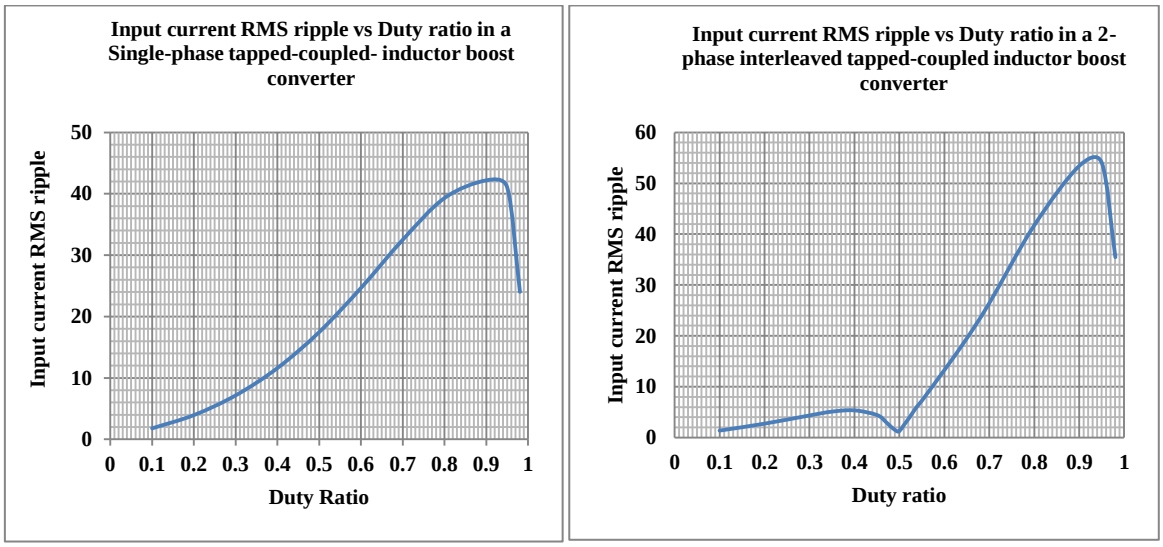
The output current and voltage ripples are lower in the converters with an even number of phases as compared to those with odd number of phases. This can be seen from waveforms in Figures 7.1, 7.2, 7.5 and 7.6, and the summarised values in tables 7.1 and 7.2. Considering a four-phase and a five-phase converter, the four-phase has an output voltage ripple of 0.073V while the five-phase has an output voltage ripple of 0.16V. The output current ripple is 0.45mA and 1mA for the four-phase and five-phase converters respectively. This shows that the converters with even number of phases yield better performance in terms of output ripple cancellation. The six-phase converter has the lowest output ripple with values of 0.036V and 0.22mA for the voltage and current respectively.

The single-phase converter has very high ripple values of 5V and 31mA for the output voltage and current respectively compared to the interleaved converters. Hence, by interleaving, the output characteristics of the tapped-coupled-inductor boost converter are improved, with the better performance being achieved by paralleling the phases and operating at a duty ratio where the best ripple overlap is achieved.

7.3.4 Input current RMS ripple

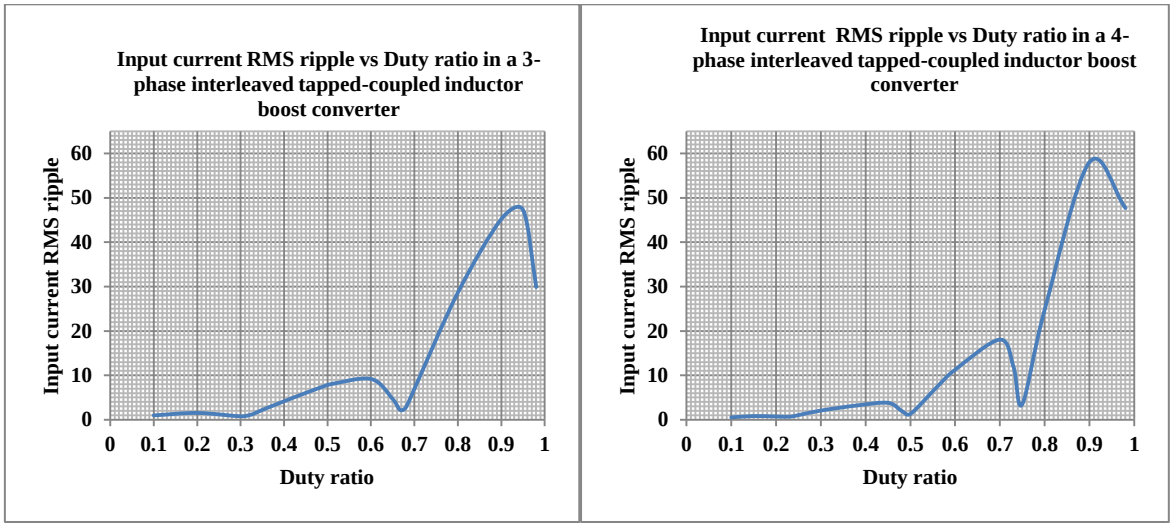
The input RMS current ripple is shown in current waveforms of Figures 7.3 and 7.7 and the tables 7.1 and 7.2 summarizing the values. It is shown that for the simulated input voltage of 40V, the converters with an even number of phases have lower values of input RMS current ripple compared to those with odd number of phases. The five-phase interleaved converter has a ripple value of 4.37A while a two-phase converter has a ripple of 3.39A. The six-phase converter has the lowest value of input ripple with a value of 1.34A while the single-phase converter has the highest ripple with a value of 25.05A. The extremely high value of input ripple in the single-phase converter as compared to the interleaved cases shows the advantages of interleaving. This is in agreement with the derived theoretical expressions for the single- and two-phase converters. Employing an even number of phases however presents converters with better input ripple characteristics for the given set of input and output voltage.

Figures 7.9 to 7.11 show plots of input RMS current ripple against duty ratio for the six boost converters with tapped-coupled-inductors. These plots were obtained for variable output power and voltage with a turns ratio, *n* of 10 between tapped-coupled-inductor.



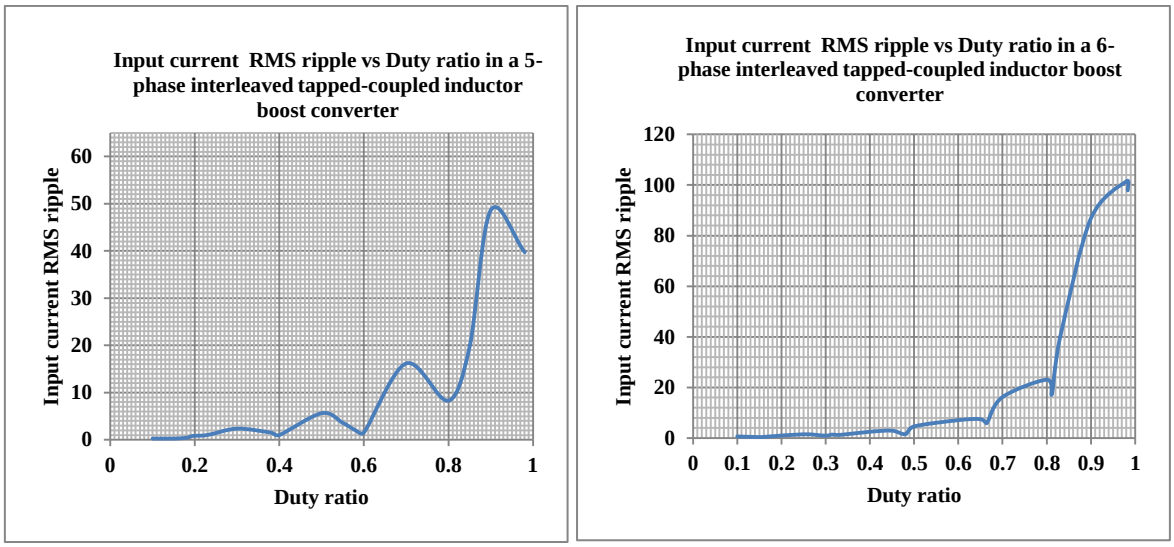
(a) single-phase (b) two-phase

Figure 7.9. Input RMS current ripple against duty ratio for single- and two-phase tapped-coupled-inductor boost converters.



(a) three-phase (b) four-phase

Figure 7.10. Input RMS current ripple against duty ratio for three- and four-phase tapped-coupled-inductor boost converters.



(a) five-phase (b) six-phase

Figure 7.11. Input current RMS ripple against duty ratio for five-and six-phase tapped-coupled-inductor boost converters.

From Figures 7.9 to 7.11, it is shown that ripple reduction in interleaved tapped-coupled-inductor boost converters is a function of phase number, N, and the duty cycle.

The degree of ripple overlap is a function of the duty ratio. Minimum ripple is obtained whenever the duty ratio, $D \approx {}^{1}/_{N}, {}^{2}/_{N}, {}^{3}/_{N} \ldots\ldots {}^{(N-1)}/_{N}$. Complete ripple cancellation can however not be achieved in the interleaved tapped-coupled-inductor boost converters. This is an inherent feature of these converters which is due to the nature of the phase current waveforms. Ripple is always lower at small duty ratios and it increases nonlinearly with duty ratio. For operation with $D \approx 0.5$, a converter with even number of phases is preferable. Ripple performance is always bad at high duty ratios irrespective of number of phases.

Considering a variable input voltage where the duty ratio varies between 0.4 and 0.65, thus avoiding an extreme duty ratio, the six-phase converter operates with the least input RMS current ripple of 7.5A at a duty ratio of 0.65 as shown if Figure 7.11(b). For the same range of duty ratio, the single-phase converter has a ripple of 28.5A as shown in Figure 7.9(a). This demonstrates that increasing the number of phases in the multi-phase tapped-coupled-inductor boost converters leads to reduced input and output ripple. Once the converter topology is selected, that is, the number of phases, a suitable turns ratio should hence be selected which enables operation at a duty ratio range with minimal ripple.

There has to be a trade-off between choice of turns ratio and duty ratio. For a given boost ratio, a choice of a low turns ratio requires use of high duty ratio and vice-versa.
Researchers in [28] made an observation that due to the tapped inductor, the total ripple in the input current of single-phase tapped-inductor boost converter increases with higher load currents unlike in a conventional boost converter. In this thesis, further research was carried out. This allowed verification of this observation by determining the input current ripple as load changes, at a fixed duty ratio for the six tapped-coupled-inductor boost converters. Analytical verification was done for single-and two-phase converters.
Figure 7.12 shows input current ripple as a function of load for the six converters at a fixed duty ratio of 0.4944.

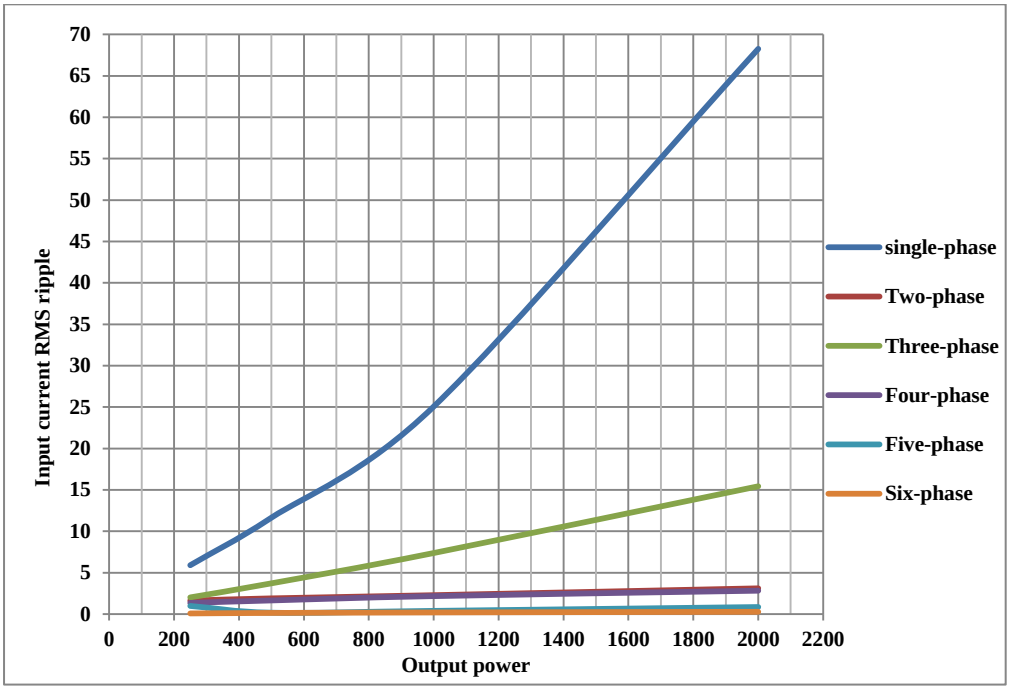


Figure 7.12. Input current RMS ripple against power characteristics

Figure 7.12 confirms that ripple in boost converters with tapped-coupled-inductors increases as load increases. Although the chosen duty ratio favours even number of phases, it is clear that the rate of increase in ripple value with load decreases as the number of phases increase. The proposed interleaved tapped-coupled-inductor boost converter therefore will have better ripple performance even at high power levels compared to a single-phase tapped-coupled-inductor boost converter.

7.3.5 Efficiency vs. Power

Figure 7.13 shows the efficiency-power characteristics of the six boost converters with tapped-coupled-inductors obtained from simulations. The relationship between the converter efficiency as the number of phases increase is shown. The effect of switching losses is ignored in all the converters. The output load was varied for each converter at a constant output voltage, hence varying the output power and duty ratio, while maintaining the same boost ratio.

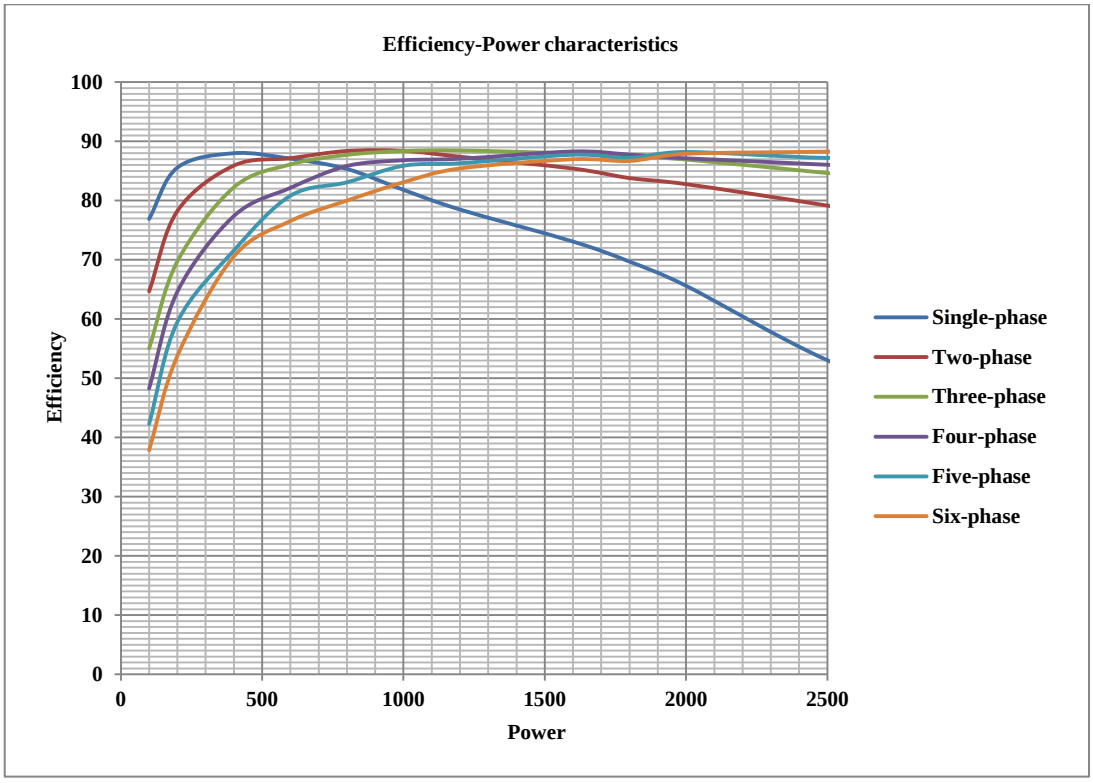


Figure 7.13. Efficiency against Power characteristics for the six converters.

It is observed from Figure 7.13 that the efficiency of the tapped-coupled-inductor boost converters increases nonlinearly with an increase in the interleaved phases at high power levels. There is however a decrease in efficiency in all the boost converters as the output power is increased. This decrease in efficiency is most significant in the single-phase converter and the rate of decrement decreases with increase in the number of phases. Efficiency curves at high power flatten as the number of phases increase.

Figure 7.13 also shows that at very low output power, the efficiency in all the converters is low and increases with load, attains a maximum and then decreases as the output power is further increased. The single-phase converter has the highest efficiency at very low output power. This shows that interleaving the tapped-coupled-inductor boost converter makes it more suitable for high power applications where the efficiency is improved by increasing the number of phases. The decrease in the efficiency at high power levels is due to the

increase in the peak and RMS values of currents in the converters resulting to higher copper, switching and conduction losses.

For variable power operation, variable number of phases should be considered to ensure high efficiency at all times. A converter that can deliver a maximum efficiency at a specific output power can therefore be designed, which is not necessarily the maximum power. Digital control allows such a system to be realised with ease.

7.3.6 Effects of input voltage variations

The effects of input voltage variations on performance were evaluated in all the six boost converters with tapped-coupled-inductors. The input voltage was varied from 35V to 45V, to simulate voltage variations encountered in PV panels, for example, at a constant output power and voltage. Values of input RMS current ripple and output capacitor RMS current were obtained and plotted against the input voltage variation as shown in Figures 7.14 to 7.17.

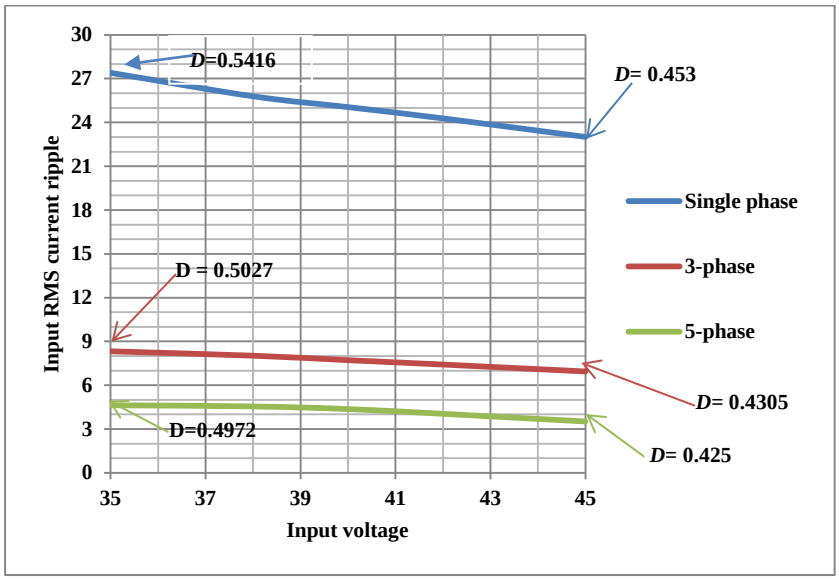


Figure 7.14. Input RMS current ripple against input voltage variation for converters with odd number of phases.

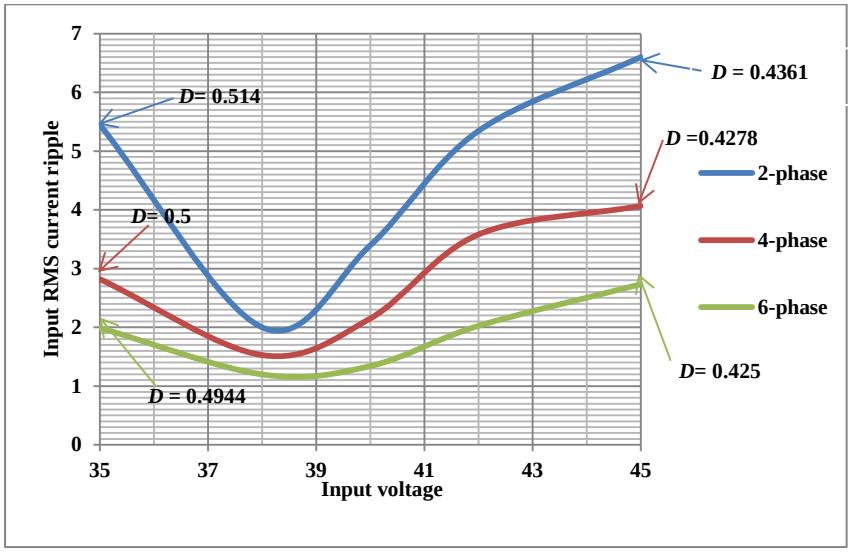


Figure 7.15. Input RMS current ripple against input voltage variation for converters with even number of phases.

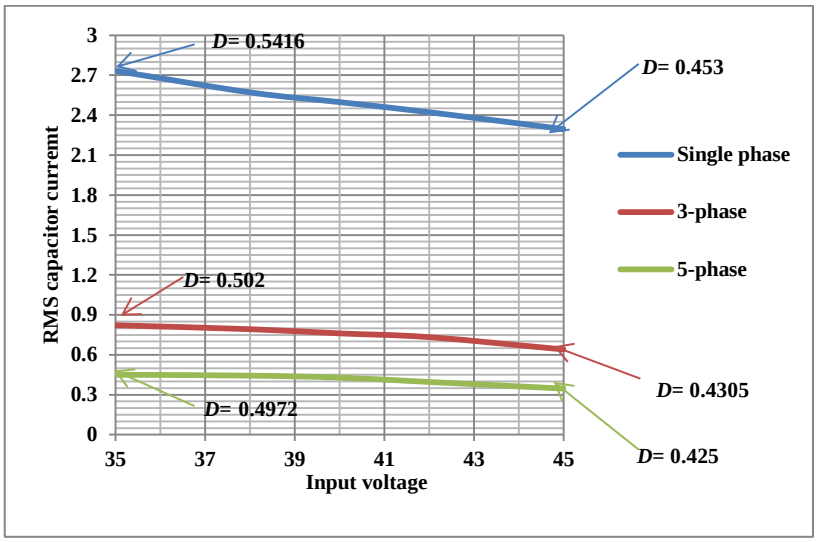


Figure 7.16. Capacitor RMS current against input voltage variation for converters with odd number of phases.

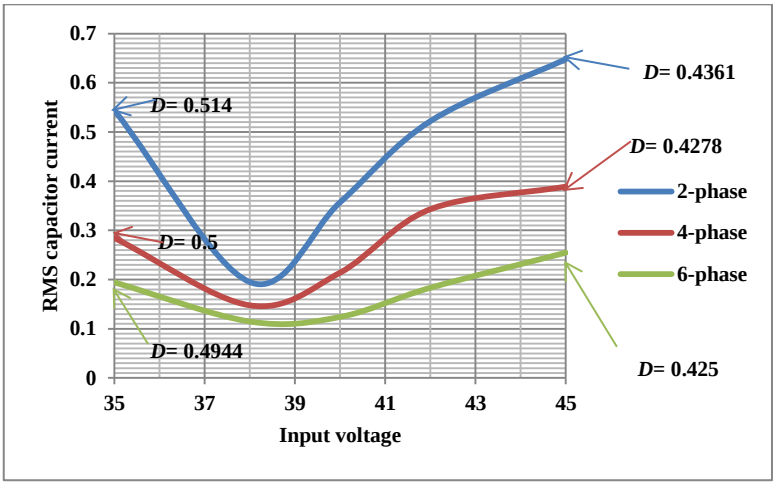


Figure 7.17. Capacitor RMS current against input voltage variation for converters with even number of phases.

From Figures 7.14 to 7.17, it is evident that the tapped-coupled inductor converters with odd number of phases perform in a manner that is very distinct from that for converters with even number of phases. The converters with odd number of phases have similar input ripple and output capacitor characteristics and likewise for converters with even number of phases. As shown in Figures 7.14 and 7.16, the input current ripple and the RMS capacitor current decreases almost linearly as the value of input voltage increases in the converters with odd number of phases with the single-phase converter having the highest input ripple and capacitor current values. This decrease is attributed to the value of duty ratio at the input voltage range. The duty ratio varied from 0.541 to 0.453, 0.502 to 0.4305 and 0.497 to 0.425 in the single-phase, three-phase and five-phase converters respectively for input voltage range considered.

Matching these duty ratios with Figures 7.9(a), 7.10(a) and 7.11(a) shows a decreasing slope towards duty ratios of ≈1, ≈1/N and ≈2/N for the single-phase, three-phase and five-phase converters respectively. In the converters with even number of phases however, the input current ripple and the capacitor RMS current decrease with an increase in the input voltage up to a minimum value at about 38V and then increase nonlinearly with increase in voltage, with the two-phase converter with the highest values. The 38V input voltage correspond to a duty ratio of 0.48 ≈1/N, 0.4777 ≈ 2/N and 0.4722≈3/N in the two-phase,

four-phase and six phase respectively. These duty ratios lie close to points of minimal ripple in the converters with even N which explains the minimal ripple and capacitor current. It is hence noted that increasing the number of phases generally decreases both the input current ripple and the RMS capacitor current. For the chosen combination of turns ratio and duty ratio, converters with an even number of phases outperform those with an odd number of phases when considering input and capacitor current ripple.

7.4 CHAPTER CONCLUSION.

In this chapter, six DC-DC converters, starting with a single-phase to a six-phase tapped-coupled-inductor boost converter are simulated for performance analysis and comparing their suitability for PV application.

From these results, it can be noted that the interleaved tapped-coupled-inductor boost converter is suitable for applications with variable input such as PV and wind energy applications. Depending on the range of input voltage variation, which then determines the duty ratio range, one can select whether to use a converter with odd N or even N since each of them presents different performance characteristics. Moreover, by using digital control, which has an advantage of improved sensitivity to variations, an appropriate duty ratio that results to the best performance can be maintained when voltage and load varies. In both converters with odd or even N, the converter with the highest N has the best performance at the expense of more components.

Figures 7.9 to 7.11 can be used to determine the converter suitable for a given voltage range. The duty ratio range can be adjusted by selecting a suitable turns ratio between the coupled inductors to match the desired performance. A high coupling coefficient should be maintained to reduce the leakage inductance and ensure a high boost ratio. The simulation and analytical results are in agreement in the case of single-and two-phase converters.

CHAPTER 8 PRACTICAL RESULTS

To verify the theoretical analyses and the simulations in the previous chapters, a 1kW prototype of a two-phase interleaved tapped-coupled-inductor boost converter designed in chapter 5 was built and tested. The practical results verify the high boost capabilities of the tapped-coupled-inductor boost converter and the advantages of interleaving, hence the suitability of this converter in PV applications. A comparison of the single-phase and the two-phase interleaved tapped-coupled-inductor boost converters were done practically. A single-phase converter was tested by powering only one of the interleaved phases. For both converters, a duty ratio of 0.55 was maintained. To test the converters at two different power levels, measurements were taken at an input voltage of 21V and 36V and results presented in tables 8.1 and 8.2.

The switches S_1 and S_2 used are the 300V, $I_{Tc=25°C}$ (I_{D25}) of 69A, MOSFET IXFT 69N30P with $R_{ds(on)}$ of 49mΩ at I_D=0.5 $I_{D25.}$ The diodes used are the 15A, 1200V, RHRP15120 hyperfast diodes. The turns ratio between the coupled inductors is 10. In tapped-coupled-inductor boost converters, the boost ratio and efficiency are directly proportional to the coupling coefficient as explained in section 3.1.1. It was therefore necessary to achieve a high coupling coefficient when winding the tapped coupled-inductors hence minimizing the leakage inductance. To achieve this, the two coupled inductor windings were alternated such that the first inductor winding was sandwiched in between the second inductor winding, which had more turns, as shown in Figure 8.1.

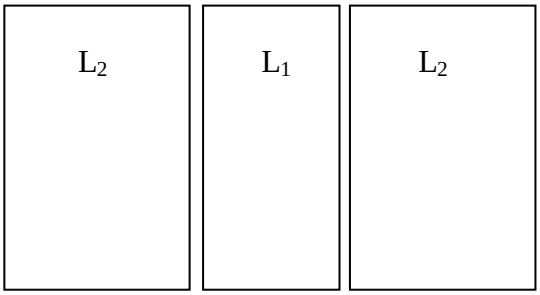


Figure 8.1. Alternating the coupled inductor winding to reduce leakage inductance.

Practically, a coupling coefficient of 0.99 was achieved. Figure 8.2 shows the practical gating signals used to switch the two MOSFETs'. For the two interleaved converters, the signals have an 180^0 phase-shift, equal duty ratio and same switching frequency.

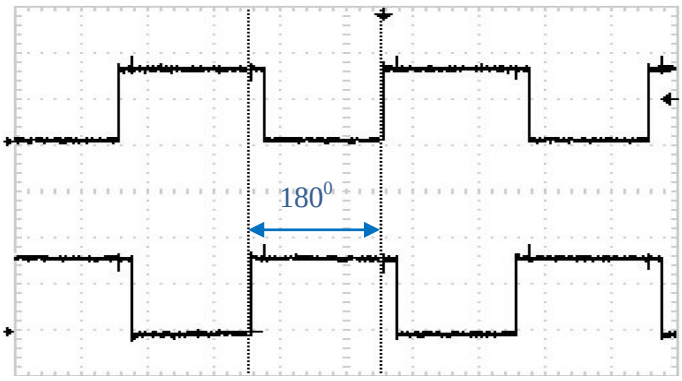
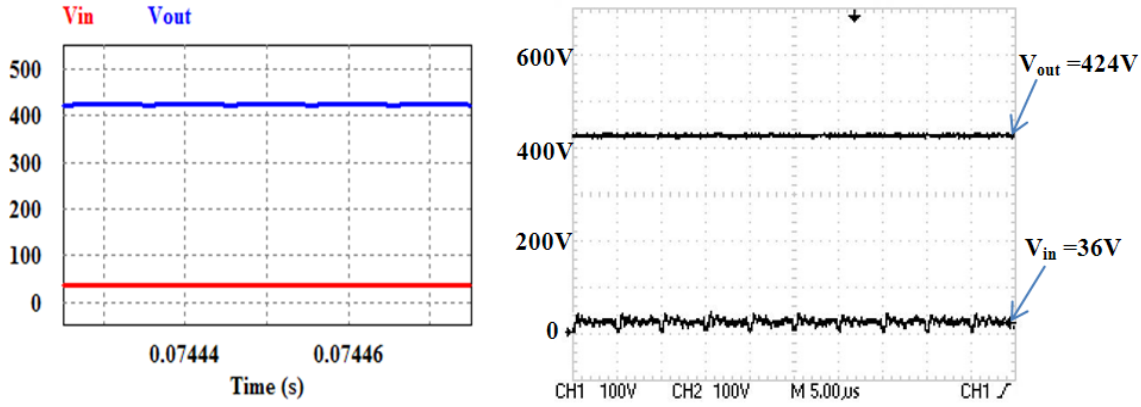


Figure 8.2. PWM gating signals for the two interleaved converters.

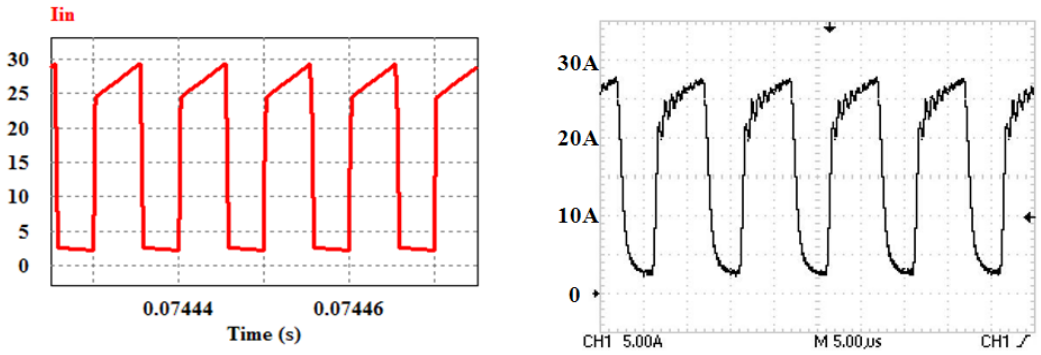
8.1 SINGLE-PHASE TAPPED-COUPLED-INDUCTOR BOOST CONVERTER

This section presents the simulated and practical waveforms from a single-phase tapped-coupled-inductor boost converter with an input voltage of 36V. Input and output voltage, input current and capacitor current waveforms are presented.



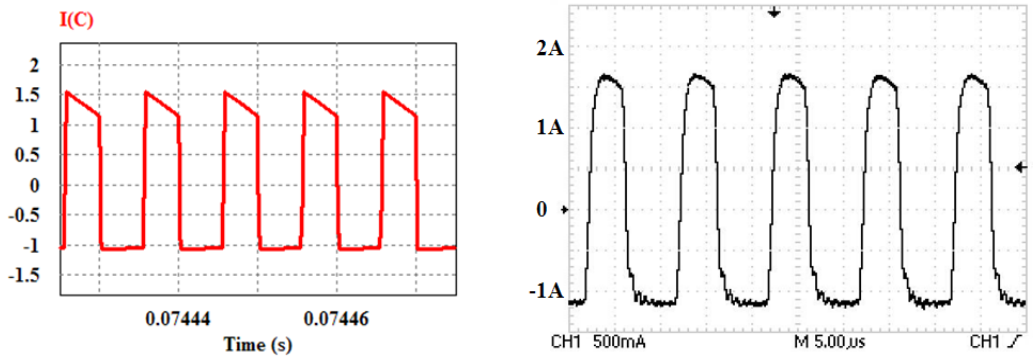
(a) Simulated (b) Experimental

Figure 8.3. Input and Output voltage waveforms.



(a) Simulated (b) Experimental

Figure 8.4. Input current waveforms.

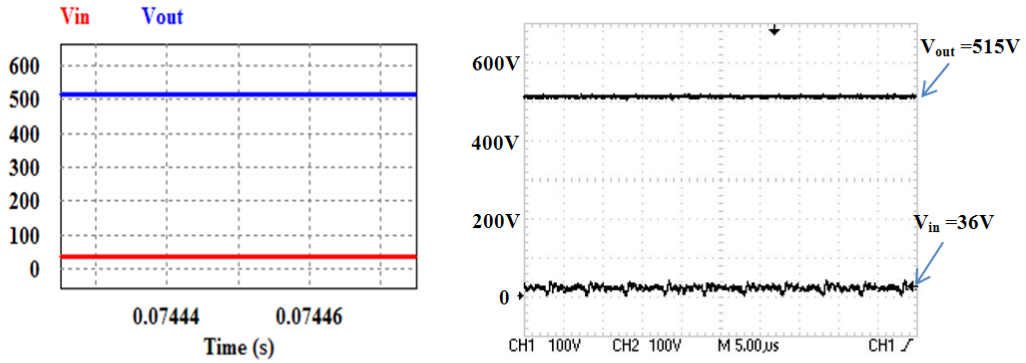


(a) Simulated (b) Experimental

Figure 8.5. Capacitor current waveforms.

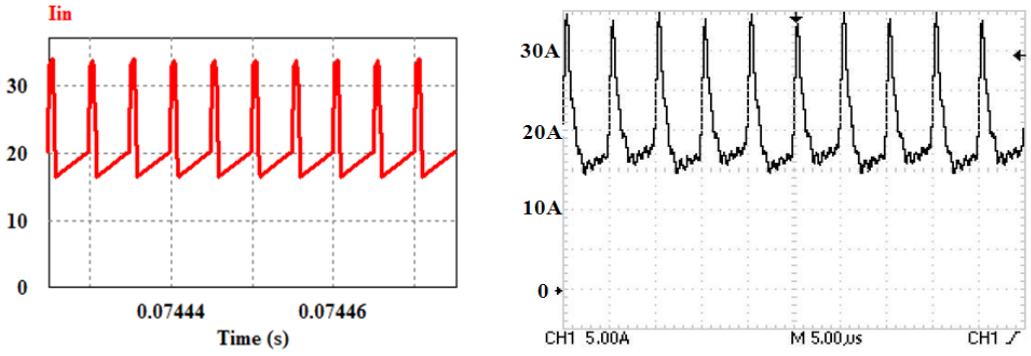
8.2 TWO-PHASE INTERLEAVED TAPPED-COUPLED-INDUCTOR BOOST CONVERTER.

This section presents the simulated and practical waveforms from a two-phase interleaved tapped-coupled-inductor boost converter with an input voltage of 36V. Waveforms of the input and output voltage, input current, phase currents, capacitor current and switch voltage are presented.



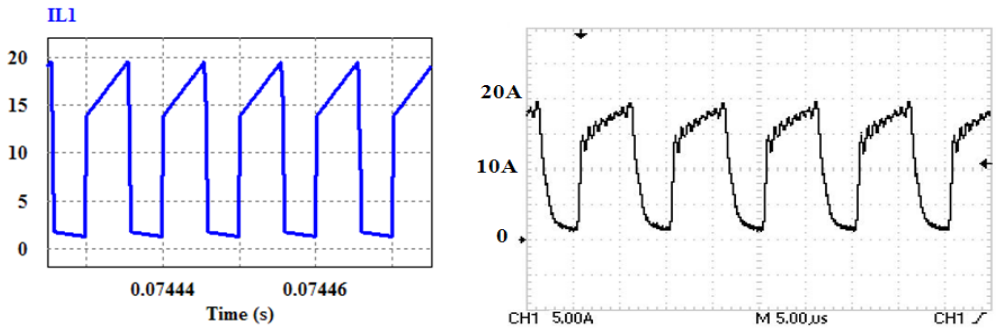
(a) Simulated (b) Experimental

Figure 8.6. Input and Output voltage waveforms.



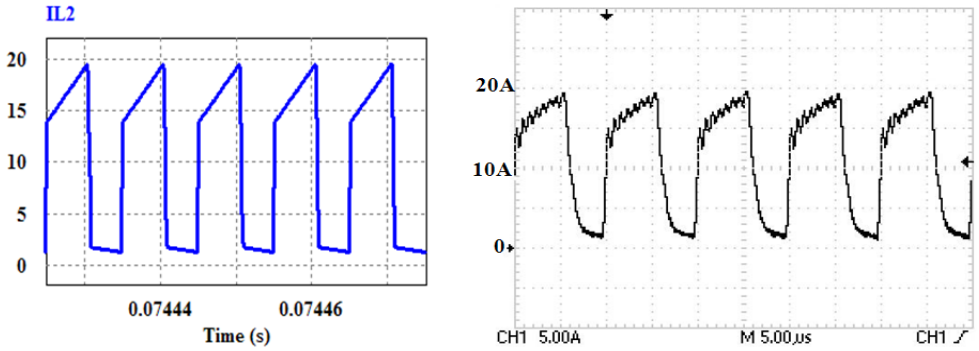
(a) Simulated (b) Experimental

Figure 8.7. Input current waveforms.



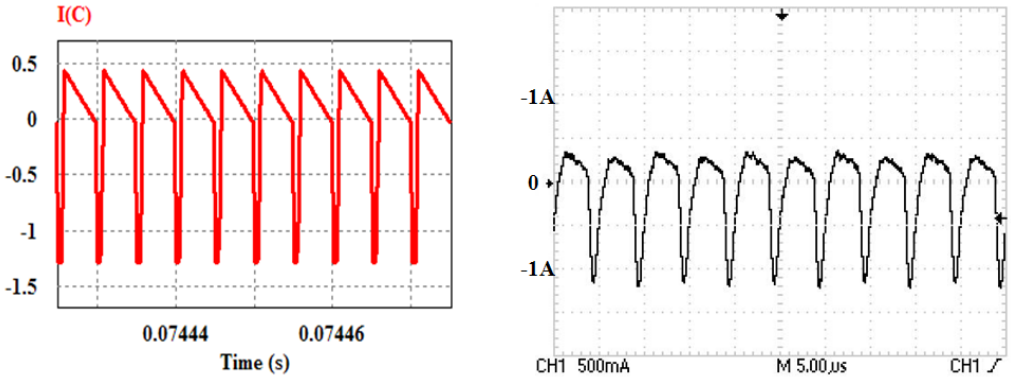
(a) Simulated (b) Experimental

Figure 8.8. Phase-one current waveforms.



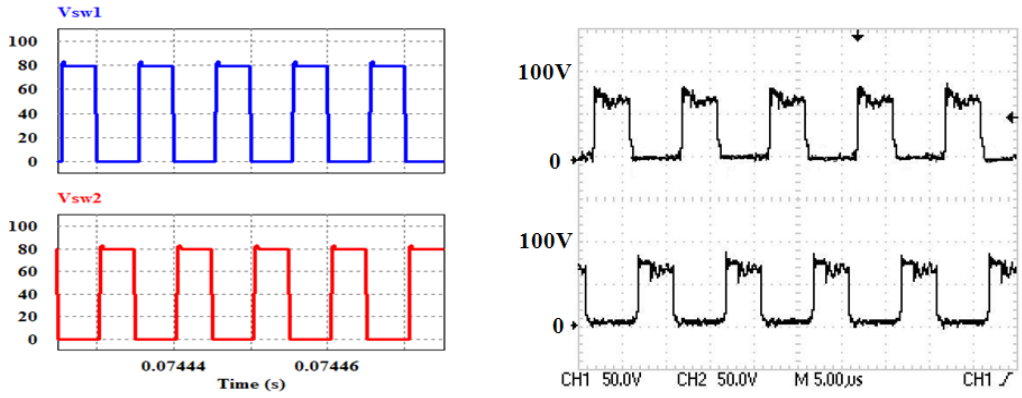
(a) Simulated (b) Experimental

Figure 8.9. Phase-two current waveforms.



(a) Simulated (b) Experimental

Figure 8.10. Capacitor current waveforms.



(a) Simulated (b) Experimental

Figure 8.11. Simulated and experimental switch voltage on phases one and two.

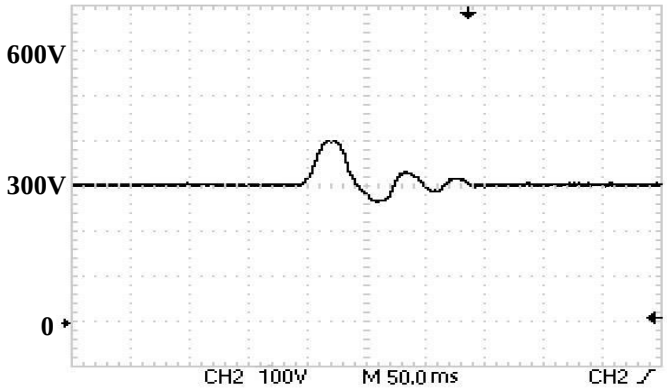


Figure 8.12. Experimental output voltage response under a step load variation with an input voltage of 21V.

8.3 DISCUSSION OF THE PRACTICAL RESULTS

Different parameter values obtained from the experimental waveforms are summarized in table 8.1 and 8.1. Both converters were tested at a duty ratio of 0.55.

TABLE 8.1

Comparison of different performance parameters for the experimental single-phase tapped-coupled-inductor boost converters

Output power	V_{in}	$I_{in,rms\ ripple}$	$I_{in,pk-pk}$	$I_{c,rms}$	V_{out}
150W	21V	7.1A	15.6A	0.68A	245V
450W	36V	11.9A	27.1A	1.18A	424V

TABLE 8.2

Comparison of different performance parameters for the experimental two-phase tapped-coupled-inductor boost converters

Output power	V_{in}	$I_{in,rms\ ripple}$	$I_{in,pk-pk}$	$I_{c,rms}$	V_{out}
225W	21V	2.96A	10.1A	0.21A	300V
663W	36V	4.71A	17.42	0.35A	515V

8.3.1 Proposed converter loss and efficiency analysis.

MOSFET switching and conduction losses, diode conduction losses, inductor copper loss snubber resistor losses and efficiency of the tested experimental converters were calculated and tabulated in tables 8.3 and 8.4. Power loss in the capacitors and the reverse recovery loss in the diodes were ignored in the calculations. Tables 8.3 and 8.4 show results from the single-phase and the two-phase tapped-coupled-inductor boost converters respectively.

Using these calculated power loss values, the converter efficiency can be calculated as:

$$Efficiency = 1 - \frac{Total\ Losses}{Output\ power\ of\ converter} \tag{8-1}$$

Table 8.3. Single-phase converter calculated experimental losses

Output power	Copper loss	Switch conduction loss	Switching loss	Snubber loss	Diode conduction loss	Total loss	Efficiency
150W	0.62W	6.9W	4.6W	20.1W	0.79W	33W	78%
450W	1.4W	15W	10.03W	43.9W	1.72W	72W	84%

Table 8.4. Two-phase converter calculated experimental losses

Output power	Copper loss	Switch conduction loss	Switching loss	Snubber loss	Diode conduction loss	Total loss	Efficiency
225W	0.76W	7.86W	8.7W	34.5W	1.1W	52.9W	76.45%
663W	1.48W	15.31W	16.9W	67.24W	2.134W	103.1W	84.45%

From Figures 8.3 to 8.11, the correlation between the simulation and experimental waveforms is clearly evident. Figure 8.3 shows the experimental and simulated input and output voltage waveforms in a single-phase tapped-coupled-inductor boost converter. It is shown that with an input voltage on 36V, an output voltage of 424V is achieved at a duty ratio of 0.55. This presents a voltage boost of about 11.7 times which confirms the high boost capabilities of tapped-coupled inductor boost converters with out an extreme duty ratio. Applying the same input voltage of 36V, at the same duty ratio, in the two-phase tapped-coupled-inductor boost converter results in an output voltage of 515V.

This translates into a higher boost ratio of about 14.3 times which is much higher than that of the single-phase converter. This confirms the higher boost capabilities with increase in the number of interleaved phases in the tapped-coupled-boost converter. This is shown in figure 8.6 where the simulated and experimental input and output voltage waveforms in a two-phase tapped-coupled-inductor boost converter are presented.

Simulated and practical input current in the single-phase and two-phase converter are shown in Figure 8.4 and 8.7 respectively. Increase in the input current ripple frequency with an increase in the phase number is evident. Compared to the single-phase converter, the two-phase converter's ripple frequency is doubled. From the input current waveforms and the tabulated values in tables 8.1 and 8.2, ripple supression is evident in the two-phase converter compared to the single-phase converter. Although lower average current flows through the single phase converter compared to the two-phase converter, higher current ripple values are shown to exist in the single-phase converter.

With an input voltage of 21V, the single-phase converter has a input RMS current ripple of 7.1A and a peak-to-peak ripple of 15.6A. These values are much higher than 2.96A and 10.1A RMS and peak-to-peak ripple obtained in the two-phase converter. Like wise, with an input voltage of 36V, the single-phase converter has a input RMS current ripple of 11.9A and a peak-to-peak ripple of 27.1A. These values are much higher than 5.05A and 17.42A RMS and peak-to-peak ripple obtained in the two-phase converter. In the two-phase converter the input current is shared into two phase currents shown in figure 8.8 and 8.9.

The capacitor current in the single-phase and two-phase converters are shown in figures 8.5 and 8.10 respectively. As tabulated in tables 8.1 and 8.2, it is shown experimentally that lower capacitor RMS currents are achieved in the two-phase converter compared to the single-phase converter. The switch voltage in the two-phase converter is shown in figure 8.11 where reduction of the switch voltage stress is demonstrated. The RCD snubber implemented in the designed converter reduces the voltage spikes introduced by the leakage inductance.

The voltage stress on the two switches is reduced to about 83V, which is far lower than the output voltage of 515V. Low –voltage and high performance devices can hence be used to

reduce the conduction losses.The RCD snubber used is however lossy and the leakage energy is dissipated through the snubber resistor.

Calculated losses in tables 8.3 and 8.4 show that snubber loss account for 61% and 65% of total converter loss in the single-phase and two-phase tapped-coupled-inductor boost converters respectively. This lowers the conversion efficiency in the two converters. Use of active-clamp lossless snubbers, which recycles the leakage energy, can however be used to improve the conversion efficiency at the expence of topology complexity.

Figure 8.12 shows the output voltage response in the two-phase tapped-coupled-inductor boost converter under a 25% step change in load. An overshoot of about 33.3% is experienced before the voltage goes back to its steady-state value of 300V.

8.4 CHAPTER CONCLUSION.

In this chapter, a prototype of a single and two-phase interleaved tapped-coupled-inductor boost converter designed in chapter 5 is built and tested. A comparison of the two converters is done practically and waveforms of each converter presented.

These practical results comparing the single-phase and the two-phase tapped-coupled-inductor boost converter verify the effectiveness of the proposed multi-phase tapped-coupled-inductor boost converter. It is shown practically that this low cost and easy to implement multi-phase converter achieves high voltage boost capabilities, reduced input current ripple and lower capacitor RMS current values. These results agree with the simulations and analyses. Experimental results verify that combining the advantages of tapped-coupled-inductors and interleaving makes this novel converter suitable for high power PV applications where current with very little ripple component needs to be drawn and a high voltage boost is required.

CHAPTER 9 CONCLUSION AND PROPOSAL FOR FUTURE WORK

9.1 CONCLUSION

The most important constraints of a PV energy generator is to obtain a high voltage gain and sourcing of low distortion reactive power by drawing current with less harmonics. The conversion efficiency of PV arrays is in general low. This work addresses the integration of a novel power electronics converter suitable for high power PV applications where high voltage boost ratios are required and also sourcing of very low distortion reactive power from the PV source is necessary. Other methods of boosting the PV voltage like connecting panels in series and use of other converter topologies were discussed in chapter 2, where their limitations were explained. The most important conclusions drawn from this research are summarised by the thesis research questions:

I. *How can the output voltage of a small PV array be boosted to high values using a DC-DC converter without extreme duty cycles?*

A boost converter utilising switch-tapped-coupled inductors is shown analytically, through simulations and experimentally to provide a high boost ratio, without an extreme duty ratio, by selecting a turns ratio. Operation with low duty ratios in this converter hence eliminate reverse-recovery problems and reduce EMI problem. Furthermore, low rated devices can be used which will translate to an improved conversion efficiency. The proposed multi-phase converter topology is derived by interleaving single-phase tapped-coupled-inductor boost converters. In the proposed multi-phase tapped-coupled-inductor boost converter, the boost ratio is shown to increase non-linearly with number of phases. This is attributed to current sharing in the phases, hence reduction in RMS and peak current values per phase which translate to reduced voltage drops and losses in the converter.

By employing the proposed interleaved tapped-coupled-inductor boost converter to PV applications, a solar array with few series connections is required to achieve high DC voltages which can be integrated to the grid through an inverter or used for a high power application. Having few series connections in the array also saves the overall cost of a PV solar project by a great margin since one of the biggest expenses in such a project is the cost of the PV panels.

II. How can the input and output ripple in the current and voltage be reduced, hence a reduced reactive power demand and an increase in the efficiency of a PV system?

It is shown in the thesis that due to interleaving of the tapped-coupled-inductor boost converter, there is an increase in the ripple frequency with an increase in the number of phases. This leads to reduction in the size of filter components hence a higher power density, improved transient response and cost reduction in the proposed converter. It is shown that ripple reduction in interleaved tapped-coupled-inductor boost converters is a function of phase number and the duty cycle. Minimum ripple is obtained whenever the duty ratio, $D \approx {}^{1}/_{\mathrm{N}}, {}^{2}/_{\mathrm{N}}\ {}^{3}/_{\mathrm{N}} \ldots\ldots {}^{(\mathrm{N}-1)}/_{\mathrm{N}}$. This means that the number of points where minimum ripple is obtained increases as the number of phases increases. Complete ripple reduction can however not be achieved in the interleaved tapped-coupled-inductor boost converters. This is an inherent feature of these converters which is due to the nature of the phase current waveforms. For all the tapped-coupled-inductor boost converters however, ripple is always lower at small duty ratios and increases nonlinearly with duty ratio. This is an advantage in that by selecting a suitable turns ratio and number of phases, high boost ratios as well as low ripple in both the input and output can be achieved at a low duty ratio.

It is also shown in this thesis that ripple in the tapped-coupled-inductor boost converter increases with load unlike in a conventional boost converter. The rate of ripple increase with load is shown to be higher in a single-phase converter compared to the interleaved converters.

III. Is it possible to obtain a converter topology suitable for variable input voltage and power operation to be used in an application such as solar PV?

In the thesis, efficiency curves at different power levels are presented for the single-phase and multi-phase tapped-coupled-inductor boost converters. High operating efficiency at high voltage boost ratios and high power levels can be easily achieved in the proposed multi-phase converters. With an increase in the number of phases, the efficiency is shown improve as the power increases. This confirms the suitability of the multi-phase tapped-coupled-inductor boost converter as an interface with a PV source for high power applications. Furthermore, for a variable power application, a converter with variable number of phases should be considered to ensure high efficiency and low ripple at all times. This can be implemented by employing digital control.

Suitability of the proposed converter for variable input voltage sources such as PV was investigated in this thesis. It was shown that depending on the range of input voltage variation, which then determines the duty ratio range, one can select whether to use a converter with odd number of phases or even number of phases since each of them presents different performance characteristics. This will ensure that there is minimal ripple in both the output and the input and that maximum efficiency is achieved throughout the whole range of input voltage variation.

IV. What are the effects of the coupling coefficient on a boost converter with a tapped-coupled inductor?

It was shown analytically in this thesis that the voltage boost ratio is a function of the coupling coefficient. Previous studies on a tapped-inductor boost converter have on the contrary been assuming an ideal coupling which is not possible in practice. This research shows that boost ratio is directly proportional to the coupling coefficient. It is necessary therefore to wind the coupled inductors such that the leakage inductance is very low hence a high coupling coefficient, close to unity. A lossless snubber can also be used to recycle the minimal leakage energy hence improve the conversion efficiency. This research also

shows that input RMS current and input current ripple are directly proportional to the coupling coefficient.

V. How can a converter with an advantage of low output current ripple suitable for charging a battery from a PV source be obtained?

Output capacitor RMS current in the proposed converter is shown to be a function of number of phases and duty ratio. By selecting an appropriate number of phases, turns ratio, and a duty ratio that results to a minimal capacitor current, a small capacitor can be used. Furthermore, very low output current ripple can be achieved. These are important factors if the proposed converter is to be used for a battery charging applications where current with minimal ripple and a small or preferably no output capacitor is needed.

From this research, an article titled "Analysis and Design of a Single-Phase Tapped-Coupled-Inductor Boost DC-DC Converter" was published in the Journal of Power Electronics.

9.2 FUTURE WORK

In the performance analysis of the proposed converter, a lossy RCD snubber was used to suppress the switch voltage spikes. The use of this snubber led to a low conversion efficiency in the proposed converter. Research on the performance of the proposed converter can be extended by use of a less complex and low-cost way to clamp the switch voltage.

Furthermore, use of digital control to reconfigure the circuit as input or output operating conditions change to ensure optimal operation at all times can be done. This could involve sensing current on each string in the PV array or the load current.

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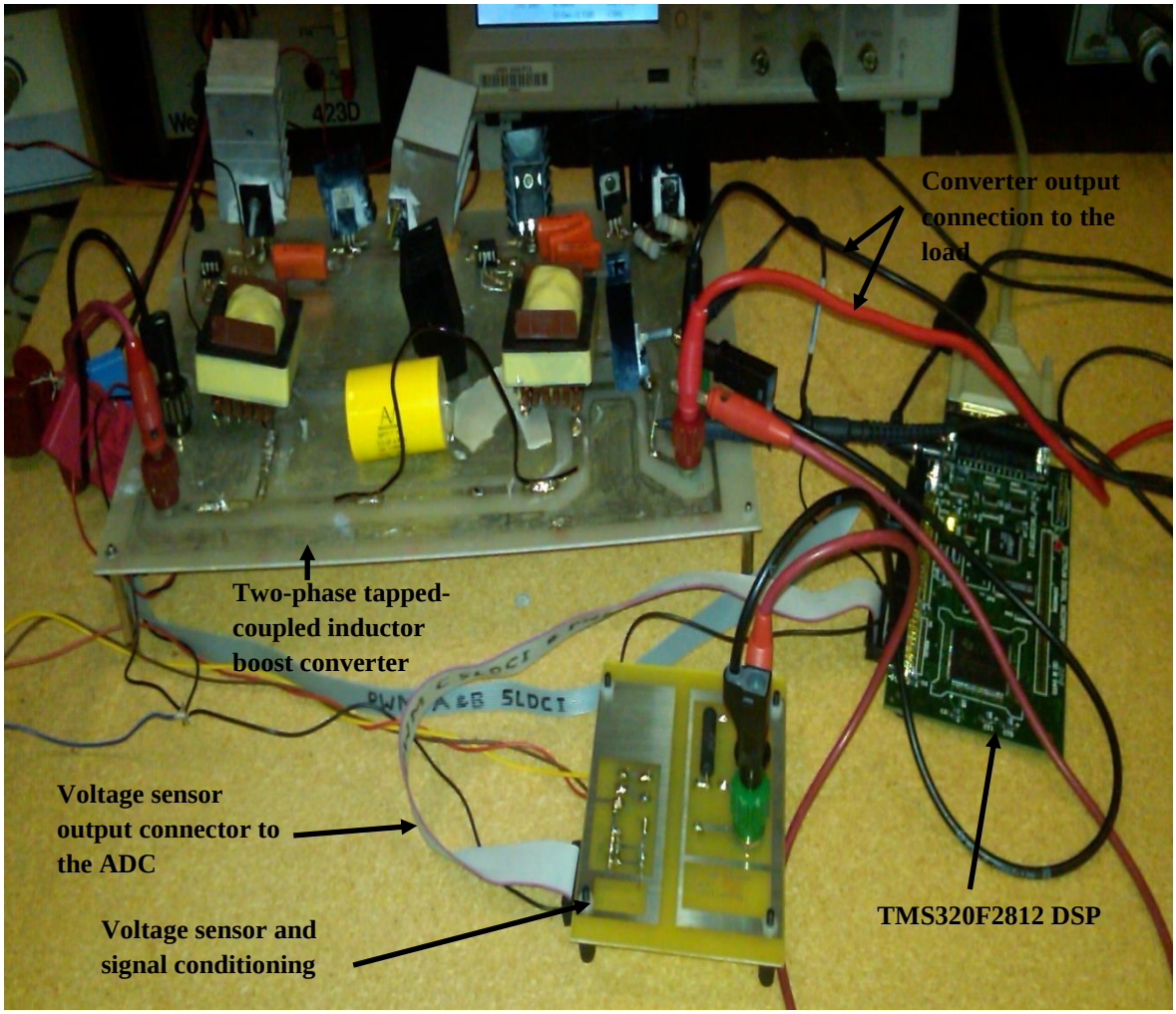
APPENDIX A CONVERTER PROTOTYPE AND DIGITAL CONTROLLER CODE

A.1 PROTOTYPE OF THE TWO-PHASE INTERLEAVED TAPPED-COUPLED-INDUCTOR BOOST CONVERTER.



A.2 DIGITAL CONTROLLER C-CODE.

```
//###########################################################################
Digital voltage-loop control implementation with the TMS320F2812
//###########################################################################
#define GLOBAL_Q 31
#include "DSP281x_Device.h"
#include "IQmathLib.h"
 b2 = _IQ26(10.27), b1 = _IQ26(-20.57), b0 = _IQ26(10.3), a2 = _IQ26(1.0), a1 = _IQ26(-
      1.0);
 max =_IQ24(0.6);
 min =_IQ24(0.0);
  _iq29 ADC_RESULT;
  _iq29 VREF = 357914120;   //0.666667 in IQ29
  _iq temp1;
_iq x_1, y_1, y_0, sum, temp, temp2;
_iq15 temp3;
_iq15 DIV_FACT= 49864;
_iq29 DIV_AVERAGE=268435456;
void Gpio_select(void);
void InitSystem(void);
```

```
interrupt void ADC_IIR_INT_ISR(void);     // Function Prototype for ADC result ISR

void main(void)

{

      InitSystem();            // Initialize the DSP's core Registers

      Gpio_select();           // Setup the GPIO Multiplex Registers

      InitPieCtrl();           // Function Call to init PIE-unit ( code : DSP281x_PieCtrl.c)

      InitPieVectTable(); // Function call to init PIE vector table ( code : DSP281x_PieVect.c )

      InitAdc();                     // Function call for basic ADC initialisation

    // re-map PIE - entry for GP Timer 1 Compare Interrupt

    EALLOW;  // This is needed to write to EALLOW protected registers

    PieVectTable.ADCINT = &ADC_IIR_INT_ISR;

    EDIS;    // This is needed to disable write to EALLOW protected registers

      // Enable ADC interrupt: PIE-Group1 , interrupt 6

    PieCtrlRegs.PIEIER1.bit.INTx6 = 1;       //INTx6

      //Enable EVA ti cmpr int in pie group

    PieCtrlRegs.PIEIER2.bit.INTx5 = 1;       //INTx6

      // Enable CPU INT1 which is connected to ADC interrupt:

  IER = 1;  //1

    // Enable global Interrupts and higher priority real-time debug events:

    EINT;   // Enable Global interrupt INTM
```

```
ERTM;   // Enable Global realtime interrupt DBGM


// Configure ADC
AdcRegs.ADCTRL1.bit.SEQ_CASC = 0;        // Dual Sequencer Mode
AdcRegs.ADCTRL1.bit.CONT_RUN = 0;        // No Continuous run, wait for trigger
AdcRegs.ADCTRL1.bit.CPS = 0;             // prescaler = 1
AdcRegs.ADCMAXCONV.all = 0x0001;         // Setup 2 conv's on SEQ1
AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0; // Setup ADCINA0 as 1st SEQ1 conv.// Assumes EVA Clock is already enabled in InitSysCtrl();
AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x8; // Setup ADCINB0 as 2nd SEQ1 conv.// Drive T1PWM / T2PWM by T1/T2 - logic
AdcRegs.ADCTRL2.bit.EVA_SOC_SEQ1 = 1;  // Enable EVASOC to start SEQ1// Polarity of GP Timer 1 Compare = Active low
AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 1;  // Enable SEQ1 interrupt (every EOEvaRegs.GPTCONA.bit.T1PIN = 1;
AdcRegs.ADCTRL3.bit.ADCCLKPS = 2;        // Divide HSPCLK by 3
AdcRegs.ADCTRL1.bit.SUSMOD=3;            // Emulation Suspend Mode= Stop Immediately
AdcRegs.ADCTRL2.bit.INT_MOD_SEQ1=0;      //interrupt request for every EOS ( =1 for every other EOS)

// Configure EVA
// Assumes EVA Clock is already enabled in InitSysCtrl();
```

```
// Disable T1PWM / T2PWM outputs
EvaRegs.GPTCONA.bit.TCMPOE = 1;  // Compare output enabled
    EvaRegs.GPTCONA.bit.T1PIN = 1;          // Polarity of GP Timer 1 Compare =
    active low
    EvaRegs.GPTCONA.bit.T1TOADC = 2;    // Enable EVASOC in EVA//set period
    interrupt flag
    EvaRegs.T1CON.bit.FREE = 0;                    // Stop on emulation
    suspend
EvaRegs.T1CON.bit.SOFT = 0;                    // Stop on emulation suspend
EvaRegs.T1CON.bit.TMODE = 1;            // Continuous-up/Down counting
    mode
EvaRegs.T1CON.bit.TPS = 0;                     // prescaler = 1
EvaRegs.T1CON.bit.TENABLE = 1;                 // enable GP Timer 1
    EvaRegs.T1CON.bit.TCLKS10 = 0;             // internal clock
    EvaRegs.T1CON.bit.TCLD10 = 0;              // Compare Reload when zero
    EvaRegs.T1CON.bit.TECMPR = 1;              // Enable Compare operation
    EvaRegs.T1PR =750;  //100kHz, TIPR=750
}
void Gpio_select(void)
{
    EALLOW;
    GpioMuxRegs.GPAMUX.all = 0x0;  // all GPIO port Pin's to I/O
```

```
    GpioMuxRegs.GPAMUX.bit.T1PWM_GPIOA6=1; // T1PWM active
    GpioMuxRegs.GPAMUX.bit.PWM1_GPIOA0=1;
    GpioMuxRegs.GPAMUX.bit.PWM2_GPIOA1=1;
        GpioMuxRegs.GPAMUX.bit.PWM3_GPIOA2=1;
        GpioMuxRegs.GPAMUX.bit.PWM4_GPIOA3=1;
    EvaRegs.ACTRA.all = 0x0965;
    EvaRegs.DBTCONA.all = 0x0000; // Disable deadband
    EvaRegs.COMCONA.all = 0xA601;
     EvaRegs.T1CNT = 0x0000;      // Timer1 counter
    GpioMuxRegs.GPADIR.all = 0x0;// GPIO PORT  as input
    GpioMuxRegs.GPAQUAL.all = 0x0;       // Set GPIO input qualifier values to zero
    EDIS;
}
void InitSystem(void)
{
        EALLOW;
        SysCtrlRegs.WDCR= 0x00E8;
          SysCtrlRegs.SCSR = 3;                          // Watchdog generates a RESET
        SysCtrlRegs.PLLCR.bit.DIV = 10;      // Setup the Clock PLL to multiply by 5
        SysCtrlRegs.HISPCP.all = 0x0; // Setup Highspeed Clock Prescaler to divide by 1
        SysCtrlRegs.LOSPCP.all = 0x2; // Setup Lowspeed CLock Prescaler to divide by 4
```

```
        // Peripheral clock enables set for the selected peripherals.
        SysCtrlRegs.PCLKCR.bit.EVAENCLK=1;
        SysCtrlRegs.PCLKCR.bit.EVBENCLK=0;
        SysCtrlRegs.PCLKCR.bit.SCIAENCLK=0;
        SysCtrlRegs.PCLKCR.bit.SCIBENCLK=0;
        SysCtrlRegs.PCLKCR.bit.MCBSPENCLK=0;
        SysCtrlRegs.PCLKCR.bit.SPIENCLK=0;
        SysCtrlRegs.PCLKCR.bit.ECANENCLK=0;
        SysCtrlRegs.PCLKCR.bit.ADCENCLK=1;
        EDIS;
}
interrupt void ADC_IIR_INT_ISR(void)
{
 ADC_RESULT =_IQ15(AdcRegs.ADCRESULT1);    //  ;_IQ15(0x3960)  ;
        ERROR = VREF - ADC_RESULT  ;
// perform the difference equation, result is y_0
sum= _IQmpy(a1, y_1);
sum= _IQmpy(a2, y_2);
sum= _IQmpy(b2,x_2)+sum ;
sum= _IQmpy(b1,x_1)+sum ;
```

```
y_0= _IQmpy(B_0,ERROR)+sum ;

 y_1 = y_0;   /* y(n-1) = y(n)   */

 y_2 = y_1;

 x_1 =ERROR;              //* x(n-1) = x(n)   */

 x_1 = x_2;

temp= y_0;

temp+=138936320;

if (temp >max)

 temp = max;

else if ( temp < min)

temp = min;

 else

 temp = temp;

temp2=temp;

temp3=_IQ15mpy(temp2,DIV_FACT);  // scaling of temp2 by multiplication by

                        //DIV_FACT, so that final value ranges

                        //btw 0- TIPR maximum value

EvaRegs.CMPR1 =temp3;

EvaRegs.CMPR2= 750-EvaRegs.CMPR1;// Obtaining two interleaved PWM signals

/*** Manage the ADC registers ***/
```

```
    AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;          // Reset SEQ1 to
    CONV00 state

    AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;        // Clear ADC SEQ1
    interrupt flag

    PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;    // Must acknowledge
    the PIE group

}
```