

**DESIGN METHODS FOR INTEGRATED SWITCHING-MODE POWER
AMPLIFIERS**

by

Mladen Božanić

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SUMMARY

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by

Mladen Božanić

Supervisor: Prof S Sinha
Department: Electrical, Electronic and Computer Engineering
University: University of Pretoria
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While a lot of time and resources have been placed into transceiver design, due to the pace of a conventional engineering design process, the design of a power amplifier is often completed using scattered resources; and not always in a methodological manner, and frequently even by an iterative trial and error process.

In this thesis, a research question is posed which enables for the investigation of the possibility of streamlining the design flow for power amplifiers. After thorough theoretical investigation of existing power amplifier design methods and modelling, inductors inevitably used in power amplifier design were identified as a major drawback to efficient design, even when examples of inductors are packaged in design HIT-Kits. The main contribution of this research is engineering of an inductor design process, which in-effect contributes towards enhancing conventional power amplifiers. This inductance search algorithm finds the highest quality factor configuration of a single-layer square spiral inductor within certain tolerance using formulae for inductance and inductor parasitics of traditional single- π inductor model. Further contribution of this research is a set of algorithms for the complete design of switch-mode (Class-E and Class-F) power amplifiers and their output matching networks. These algorithms make use of classic deterministic design equations so that values of parasitic components can be calculated given input parameters, including required output power, centre frequency, supply voltage, and choice of class of operation.

The hypothesis was satisfied for SiGe BiCMOS S35 process from Austriamicrosystems (AMS). Several metal-3 and thick-metal inductors were designed using the abovementioned algorithm and compared with experimental results provided by AMS. Correspondence was established between designed, experimental and EM simulation results, enabling qualification of inductors other than those with experimental results

available from AMS by means of EM simulations with average relative errors of 3.7 % for inductance and 21 % for the Q factor at its peak frequency. For a wide range of inductors, Q-factors of 10 and more were readily experienced. Furthermore, simulations were performed for number of Class-E and Class-F amplifier configurations with HBTs with f_t greater than 60 GHz and total emitter area of $96 \mu\text{m}^2$ as driving transistors to complete the hypothesis testing. For the complete PA system design (including inductors), simulations showed that switch-mode power amplifiers for 50Ω load at 2.4 GHz centre frequency can be designed using the streamlined method of this research for the output power of about 6 dB less than aimed. This power loss was expected, since it can be attributed to non-ideal properties of the driving transistor and Q-factor limitations of the integrated inductors, assumptions which the computations of the routine were based on. Although these results were obtained for a single micro-process, it was further speculated that outcome of this research has a general contribution, since streamlined method can be used with a much wider range of CMOS and BiCMOS processes, when low-gigahertz operating power amplifiers are needed. This theory was confirmed by means of simulation and fabrication in 180 nm BiCMOS process from IBM, results of which were also presented. The work presented here, was combined with algorithms for SPICE netlist extraction and the spiral inductor layout extraction (CIF and GDSII formats). This secondary research outcome further contributed to the completeness of the design flow.

All the above features showed that the routine developed here is substantially better than cut-and-try methods for design of power amplifiers found in the existing body of knowledge.

OPSOMMING

ONWERPMETODES VIR GEÏNTEGREERDE SKAKELMODUS- DRYWINGSVERSTERKERS

deur

Mladen Božanić

Studieleier:	Prof S Sinha
Departement:	Elektriese, Elektroniese en Rekenaaringenieurswese
Universiteit:	Universiteit van Pretoria
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Alhoewel baie tyd en hulpbronne spandeer word op die ontwerp van sender/ontvangers, word die ontwerp van drywingsversterkers dikwels voltooi met verspreide hulpbronne as gevolg van die tempo van die konvensionele ingenieursontwerpsproses en ook nie altyd op 'n metodiese manier nie, wat daartoe lei dat dit soms 'n iteratiewe proses raak.

In hierdie tesis word 'n navorsingsvraag gevra wat lei tot die ondersoek van die moontlikheid om die ontwerpsvloei van drywingsversterkers te optimeer. Na 'n sorgvuldige ondersoek van bestaande drywingsversterkerontwerpmetodes en modellering is die noodwendige gebruik van induktors geïdentifiseer as een van die groot struikelblokke in doeltreffende ontwerp, selfs wanneer induktorvoorbeelde deel vorm van die hoëprestasie-koppelvlakpakket (HIT-kit). Die grootste bydra van hierdie navorsing is die formulering van 'n ontwerpproses vir induktors, wat dan ook bydra tot die verbetering van konvensionele drywingsversterkers. Hierdie soekalgoritme vind die uitleg van 'n enkellaag- reghoekige spiraalinduktor met die hoogste kwaliteitfaktor binne sekere toleransies deur die formules vir die induktansie- en induktor- parasitiese komponente van die tradisionele enkel- π -induktormodel te gebruik. 'n Verdere bydrae van die navorsing is 'n stel algoritmes vir die volledige ontwerp van skakelmodus- (Klas-E en Klas-F) drywingsversterkers sowel as uitset-aanpasnetwerke. Hierdie algoritmes maak gebruik van die klassieke deterministiese ontwerpsvergelykings sodat die waardes van die parasitiese komponente bereken kan word vir gegewe insetparameters, wat die vereiste uitsetdrywing, werksfrekwensie, toevoerspanning en keuse van versterkerklas insluit.

Die hipotese is bewys in 'n SiGe BiCMOS S35-proses van Austriamicrosystems (AMS). Verskeie drie-metaal en dikmetaal-induktors is ontwerp deur bogenoemde algoritmes te gebruik en is vergelyk met die eksperimentele resultate wat deur AMS voorsien is.

Ooreenstemming is gevind tussen die ontwerp-, eksperimentele en elektromagnetiese simulasiereultate, wat die kwalifikasie van induktors, anders as dié waarvoor eksperimentele resultate van AMS beskikbaar is, moontlik maak deur die gebruik van EM-simulasies met 'n gemiddelde fout van 3.7 % vir die induktansie en 21 % vir die kwaliteitfaktor by die piekfrekwensie. Vir 'n wye verskeidenheid induktors is kwaliteitfaktors van 10 of meer gevind. Verder is simulaties gedoen vir 'n aantal Klas-E en Klas-F versterkerkonfigurasies met hetero-voegvlaktransistors met f_T groter as 60 GHz en 'n totale emitterarea van $96 \mu\text{m}^2$ as drywingstransistor om die hipotesetoetsing te voltooi. Vir die drywingsversterkstelontwerp (wat induktors insluit) het simulaties gewys dat skakelmodusdrywingsversterkers vir 'n 50Ω las by 'n 2.4 GHz-werksfrekwensie ontwerp kan word deur die geoptimeerde metode in hierdie navorsing te gebruik, in welke geval die uitsetdrywing ongeveer 6 dB minder is as waarvoor ontwerp is. Hierdie drywingsverlies is verwag, aangesien dit toegeskryf kan word aan die nie-ideale eienskappe van die drywingstransistor en die kwaliteitfaktorbeperkings van die geïntegreerde induktors, sowel as die aannames wat gemaak is in die berekening in die ontwerpproses. Alhoewel hierdie resultate vir 'n enkele mikroproses verkry is, is gevind dat hierdie navorsingsuitset steeds 'n algemene bydrae is deurdat die proses gebruik kan word vir 'n verskeidenheid CMOS- en BiCMOS-prosesse, wanneer laegigahertz-drywingsversterkers vereis word. Hierdie teorie is bevestig deur middel van simulatie en vervaardiging in die 180-nm BiCMOS-proses van IBM, waarvan die resultate ook voorgelê is. Die werk wat hier aangebied word, is gekombineer met algoritmes wat SPICE netlyste formuleer en ook die spiraalinduktoruitleg skryf in die CIF- en GDSII-formate.

Al bogenoemde kenmerke wys dat die roetine wat geformuleer is, aansienlik beter is as lukrake iteratiewe metodes vir drywingsversterkerontwerp wat in die bestaande literatuur gevind word.

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LIST OF ABBREVIATIONS

2-D	Two-dimensional
3-D	Three-dimensional
3-G	Third generation
3M	Third metal
AC	Alternating current
ADE	Analog Design Environment
AMS	Austriamicrosystems
BiCMOS	Bipolar complementary metal-oxide semiconductor
BJT	Bipolar junction transistor
CAD	Computer-aided design
CDMA	Code division multiple access
CMOS	Complementary metal-oxide semiconductor
CIF	Caltech intermediate form
DAT	Distributed active transformer
DC	Direct current
DRC	Design rules check
DSSS	Direct sequence spread spectrum
EDA	Electronic design automation
EM	Electromagnetic
GaAs	Gallium-arsenide
GDS	Graphic Data System
GUI	Graphical user interface
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility-transistor
HIT-Kit	High Performance Interface Tool Kit
HS	High speed
HV	High voltage
IBM	International Business Machines
ISI	Institute for Scientific Information
ISM	Industrial, Scientific and Medical
LF	Low frequency
LNA	Low-noise amplifier

LVS	Layout versus schematic
MEMS	Microelectro-mechanical system
MEP	MOSIS Education Programme
MESFET	Metal-semiconductor field-effect transistor
MOSFET	Metal-oxide semiconductor field-effect transistor
MOSIS	Metal Oxide Semiconductor Implementation Service
MPW	Multi-purpose wafer
NDA	Non-disclosure agreement
NMOS	n-channel MOS
PA	Power amplifier
PAE	Power added efficiency
PCB	Printed circuit board
PDA	Personal data assistant
PEEC	Partial Element Equivalent Circuit
pHEMT	Pseudomorphic HEMT
PMOS	p-channel MOS
PWM	Pulse-width modulated
Q-factor, Q	Quality factor
QFN	Quad flat no-lead
RF	Radio frequency
RFC	Radio-frequency choke
RFIC	Radio-frequency integrated circuit
RFID	Radio-frequency identification
Si	Silicon
SiGe	Silicon-germanium
SMA	SubMiniature version A
SPICE	Simulation program with integrated-circuit emphasis
THD	Total harmonic distortion
TM	Thick metal
VBIC	Vertical Bipolar Inter-Company
VCO	Voltage-controlled oscillator
WLAN	Wireless local area network

TABLE OF CONTENTS

CHAPTER 1	INTRODUCTION.....	1
1.1	BACKGROUND TO THE RESEARCH	1
1.2	RESEARCH PROBLEM AND HYPOTHESIS.....	3
1.3	JUSTIFICATION FOR THE RESEARCH	4
1.4	METHODOLOGY	4
1.5	DEFINITIONS.....	4
1.6	DELIMITATIONS OF SCOPE AND KEY ASSUMPTIONS	5
1.7	CONTRIBUTION OF THE RESEARCH.....	5
1.8	PUBLICATIONS LEADING FROM THIS RESEARCH.....	9
1.9	OUTLINE OF THIS THESIS.....	10
1.10	CONCLUSION	11
CHAPTER 2	LITERATURE REVIEW.....	12
2.1	INTRODUCTION	12
2.2	POWER AMPLIFICATION	12
2.2.1	Power capability	13
2.2.2	Power consumption	13
2.2.3	Power efficiency	14
2.2.4	Matching for desired power.....	15
2.2.5	Classification of PAs	16
2.2.6	Techniques for performance improvement of PAs.....	27
2.2.7	Temperature aspects of PAs	27
2.2.8	Biasing	28
2.3	INDUCTORS FOR POWER AMPLIFIER IMPLEMENTATIONS.....	29
2.3.1	Inductor implementation options.....	30
2.3.2	Spiral inductors on silicon and SiGe	36
2.4	TECHNOLOGIES FOR POWER AMPLIFIER INTEGRATION	50
2.5	RAPID POWER AMPLIFIER DESIGN AND AUTOMATION	52
2.5.1	The need for rapid PA design.....	52
2.5.2	Automating the rapid PA design	53
2.6	CONCLUSION.....	53
CHAPTER 3	METHODOLOGY.....	55
3.1	INTRODUCTION	55



3.2	RESEARCH METHODOLOGY OUTLINE	55
3.3	THE IC PROCESS	56
3.4	CONCEPTUAL DESIGN AND ALGORITHM DEVELOPMENT	57
3.5	MODELLING, SIMULATION, AND LAYOUT DESIGN	57
3.5.1	Modelling and simulation.....	57
3.5.2	Layout design and verification	58
3.5.3	EM simulation	58
3.5.4	SPICE model of the HBT	58
3.6	MEASUREMENT SETUP AND EQUIPMENT	59
3.7	CONCLUSION.....	59
CHAPTER 4	SYSTEM LEVEL DESIGN ROUTINE.....	61
4.1	INTRODUCTION	61
4.2	METHOD FOR DESIGNING THE CLASS-E POWER AMPLIFIERS	61
4.2.1	Input parameters	62
4.2.2	Subroutine outputs.....	63
4.2.3	Description and flow diagram of the Class-E subroutine.....	64
4.3	METHOD FOR DESIGNING THE CLASS-F POWER AMPLIFIERS.....	65
4.3.1	Input parameters	66
4.3.2	Subroutine outputs.....	68
4.3.3	Description and flow diagram of the Class-F subroutine	68
4.4	METHOD FOR OUTPUT MATCHING	70
4.4.1	Input parameters	70
4.4.2	Subroutine outputs.....	70
4.4.3	Description of the matching network subroutine	70
4.5	METHOD FOR DESIGNING SPIRAL INDUCTORS	74
4.5.1	Input parameters	75
4.5.2	Subroutine outputs.....	77
4.5.3	Description and flow diagrams of inductor design subroutine.....	78
4.6	MATCHING AND BIASING AT THE INPUT SIDE OF THE POWER AMPLIFIER	80
4.7	COMPLETE SYSTEM INTEGRATION	83
4.7.1	Input parameters	83
4.7.2	Routine outputs.....	83
4.7.3	Description and flow diagram of the PA design routine	84



4.8	CONCLUSION.....	86
CHAPTER 5	FULL CIRCUIT DESIGN AND SIMULATION.....	88
5.1	INTRODUCTION	88
5.2	VERIFICATION OF THE SPIRAL INDUCTOR MODEL AND THE INDUCTANCE SEARCH ALGORITHM	88
5.3	VERIFICATION OF THE FULL SYSTEM INTEGRATION ROUTINE	97
5.3.1	Lower power Class-E configuration.....	97
5.3.2	Higher power Class-E configuration	103
5.3.3	Lower power Class-F configuration	109
5.3.4	Higher power Class-F configuration	114
5.3.5	Choice of better Class-E and Class-F configuration	120
5.4	FURTHER DESIGN OF THE CLASS-E AMPLIFIER	121
5.5	FURTHER DESIGN OF THE CLASS-F AMPLIFIER.....	125
5.6	CONCLUSION.....	129
CHAPTER 6	LAYOUT, FABRICATION AND MEASUREMENT RESULTS	130
6.1	INTRODUCTION	130
6.1.1	Inductor measurements.....	130
6.2	FULL SYSTEM INTEGRATION MEASUREMENTS	131
6.2.1	Circuit layouts	131
6.2.2	Packaging	134
6.2.3	Package simulations	135
6.2.4	The PCB design.....	137
6.2.5	Measurement results	138
6.3	CONCLUSION.....	140
CHAPTER 7	CONCLUSIONS AND IMPLICATIONS.....	142
7.1	INTRODUCTION	142
7.2	CONCLUSIONS ABOUT THE RESEARCH PROBLEM	142
7.3	IMPLICATIONS FOR THE THEORY	144
7.4	IMPLICATIONS FOR FUTURE RESEARCH.....	145
REFERENCES	147	
APPENDIX A	MATLAB CODE.....	160
A.1	INTRODUCTION	160
A.2	MAIN PA DESIGN PROGRAM	160
A.3	CLASS-E DESIGN SUBROUTINE	162



A.4	CLASS-F DESIGN SUBROUTINE	164
A.5	IMPEDANCE MATCHING.....	165
A.6	INDUCTANCE VALUE OVERRIDE.....	167
A.7	SETUP OF INDUCTANCE SEARCH ALGORITHM PARAMETERS	169
A.8	SEARCH FOR REQUIRED INDUCTORS.....	169
A.9	PA NETLIST EXPORT.....	172
A.10	ENTERING PROCESS PARAMETERS	175
A.11	INDUCTANCE SEARCH ALGORITHM	177
A.12	EXPORT OF THE SPIRAL INDUCTOR SUBCIRCUIT	178
A.13	EXPORT OF THE PART OF NETLIST INVOLVING MATCHING	178
A.14	CALCULATING PARASITICS OF ANY DESIGNED SPIRAL INDUCTOR 179	
A.15	DESIGN OF SPIRAL INDUCTORS AS A MAIN ROUTINE	180
A.16	DESIGN OF INDUCTORS WITH KNOWN GEOMETRY	181
A.17	EXPORT OF THE STAND-ALONE NETLIST OF A SPIRAL INDUCTOR 183	
A.18	EXTRACTION OF INDUCTOR LAYOUT INTO A CIF FILE.....	183
A.19	EXTRACTION OF INDUCTOR LAYOUT INTO A GDSII FILE.....	186
A.20	MATCHING AS A MAIN ROUTINE	186
APPENDIX B	PROCESS FILES FOR EM SIMULATIONS.....	187
B.1	INTRODUCTION	187
B.2	PROCESS FILE FOR 3M AMS S35 TECHNOLOGY	187
B.3	PROCESS FILE FOR TM AMS S35 TECHNOLOGY.....	188
APPENDIX C	DESIGN METHOD – BE AT UP (PTY) LTD	190