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DESIGN METHODS FOR INTEGRATED SWITCHING-MODE POWER AMPLIFIERS

by

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SUMMARY

DESIGN METHODS FOR INTEGRATED SWITCHING-MODE POWER AMPLIFIERS

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Keywords: Power amplifier, spiral inductor, switch-mode amplifier, Class-E amplifier, Class-F amplifier, impedance matching, streamlined design, SPICE netlist, BiCMOS, 0.35 µm process, 180 nm process, software routine.

While a lot of time and resources have been placed into transceiver design, due to the pace of a conventional engineering design process, the design of a power amplifier is often completed using scattered resources; and not always in a methodological manner, and frequently even by an iterative trial and error process.

In this thesis, a research question is posed which enables for the investigation of the possibility of streamlining the design flow for power amplifiers. After thorough theoretical investigation of existing power amplifier design methods and modelling, inductors inevitably used in power amplifier design were identified as a major drawback to efficient design, even when examples of inductors are packaged in design HIT-Kits. The main contribution of this research is engineering of an inductor design process, which in-effect contributes towards enhancing conventional power amplifiers. This inductance search algorithm finds the highest quality factor configuration of a single-layer square spiral inductor within certain tolerance using formulae for inductance and inductor parasitics of traditional single-π inductor model. Further contribution of this research is a set of algorithms for the complete design of switch-mode (Class-E and Class-F) power amplifiers and their output matching networks. These algorithms make use of classic deterministic design equations so that values of parasitic components can be calculated given input parameters, including required output power, centre frequency, supply voltage, and choice of class of operation.

The hypothesis was satisfied for SiGe BiCMOS S35 process from Austriamicrosystems (AMS). Several metal-3 and thick-metal inductors were designed using the abovementioned algorithm and compared with experimental results provided by AMS. Correspondence was established between designed, experimental and EM simulation results, enabling qualification of inductors other than those with experimental results

available from AMS by means of EM simulations with average relative errors of 3.7 % for inductance and 21 % for the Q factor at its peak frequency. For a wide range of inductors, Q-factors of 10 and more were readily experienced. Furthermore, simulations were performed for number of Class-E and Class-F amplifier configurations with HBTs with f_t greater than 60 GHz and total emitter area of 96 μm^2 as driving transistors to complete the hypothesis testing. For the complete PA system design (including inductors), simulations showed that switch-mode power amplifiers for 50 Ω load at 2.4 GHz centre frequency can be designed using the streamlined method of this research for the output power of about 6 dB less than aimed. This power loss was expected, since it can be attributed to non-ideal properties of the driving transistor and Q-factor limitations of the integrated inductors, assumptions which the computations of the routine were based on. Although these results were obtained for a single micro-process, it was further speculated that outcome of this research has a general contribution, since streamlined method can be used with a much wider range of CMOS and BiCMOS processes, when low-gigahertz operating power amplifiers are needed. This theory was confirmed by means of simulation and fabrication in 180 nm BiCMOS process from IBM, results of which were also presented. The work presented here, was combined with algorithms for SPICE netlist extraction and the spiral inductor layout extraction (CIF and GDSII formats). This secondary research outcome further contributed to the completeness of the design flow.

All the above features showed that the routine developed here is substantially better than cut-and-try methods for design of power amplifiers found in the existing body of knowledge.

OPSOMMING

ONWERPMETODES VIR GEÏNTEGREERDE SKAKELMODUS-DRYWINGSVERSTERKERS

deur

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Sleutelwoorde: Drywingsversterker, spiraalinduktor, skakelmodusversterker, Klas-E versterker, Klas-F versterker, impedansieaanpassing, geoptimeerde ontwerp, SPICE-netlys, BiCMOS, 0.35 µm-proses, 180 nm-proses, sagtewareroetine

Alhoewel baie tyd en hulpbronne spandeer word op die ontwerp van sender/ontvangers, word die onwerp van drywingsversterkers dikwels voltooi met verspreide hulpbronne as gevolg van die tempo van die konvensionele ingenieursontwerpsproses en ook nie altyd op ’n metodiese manier nie, wat daartoe lei dat dit soms ’n iteratiewe proses raak.

In hierdie tesis word ’n navorsingsvraag gevra wat lei tot die ondersoek van die moontlikheid om die ontwerpsvloei van drywingsversterkers te optimeer. Na ’n sorgvuldige ondersoek van bestaande drywingsversterkerontwerpmetodes en modellering is die noodwendige gebruik van induktors geïdentifiseer as een van die groot struikelblokke in doeltreffende ontwerp, selfs wanneer induktorvoorbeelde deel vorm van die hoëprestasie-koppelvlakpakket (HIT-kit). Die grootste bydra van hierdie navorsing is die formulering van ’n ontwerpproses vir induktors, wat dan ook bydra tot die verbetering van konvensionele drywingsversterkers. Hierdie soekalgoritme vind die uitleg van ’n enkellaag- reghoekige spiraalinduktor met die hoogste kwaliteitfaktor binne sekere toleransies deur die formules vir die induktansie- en induktor- parasitiese komponente van die tradisionele enkel-π-induktormodel te gebruik. ’n Verdere bydrae van die navorsing is ’n stel algoritmes vir die volledige ontwerp van skakelmodus- (Klas-E en Klas-F) drywingsversterkers sowel as uitset-aanpasnetwerke. Hierdie algoritmes maak gebruik van die klassieke deterministiese ontwerpsvergelykings sodat die waardes van die parasitiese komponente bereken kan word vir gegewe insetparameters, wat die vereiste uitsetdrywing, werksfrekwensie, toevoerspanning en keuse van versterkerklas insluit.

Die hipotese is bewys in ’n SiGe BiCMOS S35-proses van Austriamicrosystems (AMS). Verskeie drie-metaal en dikmetaal-induktors is ontwerp deur bogenoemde algoritmes te gebruik en is vergelyk met die eksperimentele resultate wat deur AMS voorsien is.

Ooreenstemming is gevind tussen die ontwerps-, eksperimentele en elektromagnetiese simulasieresultate, wat die kwalifikasie van induktors, anders as dié waarvoor eksperimentele resultate van AMS beskikbaar is, moontlik maak deur die gebruik van EM-simulasies met ’n gemiddelde fout van 3.7 % vir die induktansie en 21 % vir die kwaliteitfaktor by die piekfrekwensie. Vir ’n wye verskeidenheid induktors is kwaliteitfaktors van 10 of meer gevind. Verder is simulasies gedoen vir ’n aantal Klas-E en Klas-F versterkerkonfigurasies met hetero-voegvlaktransistors met f_T groter as 60 GHz en ’n totale emitterarea van 96 μm^2 as drywingstransistor om die hipotesetoetsing te voltooi. Vir die drywingsversterkerstelselontwerp (wat induktors insluit) het simulasies gewys dat skakelmodusdrywingsversterkers vir ’n 50 Ω las by ’n 2.4 GHz-werksfrekwensie ontwerp kan word deur die geoptimeerde metode in hierdie navorsing te gebruik, in welke geval die uitsetdrywing ongeveer 6 dB minder is as waarvoor ontwerp is. Hierdie drywingsverlies is verwag, aangesien dit toegeskryf kan word aan die nie-ideale eienskappe van die drywingstransistor en die kwaliteitfaktorbeperkings van die geïntegreerde induktors, sowel as die aannames wat gemaak is in die berekeninge in die ontwerpproses. Alhoewel hierdie resultate vir ’n enkele mikroproses verkry is, is gevind dat hierdie navorsingsuitset steeds ’n algemene bydrae is deurdat die proses gebruik kan word vir ’n verskeidenheid CMOS- en BiCMOS-prosesse, wanneer laegigahertz-drywingsversterkers vereis word. Hierdie teorie is bevestig deur middel van simulasie en vervaardiging in die 180-nm BICMOS-proses van IBM, waarvan die resultate ook voorgelê is. Die werk wat hier aangebied word, is gekombineerd met algoritmes wat SPICE netlyste formuleer en ook die spiraalinduktoruitleg skryf in die CIF- en GDSII-formate.

Al bogenoemde kenmerke wys dat die roetine wat geformuleer is, aansienlik beter is as lukrake iteratiewe metodes vir drywingsversterkerontwerp wat in die bestaande literatuur gevind word.

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LIST OF ABBREVIATIONS

2-D	Two-dimensional
3-D	Three-dimensional
3-G	Third generation
3M	Third metal
AC	Alternating current
ADE	Analog Design Environment
AMS	Austriamicrosystems
BiCMOS	Bipolar complementary metal-oxide semiconductor
BJT	Bipolar junction transistor
CAD	Computer-aided design
CDMA	Code divison multiple access
CMOS	Complementary metal-oxide semiconductor
CIF	Caltech intermediate form
DAT	Distributed active transformer
DC	Direct current
DRC	Design rules check
DSSS	Direct sequence spread spectrum
EDA	Electronic design automation
EM	Electromagnetic
GaAs	Gallium-arsenide
GDS	Graphic Data System
GUI	Graphical user interface
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility-transistor
HIT-Kit	High Performance Interface Tool Kit
HS	High speed
HV	High voltage
IBM	International Business Machines
ISI	Institute for Scientific Information
ISM	Industrial, Scientific and Medical
LF	Low frequency
LNA	Low-noise amplifier

LVS	Layout versus schematic
MEMS	Microelectro-mechanical system
MEP	MOSIS Education Programme
MESFET	Metal-semiconductor field-effect transistor
MOSFET	Metal-oxide semiconductor field-effect transistor
MOSIS	Metal Oxide Semiconductor Implementation Service
MPW	Multi-purpose wafer
NDA	Non-disclosure agreement
NMOS	n-channel MOS
PA	Power amplifier
PAE	Power added efficiency
PCB	Printed circuit board
PDA	Personal data assistant
PEEC	Partial Element Equivalent Circuit
pHEMT	Pseudomorphic HEMT
PMOS	p-channel MOS
PWM	Pulse-width modulated
Q-factor, Q	Quality factor
QFN	Quad flat no-lead
RF	Radio frequency
RFC	Radio-frequency choke
RFIC	Radio-frequency integrated circuit
RFID	Radio-frequency identification
Si	Silicon
SiGe	Silicon-germanium
SMA	SubMiniature version A
SPICE	Simulation program with integrated-circuit emphasis
THD	Total harmonic distortion
TM	Thick metal
VBIC	Vertical Bipolar Inter-Company
VCO	Voltage-controlled oscillator
WLAN	Wireless local area network

TABLE OF CONTENTS