A 4.3 GHz BiCMOS VCO with multiple 360° variable phase outputs using the vector sum method

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Received: 13 September 2011 **Accepted:** 24 May 2012 **Published online:** 9 June 2012

Abstract
A 4.3 GHz voltage controlled oscillator (VCO) with multiple independently tunable phase outputs is presented. The VCO is realized by coupling two LC oscillators together in order to obtain quadrature signals and is tunable between 4.12 and 4.74 GHz. The variable phase outputs are achieved by varying the amplitudes of the in-phase and quadrature signals independently and then combining these signals together. By using multiple Gilbert cells as variable gain amplifiers (VGAs), multiple tunable phase outputs are achieved with the use of only one quadrature VCO. The VGAs are controlled using a custom non-linear digital-to-analog converter. The entire circuit is designed using a 3.3 V SiGe BiCMOS process. A maximum phase noise of −108.17 dBc/Hz was measured over the entire tuning range at a 1 MHz offset. The outputs of the VCO can be used as local oscillators that achieve phase shifting during radio frequency up or down conversion.

Keywords BiCMOS – Integrated circuit – Phased array antenna – Quadrature VCO – Variable gain amplifier – Vector sum

Abbreviations *VCO*
Voltage controlled oscillator
- *VGA*
Variable gain amplifier
- *DAC*
Digital-to-analog converter
- *RF*
Radio frequency
- *TL*
Transmission line
- *P-I-N*
Positive-Intrinsic-Negative
- *MEMS*

MicroElectroMechanical Systems
- *PA*
Power amplifier
- *LO*
Local oscillator
- *IC*
Integrated circuit
- *FOM*
Figure-of-merit

1 Introduction

Phased array antennas realize the potential of modern wireless communication systems to radiate energy more efficiently. This is due to the fact that a large portion of the radiated energy could be directed towards the receiver. This directional nature of an antenna structure is generally referred to as antenna gain. Apart from the phased array antenna, other types of antennas that also achieve directionality also exist, such as a satellite dish. However, the phased array antenna requires no mechanical movement to change its power pattern as this is determined by the amount of phase delay between the different antenna elements.

This attractive feature makes phased array antennas highly suitable for future portable wireless devices, where the trend is towards operation at much shorter wavelengths, which would result in much smaller antenna structures. This is due to the spacing required between adjacent antenna elements being proportional to the wavelength. One of the key components required by this type of antenna system would undoubtedly be the phase shifter.

A popular method of introducing phase shift is with the aid of transmission lines (TLs). By manipulating the characteristics of the TL, the angle of the phase shift can be controlled. For example, ferrite phase shifters [*1*] allow a variation in the phase shift due to the dependence of its magnetic properties on the current flowing through a bias wire. Positive-Intrinsic-Negative (P-I-N) diode phase shifters allow electronic switching between different lengths of TL and some MicroElectroMechanical Systems (MEMS) phase shifters operate on the same principle but instead use electromechanical switching.

In the past decade, work has been done on phase shifters that obtain phase shifting through the vector sum of orthogonal signals [*2*–*6*]. These phase shifters can be integrated onto the same circuit as the power amplifier (PA) of most portable wireless devices. This has the benefit of saving cost as well as physical space. An added advantage is that the phased array architecture aids with the design of the integrated power amplification stage [*4*] as it would be easier to design multiple PAs that each deliver a moderate output power, as opposed to a single high PA that has to deliver the same equivalent output power.

This paper presents the design of a solid-state phase shifter that is implemented at the local oscillator (LO) and has been integrated using a 0.35 μm SiGe BiCMOS process. The paper is organized as follows: Sect. 2 gives a general outline of the vector sum method; Sects. 3–5 discuss the design of the voltage controlled oscillator (VCO), phase shifter and the digital phase tuner respectively. Section 6 discusses the experimental results and Sect. 7 concludes this paper.

2 Vector sum phase shifting

Vector sum phase shifting is achieved by adding two out-of-phase signals (mostly by a quarter of a cycle) together as illustrated in Fig. 1. When the amplitudes of both signals are varied independently the phase will vary. For quadrature signals the resulting phase is given by

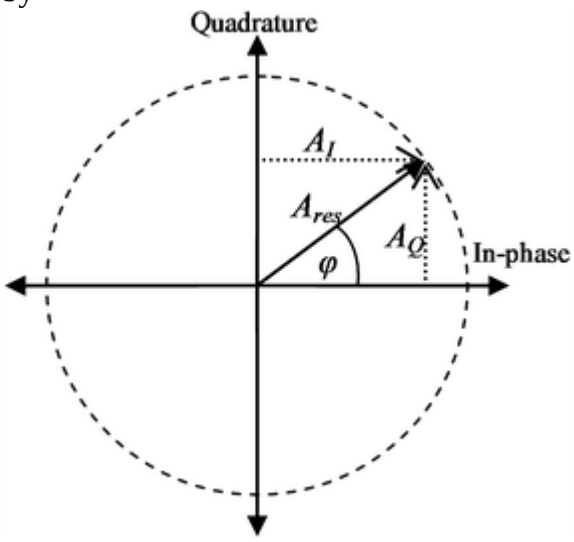

Fig. 1 Phasor representation of the vector sum method

(1)

where A_I and A_Q denote the amplitudes of the in-phase and quadrature signals respectively. The resulting amplitude is then given by

(2)

The resulting amplitude will vary by a factor of should only one of the signals be changed to obtain phase shifting. For the required amplitude to remain constant throughout the phase tuning, the following relations for both $A_I[V_I]$ and $A_Q[V_Q]$ should hold:

(3)

(4)

The most straightforward way to maintain these relations is to pre-program the required voltage levels for a discrete number of phases using a digital-to-analog converter (DAC) [2]. Such an approach also addresses the effect of the non-linear gain introduced by the variable gain amplifier (VGA).

In general, phase shifting is applied directly on the incoming or outgoing radio frequency (RF) signal using a phase delay element. These phase shifters are therefore placed quite close to the antennas and operate at high power levels when transmitting. The vector sum phase

shifter presented achieves phase shift at the LO. The phase shift then propagates through to the modulated signal that is transmitted [3]. This concept is clarified in Fig. 2. A similar approach can also be taken at the receiver side, whereby the phase shift is applied to the LO being used for RF down conversion.

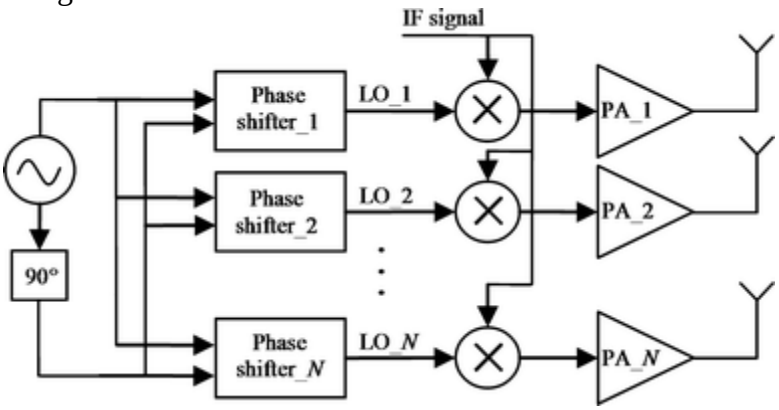

Fig. 2 Possible implementation of the vector sum phase shifter

It is reported that the rotary field ferrite phase shifter has the highest power handling capability by far but is the bulkiest and relatively more expensive when compared with other phase shifters [7]. The presented integrated vector sum phase shifter provides a low cost, small size alternative at the expense of power handling capability.

3 VCO design

The VCO schematic is shown in Fig. 3 and is realized using an LC oscillator that was adapted from [8]. Two identical VCOs are coupled together to obtain the in-phase and quadrature signals. It was found that by biasing the bases of Q_1–Q_4 using diodes D_1–D_8, phase noise improved considerably due to the reduction in the number of thermal noise sources. The purpose of diodes D_{13}–D_{16} is to lower the V_{CE} of Q_{10}–Q_{15} which must be smaller than 2 V to avoid reverse breakdown.

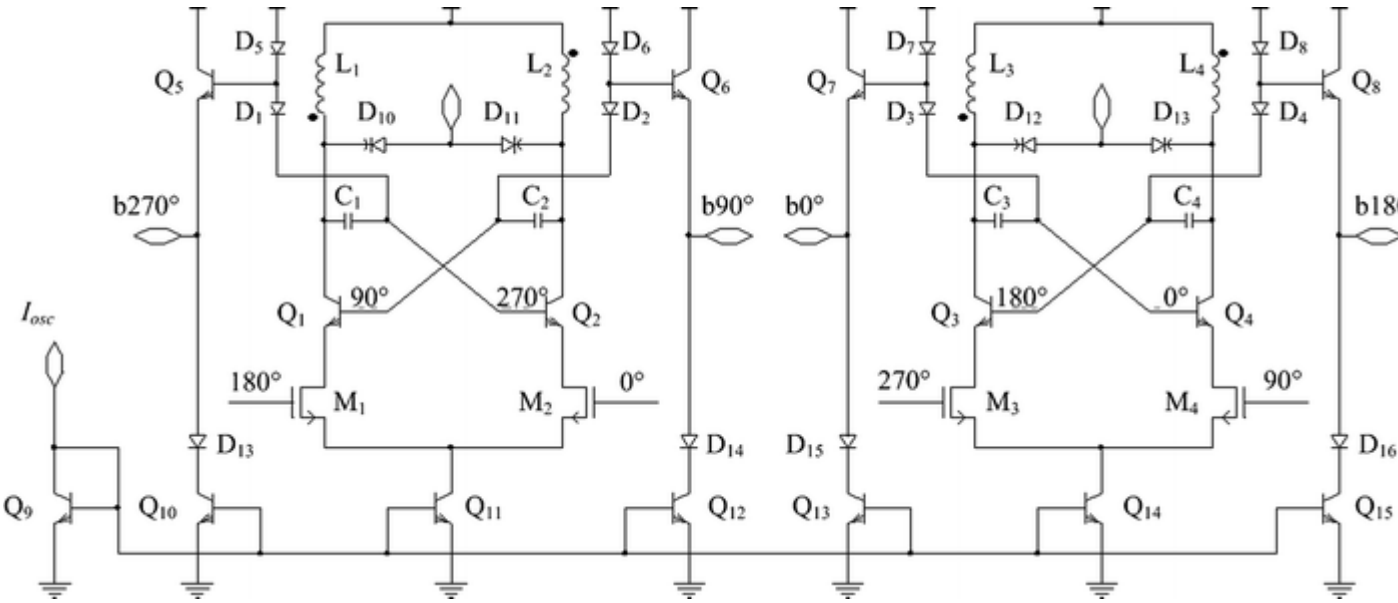

Fig. 3 Circuit *diagram* of the quadrature *LC*-VCO implementation

The NMOS coupling transistors M_1–M_4 should be designed so that their transconductances are about the same as that of the bipolar transistors [8] and their widths are therefore given by

(5)

where L = 0.35 μm, E_c = 3.85 MV/m, V_{GS} = 2 V, C_{ox} = 454 nF/cm^2, V_{TH} = 0.5 V, $v_{scl} \approx 10^7$ cm/s, I_C is the collector current of each of the transistors Q_1–Q_4 in Fig. 3, V_T is the thermal voltage at room temperature and W is measured in m.

Inductors L_1–L_2 and L_3–L_4 were implemented on-chip using two differential spiral inductors provided by the Austriamicrosystems (AMS) foundry which both have a quality factor (Q) of 11 at 10.5 GHz and consume an area of 216 × 216 μm^2 [9]. Junction varactors also provided by the AMS foundry were used for tuning. These varactors have a 32 % tuning range and a Q_{min} of 25 at 5 GHz.

The phase noise was optimized using SpectreRF by sweeping the collector currents of Q_{11} and Q_{14} at 4.55 GHz and plotting the phase noise at a 1 MHz offset as shown in Fig. 4.

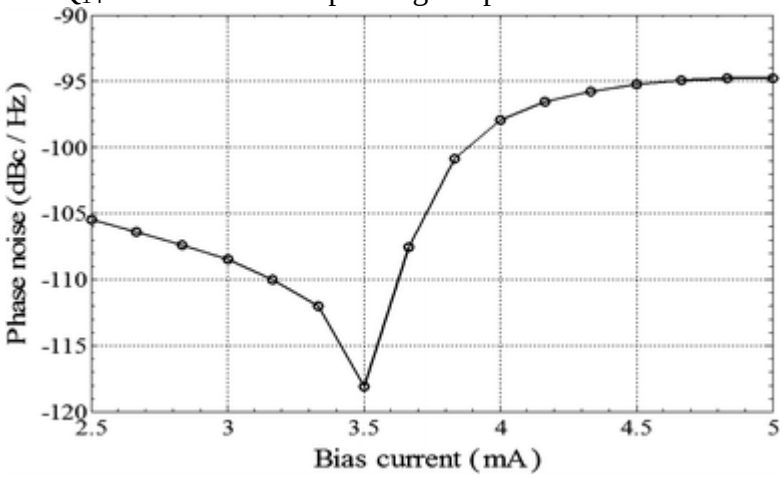

Fig. 4 Simulated phase noise over bias current at a 1 MHz offset

4 Phase shifter design

Phase shifting of the VCO outputs is achieved by using a VGA based on a Gilbert cell and its schematic is shown in Fig. 5 [10]. The RF signal generated by the oscillator is applied at V_{2+} and V_{2-} and the gain is varied using V_{1+} and V_{1-}. Resistors R_3–R_6 = 180 Ω and were added to the mixer cell in order to expand its dynamic range [11]. This was done to allow more precise control over the phase shift. The values of these resistors were designed by plotting the differential output current versus the control voltage over a range of values as shown in Fig. 6.

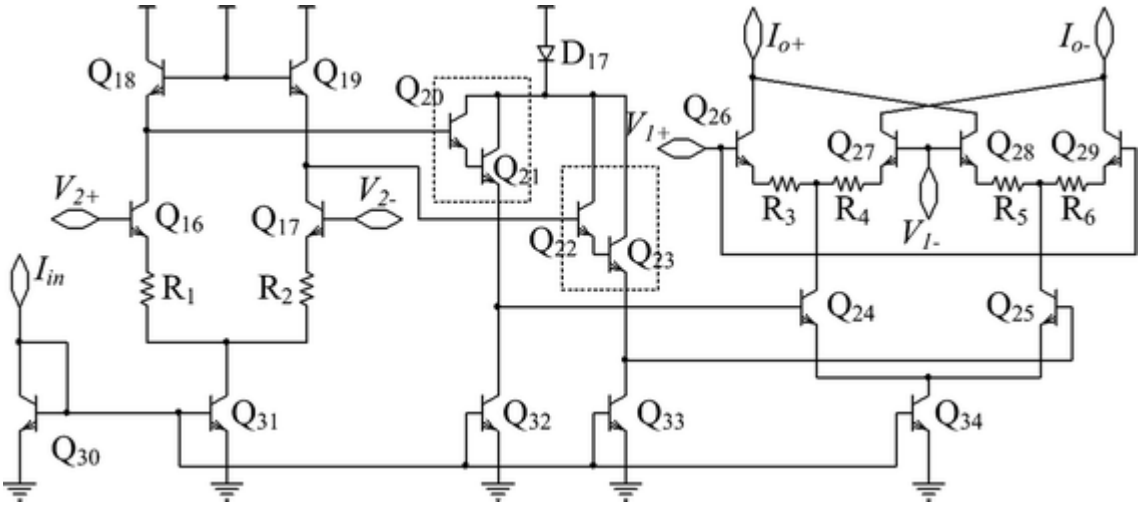

Fig. 5 Gilbert mixer implementation

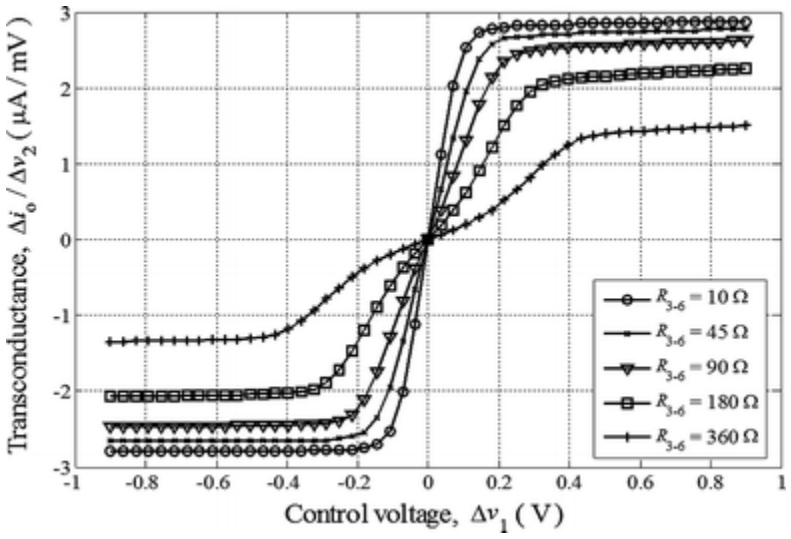

Fig. 6 Simulated transfer *curve* of the Gilbert mixer illustrating the effect of varying R_{3-6}

The current outputs of the two VGAs are combined and passed through a differential-to-single-ended converter. The converter consists of a PMOS current mirror since this particular process does not provide high quality PNP transistors. The block diagram of the phase shifter is shown in Fig. 7.

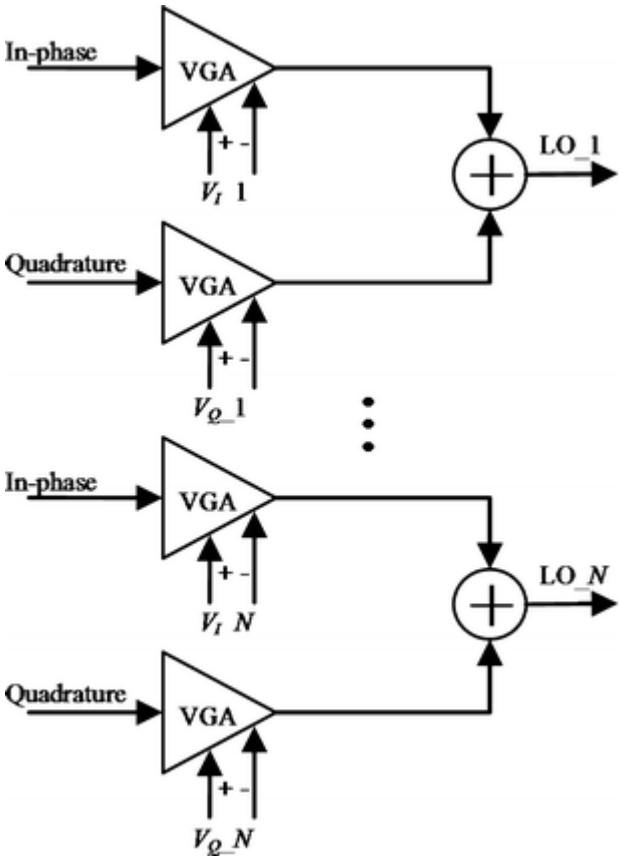

Fig. 7 Block *diagram* of the phase shifter

5 Digital phase tuner

A digital phase tuner was designed to provide an interface that allows a discrete number of pre-defined phase shifts. Due to the non-linear transfer characteristic of the phase control inputs, this circuit makes phase shifting a lot easier and also enables the phase shift to be controlled by a digital processor. The difficulty with analog phase tuning arises when a constant amplitude over the entire phase tuning range is desired as shown by Eqs. (1) and (2). The digital phase tuner was designed to enable discrete tuning between 16 different phases equally spaced between 0° and 360°. A block diagram of the digital phase tuner is shown in Fig. 8 and it consists of a decoder circuitry and two DACs. In order to obtain 16 different equally spaced phases with equal amplitudes, eight different voltage levels for both V_Q and V_I are needed. The values for these voltage levels were obtained by first using Eqs. (3) and (4) to find the amplitudes for the in-phase and quadrature currents and then using Fig. 6 to read off the voltages.

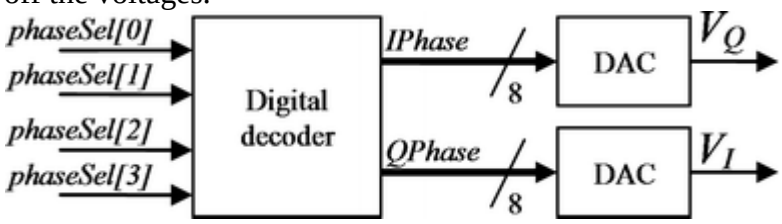

Fig. 8 Functional block *diagram* of the digital phase tuner

Figure 9 shows a circuit diagram of the DAC that was designed to deliver the eight different voltage levels required at V_Q and V_I to achieve equally spaced phases. The amount of current flowing through R_9 is controlled by switching the independently scaled gates of M_{17}–M_{25} between 0 V and $V_{BE(on)}$. V_{1+} is then determined by the voltage drop over R_9. The digital decoder of Fig. 8 was designed using VHDL and selects the gates to be turned on in order to obtain a specific output voltage at V_{1+}.

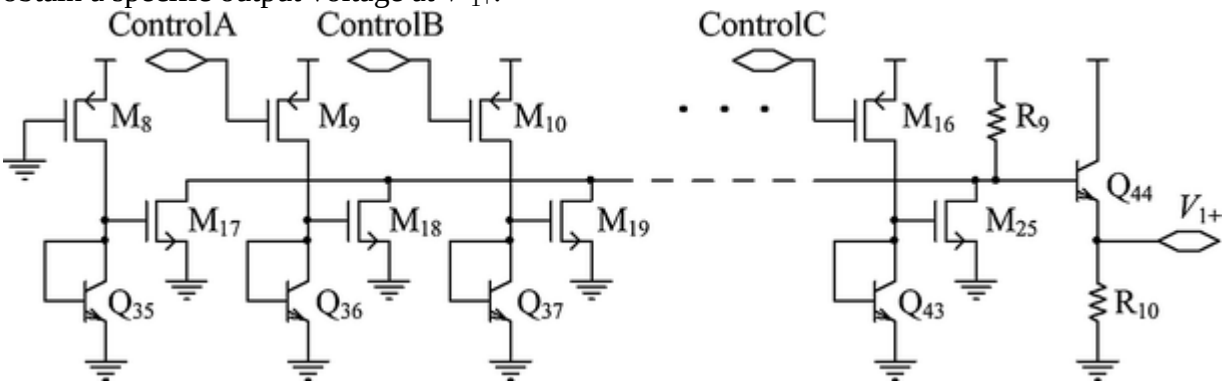

Fig. 9 Circuit *diagram* of the DAC used in the digital phase tuner

6 Experimental results

The integrated circuit (IC) was fabricated using a four metal (thick metal 4) 3.3 V 0.35 µm SiGe BiCMOS process from AMS. The foundry provides a number of on-chip spiral inductors ranging from 1 to 20 nH which are characterized up to 6 GHz for the larger inductors and 12 GHz for the smaller ones [9]. This also includes a number of differential inductors.

Figure 10(a) shows a chip photograph of the VCO with four phase shifters and Fig. 10(b) shows a photograph of the digital phase tuner. The VCO along with four phase shifters occupies an area of 1.10 × 0.85 mm^2 and the digital phase tuner an area of 0.41 × 0.13 mm^2. The two circuits were connected externally which allows the phase shifters to be measured using external analog input signals at V_{1+} of the Gilbert mixer in Fig. 5. The full layout included two digital phase tuners in order to enable a relative comparison between phase variations.

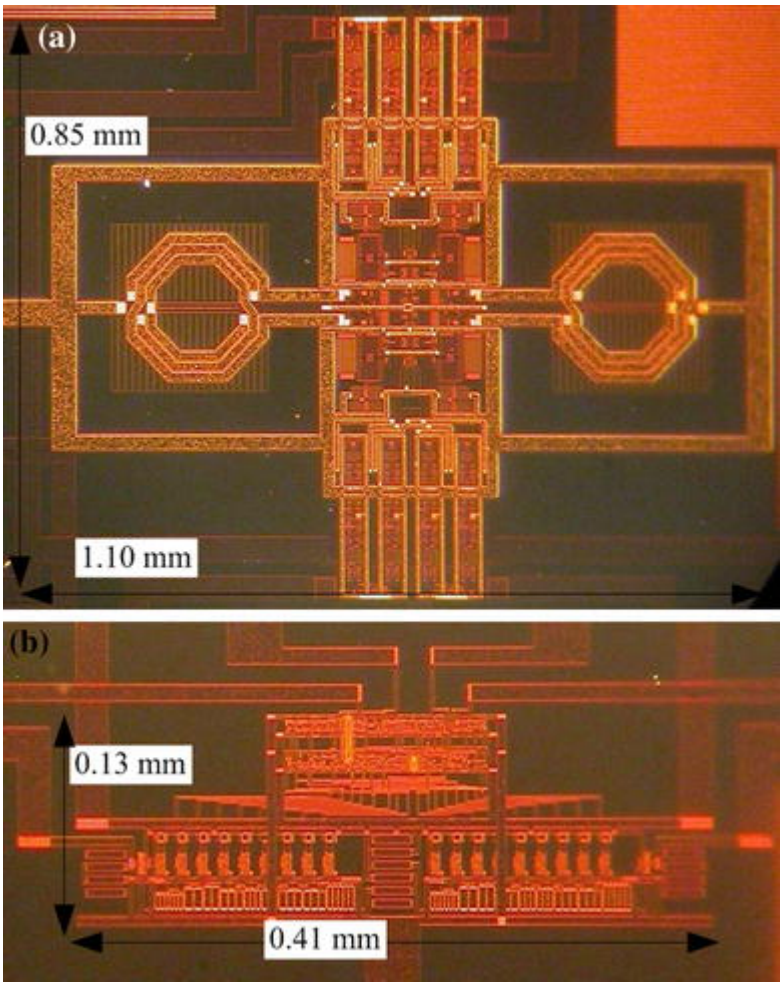

Fig. 10 *Photographs* of **a** the complete oscillator and **b** a digital phase tuner

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The quadrature *LC*-VCO was measured using an Agilent HP 8563E Spectrum Analyzer. Figure 11 shows the measured frequency tuning curve and Fig. 12 shows the phase noise at both 100 kHz and 1 MHz offsets. A frequency tuning range of 14 % was obtained and a maximum phase noise of −78.50 and −108.17 dBc/Hz was obtained at 100 kHz and 1 MHz offsets respectively. The quadrature VCO consumes 23.1 mW excluding its buffering circuitry and achieves a minimum VCO figure-of-merit (FOM) [12] of 157.81 dBc/Hz over the entire tuning range.

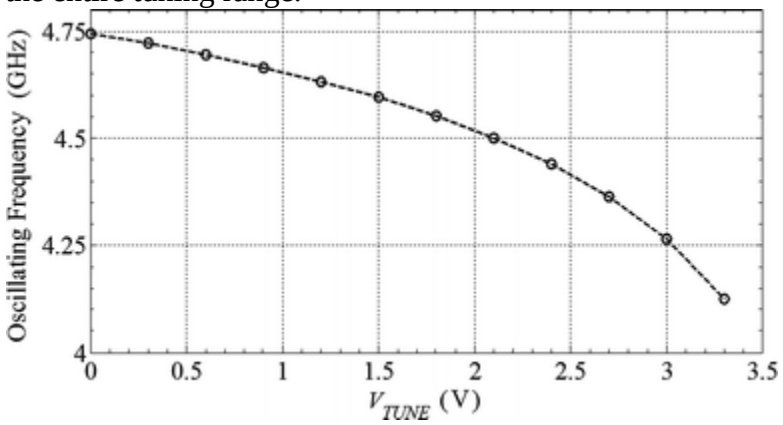

Fig. 11 Measured frequency tuning *curve* of the quadrature *LC*-VCO

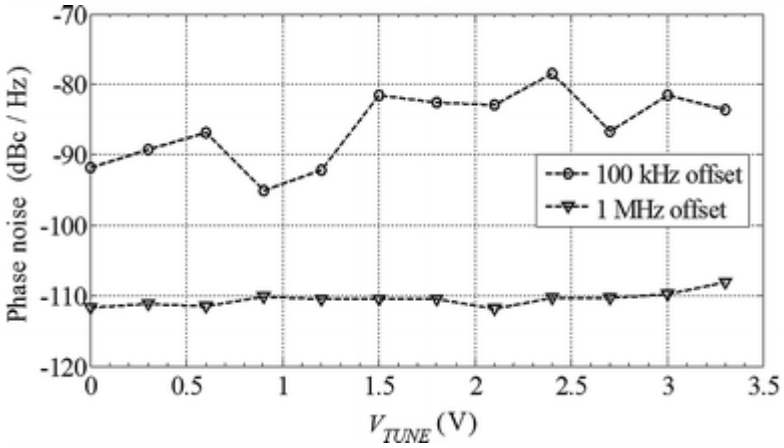

Fig. 12 Measured phase noise of the quadrature *LC*-VCO over the entire tuning range

Phase shift measurements were done using the Agilent E5071B RF Network Analyzer by forcing its input channels to scan across a 50 kHz bandwidth over the VCO carrier signal. Figure 13 shows the phase shift measurements when using the digital phase tuner described in Fig. 8 along with its expected values. These measurements were done at 4.75 GHz and show a maximum phase error of 35 %.

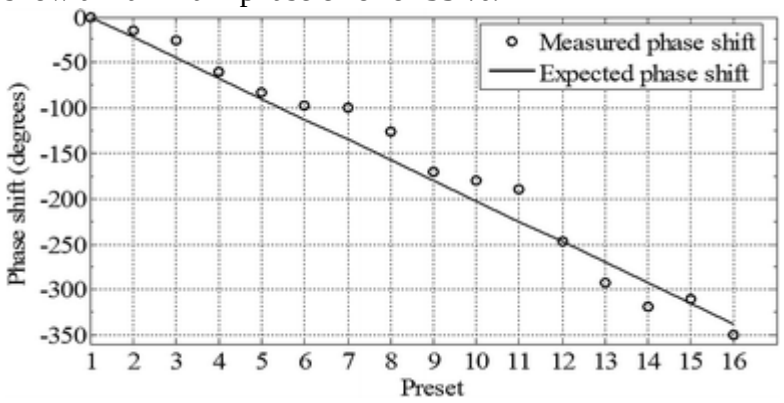

Fig. 13 Measured phase shift of the 16 different DAC presets along with its expected values

Table 1 lists a summary of the performances of the design.

Table 1 Summary of performances

Parameter	Value
VCO frequency range	4.12–4.74 GHz
VCO phase noise at 100 kHz offset	−78.50 dBc/Hz
VCO phase noise at 1 MHz offset	−108.17 dBc/Hz
VCO FOM at 100 kHz offset	−157.81 dBc/Hz
Phase shifter accuracy	<10 %
Supply voltage	3.3 V
VCO power consumption without buffer	23.1 mW

Parameter	Value
Power consumption/phase shifter	62.2 mW
Total power consumption	281 mW
Chip area—QVCO + four phase shifters	1.10×0.85 mm^2
Chip area—digital phase tuner	0.41×0.13 mm^2

7 Conclusion

This paper presented the design and measurement of a SiGe BiCMOS vector sum phase shifter at 4.3 GHz. A Gilbert mixer cell was modified by adding resistors in series with the emitters in order to increase its dynamic range. Phase noise measurements of the quadrature *LC*-VCO are comparable to that obtained in literature for similar designs [8, 12]. Phase errors from the phase shifter that are as large as 10 % would in most cases be unsuitable for a practical implementation. Even though great care was taken through simulations to ensure that phase errors were as low as possible, the shape of the graph in Fig. 6 is also frequency dependant and it would be impossible to design for all the scenarios. In future, it is suggested that the control signals to the phase shifter are adjusted using feedback from circuitry that measures the current phase difference. A negative phase error for example implies that A_{Q} should be increased whilst A_{I} is reduced. Such a proposed design would make the phase shift less sensitive to parameter variations.

Acknowledgments
The authors would like to thank Grintek Ewation (Pty) Ltd and Denel Dynamics, a division of Denel (Pty) Ltd for allowing the authors to use their calibrated measurement facilities. The authors would also like to thank Armscor S. A. Ltd and the Business Unit: Defence, Peace, Safety and Security (DPSS), Council for Scientific and Industrial Research (CSIR), South Africa for funding this project (LEDGER grant).

Conflict of interest
The authors declare that they have no conflicts of interest.

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